MGC AHB to APB Bridge (AHB2APB)

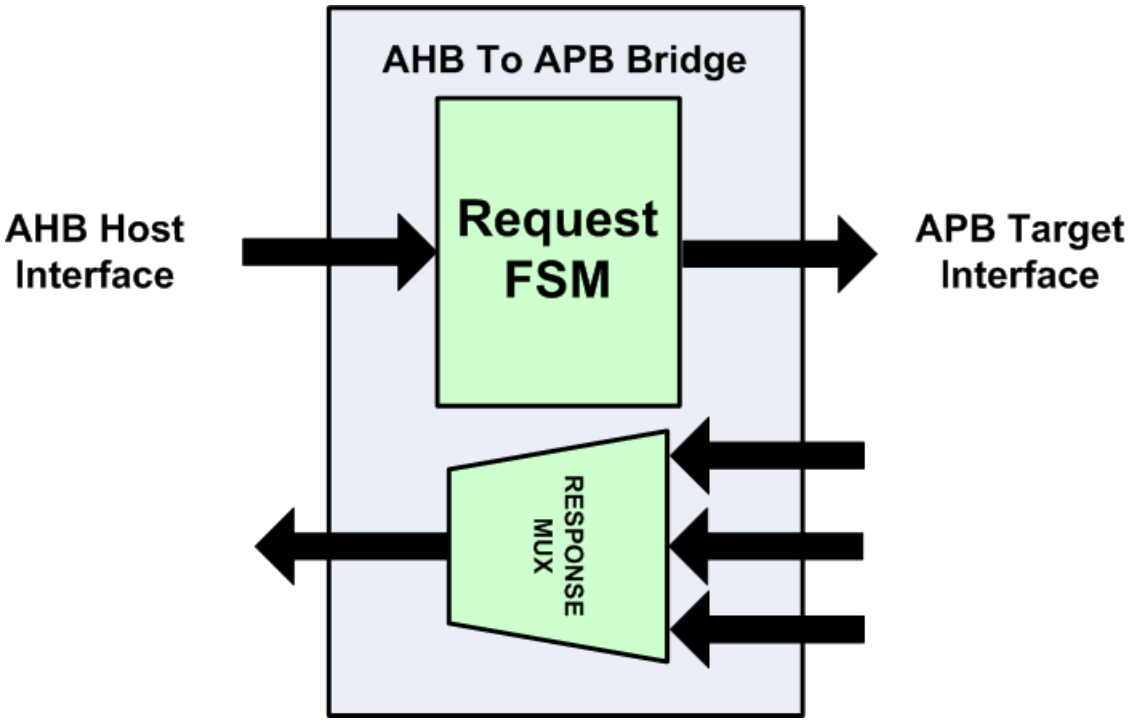
Functional Overview

The AHB to APB bridge converts host side AHB cycles to target side APB cycles. The APB side of the bridge supports up to 8 slaves and incorporates the multiplexing logic for the response path from the APB slaves to their AHB host.

The bridge does not buffer transfers and does a one to one conversion of the AHB transfers to APB cycles. AHB bursts are not directly supported, the bridge simply responds to AHB NONSEQ and SEQ transfer states and latches the necessary pipelined control signals in order to create an APB transfer.

The timing relationships between signals on both interfaces is documented in the ARM Amba specification.

The bridge has a number of parameters which are used to specify the number of APB channels and the address map for each one. Any AHB accesses to non-mapped addresses result in a null response from the bridge. The bridge contains no registers.



AHB to APB Bridge Functional block diagram

Bridge Design Parameters

Name	Type	Default	Description
NO_OF_SLAVES	int	8	Defines the number of slaves – valid range 1-8
SLAVE_START_ADDR_0	int	0	Start address for slave selected by PSEL[0]
SLAVE_END_ADDR_0	int	32'hff	End address for the slave selected by PSEL[0]
SLAVE_START_ADDR_1	int	32'h100	Start address for slave selected by PSEL[1]
SLAVE_END_ADDR_1	int	32'h1ff	End address for the slave selected by PSEL[1]
SLAVE_START_ADDR_2	int	32'h200	Start address for slave selected by PSEL[2]
SLAVE_END_ADDR_2	int	32'h2ff	End address for the slave selected by PSEL[2]
SLAVE_START_ADDR_3	int	32'h300	Start address for slave selected by PSEL[3]
SLAVE_END_ADDR_3	int	32'h3ff	End address for the slave selected by PSEL[3]
SLAVE_START_ADDR_4	int	32'h400	Start address for slave selected by PSEL[4]
SLAVE_END_ADDR_4	int	32'h4ff	End address for the slave selected by PSEL[4]
SLAVE_START_ADDR_5	int	32'h500	Start address for slave selected by PSEL[5]
SLAVE_END_ADDR_5	int	32'h5ff	End address for the slave selected by PSEL[5]
SLAVE_START_ADDR_6	int	32'h600	Start address for slave selected by PSEL[6]
SLAVE_END_ADDR_6	int	32'h6ff	End address for the slave selected by PSEL[6]
SLAVE_START_ADDR_7	int	32'h700	Start address for slave selected by PSEL[7]
SLAVE_END_ADDR_7	int	32'h7ff	End address for the slave selected by PSEL[7]

Input/Output Signal Description

Name	Width	Direction	Description
HCLK	1	Input	System clock, used by both sides of the bridge
HRESETn	1	Input	System synchronous reset, used by both sides of the bridge
HADDR	32	Input	AHB Address used by bridge address decode
HTRANS	2	Input	AHB Transfer state
HWRITE	1	Input	AHB Write command signal
HSIZE	3	Input	AHB Size – all transfers are treated as 32 bit transfers
HBURST	3	Input	AHB Burst type
HPROT	4	Input	AHB Access protection encoding
HWDATA	32	Input	AHB Write data
HSEL	1	Input	AHB Select line
HRDATA	32	Output	AHB read data
HREADY	1	Output	AHB ready, used to signal bus cycle completion
HRESP	2	Output	AHB Response field
PADDR	32	Output	APB Address, a pipelined version of the AHB address
PWDATA	32	Output	APB Write data
PENABLE	1	Output	APB Peripheral enable
PSEL	[NO_OF_SLAVES]	Output	APB Peripheral select – one per slave
PRDATA	32 * [NO_OF_SLAVES]	Input	APB Read data – 32 bits x number of slaves
PREADY	[NO_OF_SLAVES]	Input	APB Ready, one for each slave
PSELVERR	[NO_OF_SLAVES]	Input	APB Error indication, one for each slave