MGC Interrupt Controller And Programable Interval Timer (ICPIT)

Functional Description

The ICPIT provides a basic interrupt controller functionality together with the capability to implement two timers which can also be configured to generate interrupts. The host bus interface is a 32 bit APB interface.

Interrupt Controller Function

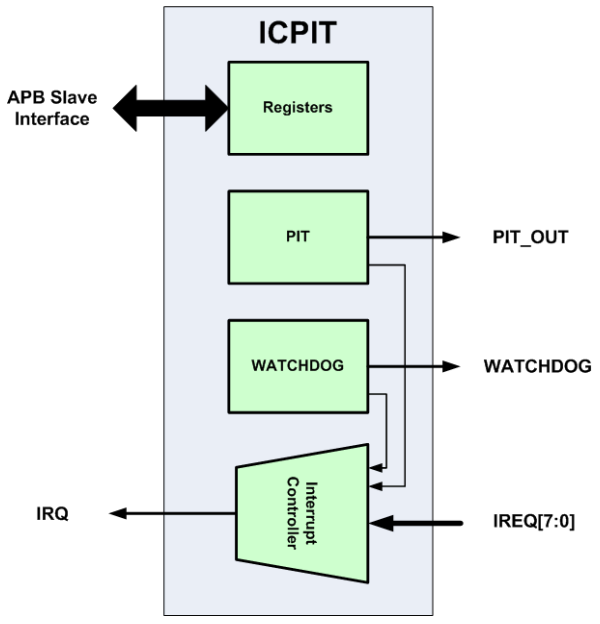
The interrupt controller monitors up to 8 external interrupt lines and 2 internal timer interrupts, sampling their state using the system clock. When a positive edge is detected on an interrupt line, then the interrupt controller latches the corresponding bit in the interrupt status register and raises the interrupt controllers interrupt line. When the interrupt status register is read, any set interrupt status bits are cleared and the interrupt line goes low.

Each interrupt input can be disabled or enabled via a bit in the interrupt enable register.

The interrupt controller also generates an interrupt from the Watchdog timer, this interrupt is not maskable via the interrupt enable register.

Timer Functions

There are two timers available, one is intended as a programmable interval timer and the other as a watchdog timer.



ICPIT Functional block diagram

Programmable Interval Timer (PIT)

The PIT loads the value set in the PIT count register and counts down on each positive edge of the system clock (PCLK). When the terminal count is reached, the PIT generates a time-out pulse which is one clock wide and then reloads the count register value on the next clock edge.

The PIT is enabled and disabled via the PIT enable bit in the PIT control register. The PITs current count value can be read back from the PIT current count register.

Watchdog Timer

The purpose of the Watchdog Timer is to provide a Watchdog function. It is implemented as a counter that counts down from 32'h4200_0000, starting from the end of reset (PRESETN). Once the watchdog reaches the zero terminal count, then it generates an interrupt.

The Watchdog Timer can be reloaded by writing a 1 to the Watchdog bit in the PIT control register, this bit is self-clearing and will be read back as a zero. The state of the Watchdog Timer cannot be read back.

Interface Port Description

The interface signal ports for the IPIT are detailed in the following table:

Port	Width	Direction	Description
PCLK	1	Input	APB System Clock
PRESETN	1	Input	APB Synchronous Reset – Active Low
PADDR	3	Input	APB Address
PSEL	1	Input	APB Peripheral Select
PENABLE	1	Input	APB Peripheral Enable
PWRITE	1	Input	APB Write Enable
PWDATA	32	Input	APB Write data
PRDATA	32	Output	APB Read data
PREADY	1	Output	APB Peripheral ready
IRQ	1	Output	Interrupt to host
IREQ	8	Input	Interrupt request inputs
PIT_OUT	1	Output	PIT terminal count flag
WATCHDOG	1	Output	Watchdog terminal count flag

Register Description

All the registers are read as 32 bit values and they are written to with a 32 bit value. Any unused bits will be read back as zeros and any writes to unused bits will have no effect.

Register Address Table:

Name	Address	Width	Access	Description
Interrupt Enable	Base + 0x0	10	RW	Interrupt Enable Register
Interrupt Status	Base + 0x4	10	R	Interrupt Status Register
PIT Count	Base + 0x8	32	RW	PIT Count value
PIT Current Count	Base + 0xc	32	RW	Current state of the PIT counter
PIT Control	Base + 0x10	2	RW	PIT and Watchdog control

Interrupt Enable Register Description

The interrupt enable register enables interrupts coming from the interrupt request inputs or the PIT terminal count. The Watchdog interrupt cannot be masked.

Bit	Access	Reset	Description
7:0	R/W	0x0	INTE Interrupt enables for each of IREQ lines
8	R/W	0x0	PITE Interrupt enable for the PIT terminal count interrupt
9	R	0x1	WDOGE Watchdog Interrupt enable – always enabled

Reset Value: 0x0000_0200

Interrupt Status Register Description

The interrupt status register indicates which interrupt(s) sources are currently active. When a status bit is read back as a '1', then it is reset to a '0'. If multiple edges occur on an interrupt line between host interrupt service routines, there is no storage of the interrupt events, the interrupt status bit is set by the first occurrence.

Bit	Access	Reset	Description
7:0	R	0x0	IREQ IREQ input interrupt event has occurred
8	R	0x0	PIT PIT terminal count interrupt
9	R	0x0	WDOG Watchdog Interrupt

Reset Value: 0x0000_0000

PIT Count Register Description

The PIT count register contains the count which is used by the PIT to count down from. Writing a value of 0 to the register will result in a permanent reload state

Bit	Access	Reset	Description
31:0	R/W	0x0	COUNT The PIT counts down from the value written to this field

Reset Value: 0x0000_0000

PIT Current Count Register Description

The PIT Current Count returns the value of the PIT counter at the point at which the register is read back.

Bit	Access	Reset	Description
31:0	R	0x0	COUNT The current PIT count value

Reset Value: 0x0000_0000

PIT Control Register Description

The PIT control register controls the enabling of the PIT and the reload of the Watchdog timer counter. The desired PIT count value should be loaded before the PIT is enabled.

A transition from not enabled to enabled will cause the PIT to be reloaded with the value in the PIT count register.

Bit	Access	Reset	Description
0	R/W	0x0	PIT_ENABLE '1' – PIT counter is enabled '0' – PIT counter is disabled
1	W	0x0	WATCHDOG_BONE '1' – Reloads the Watchdog Timer '0' – Has no effect

Reset Value: 0x0000_0000