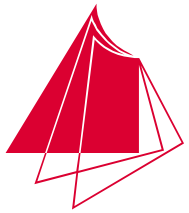

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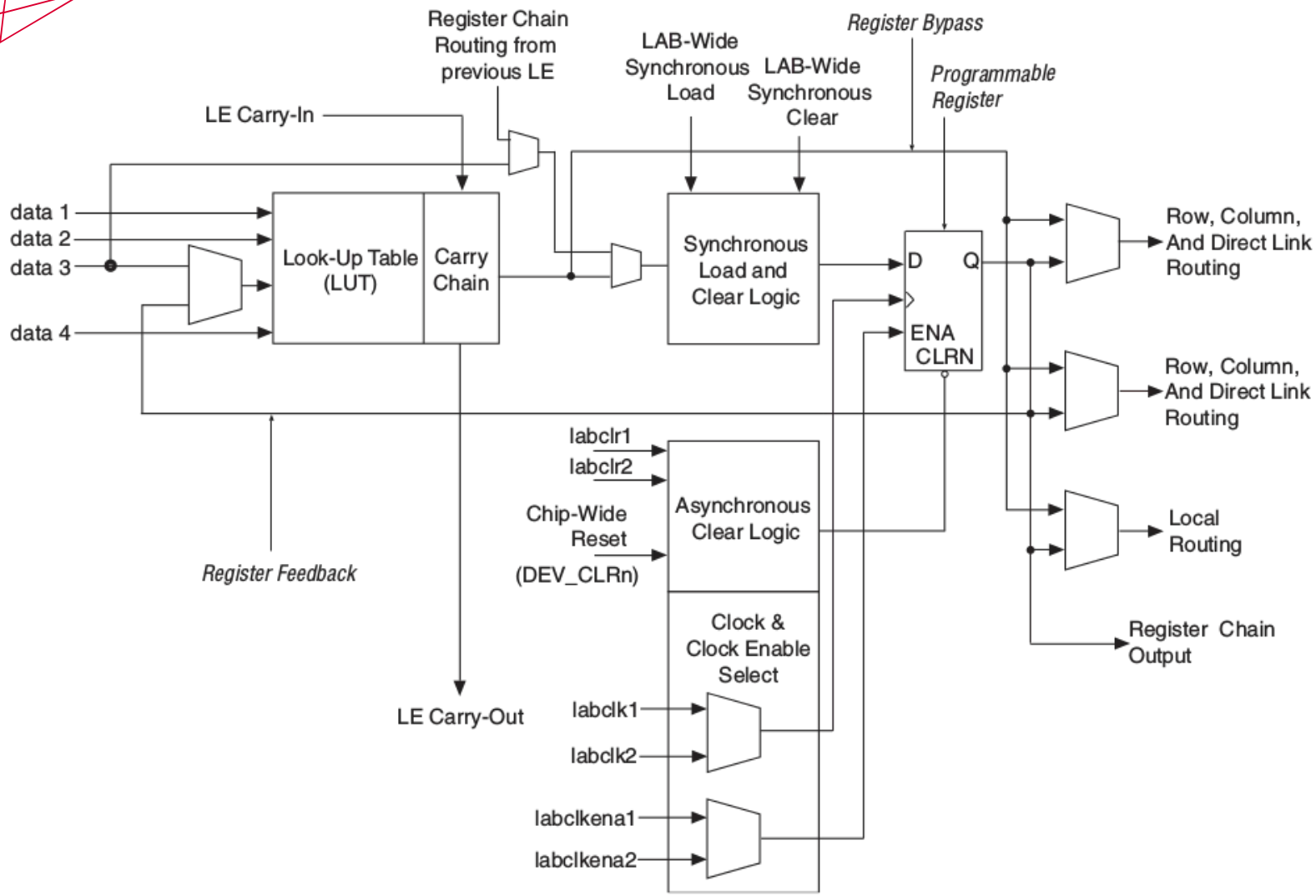
Project B Presentation

Fully Programmable Adaptive-Digital-Filter Architecture implemented on Altera DE2i-150 development board

Luis Ardila

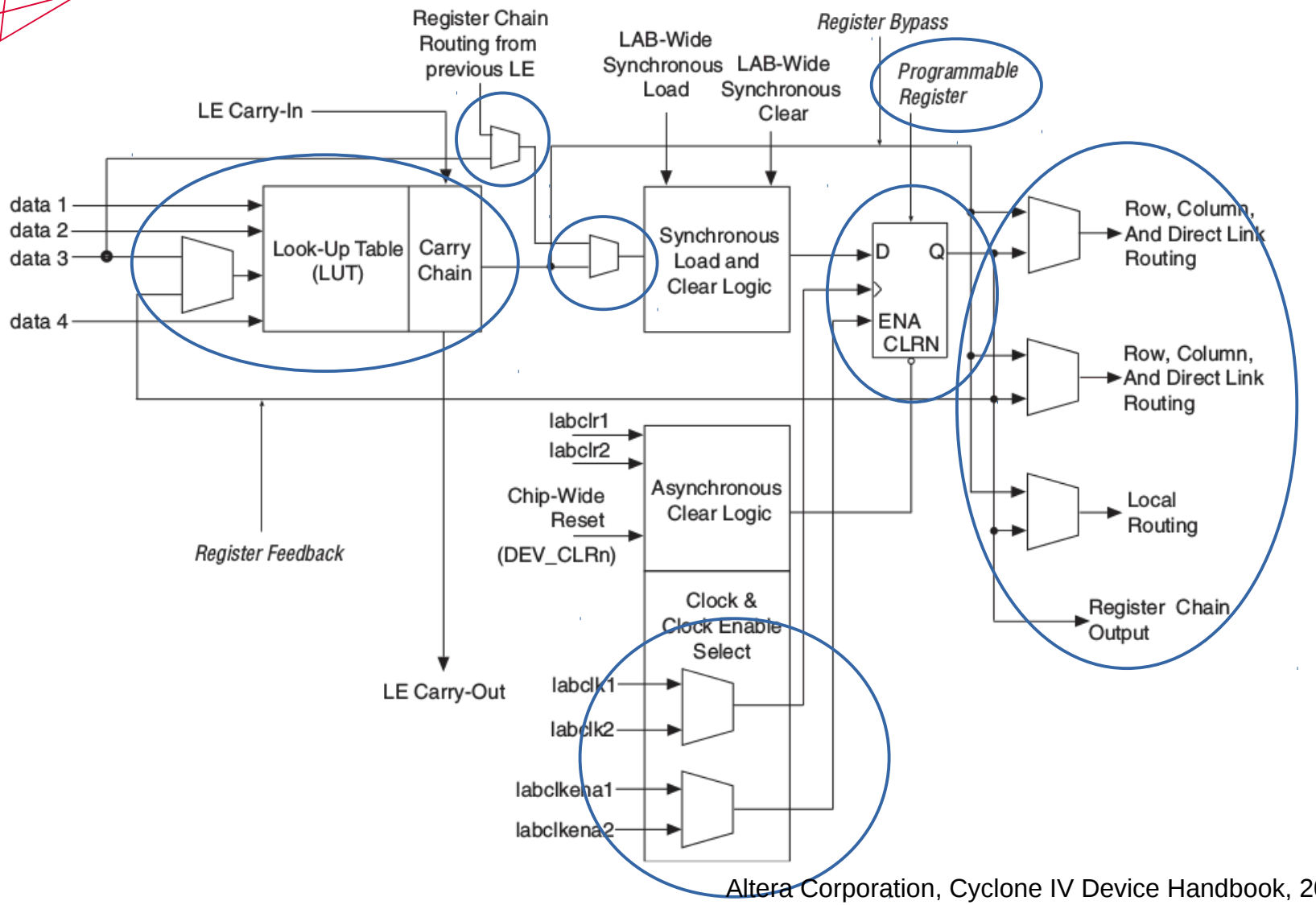
Prof. Dr. Michael Bantel
Prof. Dr. Christian Langen

Cyclone IV Logic Elements



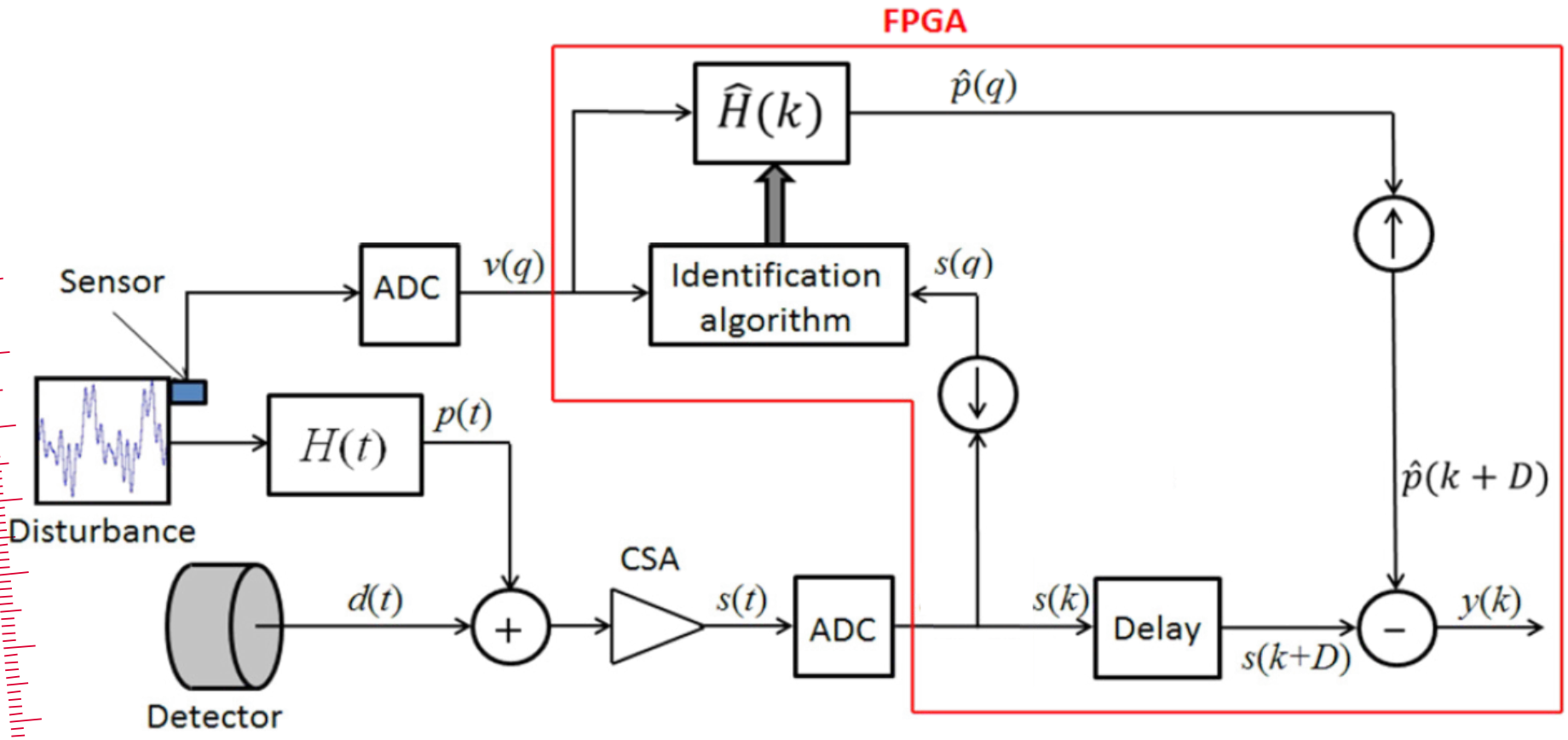
Altera Corporation, Cyclone IV Device Handbook, 2009

Cyclone IV Logic Elements



Altera Corporation, Cyclone IV Device Handbook, 2009

System Overview



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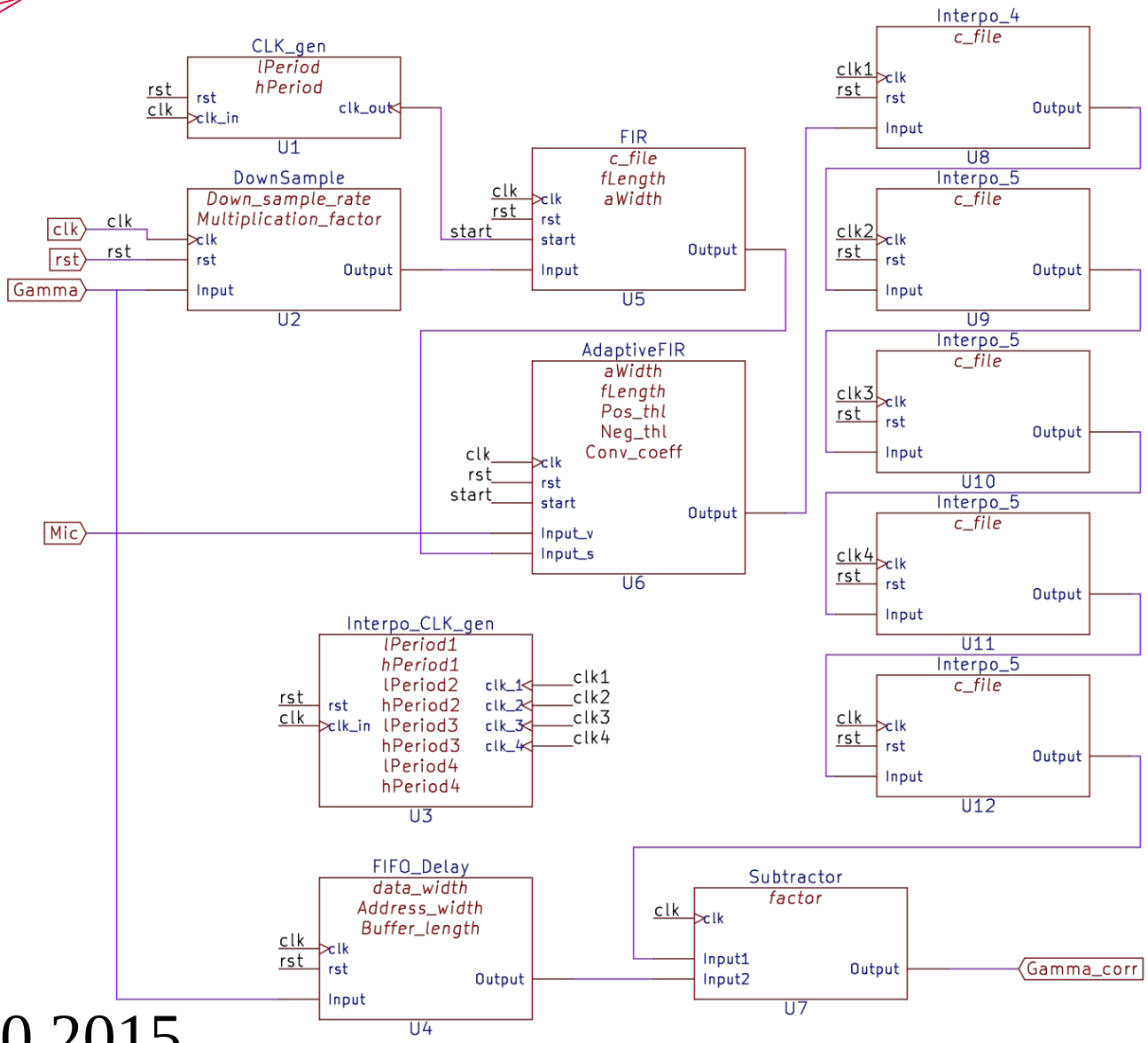
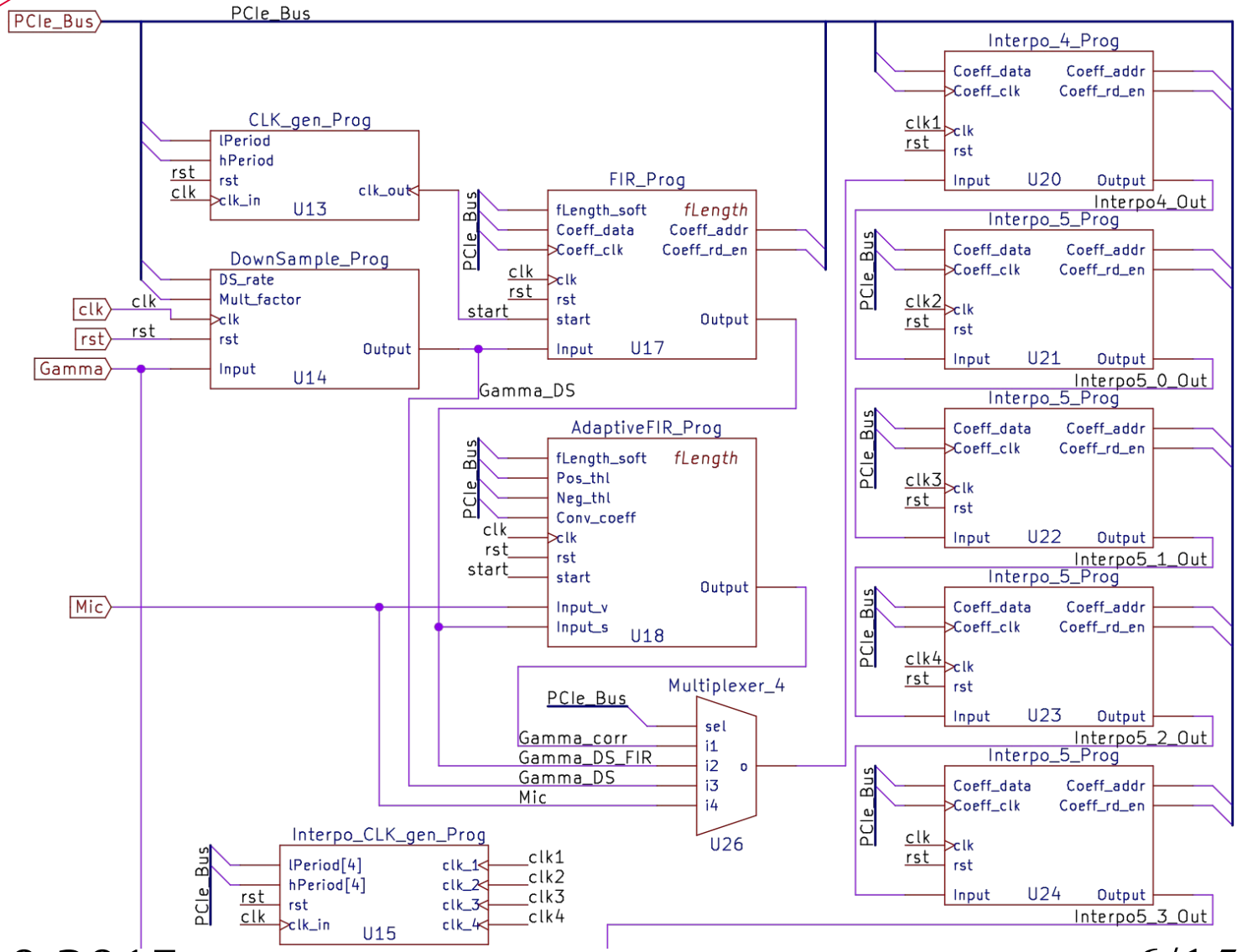
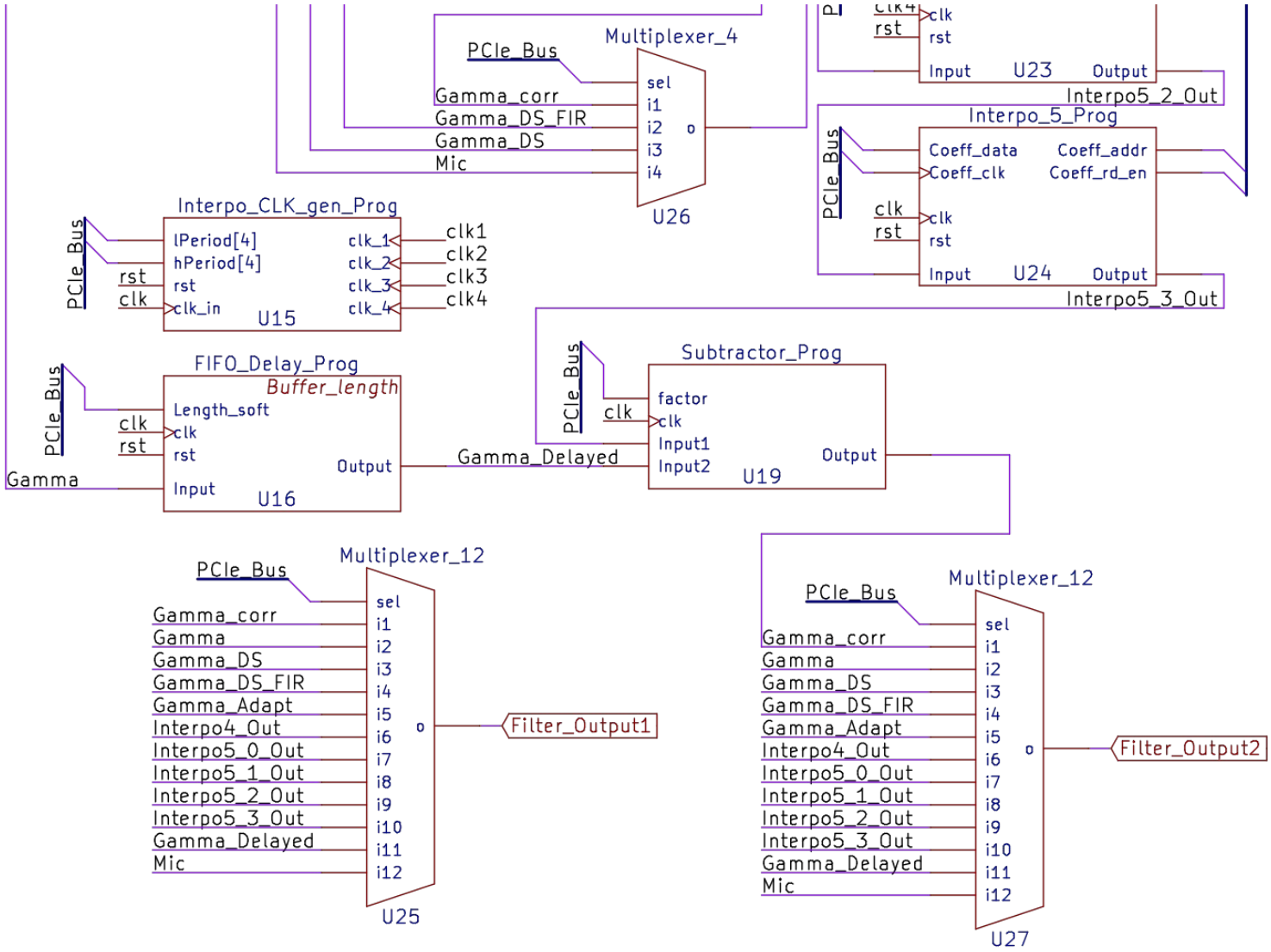
C. Pfeiffer's Architecture



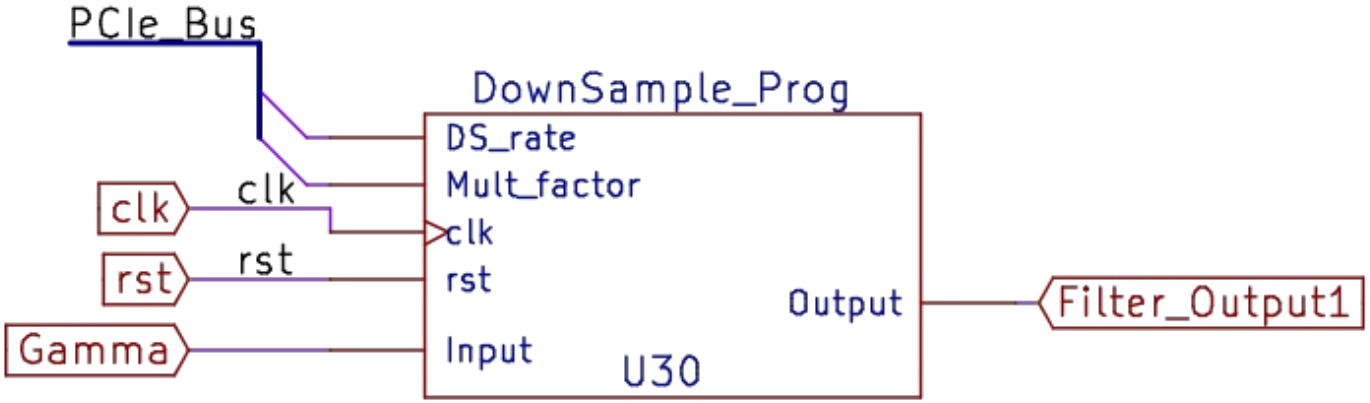
Programmable Architecture (1/2)



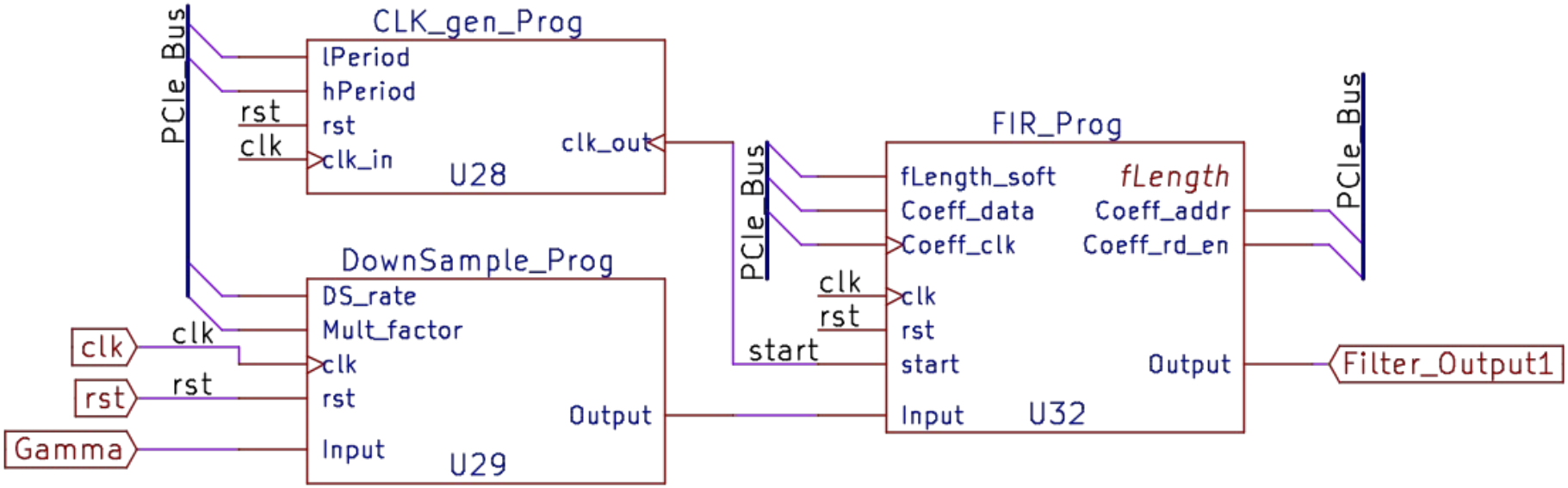
Programmable Architecture (2/2)



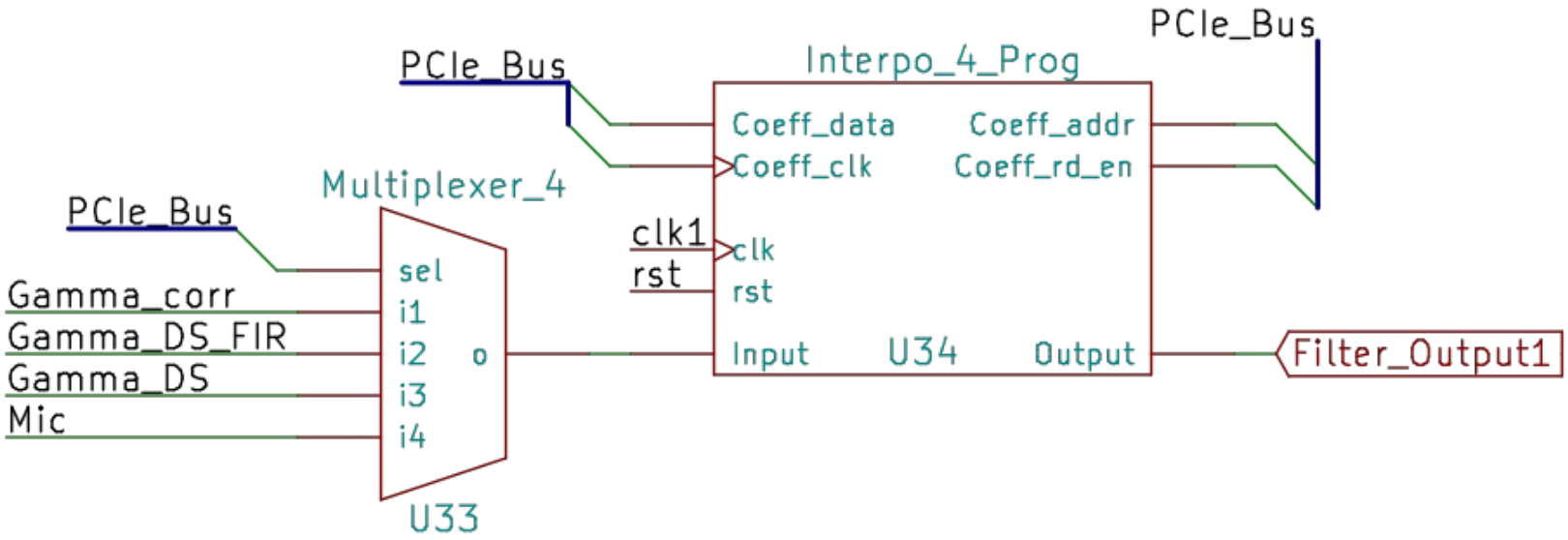
Down Sample


PCIe_Bus
DownSample_Prog
DS_rate
Mult_factor
clk
rst
Input
Output
U30
clk
clk
rst
rst
Gamma
Filter_Output1

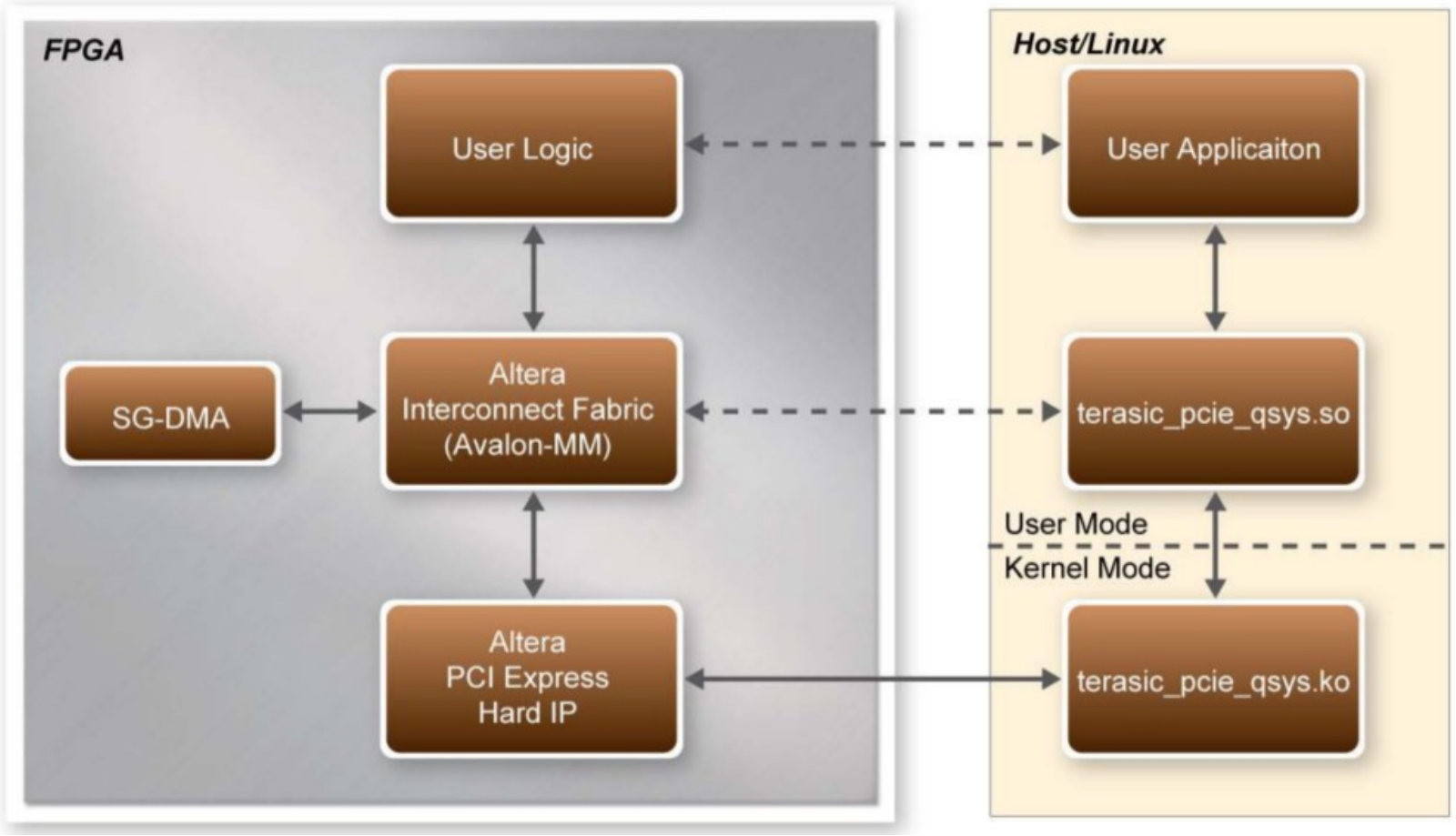
Down Sample + High Pass FIR



Interpolation x4



PCIe System Framework

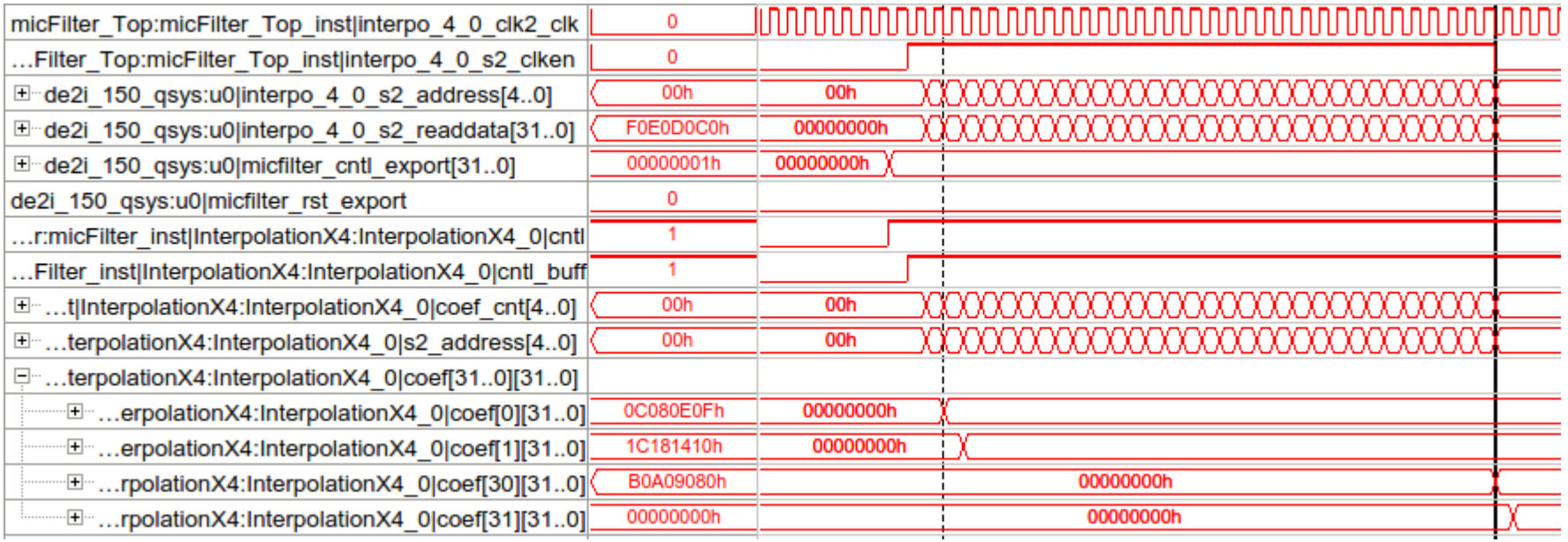


Terasic DE2i-150 Development Kit FPGA System User Manual, 2013

PCIE_API

- PCIE_Read32
- PCIE_Write32
- PCIE_Read16
- PCIE_Write16
- PCIE_Read8
- PCIE_Write8
- PCIE_DmaRead
- PCIE_DmaWrite
- PCIE_DmaFifoRead
- PCIE_DmaFifoWrite
- PCIE_Close

DMA Transfer



PCIE_API PCIE_Write32: 32 bits every 8 us → 4 Mbits/s.

PCIE_DmaWrite: 32 bits every 20 ns → 1.6 Gbit/s

Reading memory from User logic: 32 bits every 40 ns → 800 Mbit/s

Resources Utilization

Family	Cyclone IV GX
Device	EP4CGX150DF31C7
Total logic elements	88,832 / 149,760 (59 %)
Total combinational functions	61,109 / 149,760 (41 %)
Dedicated logic registers	54,165 / 149,760 (36 %)
Total registers	54165
Total pins	467 / 508 (92 %)
Total memory bits	5,431,786 / 6,635,520 (82 %)
Embedded Multiplier 9-bit elements	168 / 720 (23 %)
Total PLLs	2 / 8 (25 %)

Memory Bits: Delay FIFO: 88 %
SignalTap: 8 %
Filter Coefficients, Registers Memory: 4 %

Conclusions

- A fully programmable architecture has been successfully designed and implemented
- Complete observability over every single module and stage of the filter is achievable
- Displaying tools available for Hardware properties such as the adapted coefficient filters along the time
- A variety of routing choices are available inside the filter in order to change the architecture depending on the needs
- Fast design and evaluation of FIR filters is possible
- Topology is applicable to other architecture designs in different kind of applications