



Project B Presentation

Fully Programmable Adaptive-Digital-Filter Architecture implemented on Altera DE2i-150 development board

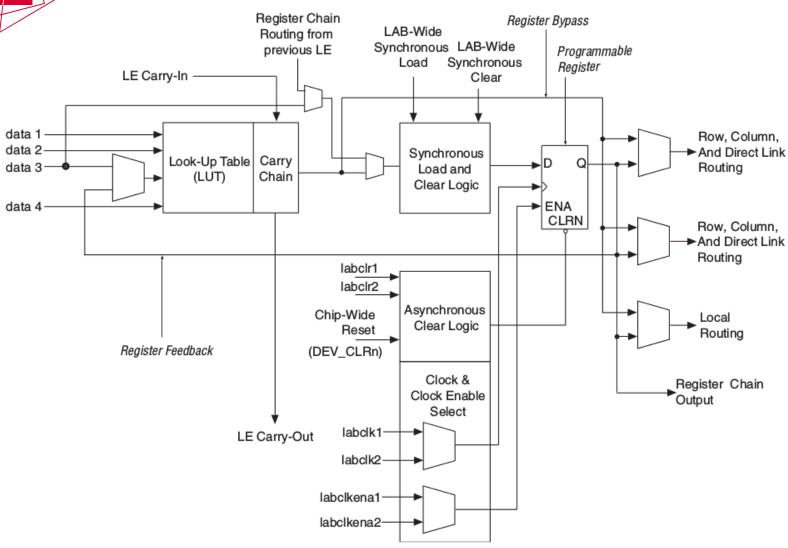
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29.10.2015



Cyclone IV Logic Elements

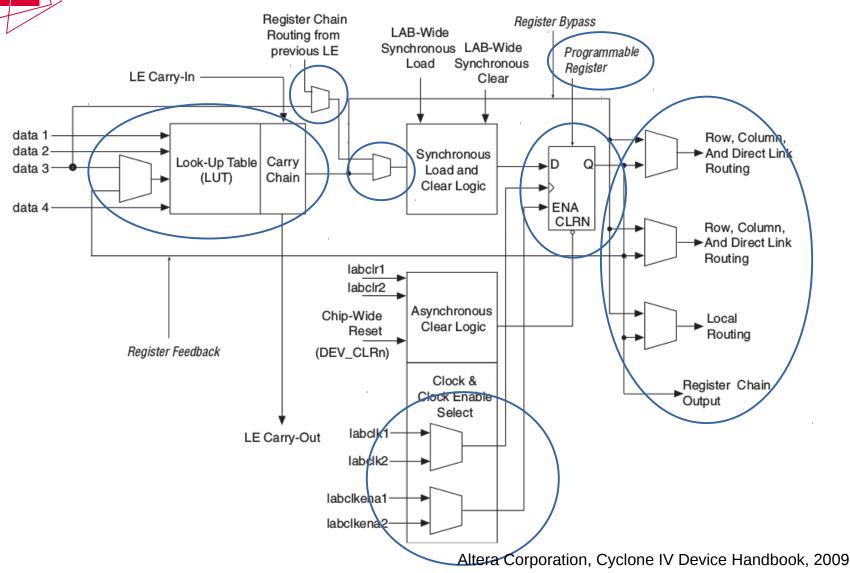


Altera Corporation, Cyclone IV Device Handbook, 2009

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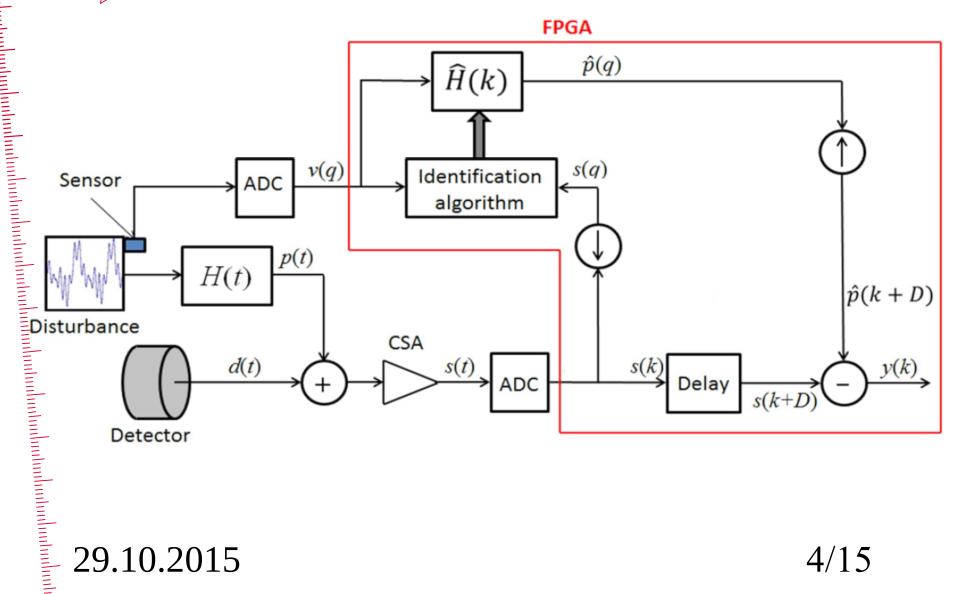
Cyclone IV Logic Elements



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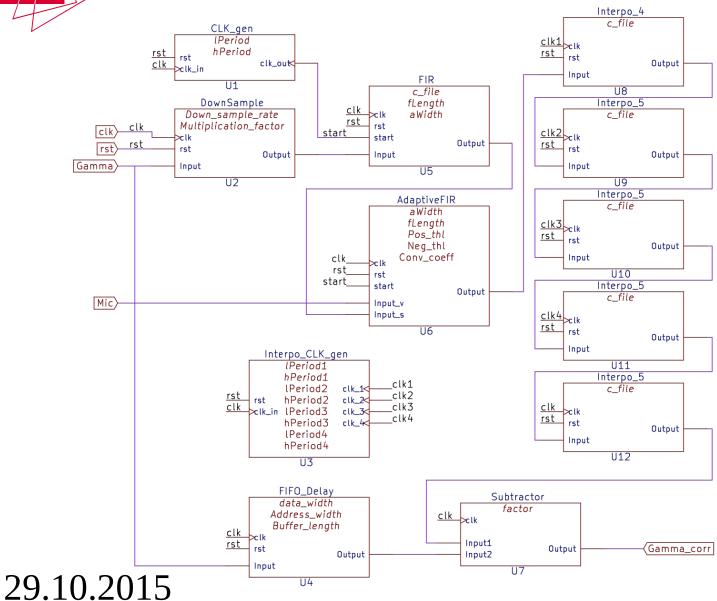
System Overview

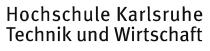


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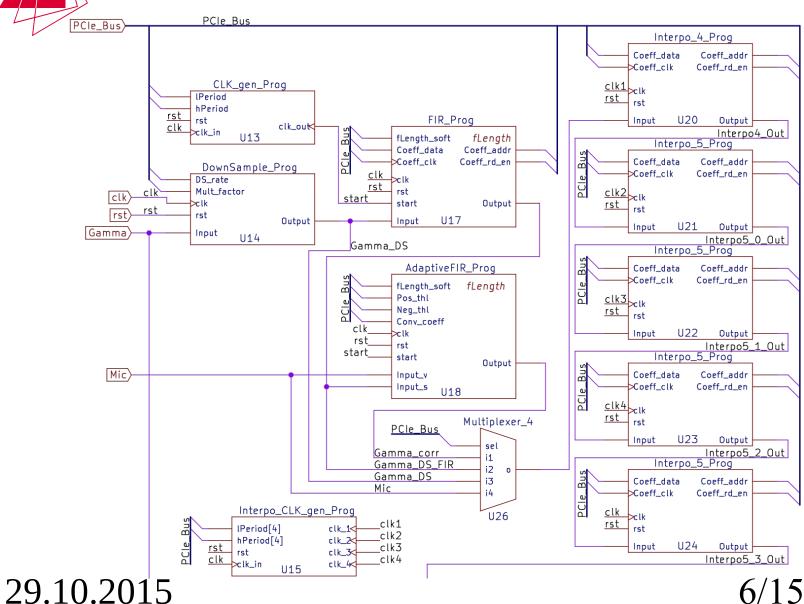
C. Pfeiffer's Architecture





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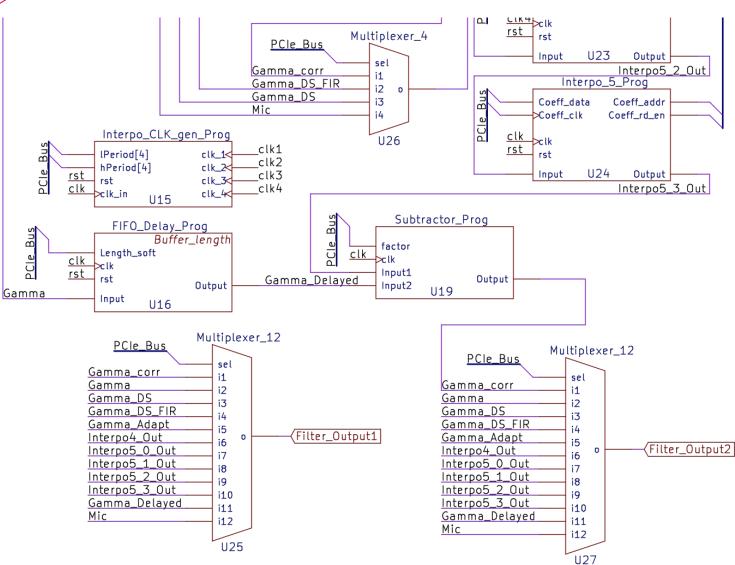
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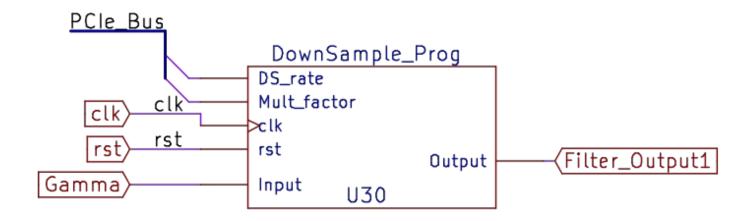
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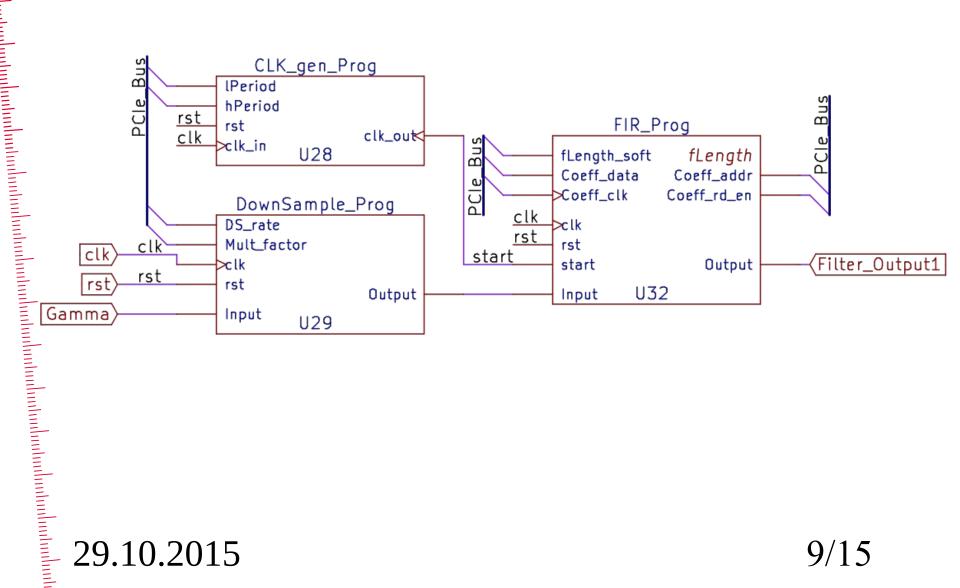
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Down Sample



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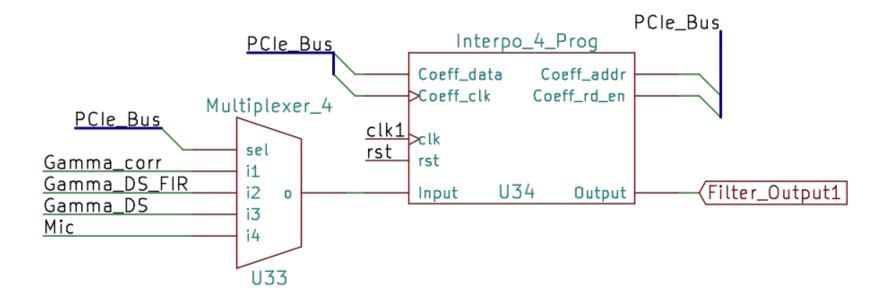
Down Sample + High Pass FIR



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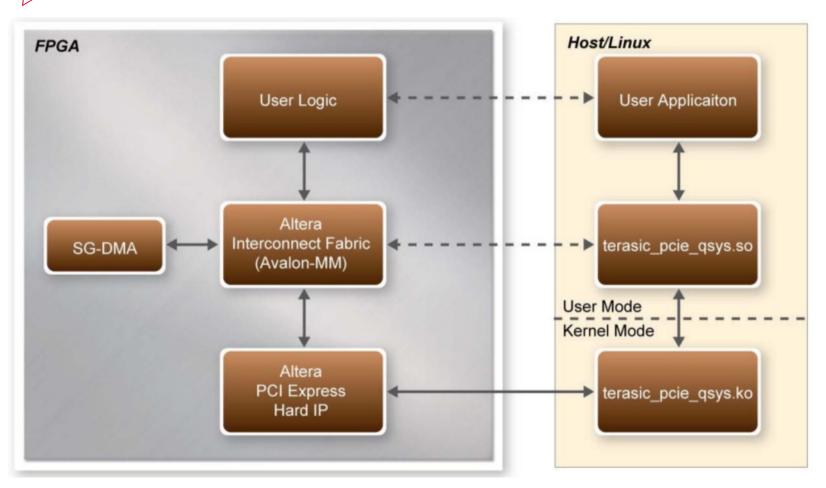


Interpolation x4



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PCIe System Framework



Terasic DE2i-150 Development Kit FPGA System User Manual, 2013

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PCIE_API

- PCIE_Read32
- PCIE Write32
- PCIE_Read16
- PCIE_Write16
- PCIE_Read8
- PCIE_Write8

- PCIE DmaRead
- PCIE_DmaWrite
- PCIE DmaFifoRead
- PCIE DmaFifoWrite
- PCIE_Close

DMA Transfer

micFilter_Top:micFilter_Top_inst interpo_4_0_clk2_clk	0	
Filter_Top:micFilter_Top_inst interpo_4_0_s2_clken	0	
de2i_150_qsys:u0 interpo_4_0_s2_address[40]	00h	00h XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
de2i_150_qsys:u0 interpo_4_0_s2_readdata[310]	F0E0D0C0h	00000000h)()()()()()()()()()()()()()()()()()()(
de2i_150_qsys:u0 micfilter_cntl_export[310]	00000001h	00000000h X
de2i_150_qsys:u0 micfilter_rst_export	0	
r:micFilter_inst InterpolationX4:InterpolationX4_0 cntl	1	
Filter_inst InterpolationX4:InterpolationX4_0 cntl_buff	1	
⊞t InterpolationX4:InterpolationX4_0 coef_cnt[40]	00h	00h XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
•terpolationX4:InterpolationX4_0 s2_address[40]	00h	00h 0000000000000000000000000000000000
terpolationX4:InterpolationX4_0 coef[310][310]		
•erpolationX4:InterpolationX4_0 coef[0][310]	0C080E0Fh	00000000h X
•erpolationX4:InterpolationX4_0 coef[1][310]	1C181410h	0000000h X
•rpolationX4:InterpolationX4_0 coef[30][310]	B0A09080h	00000000h
•rpolationX4:InterpolationX4_0 coef[31][310]	00000000h	00000000h

PCIE_API PCIE_Write32: 32 bits every 8 us → 4 Mbits/s.

PCIE_DmaWrite: 32 bits every 20 ns → 1.6 Gbit/s

Reading memory from User logic: 32 bits every 40 ns → 800 Mbit/s

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Resources Utilization

Family	Cyclone IV GX
Device	EP4CGX150DF31C7
Total logic elements	88,832 / 149,760 (59 %)
Total combinational functions	61,109 / 149,760 (41 %)
Dedicated logic registers	54,165 / 149,760 (36 %)
Total registers	54165
Total pins	467 / 508 (92 %)
Total memory bits	5,431,786 / 6,635,520 (82 %)
Embedded Multiplier 9-bit elements	168 / 720 (23 %)
Total PLLs	2/8(25%)

Memory Bits: Delay FIFO: 88 %

SignalTap: 8 %

Filter Coefficients, Registers Memory: 4 %

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Conclusions

- A fully programmable architecture has been successfully designed and implemented
- Complete observability over every single module and stage of the filter is achievable
- Displaying tools available for Hardware properties such as the adapted coefficient filters along the time
- A variety of routing choices are available inside the filter in order to change the architecture depending on the needs
- Fast design and evaluation of FIR filters is possible
- Topology is applicable to other architecture designs in different kind of applications

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