2. Address Translation

You have a multi-level paged system with a 16-bit virtual address, a two-level page table, 256-byte pages, and 4 KB of physical memory. Assuming the first-level page table holds 8 entries:

(a) [2pts] How many bits in the virtual address represent the offset?

(b) [2pts] How many frames does the system have?

(c) [2pts] How many pages are potentially available to the process?

(d) [2pts] How many entries does the second-level page table hold?

(e) [2pts] How does the kernel locate the first-level page table?

(f) [4pts] How would the number of pages potentially available to the process change if the system were a single-level paged system?