2. Address Translation

You have a multi-level paged system with a 16-bit virtual address, a two-level page table, 256-byte pages, and 4 KB of physical memory. Assuming the first-level page table holds 8 entries:

(a) [2pts] How many bits in the virtual address represent the offset?

```
8

-2 wrong
```

(b) [2pts] How many frames does the system have?

```
16

-2 wrong
```

(c) [2pts] How many pages are potentially available to the process?

```
256

-2 wrong
```

(d) [2pts] How many entries does the second-level page table hold?

```
32

-2 wrong
```

(e) [2pts] How does the kernel locate the first-level page table?

```
Using the page table base register

-2 no mention of register
```

(f) [4pts] How would the number of pages potentially available to the process change if the system were a single-level paged system?

```
It doesn't.  The multi-level page table just looks at the high-order
bits differently---it doesn't actually change the number of pages.

-4 wrong
```