Release Notes for

AT32F435_437 Firmware Library Drivers

V2.0.7-2025/11/24

1. ADC
   - Added the new function “adc_combine_mode_set()” to configure combined master/slave mode
2. CRM
   - Changed the bit name of adc14rst to tmr14rst, and added new bit name “adc2en bit”
3. GPIO
   - Added the new function “gpio_bits_toggle()”
4. QSPI
   - Changed the width of the xip_cmd_w2_bit.xipr_dcnt to 6 bits
5. TMR
   - Updated these functions: tmr_pwm_input_config(), tmr_encoder_mode_config() and tmr_output_channel_config().
     Note that the channel must be disabled before configuring channel mode, otherwise the channel mode fails to switch
6. Updated some notes

V2.0.6-2024/12/13

1. PWC
   - Updated LDO output level settings, and removed LDO configuration option “PWC_LDO_OUTPUT_1V0”.
2. CAN
   - Updated “can_transmit_cancel()” function writing to avoid cross-mailbox interference due to misoperation.
3. USB
   - Updated “usb_hch_halt()” function in host mode and improved channel halt processing flow.
   - Updated “usb_hc_enable()” function in host mode to ensure that its original state is cleared when enabling the corresponding channel.
   - Updated “usb_host_disable()” function in host mode, and updated process of disabling channels to avoid inadvertently opening the remaining channels.
   - Updated “usb_ept_open()” function in device mode, and added synchronous transfer handling (frame number ignored).
   - Updated “usb_ept_close()” function in device mode, and improved endpoint closing process.

V2.0.5-2024/08/08

1. QSPI
   - Added “qspi_auto_ispc_enable()” function for bus input clock phase matching.

- Revised FIFO depth definition from “QSPI_DMA_FIFO_THOD_WORD32” to “QSPI_DMA_FIFO_THOD_WORD24”.
- Updated “qspi_flag_clear()” function writing and fixed AC6 compilation problems.

V2.0.4-2024/01/05

1. Fixed IAR7.4 compilation warning issue of some drivers.
2. Optimized EMAC PTP driver.
3. Updated “dvp_flag_get()” and “dvp_interrupt_flag_get()” functions.

V2.0.3-2023/10/26

1. Added “interrupt_flag_get” function to each of the IP sections.
2. Optimized system clock switching process.
3. Updated IRTMR driver.
4. Updated ADC drivers to improve soft trigger process.
5. Updated some notes.

V2.0.2-2023/08/04

1. Updated “qspi_xip_enable()” function.
2. Updated the process of judging sector conditions in flash_slib_enable.
3. Added CRC polynomial support.
4. Updated the process of the “adc_ordinary_channel_set()” function and “adc_preempt_channel_set()” function.
5. Updated some notes.

V2.0.1-2023/02/16

1. Adjusted the enumeration location of CRM emac lowpower to AT32F437.

V2.0.0-2022/11/18

1. Updated “xmc_ext_timing_config()” function.
2. CRM_HICK48_NODIV is considered the default setting when HICK is used as PLL clock source.