DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4049B
buffers
HEX inverting buffers

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

HEX INVERTING BUFFERS

The HEF4049B provides six inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. Their guaranteed fan-out into common bipolar logic elements is shown in the table below.

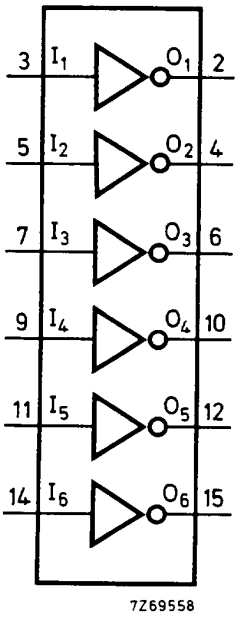

Fig. 1 Functional diagram.

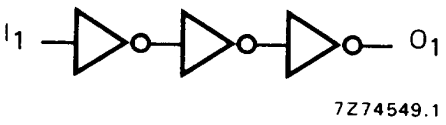

Fig. 3 Logic diagram (one gate).

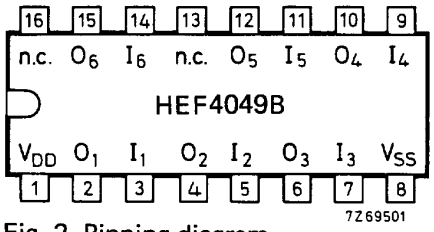

Fig. 2 Pinning diagram.

HEF4049BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4049BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4049BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

Guaranteed fan-out in common logic families

driven element	guaranteed fan-out
standard TTL	2
74LS	9
74L	16

Input protection

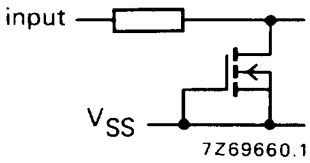

Fig. 4 Input protection circuit that allows input voltages in excess of V_{DD}.

APPLICATION INFORMATION

Some examples of applications for the HEF4049B are:

- LOCMOS to DTL/TTL converter
- HIGH sink current for driving 2 TTL loads
- HIGH-to-LOW level logic conversion

FAMILY DATA

I_{DD} LIMITS category BUFFERS } see Family Specifications

D.C. CHARACTERISTICS V_{SS} = 0 V; V_I = V_{SS} or V_{DD}

HEF	V_{DD} V	V_O V	symbol	T_{amb}(°C) −40 min.	max.	+25 min.	max.	+85 min.	max.	
Output (sink) current LOW	4,75	0,4	I_{OL}	3,5	–	2,9	–	2,3	–	mA
	10	0,5		12,0	–	10,0	–	8,0	–	mA
	15	1,5		24,0	–	20,0	–	16,0	–	mA
Output (source) current HIGH	5	4,6	$-I_{OH}$	0,52	–	0,44	–	0,36	–	mA
	10	9,5		1,3	–	1,1	–	0,9	–	mA
	15	13,5		3,6	–	3,0	–	2,4	–	mA
Output (source) current HIGH	5	2,5	$-I_{OH}$	1,7	–	1,4	–	1,1	–	mA

HEC	V_{DD} V	V_O V	symbol	T_{amb}(°C) −55 min.	max.	+25 min.	max.	+125 min.	max.	
Output (sink) current LOW	4,75	0,4	I_{OL}	3,6	–	2,9	–	1,9	–	mA
	10	0,5		12,5	–	10,0	–	6,7	–	mA
	15	1,5		25,0	–	20,0	–	13,0	–	mA
Output (source) current HIGH	5	4,6	$-I_{OH}$	0,52	–	0,44	–	0,36	–	mA
	10	9,5		1,3	–	1,1	–	0,9	–	mA
	15	13,5		3,6	–	3,0	–	2,4	–	mA

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	35	70	ns	26 ns + (0,18 ns/pF) C_L
	10		15	30	ns	11 ns + (0,08 ns/pF) C_L
	15		12	25	ns	9 ns + (0,05 ns/pF) C_L
LOW to HIGH	5	t_{PLH}	50	100	ns	23 ns + (0,55 ns/pF) C_L
	10		25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
Output transition times HIGH to LOW	5	t_{THL}	20	40	ns	3 ns + (0,35 ns/pF) C_L
	10		10	20	ns	3 ns + (0,14 ns/pF) C_L
	15		7	14	ns	2 ns + (0,09 ns/pF) C_L
LOW to HIGH	5	t_{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	2 500 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz)
	10	11 000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_o = output freq. (MHz)
	15	35 000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)