June 1998

National Semiconductor

DS90LV019
3.3V or 5V LVDS Driver/Receiver

General Description

The DS90LV019 is a Driver/Receiver designed specifically for the high speed low power point-to-point interconnect applications. The device operates from a single 3.3V or 5.0V power supply and includes one differential line driver and one receiver. The DS90LV019 features an independent driver and receiver with TTL/CMOS compatibility (D_{IN} and R_{OUT}). The logic interface provides maximum flexibility as 4 separate lines are provided (D_{IN}, DE, $\overline{RE}$, and R_{OUT}). The device also features a flow-through pin out which allows easy PCB routing for short stubs between its pins and the connector. The driver has 3.5 mA output loop current.

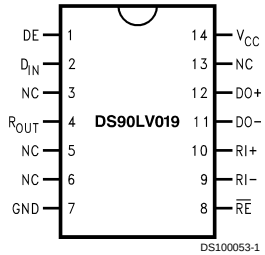
The driver translates between TTL levels (single-ended) to Low Voltage Differential Signaling levels. This allows for high speed operation, while consuming minimal power with reduced EMI. In addition, the differential signaling provides common-mode noise rejection.

The receiver threshold is ±100 mV over a ±1V common-mode range and translates the low swing differential levels to standard (TTL/CMOS) levels.

Features

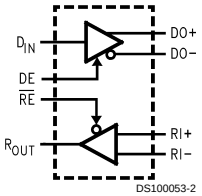
- LVDS Signaling
- 3.3V or 5.0V operation
- Low power CMOS design
- Balanced Output Impedance
- Glitch free power up/down (Driver disabled)
- High Signaling Rate Capacity (above 100 Mbps)
- Ultra Low Power Dissipation
- ±1V Common-Mode Range
- ±100 mV Receiver Sensitivity
- Product offered in SOIC package
- Flow-Through Pin Out
- Industrial Temperature Range Operation

Connection Diagram



Order Number DS90LV019TM
See NS Package Number M14A

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage V_{CC}	6.0V
Enable Input Voltage (DE, $\overline{RE}$)	−0.3V to (V_{CC} +0.3V)
Driver Input Voltage (D_{IN})	−0.3V to (V_{CC} + 0.3V)
Receiver Output Voltage (R_{OUT})	−0.3V to (V_{CC} + 0.3V)
Driver Output Voltage (DO±)	−0.3V to +3.9V
Receiver Input Voltage (RI±)	−0.3V to (V_{CC} + 0.3V)
Driver Short Circuit Current	Continuous
ESD (Note 4)	
(HBM, 1.5 kΩ, 100 pF)	> 2.0 kV
(EIAJ, 0 Ω, 200 pF)	> 200 V
Maximum Package Power Dissipation at 25˚C	
SOIC	960 mW
Derate SOIC Package	7.7mW/˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering, 4 sec.)	260˚C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC}) or	3.0	3.6	V
Supply Voltage (V_{CC})	4.5	5.5	V
Receiver Input Voltage	0.0	2.4	V
Operating Free Air Temperature T_A	−40	+85	˚C

DC Electrical Characteristics

T_A = −40˚C to +85˚C unless otherwise noted, V_{CC} = 3.3 ± 0.3V. (Notes 2, 3)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS							
V_{OD}	Output Differential Voltage	R_L = 100Ω (*Figure 1*)	DO+, DO−	250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change				6	60	mV
V_{OS}	Offset Voltage			1	1.25	1.7	V
ΔV_{OS}	Offset Magnitude Change				5	60	mV
I_{OZD}	TRI-STATE ®Leakage	V_{OUT} = V_{CC} or GND, DE = 0V		−10	±1	+10	µA
I_{OXD}	Power-Off Leakage	V_{OUT} = 3.6V or GND, V_{CC} = 0V		−10	±1	+10	µA
I_{OSD}	Output Short Circuit Current	V_{OUT} = 0V, DE = V_{CC}		−10	−6	−4	mA
DIFFERENTIAL RECEIVER CHARACTERISTICS							
V_{OH}	Voltage Output High	VID = +100 mV, I_{OH} = −400 µA	R_{OUT}	2.9	3.3		V
		Inputs Open, I_{OH} = −400 µA		2.9	3.3		V
V_{OL}	Voltage Output Low	I_{OL} = 2.0 mA, VID = −100 mV			0.1	0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V		−75	−34	−20	mA
V_{TH}	Input Threshold High		RI+, RI−			+100	mV
V_{TH}	Input Threshold Low			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V or 0V, V_{CC} = 3.6V or 0V		−10	±1	+10	µA
DEVICE CHARACTERISTICS							
V_{IH}	Minimum Input High Voltage		D_{IN}, DE, $\overline{RE}$	2.0		V_{CC}	V
V_{IL}	Maximum Input Low Voltage			GND		0.8	V
I_{IH}	Input High Current	V_{IN} = V_{CC} or 2.4V			±1	±10	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V			±1	±10	µA
V_{CL}	Input Diode Clamp Voltage	I_{CLAMP} = −18 mA		−1.5	−0.7		V
I_{CCD}	Power Supply Current	DE = $\overline{RE}$ = V_{CC}	V_{CC}		9	12.5	mA
I_{CCR}		DE = $\overline{RE}$ = 0V			4.5	7.0	mA
I_{CCZ}		DE = 0V, $\overline{RE}$ = V_{CC}			3.7	7.0	mA
I_{CC}		DE = V_{CC}, $\overline{RE}$ = 0V			15	20	mA
$C_{D\ output}$	Capacitance		DO+, DO−		5		pF
$C_{R\ input}$	Capacitance		RI+, RI−		5		pF

DC Electrical Characteristics

T_A = −40˚C to +85˚C unless otherwise noted, V_{CC} = 5.0 ± 0.5V. (Notes 2, 3)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS							
V_{OD}	Output Differential Voltage	R_L = 100Ω (*Figure 1*)	DO+, DO−	250	360	450	mV
ΔV_{OD}	V_{OD} Magnitude Change				6	60	mV
V_{OS}	Offset Voltage			1	1.25	1.8	V
ΔV_{OS}	Offset Magnitude Change				5	60	mV
I_{OZD}	TRI-STATE Leakage	V_{OUT} = V_{CC} or GND, DE = 0V		−10	±1	+10	µA
I_{OXD}	Power-Off Leakage	V_{OUT} = 5.5V or GND, V_{CC} = 0V		−10	±1	+10	µA
I_{OSD}	Output Short Circuit Current	V_{OUT} = 0V, DE = V_{CC}		−10	−6	−4	mA
DIFFERENTIAL RECEIVER CHARACTERISTICS							
V_{OH}	Voltage High	VID = +100 mV, I_{OH} = −400 µA	R_{OUT}	4.3	5.0		V
		Inputs Open, I_{OH} = −400 µA		4.3	5.0		V
V_{OL}	Voltage Output Low	I_{OL} = 2.0 mA, VID = −100 mV			0.1	0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V		−150	−75	−40	mA
V_{TH}	Input Threshold High		RI+, RI−			+100	mV
V_{TH}	Input Threshold Low			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V or 0V, V_{CC} = 5.5V or 0V		−15	±1	+15	µA
DEVICE CHARACTERISTICS							
V_{IH}	Minimum Input High Voltage		D_{IN}, DE, $\overline{RE}$	2.0		V_{CC}	V
V_{IL}	Maximum Input Low Voltage			GND		0.8	V
I_{IH}	Input High Current	V_{IN} = V_{CC} or 2.4 V			±1	±10	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V			±1	±10	µA
V_{CL}	Input Diode Clamp Voltage	I_{CLAMP} = −18 mA		−1.5	−0.8		V
I_{CCD}	Power Supply Current	DE = $\overline{RE}$ = V_{CC}	V_{CC}		12	19	mA
I_{CCR}		DE = $\overline{RE}$ = 0V			5.8	8	mA
I_{CCZ}		DE = 0V, $\overline{RE}$ = V_{CC}			4.5	8.5	mA
I_{CC}		DE = V_{CC}, $\overline{RE}$ = 0V			18	48	mA
$C_{D\ output}$	Capacitance		DO+, DO−		5		pF
$C_{R\ input}$	Capacitance		RI+, RI−		5		pF

Note 1: "Absolute Maximum Ratings" are these beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = +3.3V or +5.0V and T_A = +25˚C, unless otherwise stated.

Note 4: ESD Rating:

HBM (1.5 kΩ, 100 pF) > 2.0 kV

EIAJ (0Ω, 200 pF) > 200V.

Note 5: C_L includes probe and fixture capacitance.

Note 6: Generator waveforms for all tests unless otherwise specified; f = 1 MHz, Z_O = 50Ω, $t_r = t_f \leq 6.0$ ns (0%–100%).

AC Electrical Characteristics

T_A = −40˚C to +85˚C, V_{CC} = 3.3V ± 0.3V. (Note 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 10 pF (*Figure 2* and *Figure 3*)	2.0	4.0	6.5	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.0	5.6	7.0	ns
t_{SKD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$			0.4	1.0	ns
t_{TLH}	Transition Time Low to High		0.2	0.7	3.0	ns
t_{THL}	Transition Time High to Low		0.2	0.8	3.0	ns

AC Electrical Characteristics (Continued)

T_A = −40˚C to +85˚C, V_{CC} = 3.3V ± 0.3V. (Note 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER TIMING REQUIREMENTS						
t_{PHZ}	Disable Time High to Z	R_L = 100Ω, C_L = 10 pF (*Figure 4* and *Figure 5*)	1.5	4.0	8.0	ns
t_{PLZ}	Disable Time Low to Z		2.5	5.3	9.0	ns
t_{PZH}	Enable Time Z to High		4.0	6.0	8.0	ns
t_{PZL}	Enable Time Z to Low		3.5	6.0	8.0	ns
RECEIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 10 pF, VID = 200 mV (*Figure 6* and *Figure 7*)	3.0	5.8	7.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		3.0	5.6	9.0	ns
t_{SKD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$			0.55	1.5	ns
t_r	Rise Time		0.15	2.0	3.0	ns
t_f	Fall Time		0.15	0.9	3.0	ns
t_{PHZ}	Disable Time High to Z	R_L = 500Ω, C_L = 10 pF (*Figure 8* and *Figure 9*)	3.0	4.0	6.0	ns
t_{PLZ}	Disable Time Low to Z		3.0	4.5	6.0	ns
t_{PZH}	Enable Time Z to High		3.0	6.0	8.0	ns
t_{PZL}	Enable Time Z to Low		3.0	6.0	8.0	ns

AC Electrical Characteristics

T_A = −40˚C to +85˚C, V_{CC} = 5.0V ± 0.5V. (Note 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 10 pF (*Figure 2* and *Figure 3*)	2.0	3.3	6.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.0	3.3	5.0	ns
t_{SKD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$			0.6	1.0	ns
t_{TLH}	Transition Time Low to High		0.15	0.9	3.0	ns
t_{THL}	Transition Time High to Low		0.15	1.2	3.0	ns
t_{PHZ}	Disable Time High to Z	R_L = 100Ω, C_L = 10 pF (*Figure 4* and *Figure 5*)	1.5	3.5	7.0	ns
t_{PLZ}	Disable Time Low to Z		3.0	5.2	9.0	ns
t_{PZH}	Enable Time Z to High		2.0	4.5	7.0	ns
t_{PZL}	Enable Time Z to Low		2.0	4.5	7.0	ns
RECEIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 10 pF, VID = 200 mV (*Figure 6* and *Figure 7*)	3.0	6.0	8.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		3.0	5.6	8.0	ns
t_{SKD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$			0.7	1.6	ns
t_r	Rise Time		0.15	0.8	3.0	ns
t_f	Fall Time		0.15	0.8	3.0	ns
t_{PHZ}	Disable Time High to Z	R_L = 500Ω, C_L = 10 pF (*Figure 8* and *Figure 9*)	3.0	3.5	4.5	ns
t_{PLZ}	Disable Time Low to Z		3.5	3.6	7.0	ns
t_{PZH}	Enable Time Z to High		3.0	5.0	7.0	ns
t_{PZL}	Enable Time Z to Low		3.0	5.0	7.0	ns

Test Circuits and Timing Waveforms

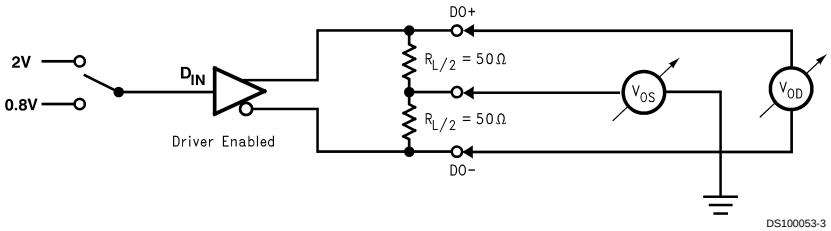


FIGURE 1. Differential Driver DC Test Circuit

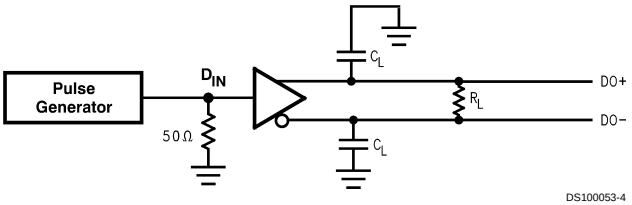


FIGURE 2. Differential Driver Propagation Delay and Transition Test Circuit

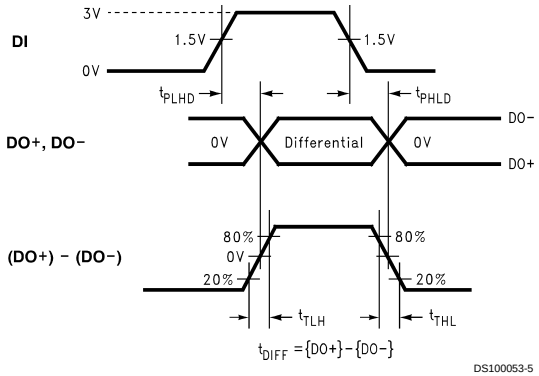


FIGURE 3. Differential Driver Propagation and Transition Time Waveforms

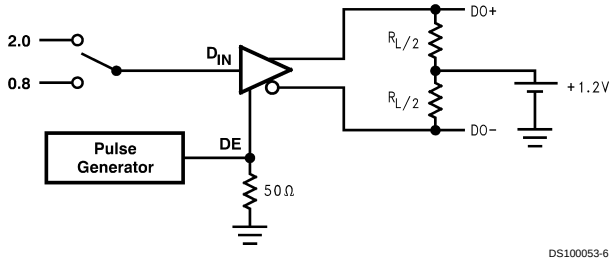


FIGURE 4. Driver TRI-STATE Delay Test Circuit

Test Circuits and Timing Waveforms (Continued)

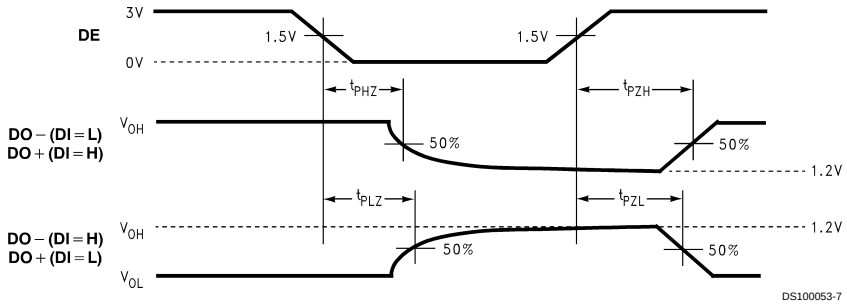


FIGURE 5. Driver TRI-STATE Delay Waveforms

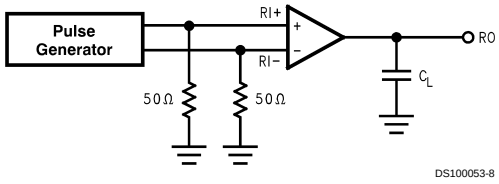


FIGURE 6. Receiver Propagation Delay and Transition Time Test Circuit

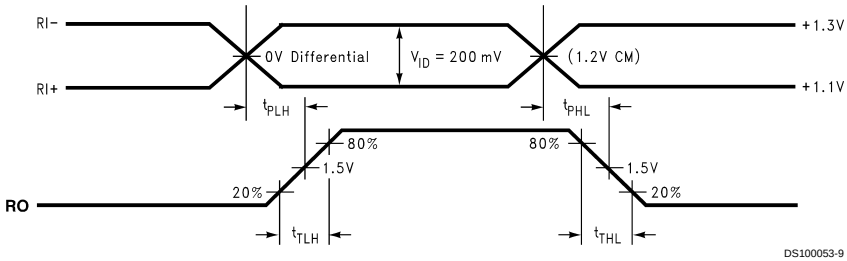


FIGURE 7. Receiver Propagation Delay and Transition Time Waveforms

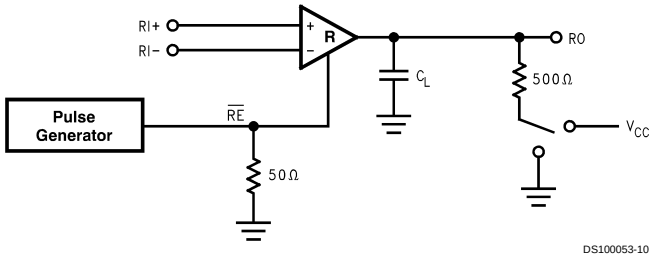


FIGURE 8. Receiver TRI-STATE Delay Test Circuit

Test Circuits and Timing Waveforms (Continued)

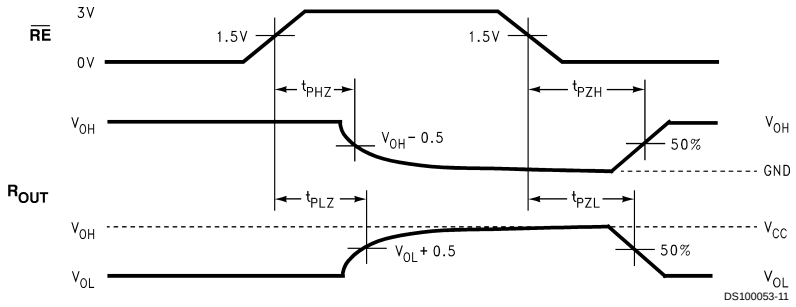


FIGURE 9. Receiver TRI-STATE Delay Waveforms TRI-STATE Delay Waveforms

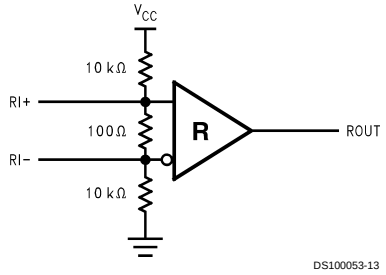
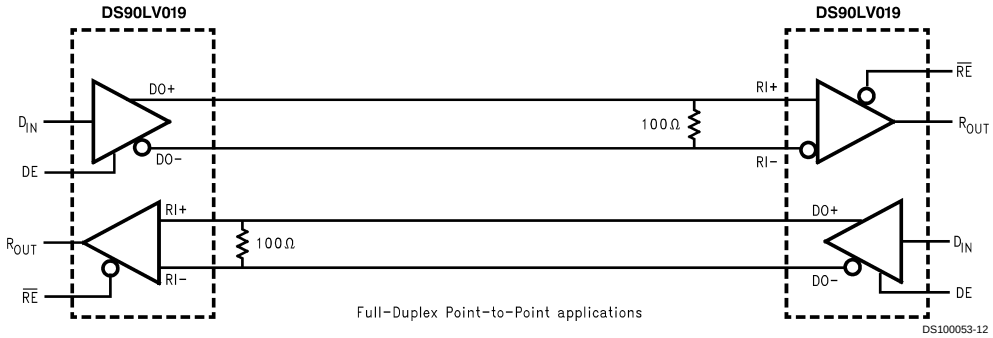


FIGURE 10. Terminated Input Fail-Safe Circuit

Typical Application Diagram



Applications Information

The DS90LV019 has two control pins, which allows the device to operate as a driver, a receiver or both driver and a receiver at the same time. There are a few common practices which should be implied when designing PCB for LVDS signaling. Recommended practices are:

- Use at least 4 PCB board layer (LVDS signals, ground, power and TTL signals).
- Keep drivers and receivers as close to the (LVDS port side) connector as possible.
- Bypass each LVDS device and also use distributed bulk capacitance. Surface mount capacitors placed close to power and ground pins work best. Two or three multilayer ceramic (MLC) surface mount capacitors 0.1 µF, and 0.01 µF in parallel should be used between each V_{CC} and ground. The capacitors should be as close as possible to the V_{CC} pin.
- Use controlled impedance traces which match the differential impedance of your transmission medium (i.e., Cable) and termination resistor.
- Use the termination resistor which best matches the differential impedance of your transmission line.
- Isolate TTL signals from LVDS signals.

MEDIA (CABLE AND CONNECTOR) SELECTION:

- Use controlled impedance media. The cables and connectors should have a matched differential impedance of about 100Ω.

Applications Information (Continued)

- Balanced cables (e.g., twisted pair) are usually better than unbalanced cables (ribbon cable, simple coax) for noise reduction and signal quality.
- For cable distances < 0.5m, most cables can be made to work effectively. For distances 0.5m ≤ d ≤ 10m, CAT 3 (category 3) twisted pair cable works well and is readily available and relatively inexpensive. For distances > 10m, and high data rates CAT 5 twisted pair is recommended.
- There are three Fail-Safe scenarios, open input pins, shorted inputs pins and terminated input pins. The first case is guaranteed for DS90LV019. A HIGH state on R_{OUT} pin can be achieved by using two external resistors (one to V_{CC} and one to GND) per *Figure 10* (Terminated Input Fail-Safe Circuit). R1 and R2 should be R_T to limit the loading to the LVDS driver . R_T is selected to match the impedance of the cable.

TABLE 1. Functional Table

MODE SELECTED	DE	$\overline{RE}$
DRIVER MODE	H	H
RECEIVER MODE	L	L
TRI-STATE MODE	L	H
FULL DUPLEX MODE	H	L

TABLE 2. Transmitter Mode

INPUTS		OUTPUTS	
DE	DI	DO+	DO−
H	L	L	H
H	H	H	L
H	2 > & > 0.8	X	X
L	X	Z	Z

X = High or Low logic state
Z = High impedance state
L = Low state
H = High state

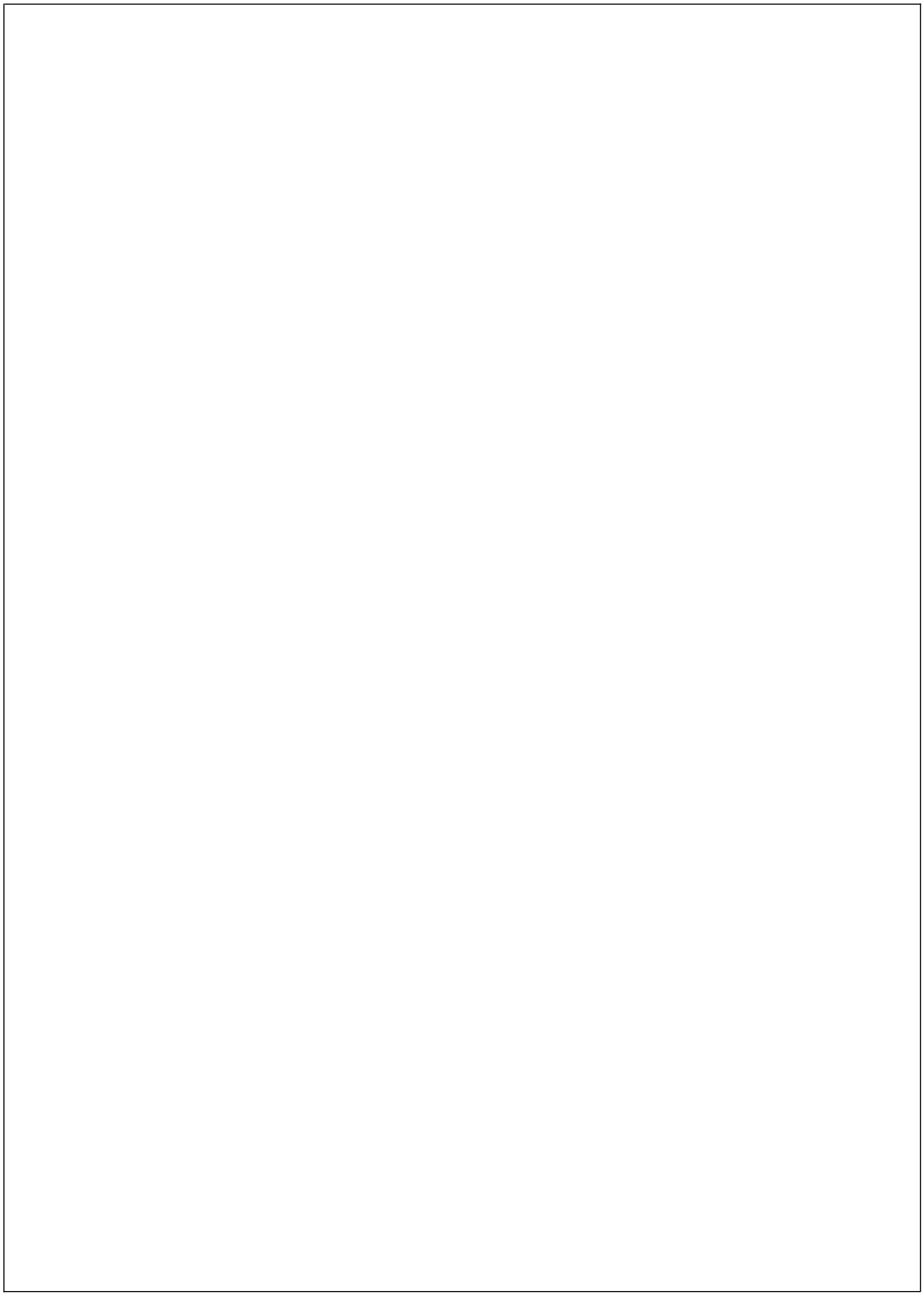
TABLE 3. Receiver Mode

INPUTS		OUTPUT
$\overline{RE}$	(RI+) − (RI−)	
L	L (< −100 mV)	L
L	H (> +100 mV)	H
L	100 mV > & > −100 mV	X
H	X	Z

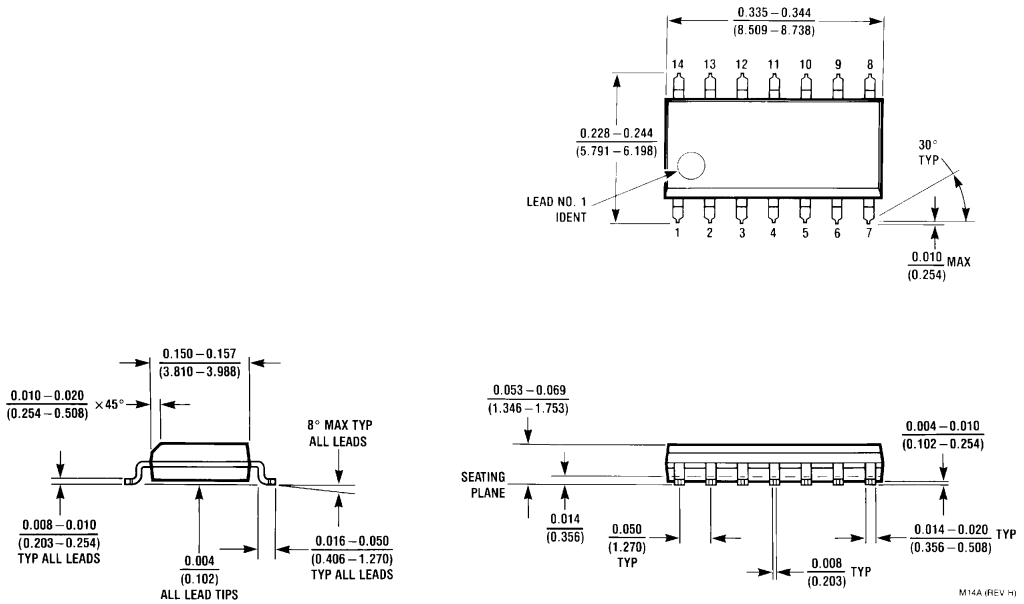
X = High or Low logic state
Z = High impedance state
L = Low state
H = High state

TABLE 4. Device Pin Description

Pin Name	Pin #	Input/Output	Description
D_{IN}	2	I	TTL Driver Input
DO±	11, 12	O	LVDS Driver Outputs
RI±	9, 10	I	LVDS Receiver Inputs
R_{OUT}	4	O	TTL Receiver Output
$\overline{RE}$	8	I	Receiver Enable TTL Input (Active Low)
DE	1	I	Driver Enable TTL Input (Active High)
GND	7	NA	Ground
V_{CC}	14	NA	Power Supply (3.3V ± 0.3V or 5.0V ± 0.5V)



Physical Dimensions inches (millimeters) unless otherwise noted



Order Number DS90LV019TM
NS Package Number M14A

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