QT OPTOELECTRONICS

HIGH-SPEED LOGIC-TO-LOGIC OPTOCOUPLERS

OPTOLOGIC™

LSTTL to

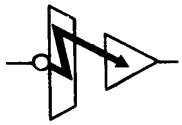
TTL BUFFER	74**OL**6000
TTL INVERTER	74**OL**6001
CMOS BUFFER	74**OL**6010
CMOS INVERTER	74**OL**6011

ORDER INFORMATION

PART NUMBER	LOGIC COMPATIBILITY		LOGIC FUNCTION	OUTPUT CONFIGURATION
	INPUT	OUTPUT		
74**OL**6000	LSTTL	TTL	BUFFER	TOTEM POLE
74**OL**6001	LSTTL	TTL	INVERTER	TOTEM POLE
74**OL**6010	LSTTL	CMOS	BUFFER	OPEN COLLECTOR
74**OL**6011	LSTTL	CMOS	INVERTER	OPEN COLLECTOR

SYMBOL

Buffer



Inverter

APPLICATIONS

- Transmission line interface—receiver and driver
- Excellent as bridged receiver in fast LAN highways
- Bus interface
- Logic family interface with ground loop noise elimination
- High speed AC/DC voltage sensing
- Driver for power semiconductor devices
- Level shifting
- Replaces fast pulse transformers

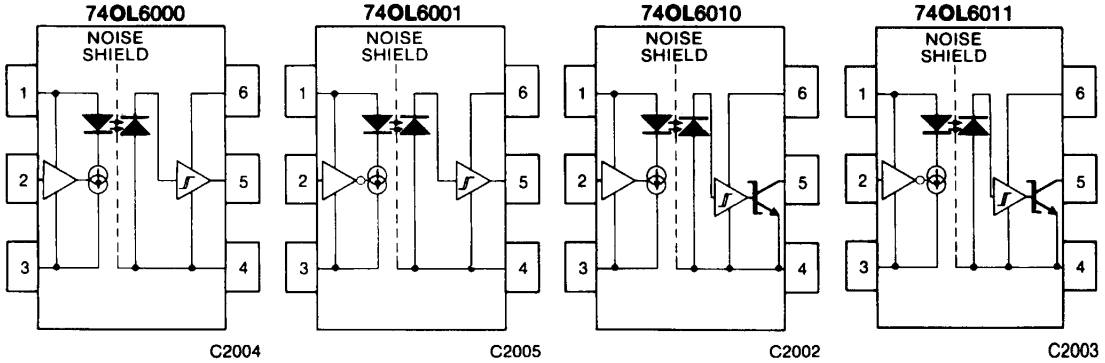
FEATURES

- Industry first LSTTL to TTL and LSTTL to CMOS complete logic-to-logic optocoupler
- Incorporates LED drive circuitry—use as logic gate
- Very high speed
- Choice of buffer or inverter
- Choice of TTL or CMOS compatible output up to 15 volts
- Fan-out of 10 TTL loads, fan-in 1 LSTTL load
- Internal noise shield—very high CMR of ±15 kV/μs
- Provides superior 5300 VRMS Withstand Test Voltage (WTV)—guarantees 480 VAC operation
- Compact 6-pin DIP
- UL recognized (File #E90700)
- Same noise immunity as LSTTL/TTL.

PIN CONFIGURATION

1–V_{CCI} (Input V_{CC})	6–V_{CCO} (Output V_{CC})
2–V_{IN} (Data in)	5–V_O (Data out)
3–GND_I (Input GND)	4–GND_O (Output GND)

EQUIVALENT CIRCUITS



LSTTL to TTL Buffer | LSTTL to TTL Inverter | LSTTL to CMOS Buffer | LSTTL to CMOS Inverter

OPTOELECTRONICS

HIGH-SPEED LOGIC-TO-LOGIC OPTOCOUPLERS

DESCRIPTION

OPTOLOGIC™ is the first family of truly logic compatible optically coupled logic interface gates.

The family consists of four device types offering LSTTL to TTL and LSTTL to CMOS interfacing. Each of these interfacing functions is available as a buffer (A=B), or as an inverter ($A=\overline{B}$).

The LSTTL input compatibility is provided by an input integrated circuit, with industry standard logic levels. This input amplifier IC switches a temperature compensated current source driving a high speed GaAsP/GaAs 700 nm LED emitter.

This novel integration scheme eliminates CTR degradation over time and temperature.

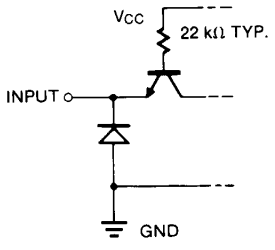
The emitter is optically coupled to an integrated photodetector/high-gain, high-speed output amplifier IC. The superior 15 kV/μs common-mode noise rejection is ensured through the use of an optically transparent noise shield.

The TTL compatible output has a totem-pole with a fan-out of 10. The CMOS compatible output has an open collector Schottky-clamped transistor that interfaces to any CMOS logic between 4.5 and 15 volts.

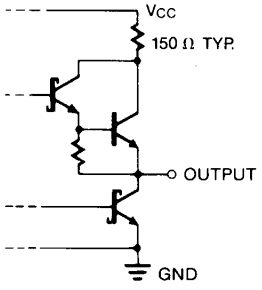
The 74**OL**6010/11 may also be used to drive power MOS FETS or transistors up to 15 volts.

The Optologic coupler family typically offers propagation of delays of 60 ns and can support 15 MBaud data communication.

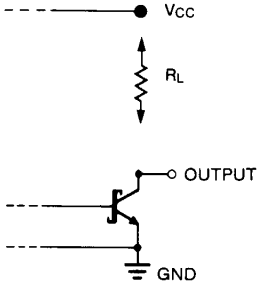
The two input chips and the output chip are assembled in a 6-pin DIP high insulation voltage plastic package. It provides a withstand test voltage of 5300 VRMS (1 minute), which is recognized as a working voltage of 480 VRMS.



LSTTL INPUT CIRCUIT
C2010
All Inputs



TTL OUTPUT CIRCUIT
C2009
74**OL**6000/01 Output



CMOS OUTPUT CIRCUIT
C2026
74**OL**6010/11 Output

ABSOLUTE MAXIMUM RATINGS 74OL6000/01

Storage temperature range	−55°C to +125°C
Operating temperature range	0°C to +70°C
Input supply voltage	7 V
Input voltage	7 V
Output supply voltage	7 V
Output voltage	7 V
Output current	40 mA
Power dissipation	350 mW
Lead temperature (soldering, 10 sec)	260°C

ABSOLUTE MAXIMUM RATINGS 74OL6010/11

Storage temperature range	−55°C to +125°C
Operating temperature range	0°C to +70°C
Input supply voltage	7 V
Input voltage	7 V
Output supply voltage	18 V
Output voltage	18 V
Output current	40 mA
Power dissipation	350 mW*
Lead temperature (soldering, 10 sec)	260°C

*See Fig. 12 for maximum allowable output supply voltage.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C Unless Otherwise Specified)

PARAMETER	SYM	MIN	TYP*	MAX	UNITS	TEST CONDITIONS 74OL6000	TEST CONDITIONS 74OL6001	TEST CONDITIONS 74OL6000/01	FIG.	NOTES
TTL OUTPUT 74OL6000/01										
Input supply voltage	V_{CCI}	4.5	5.0	5.5	V					1
Output supply voltage	V_{CCO}	4.5	5.0	5.5	V					1
High-level input voltage	V_{IH}	2.0			V					1
Low-level input voltage	V_{IL}			0.8	V					1
Input clamp voltage	V_{IK}			−1.2	V			V_{CCI}=4.5 V, I_I=−18 mA		1
High-level input current	I_{IH}		1.0	40.0	μA			V_{CCI}=5.5 V, V_{IH}=4.5 V		1
Low-level input current	I_{IL}		−200.0	−400.0	μA			V_{CCI}=5.5 V, V_{IL}=0.4 V		1
Input supply current (high)	I_{CCIH}		10.0	14.0	mA			V_{CCI}=5.5 V, V_{IN}=V_{IH}		1
Input supply current (low)	I_{CCIL}		10.0	14.0	mA			V_{CCI}=5.5 V, V_{IN}=V_{IL}		1
High-level output voltage	V_{OH}	2.4	3.0		V	V_{IN}=2.0 V	V_{IN}=0.8 V	V_{CCI}=4.5 V, V_{CCO}=4.5 V, I_{OH}=−400μA		1
Low-level output voltage	V_{OL}		0.3	0.6	V	V_{IN}=0.8 V	V_{IN}=2.0 V	V_{CCI}=4.5 V, V_{CCO}=4.5 V, I_{OL}=16 mA		1
				0.5	V			V_{CCI}=4.5 V, V_{CCO}=4.5 V, I_{OL}=4 mA		
High-level output current	I_{OH}		−8.0	−10.0	mA	V_{IN}=V_{IH}	V_{IN}=V_{IL}	V_{CCI}=4.5 V, V_{CCO}=4.5 V, V_{OH}=2.4 V		1
Low-level output current	I_{OL}	16.0			mA	V_{IN}=0.8 V	V_{IN}=2.0 V	V_{CCI}=4.5 V, V_{CCO}=4.5 V, V_{OL}=0.6 V		1
Short-circuit output current	I_{OS}	−5.0	−25.0	−40.0	mA	V_{IN}=V_{IH}	V_{IN}−V_{IL}	V_{CCI}=5.5 V, V_{CCO}=5.5 V		1
Output supply current (high)	I_{CCOH}		9.0	15.0	mA	V_{IN}=V_{IH}	V_{IN}=V_{IL}	V_{CCI}=5.5 V, V_O=V_{OH}, V_{CCO}=5.5 V		1
Output supply current (low)	I_{CCOL}		8.0	12.0	mA	V_{IN}=V_{IL}	V_{IN}=V_{IH}	V_{CCI}=5.5 V, V_O=V_{OL}, V_{CCO}=5.5 V		1

**All typical values are at T_A=25°C*

SWITCHING CHARACTERISTICS (T_A=25°C Unless Otherwise Specified)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	TEST CONDITIONS	FIG.	NOTES
TTL OUTPUT 74OL6000/01								
Propagation delay time for output low level	t_{PHL}		60	100	ns	V_{CCI}=5 V, V_{CCO}=5 V	15, 17	1
Propagation delay time for output high level	t_{PLH}		70	100	ns		15, 17	1
Output rise time for output high level	t_r		45		ns		15, 17	1
Output fall time for output low level	t_f		5		ns		15, 17	1

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C Unless Otherwise Specified)

PARAMETER	SYM	MIN	TYP*	MAX	UNITS	TEST CONDITIONS 74OL6010	TEST CONDITIONS 74OL6011	TEST CONDITIONS 74OL6010/11	FIG.	NOTES
CMOS OUTPUT 74OL6010/11										
Input supply voltage	V_{CCI}	4.5	5.0	5.5	V					1
Output supply voltage	V_{CCO}	4.5		15.0	V					1, 3
High-level input voltage	V_{IH}	2.0			V					1
Low-level input voltage	V_{IL}			0.8	V					1
Input clamp voltage	V_{IK}			−1.2	V			V_{CCI}=4.5 V, I_I=−18 mA		1
High-level input current	I_{IH}		1.0	40.0	μA			V_{CCI}=5.5 V, V_{IH}=4.5 V		1
Low-level input current	I_{IL}		−200.0	−400.0	μA			V_{CCI}=5.5 V, V_{IL}=0.4 V		1
Input supply current (high)	I_{CCIH}		10.0	14.0	mA			V_{CCI}=5.5 V, V_{IN}=V_{IH}		1
Input supply current (low)	I_{CCIL}		10.0	14.0	mA			V_{CCI}=5.5 V, V_{IN}=V_{IL}		1
Low-level output voltage	V_{OL}		0.4	0.6 0.5	V	V_{IN}=0.8 V	V_{IN}=2.0 V	V_{CCI}=4.5 V, V_{CCO}=4.5 V, I_{OL}=16 mA V_{CCI}=4.5 V, V_{CCO}=4.5 V, I_{OL}=4 mA		1
High-level output current	I_{OH}		1.0	100.0	μA	V_{IN}=V_{IH}	V_{IN}=V_{IL}	V_{CCI}=4.5 V, V_{OH}=15 V, V_{CCO}=4.5 −15 V		1
Low-level output current	I_{OL}	16.0			mA	V_{IN}=0.8 V	V_{IN}=2.0 V	V_{CCI}=4.5 V, V_{OL}=0.6 V, V_{CCO}=4.5 −15 V		1
Output supply current (high)	I_{CCOH}		9.0 11.0	12.0 18.0	mA	V_{IN}=V_{IH}	V_{IN}=V_{IL}	V_{CCI}=5.5 V, V_O=V_{OH}, V_CC_O=4.5 V V_{CCI}=5.5 V, V_O=V_{OH}, V_{CCO}=15 V		1
Output supply current (low)	I_{CCOL}		8.0 11.0	12.0 18.0	mA	V_{IN}=V_{IL}	V_{IN}=V_{IH}	V_{CCI}=5.5 V, V_O=V_{OL}, V_{CCO}=4.5 V V_{CCI}=5.5 V, V_O=V_{OL}, V_{CCO}=15 V		1

**All typical values are at T_A=25°C*

SWITCHING CHARACTERISTICS (T_A=25°C Unless Otherwise Specified)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	TEST CONDITIONS	FIG.	NOTES
TTL OUTPUT 74OL6010/11								
Propagation delay time for output low level	t_{PHL}		60	120	ns	V_{CCI}=5 V, V_{CCO}=5 V, R_L=470 Ω	15, 18	1
Propagation delay time for output high level	t_{PLH}		100	180	ns		15, 18	1
Output rise time for output high level	t_r		50		ns		15, 18	1
Output fall time for output low level	t_f		5		ns		15, 18	1

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C Unless Otherwise Specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS	FIG.	NOTES
74OL6000/01/10/11 Common mode transient immunity at logic high level output	CM_H	5000	15000		V/μs	V_{CCI}=5 V, V_{CCO}=5 V, V_{CM}=50 V_{P-P}	16, 19	
Common mode transient immunity at logic low level output	CM_L	−5000	−15000		V/μs		16, 19	
Common mode coupling capacitance	C_{CM}		0.005		pF			
Capacitance (input-output)	C_{I-O}		0.7		pF	V_{I-O}=0, f=1 MHz		2
Withstand insulation test voltage	V_{ISO}	5300			VRMS	T_A=25°C, t=1 min, I_{I-O} ≤ 1 μA		2
Insulation resistance	R_{ISO}		10^{11}		Ω	V_{I-O}=500 VDC		2

TYPICAL CHARACTERISTIC CURVES (T_A=25°C Unless Otherwise Specified)

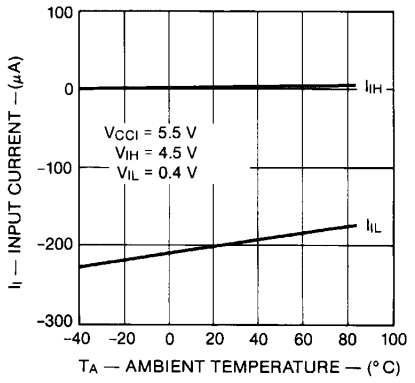


Fig. 1. Input Current vs. Ambient Temperature

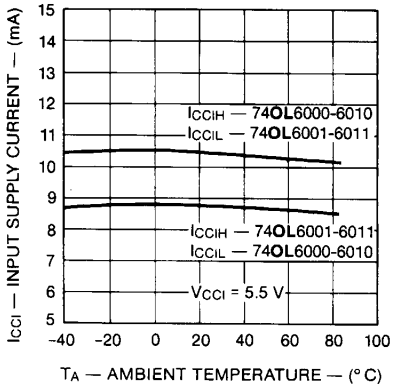


Fig. 2. Input Supply Current vs. Ambient Temperature

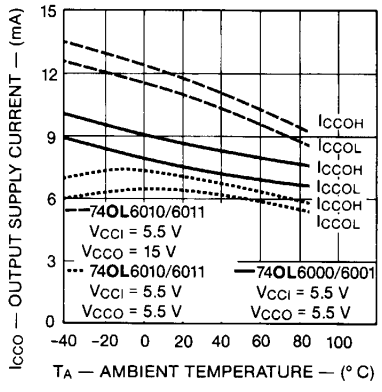


Fig. 3. Output Supply Current vs. Ambient Temperature

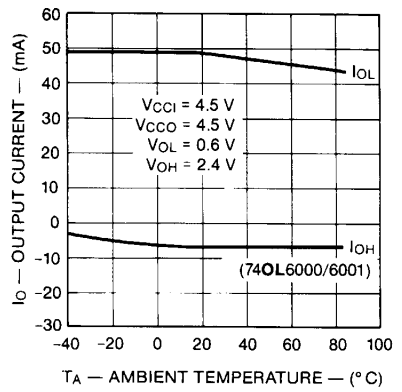


Fig. 4. Output Current vs. Ambient Temperature

TYPICAL CHARACTERISTIC CURVES (T_A=25°C Unless Otherwise Specified) (Cont'd)

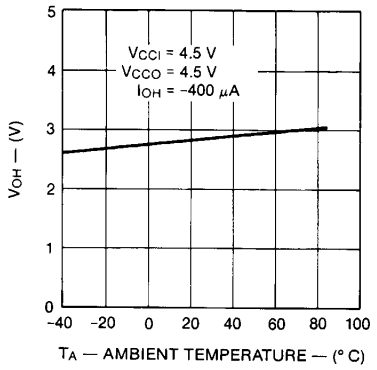


Fig. 5. High-Level Output Voltage vs. Ambient Temperature

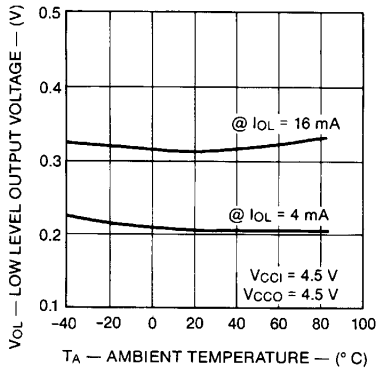


Fig. 6. Low-Level Output Voltage vs. Ambient Temperature

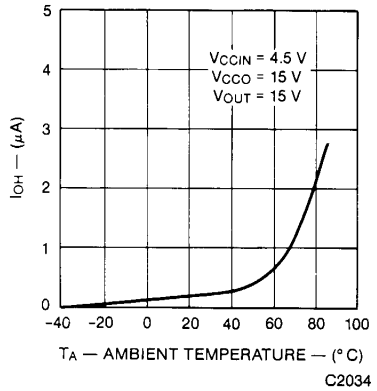


*Fig. 7. 74**OL**6010/11 Leakage Current vs. Ambient Temperature*

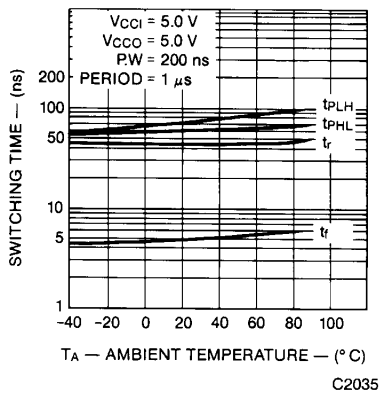


*Fig. 8. 74**OL**6000/01 Switching Times vs. Ambient Temperature*

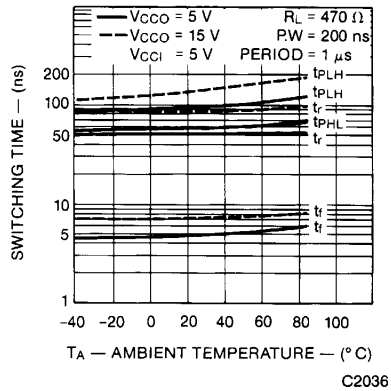


*Fig. 9. 74**OL**6010/11 Switching Times vs. Ambient Temperature*

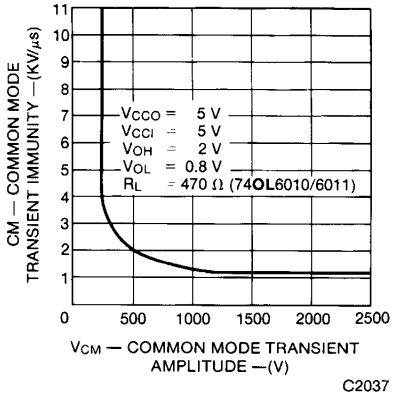


Fig. 10. Common Mode Rejection vs. Common Mode Voltage

TYPICAL CHARACTERISTIC CURVES (T_A=25°C Unless Otherwise Specified) (Cont'd)

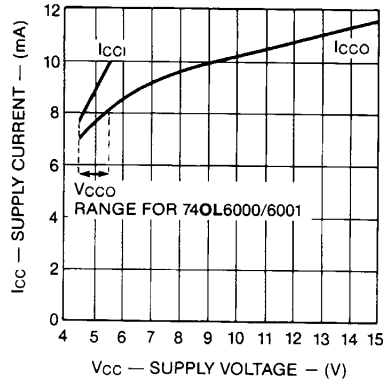


Fig. 11. Supply Current vs. Supply Voltage

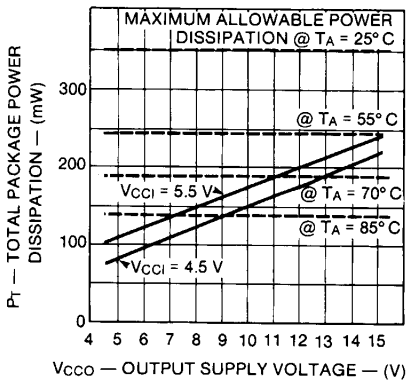


Fig. 12. Power Dissipation vs. Ambient Temperature

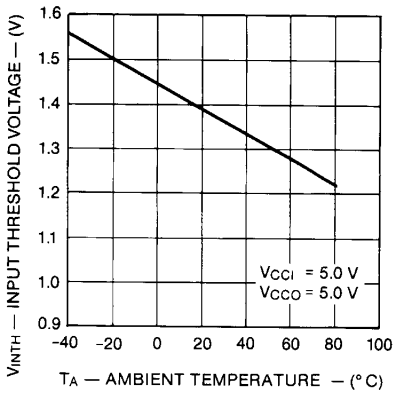


Fig. 13. Input Threshold Voltage vs. Ambient Temperature

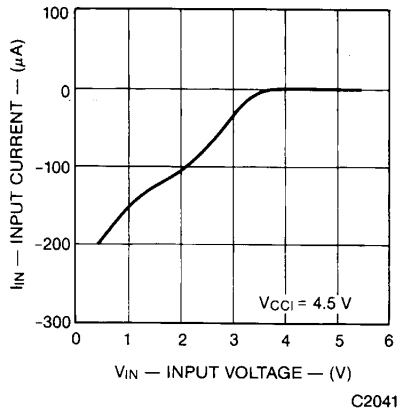


Fig. 14. Input Current vs. Input Voltage

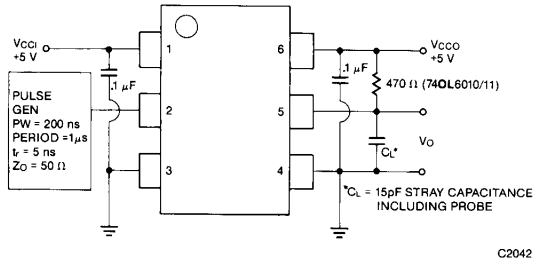


Fig. 15. Switching Time Test Circuit

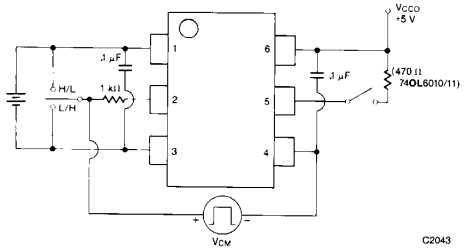


Fig. 16. Common Mode Rejection Test Circuit

TYPICAL CHARACTERISTIC CURVES (T_A=25°C Unless Otherwise Specified) (Cont'd)

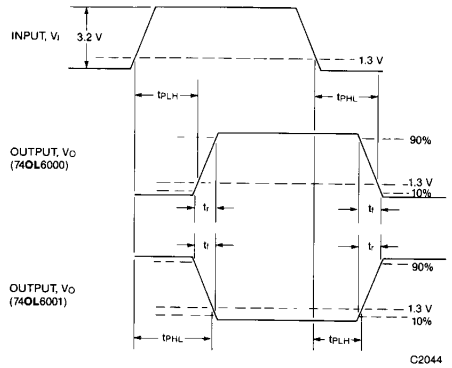


*Fig. 17. 74**OL**6000/01 Switching Times vs. Ambient Temperature*

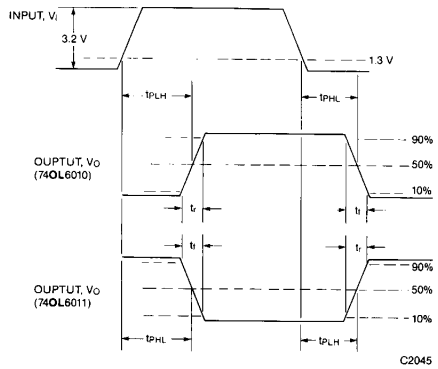
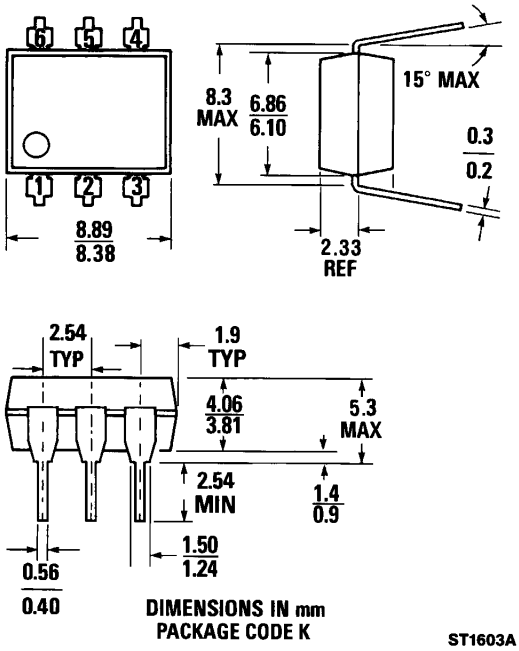


*Fig. 18. Switching Parameters 74**OL**6010/11*

PACKAGE DIMENSIONS



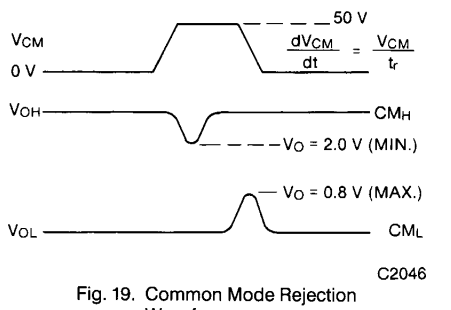


Fig. 19. Common Mode Rejection Waveforms

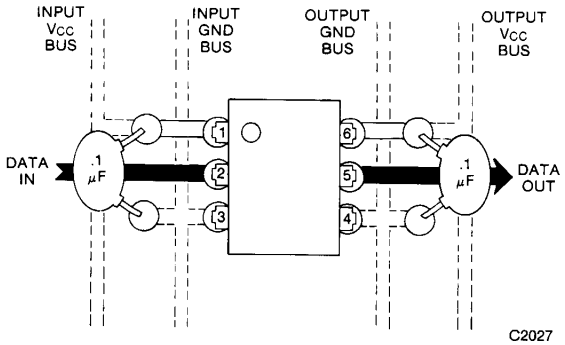
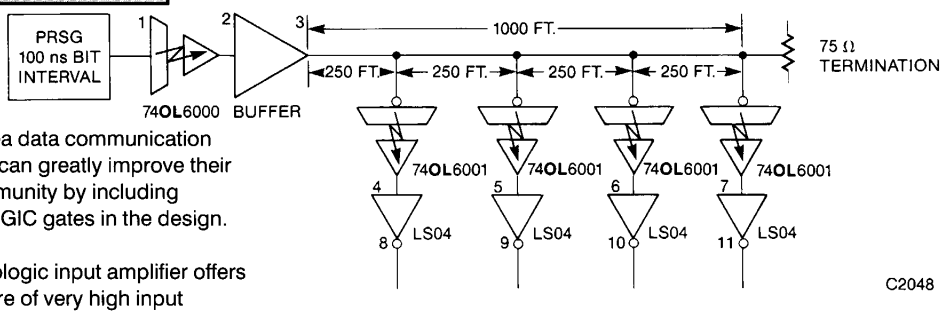


Fig. 20. Suggested PCB Lay-out

NOTES

1. *The V_{cco} and V_{cci} supply voltages to the device must each be bypassed by a 0.1 μf capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristics. Its purpose is to stabilize the operation of the high-gain amplifiers. Failure to provide the bypass will impair the DC and switching properties. The total lead length between capacitor and optocoupler should not exceed 1.5mm. See Fig. 20.*
2. *Device considered a two-terminal device: Pins 1, 2 and 3 shorted together, and Pins 4, 5 and 6 shorted together.*
3. *For example, assuming a V_{cci} of 5.0 V, and an ambient temperature of 70°C, the maximum allowable V_{cco} is 12.1 V.*

APPLICATION

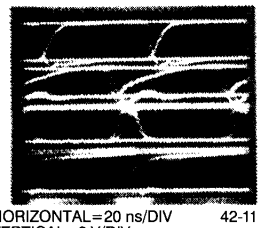


Local area data communication systems can greatly improve their noise immunity by including OPTOLOGIC gates in the design.

The Optologic input amplifier offers the feature of very high input impedance that permits their use as bridged line receivers. The system shown above illustrates an optically isolated transmitter and multidrop receiver system. The network uses a 74**OL**6000 and buffer (Figure D) to isolate the transmitter and drive the 75Ω coax cable. This application uses a 1000 ft. aerial suspension 75Ω CATV coax cable with data taps at 250 ft. intervals. The 74**OL**6001s function as bridged receivers, and as many as 30 receivers could be placed along the line with minimal signal degradation. The communication cable is terminated with a single 75Ω load at the far end of the line.

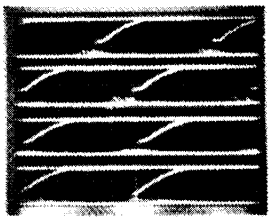
Signal quality "Eye Pattern" is shown in Figures A, B and C with a 10MBaud NRZ Psuedo-Random Sequence (PRS). Traces 1-3 in Figure A describes the transmitter section. Traces 4-7 in Figure B show the output of the four Optologic bridged terminations. Traces 8-11 in Figure C illustrate "Eye Pattern" as seen at the output of a 74LS04 logic gate. The data quality is well preserved in that only a 30% Eye closure is seen at the receiver located 1000 ft. from the transmitter.

The data communication system is completely optically isolated from all of the terminal equipments. Power for the transmitter (V_{cco}) and receiver (V_{cci}) is taken from an isolated power supply and distributed through a drain or messenger wire.



HORIZONTAL=20 ns/DIV 42-11
VERTICAL=2 V/DIV

Figure A



HORIZONTAL=20 ns/DIV 42-12,02
VERTICAL=2 V/DIV

Figure B

HORIZONTAL=20 ns/DIV 42-13,03
VERTICAL=2 V/DIV

Figure C

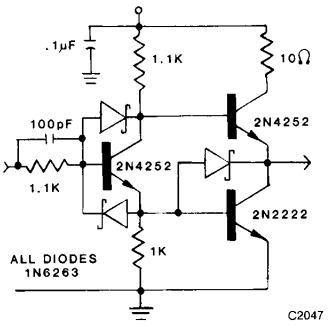


Figure D Buffer

NOTES

— All Optologic Gate Input and Output Amplifiers Bypassed With 0.1 μF Capacitors
— PRSG=Pseudo Random Sequence Generator
— 1 to 11 Refer To Testpoints; See Waveforms on Figs. A, B and C