Class 2 Bluetooth™ Module - F2M03AC2

Datasheet

Features

- Complete Bluetooth system including antenna
- No additional Bluetooth qualification needed
- Includes complete audio codec
- Available with complete Bluetooth software stack
- Headset functionality available.
- Possibility to work as a wireless UART without extra protocol.
- Serial interface, 8 digital and 2 analog I/O
- Analog and digital (PCM) voice interface for up to 3 simultaneous voice channels
- Nominal 20m range, transmit Power up to +4dBm
- Full Bluetooth data rate over UART and USB
- Low power modes
- Surface mountable, physical size: 24x13 mm
- Bluetooth v1.1 compliant

Applications

Prototyping and volume production of:

- Wireless Headsets
- Audio applications
- Industrial and Domestic Appliances
- Stand alone sensors
- Embedded systems
- Mobile Phones

General Description

This is a Class 2 surface mountable Bluetooth system. The module includes antenna and an audio codec for conversion between analog and digital voice. It is Bluetooth qualified as an end product i.e. no additional qualification needed.

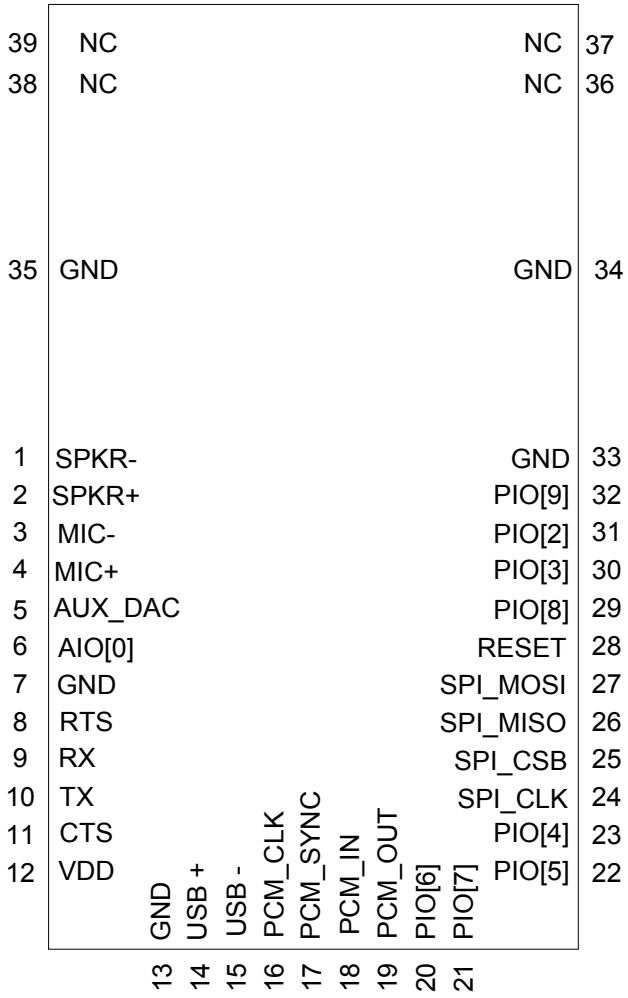
The module provides a fully compliant device for data and voice communications. The physical interfaces to a host (UART and USB) can support full Bluetooth data rate. An analog voice interface and a PCM digital audio interface are available. There are also digital and analog I/O and I^2C interfaces.

The module is available with a number of different firmware versions: The Wireless UART firmware is an embedded single processor solution that implements the Serial Port Profile (SPP). All data flows transparent through the serial port to the remote device. Using high level commands the user can configure the Bluetooth connection. Other firmware versions are: Headset, HID, HCI, RFCOMM and the possibility to get customized standalone applications implemented as an on chip solution.

Table of contents

1 Device pinout

(Top view)



2 Device terminal functions

Power supply	Pin	Pin type	Description
GND	7, 13, 33, 34, 35	VSS	Ground connections
NC	36,37,38,39	NC	Not connected, connect to unconnected pads to ensure mechanical robustness
VDD	12	VDD	Supply voltage 2.3V to 3.5V
Analog I/O	**Pin**	**Pin type**	**Description**
AUX_DAC	5	Analogue	Voltage DAC output
AIO(0)	6	Bi-directional	Programmable input/output line
Test and debug	**Pin**	**Pin type**	**Description**
RESET	28	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_MISO	26	CMOS output, tristatable with weak internal pull-down	Serial Peripheral Interface data output
SPI_CSB	25	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface active low
SPI_CLK	24	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	27	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
UART	**Pin**	**Pin type**	**Description**
UART_CTS	11	CMOS input with weak internal pull-down	UART clear to send active low
UART_TX	10	CMOS output	UART data output active high
UART_RTS	8	CMOS output, tristatable with internal pull-up	UART request to send active low
UART_RX	9	CMOS input with weak internal pull-down	UART data input active high
PCM	**Pin**	**Pin type**	**Description**
PCM_OUT	19	CMOS output, tristatable with weak internal weak pull down	Synchronous data output
PCM_SYNC	17	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_IN	18	CMOS input, with weak internal pull-down	Synchronous data input
PCM_CLK	16	Bi-directional with weak internal pull-down	Synchronous data clock
USB	**Pin**	**Pin type**	**Description**
USB_D+	14	Bi-directional	USB data plus with selectable internal 1_5k Q pull-up resistor
USB_D-	15	Bi-directional	USB data minus
PIO	**Pin**	**Pin type**	**Description**
PIO(2)	31	Bi-directional with programmable strength internal pull-up/down n	PIO
PIO(3)	30	Bi-directional with programmable strength internal pull-up/down n	PIO
PIO(4)	23	Bi-directional with programmable strength internal pull-up/down n	PIO
PIO(5)	22	Bi-directional with programmable strength internal pull-up/down n	PIO
PIO(6)	20	Bi-directional with programmable strength internal pull-up/down n	PIO
PIO(7)	21	Bi-directional with programmable strength internal pull-up/down n	PIO
PIO(8)	29	Bi-directional with programmable strength internal pull-up/down n	PIO
PIO(9)	32	Bi-directional with programmable strength internal pull-up/down n	PIO
Analog Audio	**Pin**	**Pin type**	**Description**
MIC+	4	Analogue input	Microphone input positive
MIC-	3	Analogue input	Microphone input negative
SPKR+	2	Analogue output	Speaker output positive
SPKR-	1	Analogue output	Speaker output negative

3 Electrical characteristics

Absolute Maximum Ratings

Rating	Min	Max
Storage Temperature	-40°C	+150°C
Supply voltage	-0.40V	3.60V

Recommended Operating Conditions

Operating condition	Min	Max
Operating Temperature Range	-40°C	+85°C
Supply voltage	2.3 V	3.5 V

Input/Output Terminal Characteristics

Digital Terminals	Min	Typ	Max	Unit
Input Voltage Levels				
V_{IL} input logic level low (2.7 ≤ VDD ≤ 3.5)	-0.4	-	+0.8	V
V_{IL} input logic level low (2.3 ≤ VDD < 2.7)	-0.4	-	+0.4	V
V_{IH} input logic level high	0.7VDD	-	VDD+0.4	V
Output Voltage Levels				
V_{OL} output logic level low (2.7 ≤ VDD ≤ 3.5) (I_O = 4.0mA)	-	-	0.2	V
V_{OL} output logic level low (2.3 ≤ VDD < 2.7)) (I_O = 4.0mA)	-	-	0.4	V
V_{OH} output logic level high (2.7 ≤ VDD ≤ 3.5) (I_O = -4.0mA)	VDD-0.2	-	-	V
V_{OH} output logic level high (2.3 ≤ VDD < 2.7) (I_O = -4.0mA)	VDD-0.4	-	-	V
Input and Tristate Current				
Strong pull-up	-100	-40	-10	µA
Strong pull-down	10	40	100	µA
Weake pull-up	-5	-1	0	µA
Weak pull-down	0	1	5	µA
I/O pad leakage current	-1	0	1	µA
CI Input capacitance	1.0	-	5.0	pF
USB Terminals (1)	**Min**	**Typ**	**Max**	**Unit**
Input threshold				
V_{IL} input logic level low	-	-	0.3VDD	V
V_{IH} input logic level high	0.57VDD	-	-	V
Input leakage current				
GND < V_{IN} < VDD (2)	-1	1	5	µA
CI Input capacitance	2.5	-	10.0	pF
Output levels to correctly terminated USB Cable				
V_{OL} output logic level low	0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD	V

Input/Output Terminal Characteristics (Continued)

Auxiliary DAC, 8-bit resolution	Min	Typ	Max	Unit
Resolution	-	-	8	Bits
Average output step size [3]	12.5	14.5	17.0	mV
Output Voltage		Monotonic [3]		
Voltage range	GND	-	VDD	V
Current range	-10.0	-	+0.1	mA
Minimum output voltage (I_O=100µA)	0.0	-	0.2	V
Maximum output voltage (I_O=10mA)	VDD-0.3	-	VDD	V
High Impedance leakage current	-1	-	1	µA
Offset	-220	-	+120	mV
Integral non-linearity [3]	-2	-	+2	LSB
Starting time (50pF load)	-	-	10	µS
Settling time (50pF load)	-	-	5	µS
Audio CODEC, 15-Bit Resolution (MIC and SPKR pins)	**Min**	**Typ**	**Max**	**Unit**
Microphone Amplifier				
Input full scale at maximum gain	-	3	-	mV rms
Input full scale at minimum gain	-	380	-	mV rms
Gain resolution	-	3	-	dB
Gain range		42	-	dB
Input Impedance (Microphone input)	-	20	-	kΩ
Input Impedance (Line input)	-	130	-	kΩ
Speaker Driver				
Gain Resolution	-	3	-	dB
Gain range	-	21	-	dB
Maximum output level (high impedance loads)	-	700	-	mV rms
Maximum output level (low impedance loads)	-	20	-	mA
Allowed load: resistive	8	-	OC	Ω
Allowed load: capacitive	-	-	500	pF

Notes:
VDD are at 3.0V unless shown otherwise. Current drawn into a pin is defined as positive, current supplied out of a pin is defined as negative.

[1] $3.1 \leq VDD \leq 3.5V$
[2] Internal USB pull-up disabled
[3] Specified for an output voltage between 0.2V and VDD-0.3V

Average current consumption
VDD = 3.3V Temperature = 20 °C
Measured using Wireless UART firmware.

Slave:

Mode	Average (mA)
No connection (default settings)	2,1
No connection (inquiry scan disabled)	1,7
Connected (Short range), no data transfer	28
Connected (Short range), no data transfer Sniff mode 200 ms interval	3,4
Connected (Short range), no data transfer Park mode 200 ms interval	1,6
Connected, (Short range) 115.2 kbit/s master to slave	37
Connected, (Short range) 115.2 kbit/s slave to master	37
Connected, (Short range) 115.2 kbit/s slave to master Sniff mode 125 ms interval	28
Connected, (Short range) 115.2 kbit/s master to slave Sniff mode 125 ms interval	25
Connected, (Long range) 115.2 kbit/s master to slave	46

Master:

Mode	Average (mA)
No connection (default settings)	53
Connected (Short range), no data transfer	5,6
Connected (Short range), no data transfer Sniff mode 200 ms interval	2,6
Connected (Short range), no data transfer Park mode 200 ms interval	2,7
Connected, (Short range) 115.2 kbit/s master to slave	24,6
Connected, (Short range) 115.2 kbit/s full duplex	31
Connected, (Long range) 115.2 kbit/s full duplex	
Connected, (Short range) 115.2 kbit/s slave to master Sniff mode 125 ms interval	29
Connected, (Short range) 115.2 kbit/s slave to master Sniff mode 125 ms interval	17

Peak current consumption
VDD = 3.3V Temperature = 20 °C

Mode	Typ	Unit
Peak consumption during RF peaks	85	mA

Deep sleep leakage current
VDD = 3.3V Temperature = 20 °C

Mode	Typ	Unit
Deep sleep	55	µA

Radio Characteristics

VDD = 3.0V Temperature = 23 °C Frequency = 2.441GHz

Specification	Min	Typ	Max	Bluetooth specification	Unit
Maximum RF transmit power	-	3.9	4	-6 to +4 (Class2)	dBm
RF power control range (1)	-	24	-	≥16	dB
Sensitivity at 0.1% BER (1)	-	-85	-	≤-70	dBm

4 Firmware versions

F2M03 is supplied with Bluetooth stack firmware, which runs on the internal RISC micro controller of the Bluetooth module. This chapter includes an overview of the different options for more in depth information please use separate firmware datasheets provided by Free2move.

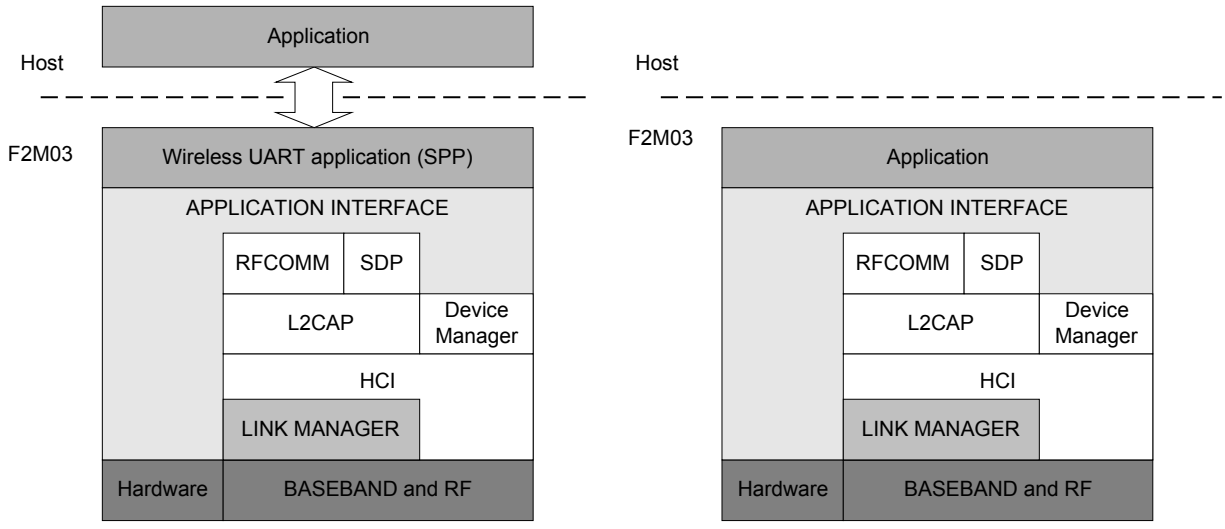
All firmware versions are compliant with the Bluetooth specification v1.1. The F2M03 software architecture allows Bluetooth processing to be shared between the internal micro controller and a host processor. Depending on application the upper layers of the Bluetooth stack (above HCI) can execute on-chip or on the host processor.

Running the upper stack on F2M03 module reduces (or eliminates, in the case of a on module application) the need for host-side software and processing time.

The integration approach depends on the type of product being developed. For example, performance will depend on the integration approach adopted. In general Free2move offers four categories of Bluetooth stack firmware:

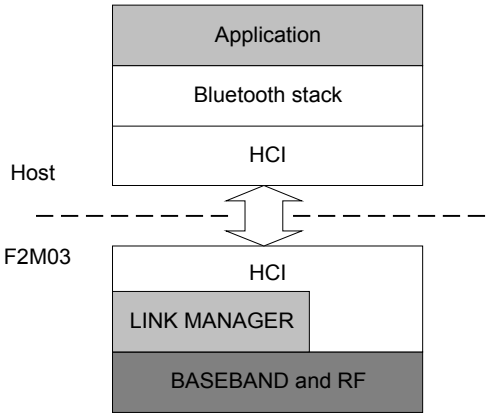
- Wireless UART; offers a transparent interface to the Bluetooth channel. There is no need for additional drivers or Bluetooth software on the host.
- Embedded module solutions offer an application to run on the module. There is no need for an external host (E.g a Bluetooth headset).
- Two-processor solution involving a host and host controller, where the higher layers of the Bluetooth stack has to be implemented on the host.
- Two-processor embedded solution offers a host with limited resources to gain access to a Bluetooth stack, with the higher layers on-chip, via a special API.

The protocol layer models for the different Bluetooth stack firmware categories can be represented as shown in the figures below.

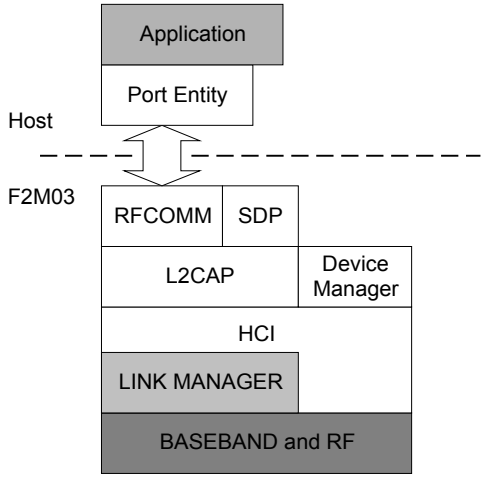


Wireless UART

Embedded single-processor architecture



HCI, (Two-Processor Architecture)



RFCOMM, (Embedded Two-Processor Architecture)

Wireless UART

Free2move's Wireless UART (WU) firmware is intended to replace the cable(s) connecting portable and/or fixed electronic devices. Key features are robustness, high configurability, high security, low complexity and low power. The WU firmware is compliant with the Bluetooth Serial Port Profile (SPP) for setting up emulated serial cable connections between connected devices. There is no additional need for drivers or an external host with Bluetooth software when using the WU firmware. When a successful Bluetooth connection is established the data channel and the voice channel can be used simultaneously or separately. All information sent/received at the data/voice interface of the WU unit is exchanged transparently via Bluetooth with the connected remote device.

Embedded Solution
This version of the stack firmware requires no host processor. All software layers, including application software, run on the internal RISC processor in a protected user software execution environment.

The embedded solution can be used for a single chip Bluetooth product. One example is a cordless headset. However this solution is equally applicable to any small wireless device that would benefit from a single processor solution.

Free2move offers the following single chip solutions:

- Headset
- Human Interface Device (Mouse, keyboard etc)
- Onboard application (development of customer specific applications)

HCI (Standard Two-Processor Solution)
For the standard two-processor solution, where the split between higher and lower layers of the stack takes place at the HCI, a complete Bluetooth stack is needed in the external host. It is often preferable to use this solution when the host is a personal computer of some description. However, in general this category can include any computing platform with communications capability that is not resource limited.

Free2move can offer a host stack solution usable for different versions of Microsoft Windows.

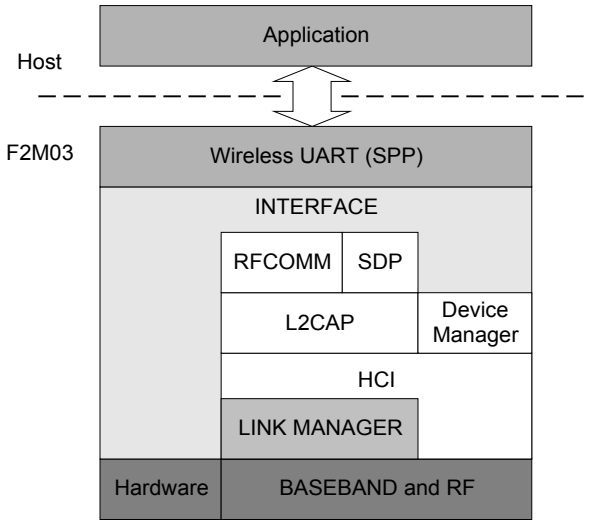
RFCOMM (Embedded Two-Processor Solution)
The embedded two-processor category is a feature of the F2M03 module. This allows products to be designed that incorporate Bluetooth, where the host is resource limited and cannot support the addition of the Bluetooth functionality.

4.1 Wireless UART

4.1.1 General Information

Free2move's Wireless UART (WU) firmware is intended to replace the cable(s) connecting portable and/or fixed electronic devices. Key features are robustness, high configurability, high security, low complexity and low power.

The WU firmware is compliant with the Bluetooth Serial Port Profile (SPP) for setting up emulated serial cable connections between connected devices. There is no additional need for drivers or an external host with Bluetooth software when using the WU firmware.



Wireless UART architecture

The WU application runs on top of an embedded Bluetooth v1.1 compliant stack, including protocols up to the RFCOMM layer. Point-to-point connections are supported. This means that a unit running WU can be either a master of one unit or participate in a piconet as a slave.

The WU firmware offers one asynchronous data channel and one synchronous voice channel, both channels capable of full duplex transmission.

When a successful Bluetooth connection is established the data channel and the voice channel can be used simultaneously or separately. All information sent/received at the data/voice interface of the WU unit is exchanged transparently via Bluetooth with the connected remote device.

The WU unit is set to operate in a default mode that allows the user to communicate via the asynchronous data channel over Bluetooth, as soon as a successful connection has been established. This can be achieved without sending any configuration commands to the WU firmware. However, as long as there is no Bluetooth connection established, it is possible to configure the WU firmware via commands (described in detail in the separate Wireless UART datasheet) sent on the data interface.

4.1.2 General I/O

General I/O interfaces are used for different purposes between the WU firmware and the Host:

- Asynchronous data interface – configuration of the WU firmware or exchange transparent digital information between the connected Bluetooth devices.
- Synchronous voice interface – exchange transparent voice information between the connected Bluetooth devices.
- Bluetooth connectivity PIO interfaces – indication and disconnection of the established Bluetooth connection.
- Emulate serial handshaking PIO lines interface – DTE or DCE serial handshake emulation between the connected Bluetooth devices.

UART interface (Asynchronous data and configuration):

UART	Signal Direction	Active (TTL)	Description
TX	Output	High	UART transmit data
RX	Input	High	UART receive data
RTS	Output	Low	UART request to send
CTS	Input	Low	UART clear to send

Voice interface:

CODEC I/O	Signal Direction	Description
MIC_P	Input (analogue)	Microphone input positive
MIC_N	Input (analogue)	Microphone input negative
AUX_DAC	Output (analogue)	Microphone input bias
SPKR_P	Output (analogue)	Speaker output positive
SPKR_N	Output (analogue)	Speaker output negative

PIO are used to control/monitor the Bluetooth connectivity of the WU firmware.

PIO	Signal Direction	Active (TTL)	Description
2	Input	High	Request to close the current Bluetooth connection to the remote device.
3	Output	High	Indicates that a successful Bluetooth connection is established with a remote device.

To prevent connections or to close the current Bluetooth connection PIO[2] can be set high.

PIO[3] is held low as long as there is no Bluetooth connection. As soon as a successful Bluetooth connection has been established with a remote device, PIO[3] goes high.

PIO can also be used to emulate serial handshaking lines between the connected Bluetooth devices (F2M03 only). Emulation can either be DTE or DCE

Emulated Signal	PIO	Signal Direction Emulate DTE	Signal Direction Emulate DCE	Active (TTL)
RI	4	Input	Output	High
DTR	5	Output	Input	High
DCD	6	Input	Output	High
DSR	7	Input	Output	High

While the handshaking lines are transparent to the data channel these I/O may also be used to transfer digital signals between to Free2movve devices running WU

4.1.3 Settings

The default settings allow the user to communicate via Bluetooth, without sending any configuration commands, as soon as a successful connection has been established. Information sent and received on the serial interface of the WU unit at 38400 bps is transmitted transparently between the two connected devices. The default settings are valid as long as the user has made no configuration.

When there is no Bluetooth connection established it is possible to configure the WU firmware via commands sent on the serial interface. All settings changed by the user are stored in persistent memory.

The following serial settings are used for configuration mode and are not configurable:

Parameter	Default Value
Baud rate	38400
Data bits	8
Parity	None
Stop bits	1
Hardware flow control	On

To be able to send commands to the Wireless UART firmware, it must be set in *Host Controlled Mode* (HCM). As previously described the Wireless UART firmware can only enter HCM when no Bluetooth connection is established.

Once entered HCM there are several commands that can be issued:

- Configuration commands
- Software / Hardware reboot
- Inquiry (search for Bluetooth devices in the neighborhood)
- Pairing (device security - authentication and encryption)
- Advanced configuration commands
- SCO commands
- Information commands
- Control commands

Configuration Commands

There are several settings stored in the Wireless UART firmware that can be read and modified by using the configuration commands.

Examples of these settings are:

- Local Bluetooth name
- Local SDP-service name
- Operating mode
- Serial port settings
- Bluetooth security settings (authentication, encryption)

There are two normal operating modes:

- Connecting mode – Bluetooth master
- Endpoint mode – Bluetooth slave

In Connecting mode the Wireless UART firmware will continuously try to establish a Bluetooth connection to a specified remote Bluetooth device in the neighborhood (Bluetooth master).

In Endpoint mode the Wireless UART firmware may accept connections from remote Bluetooth devices. A connection request will be accepted when the specified rules are fulfilled (Bluetooth slave).

Software / Hardware Reboot

This option gives the ability to be able to reboot the module via software commands.

Inquiry

Search for other Bluetooth devices in the neighborhood.

There are three configuration parameters:

- How many seconds the search should be active
- A filter, used when searching for devices of as certain class
- The possibility to include the Bluetooth name of the discovered devices

Pairing

When authentication is enabled, the devices must be paired before a successful connection can be established.

The Wireless UART firmware can either initiate pairing with a remote device or accept pairing requests.

During a pairing PIN codes are exchanged between the local and remote device. A successful pairing requires identical PIN codes. The result of the pairing attempt will be returned to the Host. If pairing was successful, a unique link key has been generated and saved in non-volatile memory. The link key is used in the connection establishment procedure for secure verification of the relationship between the paired devices.

The Wireless UART firmware allows the user to be paired with one device at a time. The last pin code entered and link key generated are saved.

Advanced configuration

Includes among others commands for enabling power save modes (sniff/park), fine tune performance, enabling modem emulation and changing transmit power.

SCO commands

Makes it possible to establish full duplex voice connections between two WU units.

4.1.4 Performance

The WU firmware is a complete on-chip application; limited resources restrict the maximum throughput. The table below shows the maximum achieved throughput when streaming data between two connected WU v3.00 devices at close range.

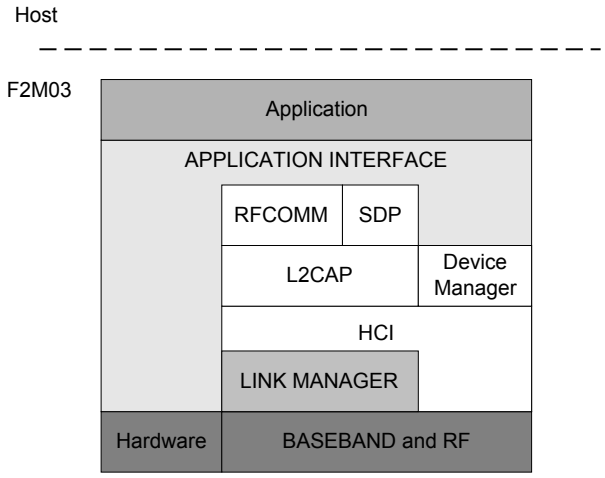
Direction	Baud Rate	Maximum Throughput (kbit/s (throughput mode))	Maximum Throughput (kbit/s) (latency mode)
Master to Slave	57600	~57.6	~57.6
Slave to Master	57600	~57.6	~57.6
Full duplex	57600	~57.6	~50.5
Master to Slave	115200	~115.1	~93.9
Slave to Master	115200	~115.1	~79.6
Full duplex	115200	~114.5	~42.0
Master to Slave	230400	~223.1	~158.0
Slave to Master	230400	~221.4	~117.7
Full duplex	230400	~172.7	~86.2
Master to Slave	460800	~228.6	~206.7
Slave to Master	460800	~222.7	~154.1
Full duplex	460800	~173.3	~109.8
Master to Slave	921600	~240.1	~235.7
Slave to Master	921600	~235.4	~186.0
Full duplex	921600	~174.7	~150.5

4.1.5 Configuration software

When purchasing the Free2move Bluetooth evaluation kit, a Windows application than can be used to configure your Wireless UART modules is included.

4.2 Onboard application

When using the onboard application firmware option no external host processor is needed. All software layers, including application software, run on the internal RISC processor. The application runs in a protected user software execution environment known as a Virtual Machine (VM).



Embedded Single-Processor Architecture

Free2move provides the service to implement he user specified functionality on the Bluetooth module. The application software will execute together with the Bluetooth stack firmware on-chip. The application is able to make calls to the firmware for various operations.

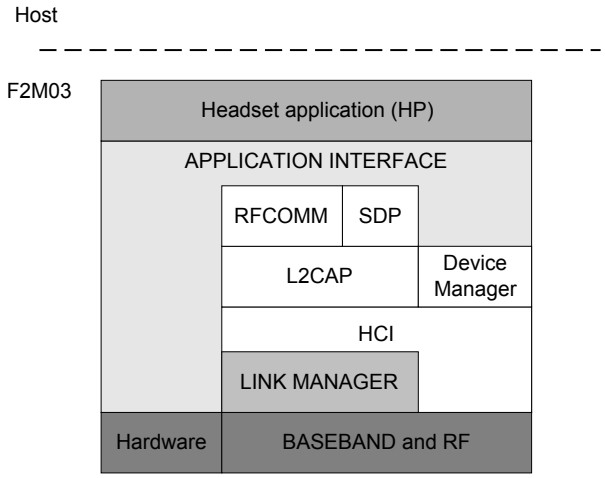
The execution environment is structured so the user application does not adversely affect the stack software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the user is able to get specific applications such as a cordless headset or other profiles without the requirement of a host controller.

4.3 Headset

Headset functionality is one implementation of the onboard application possibility. The Free2move headset firmware is available in a standard version, which is implemented to be adaptable to fit your specific requirements and needs. Adaptations may include the user interface as buttons and LEDs, but also more advanced functionality changes.

The headset firmware provides the functionality required as stated in Bluetooth Profiles Specification, volume 2, v1.1, 22 February 2001, Part K6 for a Bluetooth headset. It provides the headset part of that functionality.



Embedded Single-Processor Architecture

Headset Buttons Additional Functionality to Headset Profile

The firmware extends the standard headset functionality with the following features:

- Remote audio volume control (listed as optional in the profile)
- Park mode supported (listed as optional in the profile)
- Sniff mode supported (not listed in the profile)
- Muting of microphone under headset control (not listed in the profile)
- Playing of arbitrary tones (not listed in the profile)

Three buttons are used by the standard Headset firmware implementation:

PIO	Signal Direction	Active (TTL)	Description
7	Input	High	Talk button (Answer and initiate calls)
4	Input	High	Volume Up
5	Input	High	Volume Down

LED

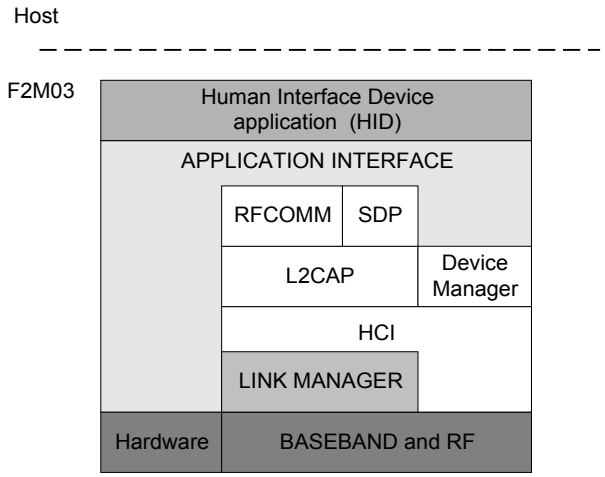
PIO	Signal Direction	Active (TTL)	Description
2	Output	High	Used for indicate connection state
3	Output	High	Used for indicate paring mode

Other I/O

PIO	Signal Direction	Active (TTL)	Description
6	Input	High	ON/OFF (The headset to goes into deep sleep)
TBD	Output	High	CODEC, Is driven high to enable the codec and low to power it down (Not needed in F2M03AC2, may instead be used to bias the microphone)

4.4 Human Interface Device

Human Interface Device (HID) functionality is one implementation of the onboard application possibility. The Free2move HID firmware is available in a standard version, which is implemented to be adaptable to fit your specific requirements and needs.

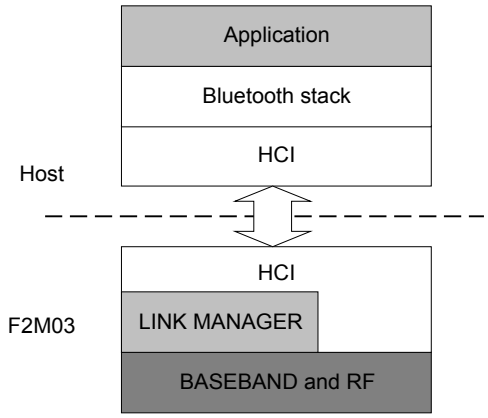


Embedded Single-Processor Architecture

The HID I/O component in the HID firmware controls low latency data acquisition from external sensor hardware. Supported external sensors include 5 mouse buttons, the Agilent ADNS-2030 optical sensor, quadrature scroll wheel, direct coupling to a keyboard matrix and a UART interface to custom hardware.

4.5 HCI

In this implementation the internal processor of the module runs the Bluetooth stack up to the Host Controller Interface (HCI) as specified in the Bluetooth specification V1.1. The external host processor must provide all upper Bluetooth stack layers.



Standard Two-Processor Architecture

4.5.1 Standard Bluetooth Functionality

The firmware has been written against the Bluetooth Core Specification v1.1.

- Bluetooth components: Baseband (including LC), LM and HCI
- Standard USB (v1.1) and UART (H4) HCI Transport Layers
- All standard radio packet types
- Full Bluetooth data rate, up to 723.2 kb/s asymmetric(1)
- Operation with up to seven active slaves(1)
- Operation with up to three SCO links, routed to one or more slaves
- Maximum number of simultaneous active ACL connections: 7(2)
- Maximum number of simultaneous active SCO connections: 3(2)
- Role switch: can reverse Master/Slave relationship
- All standard SCO voice codings, plus “transparent SCO”
- Standard operating modes: Page, Inquiry, Page-Scan and Inquiry-Scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including “Forced Hold”
- Dynamic control of peers’ transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate (CQDDR)
- All standard Bluetooth Test Modes
- Standard firmware upgrade via USB (DFU)

Note:
(1)Maximum allowed by Bluetooth specification v1.1.
(2)F2M03 supports all combinations of active ACL and SCO channels for both Master and Slave operation, as specified by the Bluetooth specification v1.1.

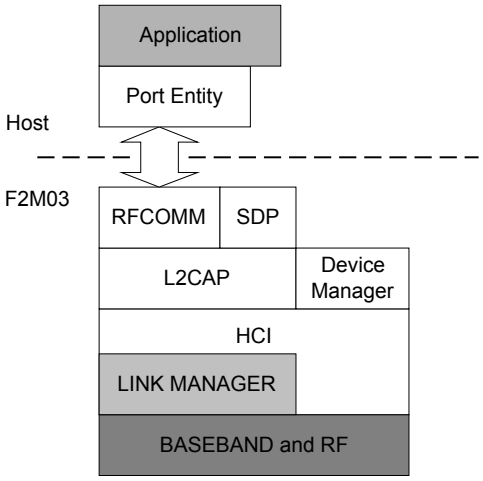
4.5.2 Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BlueCore Serial Protocol (BCSP) - a proprietary, reliable alternative to the standard Bluetooth (H4) UART Host Transport.
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set (called BCCMD – "BlueCore Command") provides:
  - Access to the module's general-purpose PIO port
  - Access to the module's Bluetooth clock - this can help transfer connections to other Bluetooth devices.
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
  - Controls to set the default and maximum transmit powers - these can help to reduce interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Radio transmitter enable/disable - a simple command connects to a dedicated hardware switch that determines whether the radio can transmit.
- The firmware can read the voltage on a pair of the module's external pins (normally used to build a battery monitor, using either VM or host code).
- A block of BCCMD commands provides access to the module's Persistent Store (PS) configuration database. The database sets the device's Bluetooth address, Class of Device, radio (transmit class) configuration, SCO routing, LM, USB and DFU constants, etc.
- A UART "break" condition can be used in three ways:
  - Presenting a UART break condition to the module can force the module to perform a hardware reboot.
  - Presenting a break condition at boot time can hold the module in a low power state, preventing normal initialisation while the condition exists.
  - With BCSP, the firmware can be configured to send a break to the host before sending data - normally used to wake the host from a Deep Sleep state.
- The DFU standard has been extended with public/private key authentication, allowing manufacturers to control the firmware that can be loaded onto their Bluetooth modules.
- A modified version of the DFU protocol allows firmware upgrade via the module's UART.
- A block of "radio test" or Built-In Self-Test (BIST) commands allows direct control of the module's radio. This aids the development of modules' radio designs and can be used to support Bluetooth qualification.
- Virtual Machine (VM). The VM allow development of customer applications on the module. Although the VM is mainly used with "RFCOMM builds" (alternative firmware builds providing L2CAP, SDP and RFCOMM), the VM can be used with this build to perform simple tasks such as flashing LEDs via the module's PIO port.
- Hardware low power modes: Shallow Sleep and Deep Sleep. The module drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed over HCI (over BCSP). However, up to three SCO channels can be routed over the module's single PCM port (at the same time as routing any other SCO channels over HCI).

4.6 RFCOMM Stack

In this firmware version the upper layers of the Bluetooth stack up to RFCOMM are run onboard the module. This reduces host-side software and hardware requirements at the expense of some of the power and flexibility of the HCI only stack.



Embedded Two-Processor Architecture

The RFCOMM firmware exposes APIs (application programming interface) to L2CAP, Service Discovery Protocol (SDP), RFCOMM and Device Manager (DM) functionality. Background information on Bluetooth and its upper layers can be found in the Bluetooth specification v1.1. The firmware also contains a Virtual Machine (VM), which may be used to develop customer applications on the module.

Two variants of this firmware are provided; one supports the BlueCore Serial Protocol (BCSP) transport protocol and the other supports the Bluetooth UART (Universal Asynchronous Receiver Transmitter) H4 protocol.

Note:
RFCOMM firmware does not expose the Host Controller Interface (HCI) and is, therefore, not suitable for use with third party stacks.

4.6.1 Key Features of the RFCOMM Stack

Interfaces to Host

- RFCOMM, an RS-232 serial cable emulation protocol
- SDP, a service database look-up protocol

Connectivity

- Maximum number of active slaves: 3
- Maximum number of simultaneous active ACL connections: 3
- Maximum number of simultaneous active SCO connections: 3
- Data Rate: up to 350 Kb/s

Security

- Full support for all Bluetooth security features up to and including strong (128-bit) encryption.

Power Saving

- Full support for all Bluetooth power saving modes (Park, Sniff and Hold).

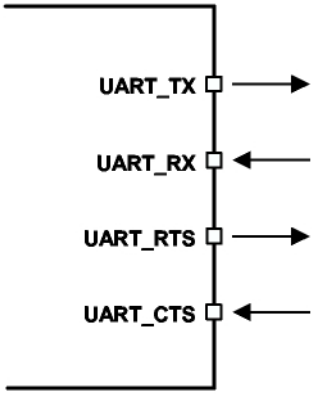
Data Integrity

- Channel quality driven data rate (CQDDR) increases the effective data rate in noisy environments.
- Received signal strength indication (RSSI) used to minimise interference to other radio devices using the ISM band.

5 Device terminal description

5.1 UART Interface

The F2M03 Bluetooth module's Universal Asynchronous Receiver Transmitter (UART) interface provides a simple mechanism for communicating with other serial devices using the RS232 standard(1).



Universal Asynchronous Receiver

Four signals are used to implement the UART function, as shown in the figure above. When F2M03 is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signalling levels of 0V and VDD. UART configuration parameters, such as Baud rate and packet format, are set by Free2move firmware.

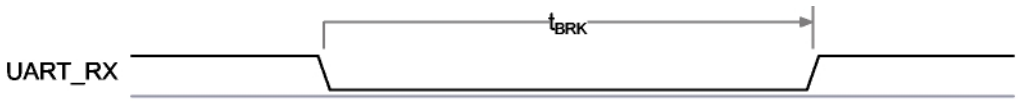
Note:
In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

(1) Uses RS232 protocol but voltage levels are 0V to VDD, (requires external RS232 transceiver IC)

Parameter		Possible Values
Baud Rate	Minimum	1200 Baud (≤2%Error)
		9600 Baud (≤1%Error)
	Maximum	1.5MBaud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per channel		8

Possible UART Settings

The UART interface is capable of resetting the Free2move module upon reception of a break signal. A Break is identified by a continuous logic low on the UART_RX terminal, as shown in figure below. If tBRK is longer than a special value, defined by the Free2move firmware a reset will occur. This feature allows a host to initialise the system to a known state. Also, the F2M03 can emit a Break character that may be used to wake the Host. This is subject to firmware support, contact Free2move for more information.



Break signal

5.2 USB Interface

F2M03 USB devices contain a full-speed (12Mbits/s) USB interface, capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented behave as specified in the USB section of the Bluetooth specification v1.1. As USB is a master-slave orientated system, F2M03 only supports USB slave operation.

5.2.1 USB Data Connections

The USB data lines emerge as pins USB_D+ and USB_D- on the package. To match the connection to the characteristic impedance of the USB cable series resistors are connected internally of the F2M03AC2. No external resistors are needed for either USB_D+ or USB_D-.

5.2.2 USB Pull-up Resistor

F2M03 features an internal USB pull-up resistor. This pulls the USB_D+ pin weakly high when F2M03 is ready to enumerate. It signals to the PC that it is a full-speed (12Mbit/s) USB device.

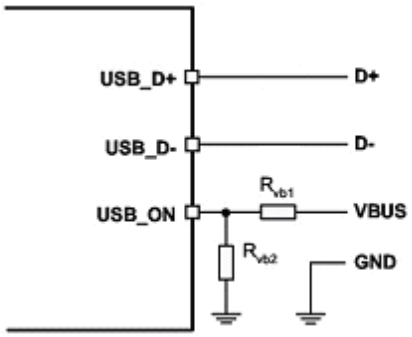
The USB internal pull-up is implemented as a current source, and is compliant with 7.1.5 of the USB specification v1.1. The internal pull-up pulls USB D+ high to at least 2.8V when loaded with a 15kΩ-5% pull-down resistor (in the hub/host) (when VDD=3.1V). This presents a thevenin resistance to the host of at least 900 ohms. Alternatively, an external 1.5kO pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used (contact Free2move). The default setting uses the internal pull-up resistor.

5.2.3 Power Supply

The minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on terminals must be an absolute minimum of 3.1V. Free2move recommends 3.3V for optimal USB signal quality.

5.2.4 Self-Powered Mode

In self-powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design for, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to F2M03 via a resistor network (Rvb1 and Rvb2), so F2M03 can detect when VBUS is powered up. F2M03 will not pull USB_D+ high when VBUS is off.



Connections to F2M03 for Self-Powered Mode

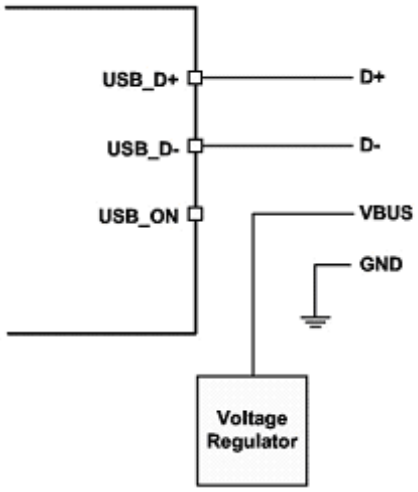
The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by settings in firmware (contact Free2move) to the corresponding pin number.

5.2.5 Bus-Powered Mode

In bus-powered mode the application circuit draws its current from the 5V VBUS supply on the USB cable. F2M03 negotiates with the PC during the USB enumeration stage about power consumption.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification (see USB 1.1 specification, section 7.2.4.1). Some applications may require soft-start circuitry to limit inrush current if more than 10µF is present between VBUS and GND.

The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator's bandwidth. Excessive noise on the 1.8V supply to the supply pins of F2M03 may result in reduced receive sensitivity and a distorted transmit signal.



Connections to F2M03 for Bus-Powered Mode

Identifier	Value	Function
R_{vb1}	47kΩ -5%	VBUS ON sense divider
R_{vb2}	22kΩ - 5%	VBUS ON sense divider

USB Interface Component Values

Note:
USB_ON is shared with F2M03's PIO terminals.

5.2.6 Suspend Current

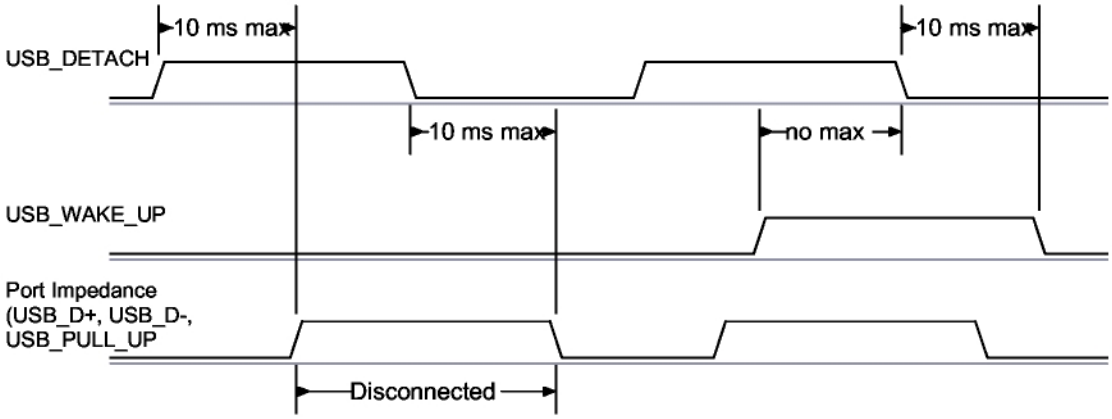
USB devices that run off VBUS must be able to enter a suspended state, whereby they consume less that 0.5mA from VBUS. The voltage regulator circuit itself should draw only a small quiescent current (typically less than 100µA) to ensure adherence to the suspend-current requirement of the USB specification. This is not normally a problem with modern regulators. Ensure that external LEDs can be turned off by F2M03. The entire circuit must be able to enter the suspend mode.

5.2.7 Detach and Wake_Up Signalling

F2M03 can provide out-of-band signalling to a host controller by using the dedicated control lines called 'USB_DETACH' and 'USB_WAKE_UP'. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding F2M03 into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by firmware settings (contact Free2move)

USB_DETACH, is an input which, when asserted high, causes F2M03 to put USB_D- and USB_D+ in a high-impedance state and to 1.5kO pull-up resistor on USB_D+. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, F2M03 will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP, is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB WAKE_UP message (which runs over the USB cable proper), and cannot be sent while F2M03 is effectively disconnected from the bus.



USB_DETACH and USB_WAKE_UP Signal

5.2.8 USB Driver

A USB Bluetooth device driver is required to provide a software interface between F2M03 and Bluetooth applications running on the host.

5.2.9 USB 1.1 Compliance

The Bluetooth chip on the F2M03 is qualified to the USB specification v1.1, details of which are available from http://www.usb.org. The specification contains valuable information on aspects such as PCB track impedance, supply inrush current and product labelling.

Although F2M03's Bluetooth chip meets the USB specification, Free2move cannot guarantee that an application circuit designed around the chip is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to Chapter 7. Independent USB qualification must be sought before an application is deemed USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plugfest or from an independent USB test house.

Terminals USB_DP and USB_DN adhere to the USB specification 1.1 (Chapter 7) electrical requirements.
For ac and dc specifications for terminals USB_DETACH, USB_WAKE_UP, USB_PULL_UP and USB_ON, refer to section PIO specification.

5.2.10 2.0 Compatibility

F2M03 is compatable with USB specification 2.0 masters; under these circumstances the two ends agree the mutually acceptable rate of 12Mbits/s according to the USB 2.0 specification.

5.3 Serial Peripheral Interface

F2M03 is a slave device that uses terminals SPI_MOSI, SPI_MISO, SPI_CLK and SPI_CSB. This interface is used for program emulation/debug and IC test. It is also the means by which the F2M03 flash may be programmed, before any 'boot' program is loaded.

Note:
The designer should be aware that no security protection is built into the hardware or firmware associated with this port, so the terminals should not be permanently connected in a PC application. This interface is not a user interface and only used for initial download and configuration by Free2move.

5.4 PCM

Pulse Code Modulation (PCM) is the standard method used to digitise human voice patterns for transmission over digital communication channels. Through its PCM interface, F2M03AC2 has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset and other audio applications F2M03 offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Please note that the F2M0AC2 also includes an analog interface for voice, which is used by default. PCM is however available for customers who want a digital interface. Contact Free2move for more information

Hardware on F2M03 allows the data to be sent to and received from a SCO connection. Up to three SCO connections can be supported by the PCM interface at any one time(1)

F2M03 can operate as the PCM interface Master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave it can operate with an input clock up to 2048kHz. F2M03 is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13 or 16-bit linear, 8-bit p-law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by firmware settings (contact Free2move).

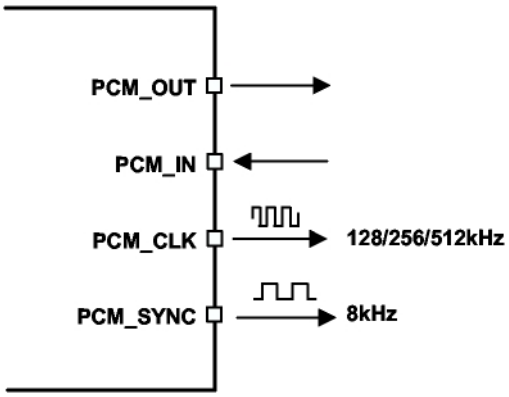
F2M03 interfaces directly to PCM audio devices includes the following:
Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
OKI MSM7705 four channel A-law and p-law CODEC
Motorola MC145481 8-bit A-law and µ-law CODEC
Motorola MC145483 13-bit linear CODEC

F2M03 is also compatible with the Motorola SSITM interface

Note:
(1) Subject to firmware support, contact Free2move for current status.

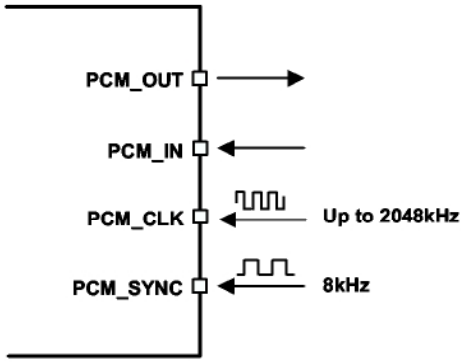
5.4.1 PCM Interface Master/Slave

When configured as the Master of the PCM interface, F2M03 generates PCM_CLK and PCM_SYNC.



F2M03 as PCM Interface Master

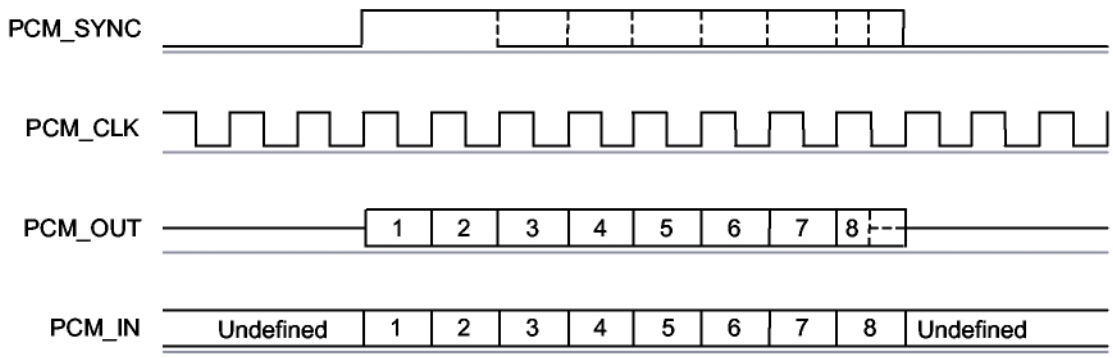
When configured as the Slave of the PCM interface, F2M03 accepts PCM_CLK rates up to 2048kHz



F2M03 as PCM Interface Master

5.4.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When F2M03 is configured as PCM Master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When F2M03 is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate (i.e., 62.5µs) long.

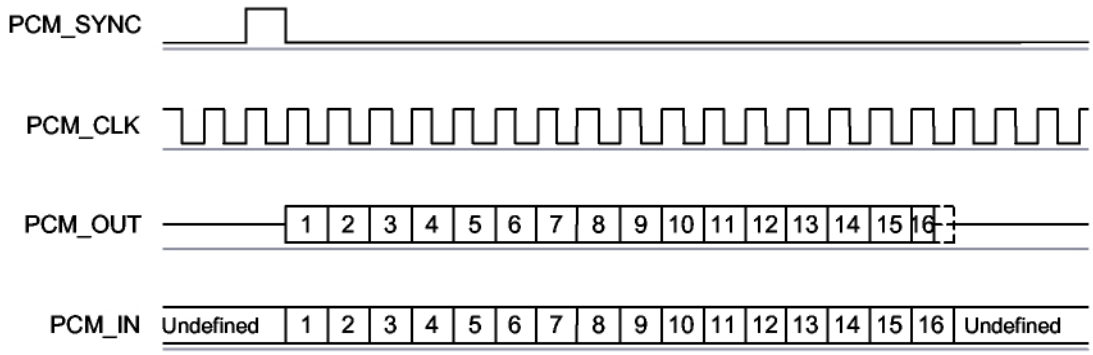


Long Frame Sync (Shown with 8-bit Companded Sample)

F2M03 samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

5.4.3 Short Frame Sync

In Short Frame Sync the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

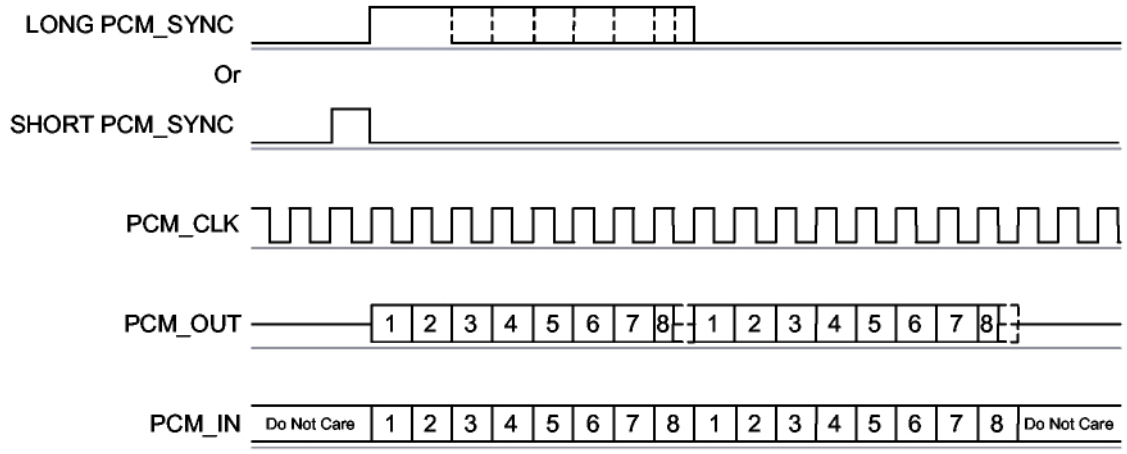


Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, F2M03 samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge

5.4.4 Multi-Slot Operation

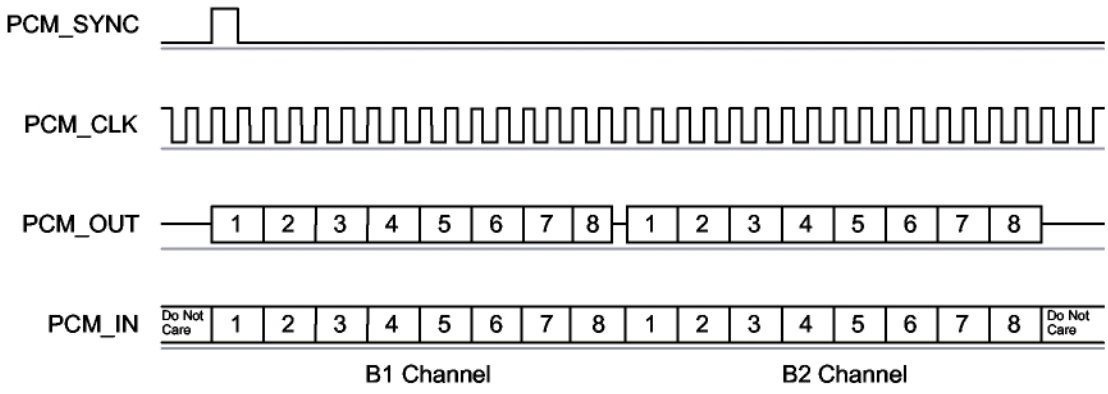
More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.



Multi-slot Operation with Two Slots and 8-bit Companded Samples

5.4.5 GCI Interface

F2M03 is compatible with the General Circuit Interface, a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured. In the GCI interface two clock cycles are required for each bit of the voice sample. The voice sample format is 8-bit companded. As for the standard PCM interface up to 3 SCO connections can be carried over the first four slots.



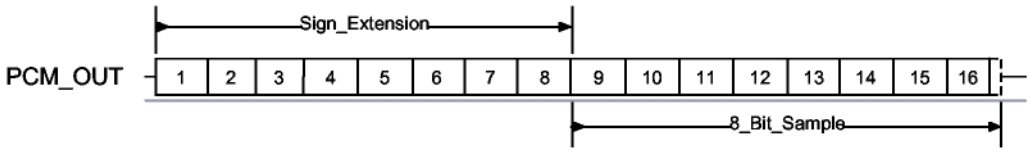
GCI Interface

The start of frame is indicated by PCM SYNC and runs at 8kHz. With F2M03 in Slave mode, the frequency of PCMCLK can be up to PCM_SYNC In order to configure the PCM interface to work in GCI mode it is necessary to have the correct firmware support (contact Free2move)

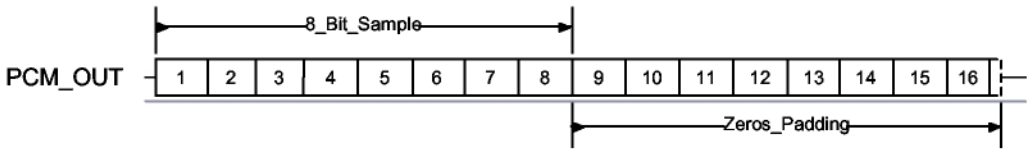
5.4.6 Slots and Sample Formats

F2M03 can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8, 13 or 16-bit sample formats.

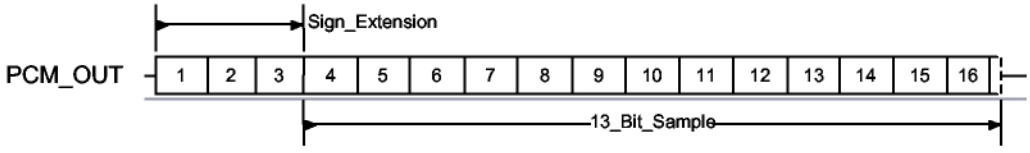
F2M03 supports 13-bit linear, 16-bit linear and 8-bit p-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.



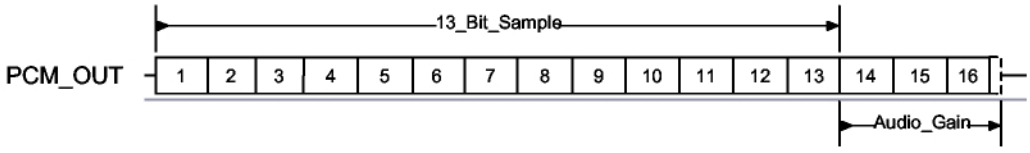
A 16-bit slot with 8-bit companded sample and sign extension selected



A 16-bit slot with 8-bit companded sample and zeros padding selected



A 16-bit slot with 13-bit linear sample and sign extension selected



A 16-bit slot with 13-bit linear sample and audio gain selected

5.4.7 Additional Features

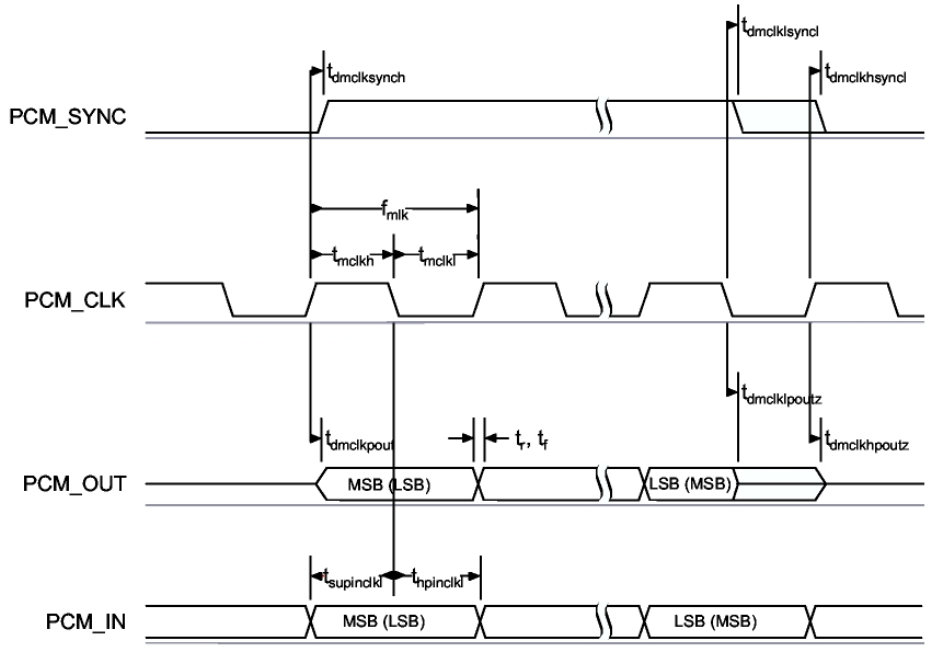
F2M03 has a mute facility that forces PCM_OUT to be 0. In Master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running (which some CODECS use to control power-down)

5.4.8 PCM Timing Information

PCM Master Timing

Symbol	Parameter	Min(1)	Typ	Max(2)	Unit
f_{mclk}	PCMCLK frequency	-	128 256 512	-	kHz
-	PCM_SYNC frequency	-	8		kHz
t_{mclkh} (1)	PCM_CLK high	980	-	-	ns
t_{mclkl} (1)	PCM_CLK low	730	-		ns
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high	-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT	-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)	-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low	-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCMOUT high impedance	-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCMOUT high impedance	-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low	30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	30	-	-	ns
t_r	Edge rise time (C_l = 50 pf, 10-90 %)	-	-	15	ns
t_f	Edge fall time (C_l = 50 pf, 10-90 %)	-	-	15	ns

Note:
(1) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.
(2) Valid for temperatures between -40°C and +105°C

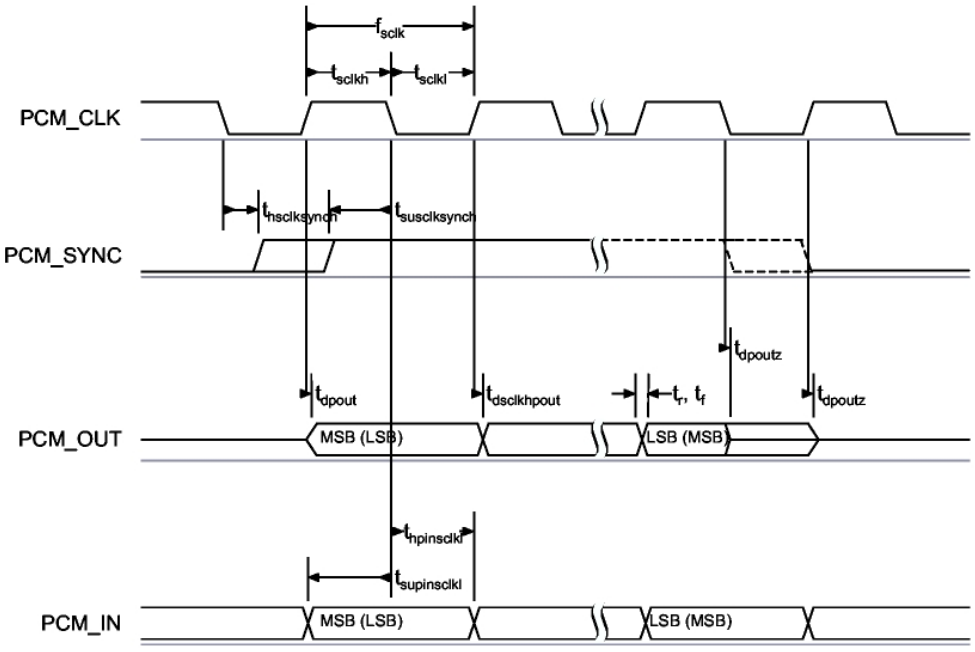


PCM Master Timing

PCM Slave Timing

Symbol	Parameter	Min (1)	Typ	Max(1)	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	30	-		ns
t_r	Edge rise time (Cl = 50 pF, 10-90 %)	-	-	15	ns
T_f	Edge fall time (Cl = 50 pF, 10-90 %)	-	-	15	ns

Note:
(1) Valid for temperatures between -40°C and +105°C



PCM slave timing

5.5 Parallel I/O

The Parallel Input Output (PIO) Port is a general-purpose I/O interface to F2M03AC2. The port consists of nine programmable, bi-directional I/O lines, PIO[9:2] and AIO[0]

Programmable I/O lines can be accessed either via an embedded application running on F2M03AC2 or via private channel or manufacturer-specific HCI commands. All access to I/O pins are subject to firmware support. Contact Free2move for more information

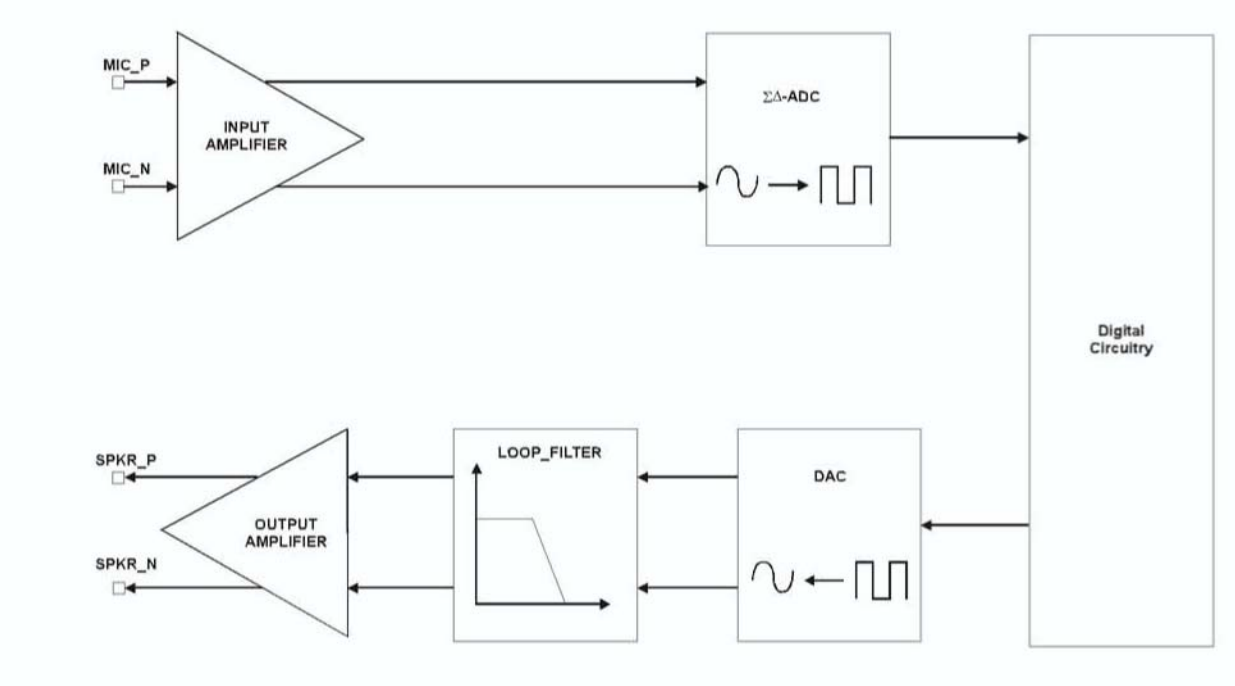
PI0 lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PI0 lines are configured as inputs with weak pull-downs at reset.

F2M03AC2 has one general purpose analogue interface pin, AIO[0], Functions available via this pin include an 8-bit ADC and an 8-bit DAC. Typically the ADC is used for battery voltage measurement. Signals selectable at this pins include the bandgap reference voltage and a variety of clock signals; 48, 24, 16, 8MHz and the XTAL clock frequency. When used with analogue signals the voltage range is 1.8V. The AIO[0] can also be used as a digital I/O.

5.6 Analog audio

The F2M03AC2 has an analog audio interface, which can be used for direct speaker drive and microphone input using a minimum number of external components. It is primarily intended for voice applications and it is fully operational from a single internal 1.8 Volt power supply. A fully differential architecture has been implemented for optimal power supply rejection and low noise performance. The digital format is 15-bit/sample linear PCM with a data rate of 8kHz.

The CODEC has an input stage containing a microphone amplifier, variable gain amplifier and ∑-Δ ADC. Its output stage contains a DAC, low-pass filter and output amplifier. The CODEC functional diagram is shown below.



5.6.1 Input Stage

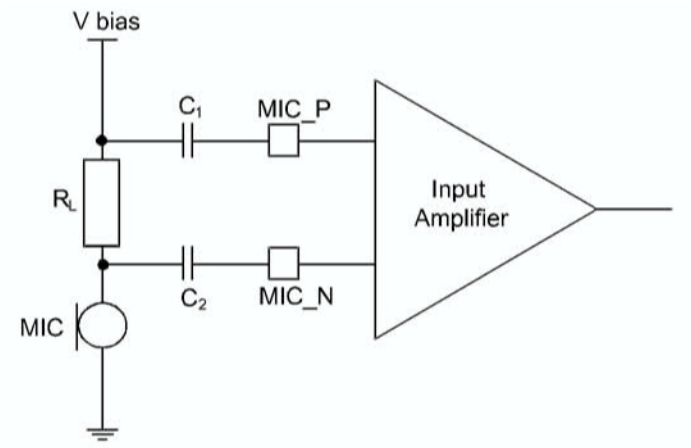
A low noise variable gain amplifier amplifies the signal difference between inputs MIC N and MIC P. The input may be from either a microphone or line. The amplified signal is then digitised by a second order ∑-Δ ADC. The high frequency single bit output from the ADC is converted to 15-bit 8kHz linear PCM data.

The gain is programmable via firmware (subject to firmware support, consult available application notes and datasheets or contact free2move). The maximum range is 42dB with 3dB resolution. At maximum gain the full scale input level is 3mV rms. A bias network is required for operation with a microphone whereas the line input may be simply a.c. coupled. The following sections explain each of these modes. Single ended signals are supported by F2M03AC2: a single ended signal may be driven into either MIC N or MIC_P with the undriven input coupled to ground by a capacitor.

The signal to noise ratio is better than 60dB and distortion is less than -75dB

5.6.2 Microphone Input

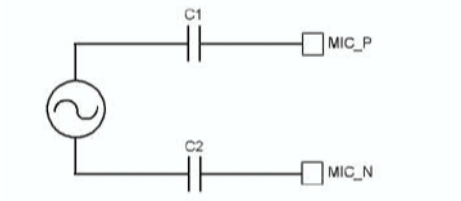
The F2M03A2 audio CODEC has been designed for use with microphones that have sensitivities between -60 and -40dBV. The sensitivity of -60dBV is equivalent to a microphone output of 1 µA when presented with an input level of 94dB SPL and loaded with 1 kid. The microphone should be biased as shown in figure below.



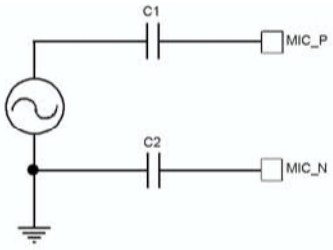
The input impedance at MIC_N and MIC_P is typically 20kΩ. C1 and C2 should be 47nF. R_L sets the microphone load impedance and is normally between 1 and 2kΩ. V bias should be chosen to suit the microphone and have sufficient low *noise. It may be* obtained by filtering the *output of a PIO* line. (Subject to firmware support, consult available application notes and datasheets or contact free2move)

5.6.3 Line Input

If the input gain is set to less than 21 dB F2M03AC2 automatically selects line input mode. In this mode the input impedance at MIC_N and MIC_P is increased to 130kQ typical. At the minimum gain setting the maximum input signal *level is 380 mV rms.* Figures below show two circuits for line input operation and show connections for either differential or single ended inputs.



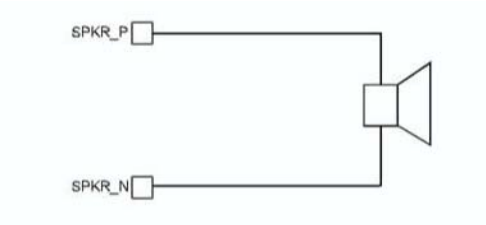
Differential Microphone Input (C1 and C2 should be 15nF)



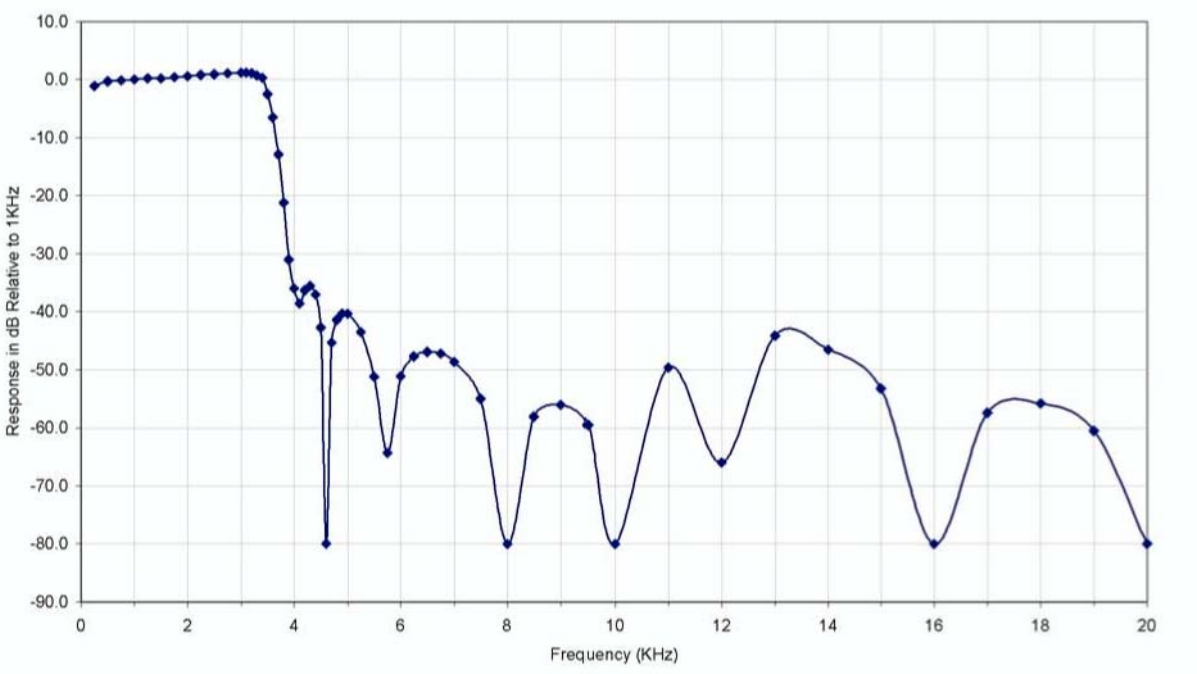
Single-ended Microphone Input (C1 and C2 should be 15nF).

5.6.4 Output stage

The digital data is converted to an analogue value by a DAC, then it is filtered prior to amplification by the output amplifier and it is available as a differential signal between SPKR P and SPKR N. The output amplifier is capable of driving a speaker directly if its impedance is greater than 8Ω. The amplifier is stable with capacitive loads up to 500pF. The gain is programmable with a range of 21dB and a resolution of 3dB. Maximum output level is typically 700 mV rms for high impedance loads, or 20mA rms for low impedance loads. The signal to noise is better than 70dB and the distortion is less than -75dB.



Speaker output



Frequency Response of the ADC and DAC Pair

5.7 Power Supplies

VDD
Power for the F2M03

GND
Ground for F2M03

NC
To guarantee correct operation, NC must not be connected externally. Free2move recommends that unconnected terminals be placed on unconnected pads to ensure mechanical robustness.

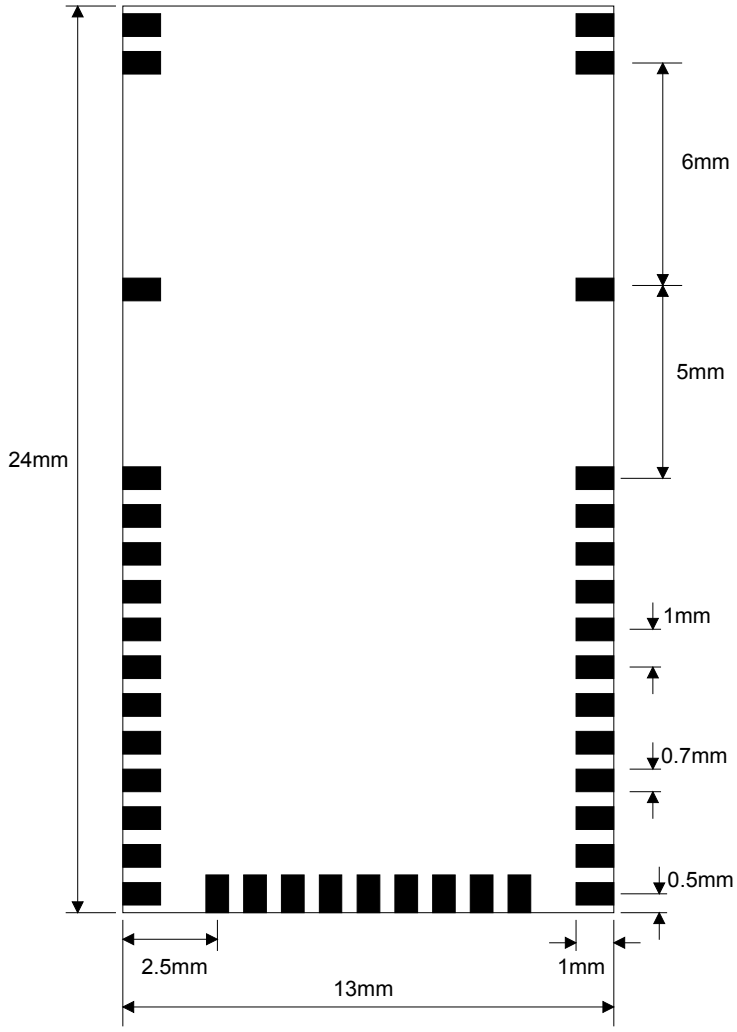
RESET
Free2move recommend the RESET to be connected to an external micro controller or reset circuit. It is recommended that RESET is applied for a period greater than 5ms.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tristated. The PIOs have weak pull-downs.

6 Application information

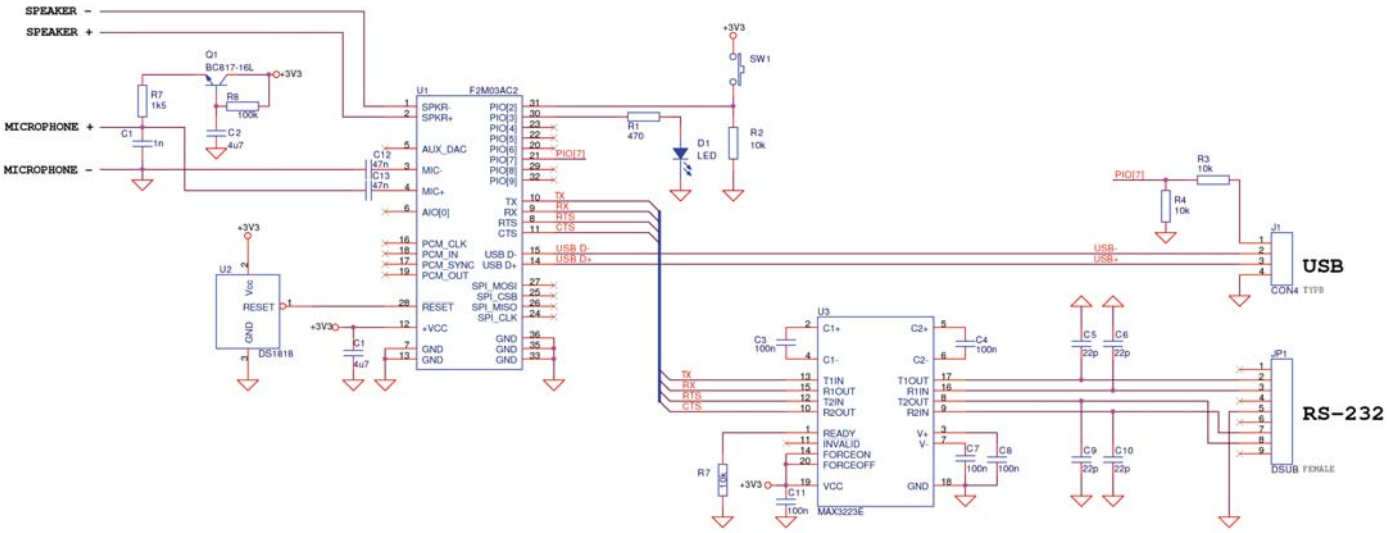
The module uses bottom pads for soldering optimized for an automatic solder line. It is also possible to solder the module manually by using hot air soldering. For manual soldering solder pads may in some situation be made slightly larger to allow easier warm up process.

(Top view)



Recommended pad layout

A typical application schematic is shown in the figure below.



All capacitors in the schematic above are ceramic and must be mounted as close as possible to its respectively IC.

The module must be reset at start-up. This can be done either with a reset-circuit such as the DS1818 from Dallas-semiconductor or using an I/O from a microcontroller. Reset cannot be done with just a R-C network.

Layout tips:
All GND pads must be connected directly to a flooded ground-plane. If more then one ground layer is used then make a good connection between them using many via holes. VDD should be connected to the power supply using a wide trace.

Audio interface:
The speaker outputs (SPKR) are differential and can be directly connected to a speaker with high impedance.

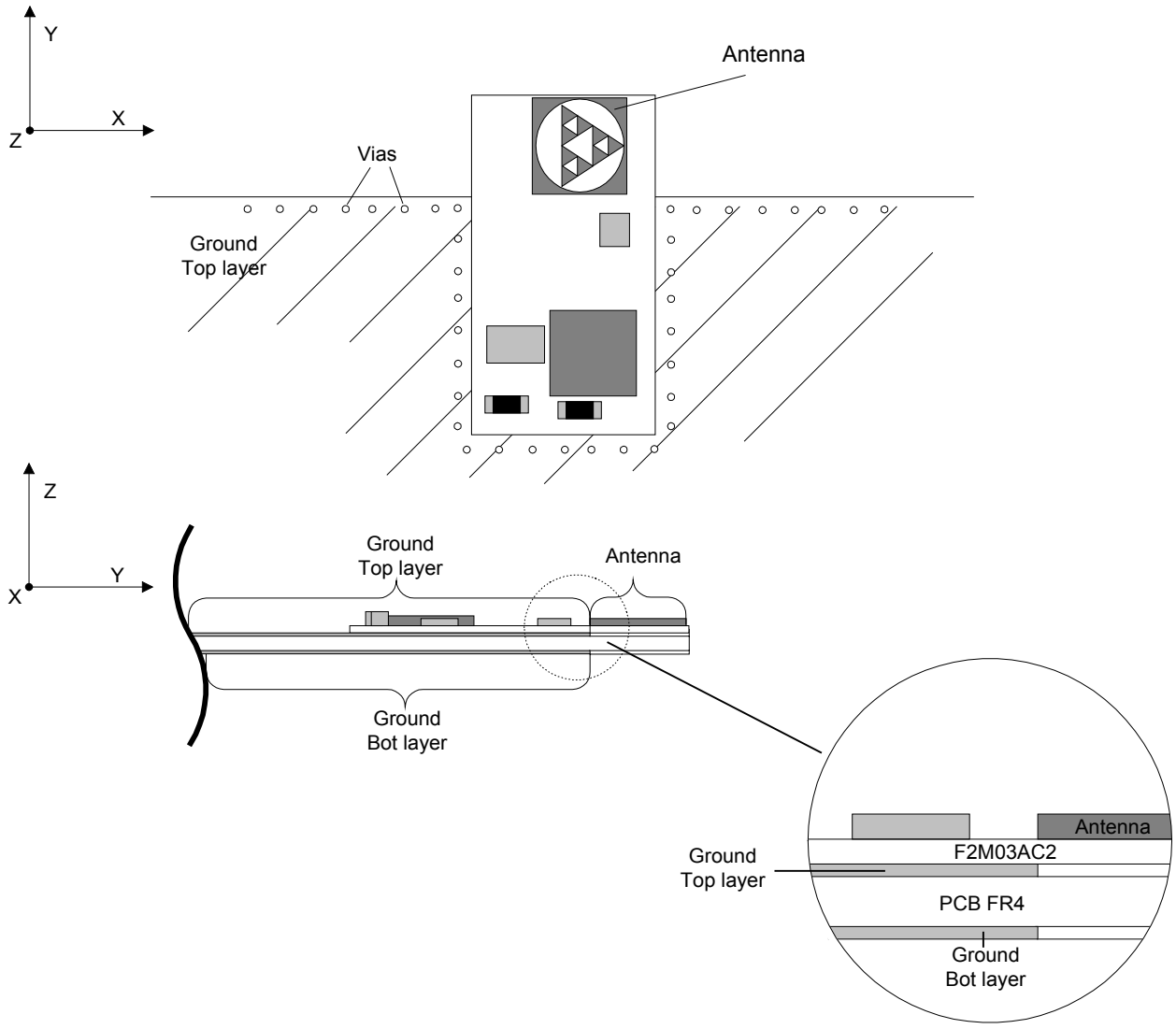
If the speaker is referred to GND a capacitor must be connected in series between SPKR+ output and the positive speaker connection. This is to prevent the dc-bias being present on the SPKR-outputs.
When the speaker is referred to GND the SPKR- must be left unconnected (NC).

In order to get as low noise as possible (when using a ground referenced speaker) it is advisable to use a differential to ground-referenced converter such as an OP-amp.

If the microphone is dynamic it can be directly connected to C12,C13. When using an electret-microphone it must however be dc-biased, which can be done using a circuit such as the one used in schematic above based on Q1.

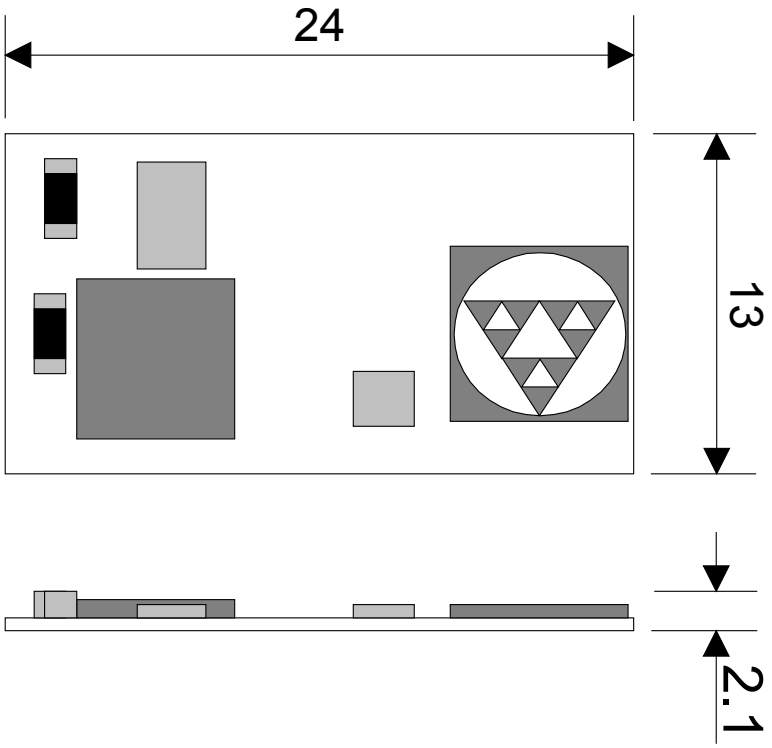
To achieve good RF performance for the antenna it is advisable to place a ground plane beneath that part of the module where the antenna is not mounted. Except from the ground plane it is preferable that there are as few components and other material as possible nearby the antenna. Free air is the best surroundings for the antenna.

- White area should be transparent, thus no ground plane.
- When using multilayer PCB, through plating is necessary.
- Other components may be placed on shaded area.



7 Package information

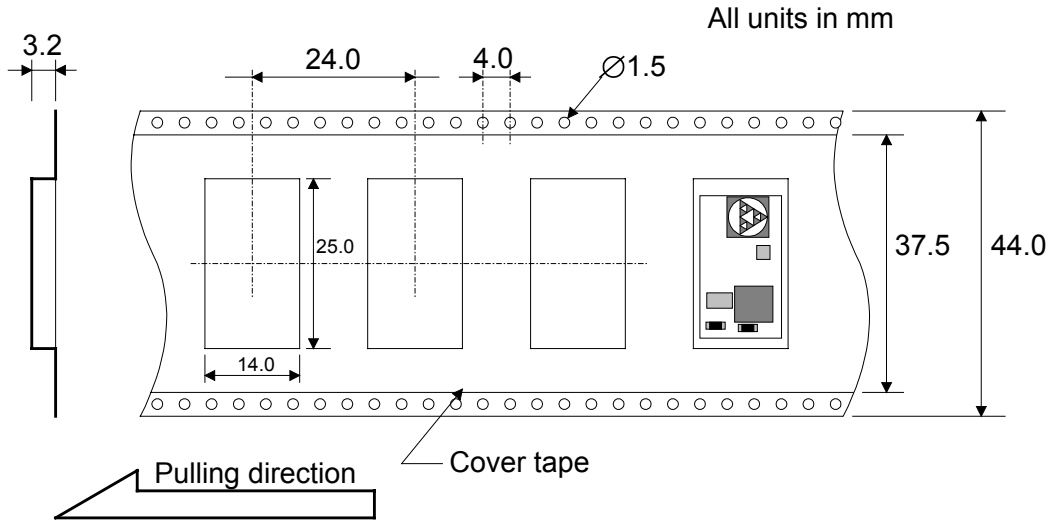
(Top and side view)



Package information

8 Tape information

TAPE DETAILS



9 Ordering information

The F2M03AC2 is available for delivery in volumes.

Part nr:	Description
F2M03AC2	Class 2 module with antenna (Always postfix with three signs for correct firmware)
F2M03AC2 001	Class 2 module with antenna. Wireless UART firmware (followed by three letters indicating version number e.g. F2M03C1-001-R1A) When not indicating version number e.g. R1A the latest available version will be delivered.

For correct part numbers for your firmware contact Free2move.

Please use our website: Twww.free2move.se for more information about local distributors and dealers.

10 Document References

Document References	Version
Specification of the Bluetooth system	v1.1, 22 February 2001
Universal Serial Bus Specification	v1.1, 23 September 1998

11 Acronyms and definitions

Term:	Definition:
Bluetooth	A set of technologies providing audio and data transfer over short-range radio
ACL	Asynchronous Connection-Less. A Bluetooth data packet.
AC	Alternating Current
A-law	Audio encoding standard
API	Application Programming Interface
BCSP	BlueCore™ Serial Protocol
BER	Bit Error Rate. Used to measure the quality of a link
C/I	Carrier Over Interferer
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder Decoder
CPU	Central Processing Unit
CQDDR	Channel Quality Driven Data Rate
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1mW
DC	Direct Current
DFU	Device Firmware Upgrade
GCI	General Circuit Interface. Standard synchronous 2B+D ISDN timing interface
HCI	Host Controller Interface
Host	Application's microcontroller
Host Controller	Bluetooth integrated chip
HV	Header Value
ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific and Medical
ksamples/s	kilosamples per second
L2CAP	Logical Link Control and Adaptation Protocol (protocol layer)
LC	Link Controller
LSB	Least-Significant Bit
p-law	Encoding standard
MISO	Master In Serial Out
OHCI	Open Host Controller Interface
PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Code Modulation. Refers to digital voice data
PIO	Parallel Input Output
RAM	Random Access Memory
RF	Radio Frequency
RFCOMM	Protocol layer providing serial port emulation over L2CAP
RISC	Reduced Instruction Set Computer
RSSI	Receive Signal Strength Indication
RTS	Ready To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented. Voice oriented Bluetooth packet
SDP	Service Discovery Protocol
SIG	Special Interest Group
SPI	Serial Peripheral Interface
SPP	Serial Port Profile
TBD	To Be Defined
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus or Upper Side Band (depending on context)
VM	Virtual Machine
www	world wide web

Contact information

For support questions please contact your local dealer
For other purposes use: info@free2move.se
Website: www.free2move.se

Your distributor