Lab # - Report Title

Name

Date

Second summer 2014

Purpose:

At least one paragraph

Analysis:

At least one paragraph

4bit adder / Sub-tractor Symbol

4bit adder / Sub-tractor Schematic

4bit adder / Sub-tractor Command File

Expected results (table of expected outputs based on your input patterns)

Simulation screenshot with **built-in** components

Simulation screenshot with **Motorola (real)** components

Appendix I

Symbol/Schematic/CMD / Expected results /Simulation for the followings using **real components:**

1 bit adder

Xor gate