Total Items	111
Pass Items	76
Fail Items	35
NY Items	0

	Section	Main Title
	1	Register test
	1.1	Read default value
	1.2	Read and Write value test
	1.3	Reserved region test
	1.4	R/W1C test
	2	Oversampling test
13X	2.1	2400 baud rate
	2.2	4800 baud rate
	2.3	9600 baud rate
	2.4	19200 baud rate
	2.5	38400 baud rate
	2.6	76800 baud rate
	2.7	115200 baud rate
	2.8	Custom baud rate
16X	2.9	2400 baud rate
	2.10	4800 baud rate
	2.11	9600 baud rate
	2.12	19200 baud rate
	2.13	38400 baud rate
	2.14	76800 baud rate

	2.15	115200 baud rate
	2.16	Custom baud rate
	3	Transmit and receive combine baud rate test
HALF DUPLEX Transmit only	3.1	5 bits + none + 1 stop
	3.2	5 bits + none + 2 stop
	3.3	5 bits + odd + 1 stop
	3.4	5 bits + odd + 2 stop
	3.5	5 bits + even + 1 stop
	3.6	5 bits + even + 2 stop
	3.7	6 bits + none + 1 stop
	3.8	6 bits + none + 2 stop
	3.9	6 bits + odd + 1 stop
	3.10	6 bits + odd + 2 stop
	3.11	6 bits + even + 1 stop
	3.12	6 bits + even + 2 stop
	3.13	7 bits + none + 1 stop
	3.14	7 bits + none + 2 stop
	3.15	7 bits + odd + 1 stop
	3.16	7 bits + odd + 2 stop
	3.17	7 bits + even + 1 stop
	3.18	7 bits + even + 2 stop
	3.19	8 bits + none + 1 stop
	3.20	8 bits + none + 2 stop
	3.21	8 bits + odd + 1 stop
	3.22	8 bits + odd + 2 stop

	3.23	8 bits + even + 1 stop
	3.24	8 bits + even + 2 stop
	3.25	Dynamic change test
HALF DUPLEX Receive only	3.26	5 bits + none + 1 stop
	3.27	5 bits + none + 2 stop
	3.28	5 bits + odd + 1 stop
	3.29	5 bits + odd + 2 stop
	3.30	5 bits + even + 1 stop
	3.31	5 bits + even + 2 stop
	3.32	6 bits + none + 1 stop
	3.33	6 bits + none + 2 stop
	3.34	6 bits + odd + 1 stop
	3.35	6 bits + odd + 2 stop
	3.36	6 bits + even + 1 stop
	3.37	6 bits + even + 2 stop
	3.38	7 bits + none + 1 stop
	3.39	7 bits + none + 2 stop
	3.40	7 bits + odd + 1 stop
	3.41	7 bits + odd + 2 stop
	3.42	7 bits + even + 1 stop
	3.43	7 bits + even + 2 stop
	3.44	8 bits + none + 1 stop
	3.45	8 bits + none + 2 stop
	3.46	8 bits + odd + 1 stop
	3.47	8 bits + odd + 2 stop

	3.48	8 bits + even + 1 stop
	3.49	8 bits + even + 2 stop
	3.50	Dynamic change test
FULL DUPLEX	3.51	5 bits + none + 1 stop
	3.52	5 bits + none + 2 stop
	3.53	5 bits + odd + 1 stop
	3.54	5 bits + odd + 2 stop
	3.55	5 bits + even + 1 stop
	3.56	5 bits + even + 2 stop
	3.57	6 bits + none + 1 stop
	3.58	6 bits + none + 2 stop
	3.59	6 bits + odd + 1 stop
	3.60	6 bits + odd + 2 stop
	3.61	6 bits + even + 1 stop
	3.62	6 bits + even + 2 stop
	3.63	7 bits + none + 1 stop
	3.64	7 bits + none + 2 stop
	3.65	7 bits + odd + 1 stop
	3.66	7 bits + odd + 2 stop
	3.67	7 bits + even + 1 stop
	3.68	7 bits + even + 2 stop
	3.69	8 bits + none + 1 stop
	3.70	8 bits + none + 2 stop
	3.71	8 bits + odd + 1 stop
	3.72	8 bits + odd + 2 stop
	3.73	8 bits + even + 1 stop

	3.74	8 bits + even + 2 stop
	3.75	Dynamic change test
	4	Interrupt test
	4.1	parity error
	4.2	disable parity error
	4.3	rx fifo empty
	4.4	disable rx fifo empty
	4.5	rx fifo full
	4.6	disable rx fifo full
	4.7	tx fifo empty
	4.8	disable tx fifo empty
	4.9	tx fifo full
	4.10	disable tx fifo full
	5	Inject error test
	3.1	parity missmatch
	3.2	stop bit missmatch
	3.3	data width missmatch
	3.4	baud rate missmatch
	3.5	Write data when tx fifo full

Description
Use pre define sequence: **uvm_reg_hw_reset_seq** to test all register except TBR and RBR
Use pre define sequence: **uvm_reg_bit_bash_seq** to test all register except FSR, TBR and RBR
Random data is written to the register at address 0x020, reading data from the register gives the result 32'hFFFF_FFFF
Config VIP baudrate 2400, 2 stop bit, no parity, 8 bit data
Config VIP baudrate 4800, 2 stop bit, no parity, 8 bit data
Config VIP baudrate 9600, 2 stop bit, no parity, 8 bit data
Config VIP baudrate 19200, 2 stop bit, no parity, 8 bit data
Config VIP baudrate 38400, 2 stop bit, no parity, 8 bit data
Config VIP baudrate 76800, 2 stop bit, no parity, 8 bit data
Config VIP baudrate 115200, 2 stop bit, no parity, 8 bit data
Config VIP random baudrate, 2 stop bit, no parity, 8 bit data
Config VIP baudrate 2400, 2 stop bit, no parity, 8 bit data
Config VIP baudrate 4800, 2 stop bit, no parity, 8 bit data
Config VIP baudrate 9600, 2 stop bit, no parity, 8 bit data
Config VIP baudrate 19200, 2 stop bit, no parity, 8 bit data
Config VIP baudrate 38400, 2 stop bit, no parity, 8 bit data
Config VIP baudrate 76800, 2 stop bit, no parity, 8 bit data

Config VIP
baudrate 115200, 2 stop bit, no parity, 8 bit data
Config VIP
random baudrate, 2 stop bit, no parity, 8 bit data
Config VIP
baudrate 115200, 1 stop bit, none parity, 5 bit data
Config VIP
baudrate 115200, 2 stop bit, none parity, 5 bit data
Config VIP
baudrate 115200, 1 stop bit, odd parity, 5 bit data
Config VIP
baudrate 115200, 2 stop bit, odd parity, 5 bit data
Config VIP
baudrate 115200, 1 stop bit, even parity, 5 bit data
Config VIP
baudrate 115200, 2 stop bit, even parity, 5 bit data
Config VIP
baudrate 115200, 1 stop bit, none parity, 6 bit data
Config VIP
baudrate 115200, 2 stop bit, none parity, 6 bit data
Config VIP
baudrate 115200, 1 stop bit, odd parity, 6 bit data
Config VIP
baudrate 115200, 2 stop bit, odd parity, 6 bit data
Config VIP
baudrate 115200, 1 stop bit, even parity, 6 bit data
Config VIP
baudrate 115200, 2 stop bit, even parity, 6 bit data
Config VIP
baudrate 115200, 1 stop bit, none parity, 7 bit data
Config VIP
baudrate 115200, 2 stop bit, none parity, 7 bit data
Config VIP
baudrate 115200, 1 stop bit, odd parity, 7 bit data
Config VIP
baudrate 115200, 2 stop bit, odd parity, 7 bit data
Config VIP
baudrate 115200, 1 stop bit, even parity, 7 bit data
Config VIP
baudrate 115200, 2 stop bit, even parity, 7 bit data
Config VIP
baudrate 115200, 1 stop bit, none parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, none parity, 8 bit data
Config VIP
baudrate 115200, 1 stop bit, odd parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, odd parity, 8 bit data

Config VIP
baudrate 115200, 1 stop bit, even parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, even parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, none parity, 8 bit data
Config VIP
baudrate 115200, 1 stop bit, none parity, 5 bit data
Config VIP
baudrate 115200, 2 stop bit, none parity, 5 bit data
Config VIP
baudrate 115200, 1 stop bit, odd parity, 5 bit data
Config VIP
baudrate 115200, 2 stop bit, odd parity, 5 bit data
Config VIP
baudrate 115200, 1 stop bit, even parity, 5 bit data
Config VIP
baudrate 115200, 2 stop bit, even parity, 5 bit data
Config VIP
baudrate 115200, 1 stop bit, none parity, 6 bit data
Config VIP
baudrate 115200, 2 stop bit, none parity, 6 bit data
Config VIP
baudrate 115200, 1 stop bit, odd parity, 6 bit data
Config VIP
baudrate 115200, 2 stop bit, odd parity, 6 bit data
Config VIP
baudrate 115200, 1 stop bit, even parity, 6 bit data
Config VIP
baudrate 115200, 2 stop bit, even parity, 6 bit data
Config VIP
baudrate 115200, 1 stop bit, none parity, 7 bit data
Config VIP
baudrate 115200, 2 stop bit, none parity, 7 bit data
Config VIP
baudrate 115200, 1 stop bit, odd parity, 7 bit data
Config VIP
baudrate 115200, 2 stop bit, odd parity, 7 bit data
Config VIP
baudrate 115200, 1 stop bit, even parity, 7 bit data
Config VIP
baudrate 115200, 2 stop bit, even parity, 7 bit data
Config VIP
baudrate 115200, 1 stop bit, none parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, none parity, 8 bit data
Config VIP
baudrate 115200, 1 stop bit, odd parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, odd parity, 8 bit data

Config VIP
baudrate 115200, 1 stop bit, even parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, even parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, none parity, 8 bit data
Config VIP
baudrate 115200, 1 stop bit, none parity, 5 bit data
Config VIP
baudrate 115200, 2 stop bit, none parity, 5 bit data
Config VIP
baudrate 115200, 1 stop bit, odd parity, 5 bit data
Config VIP
baudrate 115200, 2 stop bit, odd parity, 5 bit data
Config VIP
baudrate 115200, 1 stop bit, even parity, 5 bit data
Config VIP
baudrate 115200, 2 stop bit, even parity, 5 bit data
Config VIP
baudrate 115200, 1 stop bit, none parity, 6 bit data
Config VIP
baudrate 115200, 2 stop bit, none parity, 6 bit data
Config VIP
baudrate 115200, 1 stop bit, odd parity, 6 bit data
Config VIP
baudrate 115200, 2 stop bit, odd parity, 6 bit data
Config VIP
baudrate 115200, 1 stop bit, even parity, 6 bit data
Config VIP
baudrate 115200, 2 stop bit, even parity, 6 bit data
Config VIP
baudrate 115200, 1 stop bit, none parity, 7 bit data
Config VIP
baudrate 115200, 2 stop bit, none parity, 7 bit data
Config VIP
baudrate 115200, 1 stop bit, odd parity, 7 bit data
Config VIP
baudrate 115200, 2 stop bit, odd parity, 7 bit data
Config VIP
baudrate 115200, 1 stop bit, even parity, 7 bit data
Config VIP
baudrate 115200, 2 stop bit, even parity, 7 bit data
Config VIP
baudrate 115200, 1 stop bit, none parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, none parity, 8 bit data
Config VIP
baudrate 115200, 1 stop bit, odd parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, odd parity, 8 bit data
Config VIP
baudrate 115200, 1 stop bit, even parity, 8 bit data

Config VIP
baudrate 115200, 2 stop bit, even parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, none parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, ODD parity, 8 bit data, SEND incorrect parity
Config VIP
baudrate 115200, 2 stop bit, ODD parity, 8 bit data, SEND incorrect parity
Config VIP
baudrate 115200, 2 stop bit, ODD parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, ODD parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, ODD parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, ODD parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, ODD parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, ODD parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, ODD parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, ODD parity, 8 bit data, SEND incorrect parity
Config VIP
baudrate 115200, 2 stop bit, ODD parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, ODD parity, 6 bit data, SEND incorrect parity
Config VIP
baudrate 9600, 2 stop bit, ODD parity, 8 bit data
Config VIP
baudrate 115200, 2 stop bit, NONE parity, 8 bit data

Testname	Priority	Method	Owner	Status	Milestone
		UVM_RAL	Đ.HUY		
uart_reg_scan_test	HIGH	UVM_RAL	Đ.HUY	PASSED	11072015
read_write_value_test	HIGH	UVM_RAL	Đ.HUY	PASSED	11072015
reserved_region_value_test	HIGH	UVM_RAL	Đ.HUY	PASSED	11072015
read_write_1_clear_test	HIGH	UVM_RAL	Đ.HUY	PASSED	11072015
		Directed	Đ.HUY		
s13x_2400_test	HIGH	Directed	Đ.HUY	PASSED	11072015
s13x_4800_test	HIGH	Directed	Đ.HUY	PASSED	11072015
s13x_9600_test	HIGH	Directed	Đ.HUY	PASSED	11072015
s13x_19200_test	HIGH	Directed	Đ.HUY	PASSED	11072015
s13x_38400_test	HIGH	Directed	Đ.HUY	PASSED	11072015
s13x_76800_test	HIGH	Directed	Đ.HUY	PASSED	11072015
s13x_115200_test	HIGH	Directed	Đ.HUY	PASSED	11072015
s13x_custom_baudrate_test	HIGH	Directed	Đ.HUY	PASSED	11072015
s16x_2400_test	HIGH	Directed	Đ.HUY	PASSED	11072015
s16x_4800_test	HIGH	Directed	Đ.HUY	PASSED	11072015
s16x_9600_test	HIGH	Directed	Đ.HUY	PASSED	11072015
s16x_19200_test	HIGH	Directed	Đ.HUY	PASSED	11072015
s16x_38400_test	HIGH	Directed	Đ.HUY	PASSED	11072015
s16x_76800_test	HIGH	Directed	Đ.HUY	PASSED	11072015

s16x_115200_test	HIGH	Directed	Đ.HUY	PASSED	11072015
s16x_custom_baudrate_test	HIGH	Directed	Đ.HUY	PASSED	11072015
		Directed	Đ.HUY		
trans_5_none_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
trans_5_none_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
trans_5_odd_1_test	HIGH	Directed	Đ.HUY	FAILED	11072015
trans_5_odd_2_test	HIGH	Directed	Đ.HUY	FAILED	11072015
trans_5_even_1_test	HIGH	Directed	Đ.HUY	FAILED	11072015
trans_5_even_2_test	HIGH	Directed	Đ.HUY	FAILED	11072015
trans_6_none_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
trans_6_none_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
trans_6_odd_1_test	HIGH	Directed	Đ.HUY	FAILED	11072015
trans_6_odd_2_test	HIGH	Directed	Đ.HUY	FAILED	11072015
trans_6_even_1_test	HIGH	Directed	Đ.HUY	FAILED	11072015
trans_6_even_2_test	HIGH	Directed	Đ.HUY	FAILED	11072015
trans_7_none_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
trans_7_none_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
trans_7_odd_1_test	HIGH	Directed	Đ.HUY	FAILED	11072015
trans_7_odd_2_test	HIGH	Directed	Đ.HUY	FAILED	11072015
trans_7_even_1_test	HIGH	Directed	Đ.HUY	FAILED	11072015
trans_7_even_2_test	HIGH	Directed	Đ.HUY	FAILED	11072015
trans_8_none_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
trans_8_none_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
trans_8_odd_1_test	HIGH	Directed	Đ.HUY	FAILED	11072015
trans_8_odd_2_test	HIGH	Directed	Đ.HUY	FAILED	11072015

trans_8_even_1_test	HIGH	Directed	Đ.HUY	FAILED	11072015
trans_8_even_2_test	HIGH	Directed	Đ.HUY	FAILED	11072015
dynamic_trans_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_5_none_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_5_none_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_5_odd_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_5_odd_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_5_even_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_5_even_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_6_none_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_6_none_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_6_odd_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_6_odd_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_6_even_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_6_even_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_7_none_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_7_none_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_7_odd_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_7_odd_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_7_even_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_7_even_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_8_none_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_8_none_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_8_odd_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_8_odd_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015

receive_8_even_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
receive_8_even_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
dynamic_receive_test	HIGH	Directed	Đ.HUY	PASSED	11072015
full_5_none_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
full_5_none_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
full_5_odd_1_test	HIGH	Directed	Đ.HUY	FAILED	11072015
full_5_odd_2_test	HIGH	Directed	Đ.HUY	FAILED	11072015
full_5_even_1_test	HIGH	Directed	Đ.HUY	FAILED	11072015
full_5_even_2_test	HIGH	Directed	Đ.HUY	FAILED	11072015
full_6_none_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
full_6_none_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
full_6_odd_1_test	HIGH	Directed	Đ.HUY	FAILED	11072015
full_6_odd_2_test	HIGH	Directed	Đ.HUY	FAILED	11072015
full_6_even_1_test	HIGH	Directed	Đ.HUY	FAILED	11072015
full_6_even_2_test	HIGH	Directed	Đ.HUY	FAILED	11072015
full_7_none_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
full_7_none_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
full_7_odd_1_test	HIGH	Directed	Đ.HUY	FAILED	11072015
full_7_odd_2_test	HIGH	Directed	Đ.HUY	FAILED	11072015
full_7_even_1_test	HIGH	Directed	Đ.HUY	FAILED	11072015
full_7_even_2_test	HIGH	Directed	Đ.HUY	FAILED	11072015
full_8_none_1_test	HIGH	Directed	Đ.HUY	PASSED	11072015
full_8_none_2_test	HIGH	Directed	Đ.HUY	PASSED	11072015
full_8_odd_1_test	HIGH	Directed	Đ.HUY	FAILED	11072015
full_8_odd_2_test	HIGH	Directed	Đ.HUY	FAILED	11072015
full_8_even_1_test	HIGH	Directed	Đ.HUY	FAILED	11072015

full_8_even_2_test	HIGH	Directed	Đ.HUY	FAILED	11072015
dynamic_full_test	HIGH	Directed	Đ.HUY	PASSED	11072015
		Directed	Đ.HUY		
parity_er_status_test	HIGH	Directed	Đ.HUY	FAILED	11072015
disable_parity_error_test	HIGH	Directed	Đ.HUY	FAILED	11072015
rx_fifo_empty_status_test	HIGH	Directed	Đ.HUY	PASSED	11072015
disable_ rx_fifo_empty_status_test	HIGH	Directed	Đ.HUY	PASSED	11072015
rx_fifo_full_status_test	HIGH	Directed	Đ.HUY	PASSED	11072015
disable_ rx_fifo_full_status_test	HIGH	Directed	Đ.HUY	PASSED	11072015
tx_fifo_empty_test	HIGH	Directed	Đ.HUY	PASSED	11072015
disable_ tx_fifo_empty_test	HIGH	Directed	Đ.HUY	PASSED	11072015
tx_fifo_full_test	HIGH	Directed	Đ.HUY	PASSED	11072015
disable_ tx_fifo_full_test	HIGH	Directed	Đ.HUY	PASSED	11072015
		Directed	Đ.HUY		
parity_missmatch_test	HIGH	Directed	Đ.HUY	FAILED	11072015
stop_width_missmatch_test	HIGH	Directed	Đ.HUY	PASSED	11072015
data_width_missmatch_test	HIGH	Directed	Đ.HUY	PASSED	11072015
baudrate_missmatch_test	HIGH	Directed	Đ.HUY	PASSED	11072015
write_when_tx_fifo_full_test	HIGH	Directed	Đ.HUY	PASSED	11072015

Remark
Can not test

Parity error
Parity error
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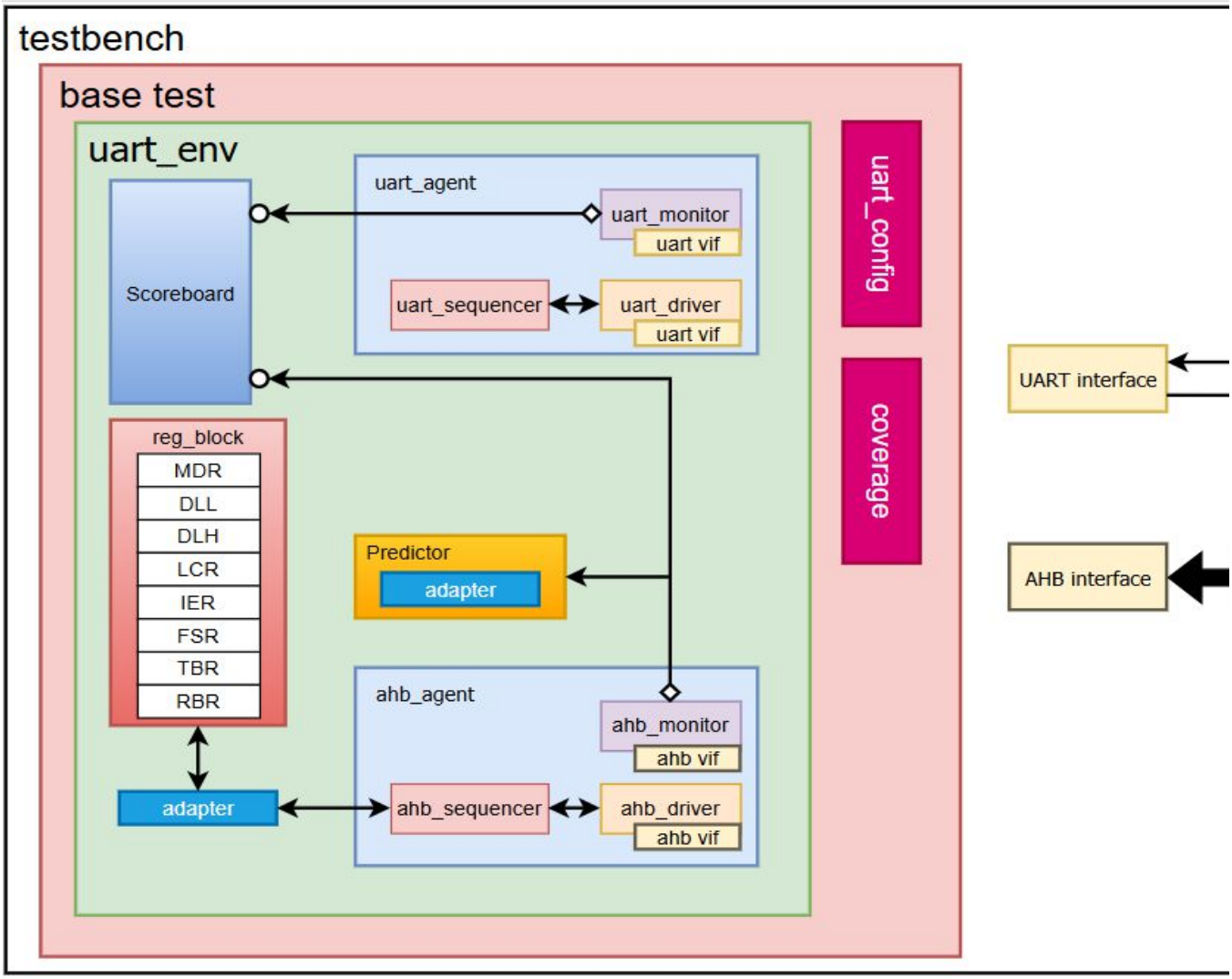
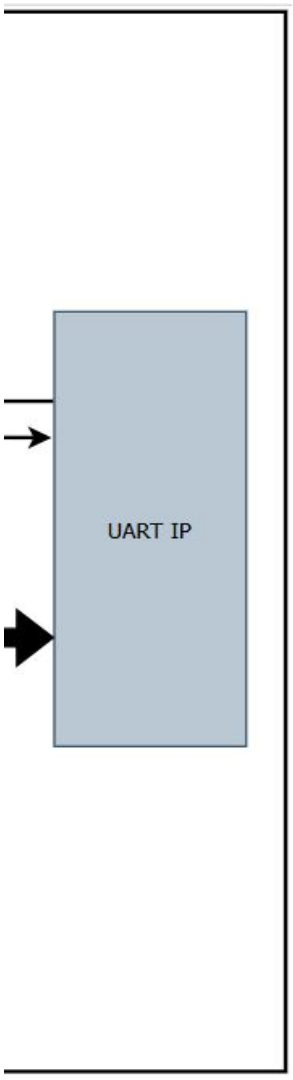
Parity error
Parity error

Parity error
interruprt not trigger
parrity error status not trigger
parrity error status not trigger


testbench
base test
uart_env
uart_agent
uart_monitor
uart vif
Scoreboard
uart_sequencer
uart_driver
uart vif
uart_config
coverage
UART interface
reg_block
MDR
DLL
DLH
LCR
IER
FSR
TBR
RBR
Predictor
adapter
AHB interface
ahb_agent
ahb_monitor
ahb vif
adapter
ahb_sequencer
ahb_driver
ahb vif


UART IP