

## Lab3

### 1 Introduction

#### 1.1 Aims

- Implement half adder, full adder circuit.
- Practice with different adder circuits.

#### 1.2 Requirements

- Understand how to implement an adder circuit.
- Have ability to combine the small circuits to implement the bigger ones.

#### 1.3 Procedure

- Verify the gates.
- Make the connections as per the circuit diagram.
- Switch on  $V_{cc}$  and apply various combinations of input according to the truth table.
- Note down the output readings for half/full adder and half/full subtractor sum/difference and the carry/borrow bit for different combinations of inputs.

#### 1.4 Report Requirements

Your report of each exercise should include:

- Answer and explain all questions (If required).
- The circuit and truth table of each exercise.
- Two or Three photos of the circuit **on KIT**.

## 2 Contents

### 2.1 Half/Full Adder

#### 2.1.1 Using X-OR and Basic Gates

##### Half Adder

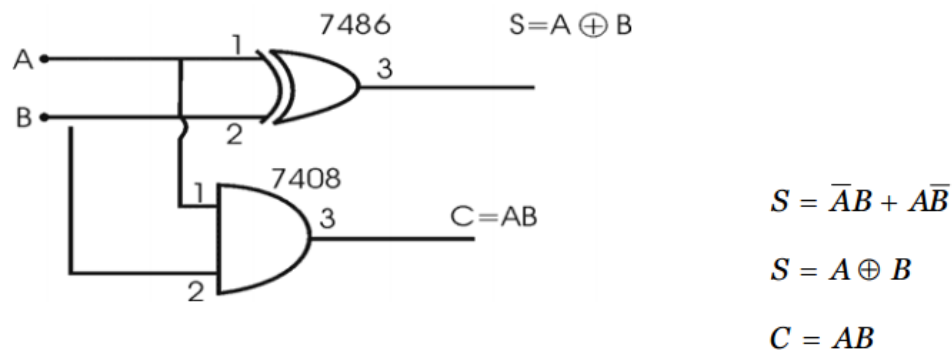


Figure 1: Half Adder circuit with X-OR and Basic Gates.

##### Full Adder

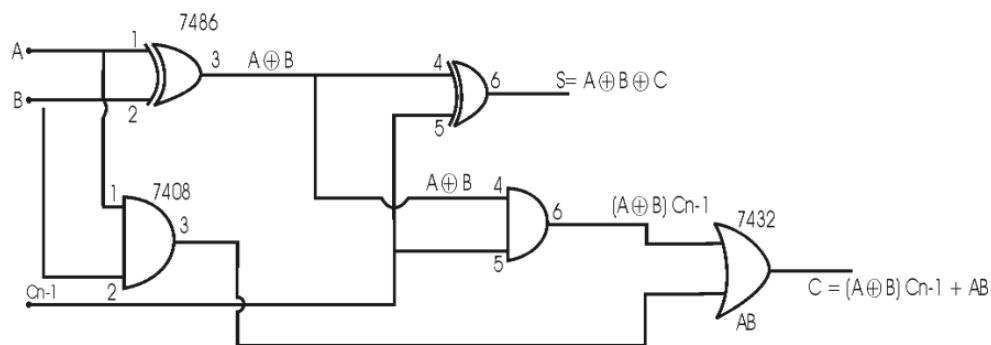


Figure 2: Full Adder circuit with X-OR and Basic Gates.

#### 2.1.2 Using only NAND gates

##### Half Adder

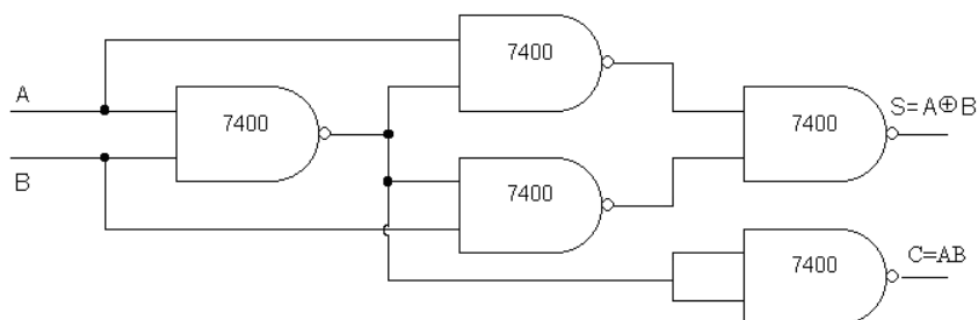


Figure 3: Half Adder circuit with only NAND gates.

## Full Adder

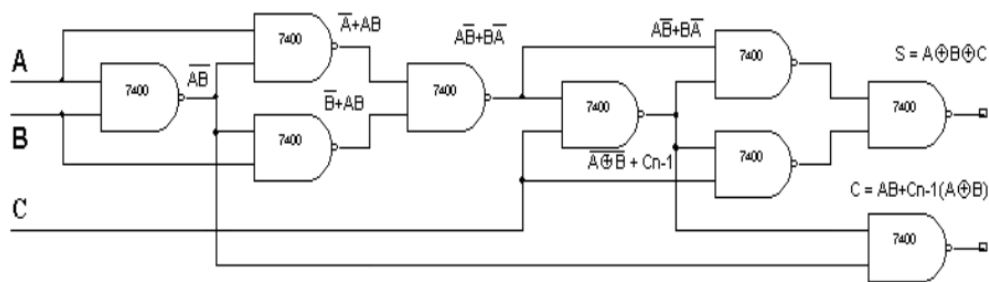


Figure 4: Full Adder circuit with only NAND gates.

## 2.2 Half/Full Subtractor

### 2.2.1 Using X-OR and Basic Gates

#### Half Subtractor

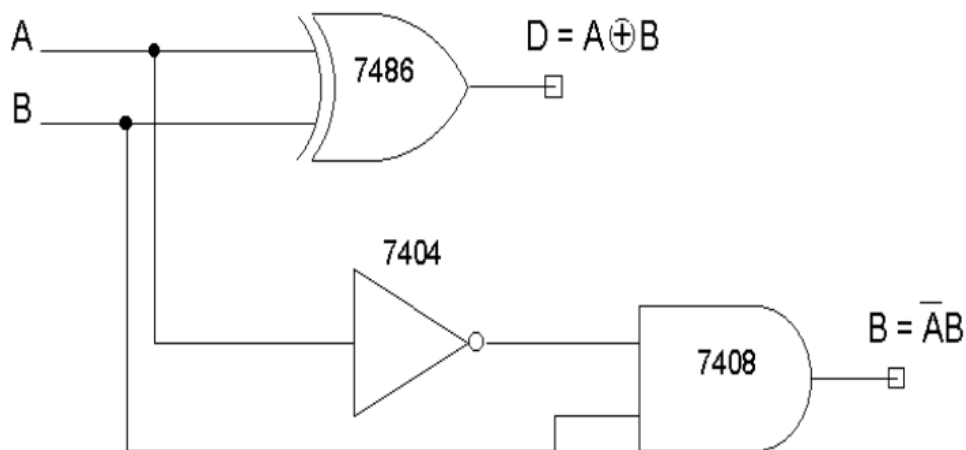


Figure 5: Half Subtractor circuit with X-OR and Basic Gates.

#### Full Subtractor

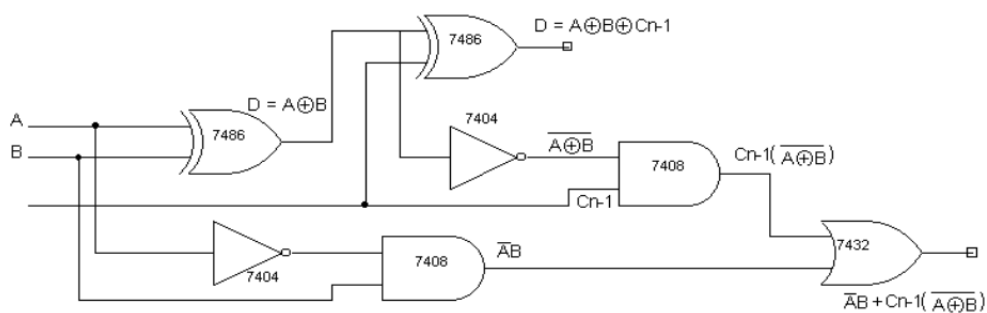


Figure 6: Full Subtractor circuit with X-OR and Basic Gates.

### 2.2.2 Using only NAND gates

#### Half Subtractor

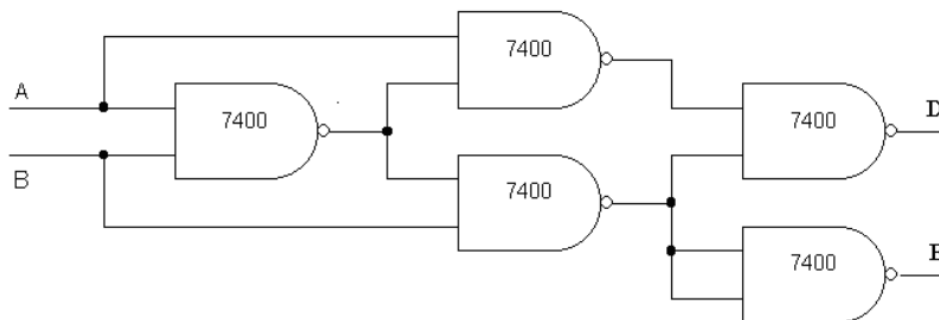


Figure 7: Half Subtractor circuit with only NAND gates.

#### Full Subtractor

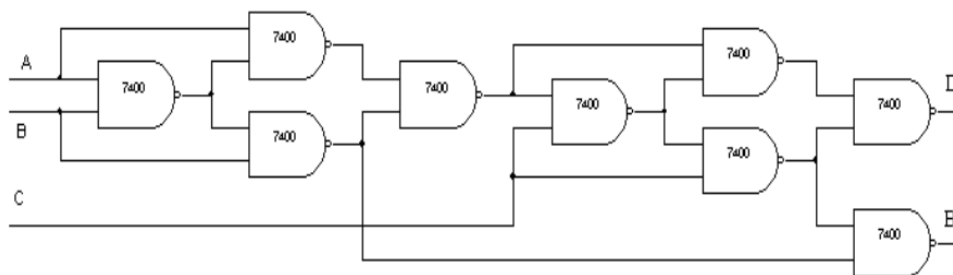


Figure 8: Full Subtractor circuit with only NAND gates.

Fill in these tables:

Half Adder					
A	B	S	C	S(V)	C(V)
	0	0	0		
0	1	1	0		
1	0	1	0		
1	1	0	1		

Half Subtractor					
A	B	D	B	D(V)	B(V)
0	0	0	0		
0	1	1	1		
1	0	1	0		
1	1	0	0		

Full Adder						
A	B	Cn-1	S	C	S(V)	C(V)
0	0	0	0	0		
0	0	1	1	0		
0	1	0	1	0		
0	1	1	0	1		
1	0	0	1	0		
1	0	1	0	1		
1	1	0	0	1		
1	1	1	1	1		

Full Subtractor						
A	B	Cn-1	D	B	D(v)	B(v)
0	0	0	0	0		
0	0	1	1	1		
0	1	0	1	1		
0	1	1	0	1		
1	0	0	1	0		
1	0	1	0	0		
1	1	0	0	0		
1	1	1	1	1		

### 3 Exercises

**Exercise 1:** Implement a half subtractor circuit use **only** NAND gate. Show results on LED diode.

**Exercise 2:** Implement full adder circuit **from the half adder**  
The full adder circuit must have 3 inputs: bit A, bit B and carry bit. Show results on LED diode.

**Exercise 3:** Implement an adder that can be work out the sum of two 2-bits numbers by using full adder circuit. Show results on both LED diot and 7-seg LED.