Laboratory 2: Oscilloscope

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III. Exercises

Exercice 1: Measurement Propagation Delay

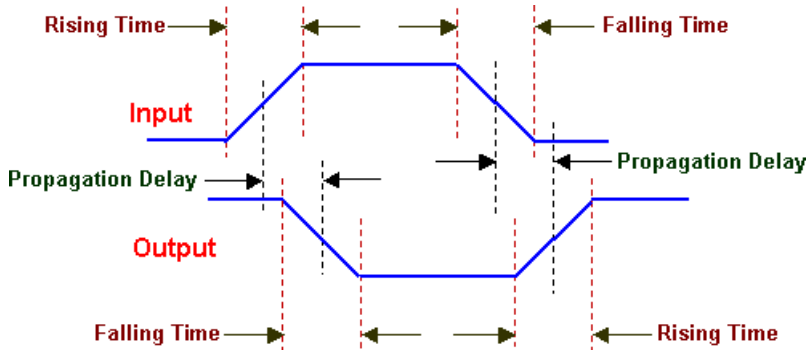
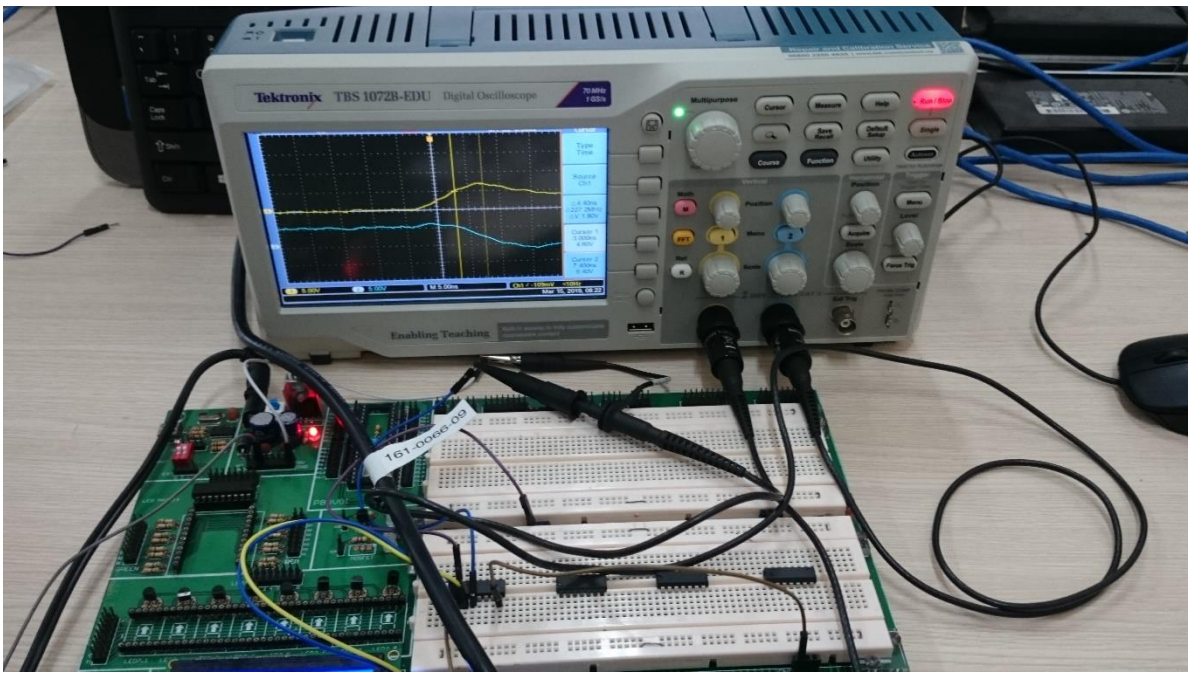


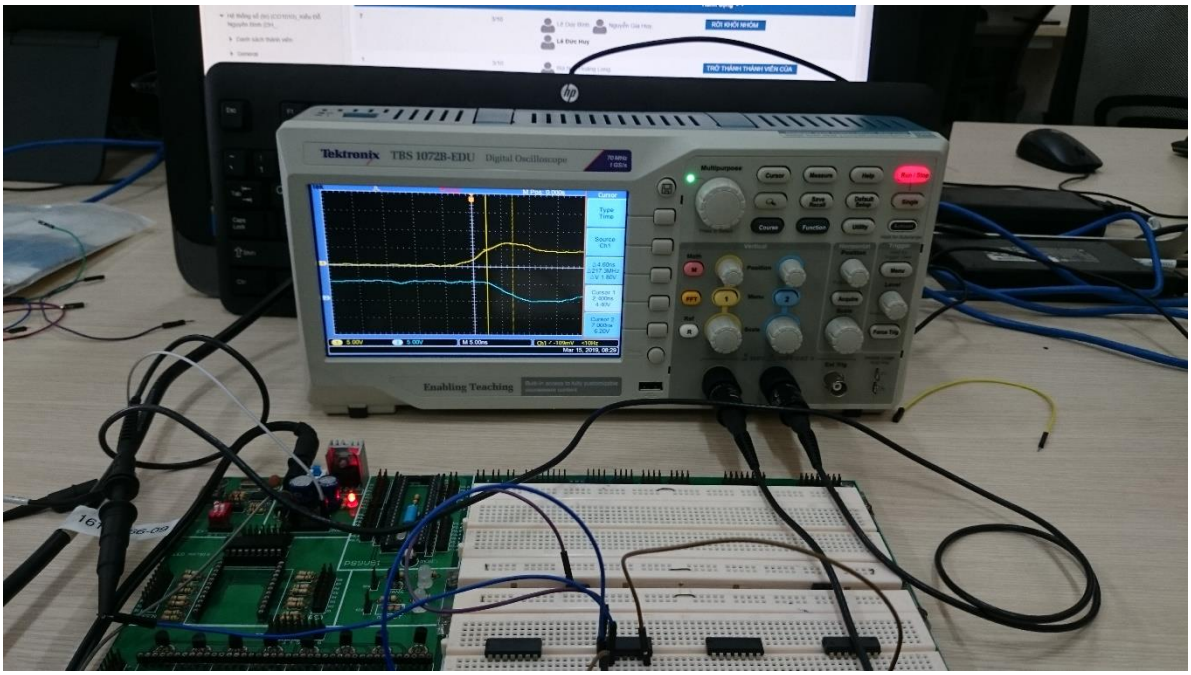
Figure 1: Propagation Delay

Use oscilloscope for measure propagation delay of these following ICs and fill these gaps below:

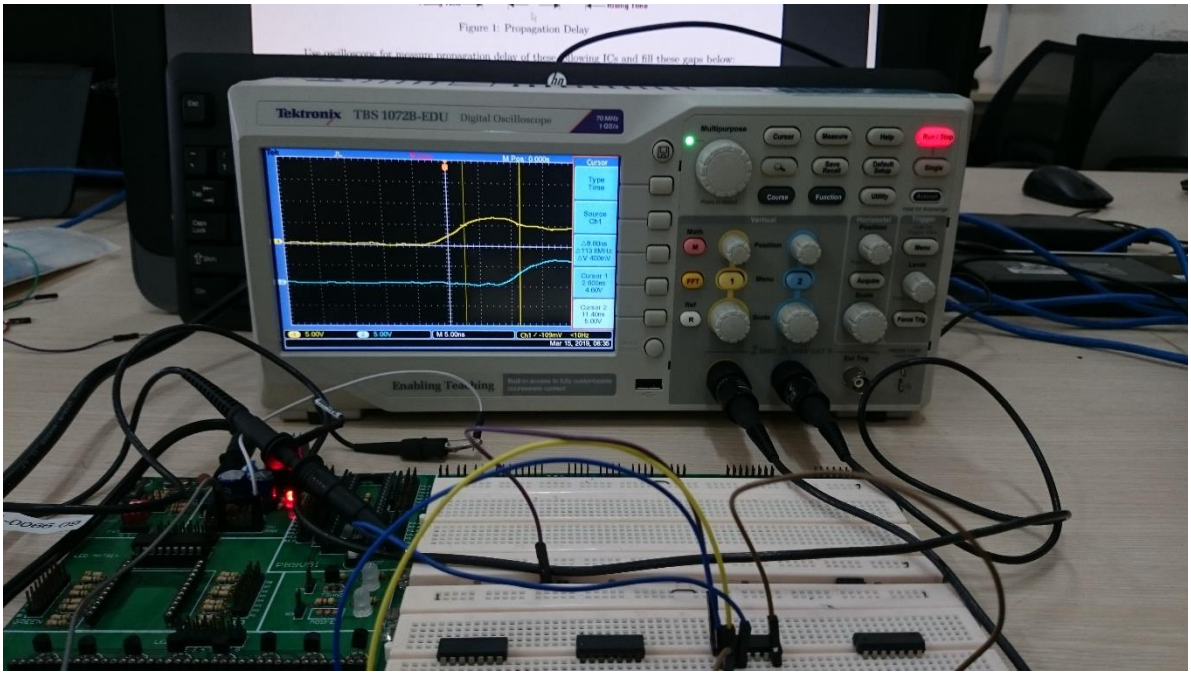
7400: 4.4 ns



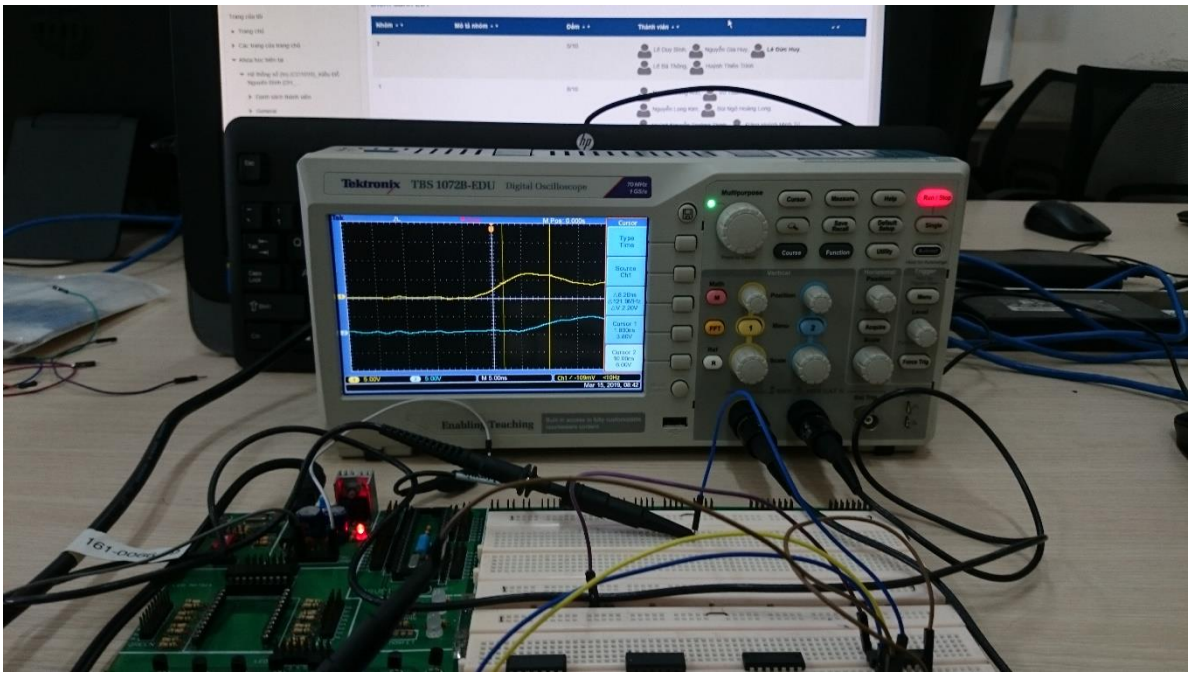
7404: 4.6 ns



7408: 8.8 ns



7432: 8.2 ns



Exercice 2: Egde Detector Circuit
Implement 1 on 3 circuits below and test it by using oscilloscope:

1. Use IC 7404 and 7408 to implement edge detector circuit.
2. Use IC 7404 and 7432 to implement edge detector circuit.
3. Use only IC 7400 to implement edge detector circuit. (+1 bonus)

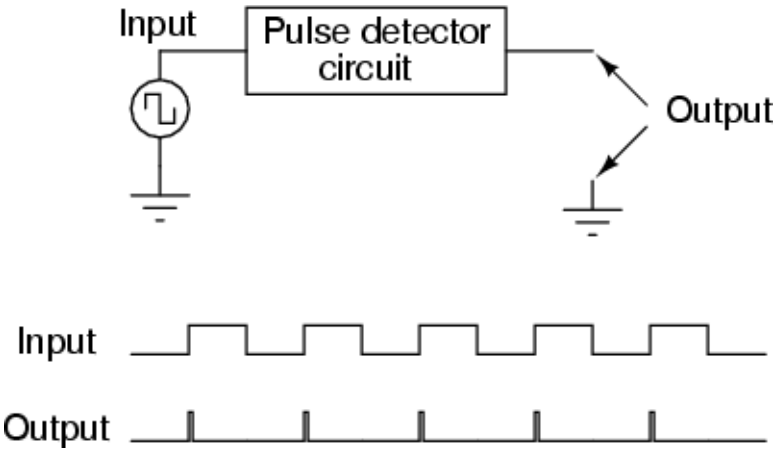


Figure 2: How edge detector circuit works

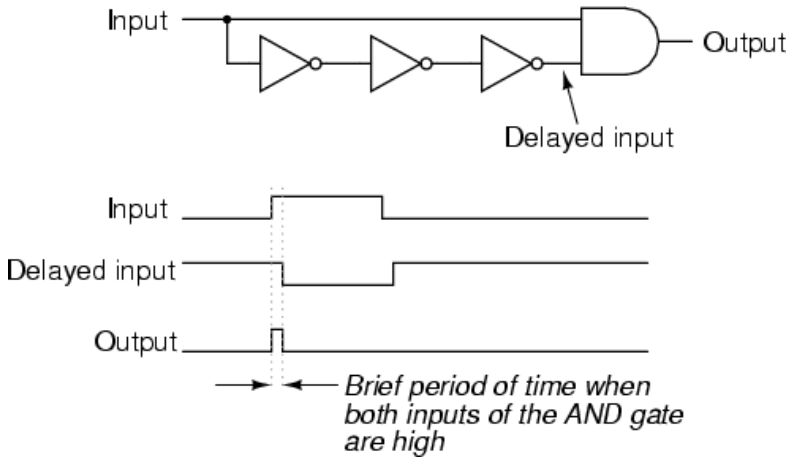
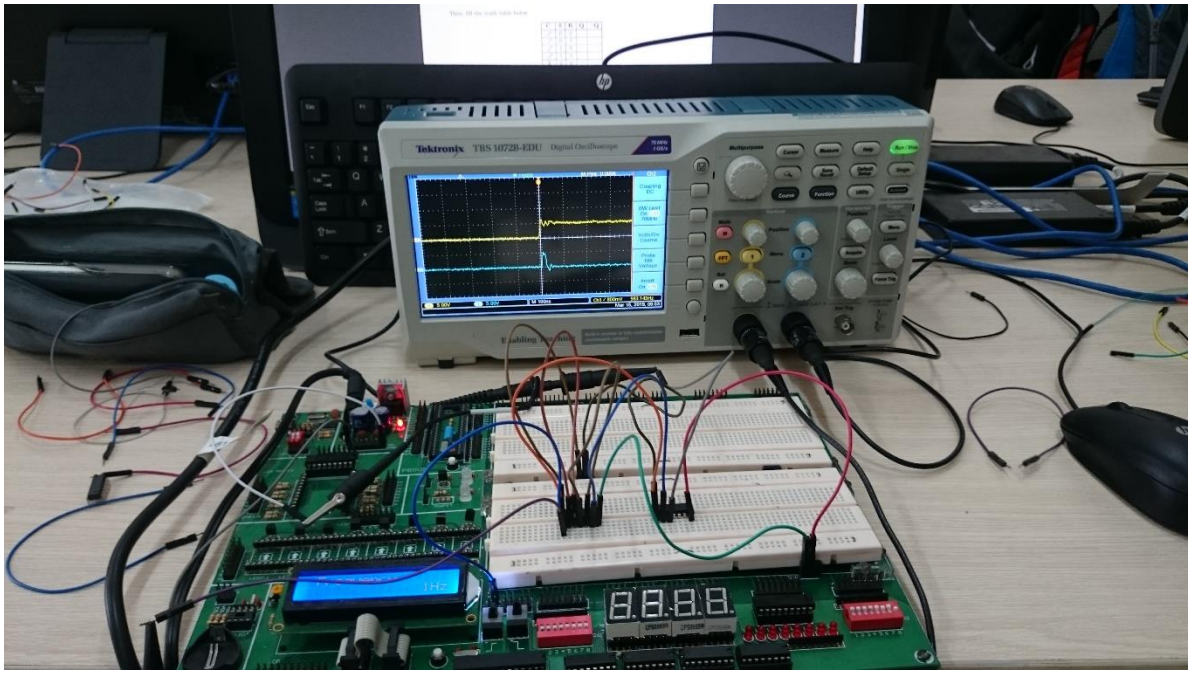


Figure 3: Sample edge detector circuit design



Exercice 3: (Extend Exercises) Implement the circuit below using edge detector circuit in Ex2.

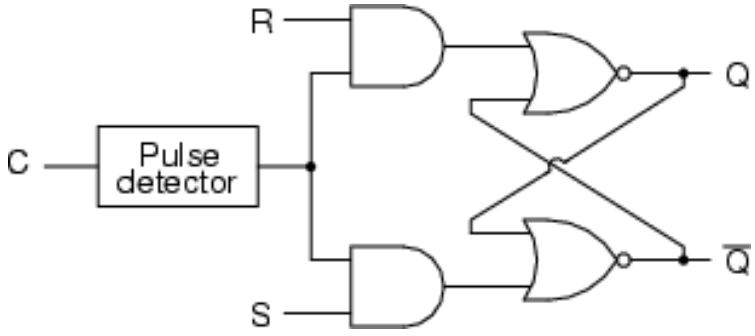


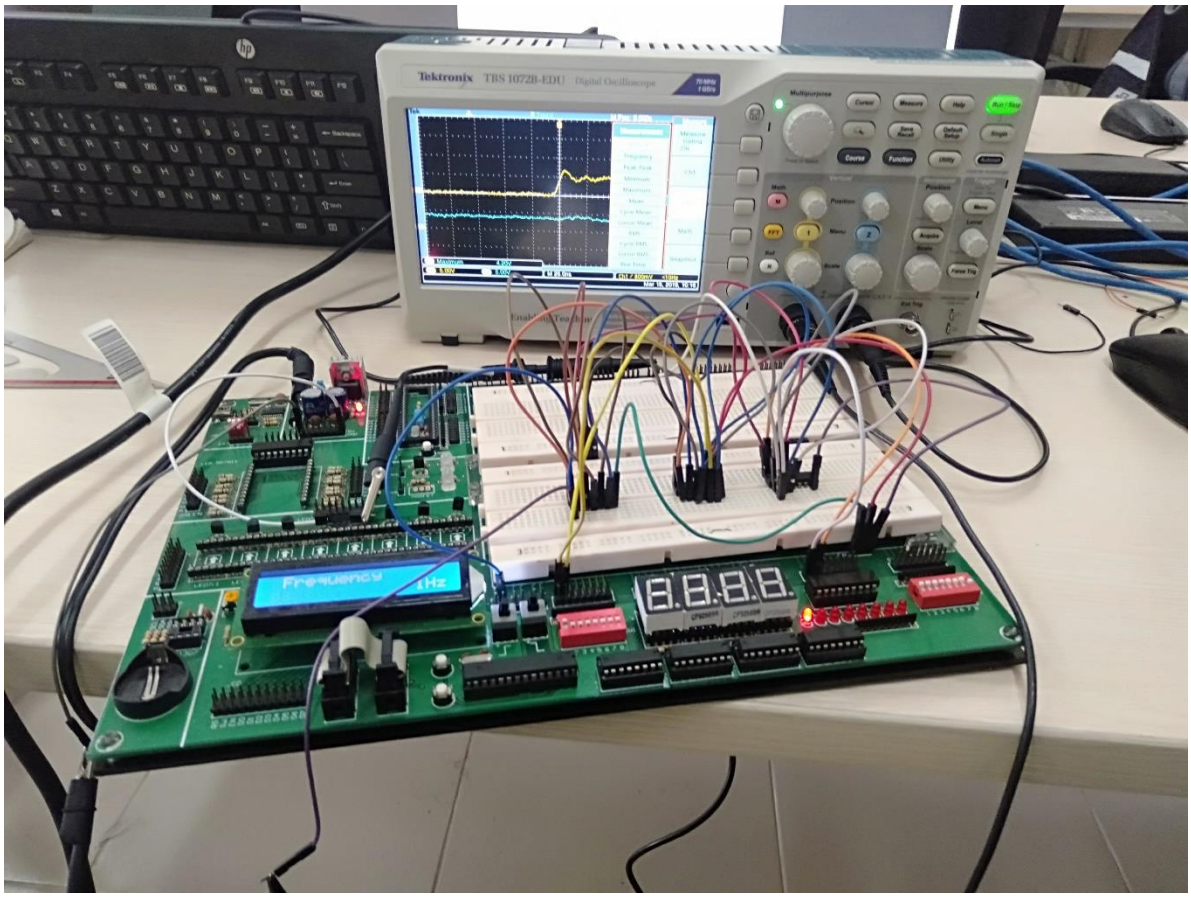
Figure 4: SR-Latch Design

Then, fill the truth table below.

C	S	R	Q	¬Q
⎍↑	0	0	NC	NC
⎍↑	0	1	0	1
⎍↑	1	0	1	0
⎍↑	1	1	Invalid	Invalid
X	0	0	X	X
X	0	1	X	X
X	1	0	X	X
X	1	1	X	X

Table 1: SR-Latch Truth Table

Test circuit using Oscilloscope (Channel 1 for C signal, Channel 2 for Q signal) and describe the function of this circuit.



The function of SR flip-flop is storing one of the two stable voltage levels (binary value 0 and 1) until a new voltage level is written to. The circuit only changes state when clock pulse is present. This circuit is triggered by positive-going transition of clock signal and has active-HIGH inputs :

- Case 1: When S=R=0 and the clock pulse is applied, the output remains in the present state (no change).
- Case 2: When S=0, R=1 (reset) and the clock pulse is applied, the output at Q is reset to 0 and ¬Q=1.
- Case 3: When S=1 (set), R=0 and the clock pulse is applied, the output at Q is set to 1 and ¬Q=0.
- Case 4: When S=R=1 and the clock pulse is applied, the output state is unpredictable since it will try to set and reset the latch at the same time. This condition should be avoided.
- Case 5: When no clock pulse is applied, the circuit will not respond to any conditions of the inputs, therefore the output remains in the present state.