VIETNAM NATIONAL UNIVERSITY HO CHI MINH CITY

HO CHI MINH UNIVERSITY OF TECHNOLOGY

ASSIGNMENT REPORT IC DESIGN – EE3165

LAB 2 : DIGITAL LOGIC CIRCUIT

CLASS L04 – GROUP 14

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OBJECTIVES

No.	Objective	Requirement
1	Implement logic gates using CMOS technology: ➢ NAND2 and NOR2. ➢ EX-OR2.	▪ Complete the truth table, schematic, and symbol for each component. ▪ Run DC analysis and transient simulation. ▪ Create layouts for each logic gate, then show DRC confirmation and corresponding schematic with proof of LVS.
2	Implement basic combinational component: ➢ 2-to-1 channel multiplexer.	
3	Implement simple storage elements: ➢ Single-positive-edge-triggered Modified TSPC D flip-flop.	▪ Demonstrate latch and flip-flop by studying a D latch and a D flip-flop using transmission gates. ▪ Complete the truth table, schematic, and symbol for each component then run transient simulation. ▪ Known definitions, and how to measure setup time, propagation, and hold time. ▪ Find the clock frequency of this element.
4	**[OPTIONAL]** Review the operation of pass transistor, transmission gate, and tristate inverter.	▪ Analyze the charge and discharge period of MOS transistors, then prove by simulation. ▪ Analyze operations of a transmission gate, then prove by simulation. ▪ Analyze operations and topologies of a tristate inverter, then prove by simulation.

<u>EXPERIMENT 1</u> : Know how to design CMOS gate using CMOS technology.

Requirements *:*

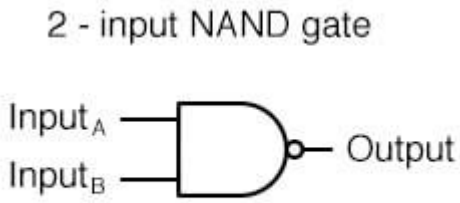
- Completet truth table, schematic, and symbol for NAND2, NOR2, and EX-OR2

- Run DC simulation and transient analysis

- Create layout and show DRC and LVS check screen

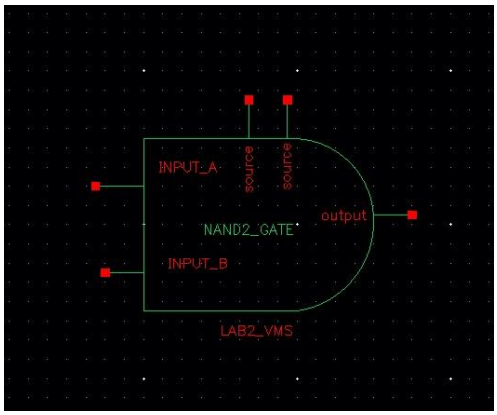
1. NAND2

The truth table of NAND2 gate and its symbol

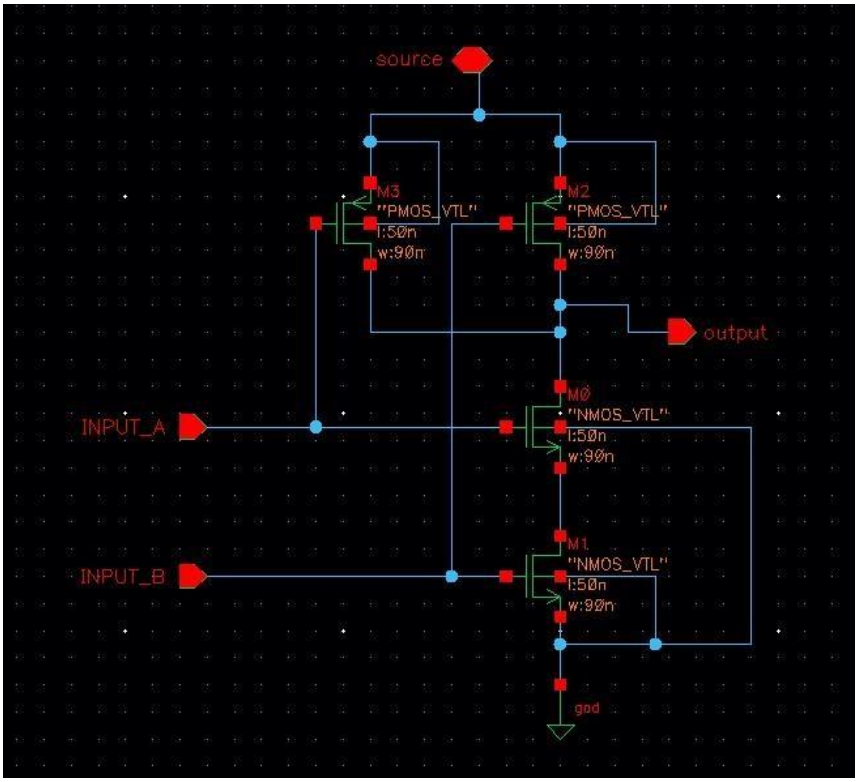


A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

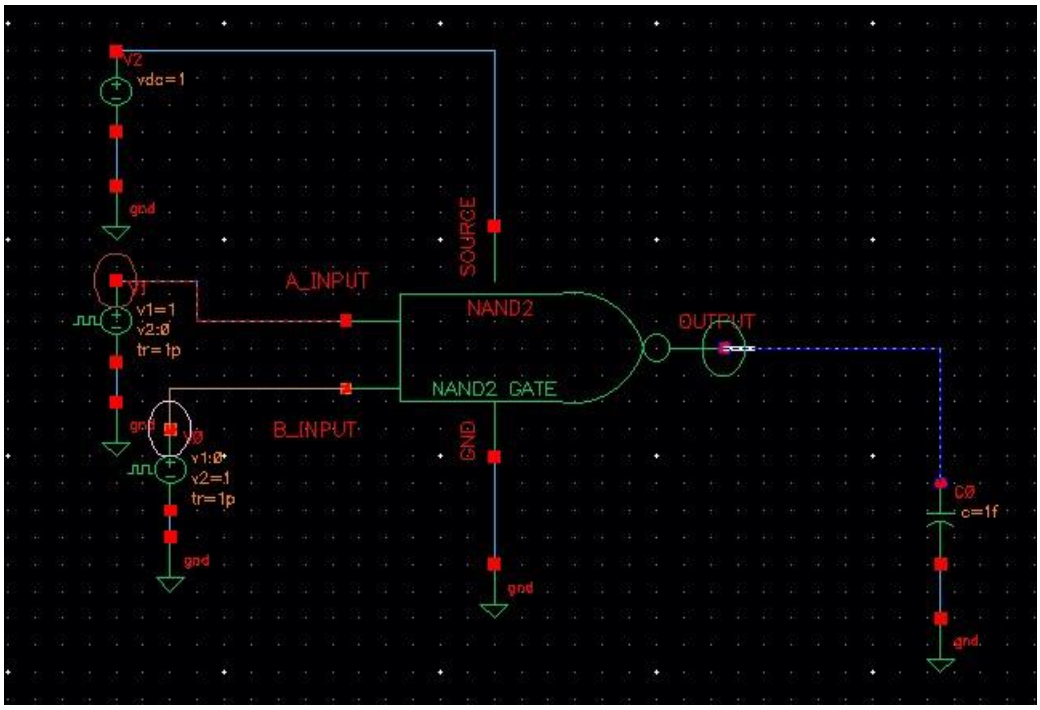
Firstly, I create NAND2 symbol but my symbol is lack of circle.

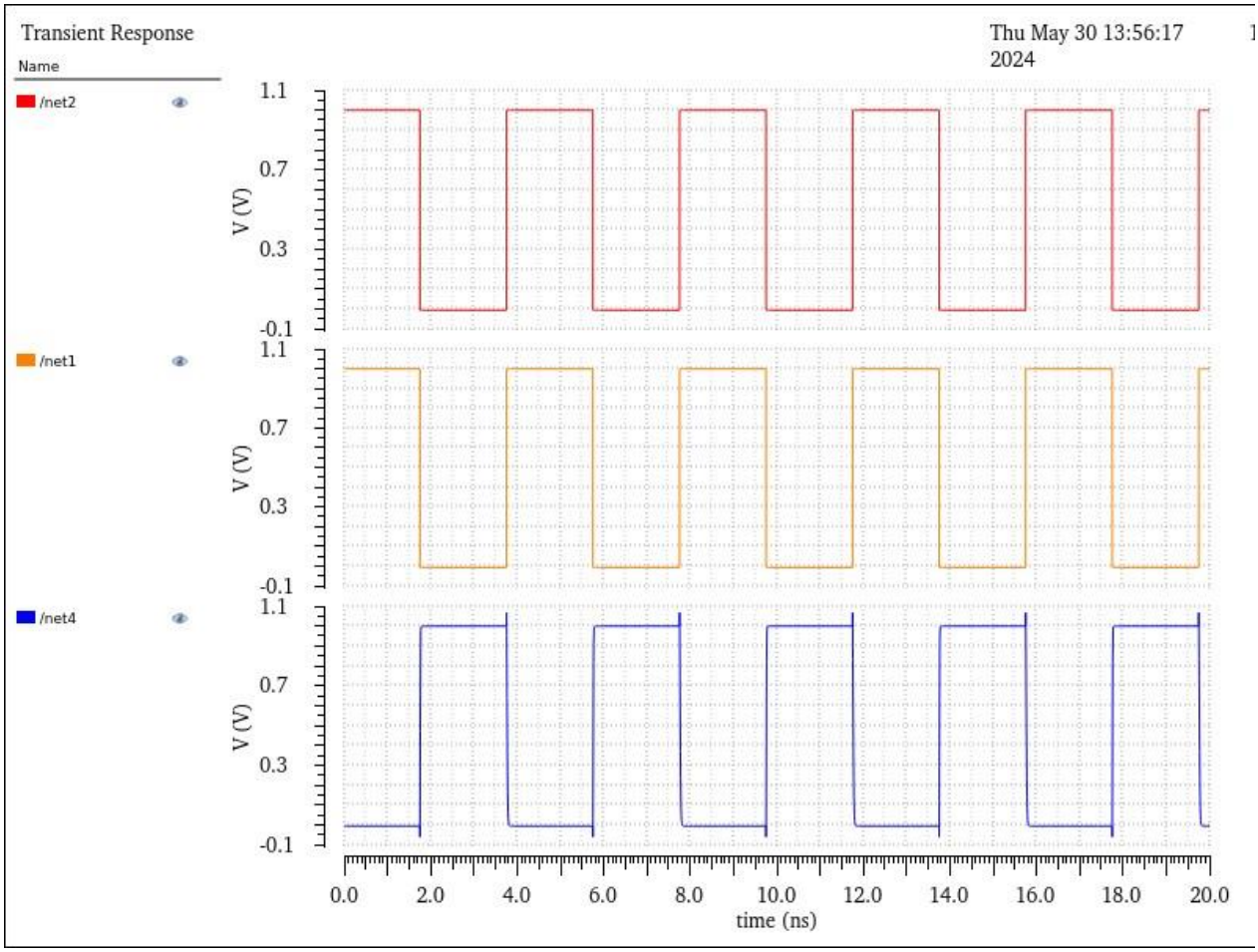


NAND2 schematic



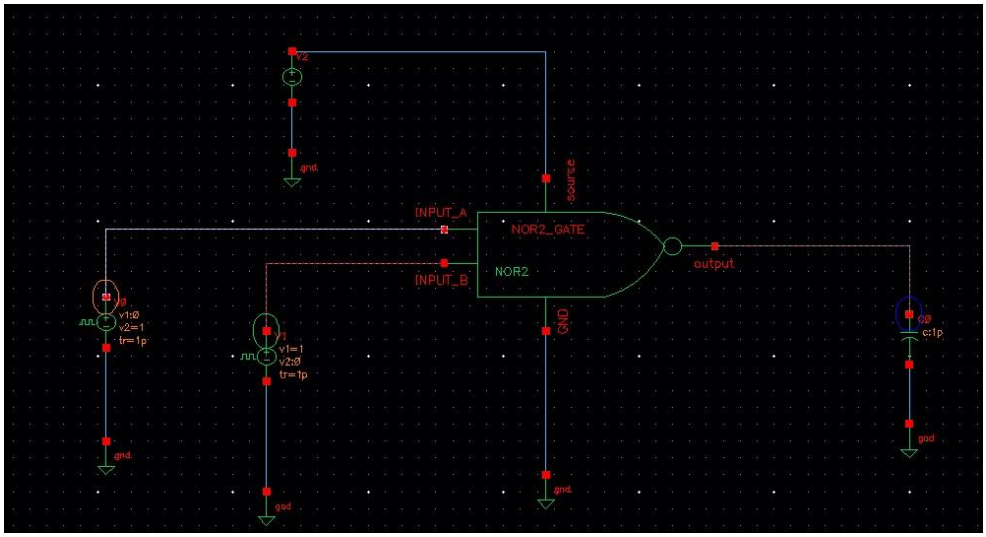
My testbench is designed as



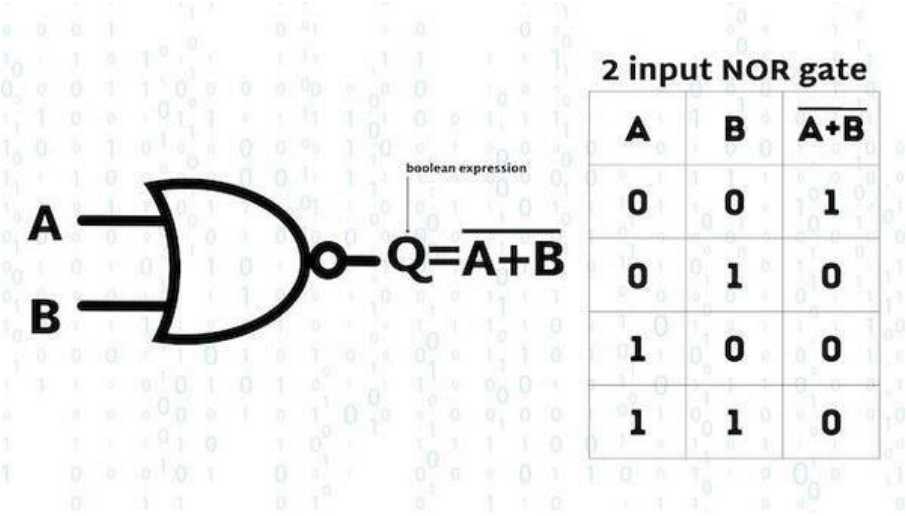


Transient simulation with 20n s **2.**

NOR2



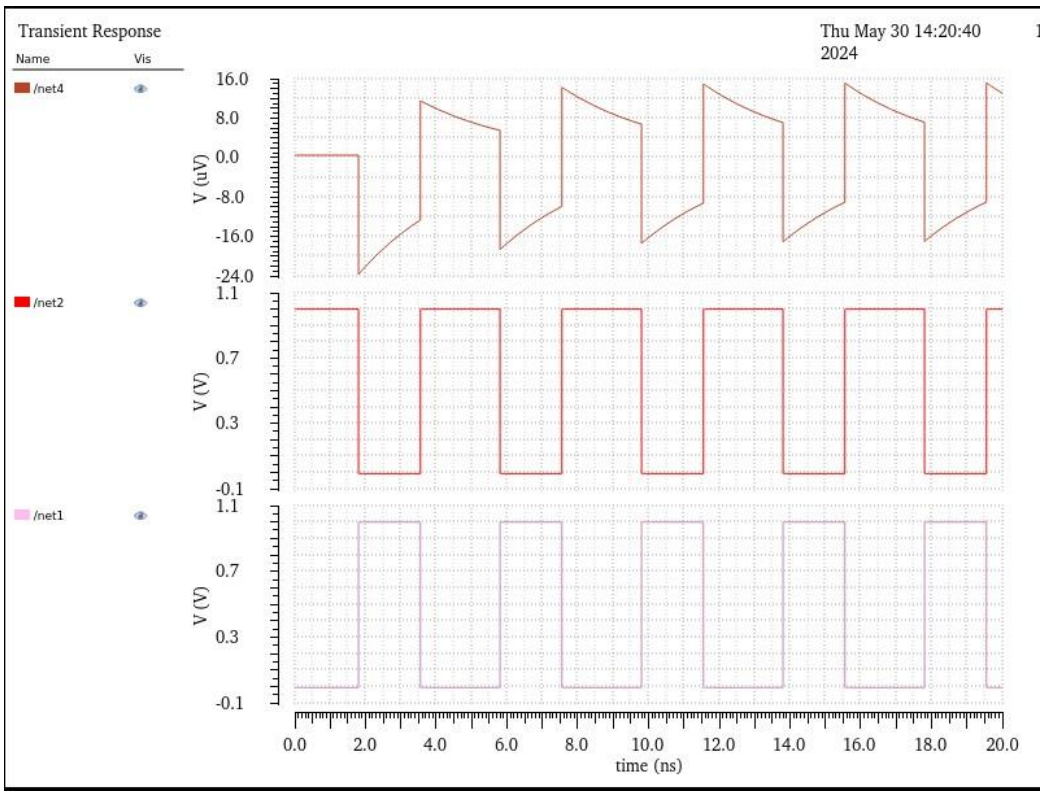
Here is my schematic and testbench for NOR2 the symbol is created as the figure below. And the testbench included 2 pulse source and a Vdc source.



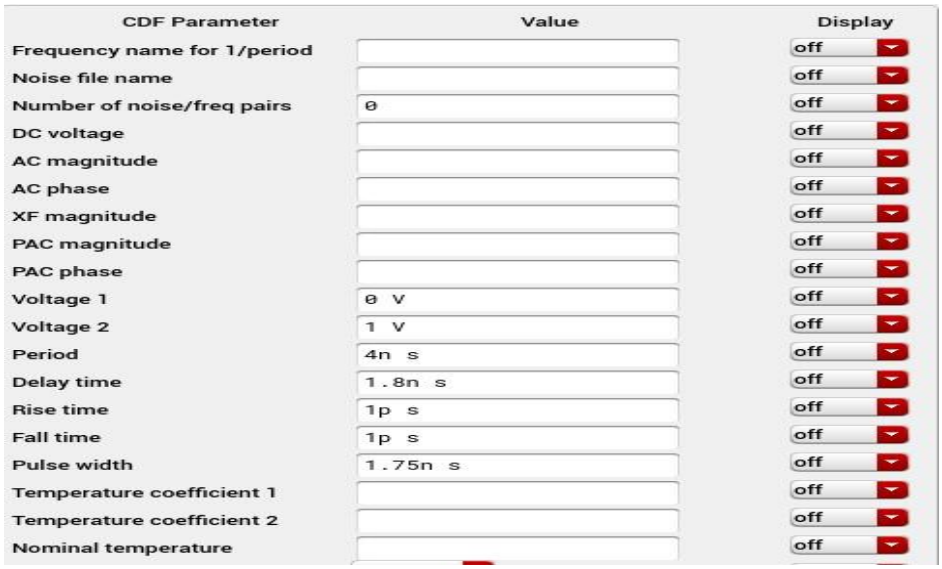
2 input NOR gate

A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

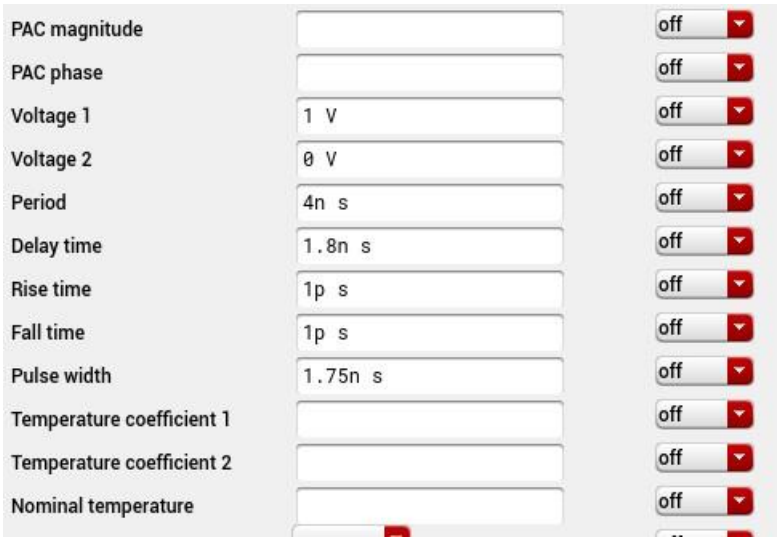
The simulation is showed with the transient of 20n s.



The plot is not perfectly the pulse source because of the setting is as the figure below :



This is the vpulse of the input B



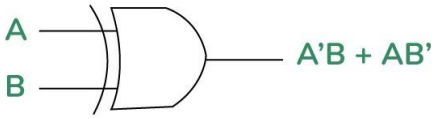
This is the vpulse of the input A

3. EX-OR

The figure below shows the EX-OR truth table and its symbol. As the theory, EXOR is created by 2 input A and B. And a AND gate and NOR gate.

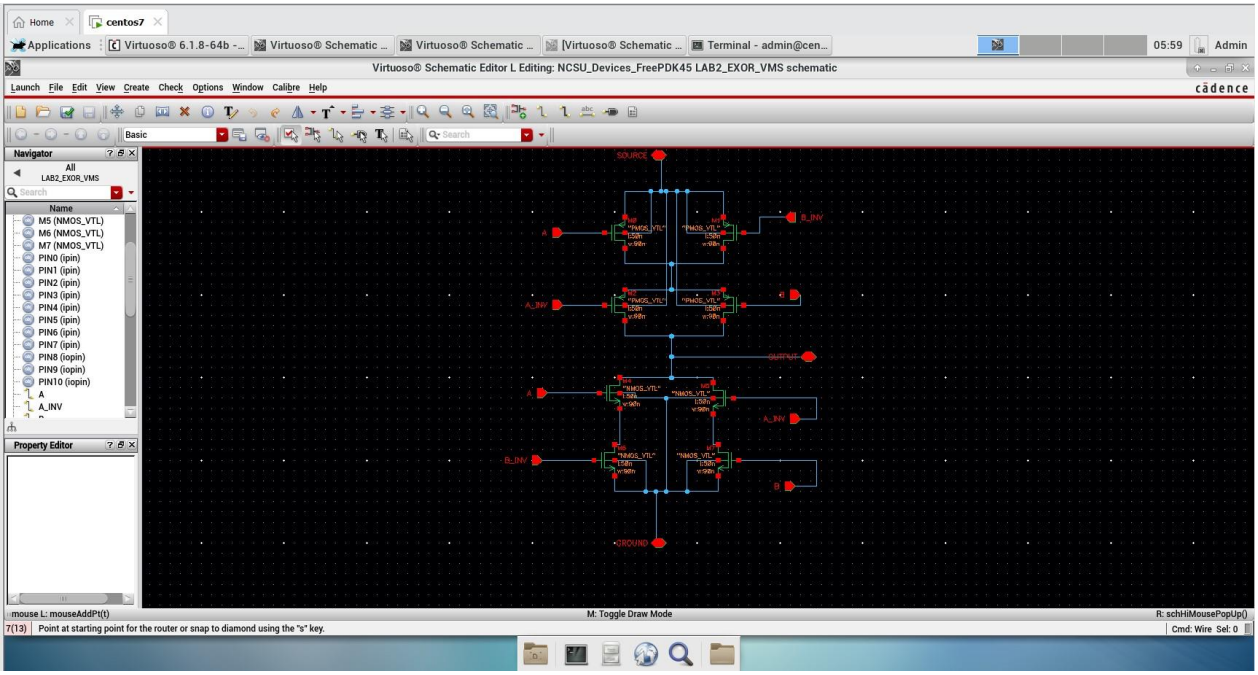
For creating EX-OR, I simulate by schematic of CMOS gate with an inverter of each inputs. By the way, we can create by using NAND2 and NOR2 gate before.

XOR Gate



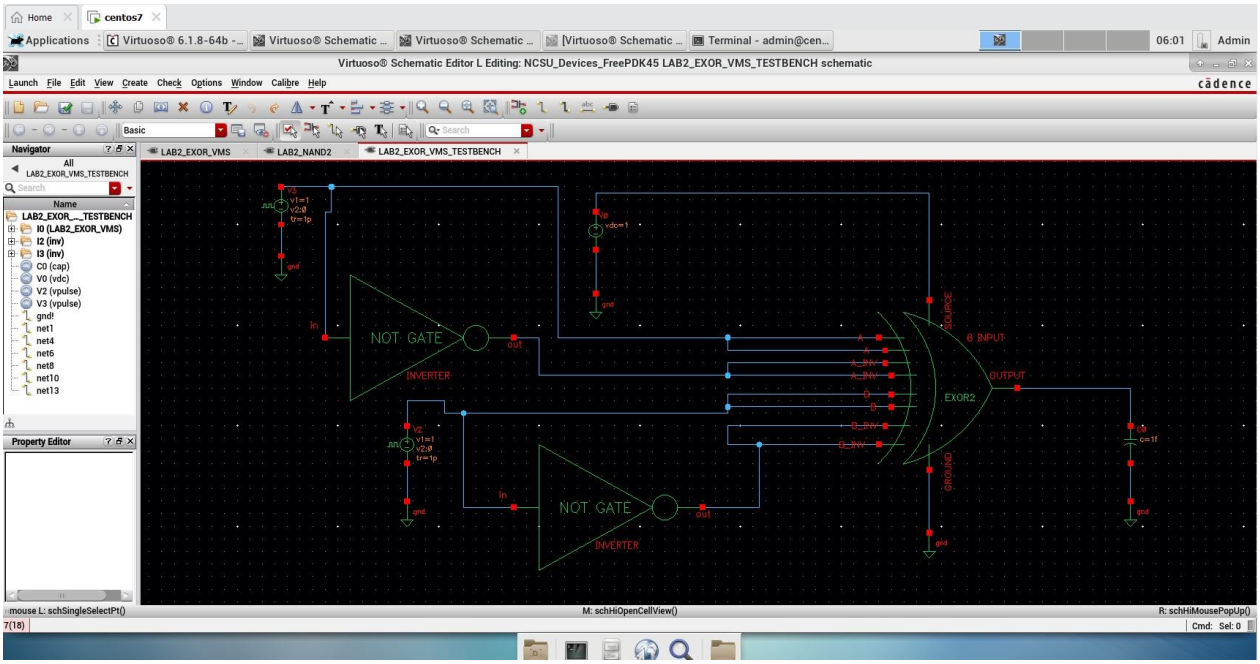
Truth Table

A (Input 1)	B (Input 2)	X = A'B + AB'
0	0	0
0	1	1
1	0	1
1	1	0

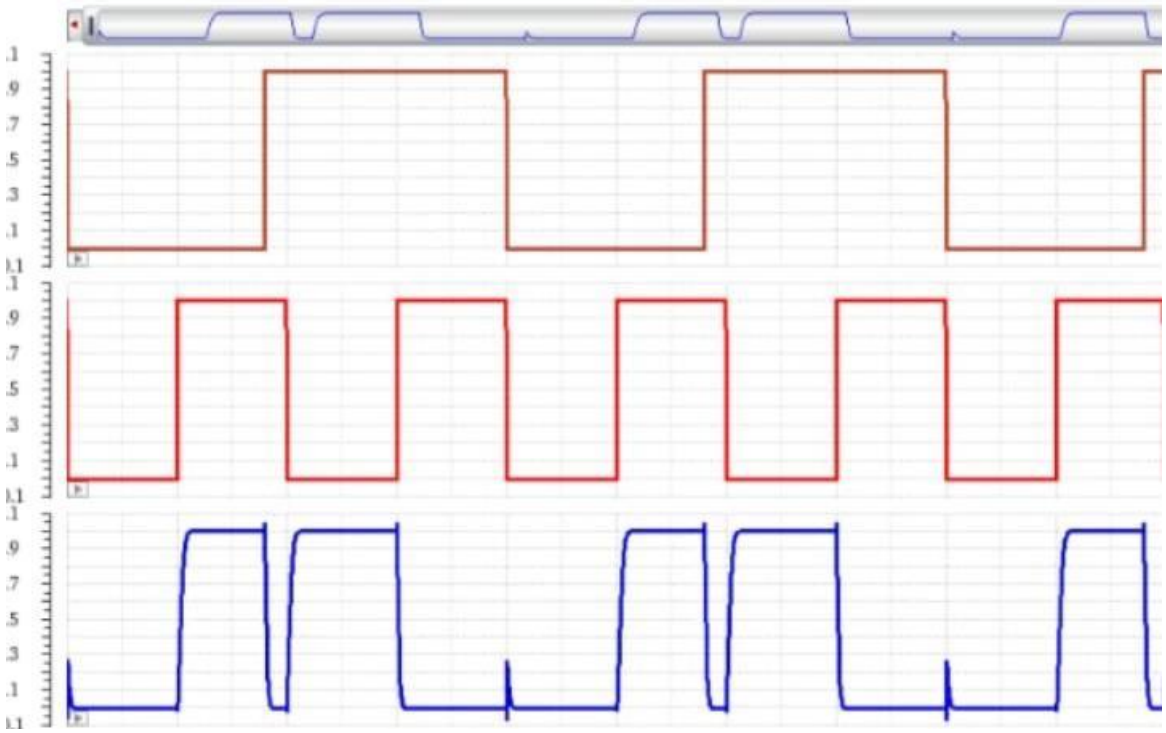


The schematic of EX-OR gate

I used compound gate theory to create this schematic with 4 inputs. But we need an inverter for creating this gate. So that the symbol I create for simulation included 4 inputs.



The result of the simulation is showed as below.



I deleted the current state of the simulation tools, the result shows that the edge rising directively affected to the wave.

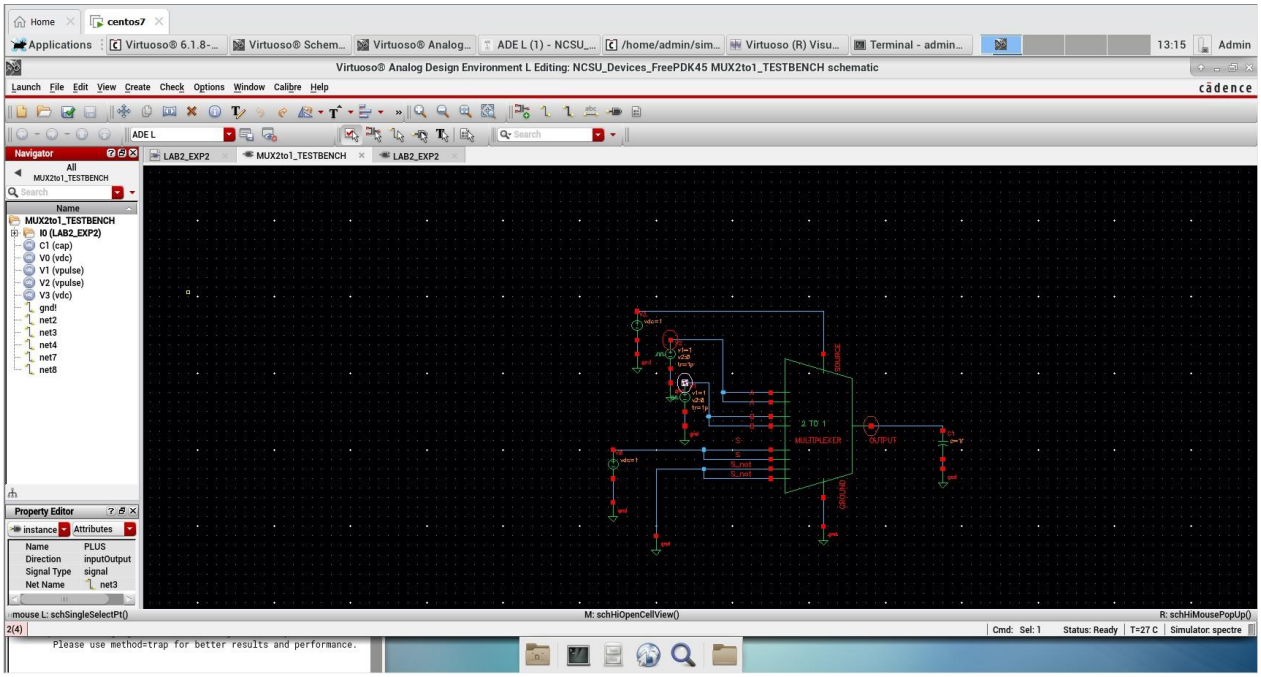
V_{in1}(V)	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
V_{in2}(V)	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
V_{out}	999mV	996.3mV	971.2mV	398.2mV	29mV	999mV	999mV	999V	999V	999V

EXPERIMENT 2 : Implement basic combinational component.

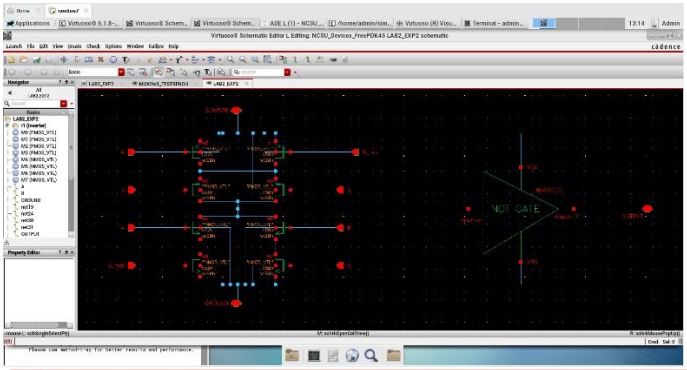
Requirements:

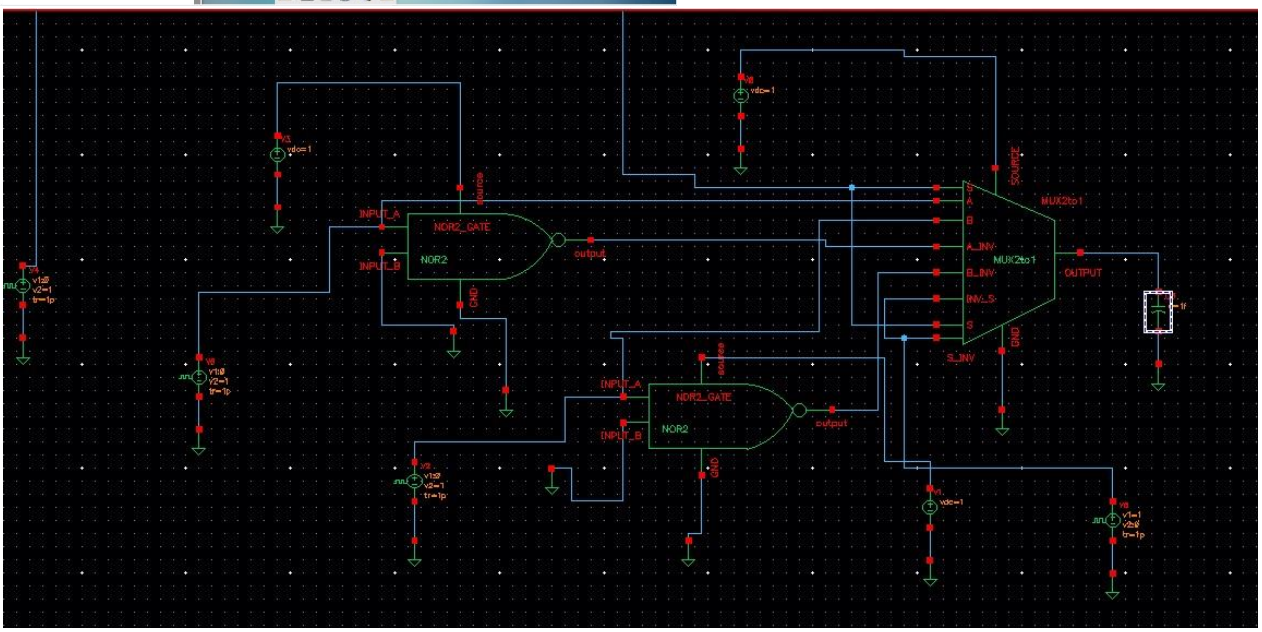
- Complete the truth table, schematic, and symbol for a 2-to-1 channel multiplexer using compound gate.
- Run DC analysis and transient simulation.
- Create layouts for each logic gate, then show DRC confirmation and corresponding schematic with proof of LVS.

My multiplexers

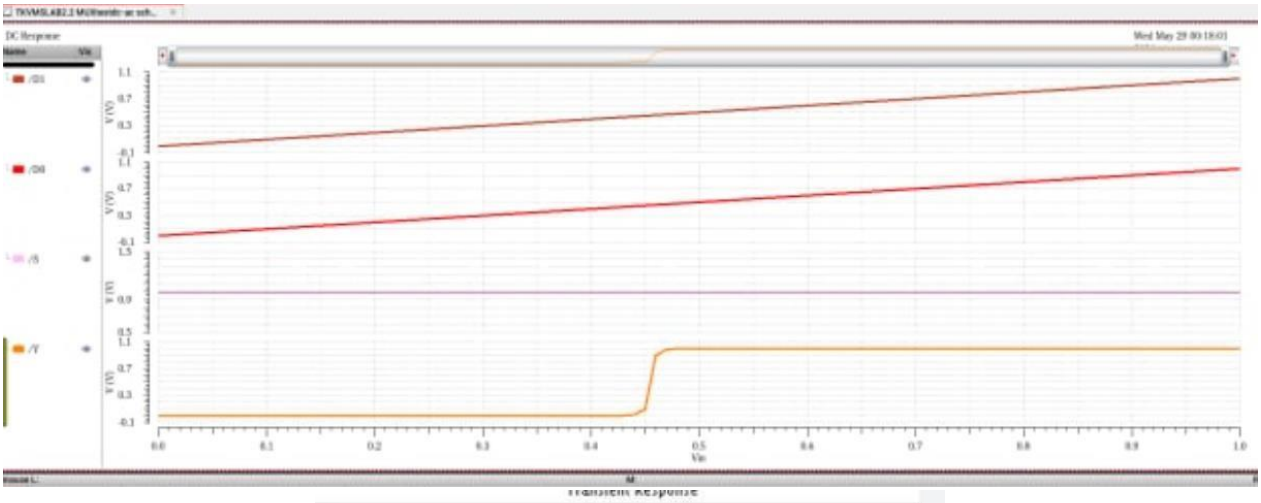


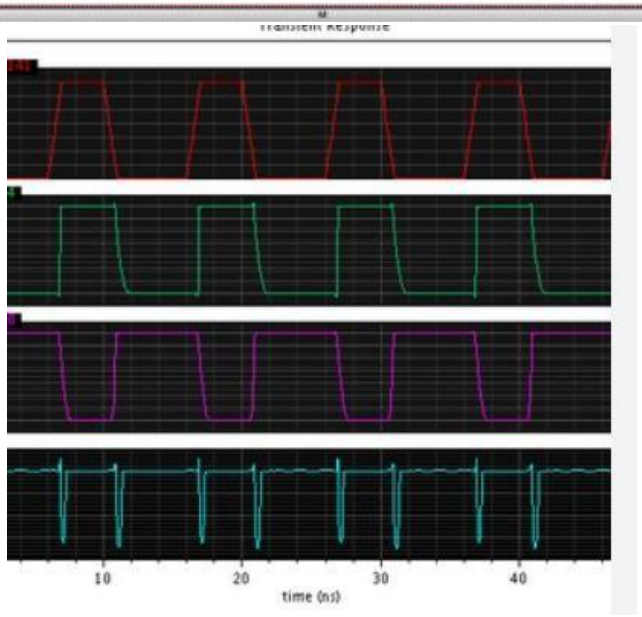
I used MUX2 to 1 as the schematic above with the testbench My schematic is



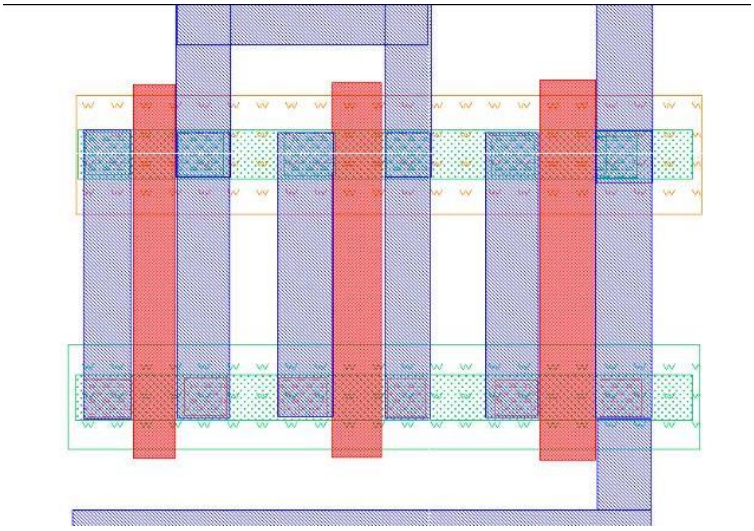


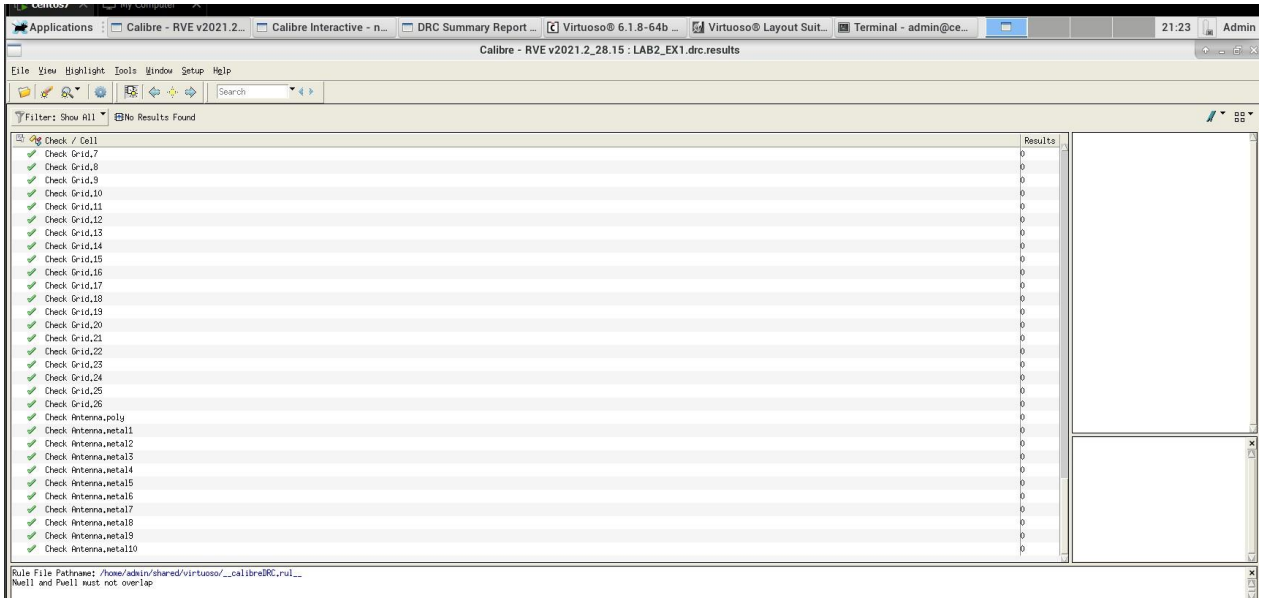
DC simulation





	S	D0	D1
V1	0	0	0
V2	1	1	1
Period	4n	3n	2n
Delay time	0	0	0
Rise time	1p	1p	1p
Fall time	1p	1p	1p
Pulse width	2n	1.5n	1n

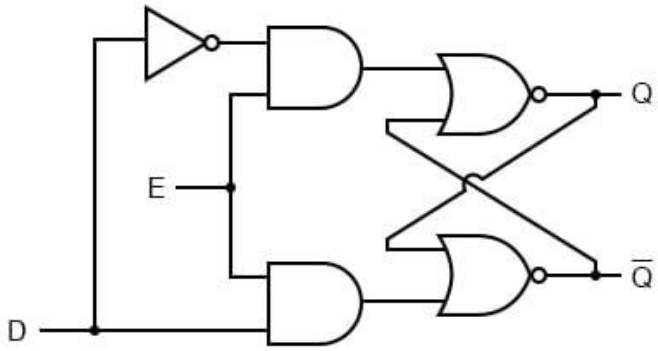




DRC check

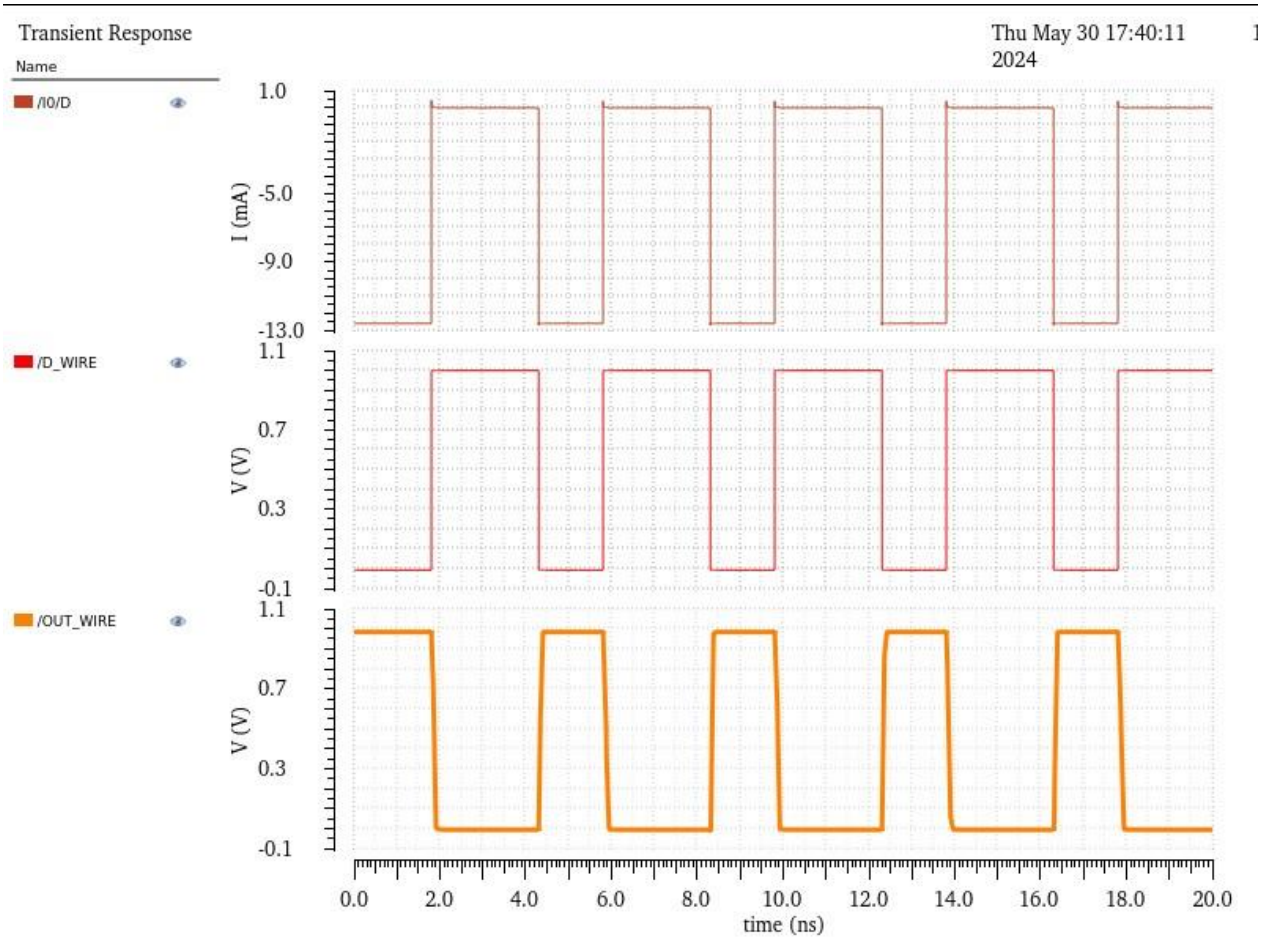
<u>EXPERIMENT 3</u> : Implementing simple storage elements- single-positive – edge triggered Modified TSPC D flip-flop.

Latch D demonstration

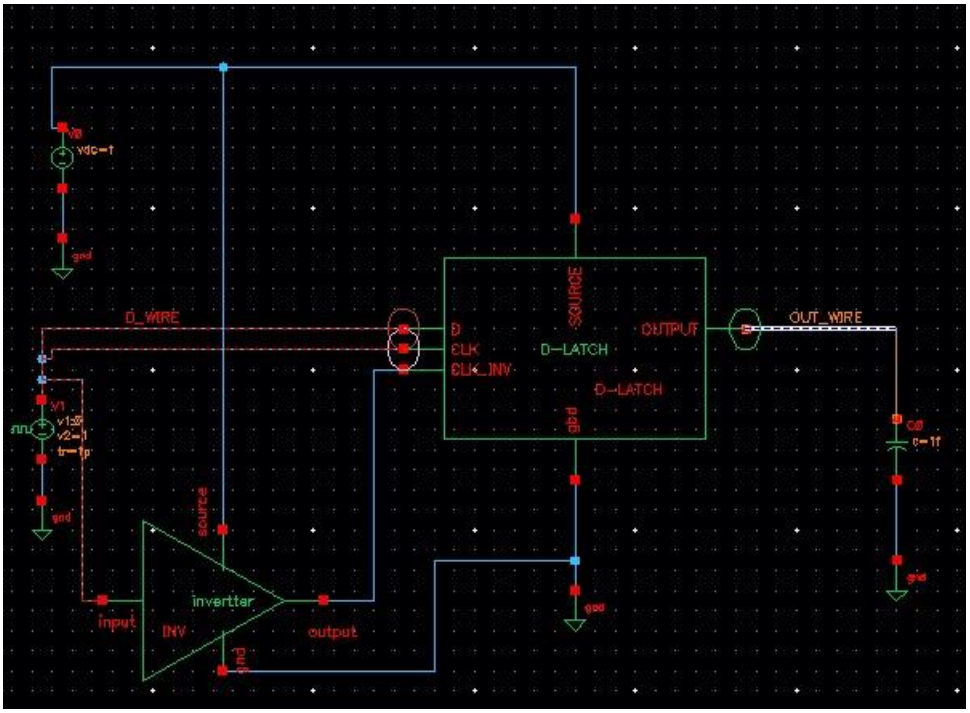


E	D	Q	$\overline{Q}$
0	0	latch	latch
0	1	latch	latch
1	0	0	1
1	1	1	0

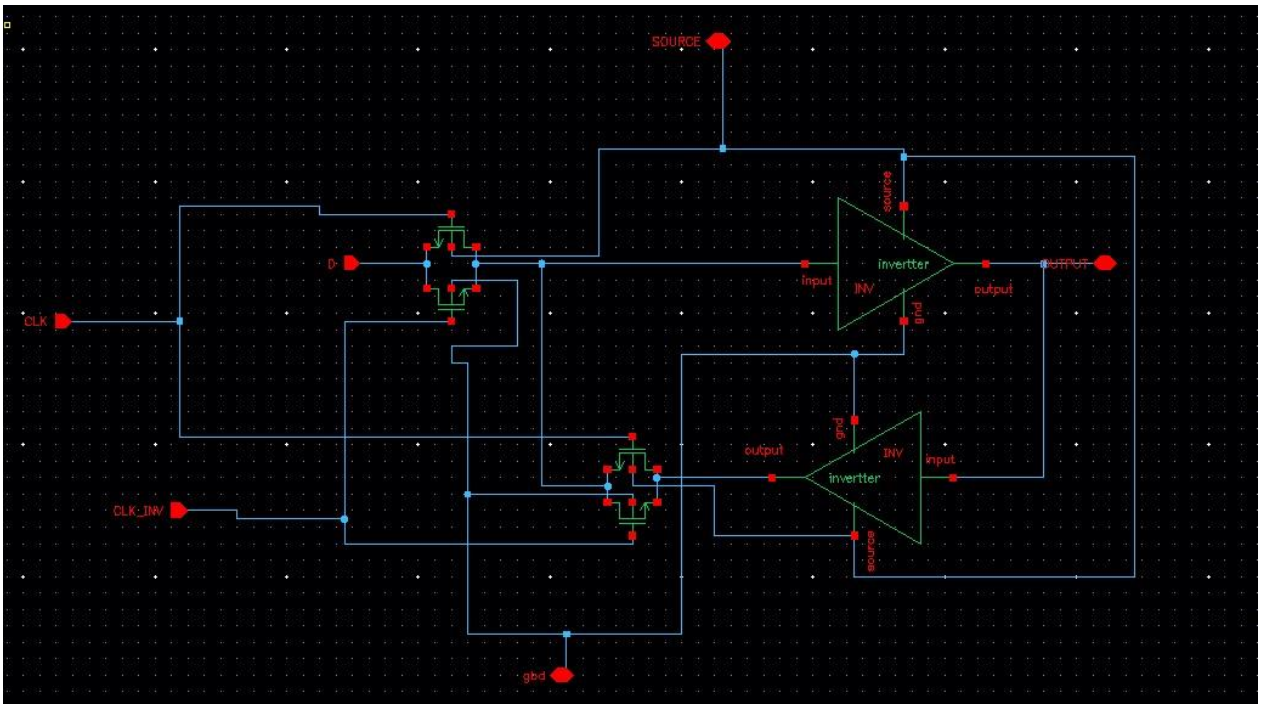
D-latch truth table



D-Latch simulation in trans 20n

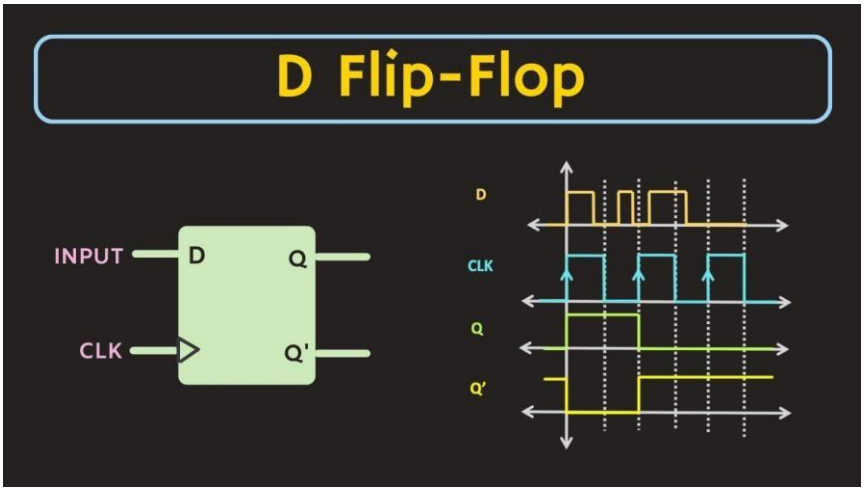


Testbench schematic



D-latch schematic

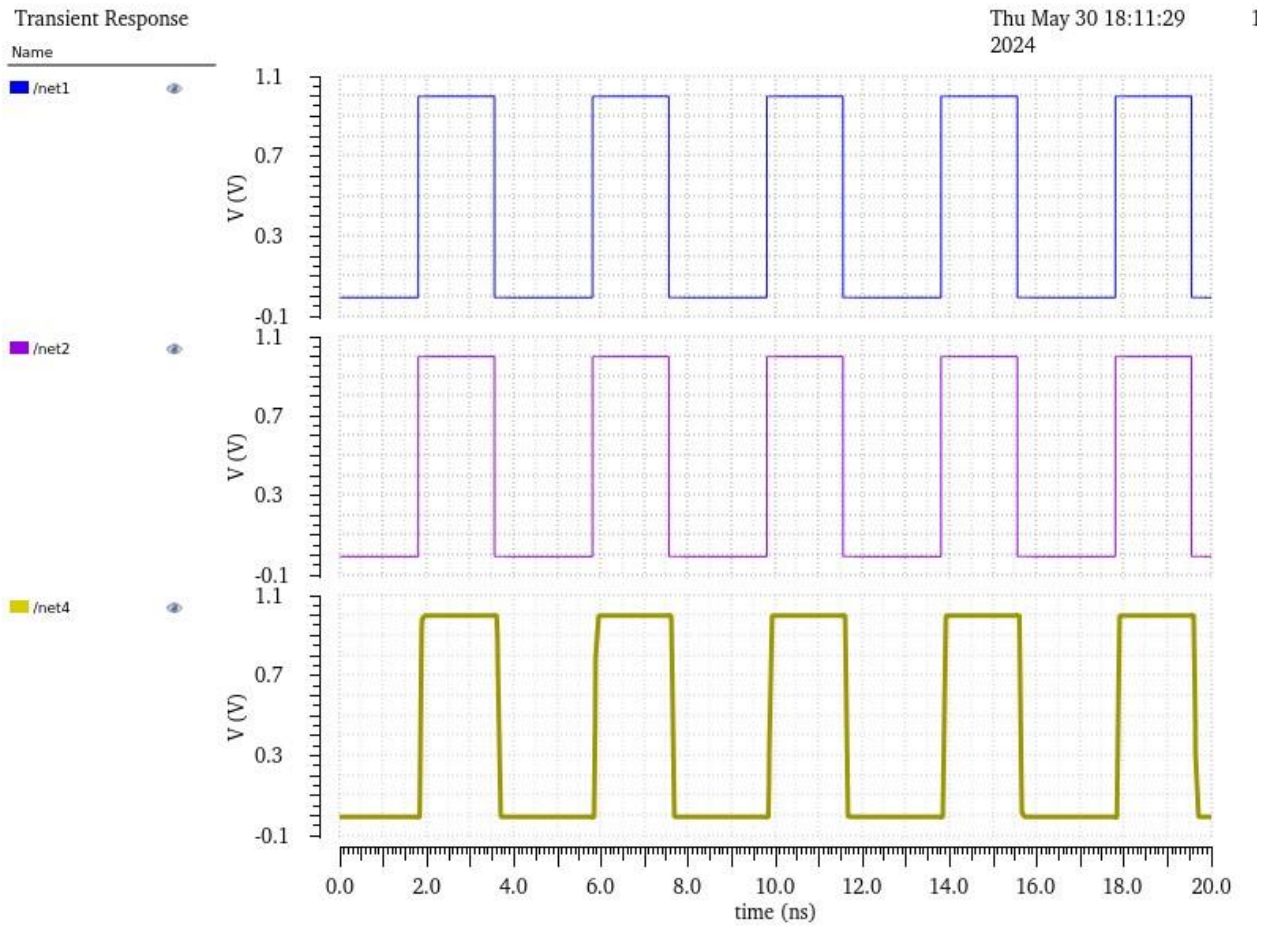
D – FLIP FLOP



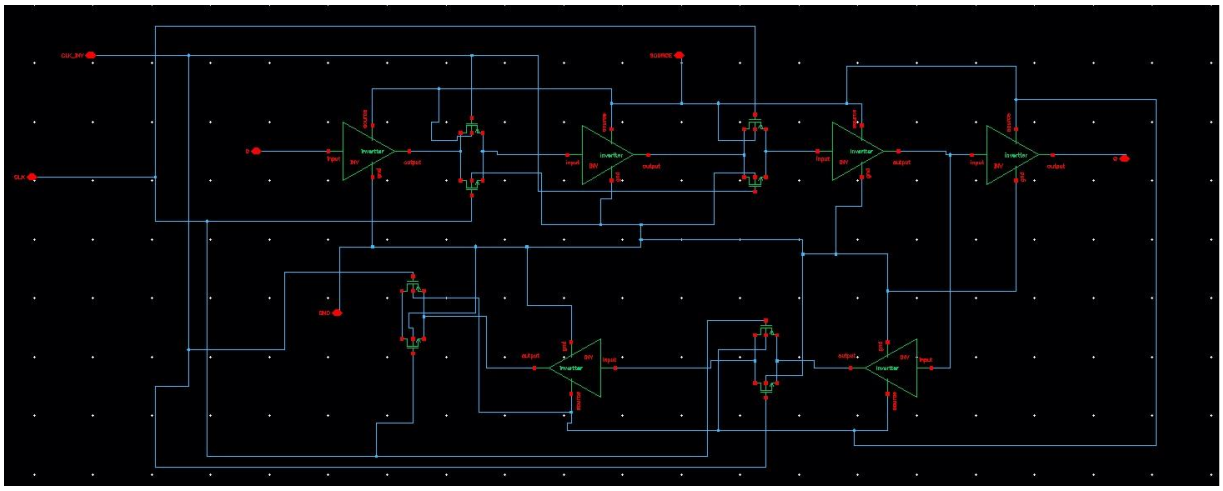
Truth table and symbol

$\overline{SET}$	$\overline{RESET}$	D	CK	Q	$\overline{Q}$
0	1	-	-	1	0
1	0	-	-	0	1
0	0	-	-	1	1
1	1	1	↓	1	0
1	1	0	↓	0	1

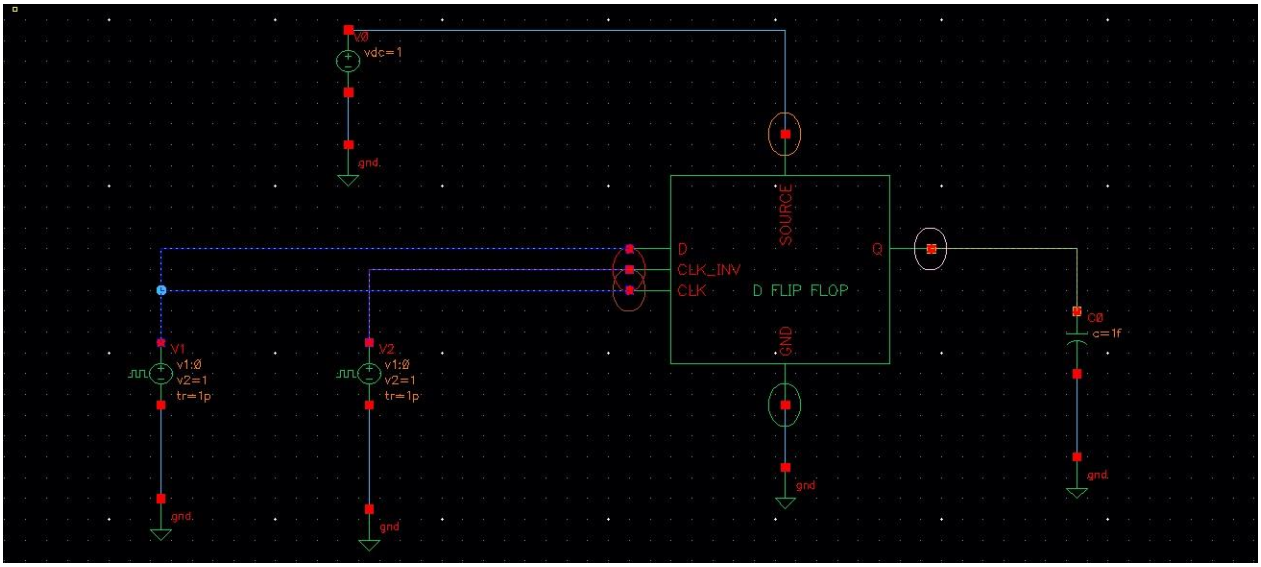
Transient response



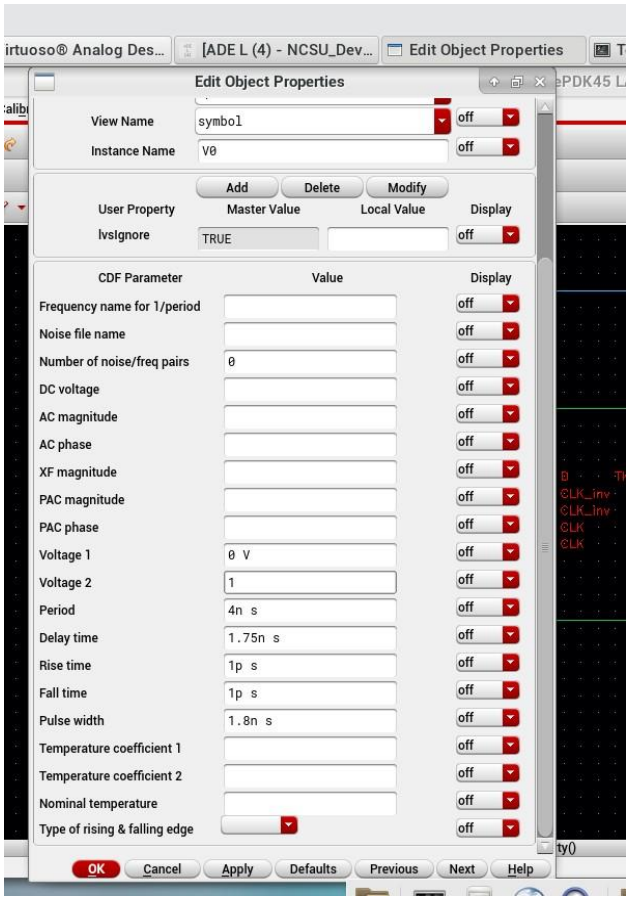
SCHEMATIC



TESTBENCH



Clock configuration



Parameters	Results
t_{pd}	0.0644(ns)
t_{cd}	0.029(ns)
t_{pcq}	0.0306(ns)
t_{ccq}	0.0219(ns)
t_{setup}	0.05312(ns)
t_{hold}	14.521pW