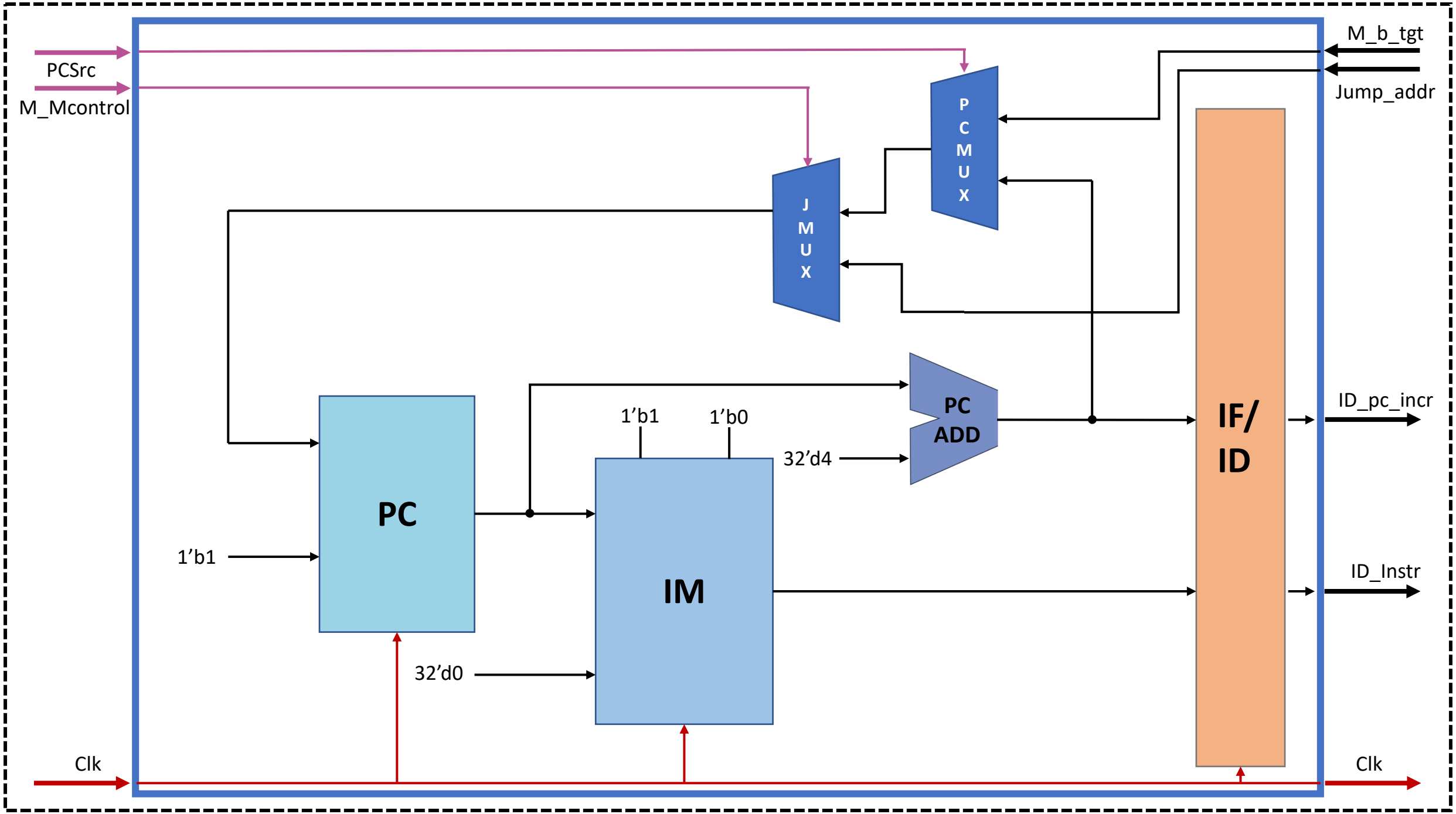
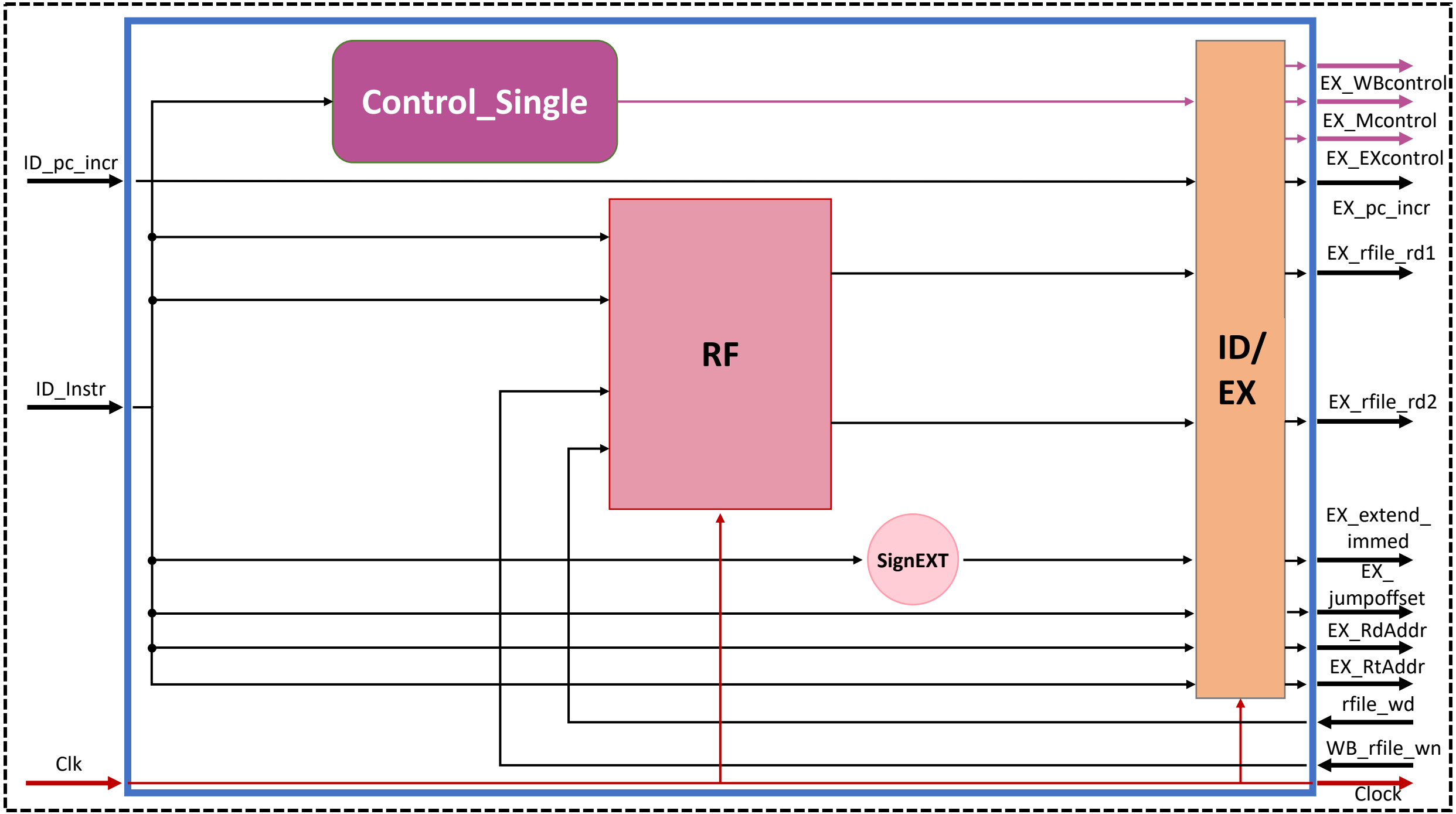
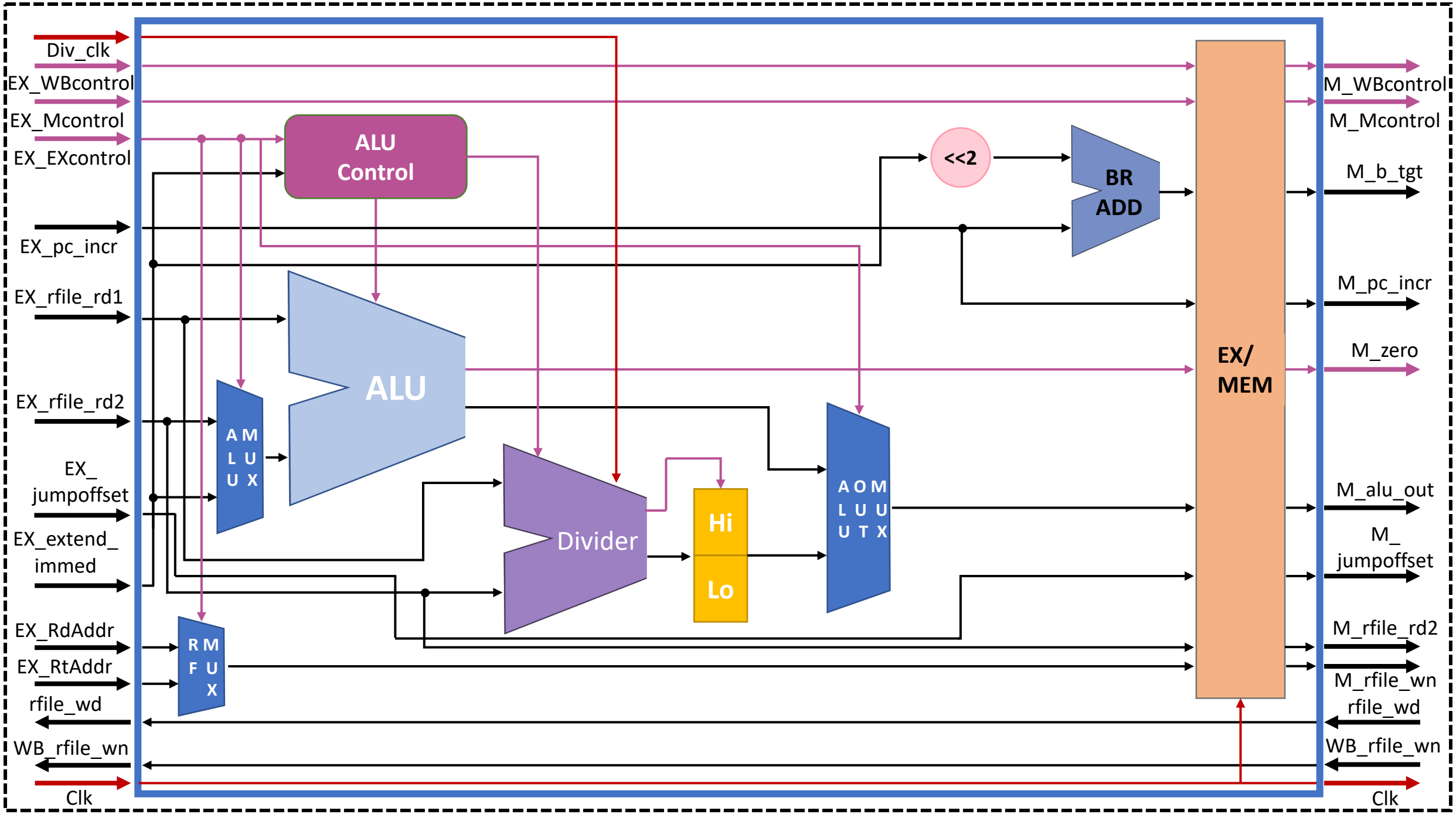
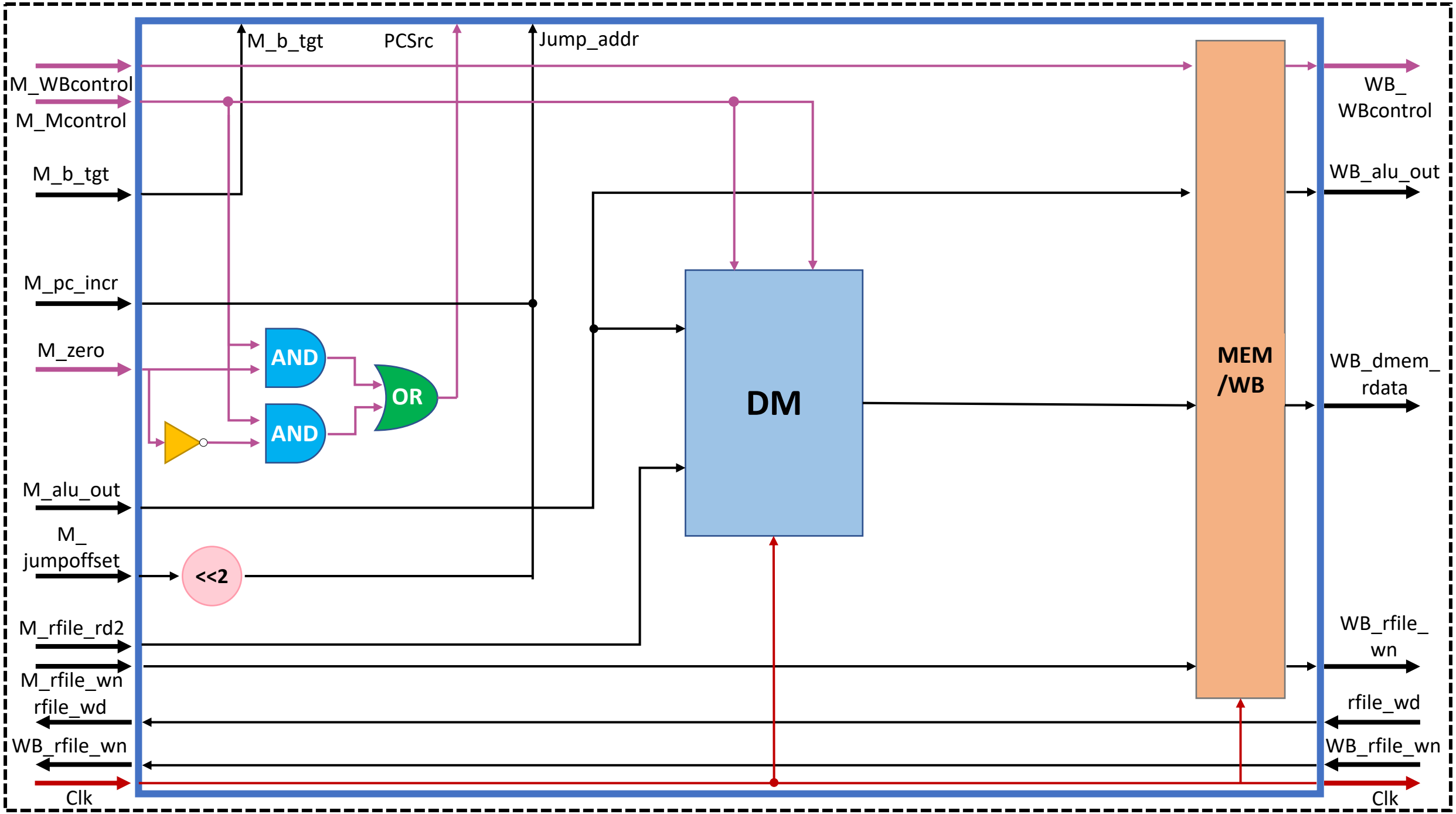
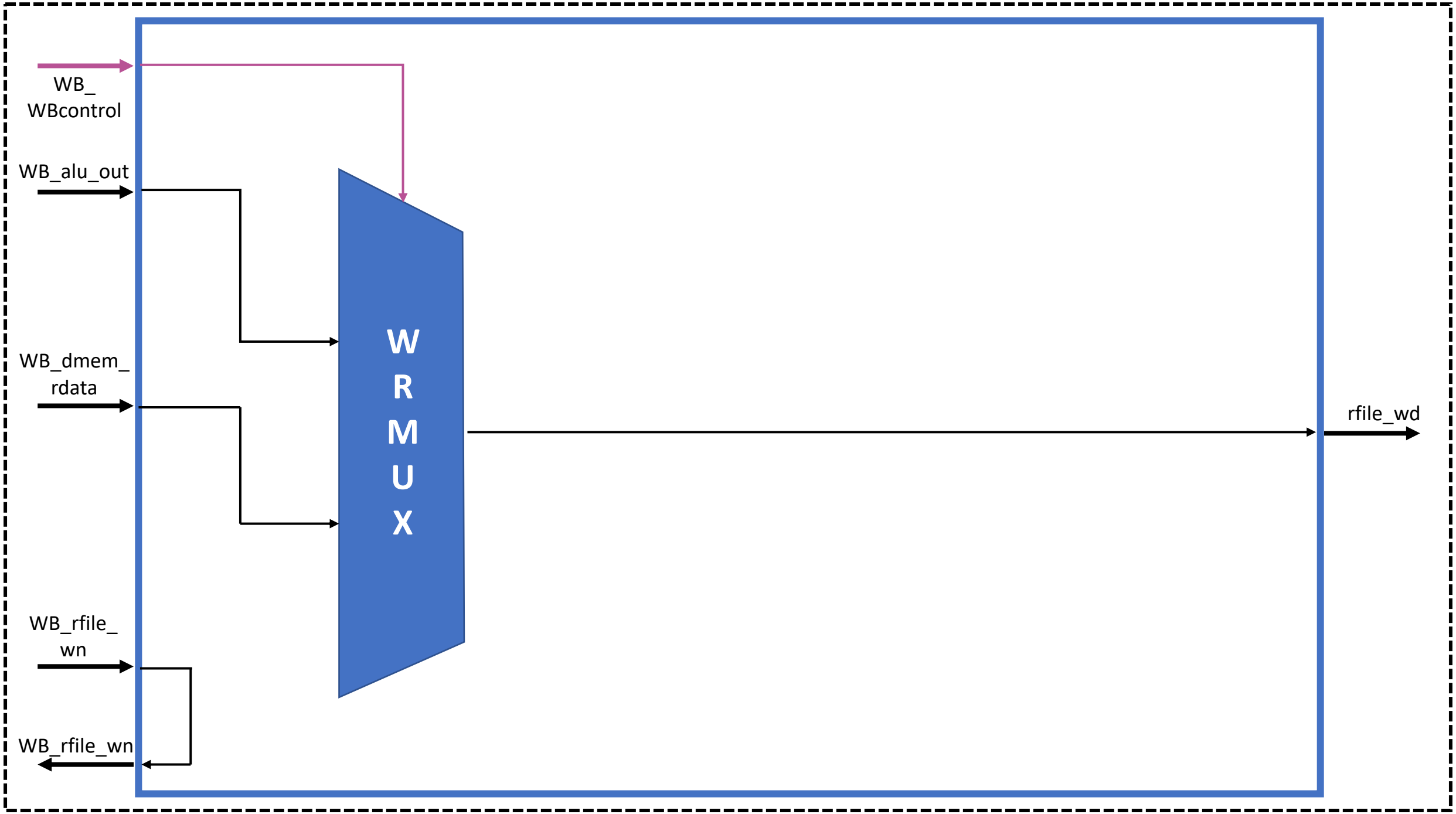

PCSrc
M_Mcontrol
M_b_tgt
Jump_addr
PCMUX
JMUX
PC
ADD
32'd4
1'b1
1'b0
PC
1'b1
IM
32'd0
IF/
ID
ID_pc_incr
ID_Instr
Clk
Clk

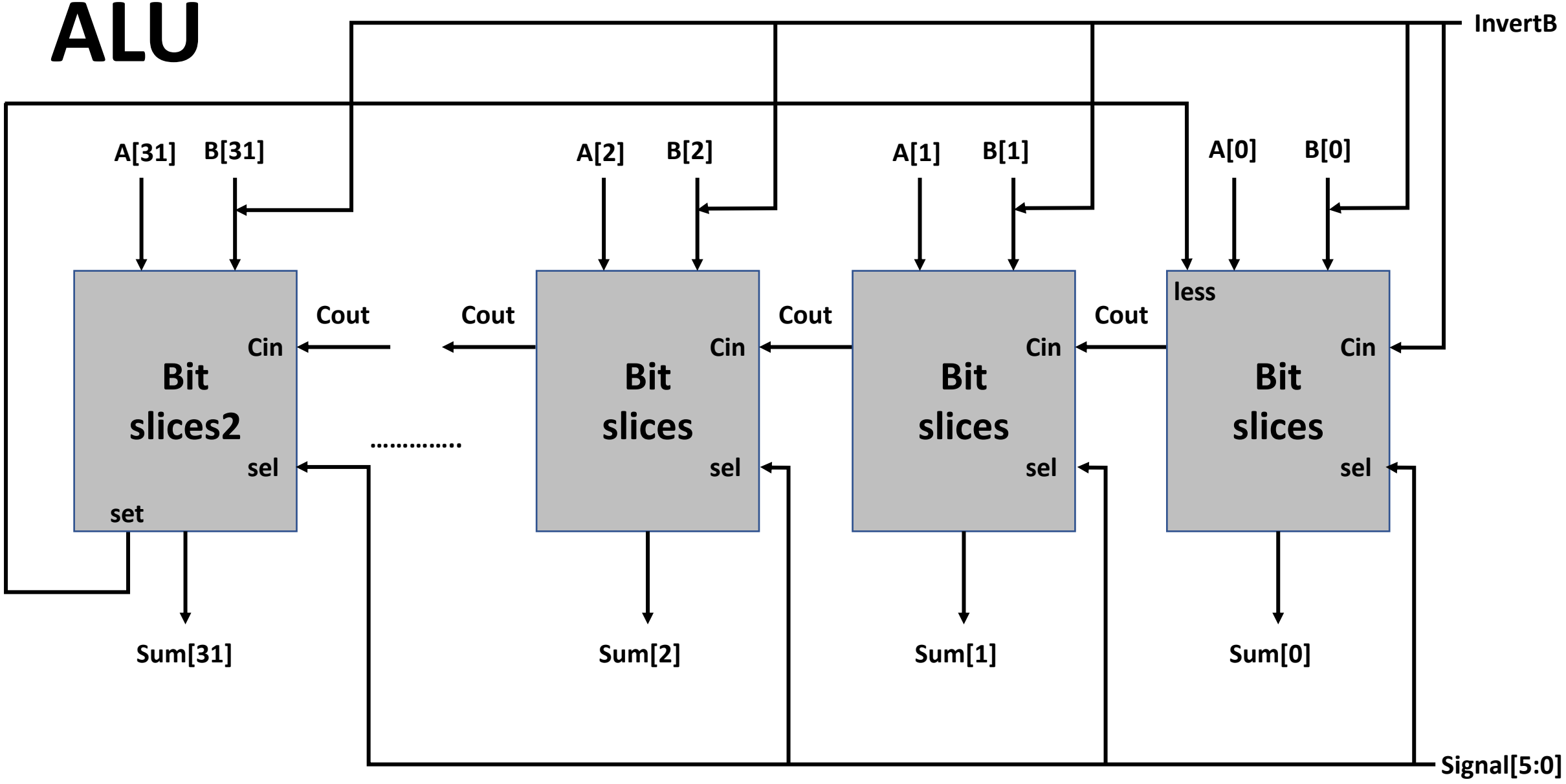

Control_Single
ID_pc_incr
ID_Instr
Clk
RF
SignEXT
ID/
EX
EX_WBcontrol
EX_Mcontrol
EX_EXcontrol
EX_pc_incr
EX_rfile_rd1
EX_rfile_rd2
EX_extend_
immed
EX_
jumpoffset
EX_RdAddr
EX_RtAddr
rfile_wd
WB_rfile_wn
Clock


Div_clk
EX_WBcontrol
EX_Mcontrol
EX_EXcontrol
EX_pc_incr
EX_rfile_rd1
EX_rfile_rd2
EX_ jumpoffset
EX_extend_ immed
EX_RdAddr
EX_RtAddr
rfile_wd
WB_rfile_wn
Clk
ALU Control
ALU
A M L U U X
Divider
Hi
Lo
<<2
BR ADD
A O M L U U U T X
R M F U X
EX/ MEM
M_WBcontrol
M_Mcontrol
M_b_tgt
M_pc_incr
M_zero
M_alu_out
M_ jumpoffset
M_rfile_rd2
M_rfile_wn
rfile_wd
WB_rfile_wn
Clk

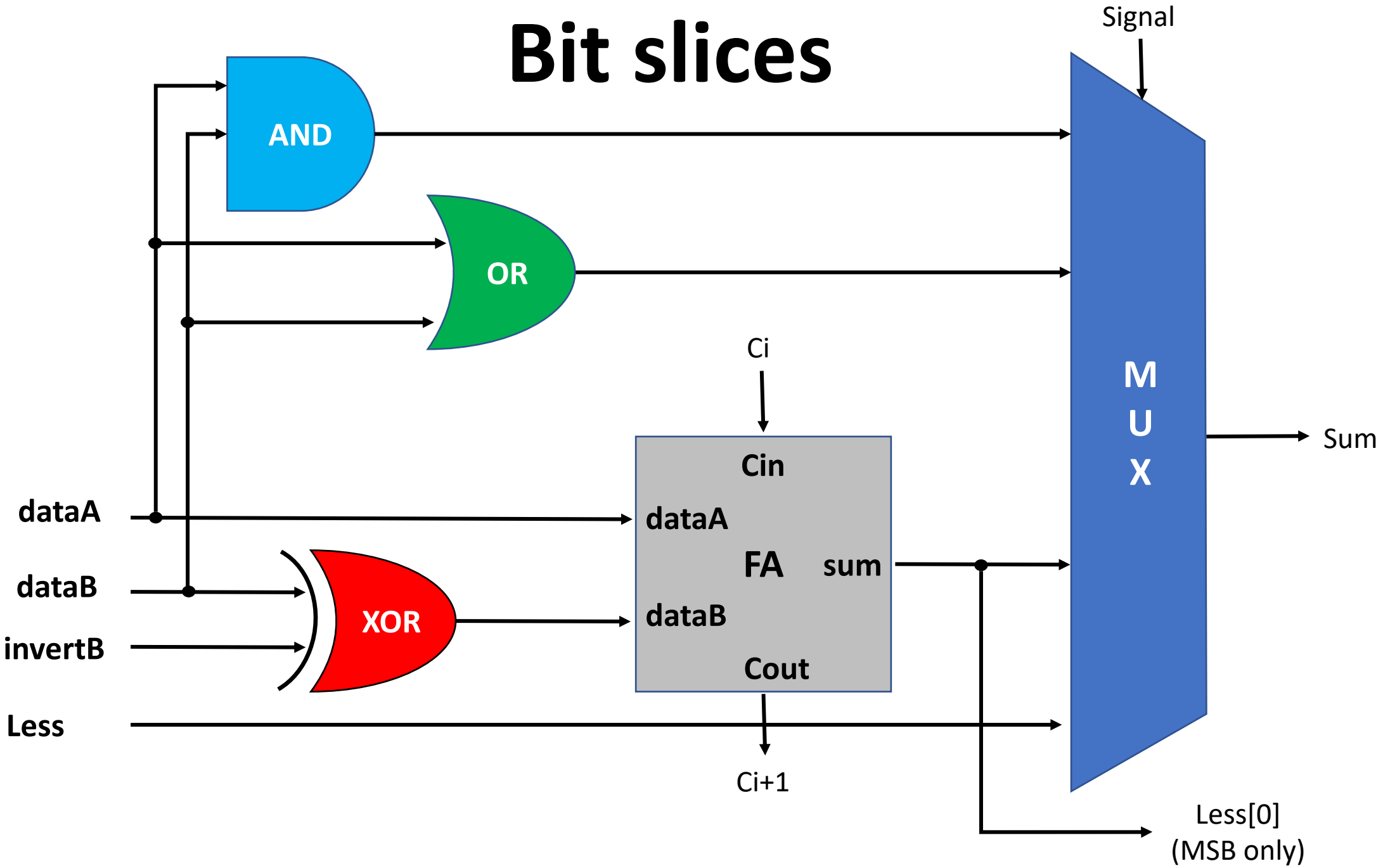

M_b_tgt
PCSrc
Jump_addr
M_WBcontrol
M_Mcontrol
M_b_tgt
M_pc_incr
M_zero
AND
AND
OR
M_alu_out
M_
jumpoffset
<<2
M_rfile_rd2
M_rfile_wn
rfile_wd
WB_rfile_wn
Clk
DM
MEM
/WB
WB_
WBcontrol
WB_alu_out
WB_dmem_
rdata
WB_rfile_
wn
rfile_wd
WB_rfile_wn
Clk

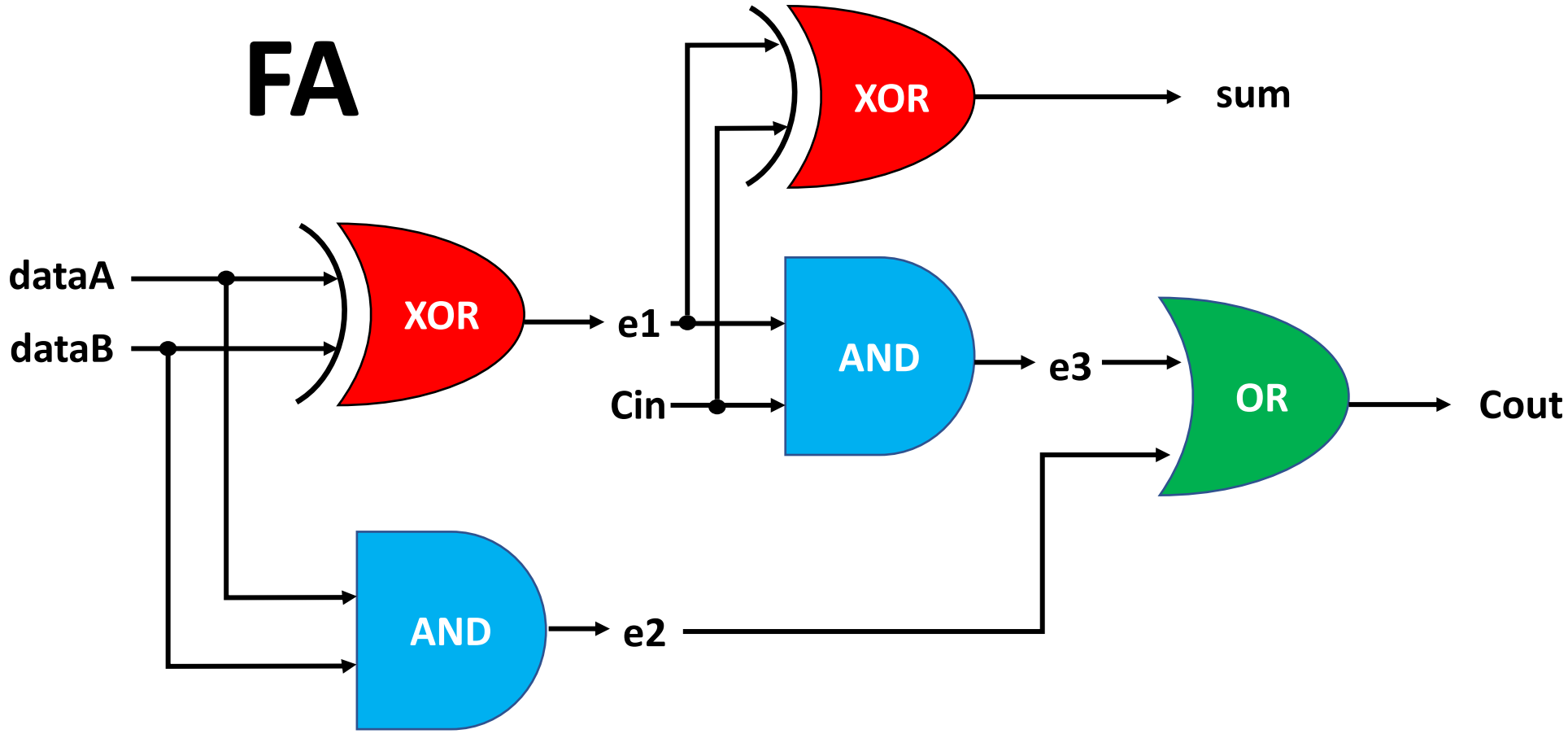

WB_
WBcontrol
WB_alu_out
WB_dmem_
rdata
WB_rfile_
wn
WB_rfile_wn
W
R
M
U
X
rfile_wd

ALU

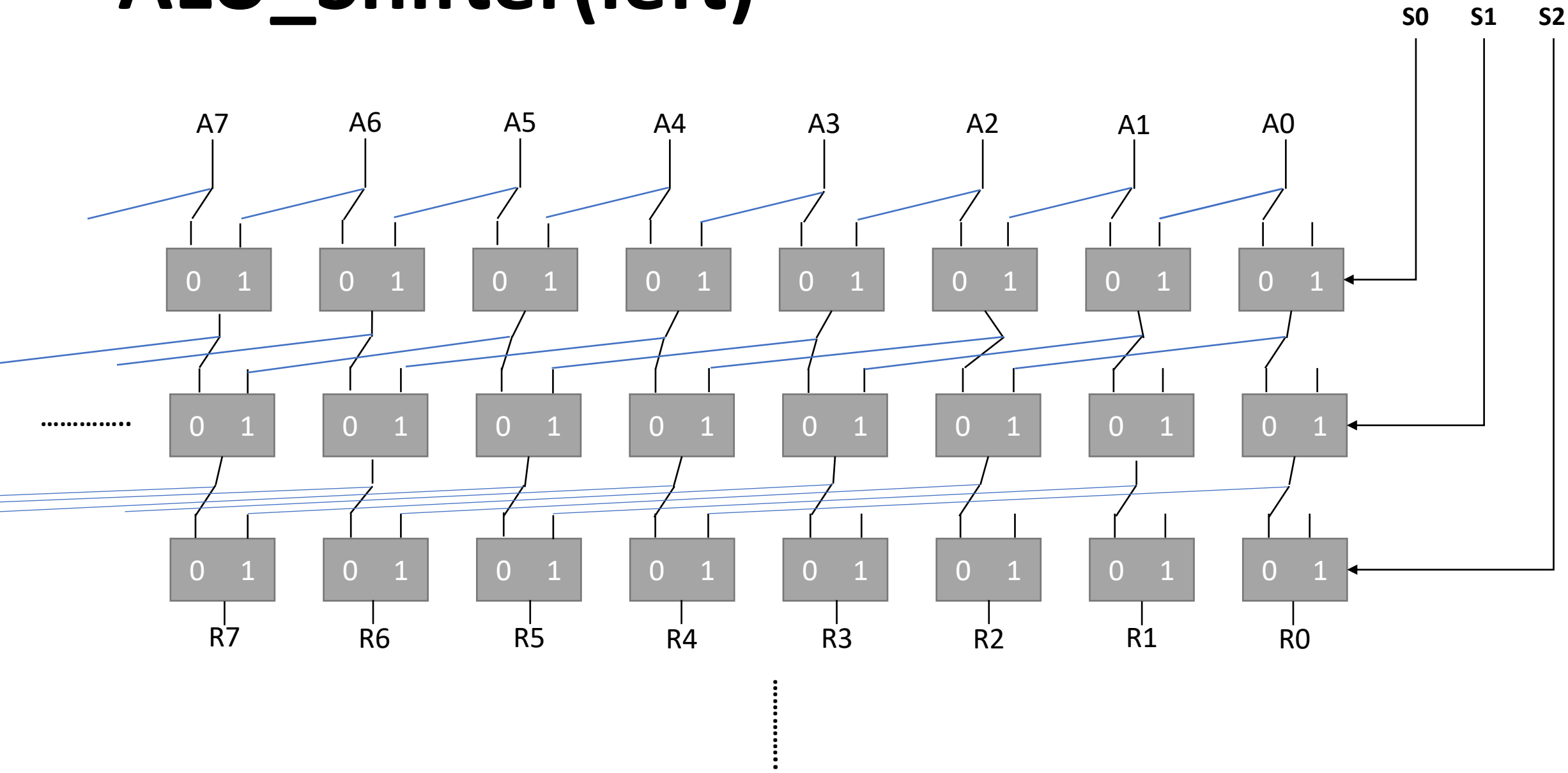

InvertB
A[31]
B[31]
A[2]
B[2]
A[1]
B[1]
A[0]
B[0]
Cout
Cout
Cout
Cout
Cin
Cin
Cin
Cin
less
Bit slices2
Bit slices
Bit slices
Bit slices
sel
sel
sel
sel
set
.....
Sum[31]
Sum[2]
Sum[1]
Sum[0]
Signal[5:0]

Bit slices

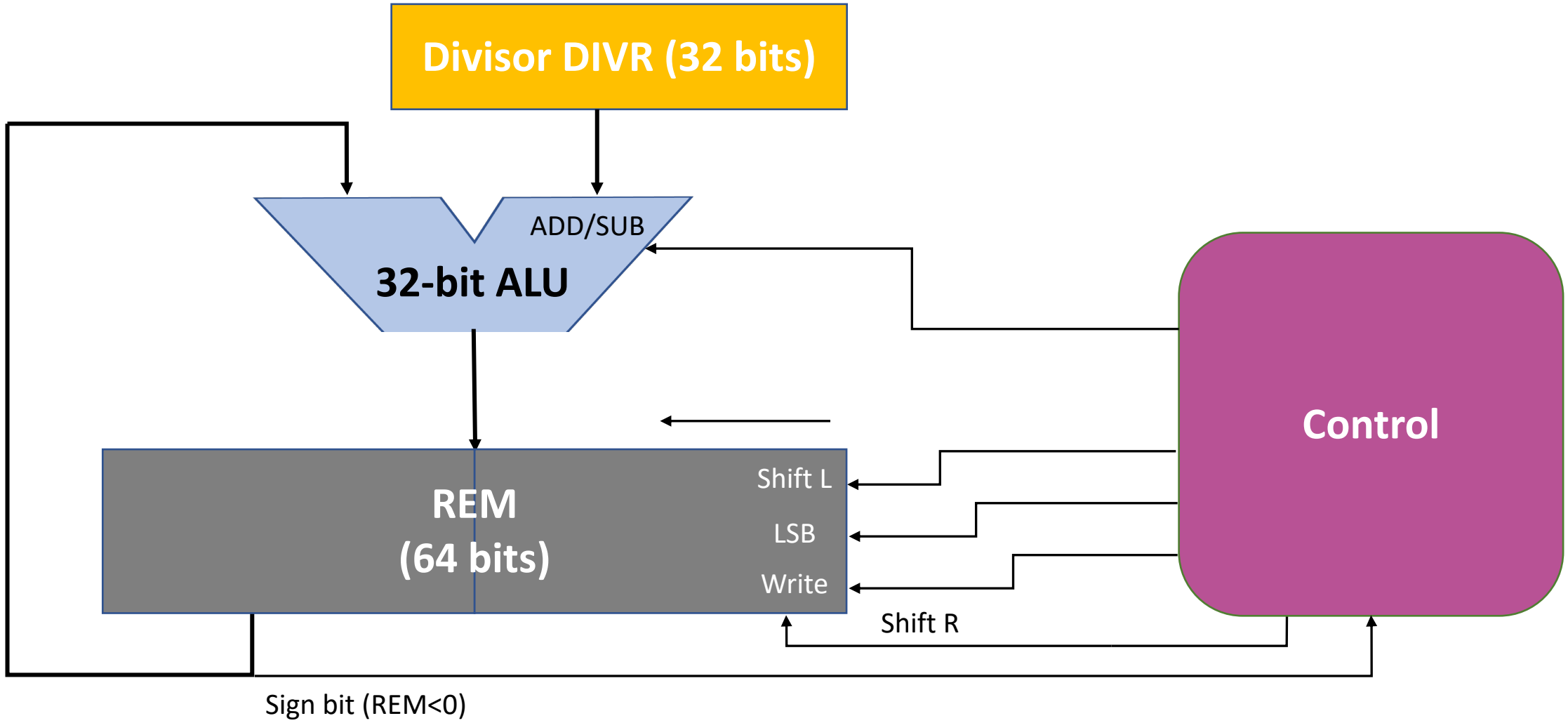

Signal
AND
OR
Ci
M
U
X
Sum
Cin
dataA
FA
sum
dataB
Cout
dataA
dataB
invertB
XOR
Less
Ci+1
Less[0]
(MSB only)


FA
XOR
sum
dataA
dataB
XOR
e1
Cin
AND
e3
OR
Cout
AND
e2

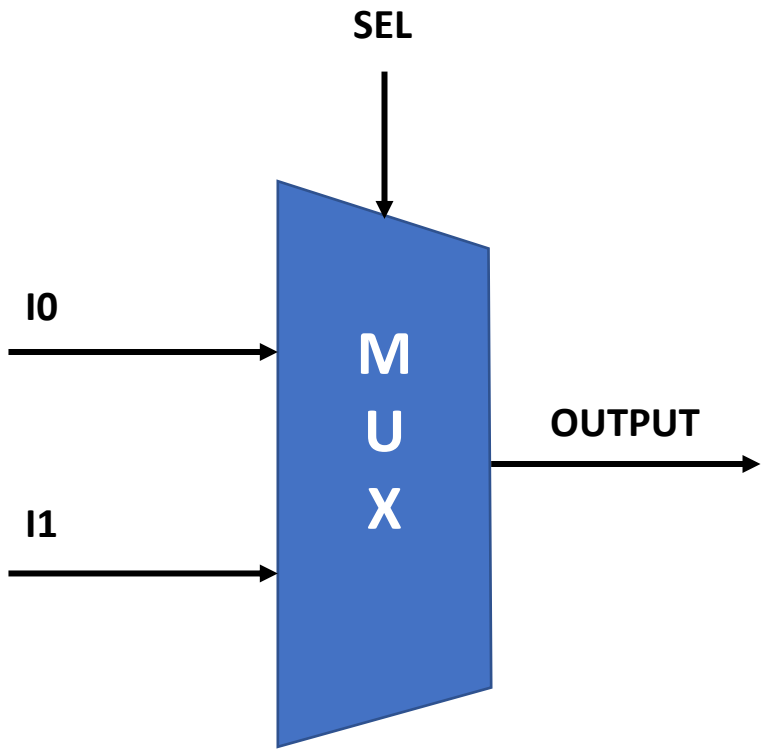
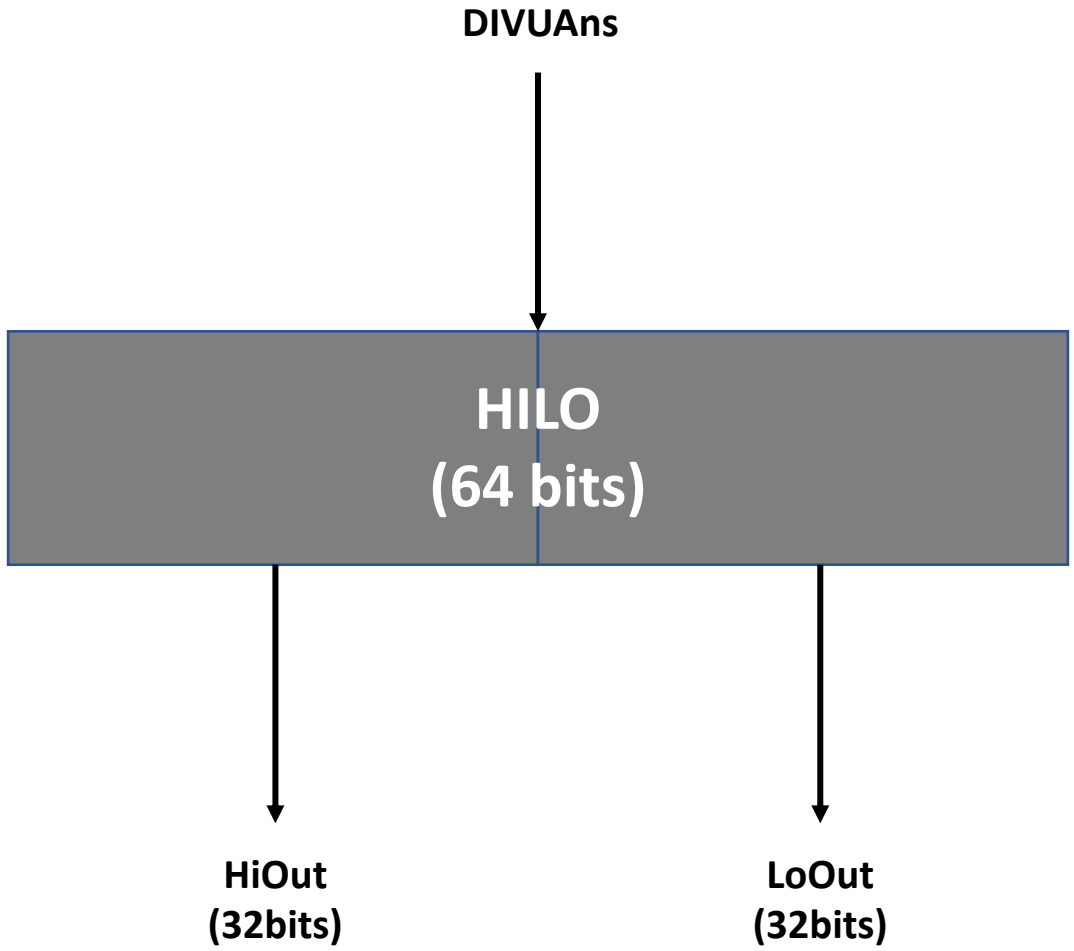
ALU_Shifter(left)



Divide Hardware – 3rd Version



MUX



HILO