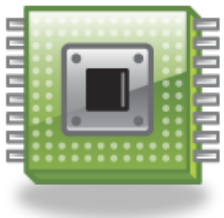

Homework #1-1 (Deadline : 2018/4/7 Sun. 9AM)

- Design a combinational 8-bit adder/subtractor by writing both (1) Verilog RTL and (2) gate-level codes. The basic I/O specification is described below. Please use this spec. to design your circuit. You are encouraged to enrich the functionality of your adder/subtractor design as much as you can. For example, you can add an output that indicates whether overflow occurs.
  - Two 8-bit binary inputs: A, B
  - One 1-bit control input for addition/subtraction: Add_ctrl (Add_ctrl=1 (0) for addition (subtraction))
  - One 8-bit sum output: SUM
  - One 1-bit carry-out output: C_out
- Please specify some reasonable delays in your components and generate some waveforms to verify your design.
- Also design a testbench to verify your designs. Must include $finish command in your testbench. Describe what test inputs you use in the testbench to verify your design.
- Describe the longest path in your design and accordingly calculate or estimate the maximum delay in your design