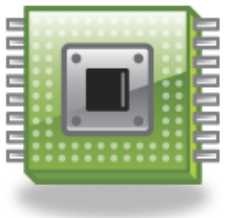
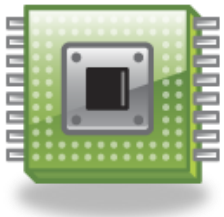


Homework #3
(Deadline : 2018/5/29 Tue. 23:59)

- Design an useful and practical traffic light controller by writing Verilog RTL codes. You are encouraged to add any special property to your design, but the controller must have at least 6 states.

- Use the *Synopsys Design Vision* EDA tool to synthesize your traffic light controller

- Also design a testbench to verify your designs.
  Must include $finish command in your testbench.



Homework #3 (Deadline : 2018/5/29 Tue. 23:59)

- Hand in a report that explains your design in detail. The report must contain at least
  - A general description of the design, with emphasis on the special properties of your design
  - I/O specifications
  - State transition diagram
  - Simulation results and explanations
  - Your synthesis procedure
  - The statistics of your designs including (1) gate count, (2) critical path delay, and (3) power consumption.
  - The simulation results of the synthesized design and their correctness explanation. Compare the post-synthesis results with those of your original (pre-synthesis) designs. Describe the delay effect.
  - Discussions
- Upload your report and designs including the pre-synthesized and post-synthesized circuits, testbench files and .sdf timing files to the course FTP.