# Bonus Homework
# (Deadline : 2018/7/2(一) 9AM前)

- 用Verilog實現 16-bit ripple carry adder, 16-bit block carry lookahead adder, 16-bit carry-skip adder、16-bit carry-select adder
- 完成邏輯合成並驗證成功
- 分析、比較與討論這些加法器之面積、delay與功率消耗
- Hand in your report and designs including the pre-synthesized and post-synthesized circuits, testbench files and .sdf timing files.