實用數位系統設計

Use the Synopsys Design Vision EDA tool to synthesize my circuits in HW1-1_gatelevel

I. my synthesis procedure :

step1.check setup file:確定要執行設計檔的資料夾中

有 .synopsys_dc.setup 沒有則前往課程的FTP複製並改檔名

step2.invoke design compiler:在putty指令輸入 dv

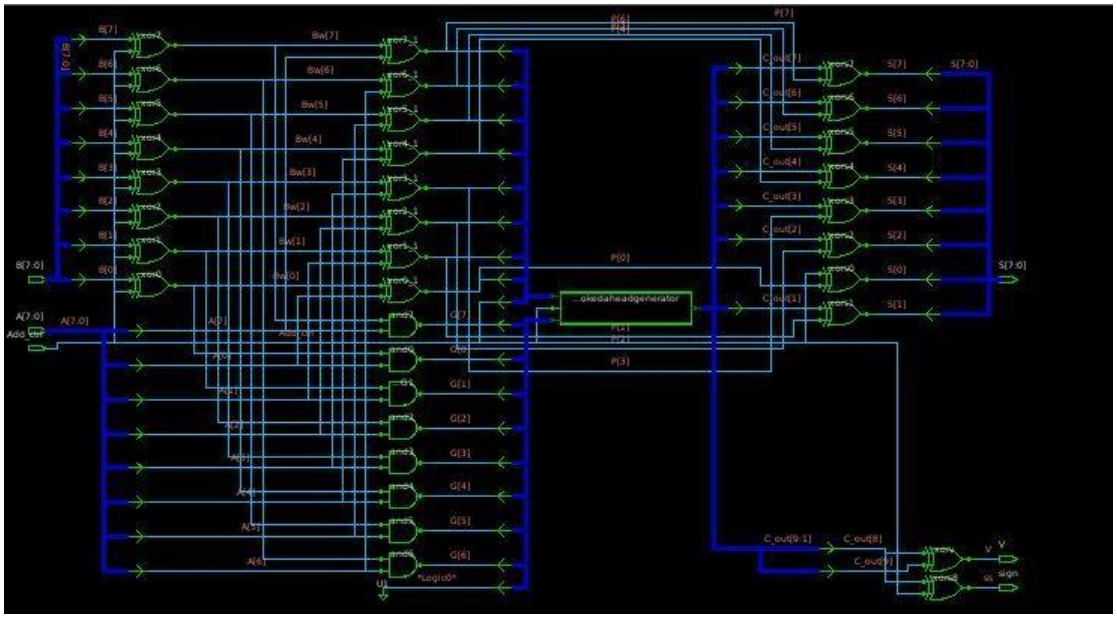
step3.:check if library is correctly loaded 結果:有

step4.read file :選擇想要合成的檔案並確認沒有errors及warning

結果：無errors及warning

Step5.symbol view

Step6.schematic view



Step7. Prevent Possible Assign Statement Problem:

在command line 鍵入

set_fix_multiple_port_nets -all -buffer_constants

step9:compile design:結果 Optimization Complete

step10.Area report:

```
Noncombinational area:        0.000000
Net Interconnect area:       undefined

Total cell area:           443.021395
Total area:                  undefined

***** End Of Report *****
```

Step11Timing report:

MAX

```
  U38/Y (XOR2X1)                                          0.13       3.35 f
  V (out)                                                 0.00       3.35 f
  data arrival time                                                  3.35
  ---------------------------------------------------------------------------
  (Path is unconstrained)


***** End Of Report *****
```

MIN

```
  input external delay                    0.00       0.00 r
  Add_ctrl (in)                           0.00       0.00 r
  U46/Y (XOR2X1)                          0.02       0.02 f
  S[0] (out)                              0.00       0.02 f
  data arrival time                                  0.02
  ----------------------------------------------------------
  (Path is unconstrained)
  Cell Internal Power  =   60.7120 uW   (79%)
  Net Switching Power  =   16.2616 uW   (21%)
                           ---------
Total Dynamic Power    =   76.9735 uW  (100%)

Cell Leakage Power     = 600.3915 nW


***** End Of Report *****
```

Step13.

Save Design - Circuit and Timing Files:

Step14. Rerun Verilog Simulation:修改testbench.v並跑波型觀察

II. The statistics of your designs including (1) gate count, (2) critical path delay, and (3) power consumption.

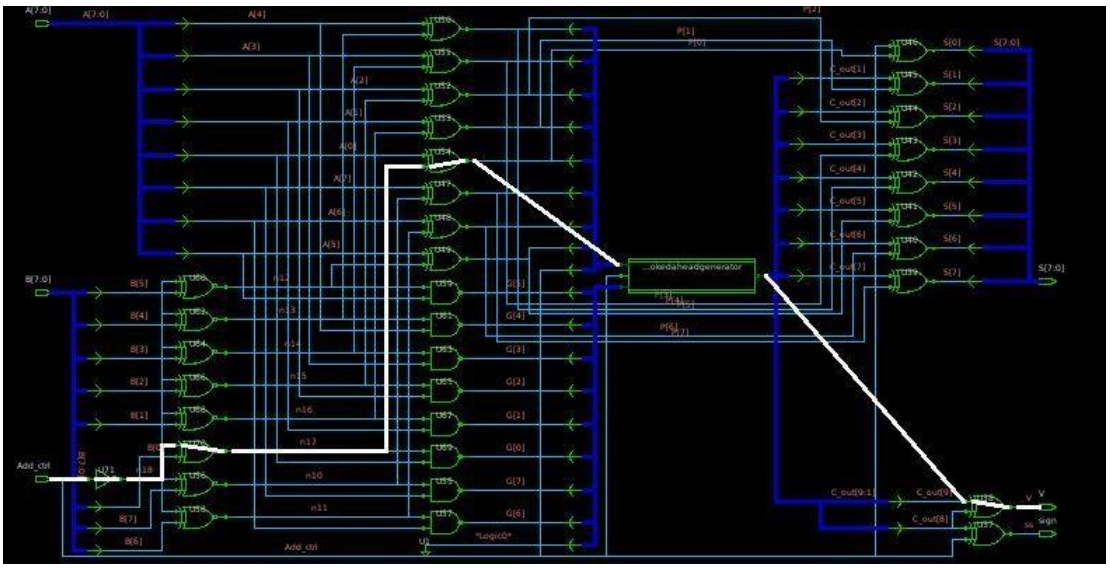
(1) gate count

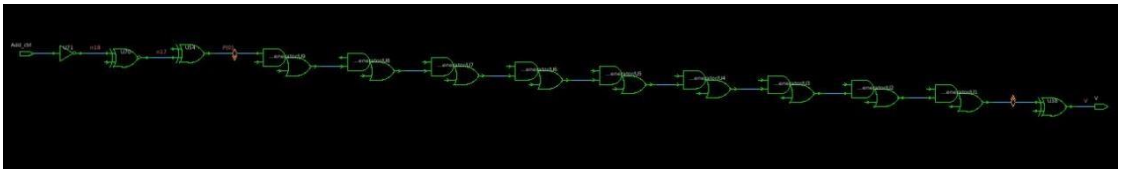
由AREA report中的total cell area 443，除以NAND2 gate area約5um^2

Gate count=443/5

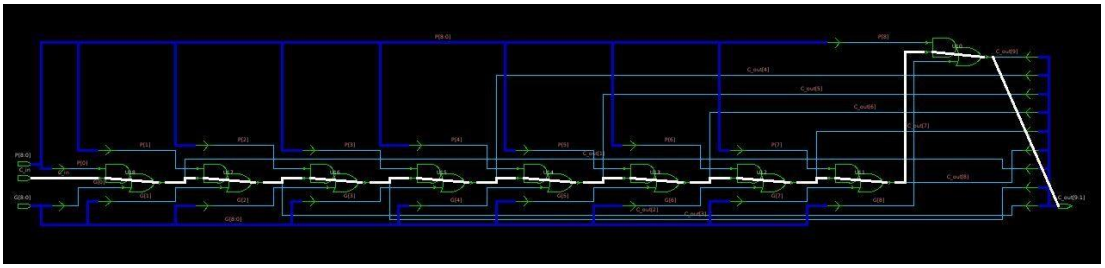
(2)critical path delay

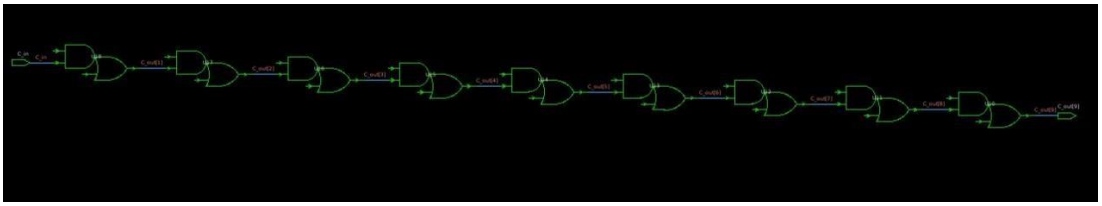
adder.v





Adder_syn.v





(3)power consumption

由power report 知

```
  Cell Internal Power  =   60.7120 uW    (79%)
  Net Switching Power  =   16.2616 uW    (21%)
                           ---------
Total Dynamic Power    =   76.9735 uW   (100%)

Cell Leakage Power     =  600.3915 nW


***** End Of Report *****
```

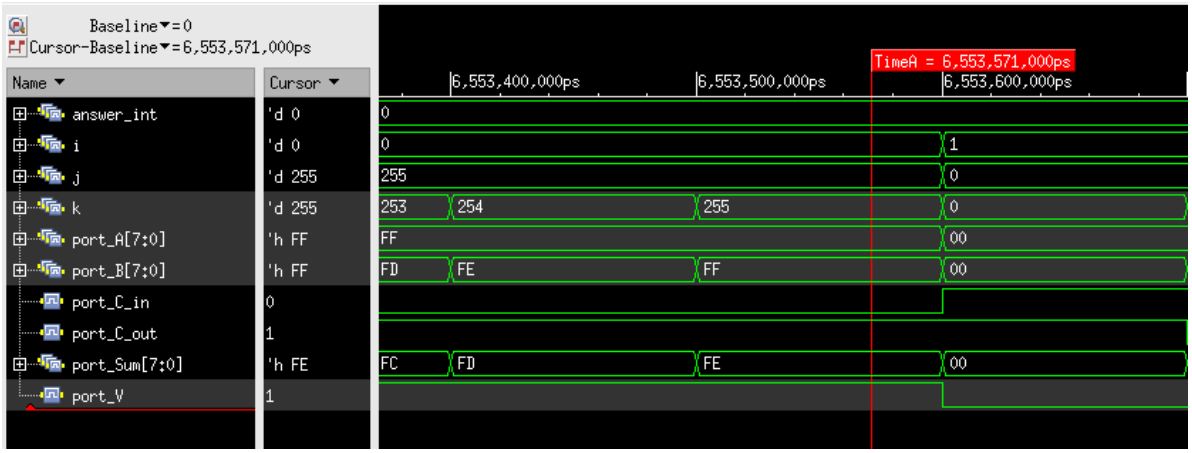
III. 結果分析：

加減法器波型(A 為被加數，B 為加數，C_in 為判斷加法減法)

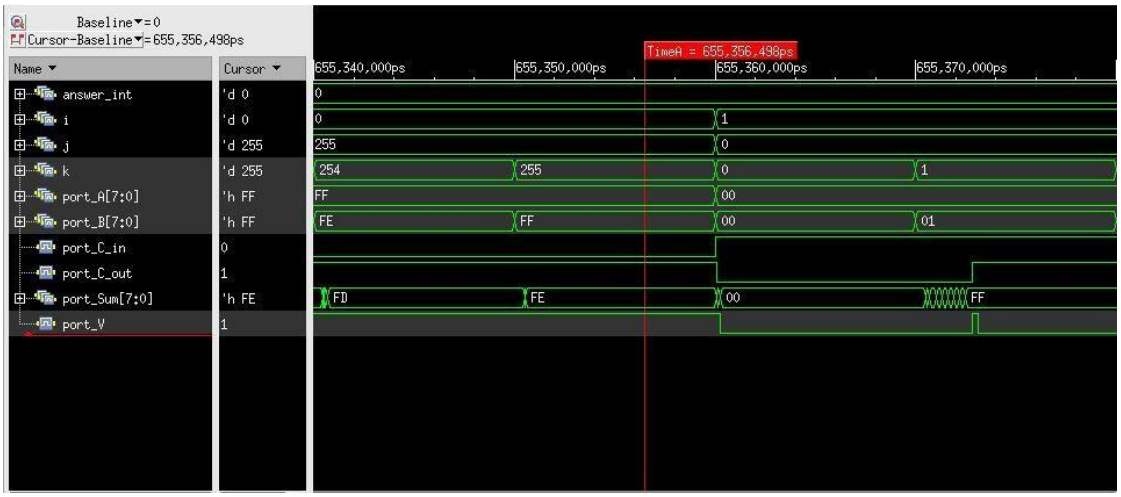
因為 C_in=0 所以加法，255+255 為下圖 v=1 所以表示此加法運算會進位到 9bits

(加法溢位)

合成前:



合成後:
由下圖可知，訊號數值會有一段時間為不穩定的數值，之後才穩定到正確的數值

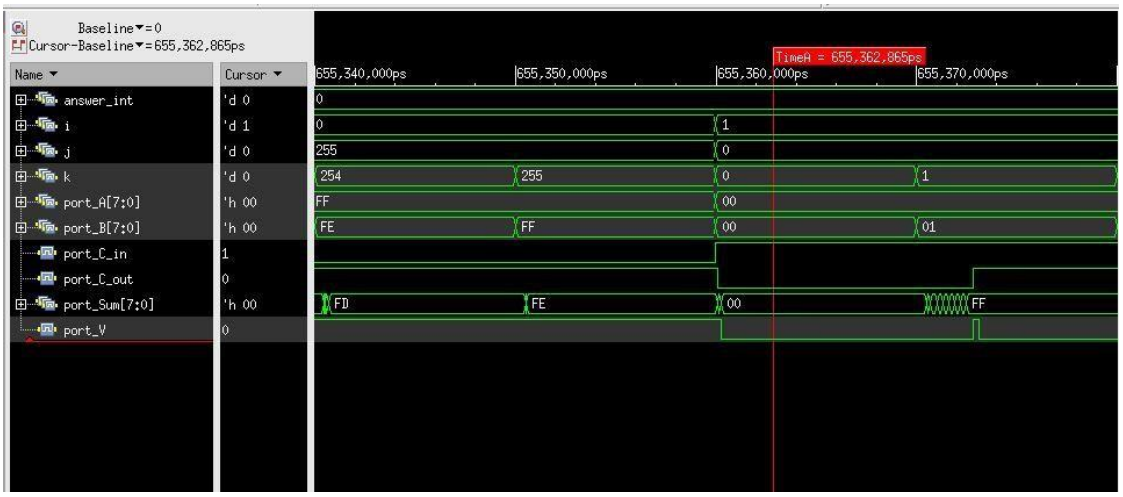


減法 當 A+(-B)
因為C_in=1，所以為減法器，0+(-0)為下圖，第九 bit 為符號數，將結果減1在01 互換回去加負號即為答案負的 0

0 0000 0000
\+ 0 0000 0000
---
0 0000 0000

合成後

由下圖可知，訊號數值會有一段時間為不穩定的數值，之後才穩定到正確的數值，其中在0-1時候delay較長



減法 當 A+(-B)

因為 C_in=1，所以為減法器，1+(-255)為下圖，第九 bit 為符號數，將結果減 1 在01 互換回去加負號即為答案 負的 254

0 0000 0001

\+ 1 0000 0001

---

1 0000 0010

合成前

合成後

由下圖可知，訊號數值會有一段時間為不穩定的數值，之後才穩定到正確的數值，其中訊號數值delay時間不一

減法 當 A+(-B)

因為 C_in=1，所以為減法器，14+(-1)為下圖，第九 bit 為符號數，忽略掉第 10bit 結果為13

11 1111 111

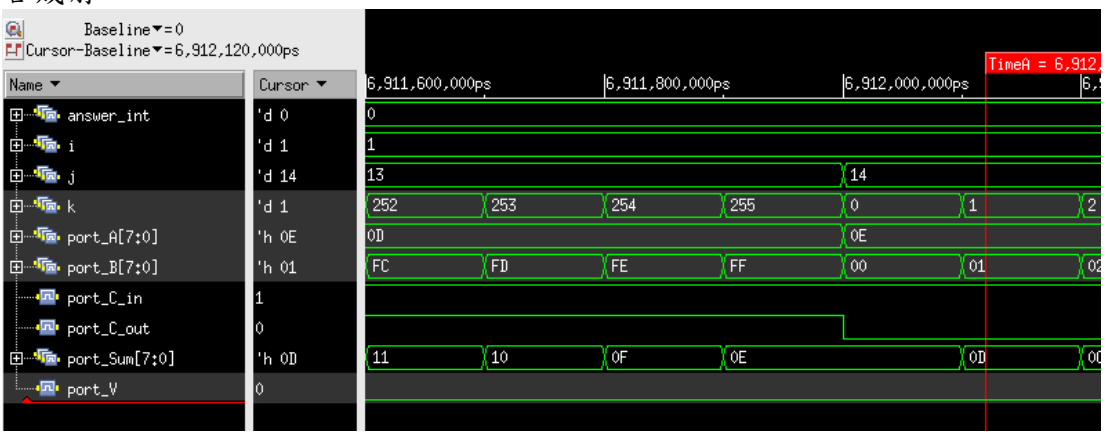
0 0000 1110

\+ 1 1111 1111

---

10 00001101

合成前



合成後
由下圖可知，訊號數值會有一段時間為不穩定的數值，之後才穩定到正確的數值，其中訊號數值delay時間不一

Use the Synopsys Design Vision EDA tool to synthesize my circuits in HW1-1_RTL

1. my synthesis procedure :

step1.check setup file:確定要執行設計檔的資料夾中

有 .synopsys_dc.setup 沒有則前往課程的FTP複製並改檔名

step2.invoke design compiler:在putty指令輸入 dv

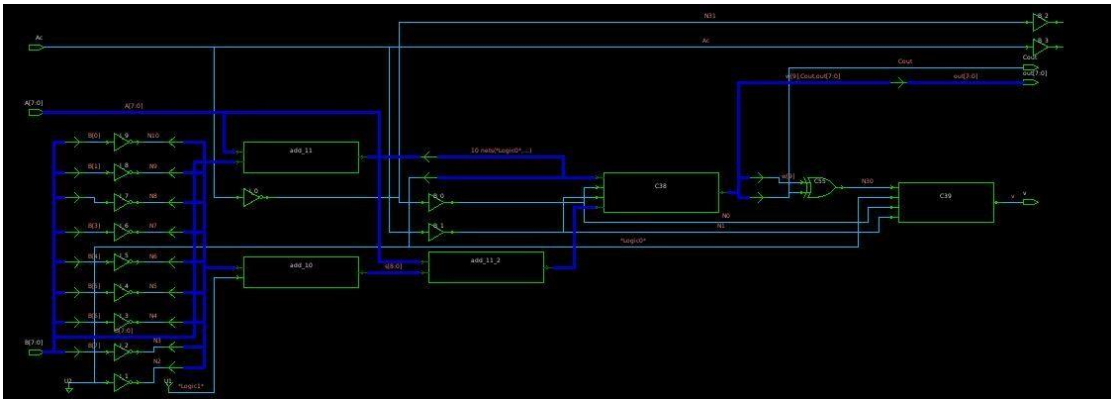
step3.:check if library is correctly loaded 結果:有

step4.read file :選擇想要合成的檔案並確認沒有errors及warning

結果：無errors及warning

Step5.symbol view

Step6.schematic view



Step7. Prevent Possible Assign Statement Problem:

在command line 鍵入

set_fix_multiple_port_nets -all -buffer_constants

step9:compile design:結果 Optimization Complete

step10.Area report:

```
Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /mnt2/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                27
Number of nets:                 55
Number of cells:                20
Number of references:            6

Combinational area:        560.142010
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:           560.142010
Total area:                 undefined

***** End Of Report *****
```

Step11Timing report:
MAX

Point	Incr	Path
input external delay	0.00	0.00 r
B[1] (in)	0.00	0.00 r
U32/Y (CLKINVX1)	0.03	0.03 f
add_10/A[1] (Add_DW01_inc_0)	0.00	0.03 f
add_10/U1_1_1/S (ADDHXL)	0.22	0.25 f
add_10/SUM[1] (Add_DW01_inc_0)	0.00	0.25 f
U41/Y (CLKMX2X2)	0.18	0.43 f
r311/B[1] (Add_DW01_add_0)	0.00	0.43 f
r311/U1_1/CO (ADDFXL)	0.61	1.04 f
r311/U1_2/CO (ADDFXL)	0.38	1.41 f
r311/U1_3/CO (ADDFXL)	0.38	1.79 f
r311/U1_4/CO (ADDFXL)	0.38	2.16 f
r311/U1_5/CO (ADDFXL)	0.38	2.54 f
r311/U1_6/CO (ADDFXL)	0.38	2.92 f
r311/U1_7/CO (ADDFXL)	0.37	3.29 f
r311/U2/Y (XOR2X1)	0.16	3.45 f
r311/SUM[8] (Add_DW01_add_0)	0.00	3.45 f
U25/Y (NOR2BX1)	0.16	3.61 f
v (out)	0.00	3.61 f
data arrival time		3.61

(Path is unconstrained)

MIN

Startpoint: Ac (input port)
Endpoint: v (output port)
Path Group: (none)
Path Type: min

Point	Incr	Path
input external delay	0.00	0.00 r
Ac (in)	0.00	0.00 r
U25/Y (NOR2BX1)	0.02	0.02 f
v (out)	0.00	0.02 f
data arrival time		0.02

(Path is unconstrained)

Step12.power report:

```
Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  62.3304 uW   (87%)
  Net Switching Power  =   9.5161 uW   (13%)
                         ---------
Total Dynamic Power    =  71.8464 uW  (100%)

Cell Leakage Power     = 630.9841 nW


***** End Of Report *****
```

Step13.

Save Design - Circuit and Timing Files:

Step14. Rerun Verilog Simulation:修改testbench.v並跑波型觀察

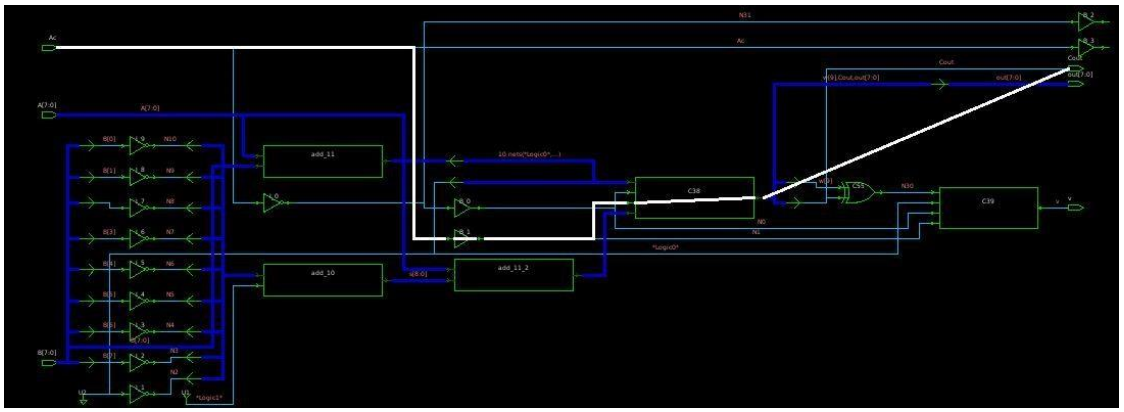
2. The statistics of your designs including (1) gate count, (2) critical path delay, and (3) power consumption.

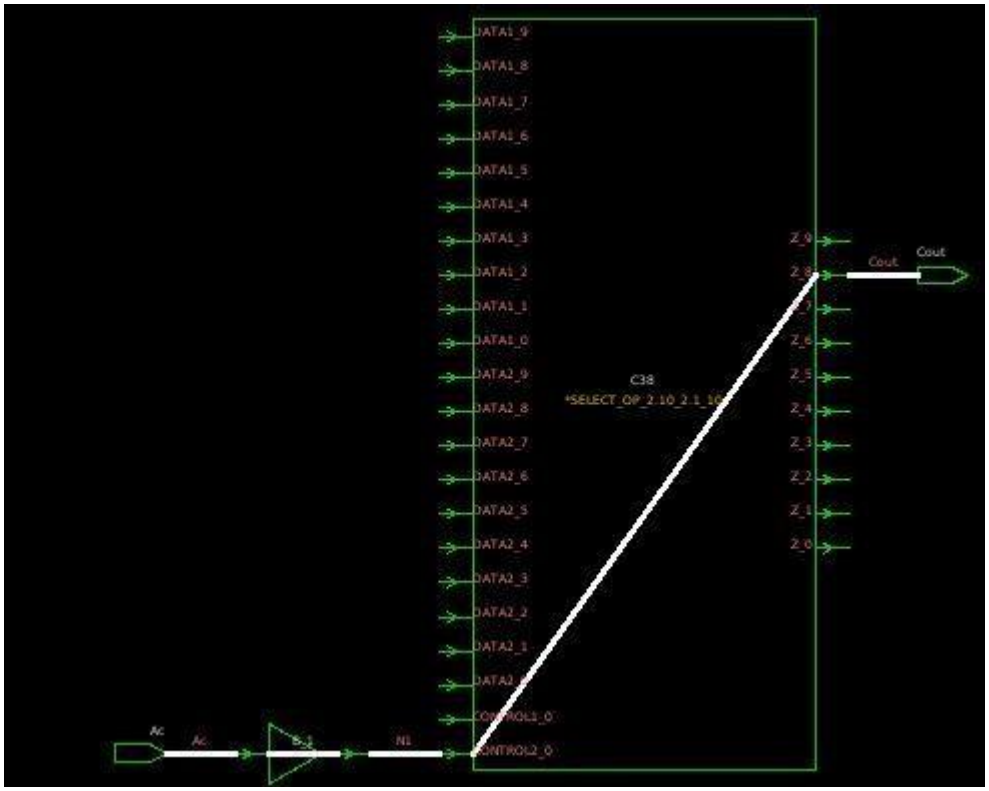
   (1) gate count

   由AREA report中的total cell area 560，除以NAND2 gate area約5um^2

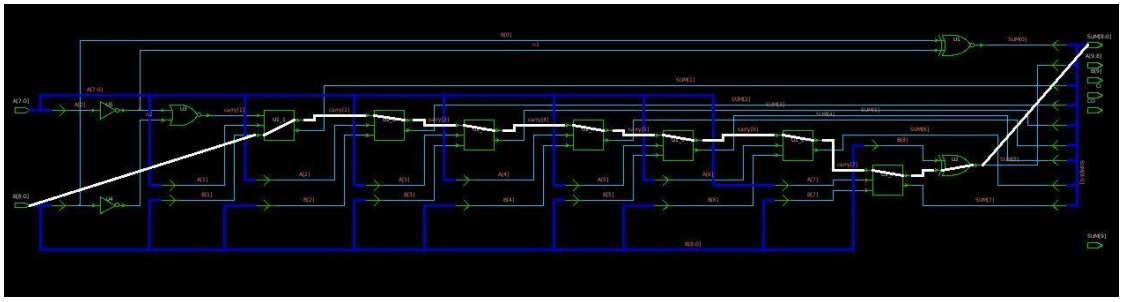
   Gate count=560/5=112

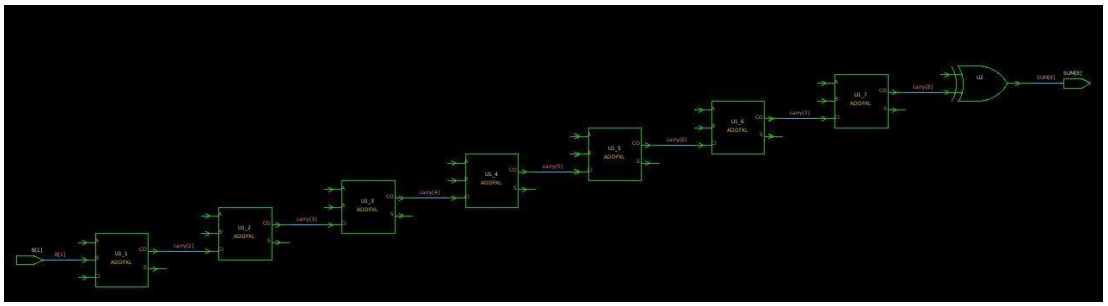
(2) critical path delay
add.v





add_syn.v





(3) power consumption

```
Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =  62.3304 uW   (87%)
  Net Switching Power  =   9.5161 uW   (13%)
                         ---------
Total Dynamic Power    =  71.8464 uW  (100%)

Cell Leakage Power     = 630.9841 nW


***** End Of Report *****
```

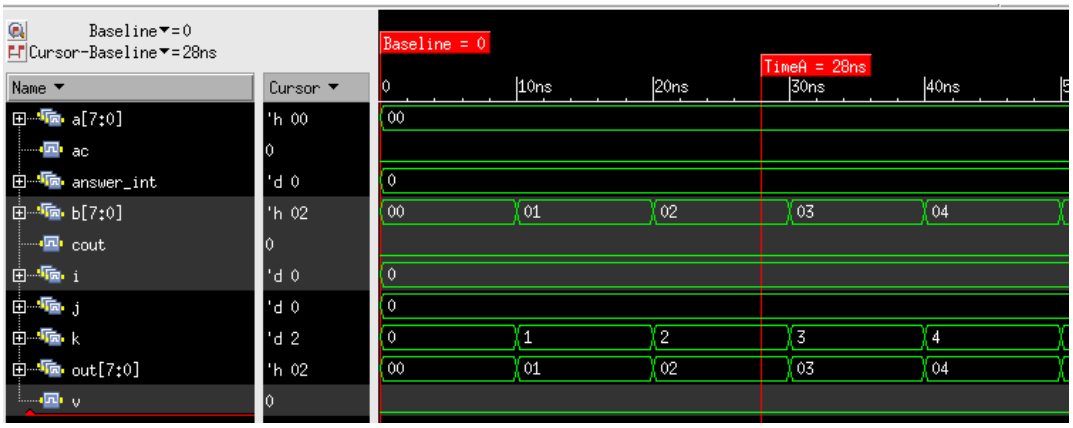
3. 結果分析

結果分析：

沒有 overflow 的加法

```
  00  000  000
      0
   0  000  0000
      0
+  0  000  0010
      0
-------------------
   0  000  0010
      0
```

合成前



合成後

Output有delay不會因INPUT改變馬上改變

有 overflow 的加法

01 111 111

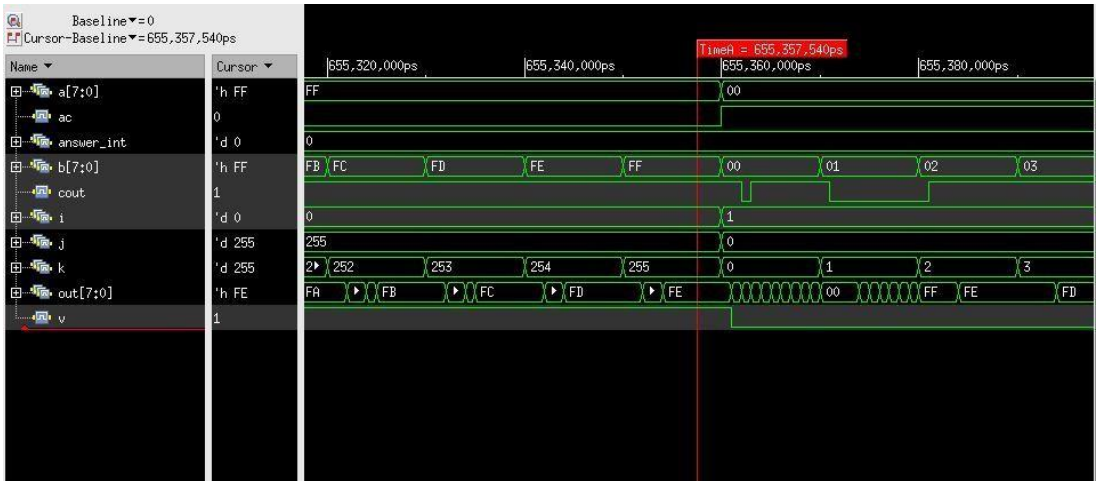
1

合成前 0 111 1111

1

合成後

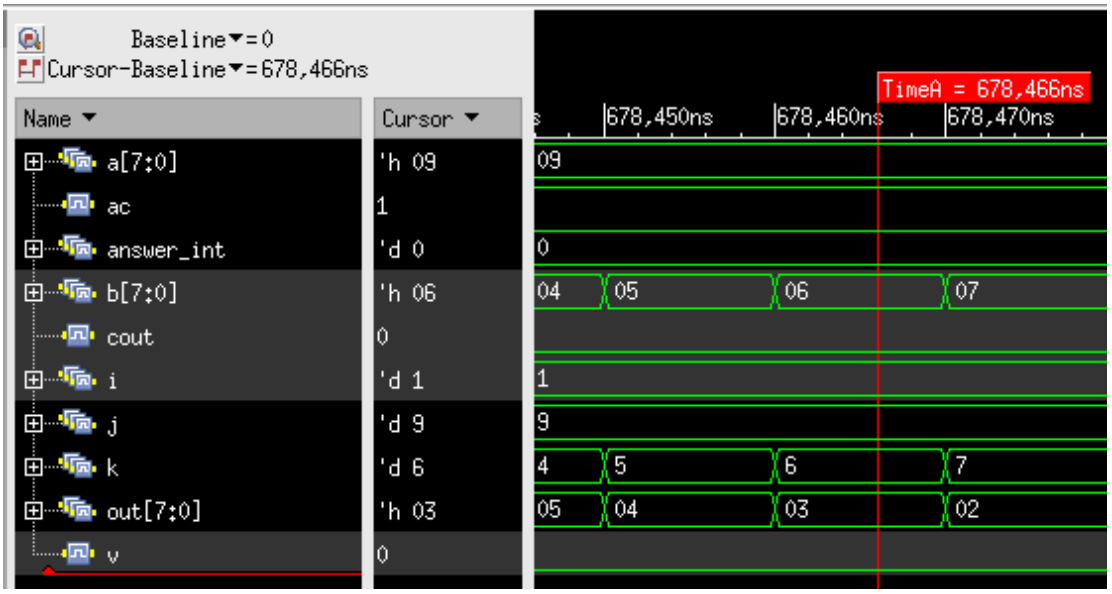
可能code寫不好，delay太久



無 overflow 但是運算完為正數的減法

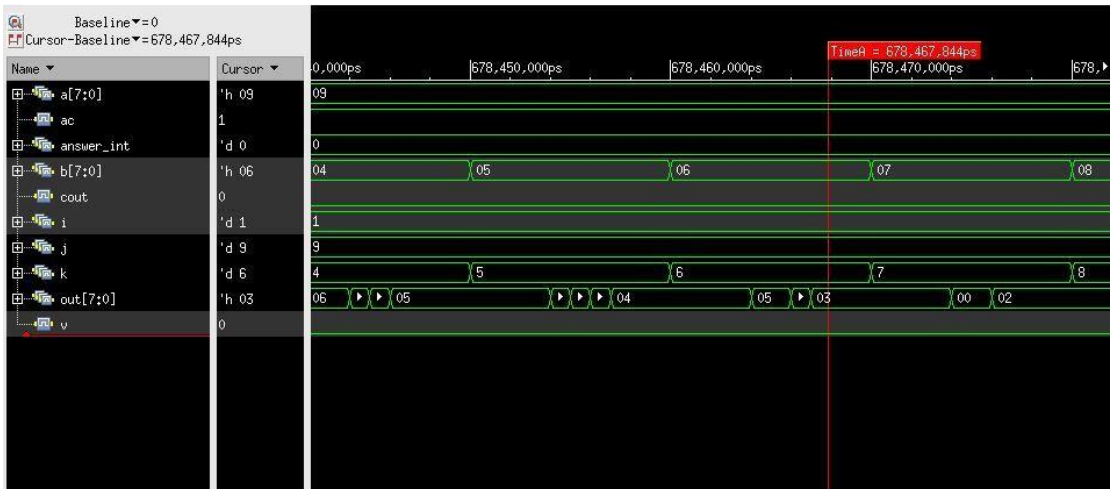
1 111 000
1
0 000 1001
0
+ 1 111 1010
1

合成前 0 000 0011
0



合成後

Delay時間都偏長



無overflow 但是運算完為負數的減法 將結果減一再 1 跟0 互換再加上負號即為所求

```
  00  000  000
        0
   0  000  0000
        0
+ 1  000  0001
        0
-------------------
   1  000  0001
        0
```

合成前

合成後

波型正確但delay相對HW1_1 長

Use the Synopsys Design Vision EDA tool to synthesize my circuits in HW1-2_Vote

1. my synthesis procedure :

   step1.check setup file:確定要執行設計檔的資料夾中

   有 .synopsys_dc.setup 沒有則前往課程的FTP複製並改檔名

   step2.invoke design compiler:在putty指令輸入 dv

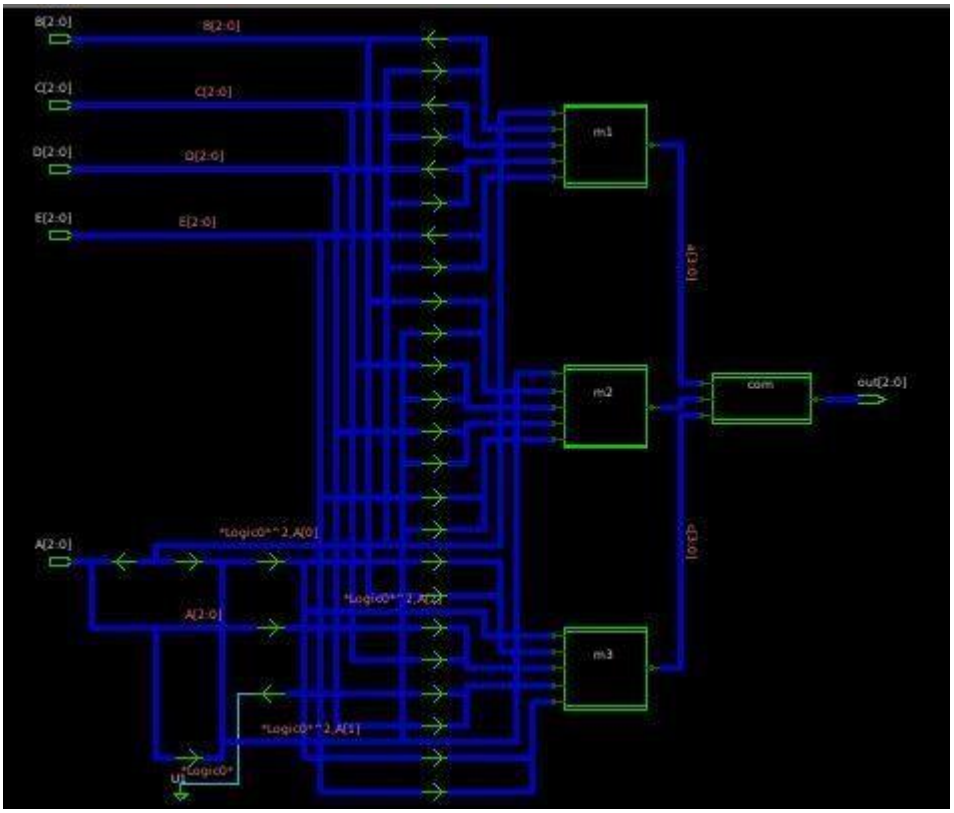
   step3.:check if library is correctly loaded 結果:有

   step4.read file :選擇想要合成的檔案並確認沒有errors及warning

   結果：無errors及warning

   Step5.symbol view

   Step6.schematic view



Step7. Prevent Possible Assign Statement Problem:

在command line 鍵入

set_fix_multiple_port_nets -all -buffer_constants

step9:compile design:結果 Optimization Complete

step10.Area report:

```
Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /mnt2/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:                18
Number of nets:                 31
Number of cells:                 4
Number of references:            4

Combinational area:       1537.844365
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:          1537.844365
Total area:                 undefined

***** End Of Report *****
```

Step11Timing report:
MAX

Point	Incr	Path
input external delay	0.00	0.00 f
B[0] (in)	0.00	0.00 f
m1/B[0] (fa4_0)	0.00	0.00 f
m1/f0/B[0] (rca3_0)	0.00	0.00 f
m1/f0/fa1/b (fa_0)	0.00	0.00 f
m1/f0/fa1/U3/Y (XOR2X1)	0.14	0.14 f
m1/f0/fa1/U2/Y (AO22X1)	0.34	0.48 f
m1/f0/fa1/cout (fa_0)	0.00	0.48 f
m1/f0/fa2/cin (fa_35)	0.00	0.48 f
m1/f0/fa2/U2/Y (AO22X1)	0.36	0.84 f
m1/f0/fa2/cout (fa_35)	0.00	0.84 f
m1/f0/fa3/cin (fa_34)	0.00	0.84 f
m1/f0/fa3/U2/Y (AO22X1)	0.36	1.19 f
m1/f0/fa3/cout (fa_34)	0.00	1.19 f
m1/f0/Cout (rca3_0)	0.00	1.19 f
m1/f1/C_in (rca3_11)	0.00	1.19 f
m1/f1/fa1/cin (fa_33)	0.00	1.19 f
m1/f1/fa1/U2/Y (AO22X1)	0.36	1.55 f
m1/f1/fa1/cout (fa_33)	0.00	1.55 f
m1/f1/fa2/cin (fa_32)	0.00	1.55 f
m1/f1/fa2/U2/Y (AO22X1)	0.36	1.91 f
m1/f1/fa2/cout (fa_32)	0.00	1.91 f
m1/f1/fa3/cin (fa_31)	0.00	1.91 f
m1/f1/fa3/U2/Y (AO22X1)	0.36	2.26 f
m1/f1/fa3/cout (fa_31)	0.00	2.26 f
m1/f1/Cout (rca3_11)	0.00	2.26 f
m1/f2/C_in (rca3_10)	0.00	2.26 f

m1/f2/fa1/cin (fa_30)	0.00	2.26 f
m1/f2/fa1/U2/Y (AO22X1)	0.36	2.62 f
m1/f2/fa1/cout (fa_30)	0.00	2.62 f
m1/f2/fa2/cin (fa_29)	0.00	2.62 f
m1/f2/fa2/U2/Y (AO22X1)	0.36	2.98 f
m1/f2/fa2/cout (fa_29)	0.00	2.98 f
m1/f2/fa3/cin (fa_28)	0.00	2.98 f
m1/f2/fa3/U2/Y (AO22X1)	0.36	3.34 f
m1/f2/fa3/cout (fa_28)	0.00	3.34 f
m1/f2/Cout (rca3_10)	0.00	3.34 f
m1/f3/C_in (rca3_9)	0.00	3.34 f
m1/f3/fa1/cin (fa_27)	0.00	3.34 f
m1/f3/fa1/U2/Y (AO22X1)	0.36	3.69 f
m1/f3/fa1/cout (fa_27)	0.00	3.69 f
m1/f3/fa2/cin (fa_26)	0.00	3.69 f
m1/f3/fa2/U2/Y (AO22X1)	0.36	4.05 f
m1/f3/fa2/cout (fa_26)	0.00	4.05 f
m1/f3/fa3/cin (fa_25)	0.00	4.05 f
m1/f3/fa3/U1/Y (XOR2X1)	0.17	4.22 r
m1/f3/fa3/s (fa_25)	0.00	4.22 r
m1/f3/Sum[2] (rca3_9)	0.00	4.22 r
m1/out[2] (fa4_0)	0.00	4.22 r
com/A[2] (compare)	0.00	4.22 r
com/U39/Y (CLKINVX1)	0.14	4.36 f
com/U38/Y (XOR2X1)	0.18	4.54 f
com/U5/Y (AOI32X1)	0.23	4.77 r
com/U4/Y (NOR2X1)	0.08	4.85 f
com/U3/Y (OAI21XL)	0.18	5.03 r
com/U2/Y (OAI2BB1X1)	0.07	5.10 f
com/U1/Y (AO22X1)	0.30	5.40 f
com/out[2] (compare)	0.00	5.40 f
out[2] (out)	0.00	5.40 f
data arrival time		5.40

(Path is unconstrained)

MIN

```
input external delay                          0.00       0.00 r
E[0] (in)                                     0.00       0.00 r
m1/E[0] (fa4_0)                               0.00       0.00 r
m1/f3/B[0] (rca3_9)                           0.00       0.00 r
m1/f3/fa1/b (fa_27)                           0.00       0.00 r
m1/f3/fa1/U2/Y (AO22X1)                       0.16       0.16 r
m1/f3/fa1/cout (fa_27)                        0.00       0.16 r
m1/f3/fa2/cin (fa_26)                         0.00       0.16 r
m1/f3/fa2/U1/Y (XOR2X1)                       0.09       0.25 f
m1/f3/fa2/s (fa_26)                           0.00       0.25 f
m1/f3/Sum[1] (rca3_9)                         0.00       0.25 f
m1/out[1] (fa4_0)                             0.00       0.25 f
com/A[1] (compare)                            0.00       0.25 f
com/U16/Y (OAI22XL)                           0.13       0.39 r
com/U15/Y (NOR3BXL)                           0.11       0.50 f
com/U14/Y (AOI211X1)                          0.13       0.63 r
com/out[1] (compare)                          0.00       0.63 r
out[1] (out)                                  0.00       0.63 r
data arrival time                                        0.63
-----------------------------------------------------------------
(Path is unconstrained)
```

Step12.power report:

```
        slow (File: /mnt2/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)


    Operating Conditions: slow   Library: slow
    Wire Load Model Mode: top


    Global Operating Voltage = 1.08
    Power-specific unit information :
        Voltage Units = 1V
        Capacitance Units = 1.000000pf
        Time Units = 1ns
        Dynamic Power Units = 1mW    (derived from V,C,T units)
        Leakage Power Units = 1pW


      Cell Internal Power  = 120.0071 uW   (67%)
      Net Switching Power  =  60.2136 uW   (33%)
                             ---------
    Total Dynamic Power    = 180.2206 uW  (100%)

    Cell Leakage Power     =   1.7432 uW


    ***** End Of Report *****
```

Step13.

Save Design - Circuit and Timing Files:

Step14. Rerun Verilog Simulation:修改testbench.v並跑波型觀察2.The statistics of your designs including (1) gate count, (2) critical path delay, and (3) power consumption.

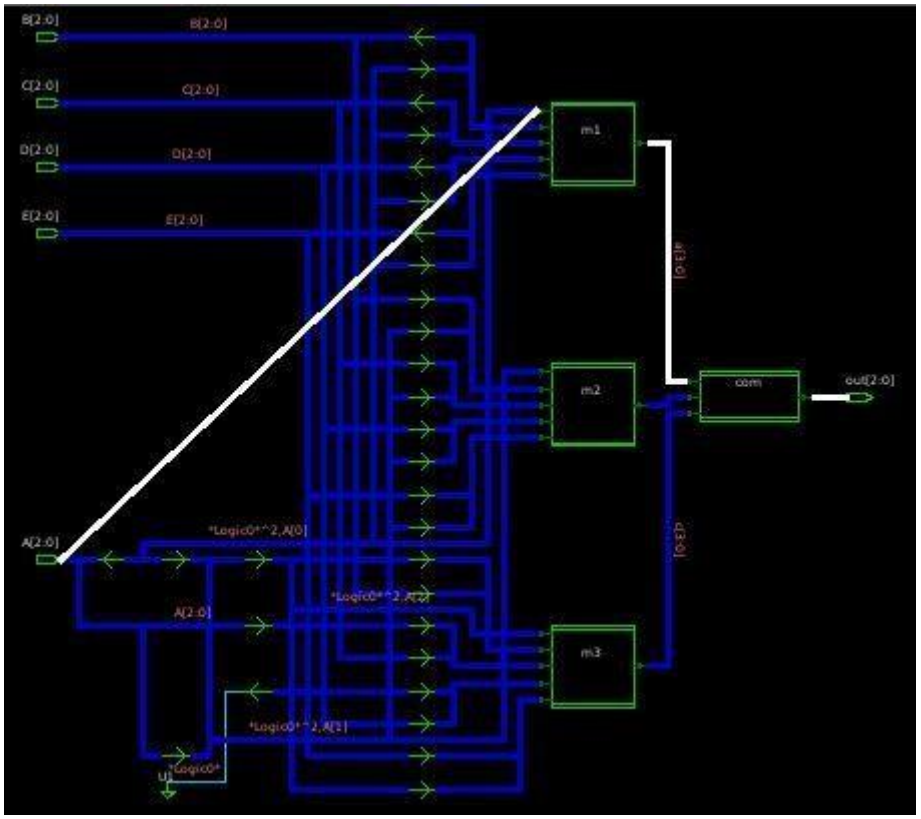
(1) gate count

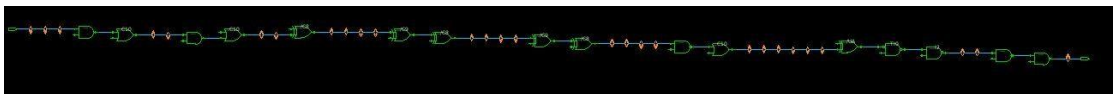
由AREA report中的total cell area 1537，除以NAND2 gate area約5um^2

Gate count=1537/5

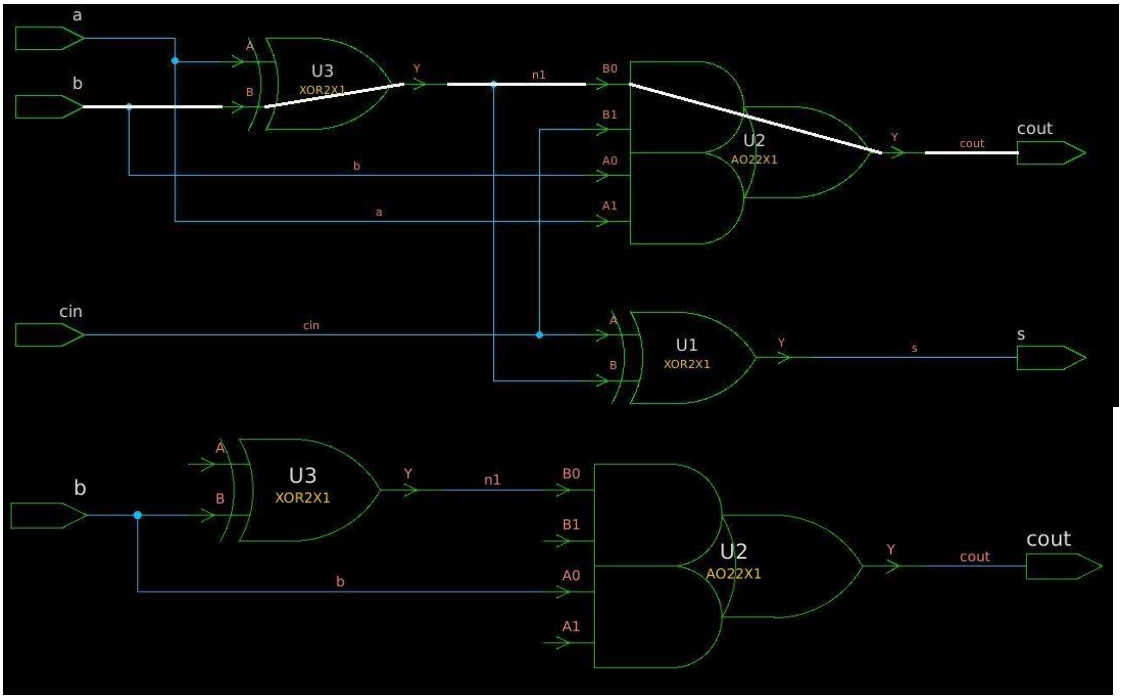
(2) critical path delay

Vote1.v





Vote1_syn.v



3.結果分析

結果分析：

當 A 為 1、B 為 4、C 為 4、D 為 2、E 為 1 時，a、b、c 分別為第 1bit 和、第 2bit 和 、 第 3bit， a=1+0+0+0+1=2，

b=0+0+0+1+0=1，c=0+1+1+0+0=2，

其因為 a=c 代表兩個數出現次數多為最多，故輸出為 000。

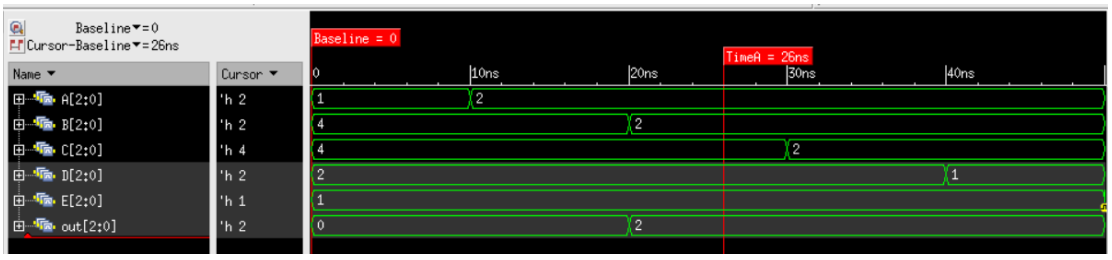
當A 為2、B 為2、C 為4、D 為2、E 為1 時， a=0+0+0+0+1=1，

b=1+1+0+1+0=3，c=0+0+1+0+0=1，

其中 b 大於a 跟c，故輸出為 010。合

成前

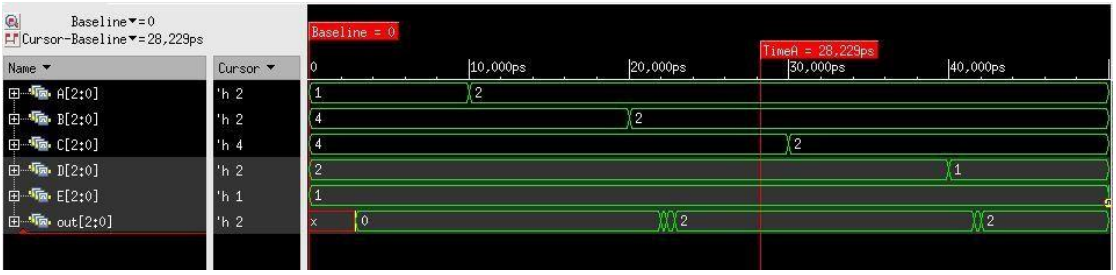
```
 0 A=001, B=100, C=100, D=010, E=001, out=000
10 A=010, B=100, C=100, D=010, E=001, out=000
20 A=010, B=010, C=100, D=010, E=001, out=010
30 A=010, B=010, C=010, D=010, E=001, out=010
40 A=010, B=010, C=010, D=001, E=001, out=010
```

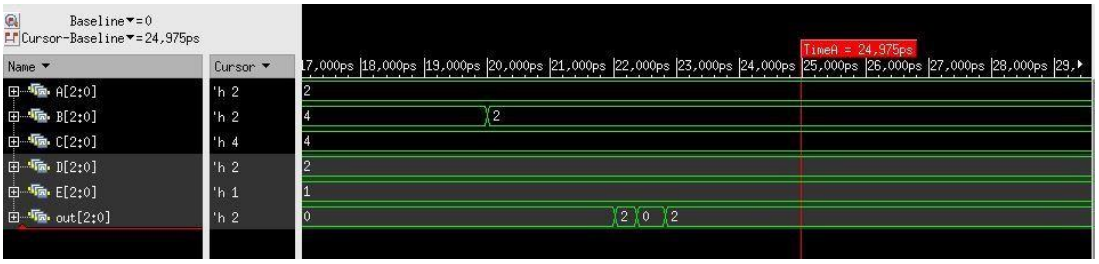


合成後

波型出現明顯的delay，而因為monitor是A,B,C,D,E,out有改變就印一次，所以putty結果比合成前多印好幾次

```
 0 A=001, B=100, C=100, D=010, E=001, out=xxx
 3 A=001, B=100, C=100, D=010, E=001, out=x0x
 3 A=001, B=100, C=100, D=010, E=001, out=x00
 3 A=001, B=100, C=100, D=010, E=001, out=000
10 A=010, B=100, C=100, D=010, E=001, out=000
20 A=010, B=010, C=100, D=010, E=001, out=000
22 A=010, B=010, C=100, D=010, E=001, out=010
22 A=010, B=010, C=100, D=010, E=001, out=000
23 A=010, B=010, C=100, D=010, E=001, out=010
30 A=010, B=010, C=010, D=010, E=001, out=010
40 A=010, B=010, C=010, D=001, E=001, out=010
42 A=010, B=010, C=010, D=001, E=001, out=000
42 A=010, B=010, C=010, D=001, E=001, out=010
```





Use the Synopsys Design Vision EDA tool to synthesize my circuits in HW1-2_Mid

2. my synthesis procedure :

step1.check setup file:確定要執行設計檔的資料夾中

有 .synopsys_dc.setup 沒有則前往課程的FTP複製並改檔名

step2.invoke design compiler:在putty指令輸入 dv

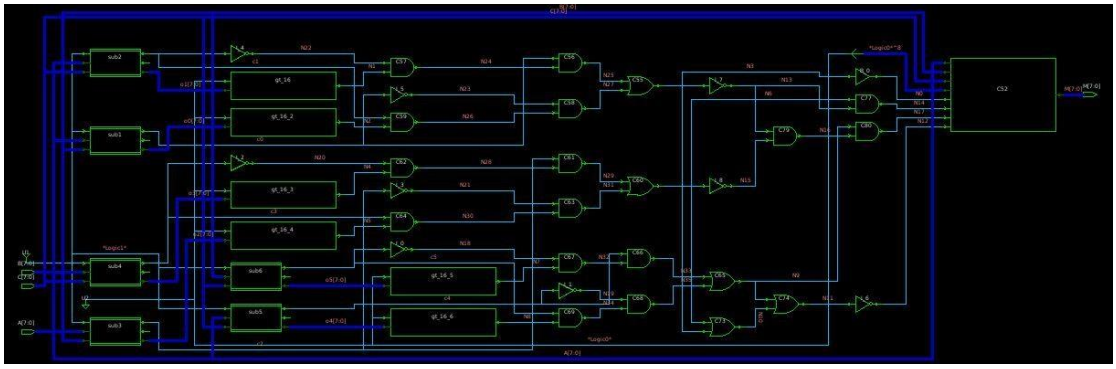
step3.:check if library is correctly loaded 結果:有

step4.read file :選擇想要合成的檔案並確認沒有errors及warning

結果：無errors及warning

Step5.symbol view

Step6.schematic view



Step7. Prevent Possible Assign Statement Problem:

在command line 鍵入

set_fix_multiple_port_nets -all -buffer_constants

step9:compile design:結果 Optimization Complete

step10.Area report:

```
Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /mnt2/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:              32
Number of nets:              118
Number of cells:              45
Number of references:         14

Combinational area:       3700.332067
Noncombinational area:       0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:          3700.332067
Total area:                 undefined

***** End Of Report *****
```

Step11Timing report:
MAX

```
Point                                                    Incr       Path
---------------------------------------------------------------------------
input external delay                                     0.00       0.00 r
B[1] (in)                                                0.00       0.00 r
sub1/B[1] (Add_0)                                        0.00       0.00 r
sub1/U12/Y (CLKINVX1)                                    0.03       0.03 f
sub1/add_28/A[1] (Add_0_DW01_inc_0)                      0.00       0.03 f
sub1/add_28/U1_1_1/S (ADDHXL)                            0.22       0.25 f
sub1/add_28/SUM[1] (Add_0_DW01_inc_0)                    0.00       0.25 f
sub1/U21/Y (CLKMX2X2)                                    0.18       0.43 f
sub1/r311/B[1] (Add_0_DW01_add_0)                        0.00       0.43 f
sub1/r311/U1_1/CO (ADDFXL)                               0.61       1.04 f
sub1/r311/U1_2/CO (ADDFXL)                               0.38       1.41 f
sub1/r311/U1_3/CO (ADDFXL)                               0.38       1.79 f
sub1/r311/U1_4/CO (ADDFXL)                               0.38       2.16 f
sub1/r311/U1_5/CO (ADDFXL)                               0.38       2.54 f
sub1/r311/U1_6/CO (ADDFXL)                               0.38       2.92 f
sub1/r311/U1_7/CO (ADDFXL)                               0.37       3.29 f
sub1/r311/U2/Y (XOR2X1)                                  0.18       3.47 f
sub1/r311/SUM[8] (Add_0_DW01_add_0)                      0.00       3.47 f
sub1/Cout (Add_0)                                        0.00       3.47 f
U77/Y (AO21X1)                                           0.26       3.73 f
U76/Y (MXI2X1)                                           0.33       4.06 r
U60/Y (NOR3BXL)                                          0.32       4.38 f
U45/Y (AOI222XL)                                         0.45       4.83 r
U44/Y (CLKINVX1)                                         0.06       4.89 f
M[7] (out)                                               0.00       4.89 f
data arrival time                                                   4.89
---------------------------------------------------------------------------
(Path is unconstrained)
```

MIN

```
Startpoint: A[7] (input port)
Endpoint: M[7] (output port)
Path Group: (none)
Path Type: min

Point                                              Incr       Path
-----------------------------------------------------------------
input external delay                               0.00       0.00 r
A[7] (in)                                          0.00       0.00 r
U45/Y (AOI222XL)                                   0.07       0.07 f
U44/Y (CLKINVX1)                                   0.04       0.11 r
M[7] (out)                                         0.00       0.11 r
data arrival time                                             0.11
-----------------------------------------------------------------
(Path is unconstrained)



**** End Of Report *****
```

Step12.power report:

```
Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 360.4350 uW   (79%)
  Net Switching Power  =  97.4219 uW   (21%)
                         ---------
Total Dynamic Power    = 457.8570 uW  (100%)

Cell Leakage Power     =   3.9603 uW
```

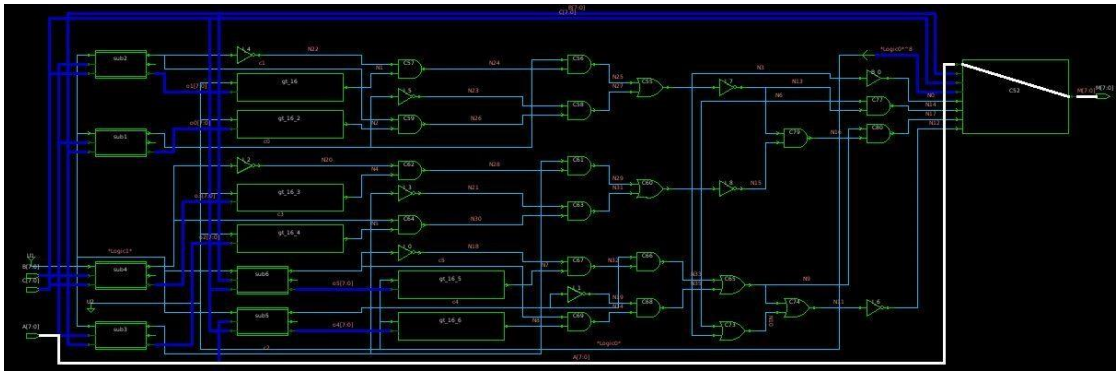
Step13.

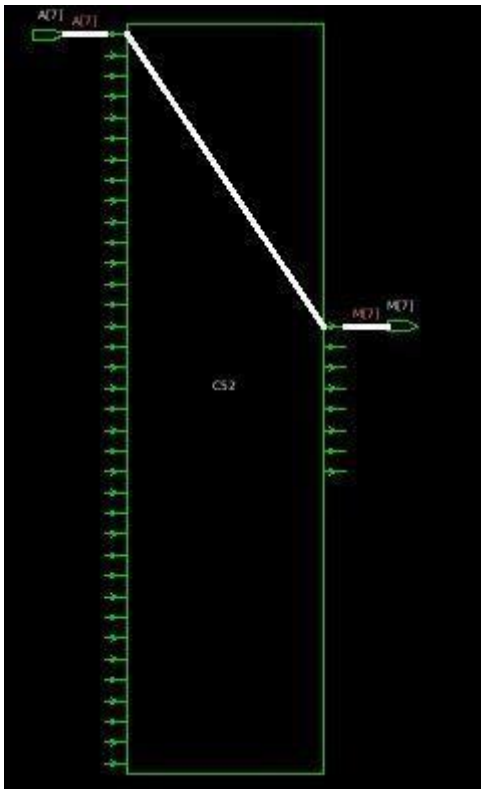
Save Design - Circuit and Timing Files:

Step14. Rerun Verilog Simulation:修改testbench.v並跑波型觀察

2. The statistics of your designs including (1) gate count, (2) critical path delay, and (3) power consumption.
   (1) gate count
   由AREA report中的total cell area 3700，除以NAND2 gate area約5um^2
   Gate count=3700/5=740

   (2) critical path delay
   Mid.v





Mid_syn.v

3. 結果分析

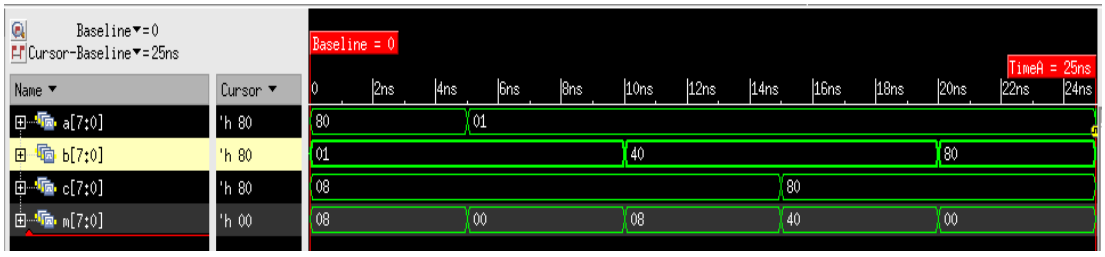
合成前

如下圖

第一行：當 A 為'h80，B 為'h01，C 為'h08 時，因為 B 符合[(B-C>0 且B-A<0)或(B-C<0 且 B-A>0)](即 B 大小位於 A、C 之間)，故輸出 B。

第二行：當 A 為'h01，B 為'h01，C 為'h08 時，因為有輸入相同，故無法符合[(A-B>0且A-C<0)或(A-B<0且A-C>0)]或[(B-C>0且B-A<0)或(B-C<0且B-A>0)]或[(C-B>0且C-A<0)或(C-B<0且C-A>0)]，於是輸出為 8'b00000000。

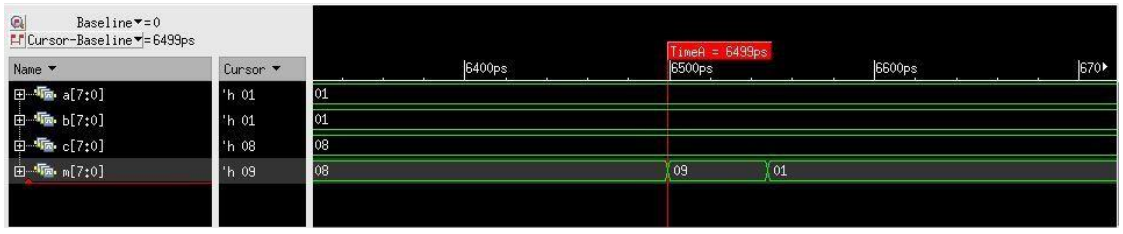
```
  0 A=10000000, B=00000001, C=00001000, M=00001000
  5 A=00000001, B=00000001, C=00001000, M=00000000
 10 A=00000001, B=01000000, C=00001000, M=00001000
 15 A=00000001, B=01000000, C=10000000, M=01000000
 20 A=00000001, B=10000000, C=10000000, M=00000000
```

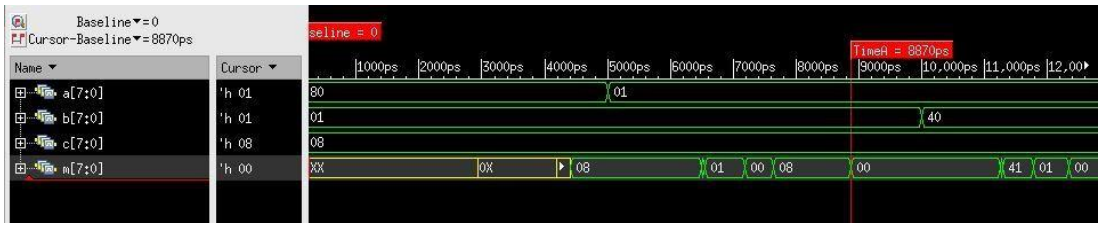


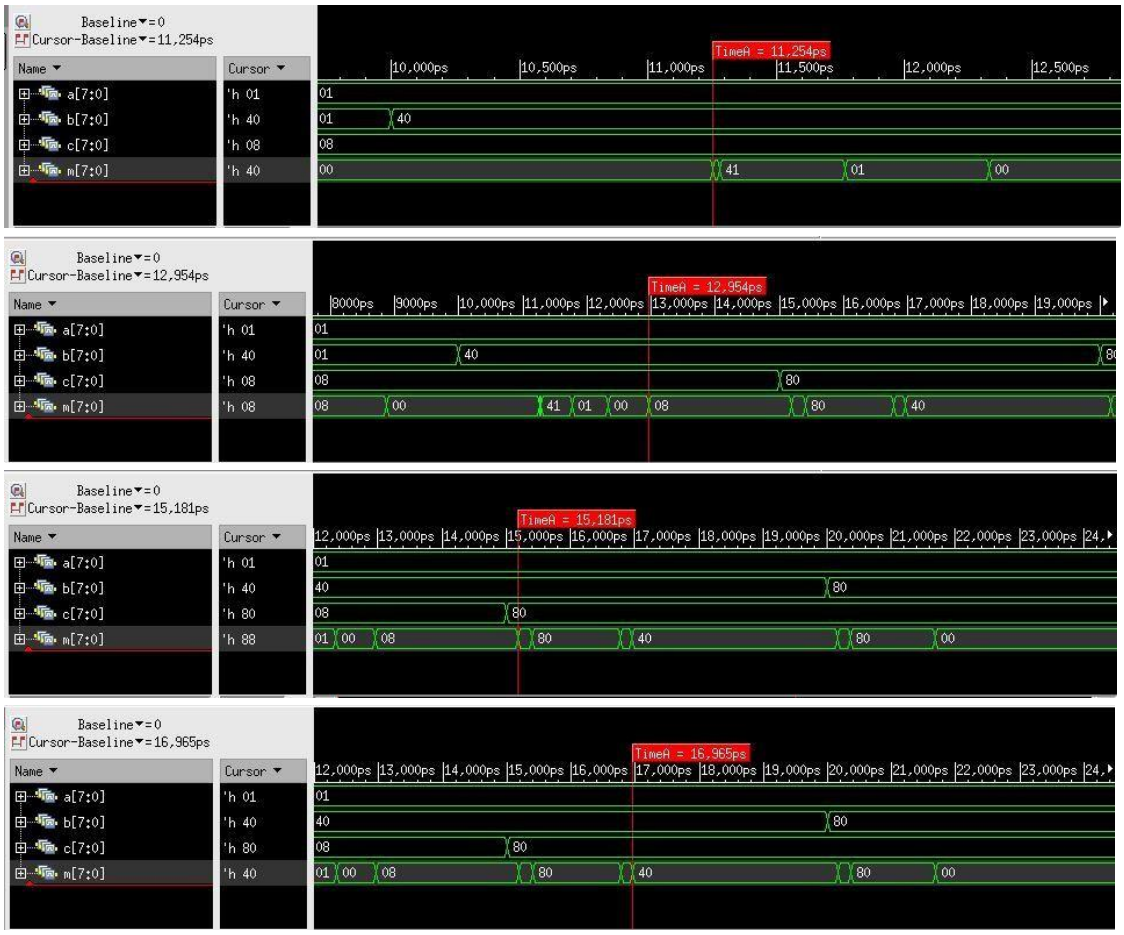
合成後

波型出現明顯的delay，而因為monitor是A,B,C,D,E,out有改變就印一次，所以putty結果比合成前多印好幾次

```
 0 A=10000000, B=00000001, C=00001000, M=xxxxxxxx
 0 A=10000000, B=00000001, C=00001000, M=x000x00x
 3 A=10000000, B=00000001, C=00001000, M=0000x00x
 4 A=10000000, B=00000001, C=00001000, M=0000x000
 4 A=10000000, B=00000001, C=00001000, M=00001000
 5 A=00000001, B=00000001, C=00001000, M=00001000
 6 A=00000001, B=00000001, C=00001000, M=00001001
 7 A=00000001, B=00000001, C=00001000, M=00000001
 7 A=00000001, B=00000001, C=00001000, M=00000000
 8 A=00000001, B=00000001, C=00001000, M=00001000
 9 A=00000001, B=00000001, C=00001000, M=00000000
10 A=00000001, B=01000000, C=00001000, M=00000000
11 A=00000001, B=01000000, C=00001000, M=01000000
11 A=00000001, B=01000000, C=00001000, M=01000001
12 A=00000001, B=01000000, C=00001000, M=00000001
12 A=00000001, B=01000000, C=00001000, M=00000000
13 A=00000001, B=01000000, C=00001000, M=00001000
15 A=00000001, B=01000000, C=10000000, M=00001000
15 A=00000001, B=01000000, C=10000000, M=10001000
15 A=00000001, B=01000000, C=10000000, M=10000000
17 A=00000001, B=01000000, C=10000000, M=00000000
17 A=00000001, B=01000000, C=10000000, M=01000000
20 A=00000001, B=10000000, C=10000000, M=01000000
20 A=00000001, B=10000000, C=10000000, M=11000000
20 A=00000001, B=10000000, C=10000000, M=10000000
22 A=00000001, B=10000000, C=10000000, M=00000000
```







討論:

再跑模擬合成軟體時，遇到一個問題，那就是所謂的求critical path 好像是跑你當前讀入的.v檔，也就是為合成的電路，於是我要找critical path 時讀入 _syn.v檔，