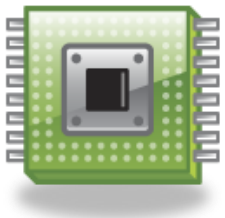

Homework #1-2 (Deadline : 2018/4/29 Sun. 9AM)

- **Use the *Synopsys Design Vision* EDA tool to synthesize your circuits in HW1-1.**
- **Hand in a report describing:**
  1. **Your synthesis procedure** 說明一下你在合成的時候做了哪些設定，還有為什麼要這樣做
  2. **The statistics of your designs including (1) gate count, (2) critical path delay, and (3) power consumption.**
  3. **The simulation results of the synthesized design and their correctness explanation. Compare the post-synthesis results with those of your original (pre-synthesis) designs. Describe the delay effect.**
  4. **Discussions**
- **Upload your report and designs including the synthesized circuits, testbench files and .sdf timing files to the course FTP.**