UG-2864ASYCG01

UG-2864ASOCG01

Evaluation Kit User Guide

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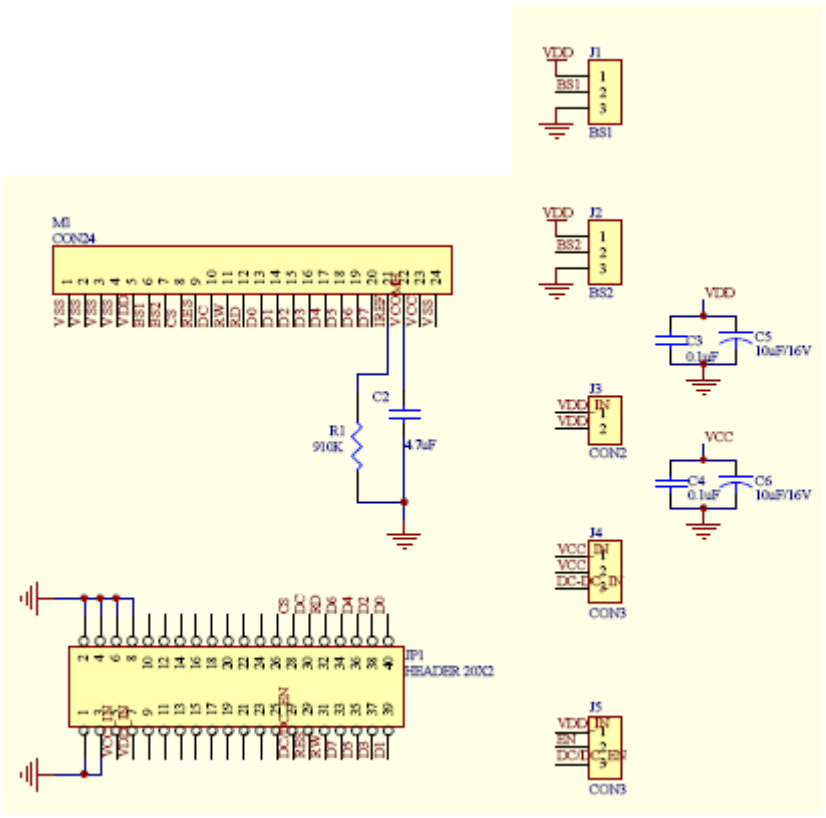
Version: Preliminary

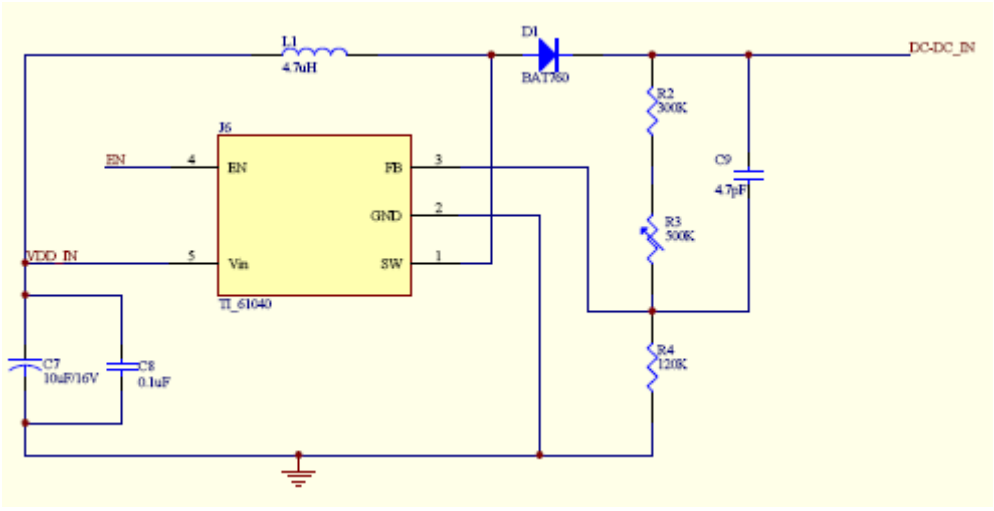
Contents

1. REVISION HISTORY

Date	Page	Contents	Version
2007/11/28		Preliminary	Preliminary 0.0

2. EVK Schematic





3. Symbol define

VCC : Power supply for panel driving voltage.

VSS：This is ground pin.

VDD：Power supply for core logic operation.

VDDIO：Power supply for interface logic level.

BS0~BS2：MUC bus interface selection pin(BS0 pulled LOW in internal).

CS：This pin is chip select input(active LOW).

RES：This pin is reset signal input(active LOW).

D/C：This is DATA/COMMAND control pin. When it is Pulled HIGH, the data at D[0~7] is treated as data. When it is pulled LOW, the data at D[0~7] will be transferred to the command register.

In I2C mode, this pin acts as SA0 for slave address select.

R/W：This is read/write control input pin connecting to the MCU interface.

When interface to a 6800-series microprocessor , Read mode will be carried out when this pin is pulled HIGH and write mode when low .

When interface to an 8080-microprocessor , this pin when be the data Write input.

When serial interface is selected, this pin must be connected to Vss.

E/RD：When interface to a 6800-series microprocessor , this pin will be used as the Enable(E) signal.

When interface to an 8080-microprocessor , this pin receives the Read(RD#)signal.

D0~D7：These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus.

When serial interface mode is selected, D0(SCLK) will be the serial clock input,D1(SDIN) will be the serial data input,D2 should be left opened.

When I2C mode is selected,D1(SDA_{in}) AND D2(SDA_{out}) should be tied together,D0(SCL) is the I2Cclock input

IREF：This is segment output current reference pin.

VCOMH：This pin for COM signal deselected level voltage.

4.TIMMING CHARACTERISTICS

4.1 80-Series MPU parallel Interface

WRITE CHARACTERISTICS

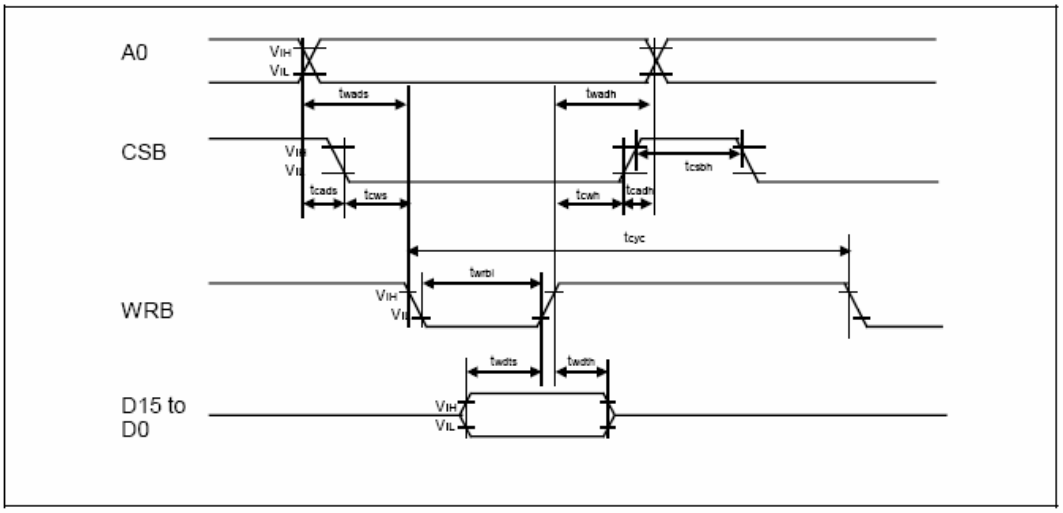


Figure 1 80-Series MPU parallel Interface Write Timing Diagram

(V_{DD} = 2.8V, Ta = 25 °C)

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{cyc}	Write cycle time	-	WRB	100	-	-	ns
t_{cads} t_{cadh}	Address and Select setup time Address and Select hold time	-	CSB,A0	0 0	- -	- -	ns
t_{wads} t_{wadh}	Address setup time Address hold time	-	A0	50 20	- -	- -	ns
t_{cws} t_{cwh}	Select setup time Select hold time	-	CSB	10 10	- -	- -	ns
t_{wrbl}	Write Low pulse width	-	WRB	30	-	-	ns
t_{csbh}	Select High pulse width	-	CSB	10	-	-	ns
t_{wdts} t_{wdth}	Data setup time Data hold time	-	D15 to D0	10 20	- -	- -	ns

Table 1 80-Series MPU parallel Interface Write Timing Characteristics

READ CHARACTERISTICS

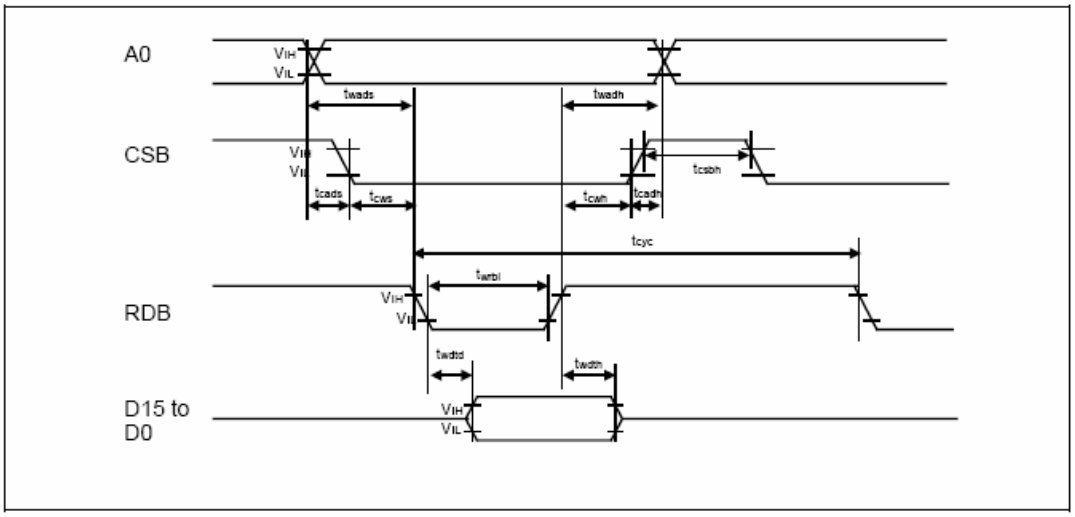


Figure 2 80-Series MPU parallel Interface Read Timing Diagram

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{cyc}	Read cycle time	-	RDB	500	-	-	ns
t_{cads} t_{cadh}	Address and Select setup time Address and Select hold time	-	CSB,A0	0 0	- -	- -	ns
t_{rads} t_{radh}	Address setup time Address hold time	-	A0	50 20	- -	- -	ns
t_{crs} t_{crh}	Select setup time Select hold time	-	CSB	10 10	- -	- -	ns
t_{rdbl}	Read Low pulse width	-	RDB	250	-	-	ns
t_{csbh}	Select High pulse width	-	CSB	10	-	-	ns
t_{rdtd} t_{rdth}	Data output delay time Data output hold time	CL = 100pF	D15 to D0	- 5	- -	200 -	ns

Table 2 80-Series MPU parallel Interface Read Timing Characteristics

4.2 6800-Series MPU parallel Interface

PARALLEL INTERFACE CHARACTERISTICS (6800-SERIES MPU)

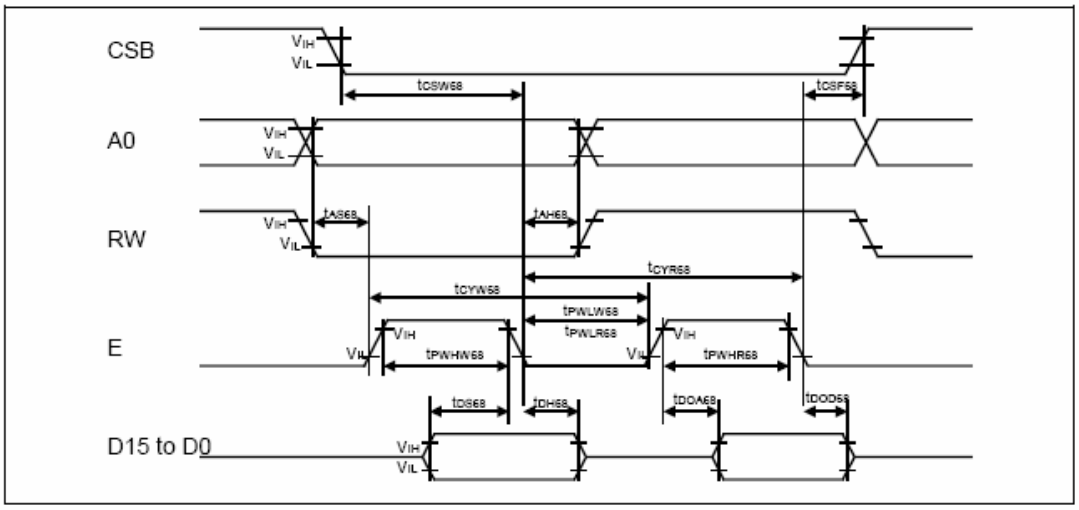


Figure 3 68-Series MPU parallel Interface Write Timing Diagram

(VSS=0V, VDD=2.8V,Ta = 25°C)

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CSW68} t_{CSF68}	Chip select setup time Chip select hold time	-	CSB	10 10	- -	- -	ns
t_{AS68} t_{AH68}	Address setup time Address hold time	-	A0 RW	50 20	- -	- -	ns
t_{CYW68} t_{PWHW68} t_{PWLW68}	Write cycle time Write High Time Write Low Time	-	E	160 40 90	-	-	ns
t_{CYR68} t_{PWHR68} t_{PWLR68}	Read cycle time (Parameter read) Read High (Parameter read) Read Low (Parameter read)	-	E	160 40 90	-	-	ns
t_{CYR68} t_{PWHR68} t_{PWLR68}	Read cycle time (Data read) Read High (Data read) Read Low (Data read)	-	E	450 355 90	-	-	ns
t_{DS68} t_{DH68}	Data setup time Data hold time	-	D15 to D0	10 20	- -	- -	ns
t_{DOA68} t_{DOD68}	Data output access time Data output disable time	CL = 30pF		- 40	- -	40 80	ns

Table 3 68-Series MPU parallel Interface Write Timing Characteristics

4.3 SPI Interface

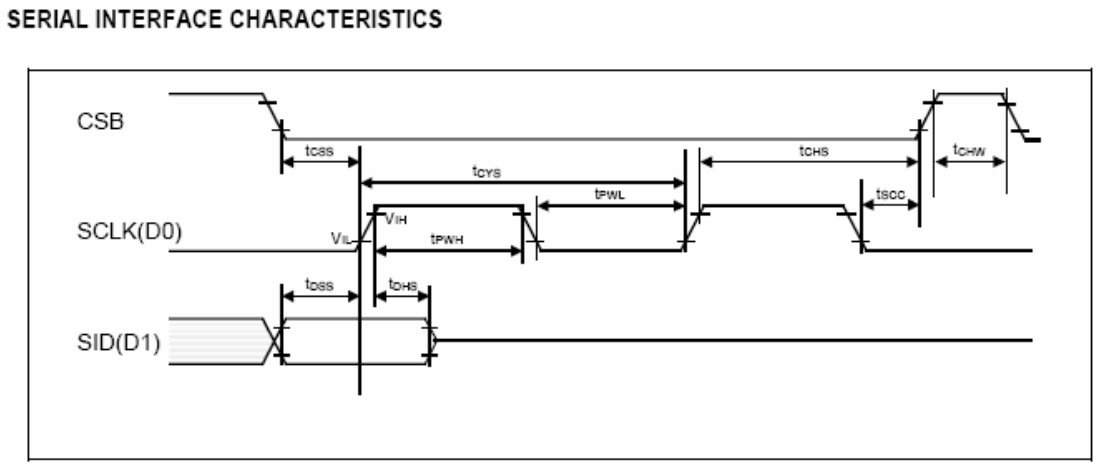


Figure 4 Serial peripheral interface Timing Diagram

(VSS=0V, VDD=2.8V,Ta = 25°C)

Symbol	Parameter	Conditions	Related Pins	MIN	TYP	MAX	Unit
t_{CYS} t_{WHS} t_{WLS}	Serial clock cycle High pulse width Low pulse width	-	SCLK	160 60 60	- -	- -	ns
t_{DSS} t_{DHS}	Data setup time Data hold time		SID (D1)	60 60	- -	- -	ns
t_{CSS} t_{CHS} t_{CHW}	Chip select setup time Chip select hold time Chip select high pulse width	-	CSB	60 65 45	- - -	- - -	ns
t_{SCC}	SCLK to Chip select	-	SCLK, CSB	20	-	-	ns

Table 4 Serial peripheral interface Timing Characteristics

5.EVK use introduction

Figure 5 EVK PCB and OLED Module

UG-2864ASYCG01 is COG type module, please refer to Fig5, Fig6.User can use leading wire to connect EVK with customer's system. The example shows as Fig7.

Figure 6 The combination of the module and EVK

Fig 7 EVK with test platform

Note 1：It is OLED high voltage supply.

Note 2：It is logic voltage supply.

Note 3：Those are leading wire connect to control board. Those are data pin.(D0-D7)

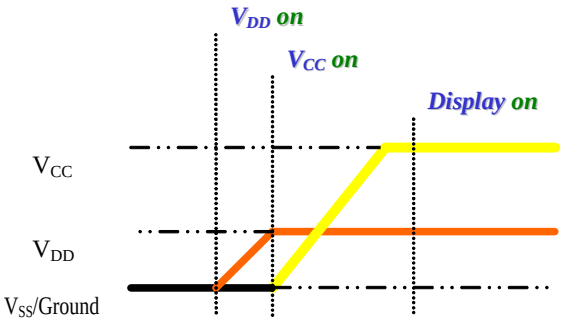
Note 4：Those are leading wire connect to control board. Those are control pin.
(DC, CS, RD, WR, RES)

6. Power down and Power up Sequence

To protect OLED panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

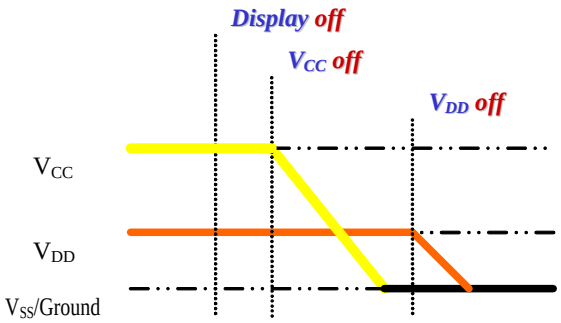
Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Driver IC Initial Setting
4. Clear Screen
5. Power up V_{DDH}
6. Delay 100ms
   (when V_{DD} is stable)
7. Send Display on command



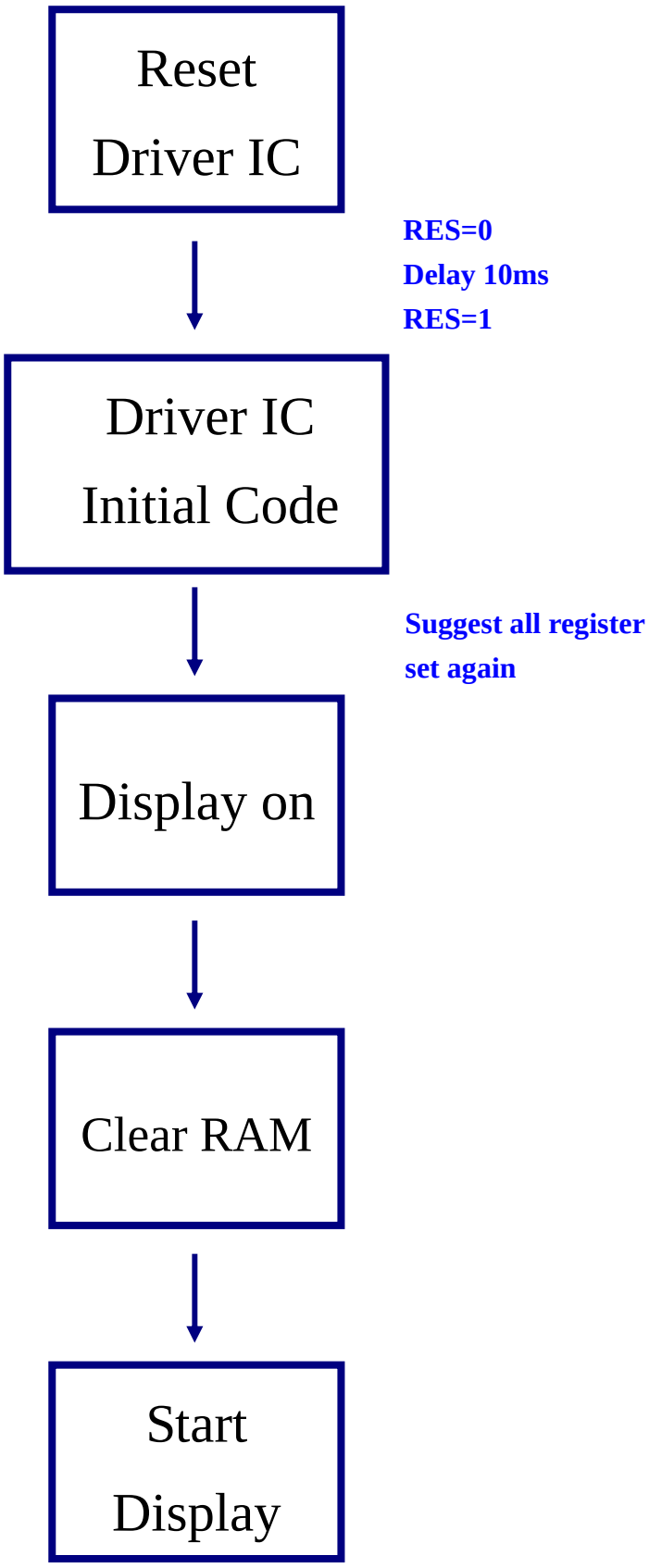
Power down Sequence:

1. Send Display off command
2. Power down V_{DDH}
3. Delay 100ms
   (when V_{DDH} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



7. How to use SSD1305 module

7.1 Initial Step Flow



7.2 RD recommends Initial Code:

```
void initial()
{
write_command(0xae);//(display on)
write_command(0x00);//set low column address
write_command(0x10);//set high column address
write_command(0x40);//(display start set)
write_command(0x2e);//(stop horzontal scroll)
write_command(0xb0);//(page address)
write_command(0x81);//(set contrast control register)
write_command(0x7f);
write_command(0xa1);//(set segment re-map)
write_command(0xa4);//(normal display mode)
write_command(0xa6);//(set normal/inverse display)
write_command(0xa8);//(set multiplex ratio)
write_command(0x3f);
write_command(0xd3);//(set display offset)
write_command(0x00);
write_command(0xad);//(set dc-dc on/off)
write_command(0x8e);//
write_command(0xc8);//(set com output scan direction)
write_command(0xd5);//(set display clock divide ratio/oscillator/frequency)
write_command(0xf0);//
write_command(0xd8);//(set area color mode on/off & low power display mode )
write_command(0x05);//
write_command(0xd9);//(set pre-charge period)
write_command(0xc2);
write_command(0xda);//(set com pins hardware configuration)
write_command(0x12);
write_command(0xdb);//(set vcom deselect level)
write_command(0x08);
write_command(0xaf);//(display on)
}
```

WRITE DATA & COMMAND SUB FUNCTION

```
void write_command(unsigned char aa)
{
IOCLR = 0x000000ff;
IOSET = RD_IN;//RD=1
```

```
IOCLR = DC_IN;//DC=0
IOCLR = CS_IN;//CS=0
IOCLR = WR_IN;//WR=0
IOSET = aa;//--------input command
IOSET = WR_IN;//WR=1
IOSET = CS_IN;//CS=1
IOCLR = RD_IN;
}
void write_data(unsigned char bb)
{
IOCLR = 0x000000ff;
IOSET = RD_IN;//RD=1
IOSET = DC_IN;//DC=1
IOCLR = CS_IN;//CS=0
IOCLR = WR_IN;//WR=0
IOSET = bb; //--------input data
IOSET = WR_IN;//WR=1
IOSET = CS_IN;//CS=1
}
```

Note：RD recommends Initial code and sub function for 8080 series CPU interface.