Lab01
Combinational Circuit

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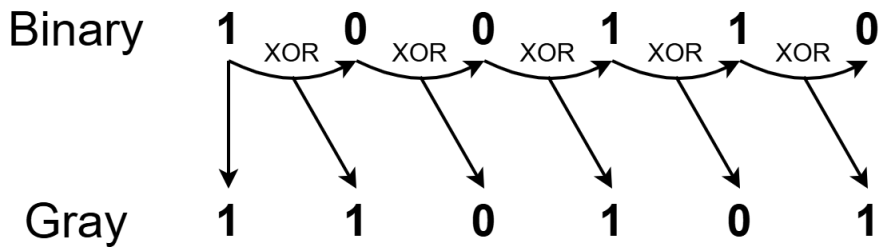
Combinational Circuit

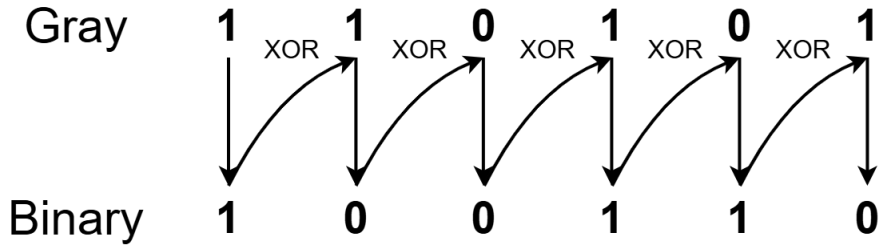
- The system takes four input numbers: **in_num0 ~ in_num3**
- Perform the specified **bitwise** operations based on the block diagram:
  - A = in_num0 XNOR in_num1
  - B = in_num1 OR in_num3
  - C = in_num0 AND in_num2
  - D = in_num2 XOR in_num3
- Then, group and calculate the sum
  - E = max(A, B) + max(C, D)
  - F = min(A, B) + min(C, D)
- Convert F into its **Gray code** representation, the outputs are E and the Gray-coded F

Combinational Circuit

- Gray code representation:
  - A Gray code has a property that the codes for successive decimal digits differ in exactly one bit
  - Binary to Gray conversion:

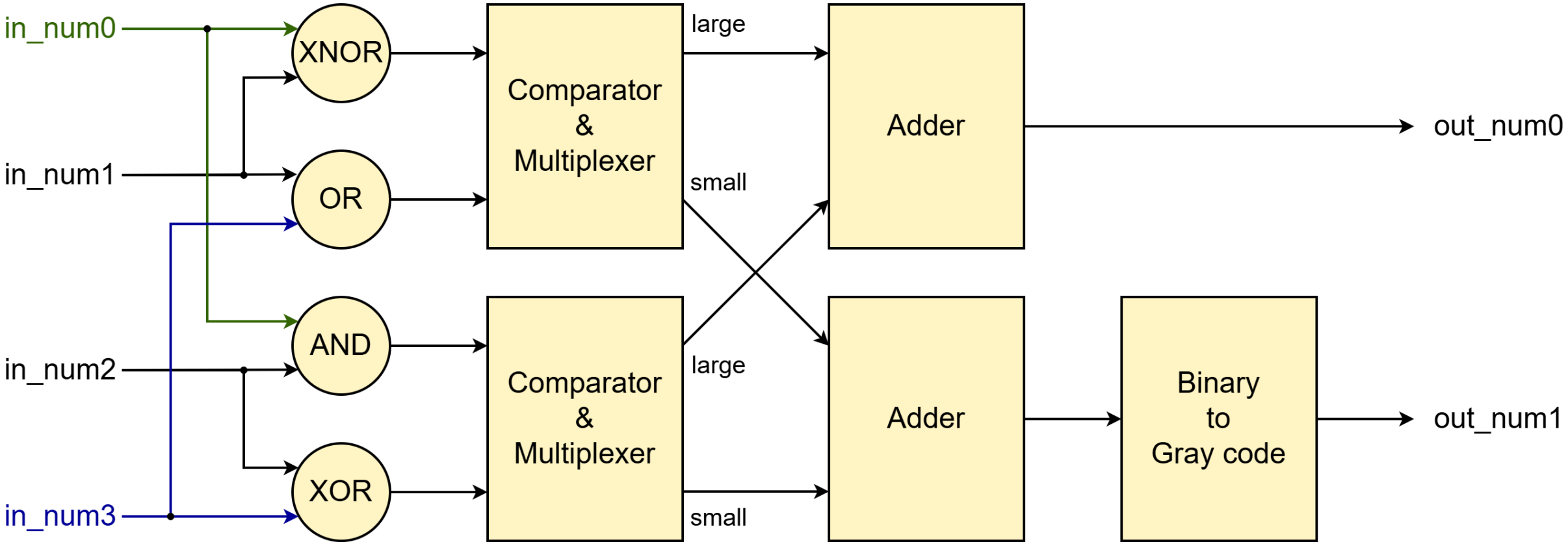


  - Gray to binary conversion:

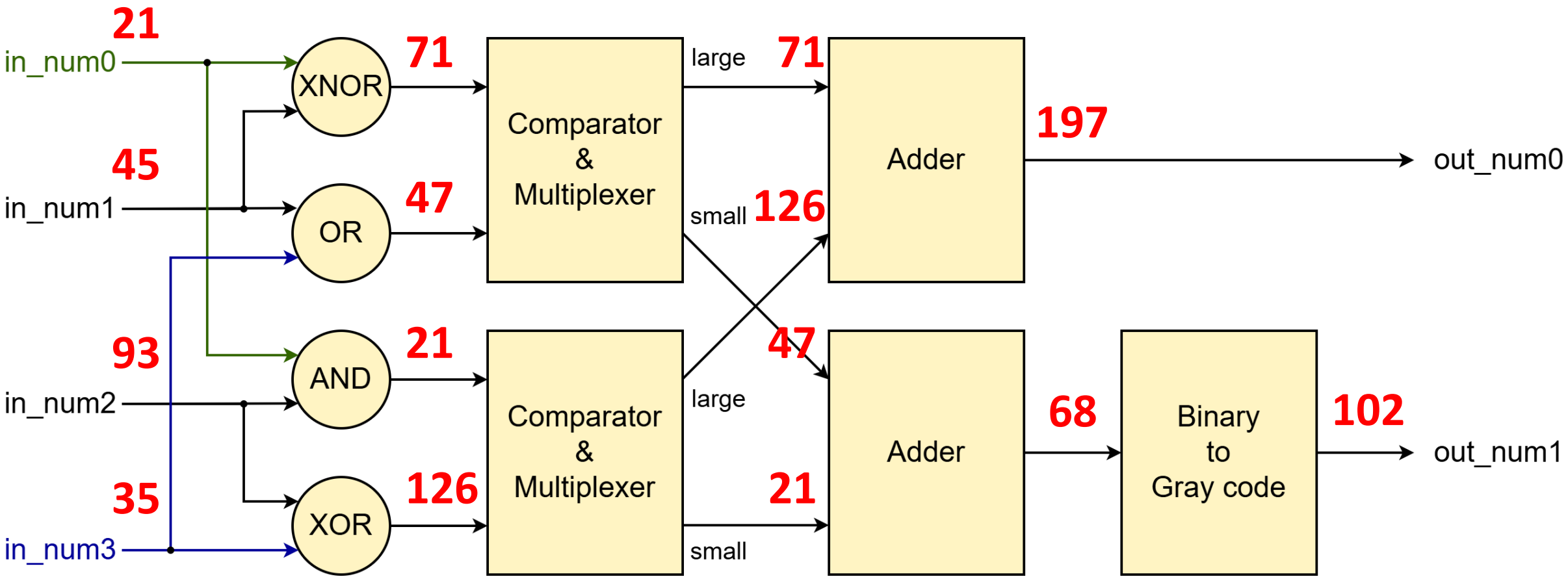


Decimal	Binary	Gray
0	000	000
1	001	001
2	010	011
3	011	010
4	100	110
5	101	111
6	110	101
7	111	100

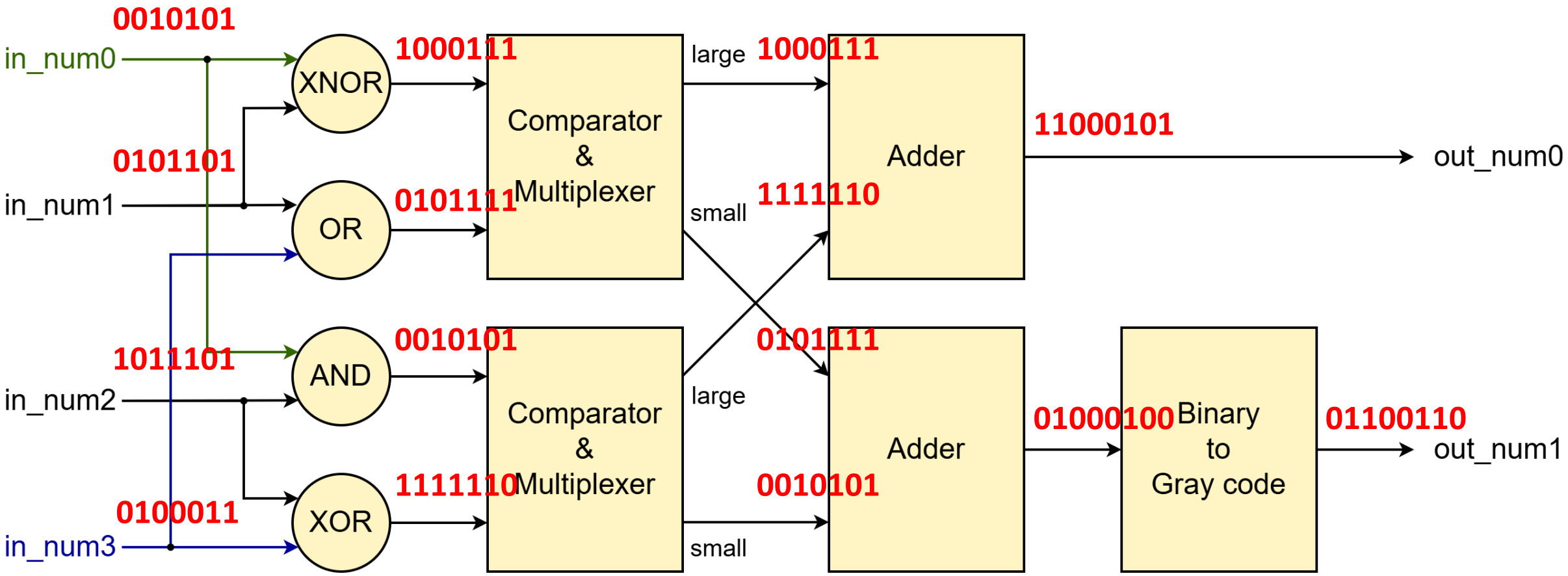
Block Diagram



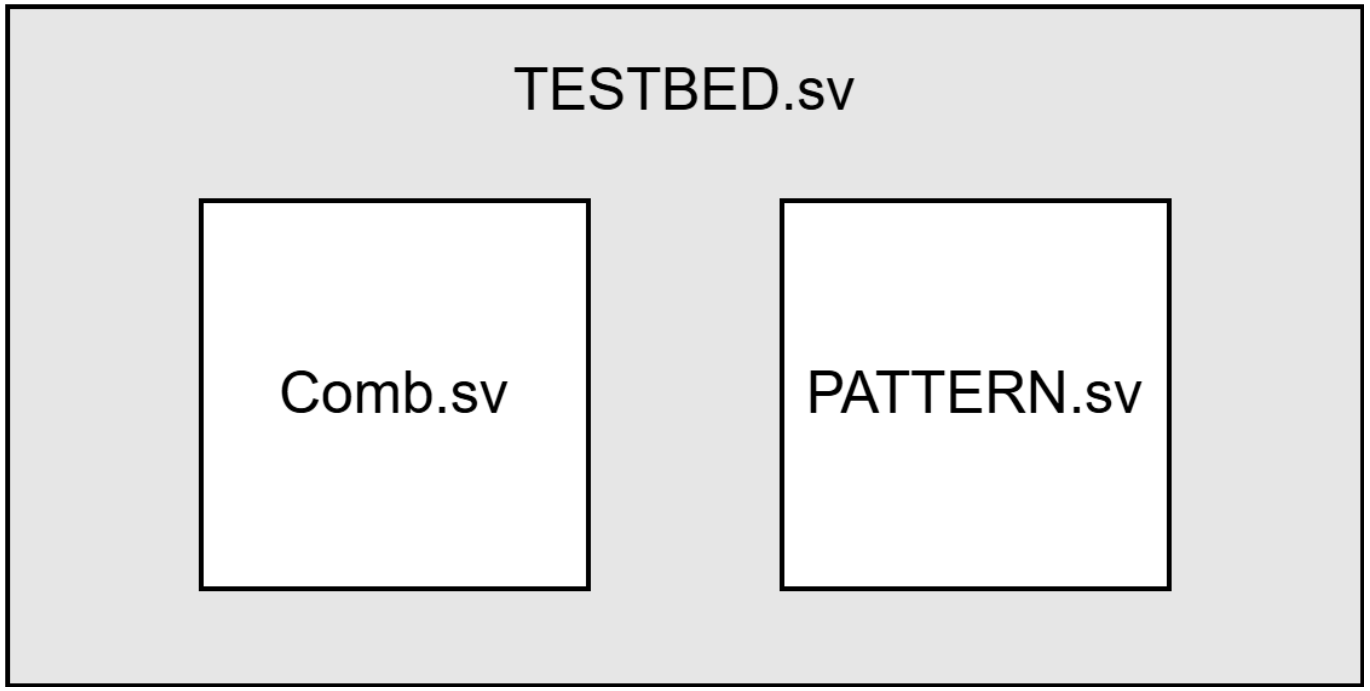
Block Diagram (Example)



Block Diagram (Example)



Block Diagram



Specification

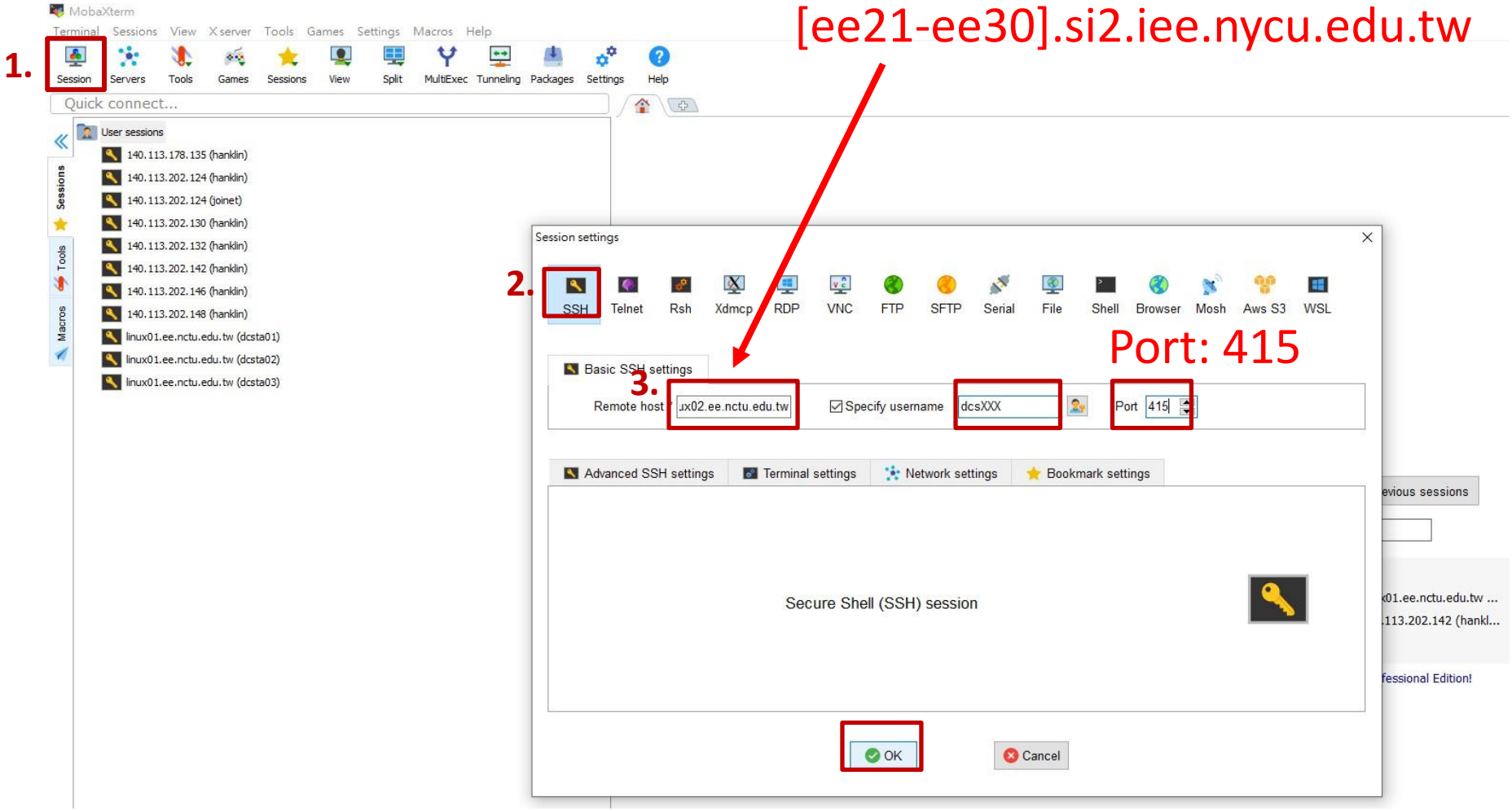
- Comb.sv

Input Signal	Bit Width	Definition
in_num0	7	Random 7-bit unsigned numbers
in_num1	7	
in_num2	7	
in_num3	7	

Output Signal	Bit Width	Definition
out_num0	8	max(A, B) + max(C, D)
out_num1	8	The gray code of min(A, B) + min(C, D)

MobaXterm

- Create New Session



Change Password

- Change password: passwd

```
+-------------------------------------------------------------------------+
|          CAD tools available on this machine (2022.03.13 updated)       |
+-------------------------------------------------------------------------+
| Cell-Based Design  |        Synopsys          |        Cadence          |
+-------------------------------------------------------------------------+
| Simulation         | VCS_2020.12(vcs)         | XCELIUM_20.09(xrun)     |
|                    | VERDI_2020.12(nWave)     | INCISIV_15.20(irun)     |
| Synthesis          | DC_2020.09(dc_shell)     | GENUS_20.10(genus)      |
| Physical Design    | ICC2_2020.09(icc2_shell) | INNOVUS_20.15(innovus)  |
| STA / Power        | PT_2019.03(pt_shell)     |                         |
| Formal             |                          | JG_2021.03(jg)          |
+-------------------------------------------------------------------------+
| Full-Custom Design |        Synopsys          |        Cadence          |
+-------------------------------------------------------------------------+
| Simulation         | HSP_2020.03(hspice)      |                         |
|                    | CEX_2020.12(cx,wv)       |                         |
| Layout             | LAKER_2021.03(laker)     | IC_06.17(virtuoso)      |
+-------------------------------------------------------------------------+
| Others             | Siemens  Calibre                                   |
|                    | Synopsys MetaWare Development Toolkit              |
|                    | Synopsys Tetra Max                                 |
|                    | Python3.6                                          |
+-------------------------------------------------------------------------+
| License Server     | 1717@lshc:5280@lshc:26585@lshc                     |
+-------------------------------------------------------------------------+
| Useful Command:                                                         |
| 1. quota -us [username] --> check out your quota                        |
| 2. passwd               --> change your password                        |
| 3. htop                 --> check out server usage                      |
| 4. scheck               --> check available server usage                |
+-------------------------------------------------------------------------+
linux01 [dcs/dcs240]% passwd
Changing NIS account information for dcs240 on raid.
Please enter old password:
```

Command

- tar -xvf ~dcsTA01/Lab01.tar
- cd Lab01/01_RTL/

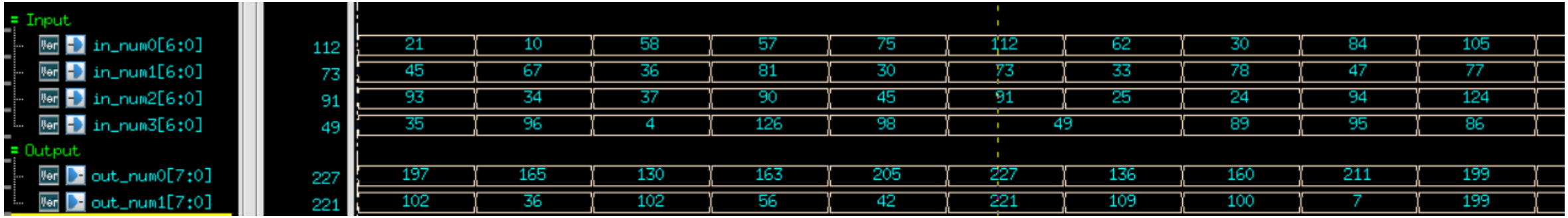
- vim Comb.sv (text editor)
  - i (輸入模式)
  - [Esc] (退回普通模式)
  - :w (儲存)
  - :q (結束)
- gedit Comb.sv (text editor)
  - view →Highlight Mode →Sources→Verilog
  - If you use Windows/MacOS, you can use Notepad++, or any editors you are used to using.

Directory

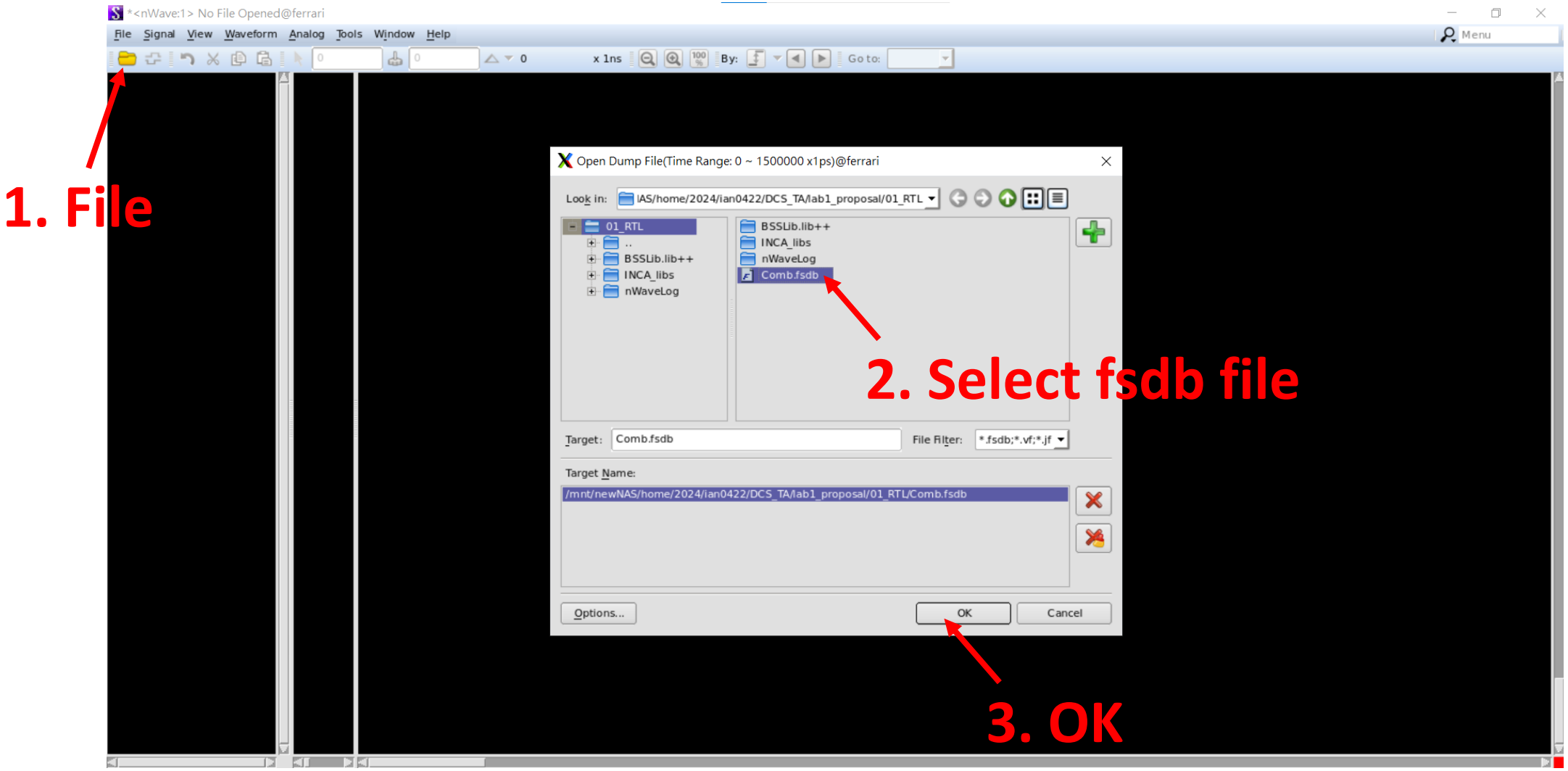
- 00_TESTBED
  - TESTBED.sv
  - PATTERN.sv
- 01_RTL
  - 01_run
  - 09_clean_up
  - Comb.sv
- 02_SYN
  - 01_run_dc
  - 09_clean_up
- 03_GATE
  - 01_run
  - 09_clean_up

RTL Simulation

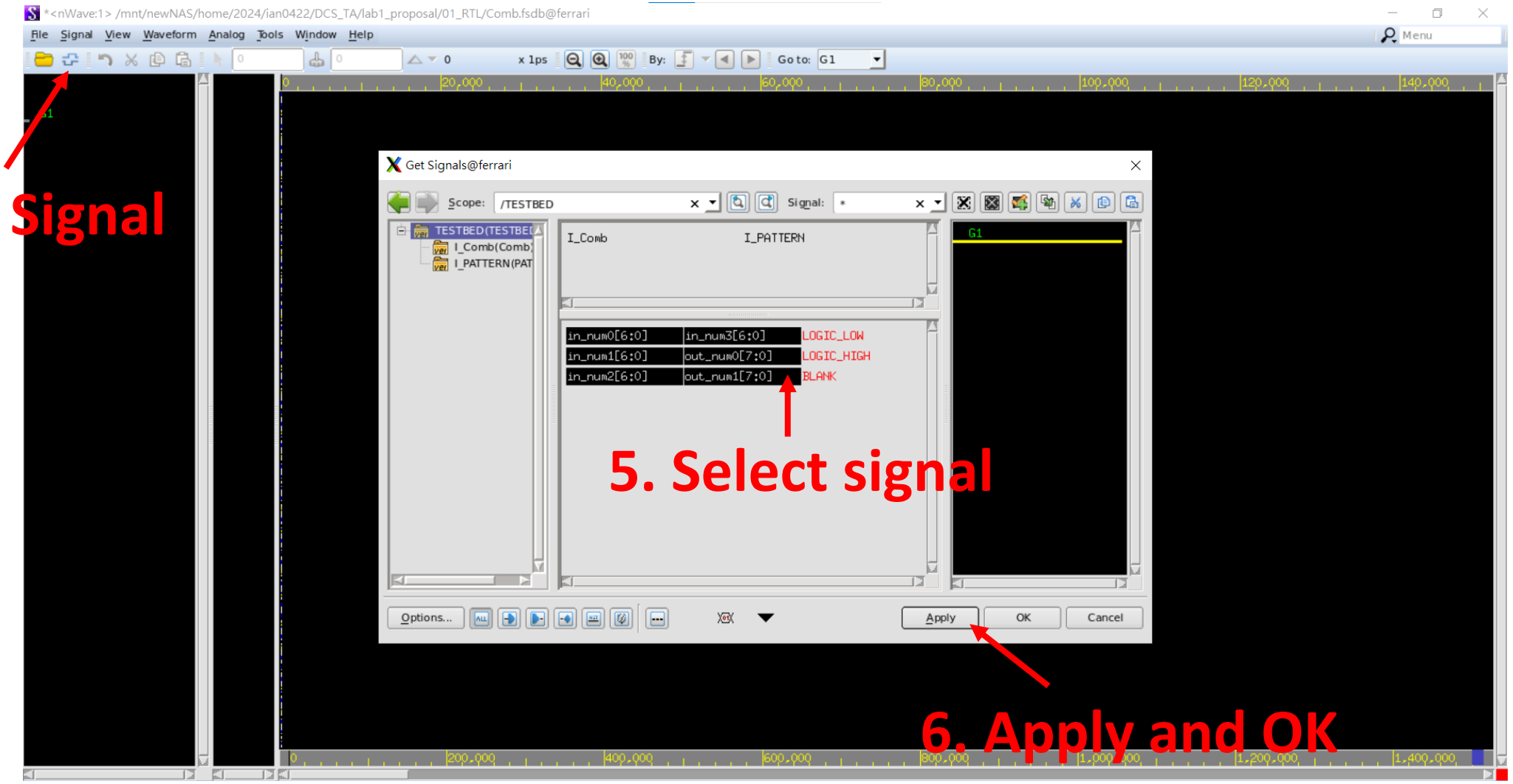
- cd Lab01/01_RTL/
- ./01_run (電路模擬)
- ./09_clean_up (清除波型檔)
- nWave & (看波型)
  - 範例波型



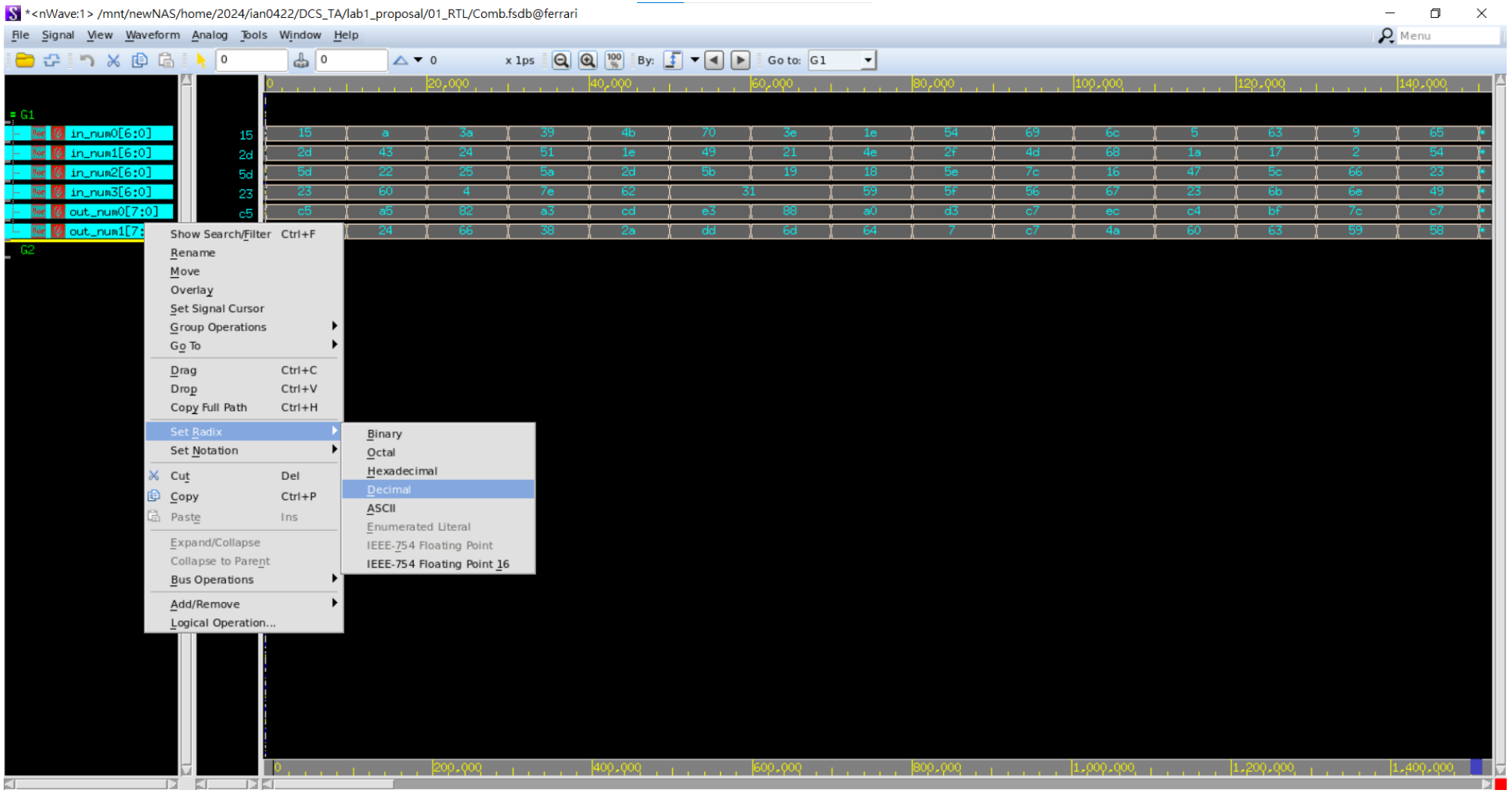
nWave


*<nWave:1> No File Opened@ferrari
File Signal View Waveform Analog Tools Window Help
Menu
x 1ns
By:
Go to:
1. File
Open Dump File(Time Range: 0 ~ 1500000 x1ps)@ferrari
Look in:
/AS/home/2024/ian0422/DCS_TA/lab1_proposal/01_RTL
01_RTL
..
BSSLib.lib++
INCA_libs
nWaveLog
BSSLib.lib++
INCA_libs
nWaveLog
Comb.fsdb
2. Select fsdb file
Target:
Comb.fsdb
File Filter:
.fsdb;.vf;*.jf
Target Name:
/mnt/newNAS/home/2024/ian0422/DCS_TA/lab1_proposal/01_RTL/Comb.fsdb
Options...
OK
Cancel
3. OK

nWave


4. Signal
5. Select signal
6. Apply and OK
Get Signals@ferrari
Scope: /TESTBED
Signal:
I_Comb
I_PATTERN
in_num0[6:0]
in_num1[6:0]
in_num2[6:0]
in_num3[6:0]
out_num0[7:0]
out_num1[7:0]
LOGIC_LOW
LOGIC_HIGH
BLANK
Options...
Apply
OK
Cancel

nWave (change radix)



Synthesis

- cd ../02_SYN/
- ./01_run_dc (電路合成)
- ./09_clean_up (清除合成結果)
  - 合成結果: (不能有Error、要有Area report、Timing report slack met、不能有Latch)

```
Number of ports:                          44
Number of nets:                          162
Number of cells:                         122
Number of combinational cells:           122
Number of sequential cells:                0
Number of macros/black boxes:              0
Number of buf/inv:                        25
Number of references:                     25

Combinational area:             151.955997
Buf/Inv area:                    11.340000
Noncombinational area:            0.000000
Macro/Black Box area:             0.000000
Net Interconnect area:            0.000000

Total cell area:                151.955997
Total area:                     151.955997
```

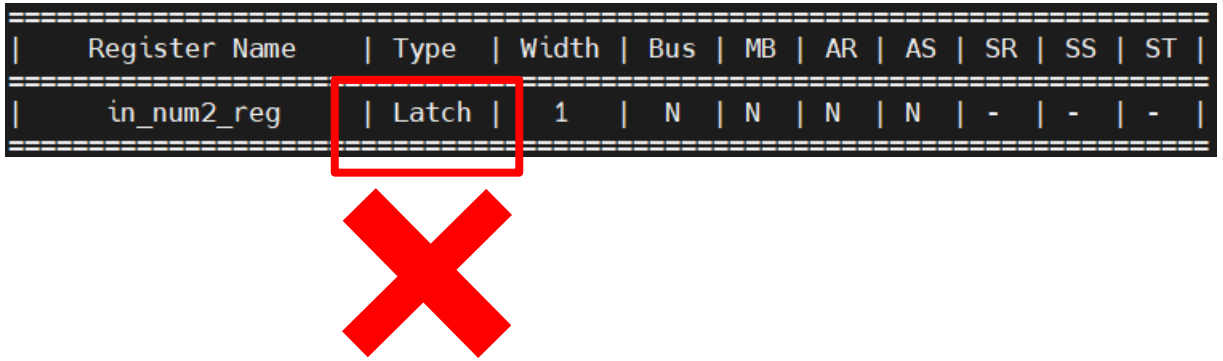
Synthesis

- 合成的timing report中的slack必須≧0 (MET)
- 如果出現timing violation → Demo Fail ! (slack < 0)

Point	Incr	Path
input external delay	0.00	0.00 r
in_num0[3] (in)	0.00	0.00 r
U196/Y (INV_X0P5B_A9TR)	0.03	0.03 f
U134/Y (OAI22BB_X0P5M_A9TR)	0.10	0.13 f
U199/Y (INV_X0P5B_A9TR)	0.05	0.19 r
U127/Y (OAI22_X0P5M_A9TR)	0.04	0.23 f
U172/Y (OA21A1OI2_X0P5M_A9TR)	0.08	0.31 r
U201/Y (INV_X0P5B_A9TR)	0.04	0.35 f
U123/Y (AOI22_X0P5M_A9TR)	0.05	0.40 r
U202/Y (AO21A1AI2_X1M_A9TR)	0.14	0.55 f
U175/Y (INV_X0P5B_A9TR)	0.25	0.80 r
U113/Y (NOR2_X0P7M_A9TR)	0.06	0.86 f
U173/Y (OA21A1OI2_X0P5M_A9TR)	0.12	0.98 r
U106/Y (NOR2_X0P7M_A9TR)	0.08	1.06 f
intadd_0_U7/CO (ADDF_X1M_A9TR)	0.07	1.13 f
intadd_0_U6/CO (ADDF_X1M_A9TR)	0.05	1.19 f
intadd_0_U5/CO (ADDF_X1M_A9TR)	0.05	1.24 f
intadd_0_U4/CO (ADDF_X1M_A9TR)	0.05	1.29 f
intadd_0_U3/CO (ADDF_X1M_A9TR)	0.05	1.35 f
intadd_0_U2/S (ADDF_X1M_A9TR)	0.07	1.42 r
U214/Y (XOR2_X0P5M_A9TR)	0.04	1.46 r
out_num1[5] (out)	0.00	1.46 r
data arrival time		1.46
max_delay	10.00	10.00
output external delay	0.00	10.00
data required time		10.00
data required time		10.00
data arrival time		-1.46
slack (MET)		8.54

Synthesis

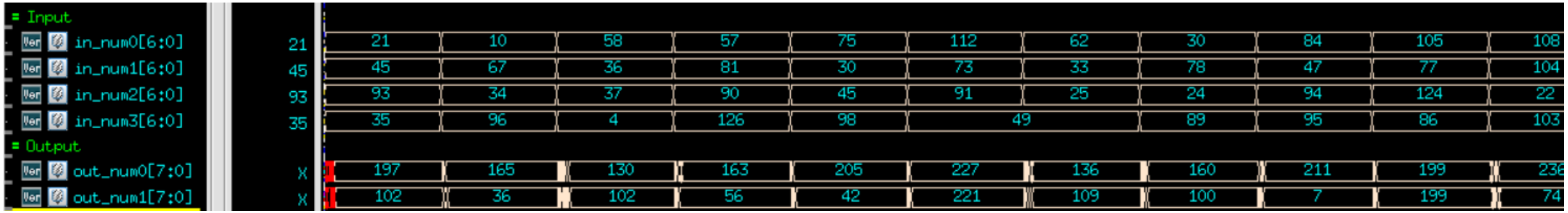
- 記得檢查是否合成出Latch和error
  - 可以在syn.log用ctrl+F尋找關鍵字Latch、error
- 如果出現Latch 、error → Demo Fail



Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST
in_num2_reg	Latch	1	N	N	N	N	-	-	-

Gate-Level Simulation

- cd ../03_GATE/
- ./01_run (電路模擬)
- ./09_clean_up (清除波型檔)
- nWave& (看波型)
  - 範例波形



Grading Policy

- Pass the RTL & Synthesis & Gate-level simulation: 100%
  - 合成結果: (**不能有Error、Timing report slack met、不能有Latch**)
- Demo2 打7折

Upload

- 請將Lab01/01_RTL裡的Comb.sv依以下命名規則重新命名後上傳至E3
- 命名規則：Comb_dcsxxx.sv，xxx為工作站帳號號碼
- **命名錯誤扣5分!!!**
- **Deadline:**
  - **Demo 1: 3/5 17:25**
  - **Demo 2: 3/5 23:59**