2025 DCS Lab10

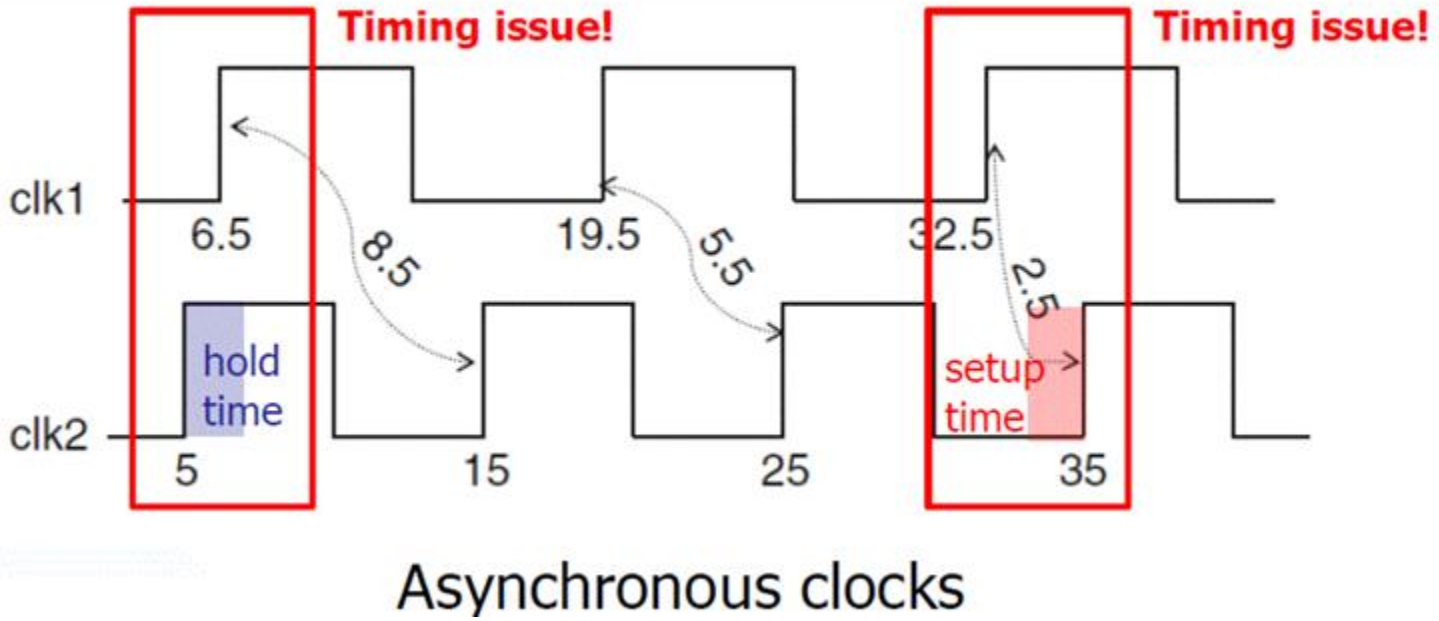
Clock Domain Crossing(CDC)

Purpose

- Learn how to design a Clock Domain Crossing (CDC) circuit in Verilog.
- Handshake synchronizer

Clock Domain Crossing (CDC)

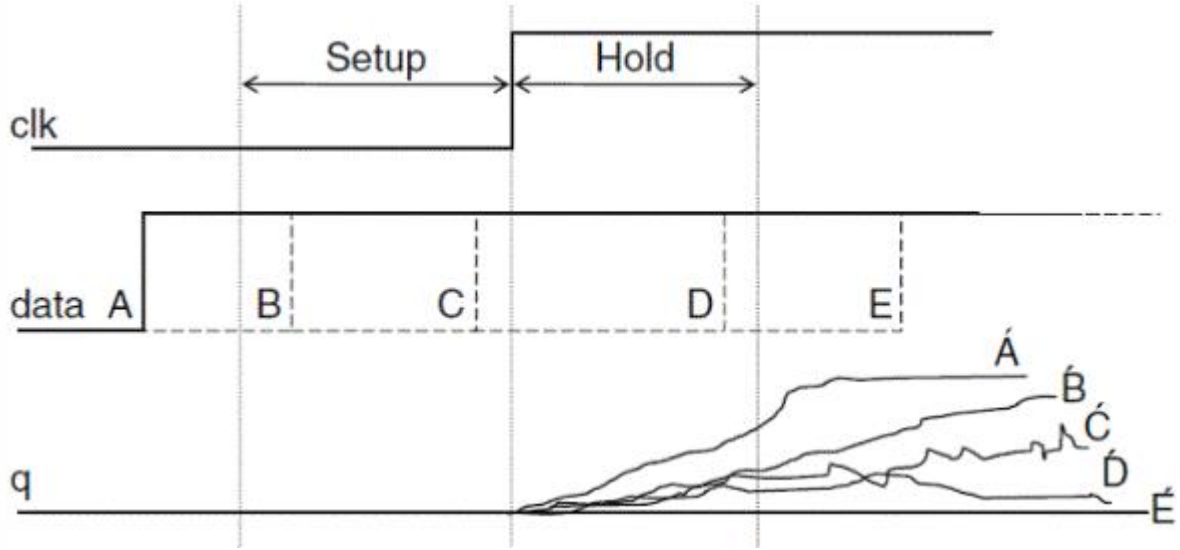
- CDC: When the data launched and captured by different (asynchronous) clock domain, this case is called Clock Domain Crossing.
- Consider two clocks, clk1 and clk2, with periods 13 and 10 respectively.



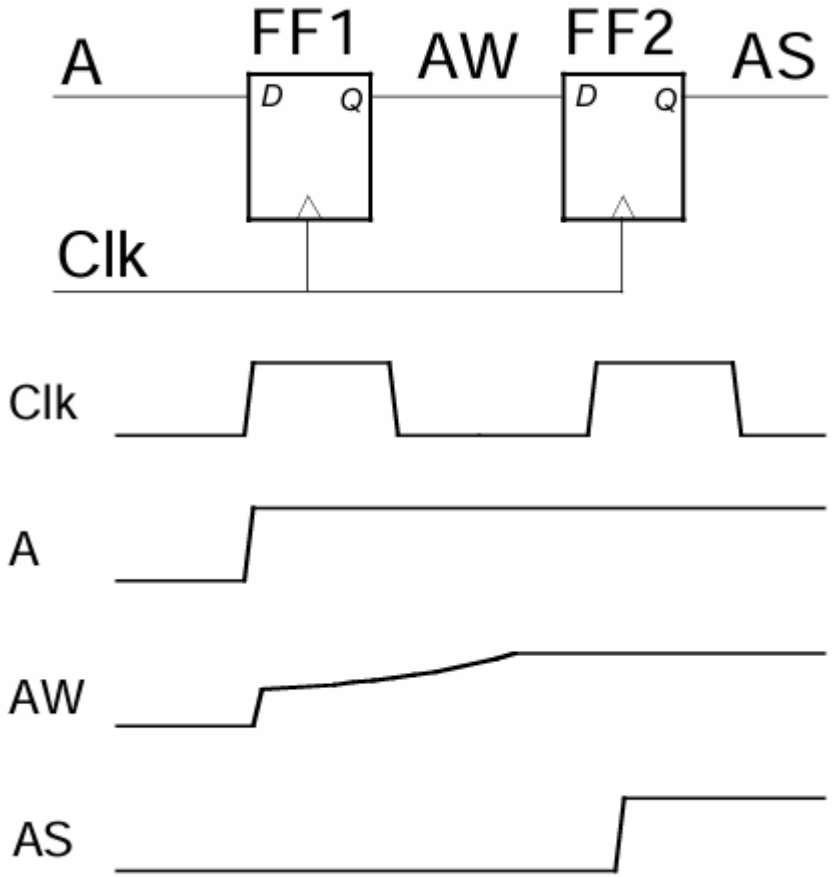
Asynchronous clocks

Metastability

- The unstable status due to non-ideal data transition is called metastability.
- To avoid this phenomenon, we have to ensure that data should be stable during setup/hold timing check.
- However, CDC designs will inevitably face this problem.



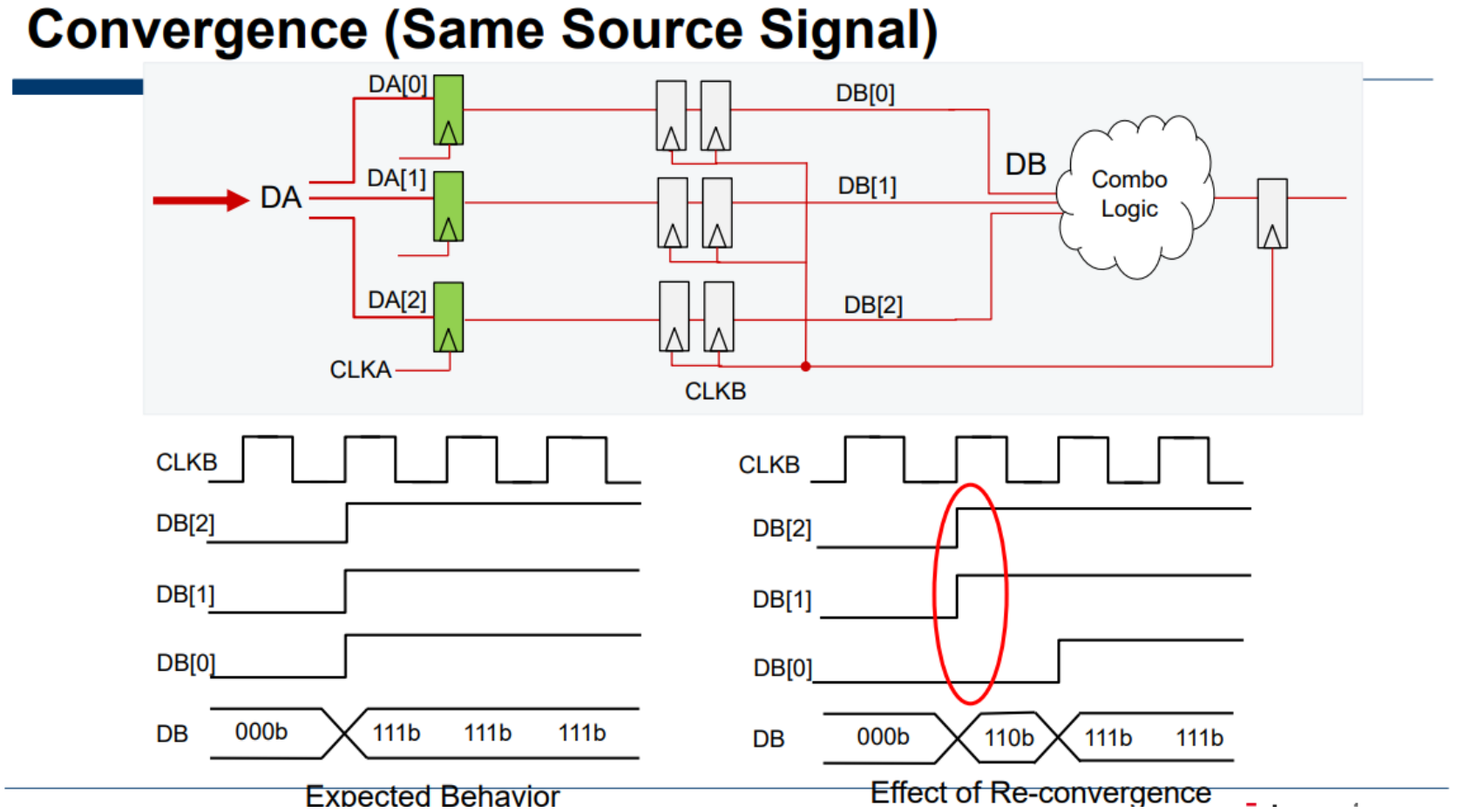
Solution: A Brute-Force Synchronizer



細節請參考: 上課講義 Lecture 12

Convergence issue

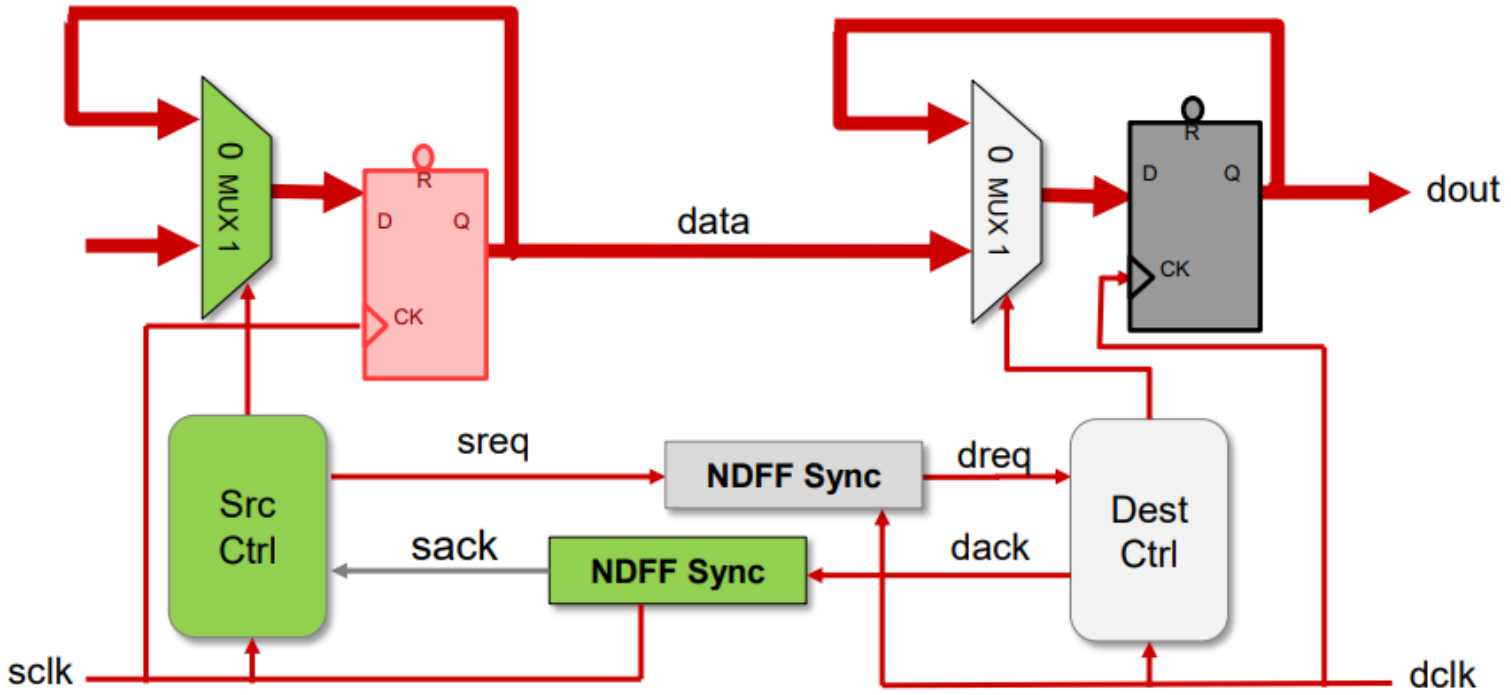
- 在傳送multi-bit時無法保證每個bit都同時抵達



Source: 2023 Fall iclab Lec07 (Jasper_CDC_introduction_lhlai)

Handshake synchronizer

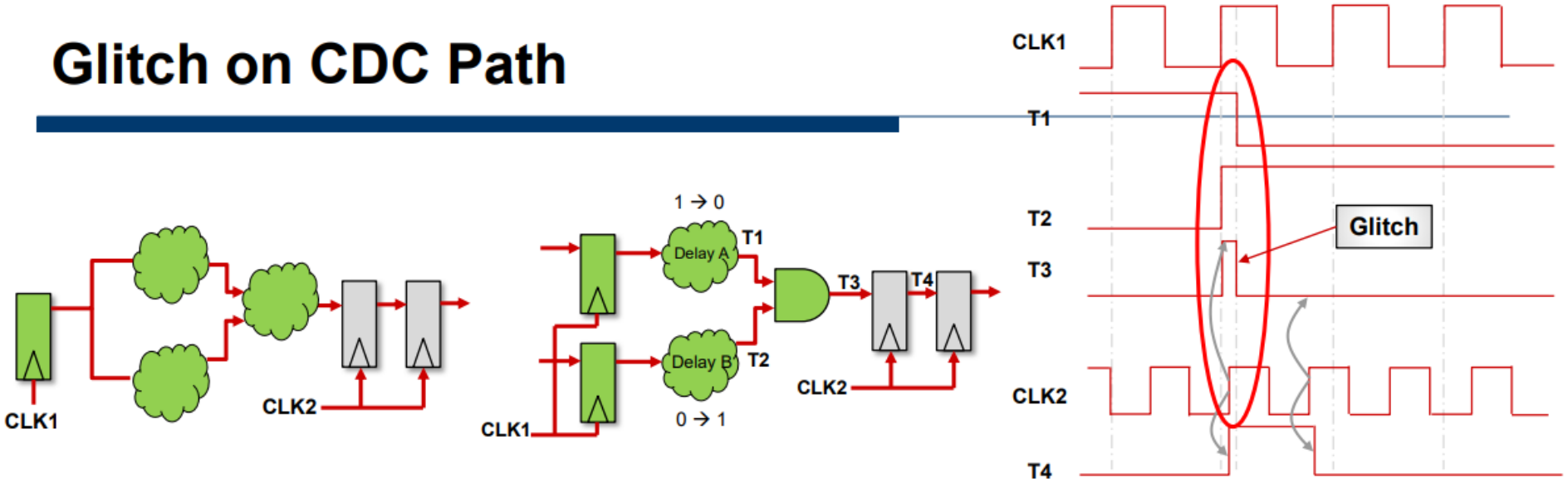
- Request-acknowledge protocol
- High latency



Source: 2023 Fall iclab Lec07 (Jasper_CDC_introduction_lhlai)

Glitch on CDC Path

- 只讓DFF的output通過synchronizer，中間不要經過combinational運算，否則可能有glitch

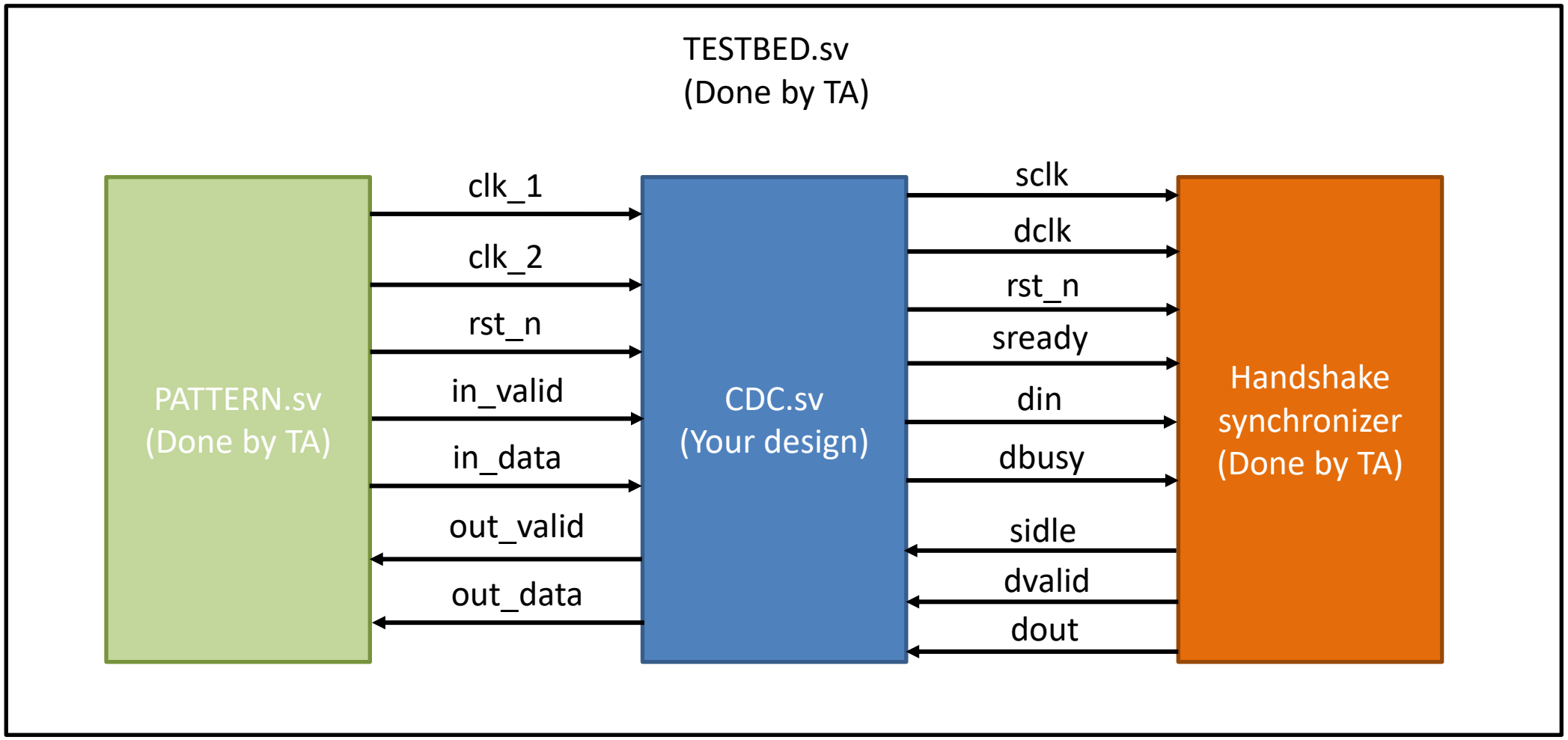


Source: 2023 Fall iclab Lec07 (Jasper_CDC_introduction_lhlai)

Design

- clk_1 = 14.1ns, clk_2 = 2.5ns
- Input在clk_1 domain傳送
  - 包含1 bit control signal (in_valid)和4 bit data signal (in_data)，一次連續傳兩筆
- 將這4 bit的data經由Handshake synchronizer傳送到clk_2 domain
- 在clk_2 domain接受Handshake synchronizer傳過來的資料並計算輸出
  - 計算 data 1 + data 2並輸出

Block diagram



CDC.sv

- Design and PATTERN

Input signal	Bit width	Definition
clk_1	1	clk_1 domain 14.1ns
clk_2	1	clk_2 domain 2.5ns
rst_n	1	Asynchronous active-low reset
in_valid	1	在clk_1 domain，此訊號拉起時給in_data
in_data	4	在clk_1 domain，當in_valid為1時給予資料，一次連續給兩筆

Output signal	Bit width	Definition
out_valid	1	在clk_2 domain，當out_valid為1時檢查out_data，必須為一個cycle，不能多也不能少 必須在300個clk_2 cycle內拉起out_valid
out_data	5	在clk_2 domain，輸出in_data 1 + in_data 2的結果

CDC.sv

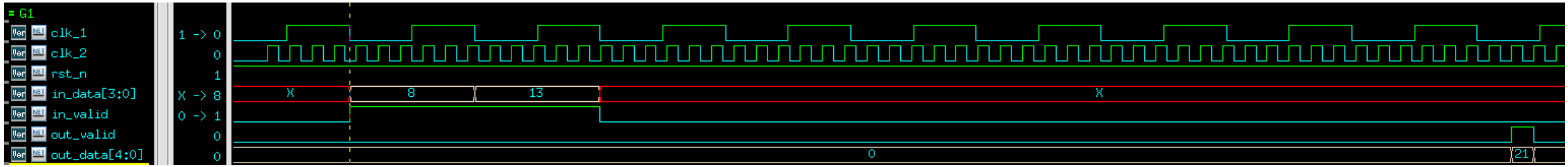
- Design and Handshake_syn.sv

Output signal	Bit width	Definition
sclk	1	Source clock (clk_1)
dclk	1	Destination clock (clk_2)
rst_n	1	Asynchronous active-low reset
sready	1	當design傳送資料(din)給synchronizer時拉起 (類似給in_valid)
din	4	要給synchronizer的資料 (PATTERN給的4 bit data)
dbusy	1	告訴synchronizer現在design是否可以接收來自synchronizer的資料 (hint: 這次Lab可以直接設成0會比較簡單)

Input signal	Bit width	Definition
sidle	1	告訴design現在synchronizer是否可以接受來自design的資料
dvalid	1	Synchronizer告訴design現在的資料是合法的 (類似給in_valid)
dout	4	Synchronizer的資料輸出，由design接收後計算

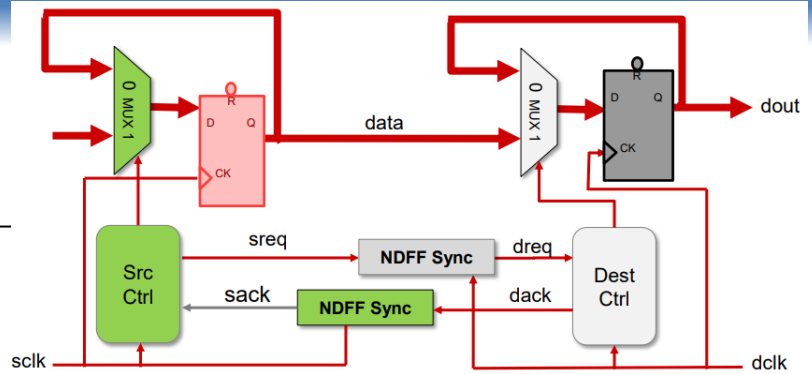
Waveform

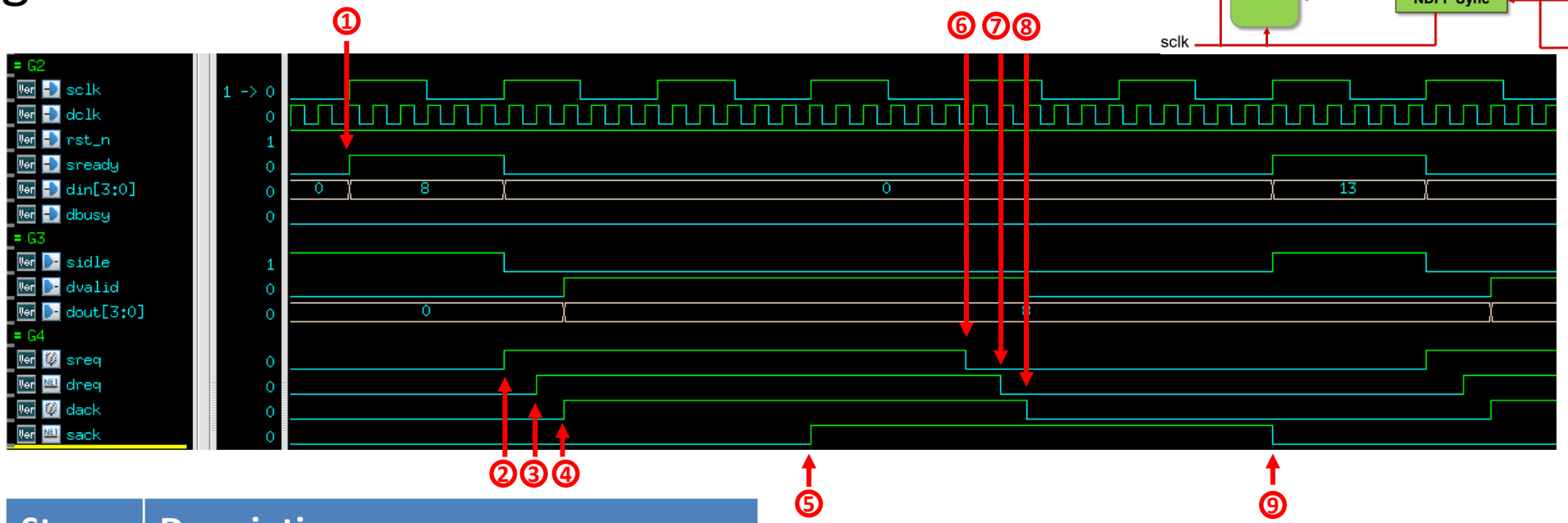
- Design and PATTERN



Waveform

- Design and Handshake



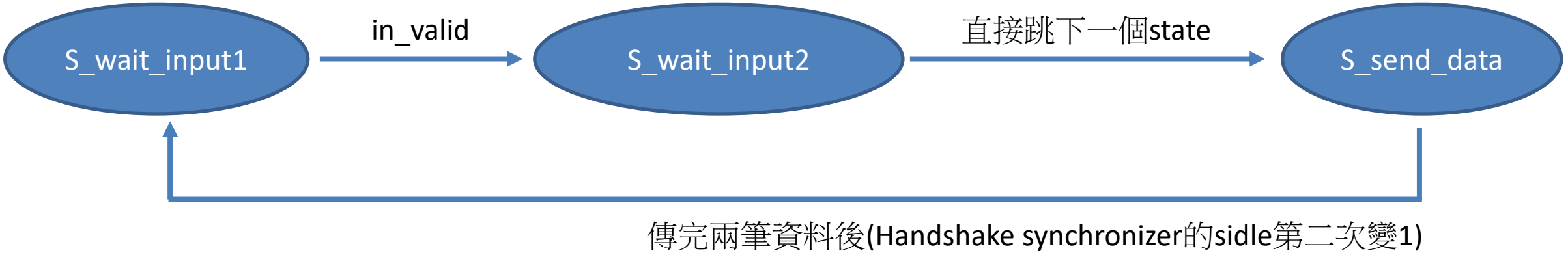


Stage	Description
1	din送一筆data給synchronizer
2	sreq拉為1
3	數個clk_2 cycle後dreq拉為1
4	下個clk_2 cycle後dack拉為1
5	數個clk_1 cycle後sack拉為1

Stage	Description
6	下個clk_1 cycle後sreq拉為0
7	數個clk_2 cycle後dreq拉為0
8	下個clk_2 cycle後dack拉為0
9	數個clk_1 cycle後sack拉為0

Reference FSM

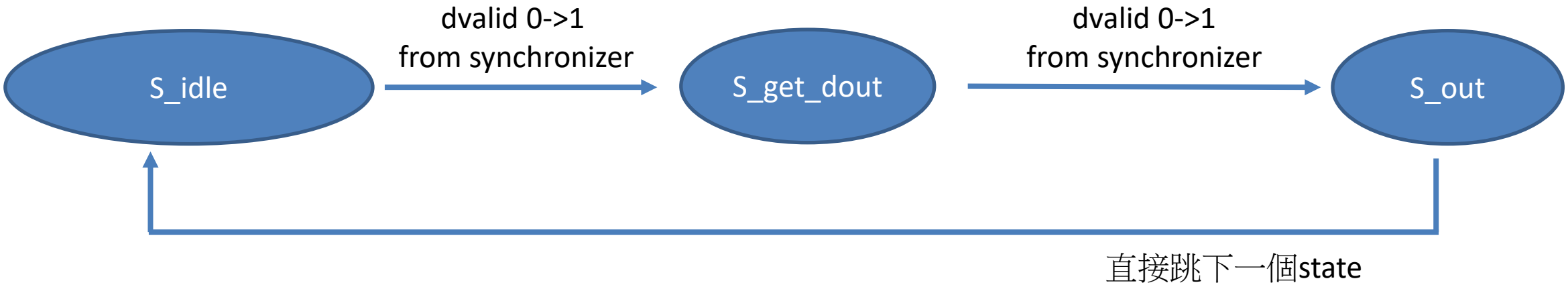
- clk_1 domain



State	description
S_wait_input1	等待PATTERN的in_valid及in_data
S_wait_input2	讀進第二筆in_data
S_send_data	將兩筆in_data送給synchronizer，一次只能送一筆，且需等待sidle為1才能送

Reference FSM

- clk_2 domain



State	description
S_idle	等待synchronizer的第一筆dvalid及dout (dvalid為1時, dout才是有效的資料)
S_get_dout	等待synchronizer的第二筆dvalid及dout
S_out	計算並輸出兩筆dout相加的結果

Spec

- 請勿更改Handshake_syn.sv及NDFF_syn.sv，僅須完成CDC.sv即可
- 請使用Handshake_syn完成這次Lab
- 所有output必須非同步準位reset
- 01_RTL必須PASS
- 02_SYN不能有error跟latch
- 02_SYN timing slack必須為MET
- 03_GATE必須PASS且沒有timing violation

Note for 01_RTL

- 如果跑01_run看到這個紅色的提示不用慌張，只是include檔案而已

```
15:23 dcs180@ee31[~/Lab10/01_RTL]$ ./01_run
irun(64): 15.20-s084: (c) Copyright 1995-2020 Cadence Design Systems, Inc.
ncvlog: *W,NOTIND: unable to access -INCDIR /usr/synthesis/dw/sim_ver (No such file or directory).
file: TESTBED.sv
`ifdef RTL
|
ncvlog: *W,NONPRT (PATTERN.sv,1|0): non-printable character (0xef) ignored.
(`include file: PATTERN.sv line 1, file: TESTBED.sv line 2)
`ifdef RTL
 |
ncvlog: *W,NONPRT (PATTERN.sv,1|1): non-printable character (0xbb) ignored.
(`include file: PATTERN.sv line 1, file: TESTBED.sv line 2)
`ifdef RTL
  |
ncvlog: *W,NONPRT (PATTERN.sv,1|2): non-printable character (0xbf) ignored.
(`include file: PATTERN.sv line 1, file: TESTBED.sv line 2)
        module worklib.NDFF_syn:v
                errors: 0, warnings: 0
        module worklib.Handshake_syn:v
                errors: 0, warnings: 0
        module worklib.CDC:sv
                errors: 0, warnings: 0
        module worklib.PATTERN:sv
                errors: 0, warnings: 0
module NDFF_syn(D, Q, clk, rst_n);
               |
ncvlog: *W,RECOME (./NDFF_syn.v,2|14): recompiling design unit worklib.NDFF_syn:v.
        First compiled from line 2 of NDFF_syn.v.
(`include file: ./NDFF_syn.v line 2, `include file: ./Handshake_syn.v line 2, `include file: ./CDC.sv line 2, file: TESTBED.sv line 5)
module Handshake_syn #(parameter WIDTH=4) (
                      |
ncvlog: *W,RECOME (./Handshake_syn.v,3|19): recompiling design unit worklib.Handshake_syn:v.
        First compiled from line 3 of Handshake_syn.v.
(`include file: ./Handshake_syn.v line 3, `include file: ./CDC.sv line 2, file: TESTBED.sv line 5)
module CDC(
        |
ncvlog: *W,RECOME (./CDC.sv,4|9): recompiling design unit worklib.CDC:sv.
        First compiled from line 4 of CDC.sv.
(`include file: ./CDC.sv line 4, file: TESTBED.sv line 5)
        module worklib.TESTBED:sv
                errors: 0, warnings: 0
        Total errors/warnings found outside modules and primitives:
                errors: 0, warnings: 4
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
        Top level design units:
                TESTBED
ncelab: *W,DSEMEL: This SystemVerilog design will be simulated as per IEEE 1800-2009 SystemVerilog simulation semantics. Use -disable_sem2009 option for turning off SV 2009 simulation semantic
s.
        Building instance overlay tables: .................... Done
        Generating native compiled code:
                worklib.CDC:sv <0x0fb04973>
                        streams:  30, words: 10761
                worklib.Handshake_syn:v <0x62e29649>
                        streams:  13, words:  3750
```

Command

- tar -xvf ~dcsTA01/Lab10.tar

Grading Policy

- Pass the RTL & Synthesis & Gate-level simulation: 100%
  - 合成結果: (**不能有Error、Timing report slack met、不能有Latch**)
  - Gate-level simulation**不可以發生timing violation**
- Demo 2 打7折

```
Warning!  Timing violation
          $hold( posedge RN:119954 FS, posedge SN:204217 FS,  0.229292 : 229292 FS );
           File: /usr/cad/umc018/Verilog/umc18_neg.v, line = 9379
          Scope: TESTBED.I_Seq.lose_reg
           Time: 204217 FS
```

Upload

- 請將Lab10/01_RTL裡的CDC.sv依以下命名規則重新命名後上傳至E3
- 命名規則：CDC_dcsxxx.sv，xxx為工作站帳號號碼
- **命名錯誤扣5分!!!**
- **Deadline:**
  - **Demo 1: 5/15 17:25**
  - **Demo 2: 5/15 23:59**