Lab02
Counter

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Purpose

- Be familiar with Verilog syntax
  - Avoid multiple-driven
  - Separate sequential and combinational block
- Be familiar with circuit specification
  - Output data should be strictly **RESET** !!!
- Sequential circuit
- Counter

Sequential Circuit

- Different from combinational circuit, sequential circuit will synthesize registers which can store previous data.

O

```
always @(posedge clk or negedge rst_n) begin
    if(!rst_n)
        a <= 0;
    else
        a <= a + 1;
end
```

← Sequential circuit

X

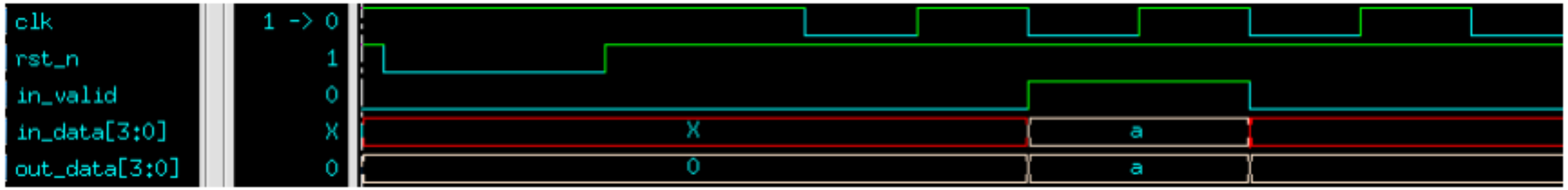
```
assign a = a + 1;

always @(*) begin
  a = a + 1;
end

always @(*) begin
  if(a > b) a = b;
  else a = a;
end
```

← Combinational circuit

Waveform Difference

- Combinational Circuit

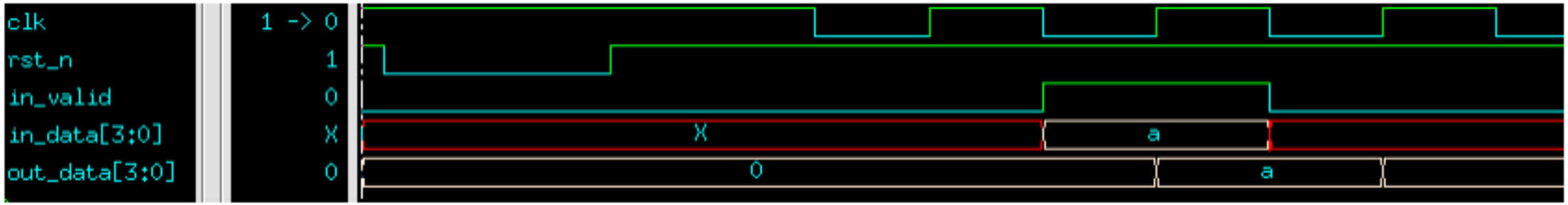
```
always@(*)begin
    if(in_valid) out_data = in_data;
    else out_data = 0;
end

assign out_data = (in_valid) ? in_data : 0;
```



Waveform Difference

- Sequential Circuit

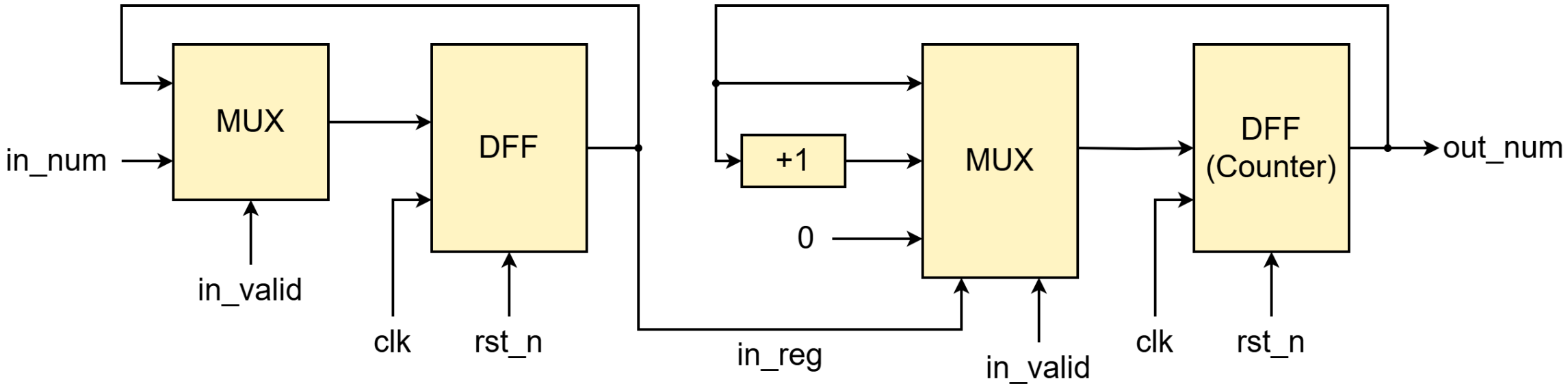
```
always@(posedge clk or negedge rst_n)begin
    if(!rst_n)
        out_data <= 0;
    else begin
        if(in_valid) out_data <= in_data;
        else out_data <= 0;
    end
end
```



Counter

- At the beginning, the pattern will send rst_n, you should reset out_num to 0
  - Reset when rst_n is low
- When the “in_valid” is high, the pattern will provide a number: in_num for counting
  - “in_valid” will be high for one cycle
  - The range of in_num is 1~31
- After receiving in_num, you should increment out_num from 0 to in_num over the following cycles
  - Once counting is finished, you should hold out_num (out_num = in_num) until the next pattern
- The next counting pattern will arrive in 2~6 cycles

Reference Block Diagram



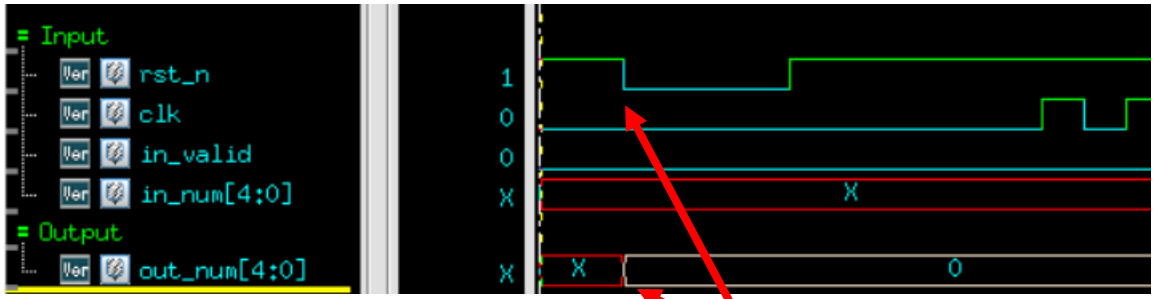
Specification

- Counter.sv

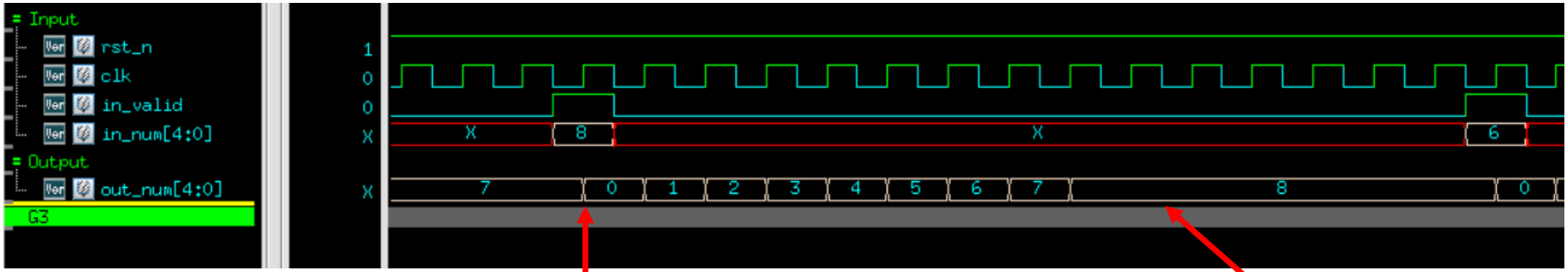
Input Signal	Bit Width	Definition
clk	1	Clock
rst_n	1	Asynchronous active-low reset
in_valid	1	High when input signal is ready
in_num	5	The number of cycles to count

Output Signal	Bit Width	Definition
out_num	5	Count from 0 to in_num after input, then hold out_num until next pattern arrives

Output and Waveform



out_num should be reset to zero when rst_n is low



start counting after input is received

hold out_num until next pattern

Separate sequential and combinational block

```
always_ff @(posedge clk, negedge rst_n) begin
    if(!rst_n) Q <= 0;
    else Q <= Q_next;
end
assign Q_next = A + B;
```

Good design

```
always_ff @(posedge clk, negedge rst_n) begin
    if(!rst_n) Q <= 0;
    else Q <= A + B;
end
```

Bad design

Directory

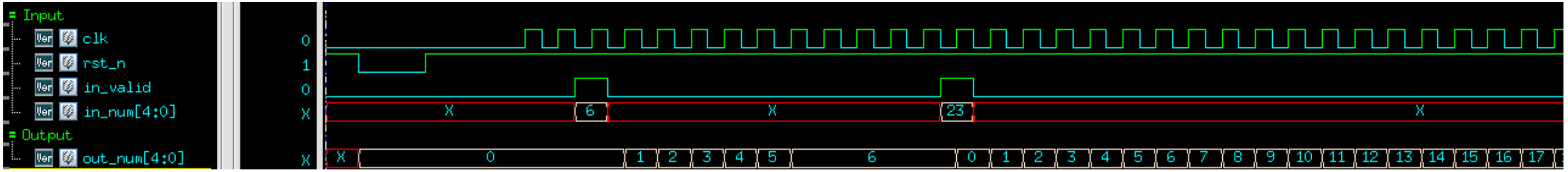
- 00_TESTBED
  - TESTBED.sv
  - PATTERN.sv
- 01_RTL
  - 01_run
  - 09_clean_up
  - Counter.sv
- 02_SYN
  - 01_run_dc
  - 09_clean_up
- 03_GATE
  - 01_run
  - 09_clean_up

Command

- tar -xvf ~dcsTA01/Lab02.tar
- cd Lab02/01_RTL/

RTL Simulation

- cd Lab02/01_RTL/
- ./01_run (電路模擬)
- ./09_clean_up (清除波型檔)
- nWave & (看波型)
  - 範例波型



Synthesis

- cd ../02_SYN/
- ./01_run_dc (電路合成)
- ./09_clean_up (清除合成結果)
  - 合成結果: (不能有Error、要有Area report、Timing report slack met、不能有Latch)

```
Number of ports:                           13
Number of nets:                            52
Number of cells:                           44
Number of combinational cells:             34
Number of sequential cells:                10
Number of macros/black boxes:               0
Number of buf/inv:                          8
Number of references:                      15

Combinational area:                31.298400
Buf/Inv area:                       3.628800
Noncombinational area:             45.359998
Macro/Black Box area:               0.000000
Net Interconnect area:              0.000000

Total cell area:                   76.658397
Total area:                        76.658397
```

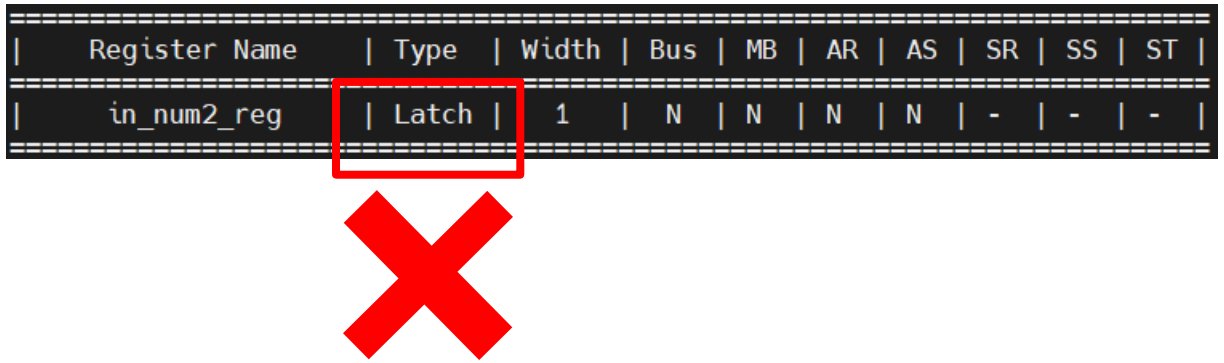
Synthesis

- 合成的timing report中的slack必須≧0 (MET)
- 如果出現timing violation → Demo Fail ! (slack < 0)

```
Point                                    Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                    0.00       0.00
clock network delay (ideal)              0.00       0.00
input external delay                     5.00       5.00 r
in_valid (in)                            0.00       5.00 r
U41/Y (INV_X0P5B_A9TR)                   0.06       5.06 f
U42/Y (NAND2_X0P5A_A9TR)                 0.10       5.16 r
U56/Y (NAND2_X0P5A_A9TR)                 0.09       5.24 f
U61/Y (NOR2_X0P5A_A9TR)                  0.10       5.35 r
U63/Y (OAI21_X0P5M_A9TR)                 0.05       5.40 f
U64/Y (OAI31_X0P5M_A9TR)                 0.07       5.47 r
out_num_reg_2_/D (DFFRPQ_X1M_A9TR)       0.00       5.47 r
data arrival time                                   5.47

clock clk (rise edge)                   10.00      10.00
clock network delay (ideal)              0.00      10.00
out_num_reg_2_/CK (DFFRPQ_X1M_A9TR)      0.00      10.00 r
library setup time                      -0.04       9.96
data required time                                  9.96
-----------------------------------------------------------
data required time                                  9.96
data arrival time                                  -5.47
-----------------------------------------------------------
slack (MET)                                         4.49
```

Synthesis

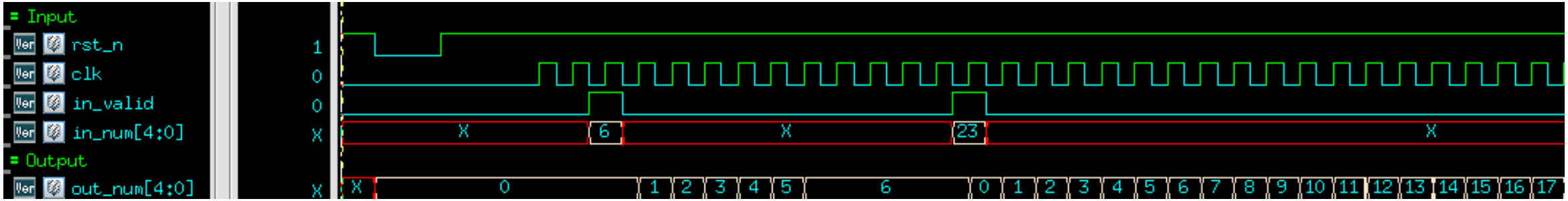
- 記得檢查是否合成出Latch和error
  - 可以在syn.log用ctrl+F尋找關鍵字Latch、error
- 如果出現Latch 、error → Demo Fail



Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST
in_num2_reg	Latch	1	N	N	N	N	-	-	-

Gate-Level Simulation

- cd ../03_GATE/
- ./01_run (電路模擬)
- ./09_clean_up (清除波型檔)
- nWave & (看波型)
  - 範例波形



Grading Policy

- Pass the RTL & Synthesis & Gate-level simulation: 100%
  - 合成結果: (**不能有Error、Timing report slack met、不能有Latch**)
- Demo2 打7折

Upload

- 請將Lab02/01_RTL裡的Counter.sv依以下命名規則重新命名後上傳至E3
- 命名規則：Counter_dcsxxx.sv，xxx為工作站帳號號碼
- **命名錯誤扣5分!!!**
- **Deadline:**
  - **Demo 1: 3/6 17:25**
  - **Demo 2: 3/6 23:59**