# DCS Lab 5
# Finite State Machine

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# Purpose

- Learn how to design a finite state machine (FSM) using Verilog.

# Lab05

- Run the command below to get files for this lab.
  - tar -xvf ~dcsTA01/Lab05.tar

# Branch

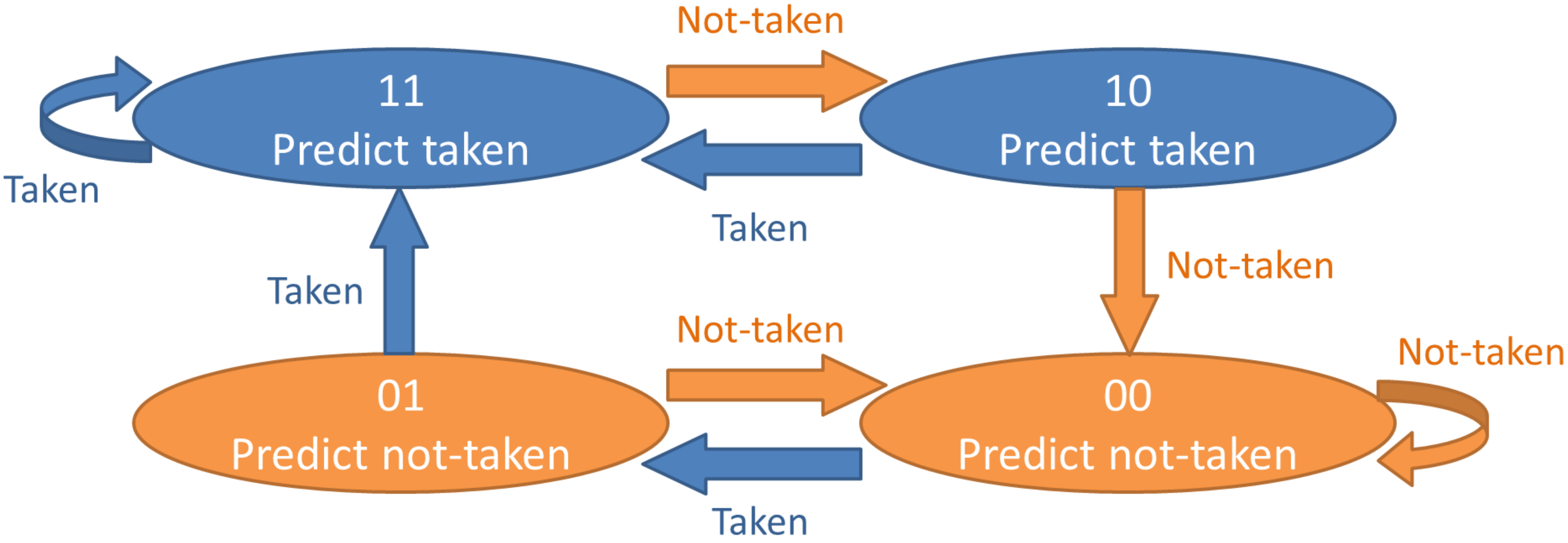
- Some common branch instruction in RISC-V ISA:

1. BEQ (Branch if Equal)
2. BNE (Branch if Not Equal)
3. BLT (Branch if Less Than)
4. BGE (Branch if Greater or Equal)

| Instruction | Branch taken | Branch not taken |
|---|---|---|
| BEQ A, B, dest | A == B | A != B |
| BNE A, B, dest | A != B | A == B |
| BLT A, B, dest | A < B | A >= B |
| BGE A, B, dest | A >= B | A < B |

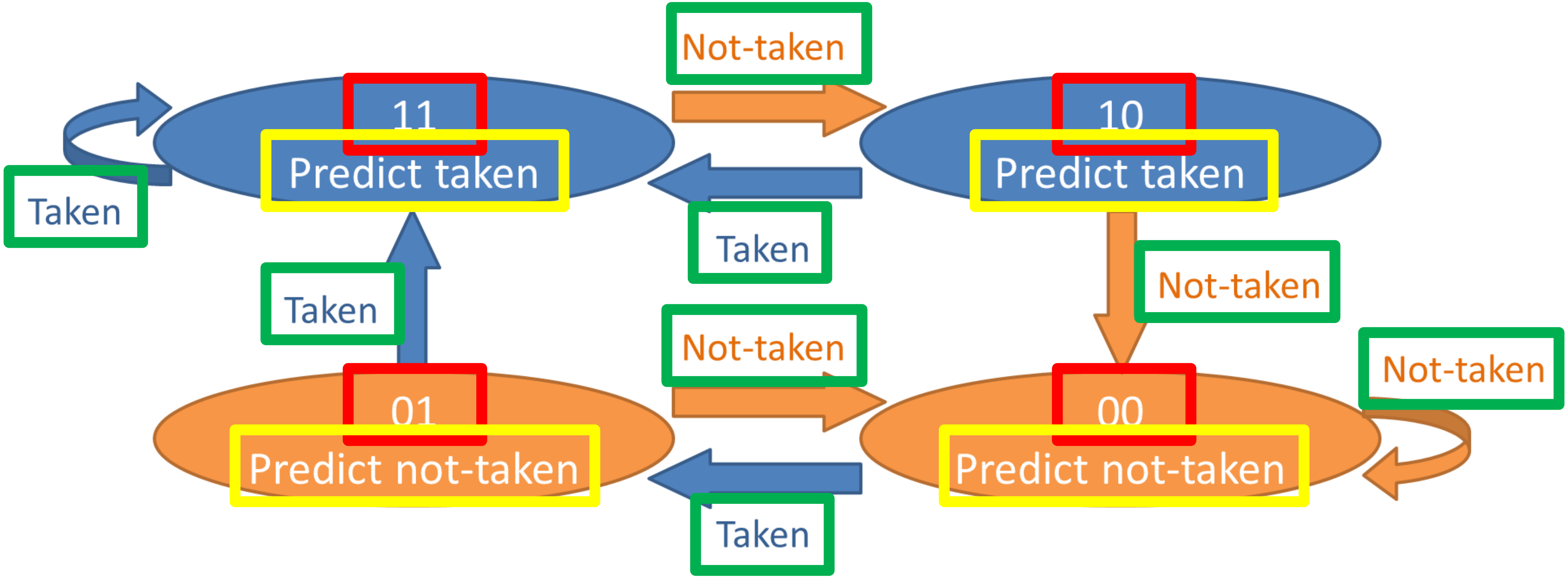
# Problem for This Lab: 2-bit Branch Predictor

- Predicting a branch is taken or not can speed up the execution.
- 2-bit branch predictor change its prediction if two misses occur.



# 2-bit Branch Predictor as a FSM

- State, output, condition (generated from inputs and current state)



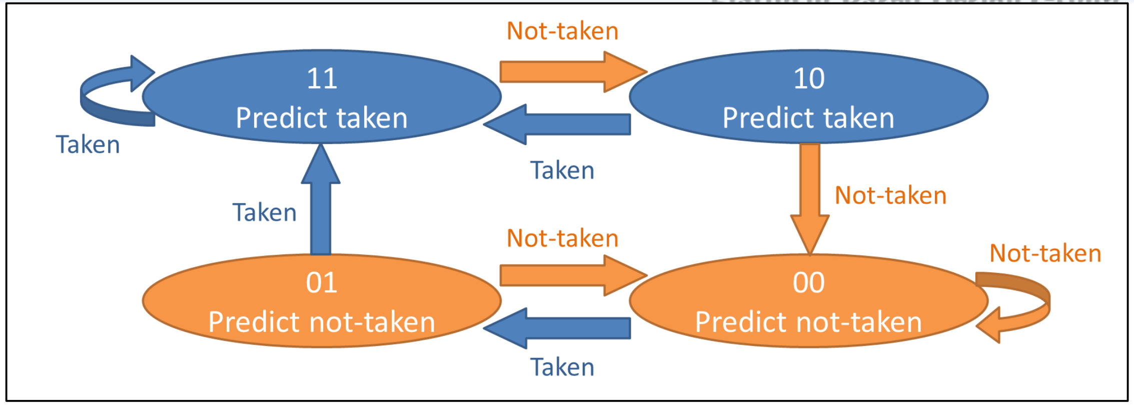
# FSM.sv

| Input Signal | Bit Width | Definition |
|---|---|---|
| clk | 1 | Clock. |
| rst_n | 1 | Asynchronous active-low reset. |
| in_valid | 1 | High when input is valid. |
| op | 2 | Type of branch instruction. **(BEQ=00, BNE=01, BLT=10, BGE=11)** |
| A | 4 | The first variable for branch instruction. |
| B | 4 | The second variable for branch instruction. |

| Output Signal | Bit Width | Definition |
|---|---|---|
| pred_taken | 1 | High when the prediction is taken.<br>Should be reset when rst_n is low. |
| state | 2 | Current state of your 2-bit predictor.<br>Should be reset when rst_n is low. |

# FSM.sv

| Instruction | Branch taken | Branch not taken |
|---|---|---|
| BEQ A, B, dest | A == B | A != B |
| BNE A, B, dest | A != B | A == B |
| BLT A, B, dest | A < B | A >= B |
| BGE A, B, dest | A >= B | A < B |



BEQ 9, 3

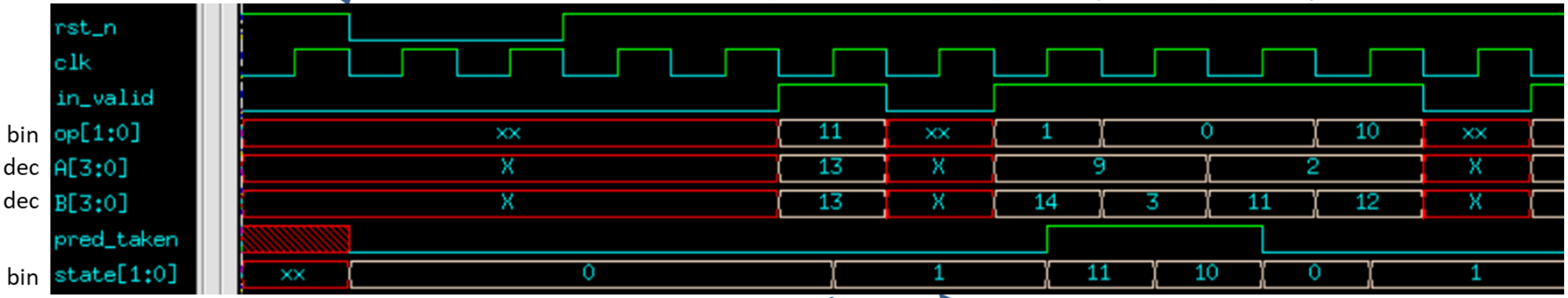
BLT 2, 12

All outputs should be reset when rst_n is low

BGE 13, 13

BNE 9, 14

BEQ 2, 11



Outputs should change at the posedge of clk if in_valid is high

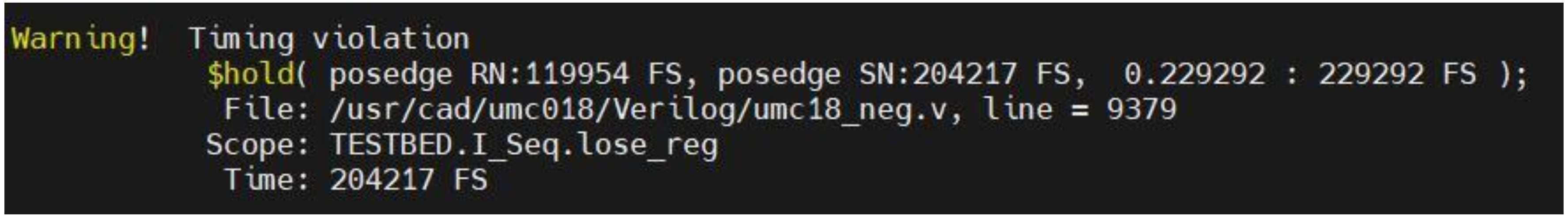
Outputs should NOT change if in_valid is low

# Reminder

1. **You must follow the state diagram in p.5.**
2. State should be reset to 2’b00 when rst_n is low. (And pred_taken should be low at the same time.)
3. Outputs should change at posedge of clk if in_valid is high. (unless the inputs don’t change the state.)
4. Both pred_taken and state should not change when in_valid is low.

# Grading Policy

- Pass the RTL & Synthesis & Gate-level simulation: 100%
  - 合成結果: (**不能有Error**、**Timing report slack met**、**不能有Latch**)
  - Gate-level simulation**不可以發生timing violation**
- Demo 2 打7折



```
Warning!  Timing violation
           $hold( posedge RN:119954 FS, posedge SN:204217 FS,  0.229292 : 229292 FS );
            File: /usr/cad/umc018/Verilog/umc18_neg.v, line = 9379
           Scope: TESTBED.I_Seq.lose_reg
            Time: 204217 FS
```

# Upload

- 請將Lab05/01_RTL裡的FSM.sv依以下命名規則重新命名後上傳至E3
- 命名規則：FSM_dcsxxx.sv，xxx為工作站帳號號碼
- **命名錯誤扣5分!!!**
- **Deadline:**
  - **Demo 1:  3/27 17:25**
  - **Demo 2:  3/27 23:59**