DCS Lab 6
Pattern

葉曜銘

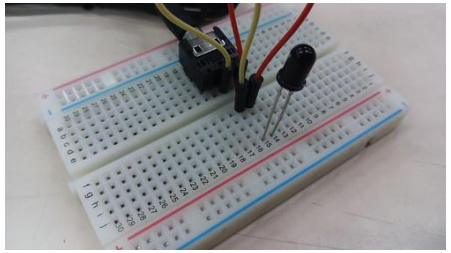
Purpose

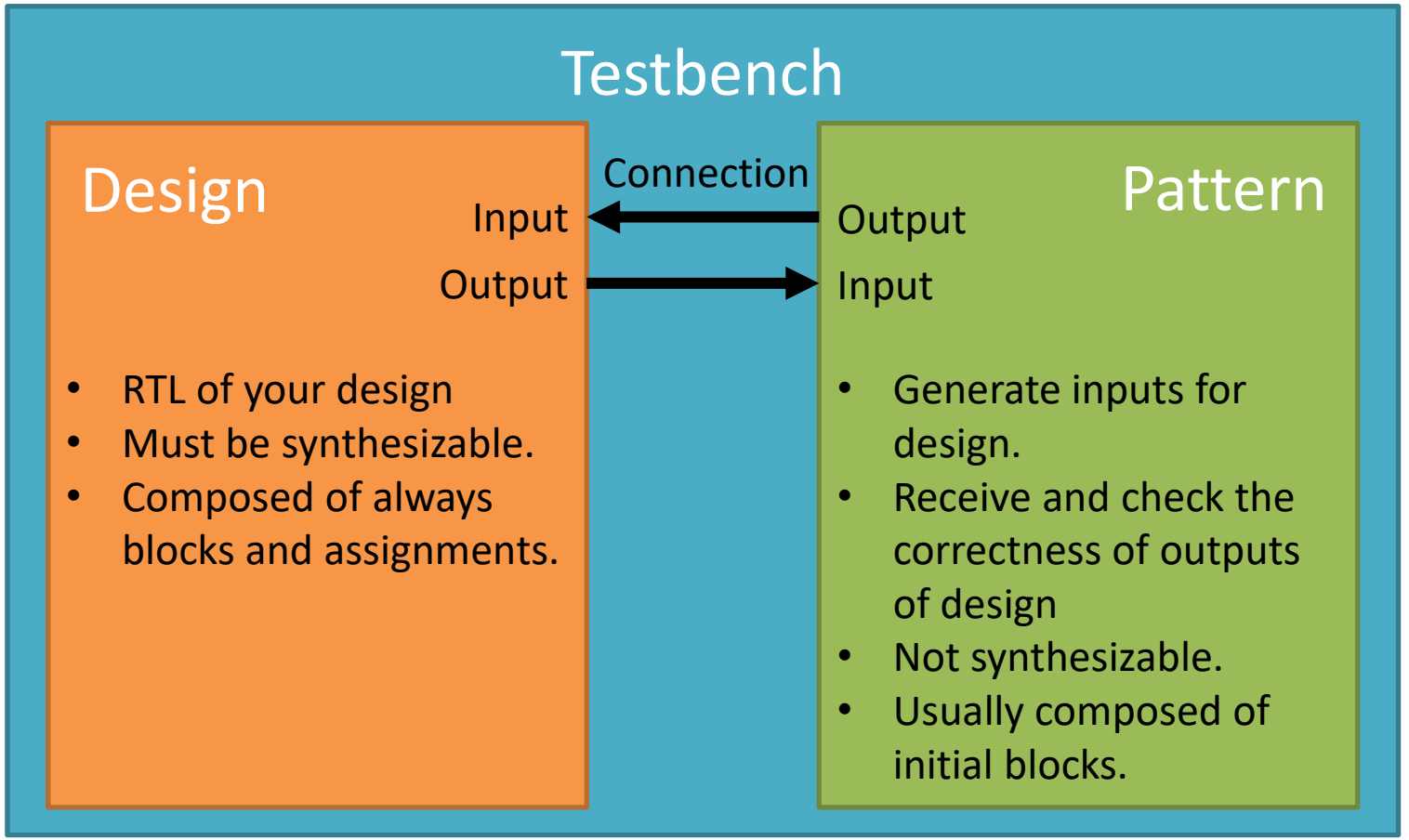
- Learn how to write a pattern to test your design.

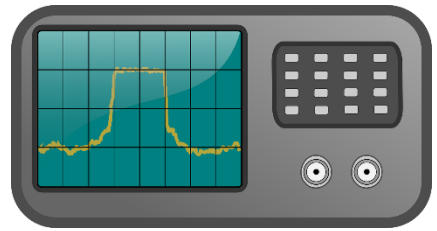
Lab06

- Run the command below to get files for this lab.
  - tar -xvf ~dcsTA01/Lab06.tar

Design vs. Testbench vs. Pattern







Always Block vs. Initial Block

```
always_ff @ (posedge clk or negedge rst_n) begin
    if(!rst_n) begin
        time_cs <= 'b0;
        out_valid_cs <= 'b0;
    end
    else begin
        time_cs <= time_ns;
        out_valid_cs <= out_valid_ns;
    end
end
always_comb begin
    if(in_valid) time_ns = in_time;
    else if(time_cs == 'b0) time_ns = 'd0;
    else time_ns = time_cs - 'd1;
end
```

Timer for this Lab

```
initial begin
    clk = 'b0;
    rst_n = 'b1;
    in_valid = 'b0;
    card = 'bx;

    #(10) check_reset;
    repeat(3) @(negedge clk);

    for(int i = 0; i < PATNUM; i++) begin
        input_task;
        check_ans;
        $display("\033[0;32mPASS PATTERN NO.%3d \033[m", i);
        repeat(($urandom % 3) + 3) @(negedge clk);
    end
    YOU_PASS_task;
    $finish;
end
```

Pattern for Lab03

Timer.sv (TA has written.)

- THIS IS NOT WHAT YOU SHOULD DO FOR THIS LAB!!!

Input Signal	Bit Width	Definition
clk	1	Clock.
rst_n	1	Asynchronous active-low reset.
in_valid	1	High when input is valid.
in_time	4	Start time for the timer.

Output Signal	Bit Width	Definition
out_time	4	Current time of the timer. Should be reset when rst_n is low.
out_finish	1	High for one cycle when the timer finishes. Should be reset when rst_n is low.

PATTERN.sv

- 00_TESTBED/PATTERN.sv

Input Signal	Bit Width	Definition
out_time	4	Current time of the timer.
out_finish	1	High for one cycle when the timer finishes.

Output Signal	Bit Width	Definition
clk	1	Clock.
rst_n	1	Asynchronous active-low reset.
in_valid	1	High when input is valid.
in_time	4	Start time for the timer.

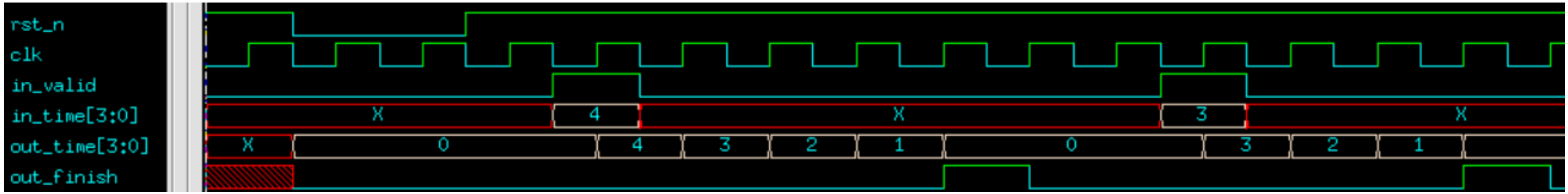
Timer.sv

- THIS IS NOT WHAT YOU SHOULD DO FOR THIS LAB!!!

All outputs should be reset when rst_n is low.

Pattern generate inputs.

Next pattern.



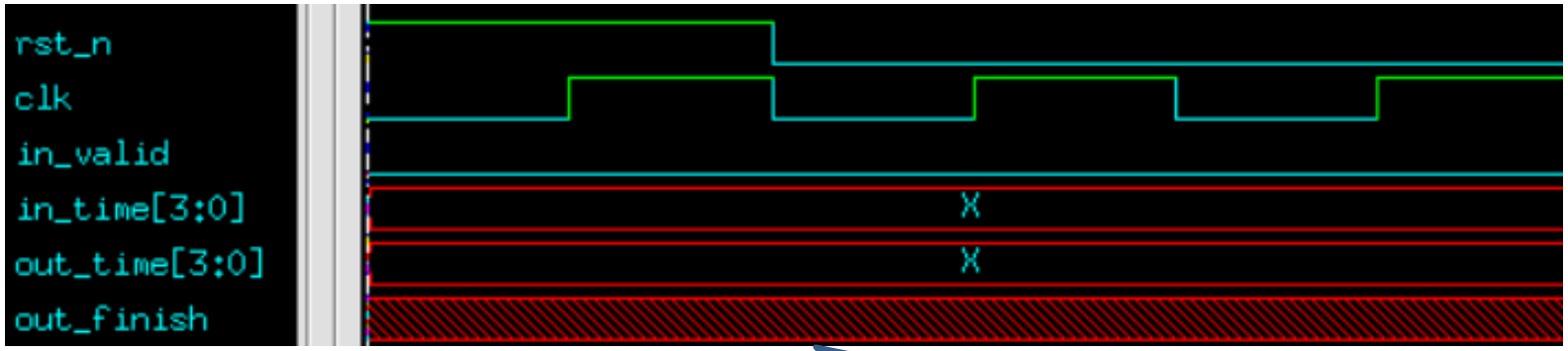
Timer start at posedge.

Timer finishes. out_finish is set for one cycle.

Specifications

Error code	Description
0	Outputs should be reset to zero when rst_n is low.
1	out_finish should be low before timer finishes.
2	out_time is incorrect.
3	out_finish should be high when timer finishes.
4	out_finish should be high for only one cycle. (after timer finishes)

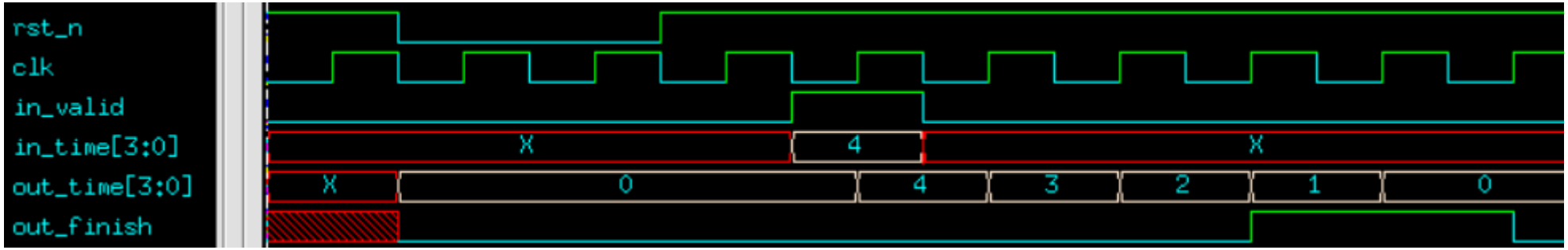
Error 0



Report this error if any output is not 0 after reset.

```
--------------------------------------------------------------------------------------------------------------------
                                                YOU FAIL!!!
                                                ERROR_0
                                Outputs should be reset to zero when rst_n is low.
--------------------------------------------------------------------------------------------------------------------
```

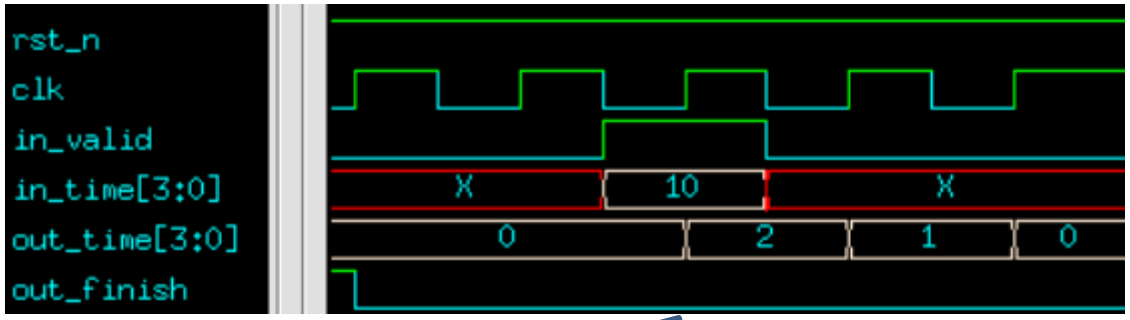
Error 1



Report this error if out_finish is 1 while out_time isn't 0.

```
--------------------------------------------------------------------------------
                                YOU FAIL!!!
                                ERROR_1
                out_finish should be low before timer finishes.
--------------------------------------------------------------------------------
```

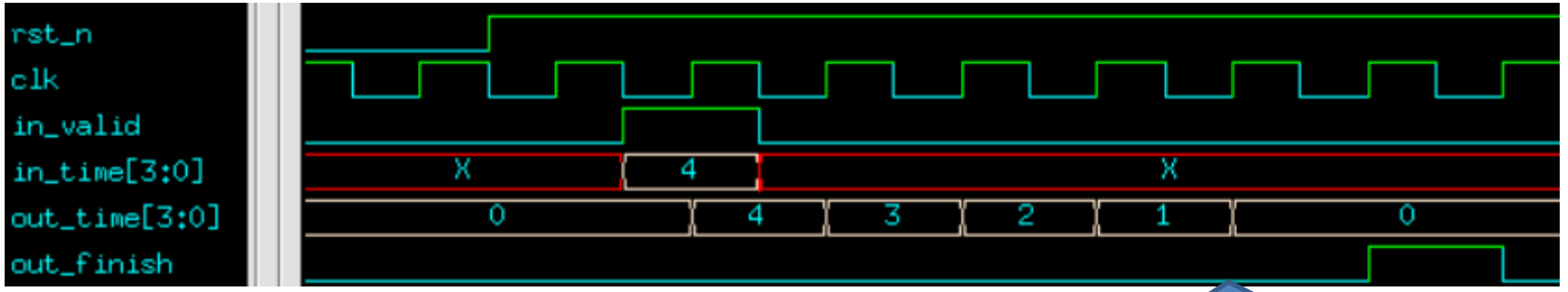
Error 2



Report this error if out_time is not correct value.

```
--------------------------------------------------------------------------------------------------------------------
                                                YOU FAIL!!!
                                                ERROR_2
                                           out_time is incorrect.
--------------------------------------------------------------------------------------------------------------------
```

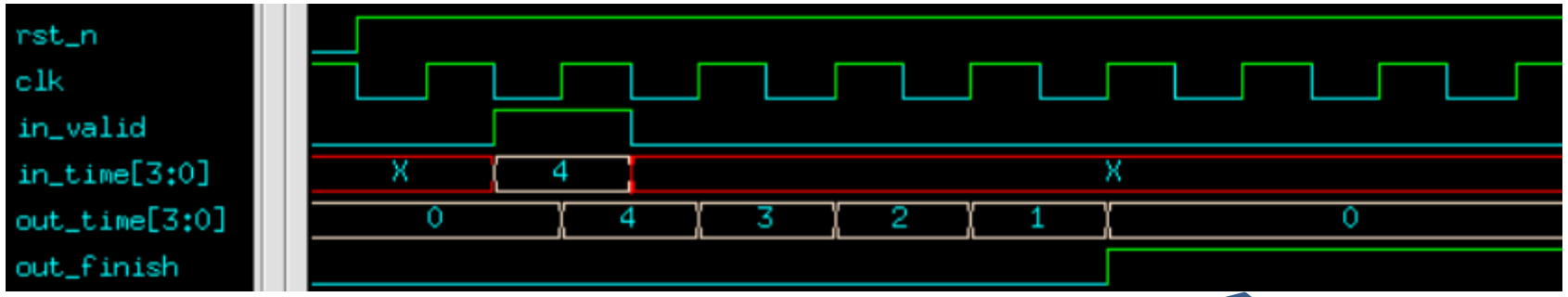
Error 3



Report this error if out_finish isn't 1 when out_time reaches 0.

```
--------------------------------------------------------------------------------------------------------
                                            YOU FAIL!!!
                                             ERROR_3
                                out_finish should be high when timer finishes.
--------------------------------------------------------------------------------------------------------
```

Error 4



Report this error if out_finish is still 1 at the second cycle after out_time reaches 0.

```
--------------------------------------------------------------------------------------------------------
                                            YOU FAIL!!!
                                            ERROR_4
                                out_finish should be high for only one cycle.
--------------------------------------------------------------------------------------------------------
```

Rules for Pattern

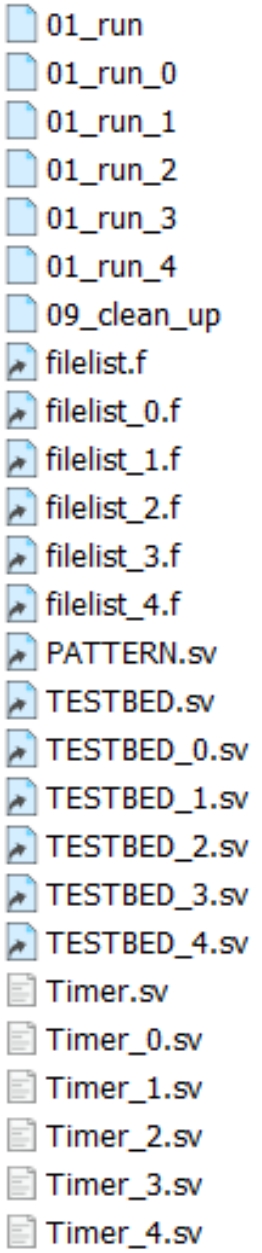
1. You should reset the design before testing patterns.
2. You should not provide a new pattern until the next cycle after the previous pattern finishes (out_finish is high).
3. You should call the task “fail(error code)” provided by TA when you detect an error, and call the task “YOU_PASS_task” if the design has no error.
4. You should not print anything ($display, $write, etc.) on screen except what is mentioned in “fail” and “YOU_PASS_task” tasks.

```
if(out_finish !== 'b0 || out_time !== 'b0) fail(0);
```

```
YOU_PASS_task;
```

File Usage

- **You should modify and submit the file 00_TESTBED/PATTERN.sv instead of 01_RTL/Timer.sv.**
- You should not modify or remove the tasks, “fail” and “YOU_PASS_task” in PATTERN.sv
- In 01_RTL directory:
  - Run 01_run for correct design. (Timer.sv)
  - Run 01_run_x for design with error code x. (Timer_x.sv)
- **There will be hidden cases for demo!**



Hidden Cases Release

- There is one hidden case for each error.
- The environment with hidden cases will be released **after the result of 1st demo is announced**. You can get it with:

  tar -xvf ~dcsTA01/Lab06_hid.tar

- To run a hidden case, you can use the command below in Lab06_hid/01_RTL directory:

  ./01_run_x_hid (x is the error code.)

Grading Policy

- Successfully distinguish correct design and every faulty design (print the message on screen): 100%
- Demo 2 打7折

Upload

- 請將Lab06/00_TESTBED裡的PATTERN.sv依以下命名規則重新命名後上傳至E3
- 命名規則：PATTERN_dcsxxx.sv，xxx為工作站帳號號碼
- **命名錯誤扣5分!!!**
- **Deadline:**
  - **Demo 1: 4/17 17:25**
  - **Demo 2: 4/17 23:59**