ARM Cortex-A8 Architecture

Key Characteristics

- Configurable IP core supporting ARMv7 instruction set
- Used in Apple iPad and smartphones by Motorola and Samsung

- Can issue two instructions per clock at rates up to 1GHz
- Two-level cache hierarchy with 16KB or 32KB L1 caches
- Optional L2 cache (128KB to 1MB) organized into 1-4 banks
- 64-byte block size for both cache levels

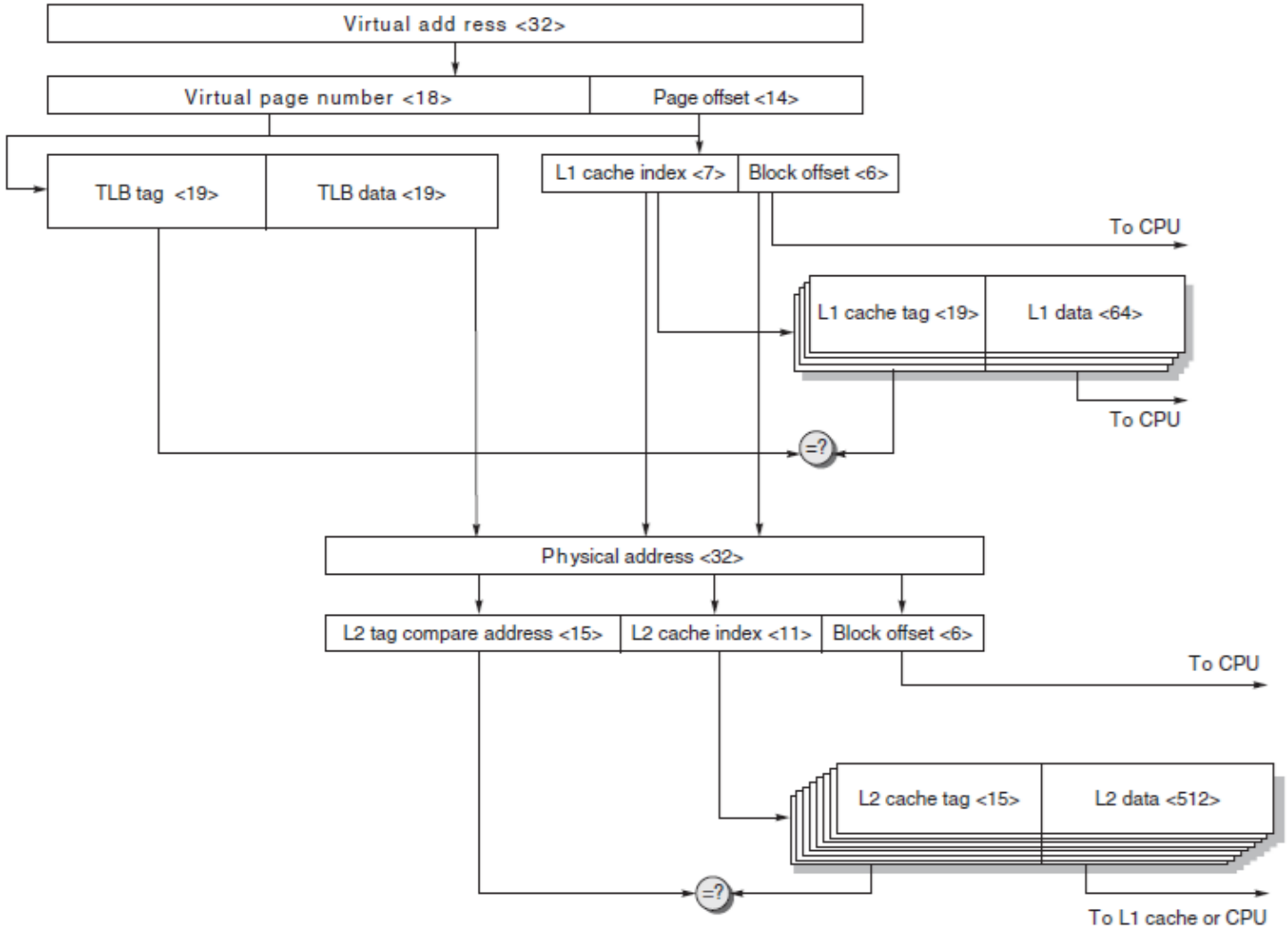
Memory Management

- Pair of fully associative TLBs (I and D) with 32 entries each
- Variable page sizes (4KB to 16MB)
- Round robin replacement algorithm
- Hardware-handled TLB misses

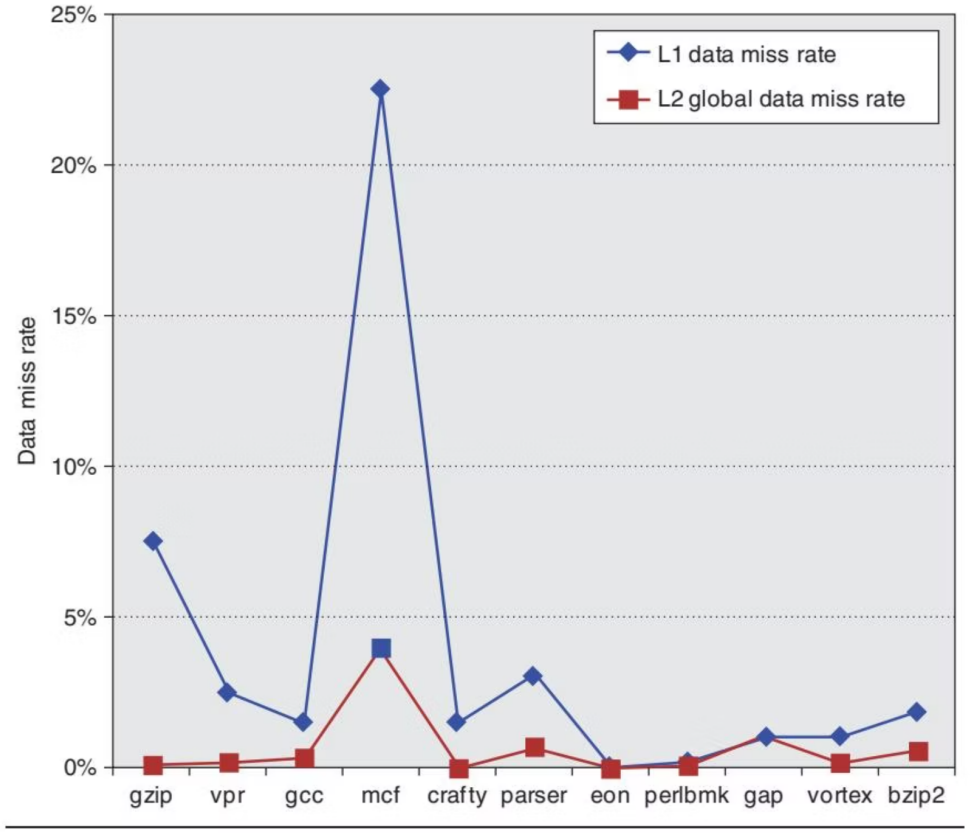
The Cortex-A8 comes in two flavors: Hard cores (optimized for specific vendors, higher performance) and Soft cores (can be compiled for different vendors and modified).

Cortex-A8 Memory Addressing

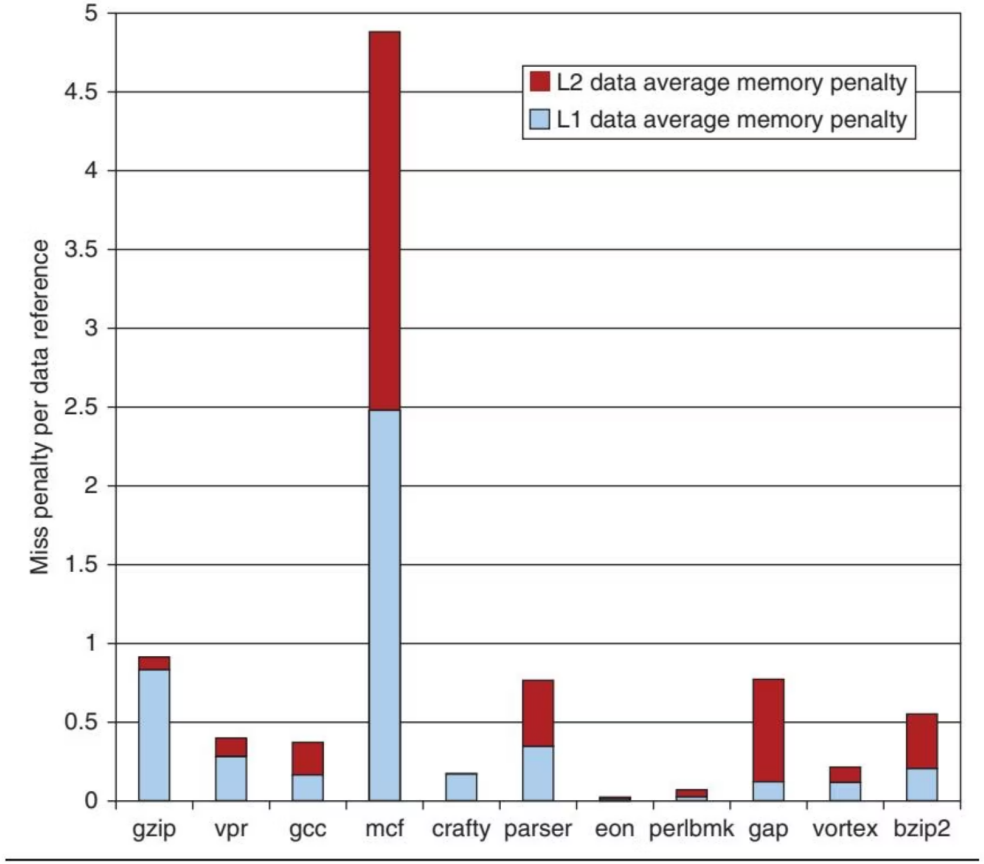
The figure shows how the 32-bit virtual address is used to index the TLB and caches, assuming 32KB primary caches and a 512KB secondary cache with 16KB page size. The TLB is fully associative with 32 entries, the L1 cache is four-way set associative, and the L2 cache is eight-way set associative.



Cortex-A8 Memory Performance



Data miss rates for ARM with 32KB L1 and 1MB L2 using integer Minnespec benchmarks. Applications with larger memory footprints have higher miss rates in both L1 and L2.



Average memory access penalty per data reference. Although L1 miss rates are significantly higher, the L2 miss penalty (60 cycles vs. 11 for L1) means L2 misses contribute significantly to overall penalty.

Intel Core i7 Architecture

Core Architecture

- Supports x86-64 instruction set architecture
- Four cores with out-of-order execution
- Up to four instructions per clock cycle
- 16-stage pipeline with dynamic scheduling
- Up to two simultaneous threads per processor

Memory System

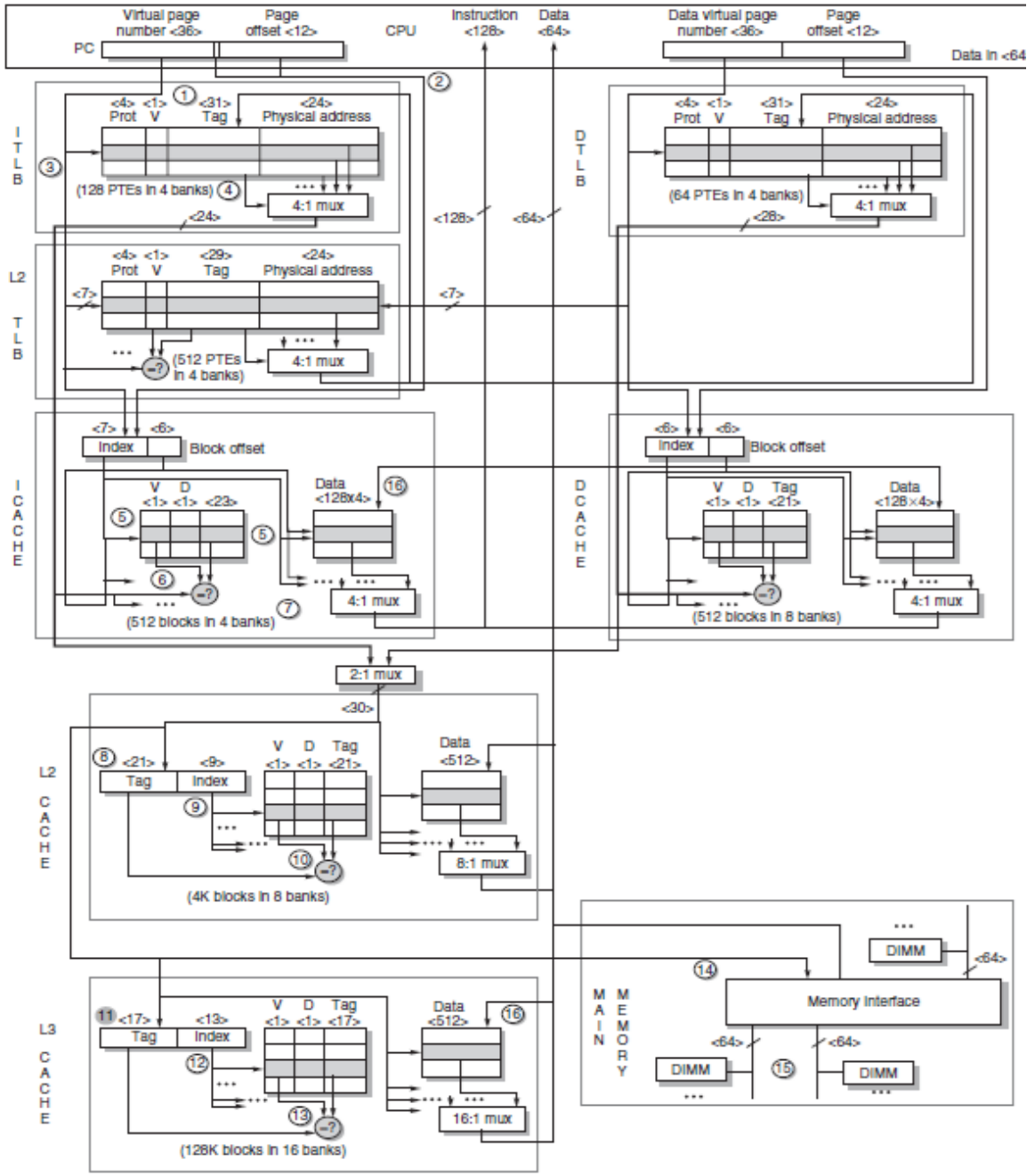
- 48-bit virtual addresses, 36-bit physical addresses
- Maximum physical memory of 36GB
- Three memory channels with separate DIMMs
- Peak memory bandwidth of 25GB/sec (DDR3-1066)
- Two-level TLB structure

The fastest i7 in 2010 had a clock rate of 3.3GHz, yielding a peak instruction execution rate of 13.2 billion instructions per second per core, or over 50 billion instructions per second for the four-core design.

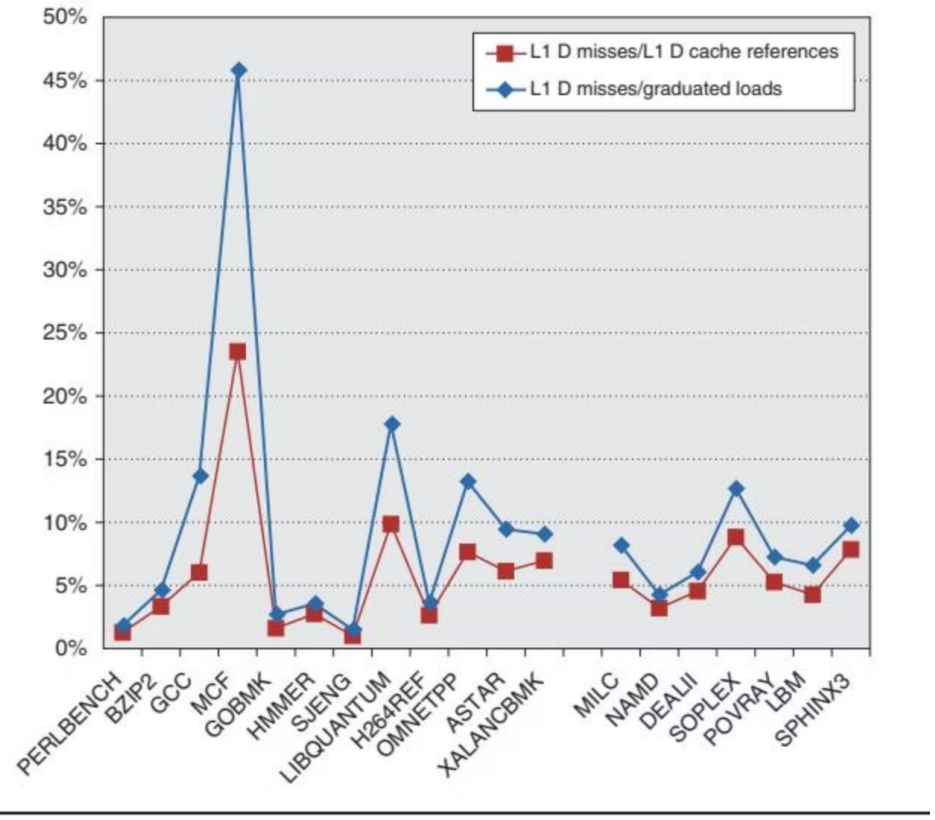
i7 Memory

Characteristic	Instruction TLB	Data DLB	Second-level TLB
Size	128	64	512
Associativity	4-way	4-way	4-way
Replacement	Pseudo-LRU	Pseudo-LRU	Pseudo-LRU
Access latency	1 cycle	1 cycle	6 cycles
Miss	7 cycles	7 cycles	Hundreds of cycles to access page table

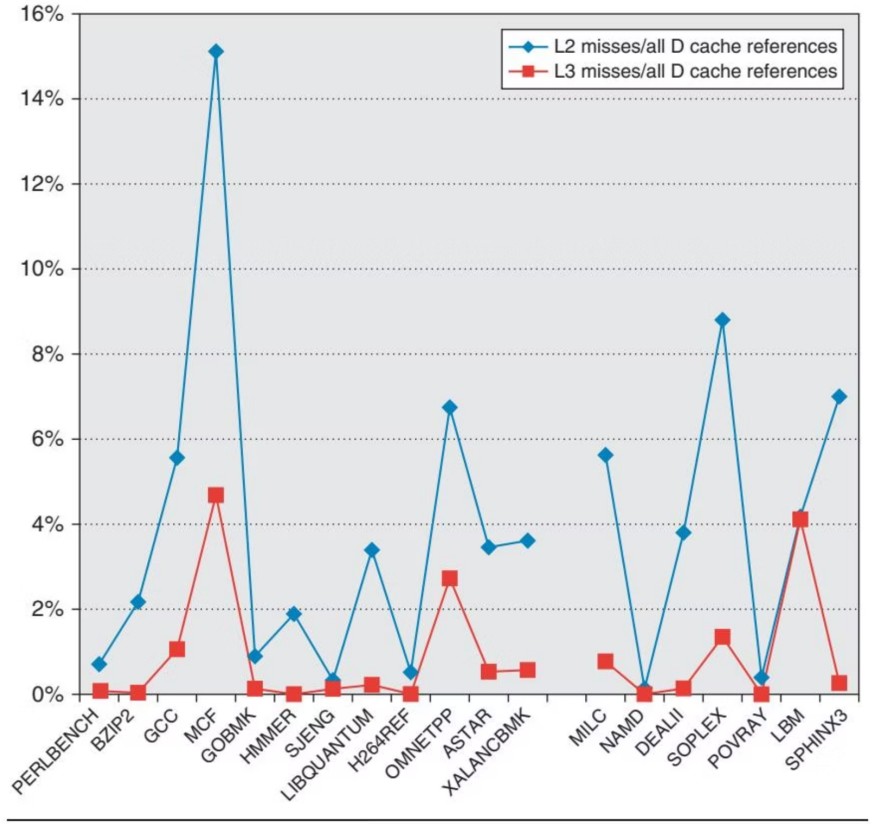
Characteristic	L1	L2	L3
Size	32 KB I/32 KB D	256 KB	2 MB per core
Associativity	4-way I/8-way D	8-way	16-way
Access latency	4 cycles, pipelined	10 cycles	35 cycles
Replacement scheme	Pseudo-LRU	Pseudo-LRU	Pseudo-LRU but with an ordered selection algorihtm



Intel i7 Memory Performance



L1 data cache miss rates for SPECCPU2006 benchmarks shown two ways: relative to completed loads (9.5% average) and relative to all L1 references (5.9% average).



L2 and L3 data cache miss rates relative to all L1 references. The average L2 miss rate is 4%, while L3 averages 1% - critical for performance as memory access costs over 100 cycles.