

# Putting It All Together

- When we combine **dynamic scheduling**, **multiple issue**, and **speculation**, we create a microarchitecture similar to those in modern processors.
- This integration allows for significant performance improvements by executing **multiple instructions** simultaneously while **handling dependencies** and **branch predictions**.



# Example

```

Loop:   LD      R2,0(R1)      ;R2=array element
        DADDIU  R2,R2,#1      ;increment R2
        SD      R2,0(R1)      ;store result
        DADDIU  R1,R1,#8      ;increment pointer
        BNE     R2,R3,LOOP    ;branch if not last element
  
```

One address calculation  
 One ALU operation  
 One branch evaluation  
 Two instruction committed  
 Per cycle

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
LD	R2,0(R1)	Issue	Execute	Memory	Write															
DADDIU	R2,R2,#1	Issue				Execute	Write													
SD	R2,0(R1)		Issue	Execute				Execute	Memory											
DADDIU	R1,R1,#8		Issue	Execute	Write															
BNE	R2,R3,LOOP			Issue				Execute												
LD	R2,0(R1)				Issue				Execute	Memory	Write									
DADDIU	R2,R2,#1				Issue					Execute	Write									
SD	R2,0(R1)					Issue			Execute				Execute	Memory						
DADDIU	R1,R1,#8					Issue				Execute	Write									
BNE	R2,R3,LOOP						Issue							Execute						
LD	R2,0(R1)							Issue							Execute	Memory	Write			
DADDIU	R2,R2,#1							Issue								Execute	Write			
SD	R2,0(R1)								Issue						Execute				Execute	Memory
DADDIU	R1,R1,#8								Issue							Execute	Write			
BNE	R2,R3,LOOP									Issue										Execute

Issue
Execute
Memory
Write

# Example with Speculation

```

Loop:   LD      R2, 0(R1)      ;R2=array element
        DADDIU  R2, R2, #1     ;increment R2
        SD      R2, 0(R1)     ;store result
        DADDIU  R1, R1, #8     ;increment pointer
        BNE     R2, R3, LOOP  ;branch if not last element
  
```

One address calculation  
 One ALU operation  
 One branch evaluation  
 Two instruction committed  
 Per cycle

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
LD	R2, 0(R1)	Issue	Execute	Memory	Write	Commit														
DADDIU	R2, R2, #1	Issue				Execute	Write	Commit												
SD	R2, 0(R1)		Issue	Execute					Write	Commit										
DADDIU	R1, R1, #8		Issue	Execute	Write				Commit											
BNE	R2, R3, LOOP			Issue				Execute	Commit											
LD	R2, 0(R1)				Issue	Execute	Memory	Write		Commit										
DADDIU	R2, R2, #1				Issue				Execute	Write	Commit									
SD	R2, 0(R1)					Issue	Execute				Write	Commit								
DADDIU	R1, R1, #8					Issue	Execute					Commit								
BNE	R2, R3, LOOP						Issue				Execute	Commit								
LD	R2, 0(R1)							Issue	Execute	Memory	Write		Commit							
DADDIU	R2, R2, #1							Issue				Execute	Write	Commit						
SD	R2, 0(R1)								Issue	Execute				Write	Commit					
DADDIU	R1, R1, #8								Issue	Execute		Write			Commit					
BNE	R2, R3, LOOP									Issue				Execute	Commit					

Issue
Execute
Memory
Write
Commit