MSI Protocol Example

- P0: read 120
- P0: write 120 <-- 80
- P2: write 120 <-- 80
- P1: read 110
- P0: write 108 <-- 48
- P0: write 130 <-- 78
- P2: write 130 <-- 78

P0

	State	Addr	Data
B0	I	100	00 10
B1	S	108	00 08
B2	M	110	00 30
B3	I	118	00 10

P1

	State	Addr	Data
B0	I	100	00 10
B1	M	128	00 68
B2	I	110	00 10
B3	S	118	00 10

P2

	State	Addr	Data
B0	S	120	00 20
B1	S	108	00 08
B2	I	110	00 10
B3	I	118	00 10

Memory

Addr	Data
100	00 10
108	00 08
110	00 10
118	00 18
120	00 20
128	00 28
130	00 30

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- P0: write 108 <-- 48
- P0: write 130 <-- 78
- P2: write 130 <-- 78

P0

	State	Addr	Data
B0	I→S	120	00 20
B1	S	108	00 08
B2	M	110	00 30
B3	I	118	00 10

P1

	State	Addr	Data
B0	I	100	00 10
B1	M	128	00 68
B2	I	110	00 10
B3	S	118	00 10

P2

	State	Addr	Data
B0	S	120	00 20
B1	S	108	00 08
B2	I	110	00 10
B3	I	118	00 10

Memory

Addr	Data
100	00 10
108	00 08
110	00 10
118	00 18
120	00 20
128	00 28
130	00 30

Place read miss on bus

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P1

	State	Addr	Data
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B1	M	128	00 68
B2	I	110	00 10
B3	S	118	00 10

P2

	State	Addr	Data
B0	S→I	120	00 20
B1	S	108	00 08
B2	I	110	00 10
B3	I	118	00 10

Place invalidate on bus

Memory

Addr	Data
100	00 10
108	00 08
110	00 10
118	00 18
120	00 20
128	00 28
130	00 30

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B3	S	118	00 10

P2

	State	Addr	Data
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B1	S	108	00 08
B2	I	110	00 10
B3	I	118	00 10

Memory

Addr	Data
100	00 10
108	00 08
110	00 10
118	00 18
120	00 80
128	00 28
130	00 30

Write-back block

Place write miss on bus

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B2	M→S	110	00 30
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P1

	State	Addr	Data
B0	I	100	00 10
B1	M	128	00 68
B2	I→S	110	00 30
B3	S	118	00 10

P2

	State	Addr	Data
B0	M	120	00 80
B1	S	108	00 08
B2	I	110	00 10
B3	I	118	00 10

Memory

Addr	Data
100	00 10
108	00 08
110	00 30
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Write-back block

Place read miss on bus

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B2	S	110	00 30
B3	I	118	00 10

P1

	State	Addr	Data
B0	I	100	00 10
B1	M	128	00 68
B2	S	110	00 30
B3	S	118	00 10

P2

	State	Addr	Data
B0	M	120	00 80
B1	S→I	108	00 08
B2	I	110	00 10
B3	I	118	00 10

Place invalidate on bus

Memory

Addr	Data
100	00 10
108	00 08
110	00 30
118	00 18
120	00 80
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P1

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B0	I	100	00 10
B1	M	128	00 68
B2	S	110	00 30
B3	S	118	00 10

P2

	State	Addr	Data
B0	M	120	00 80
B1	I	108	00 08
B2	I	110	00 10
B3	I	118	00 10

Place write miss on bus

Memory

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100	00 10
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118	00 18
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B2	S	110	00 30
B3	S	118	00 10

P2

	State	Addr	Data
B0	M	120	00 80
B1	I→M	130	00 78
B2	I	110	00 10
B3	I	118	00 10

Memory

Addr	Data
100	00 10
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