Crosscutting Issues in Memory Hierarchy Design

Protection & Instruction Set Architecture

Protection requires joint effort between architecture and operating systems. ISAs often needed modification to support virtual memory:

- IBM had to change the 360 ISA just 6 years after announcement
- 80x86 POPF instruction required virtualization extensions
- IBM mainframe hardware took three steps to improve VM performance

Coherency of Cached Data

Data can exist in both memory and cache, creating potential consistency issues:

- Multiprocessors: Sharing data across caches is common and critical for performance
- I/O coherency: Must determine if I/O occurs between device and cache or device and memory
- Solutions include write-through caches, noncachable buffer pages, and cache invalidation on I/O