

MSI Protocol Example

- P0: read 120
- P0: write 120 <-- 80
- P2: write 120 <-- 80
- P1: read 110
- P0: write 108 <-- 48
- P0: write 130 <-- 78
- P2: write 130 <-- 78

P0				P1				P2				Memory	
	State	Addr	Data		State	Addr	Data		State	Addr	Data	Addr	Data
B0	I	100	00 10	B0	I	100	00 10	B0	S	120	00 20	100	00 10
B1	S	108	00 08	B1	M	128	00 68	B1	S	108	00 08	108	00 08
B2	M	110	00 30	B2	I	110	00 10	B2	I	110	00 10	110	00 10
B3	I	118	00 10	B3	S	118	00 10	B3	I	118	00 10	118	00 18
												120	00 20
												128	00 28
												130	00 30

Diagram illustrating the MSI protocol sequence:

- P0:** Initiates a read operation at address 120.
- P1:** Initiates a read operation at address 110.
- P2:** Initiates a write operation at address 120 with data 80.
- P0:** Initiates a write operation at address 108 with data 48.
- P0:** Initiates a write operation at address 130 with data 78.
- P2:** Initiates a write operation at address 130 with data 78.

The sequence shows a back-to-back read operation (B0, B1) followed by a write operation (B0, B2). This pattern repeats for P1 and P2. The final row shows the state of memory after all operations have been completed.

MSI Protocol Example

- P0: read 120
 - P0: write 120 <- 80
 - P2: write 120 <- 80
 - P1: read 110
 - P0: write 108 <- 48
 - P0: write 130 <- 78
 - P2: write 130 <- 78

	State	Addr	Data
B0	I → S	120	00 20
B1	S	108	00 08
B2	M	110	00 30
B3	I	118	00 10

P1			
	State	Addr	Data
B0	I	100	00 10
B1	M	128	00 68
B2	I	110	00 10
B3	S	118	00 10

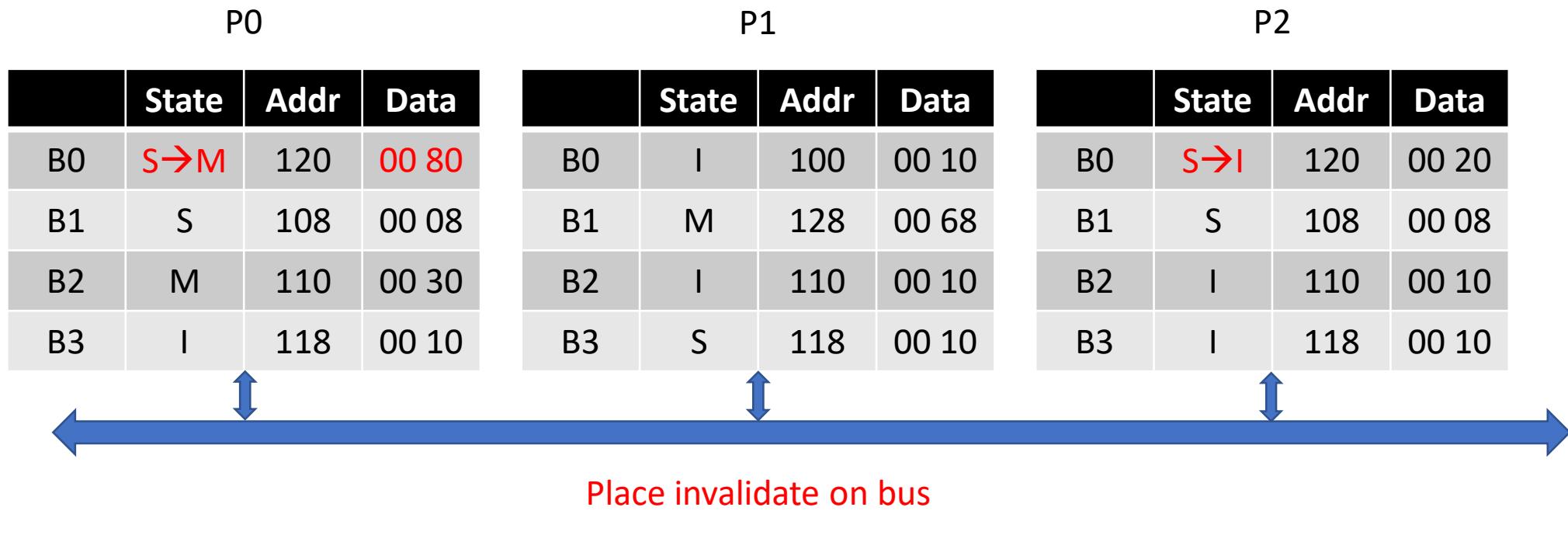
	State	Addr	Data
B0	S	120	00 20
B1	S	108	00 08
B2	I	110	00 10
B3	I	118	00 10

Memory	
Addr	Data
100	00 10
108	00 08
110	00 10
118	00 18
120	00 20
128	00 28
130	00 30

Place read miss on bus

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- P0: write 108 <-- 48
- P0: write 130 <-- 78
- P2: write 130 <-- 78



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- P0: read 120
- P0: write 120 <-- 80
- **P2: write 120 <-- 80**
- P1: read 110
- P0: write 108 <-- 48
- P0: write 130 <-- 78
- P2: write 130 <-- 78

P0				P1				P2				Memory	
	State	Addr	Data		State	Addr	Data		State	Addr	Data	Addr	Data
B0	M→I	120	00 80	B0	I	100	00 10	B0	I→M	120	00 80	100	00 10
B1	S	108	00 08	B1	M	128	00 68	B1	S	108	00 08	108	00 08
B2	M	110	00 30	B2	I	110	00 10	B2	I	110	00 10	110	00 10
B3	I	118	00 10	B3	S	118	00 10	B3	I	118	00 10	118	00 18
													

Write-back block

Place write miss on bus

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- P0: read 120
- P0: write 120 <-- 80
- P2: write 120 <-- 80
- **P1: read 110**
- P0: write 108 <-- 48
- P0: write 130 <-- 78
- P2: write 130 <-- 78

P0				P1				P2				Memory	
	State	Addr	Data		State	Addr	Data		State	Addr	Data	Addr	Data
B0	I	120	00 80	B0	I	100	00 10	B0	M	120	00 80	100	00 10
B1	S	108	00 08	B1	M	128	00 68	B1	S	108	00 08	108	00 08
B2	M→S	110	00 30	B2	I→S	110	00 30	B2	I	110	00 10	110	00 30
B3	I	118	00 10	B3	S	118	00 10	B3	I	118	00 10	118	00 18
												120	00 80
												128	00 28
												130	00 30

↑↓ Write-back block
 ↑↓ Place read miss on bus
 ↑↓

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- P1: read 110
- **P0: write 108 <-- 48**
- P0: write 130 <-- 78
- P2: write 130 <-- 78

P0				P1				P2				Memory	
	State	Addr	Data		State	Addr	Data		State	Addr	Data	Addr	Data
B0	I	120	00 80	B0	I	100	00 10	B0	M	120	00 80	100	00 10
B1	S→M	108	00 48	B1	M	128	00 68	B1	S→I	108	00 08	108	00 08
B2	S	110	00 30	B2	S	110	00 30	B2	I	110	00 10	110	00 30
B3	I	118	00 10	B3	S	118	00 10	B3	I	118	00 10	118	00 18
 <p>Place invalidate on bus</p>												120	00 80
												128	00 28
												130	00 30

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- **P0: write 130 <-- 78**
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