Arm Cortex-M Processor Comparison Table

The Cortex-M processor family is optimized for cost and energy-efficient microcontrollers. These processors are found in a variety of applications, including IoT, industrial and everyday consumer devices.
The processor family is based on the M-Profile Architecture that provides low-latency and a highly deterministic operation, for deeply embedded systems.

Feature	Cortex-M0	Cortex-M0+	Cortex-M1	Cortex-M23	Cortex-M3	Cortex-M4	Cortex-M33	Cortex-M35P	Cortex-M55	Cortex-M7
Instruction Set Architecture	Armv6-M	Armv6-M	Armv6-M	Armv8-M Baseline	Armv7-M	Armv7-M	Armv8-M Mainline	Armv8-M Mainline	Armv8.1-M Mainline	Armv7-M
TrustZone for Armv8-M	No	No	No	Yes (option)	No	No	Yes (option)	Yes (option)	Yes (option)	No
Helium (M-Profile Vector Extension)	No	No	No	No	No	No	No	No	Yes (option)	No
Floating-Point Unit (FPU)	No	No	No	No	No	SP (option)	SP (option)	SP (option)	HP, SP, DP (option)	SP, DP (option)
Digital Signal Processing (DSP) Extension	No	No	No	No	No	Yes	Yes (option)	Yes (option)	Yes	Yes
Hardware Divide	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Arm Custom Instructions	No	No	No	No	No	No	Yes (option)	No	Yes (option)	No
Coprocessor Interface	No	No	No	No	No	No	Yes (option)	Yes (option)	Yes (option)	No
DMIPS/MHz*	0.96	0.99	0.88	1.03	1.24	1.26	1.54	1.50	1.69	2.31
CoreMark®/MHz*	2.33	2.46	1.83	2.64	3.45	3.54	4.10	4.10	4.40	5.29
Maximum # External Interrupts	32	32	32	240	240	240	480	480	480	240
Maximum MPU Regions	0	8	0	16	8	8	16	16	16	16
Bus Protocol	AHB Lite	AHB Lite	AHB Lite	AHB	AHB Lite	AHB Lite	AHB	AHB	AXI	AXI
Instruction Cache	No	No	No	No	No	No	No	2-16kB	0-64kB	0-64kB
Data Cache	No	No	No	No	No	No	No	No	0-64kB	0-64kB
Instruction TCM	No	No	0-1MB	No	No	No	No	No	0-16MB	0-16MB
Data TCM	No	No	0-1MB	No	No	No	No	No	0-16MB	0-16MB
Dual Core Lock-Step (DCLS)	No	No	No	No	No	No	No	Yes	Yes	Yes
Common Criteria Certification	No	No	No	No	No	No	Yes	Yes	No	No
Reference Package / System Example	Corstone-101	Corstone-101	-	Corstone-102	Corstone-101	-	Corstone-201	-	Corstone-300	-