

BÁO CÁO THỰC HÀNH

Họ tên	Lê Minh Nhựt	Lớp: IT012.N22.1
MSSV	22521060	STT: 21
Bài Thực Hành	LAB 2	
CBHD	Trương Văn Cường	

Yêu cầu thực hành

Về phần trình bày:

- Sinh viên trình bày đúng theo định dạng báo cáo mà CBHD đưa ra.
- Cần chú thích bảng, hình (nếu có).
- Sử dụng chức năng Insert Caption và Cross-reference cho chú thích Bảng, Hình
- Sử dụng tính năng Screenshot để chụp kết quả mô phỏng.

Quy trình thực hành:

- Sinh viên chuẩn bị bài ở nhà, và có mặt đúng giờ tại phòng LAB.
- Sinh viên thực hành theo hướng dẫn, và nộp bài đúng hạn.
- Hoàn thành bài tập về nhà (nếu có)
- Tất cả các bài báo cáo có hành vi sao chép của nhau sẽ bị **điểm 0**

Điểm buổi thực hành

Chuyên cần (20%)		
Trình bày (20%)		
Nội dung thực hành (60%)		
Câu 1:		
Câu 2:		
Tổng (100%)		

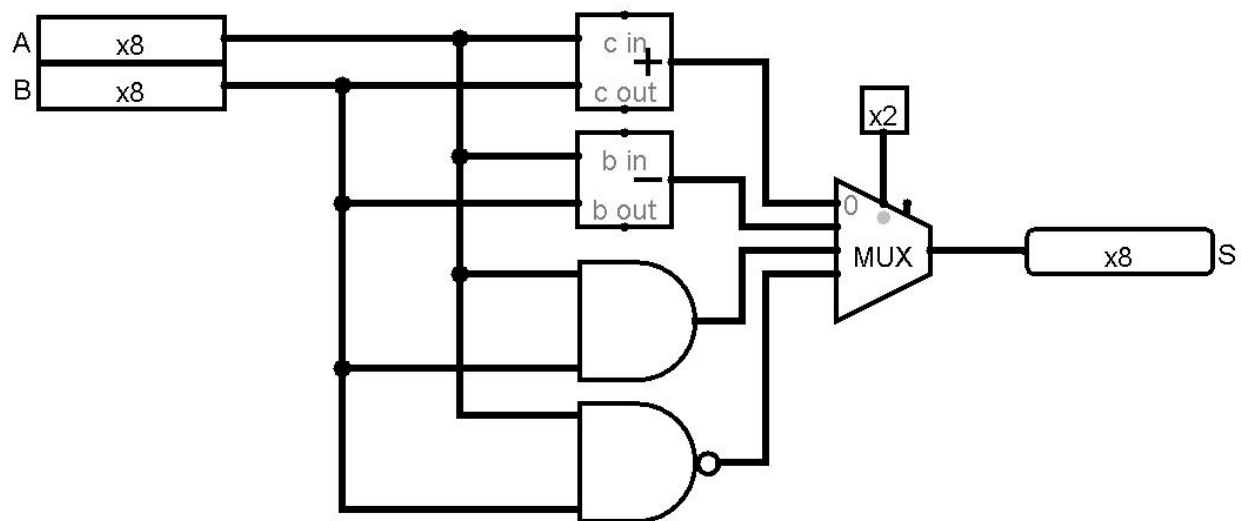
Bài tập thực hành:

- 1 Mô phỏng ALU
- 2 Mô phỏng Register Files
- 3.1 Cải tiến và mô phỏng ALU
- 3.2 Register Files với địa xuất riêng với địa chỉ ghi
4. Mô phỏng D-latch và D-fliplop

THỰC HÀNH

1. Mô phỏng ALU

-Sơ đồ mạch (xuất hình từ Logisim)

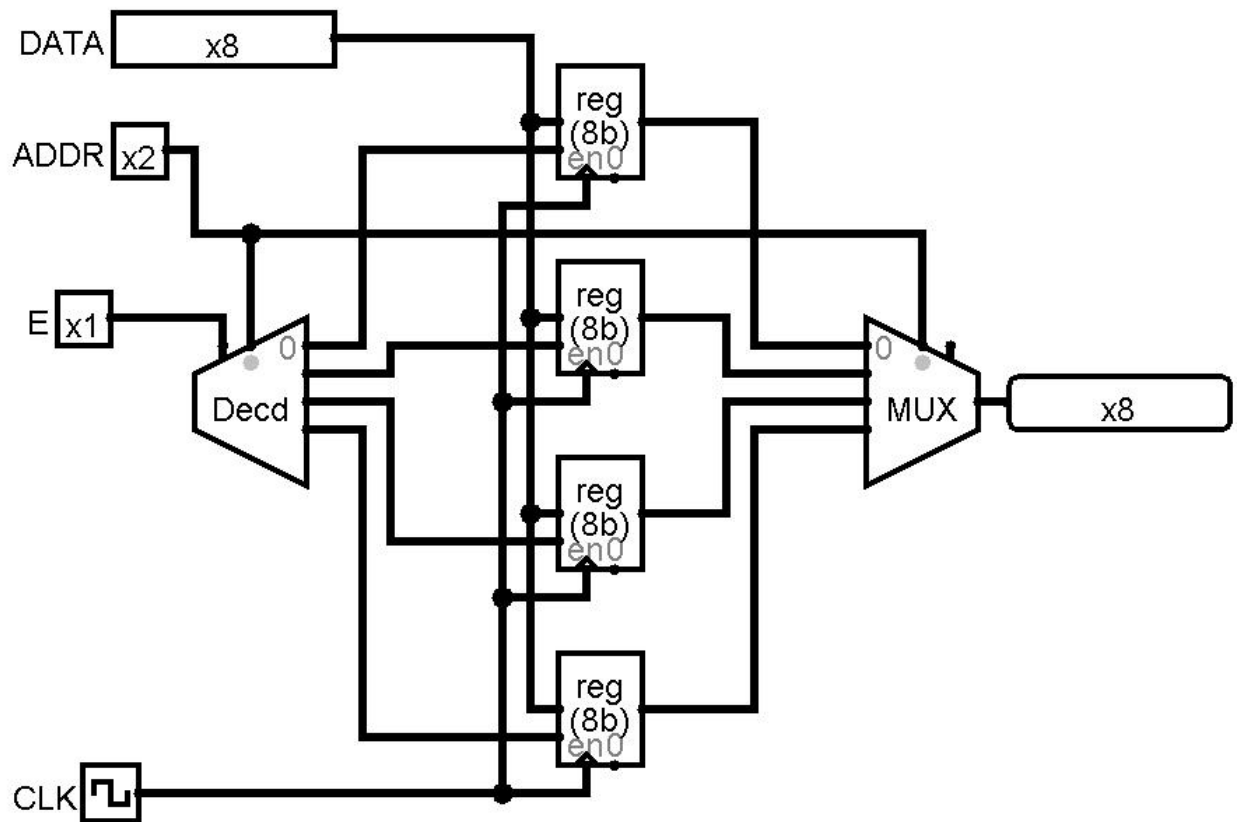


-Bảng mô phỏng

A	B	O	S
0x00	0x00	00	0x00
0xFF	0xFF	10	0xFF
0xF0	0x0F	01	0xE1
0xF0	0x0F	11	0xFF
0x5A	0xA5	00	0xFF
0xA5	0x5A	10	0x00
0xC3	0x3C	01	0x87
0xC3	0x3C	11	0xFF

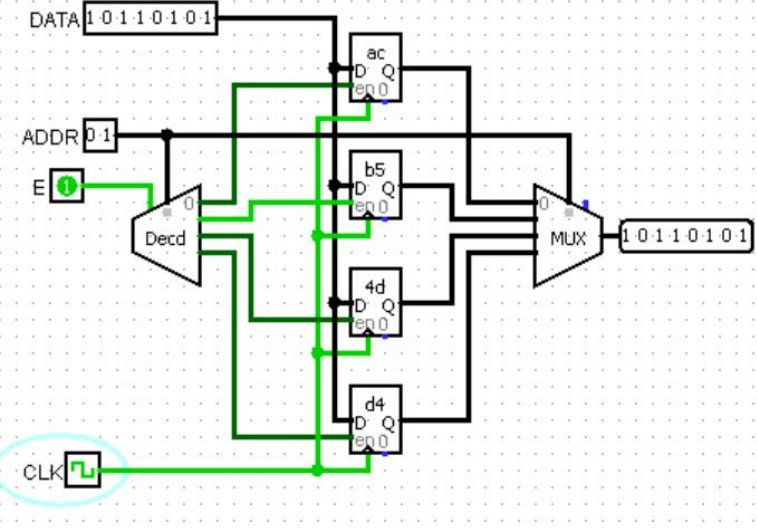
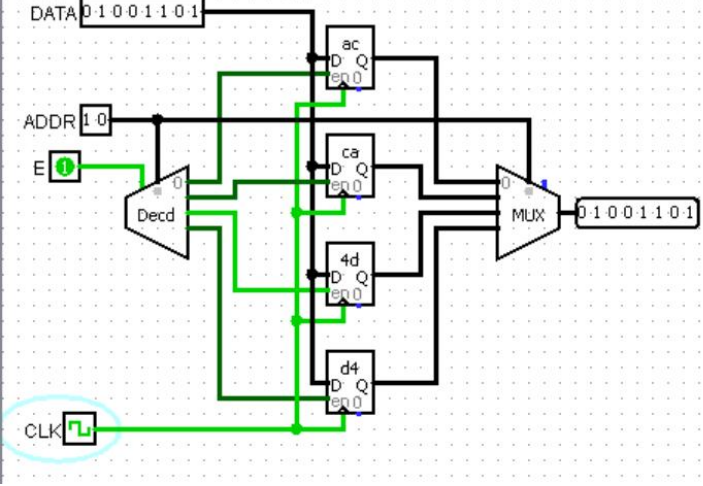
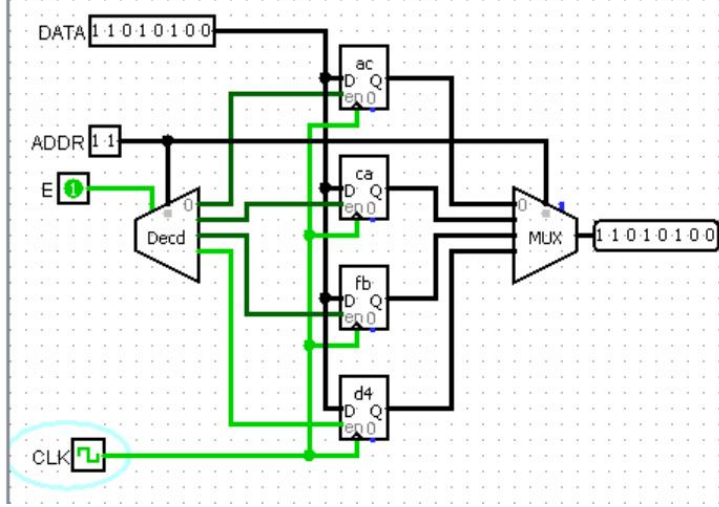
2. Mô phỏng Register Files

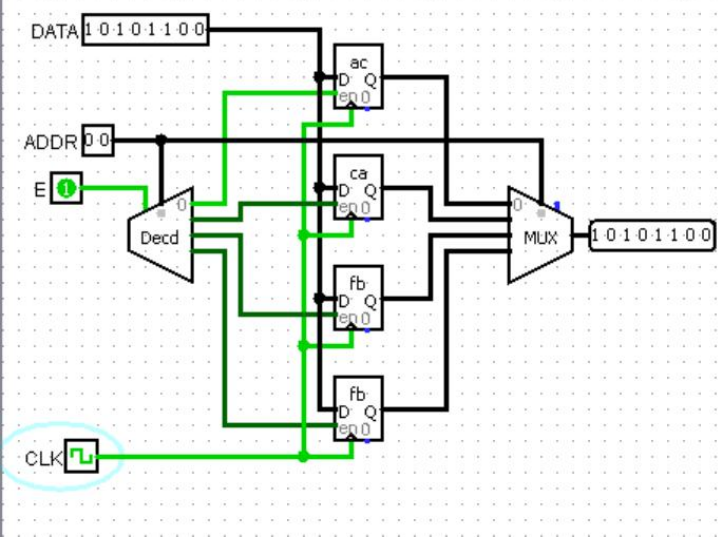
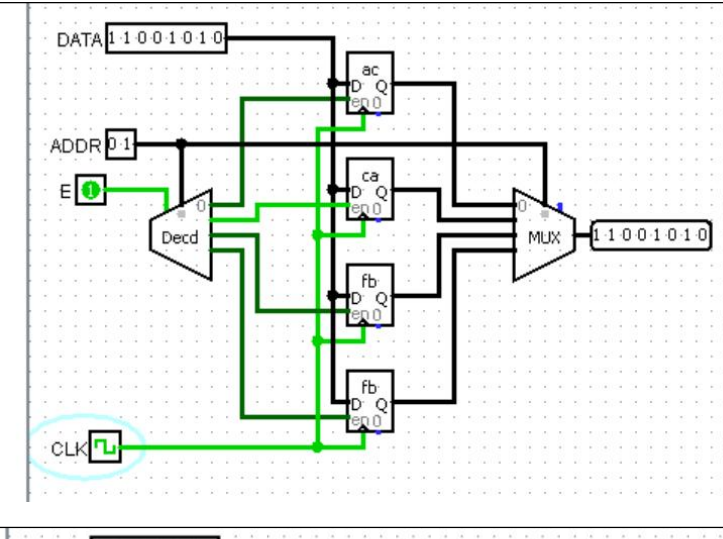
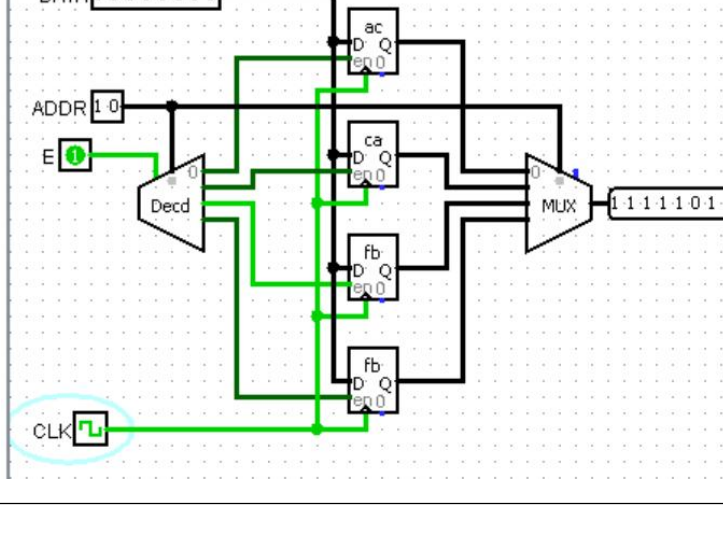
- Sơ đồ mạch(xuất hình từ Logisim)

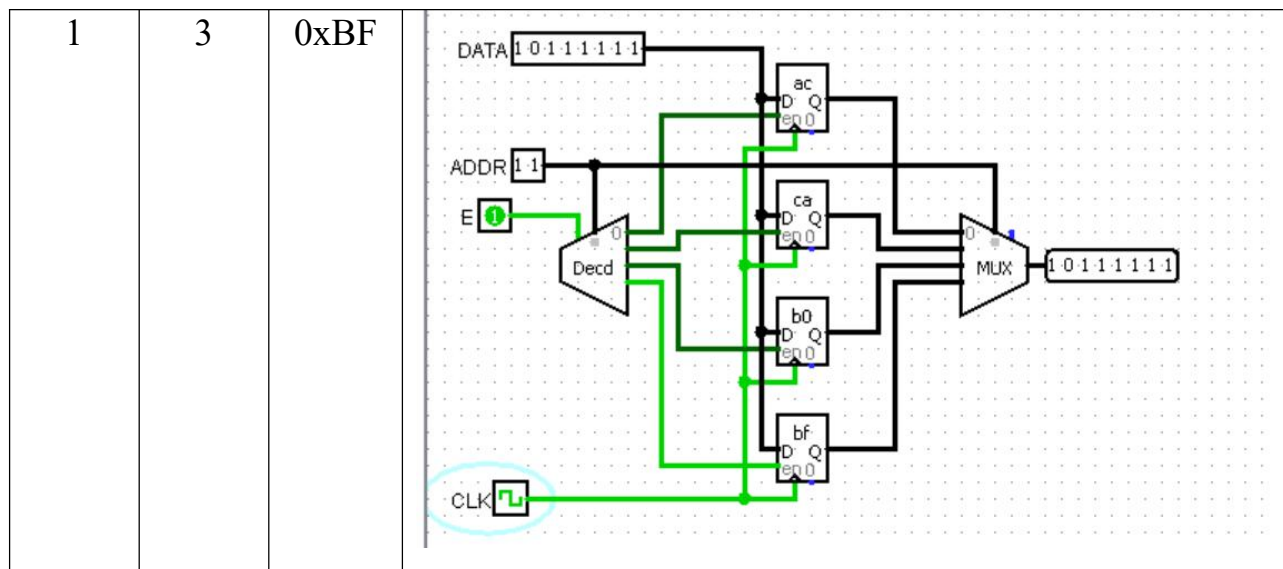


- Bảng mô phỏng khi cho clock tích cực

Enabl e	Addre ss	Data	Result
1	0	0x5B	

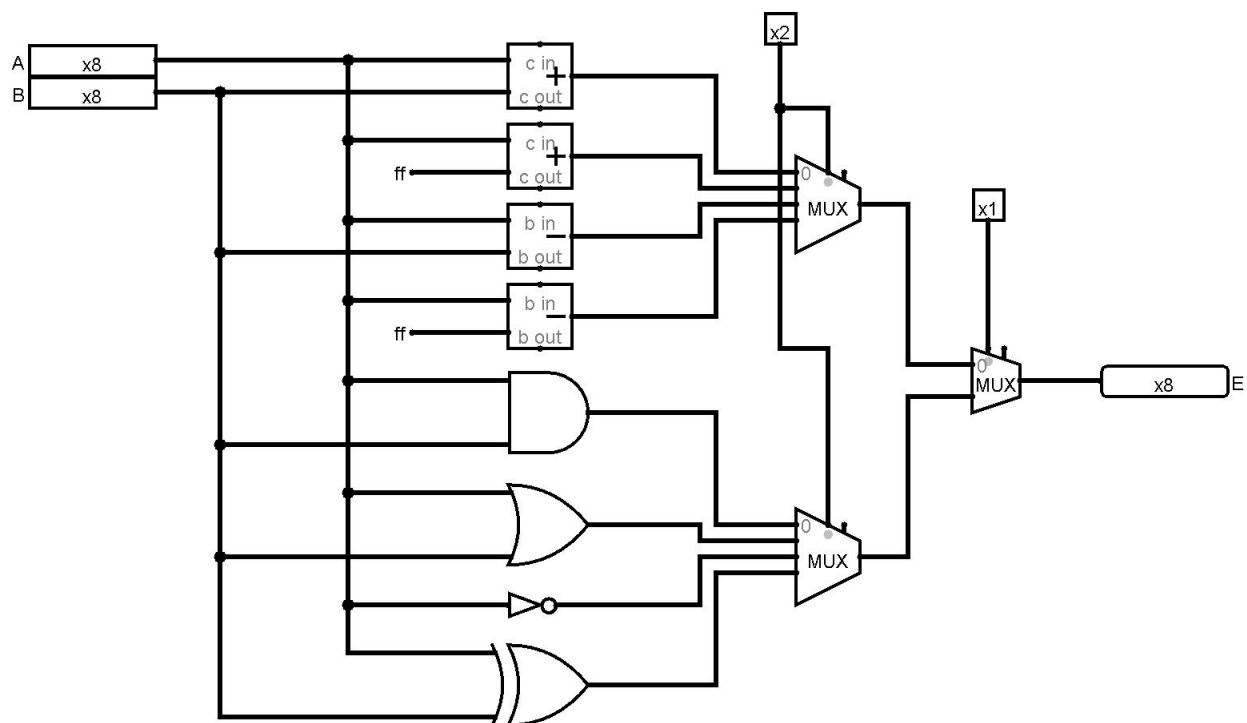
1	1	0xB5	 <p>Circuit diagram for 0xB5. The DATA input is 10110101. The ADDR input is 01. The enable signal E is 1. The clock signal CLK is active low. The circuit consists of a 2-to-4 decoder (Decd) with inputs ADDR and E. The decoder outputs are connected to four D flip-flops: ac, b5, 4d, and d4. The DATA input is connected to the D inputs of all four flip-flops. The clock signal CLK is connected to the clock inputs of all four flip-flops. The outputs of the flip-flops are connected to a 4-to-1 multiplexer (MUX). The MUX output is 10110101.</p>
1	2	0x4D	 <p>Circuit diagram for 0x4D. The DATA input is 01001101. The ADDR input is 10. The enable signal E is 1. The clock signal CLK is active low. The circuit consists of a 2-to-4 decoder (Decd) with inputs ADDR and E. The decoder outputs are connected to four D flip-flops: ac, ca, 4d, and d4. The DATA input is connected to the D inputs of all four flip-flops. The clock signal CLK is connected to the clock inputs of all four flip-flops. The outputs of the flip-flops are connected to a 4-to-1 multiplexer (MUX). The MUX output is 01001101.</p>
1	3	0xD4	 <p>Circuit diagram for 0xD4. The DATA input is 11010100. The ADDR input is 11. The enable signal E is 1. The clock signal CLK is active low. The circuit consists of a 2-to-4 decoder (Decd) with inputs ADDR and E. The decoder outputs are connected to four D flip-flops: ac, ca, fb, and d4. The DATA input is connected to the D inputs of all four flip-flops. The clock signal CLK is connected to the clock inputs of all four flip-flops. The outputs of the flip-flops are connected to a 4-to-1 multiplexer (MUX). The MUX output is 11010100.</p>

1	0	0xAC	 <p>The circuit diagram for 0xAC shows the following state: DATA is 10101100, ADDR is 00, and E is 1. The CLK signal is active. The Decd (decoder) has two outputs, 0 and 1, both of which are connected to the 'ca' register. The 'ca' register is currently holding 10101100. The 'fb' register is currently holding 00000000. The MUX (multiplexer) has four inputs: 'ac' (00000000), 'ca' (10101100), 'fb' (00000000), and 'fb' (00000000). The MUX output is 10101100.</p>
1	1	0xCA	 <p>The circuit diagram for 0xCA shows the following state: DATA is 11001010, ADDR is 01, and E is 1. The CLK signal is active. The Decd (decoder) has two outputs, 0 and 1, both of which are connected to the 'ca' register. The 'ca' register is currently holding 11001010. The 'fb' register is currently holding 00000000. The MUX (multiplexer) has four inputs: 'ac' (00000000), 'ca' (11001010), 'fb' (00000000), and 'fb' (00000000). The MUX output is 11001010.</p>
1	2	0xFB	 <p>The circuit diagram for 0xFB shows the following state: DATA is 11111011, ADDR is 10, and E is 1. The CLK signal is active. The Decd (decoder) has two outputs, 0 and 1, both of which are connected to the 'ca' register. The 'ca' register is currently holding 11111011. The 'fb' register is currently holding 00000000. The MUX (multiplexer) has four inputs: 'ac' (00000000), 'ca' (11111011), 'fb' (00000000), and 'fb' (00000000). The MUX output is 11111011.</p>



3. Cải tiến và mô phỏng ALU

- Sơ đồ mạch(xuất hình từ Logisim)



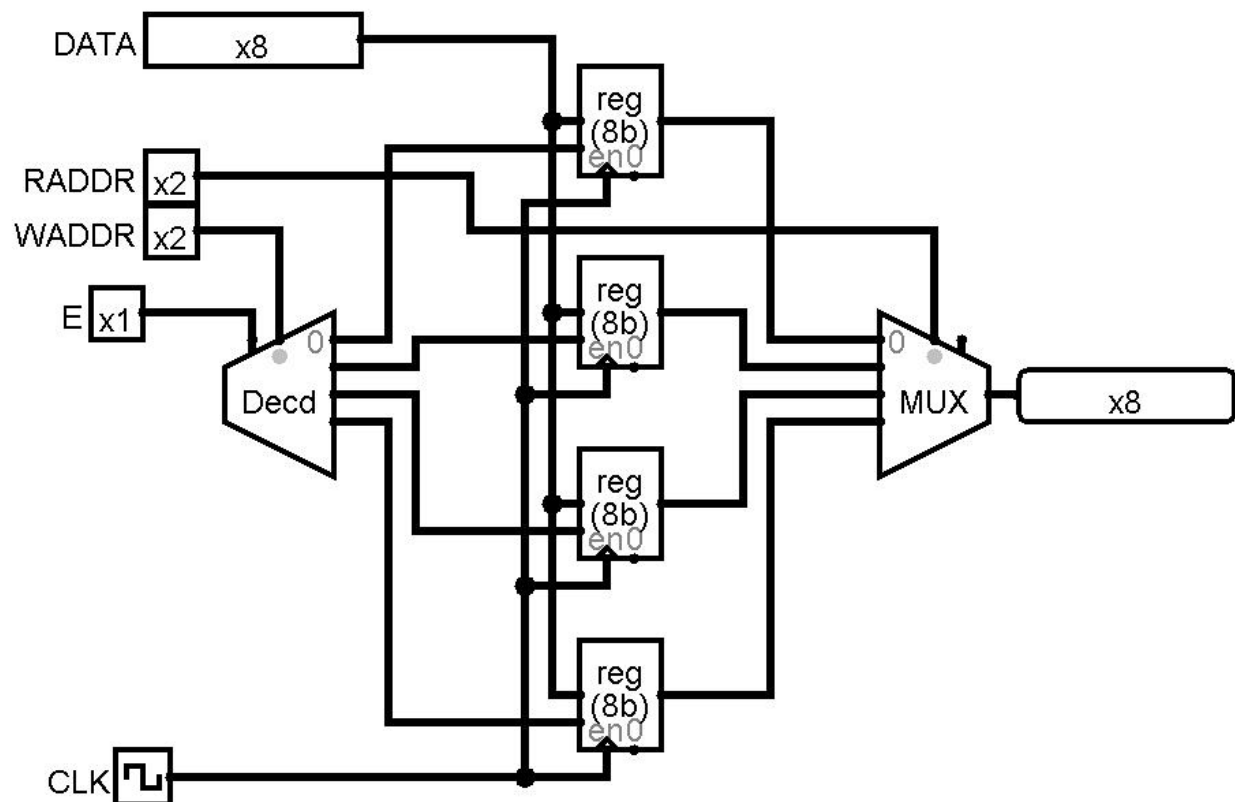
-Bảng mô phỏng

Cho A=00101100, B=00011101

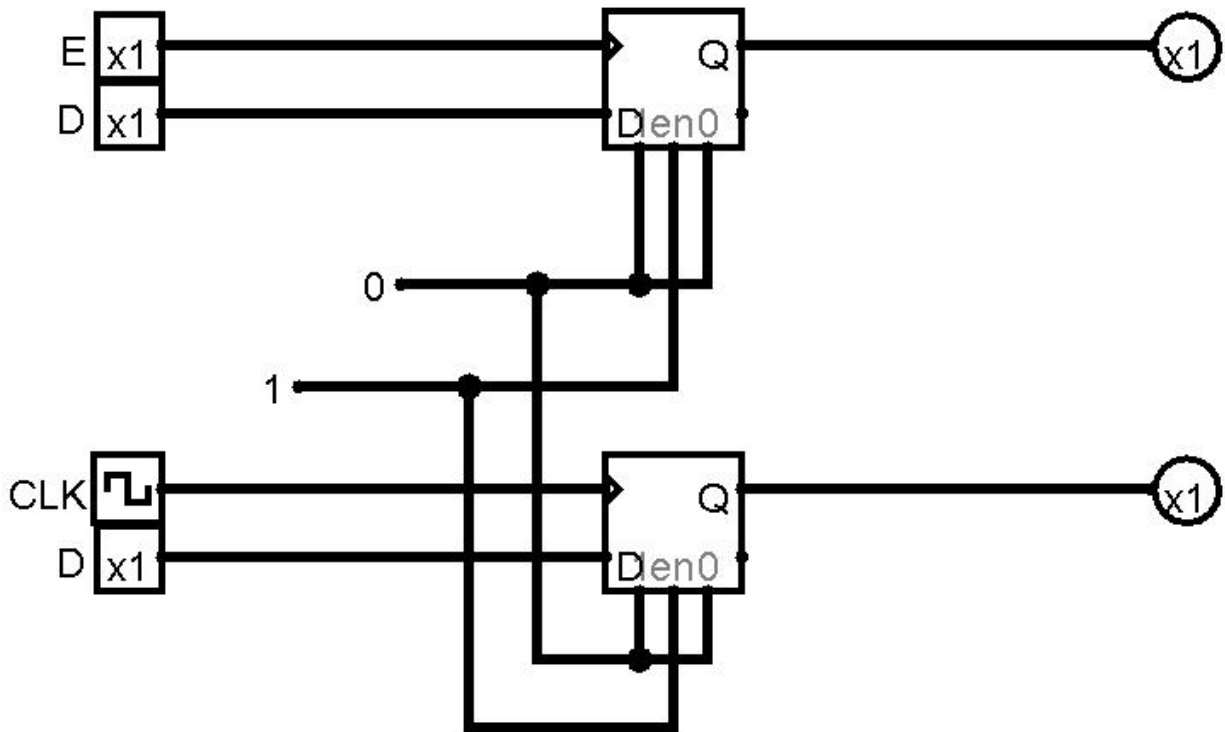
Thao tác	Kết quả
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A+B	01001001
A+1	00101011
A-B	00001111
A-1	00101101
A and B	00001100
A or B	00111101
Not A	11010011
A Xor B	00110001

3.2 Register Files với địa xuất riêng với địa chỉ ghi



4. Mô phỏng D-latch và D-fliplop



- D-Latch

E	Q+
0	Q
1	D

- D-Flipflop

CLK	Q+
-	Q
↑	D