Princess Sumaya University for Technology

Digital Electronics

Done by: *Supervisor:*

Leen Amr 20210258 NIS Eng. Dr. Khaldoon Mhaidat

ECL NOR/OR SPICE Simulation Project Report

May 23, 2024

Abstract

This report details the simulation of Emitter-Coupled Logic (ECL) NOR and OR gates using LTSpice. ECL is valued for its high-speed performance and low propagation delay, crucial for high-frequency applications. The project aims to design and analyze these gates, focusing on key parameters like propagation delay and power consumption. The report covers the design methodology, simulation setup, and results, showcasing LTSpice's effectiveness in modeling high-speed ECL circuits and offering insights into the practical applications of ECL technology in digital electronics.

Table of Contents

List of figures

1- Introduction

This project report focuses on the simulation of Emitter-Coupled Logic (ECL) NOR and OR gates using LTSpice, a leading tool for electronic circuit simulation. ECL is known for its high-speed performance and low propagation delay, making it ideal for applications requiring fast data processing. By simulating these logic gates in LTSpice, we aim to explore their operational characteristics, validate theoretical concepts, and measure key performance parameters such as propagation delay and power consumption. This report will detail the design process, simulation setup, and analysis of the results, providing insights into the efficiency and practicality of ECL technology in high-speed digital electronics.

2- Circuit Simulation on LTSpice

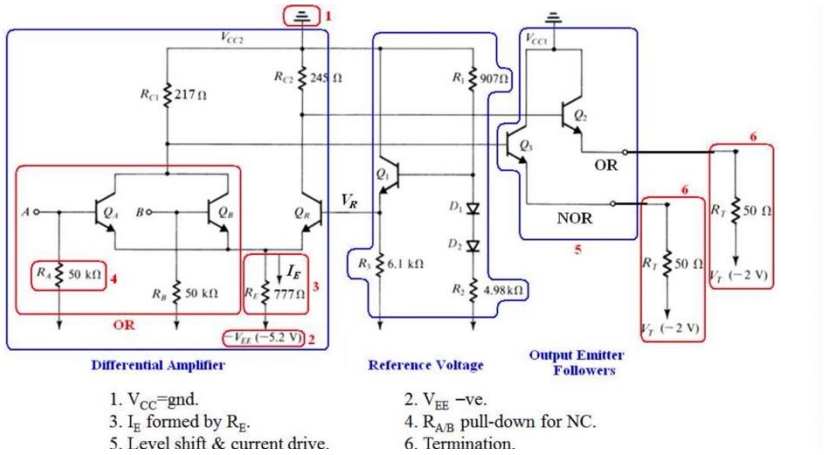


Figure 1: Circuit Schematic

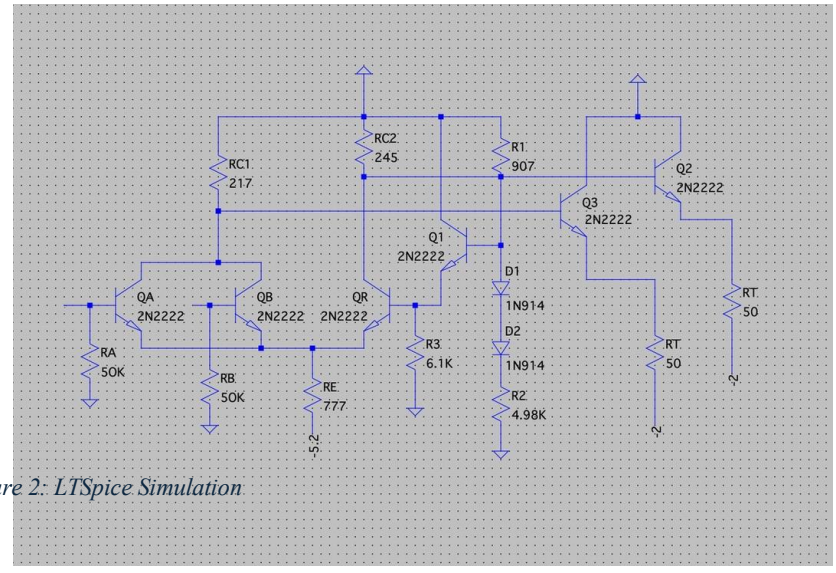
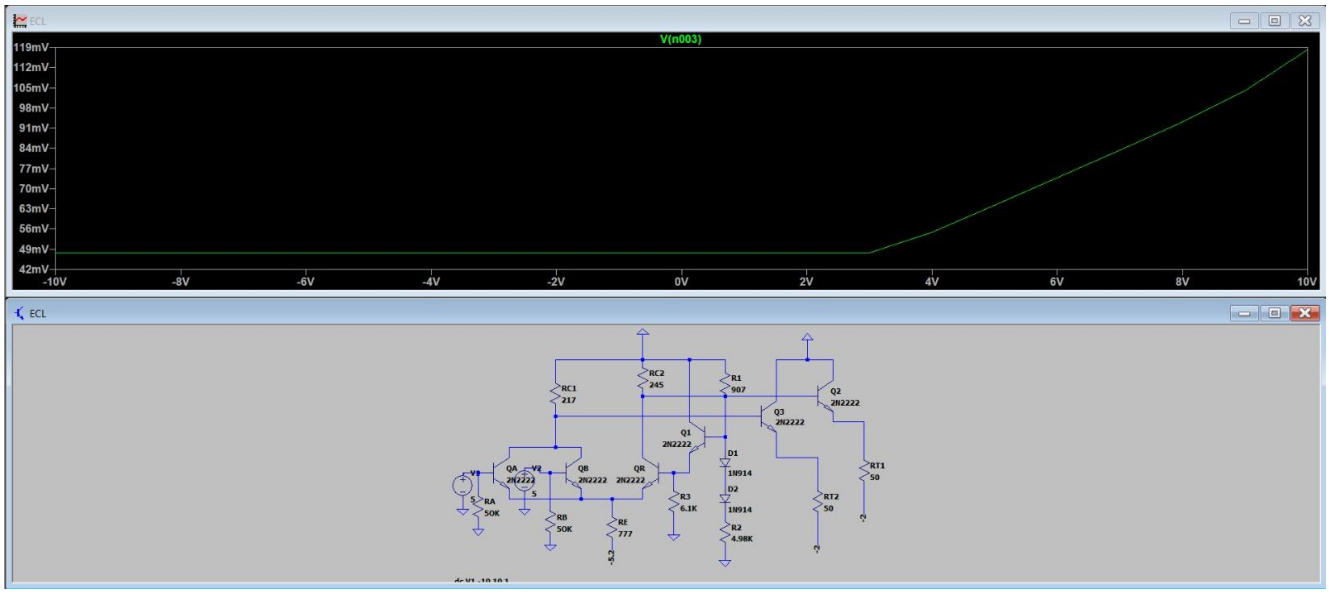
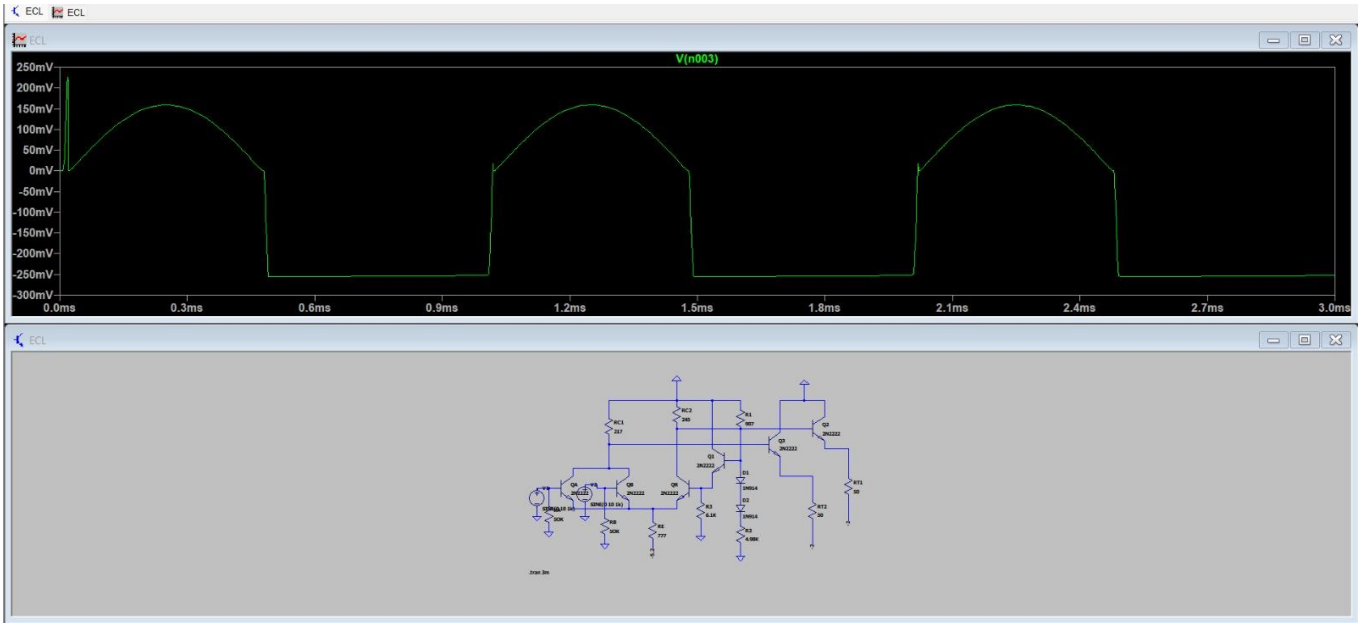


Figure 2: LTSpice Simulation

3- DC Sweep Analysis



4- Transient Analysis



5- Circuit Analysis and Calculations

3.1 Analysis:

Differential Amplifier:

• Two input transistors QA and QB with inputs A and B.

• A constant current source provided by IE formed by resistor RE and the voltage VEE.

Reference Voltage:

• Transistors QR and Q3 with resistors R1 and R2.

• Diodes D1 and D, to stabilize the voltage.

Output Emitter Followers:

• Transistors Q2 and Q4 forming the NOR and OR gates.

• Resistors R for output termination.

3.2 Calculations:

1. Differential Amplifier Calculations:

Given Values:

• RE = 777 Ω

• VEE = -5.2V

• RC1 = 217Ω

• RC2 = 245Ω

• VCC2 = 0V (Ground)

- Emitter Current (IE):

$$IE = \frac{VEE - VBE}{RE}$$

Assuming VBE ≈ 0.7V

$$IE = \frac{VEE - VBE}{RE} = \frac{-5.2V - 0.7V}{777\Omega} \approx -7.6mA$$

2. Reference Voltage Calculations:

Given Values:

• R1 = 907Ω

• R2 = 4.98kΩ

• Diodes: 1N914

- Reference Voltage (VR):

Assuming each diode forward voltage drop (VD) is approximately 0.7V,

VR = VD1 + VD2 = 0.7V + 0.7V = 1.4V

3. Output Emitter Calculations:

Given Values:

• RT = 50Ω

• Termination voltage (VT) = -2V

- Output Voltages:

For **NOR** gate output (VOUT (NOR)):

VOUT(NOR) = VR - VBE(Q4)

Assuming VBE(Q4) ≈ 0.7V,

VOUT (NOR) = 1.4V - 0.7V = 0.7V

For **OR** gate output (VOUT(OR)):

VOUT(OR) = VR - VBE(Q2)

Assuming VBE(Q4) ≈ 0.7V,

VOUT(OR) = 1.4V - 0.7V = 0.7V

6- Conclusion

The LTspice simulation of the NOR/OR Emitter-Coupled Logic (ECL) circuit was successfully executed using specified components and values, including the 2N2222 NPN transistor and 1N914 diode. Through DC sweep and transient analyses, critical voltages, propagation times, and rise/fall times were effectively measured and validated. The results confirmed the circuit's high-speed performance and functionality, demonstrating its reliability and efficiency in high-speed logic applications.