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| Gerb-BMSTU_01 | **Министерство науки и высшего образования Российской Федерации**  **Федеральное государственное бюджетное образовательное учреждение**  **высшего образования**  **«Московский государственный технический университет**  **имени Н.Э. Баумана**  **(национальный исследовательский университет)»**  **(МГТУ им. Н.Э. Баумана)** |

ФАКУЛЬТЕТ **Информатика и системы управления**

КАФЕДРА **Компьютерные системы и сети (ИУ6)**

НАПРАВЛЕНИЕ ПОДГОТОВКИ **09.03.04 ПРОГРАММНАЯ ИНЖЕНЕРИЯ**

**Отчет**

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| --- | --- |
| **по лабораторной работе №** | 4 |

**Название:**

Методология разработки и верификации ускорителей вычислений на платформе Xilinx Alveo

**Дисциплина:** Архитектура ЭВМ

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|  | (Группа) |  | (Подпись, дата) | (И.О. Фамилия) |
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|  |  |  | (Подпись, дата) | (И.О. Фамилия) |

Москва, 2021

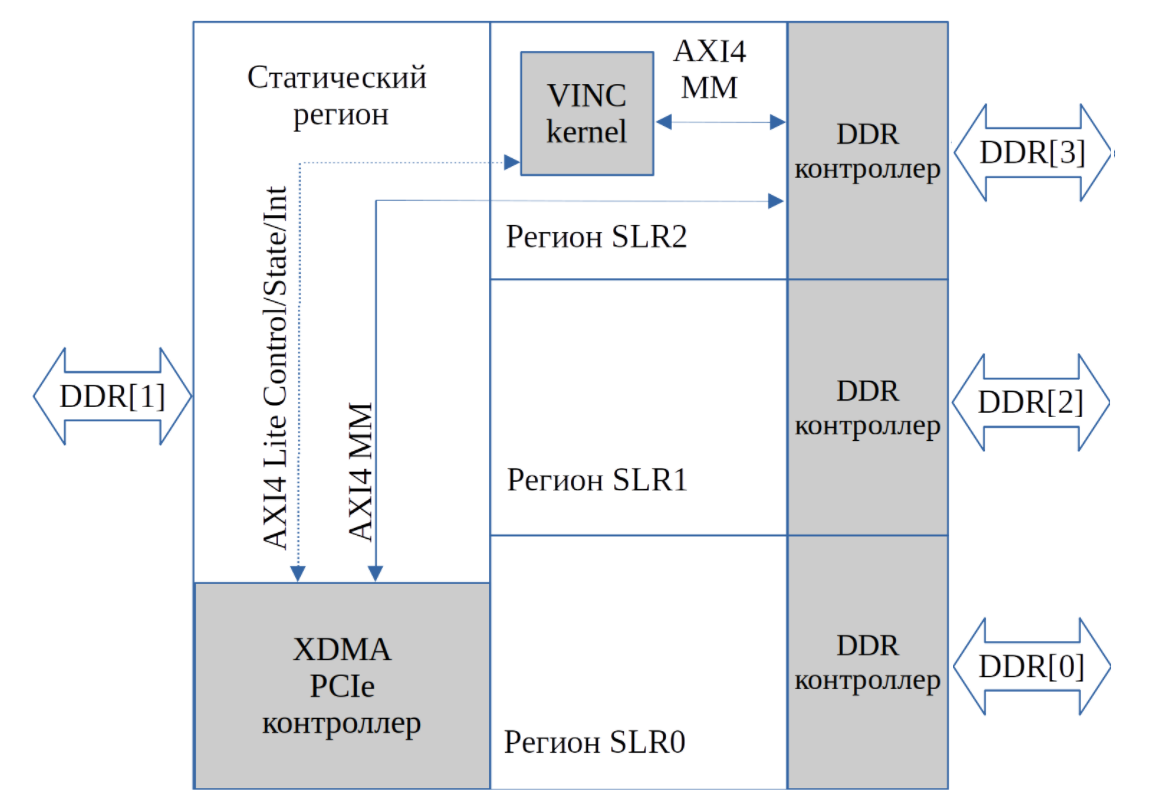
# Введение

Целью данной лабораторной работы является изучение архитектуры гетерогенных вычислительных систем и технологии разработки ускорителей вычислений на базе ПЛИС фирмы Xilinx.

Для достижения данной цели необходимо выполнить следующие задачи:

1. Изучить основные сведения о платформе Xilinx Alveo U200.
2. Разработать RTL описание ускорителя вычислений по индивидуальному варианту.
3. Выполнить генерацию ядра ускорителя.
4. Выполнить синтез и сборку бинарного модуля ускорителя.
5. Разработать и отладить тестирующее ПО на серверной хост-платформе.
6. Провести тесты работы ускорителя вычислений.

# Функциональная схема разрабатываемой аппаратной системы



# Изучение работы шины AXI

В данном разделе приведены диаграммы, иллюстрирующие процесс рукопожатия и пакетного чтения.

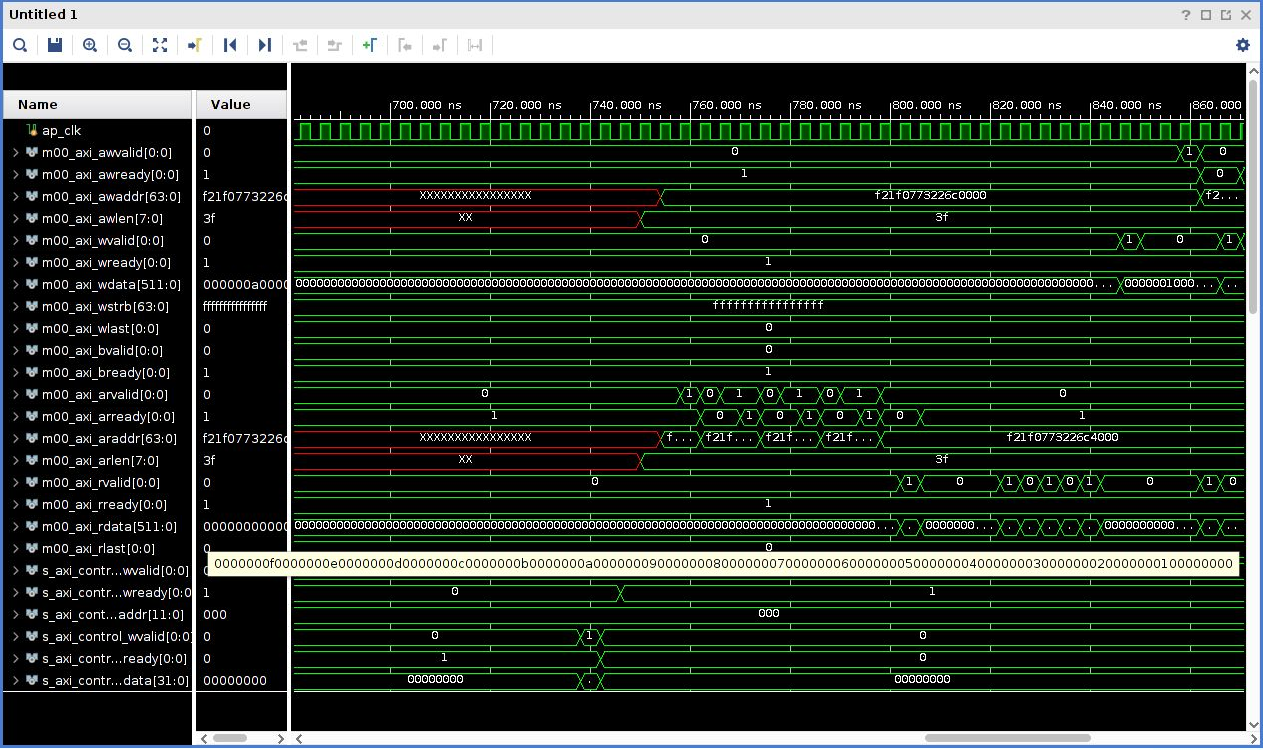


Рисунок . Транзакция чтения данных вектора на шине AXI4 MM из DDR памяти

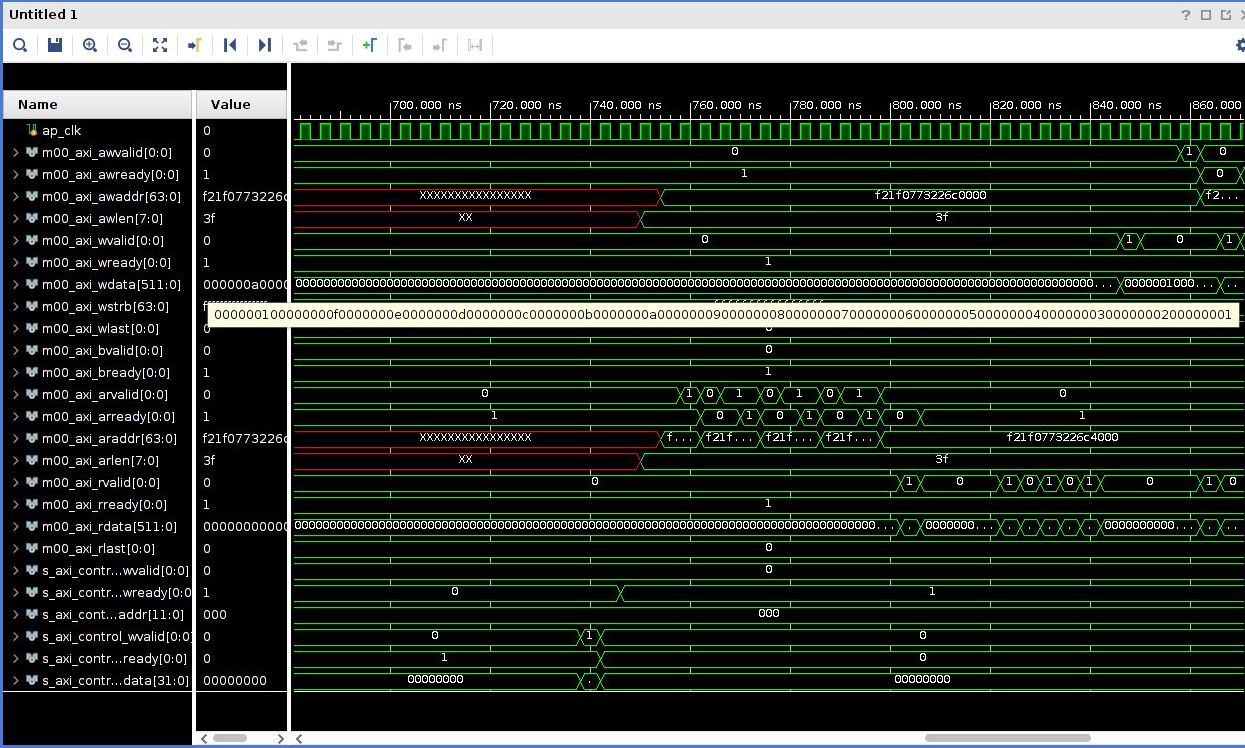


Рисунок . Транзакция записи результата инкремента данных на шине AXI4 MM

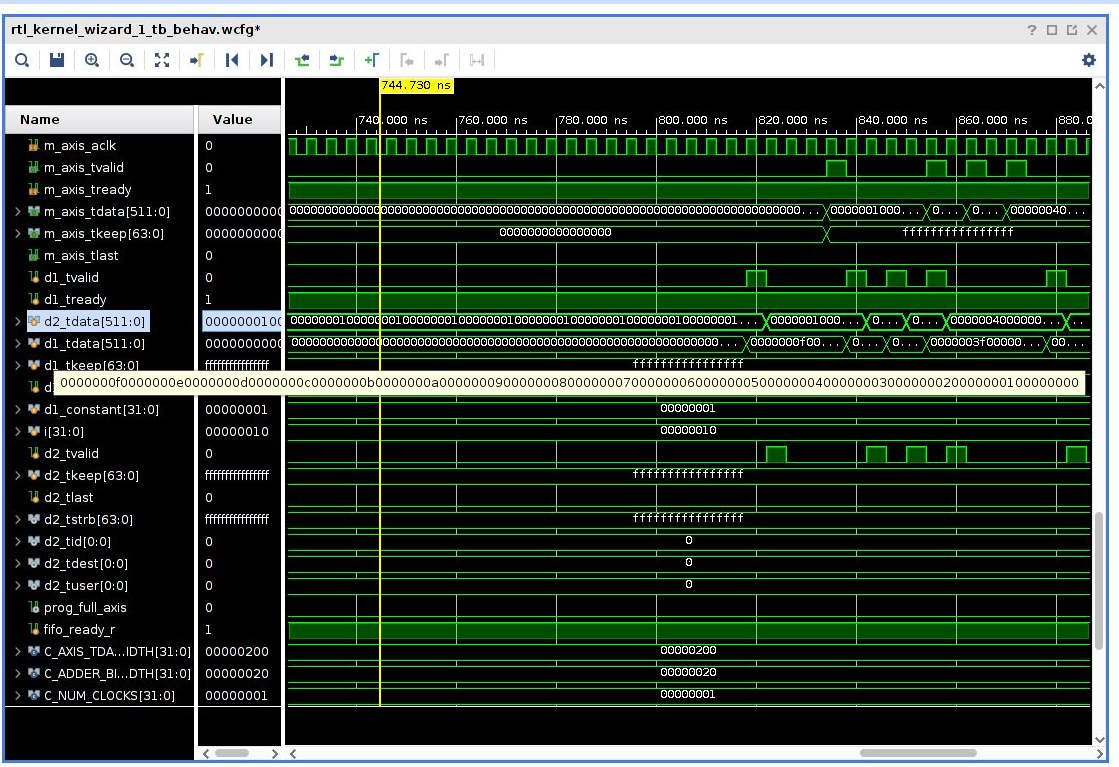


Рисунок . Инкремент данных

Теперь изменим модуль ***rtl\_kernel\_wizard\_0\_example\_adder.v***, чтобы ускоритель выполнял предложенную функцию:

Ниже представлен фрагмент листинга кода.

// Adder function

always @(posedge s\_axis\_aclk) begin

**for** (i = **0**; i < LP\_NUM\_LOOPS; i = i + **1**) begin

d2\_tdata[i\*C\_ADDER\_BIT\_WIDTH+:C\_ADDER\_BIT\_WIDTH] <= \

(d1\_tdata[C\_ADDER\_BIT\_WIDTH\*i+:C\_ADDER\_BIT\_WIDTH] + **10**) & (**255** << **8**);

end

end

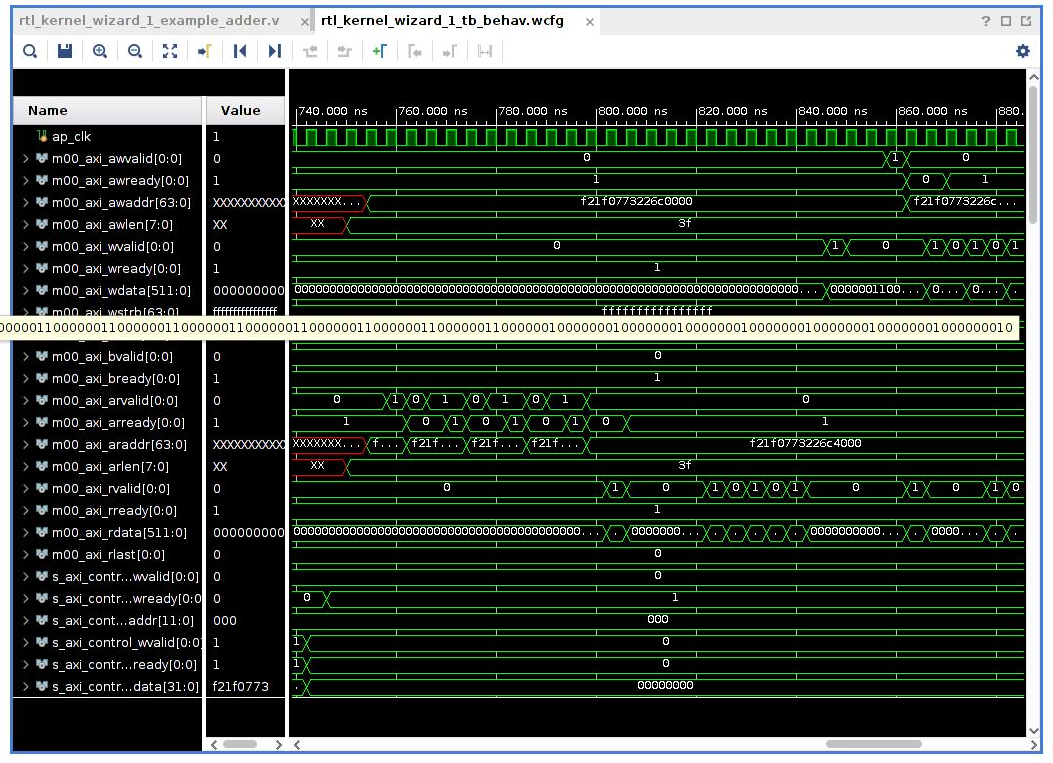


Рисунок . Транзакция чтения данных вектора на шине AXI4 MM из DDR памяти

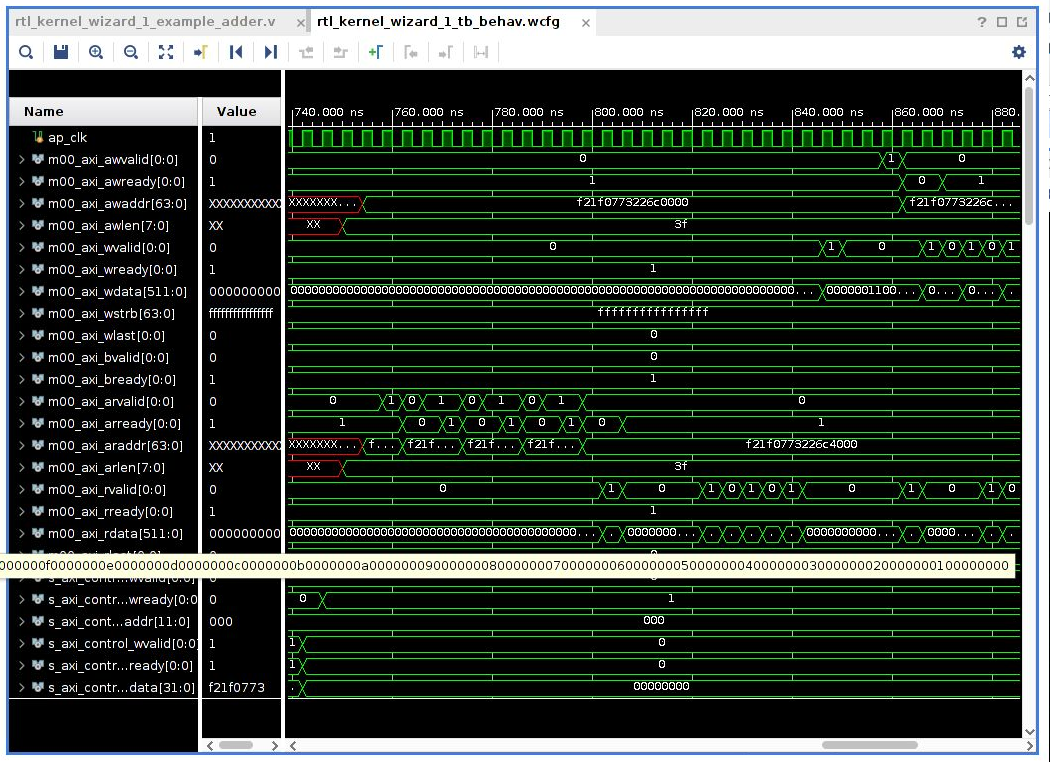


Рисунок . Транзакция записи результата инкремента данных на шине AXI4 MM

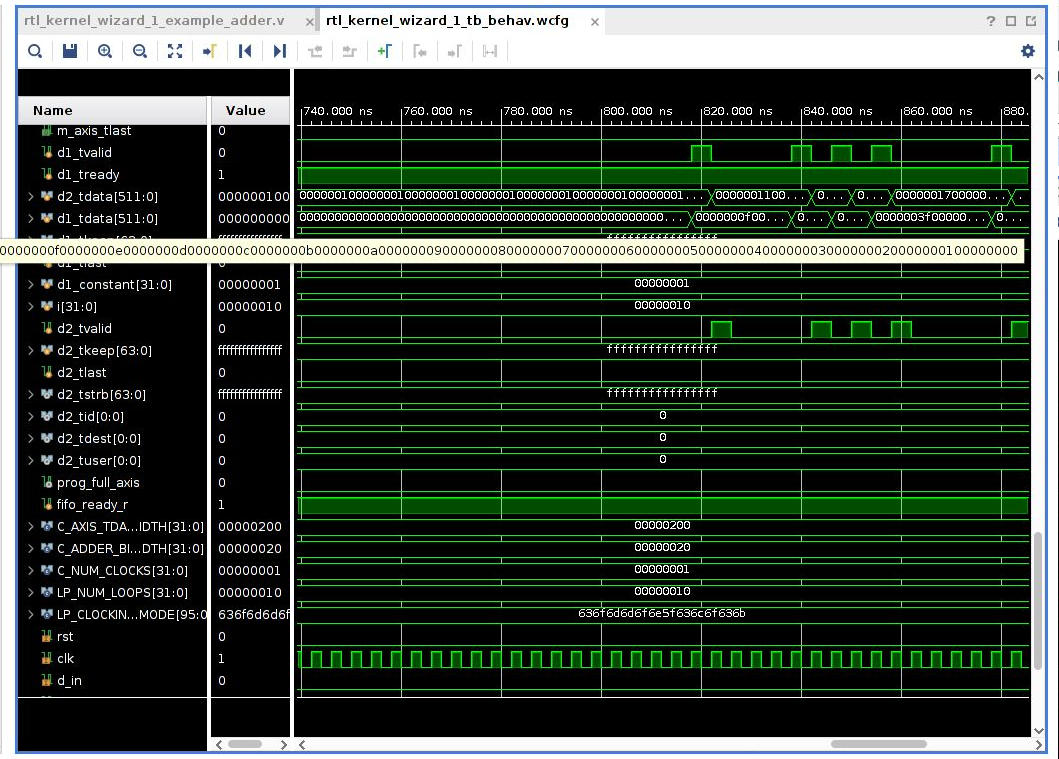


Рисунок . Инкремент данных

# Сборка проекта

Ниже приведено содержимое конфигурационного файла. В соответствии с вариантом требовалось использовать регионы SLR2, DDR[3].

[connectivity]

nk=rtl\_kernel\_wizard\_0:1:vinc0

slr=vinc0:SLR2

sp=vinc0.m00\_axi:DDR[3]

[vivado]

prop=run.impl\_1.STEPS.OPT\_DESIGN.ARGS.DIRECTIVE=Explore prop=run.impl\_1.STEPS.PLACE\_DESIGN.ARGS.DIRECTIVE=Explore prop=run.impl\_1.STEPS.PHYS\_OPT\_DESIGN.IS\_ENABLED=true prop=run.impl\_1.STEPS.PHYS\_OPT\_DESIGN.ARGS.DIRECTIVE=AggressiveExplore prop=run.impl\_1.STEPS.ROUTE\_DESIGN.ARGS.DIRECTIVE=Explore

# Содержимое xclbin.info

==============================================================================

XRT Build Version: 2.8.743 (2020.2)

Build Date: 2020-11-16 00:19:11

Hash ID: 77d5484b5c4daa691a7f78235053fb036829b1e9

==============================================================================

xclbin Information

------------------

Generated by: v++ (2020.2) on 2020-11-18-05:13:29

Version: 2.8.743

Kernels: rtl\_kernel\_wizard\_0

Signature:

Content: Bitstream

UUID (xclbin): 049e3bde-e4f4-4d57-98f8-43b540498a19

Sections: DEBUG\_IP\_LAYOUT, BITSTREAM, MEM\_TOPOLOGY, IP\_LAYOUT,

CONNECTIVITY, CLOCK\_FREQ\_TOPOLOGY, BUILD\_METADATA,

EMBEDDED\_METADATA, SYSTEM\_METADATA,

GROUP\_CONNECTIVITY, GROUP\_TOPOLOGY

==============================================================================

Hardware Platform (Shell) Information

-------------------------------------

Vendor: xilinx

Board: u200

Name: xdma

Version: 201830.2

Generated Version: Vivado 2018.3 (SW Build: 2568420)

Created: Tue Jun 25 06:55:20 2019

FPGA Device: xcu200

Board Vendor: xilinx.com

Board Name: xilinx.com:au200:1.0

Board Part: xilinx.com:au200:part0:1.0

Platform VBNV: xilinx\_u200\_xdma\_201830\_2

Static UUID: c102e7af-b2b8-4381-992b-9a00cc3863eb

Feature ROM TimeStamp: 1561465320

Clocks

------

Name: DATA\_CLK

Index: 0

Type: DATA

Frequency: 300 MHz

Name: KERNEL\_CLK

Index: 1

Type: KERNEL

Frequency: 500 MHz

Memory Configuration

--------------------

Name: bank0

Index: 0

Type: MEM\_DDR4

Base Address: 0x4000000000

Address Size: 0x400000000

Bank Used: No

Name: bank1

Index: 1

Type: MEM\_DDR4

Base Address: 0x5000000000

Address Size: 0x400000000

Bank Used: No

Name: bank2

Index: 2

Type: MEM\_DDR4

Base Address: 0x6000000000

Address Size: 0x400000000

Bank Used: No

Name: bank3

Index: 3

Type: MEM\_DDR4

Base Address: 0x7000000000

Address Size: 0x400000000

Bank Used: Yes

Name: PLRAM[0]

Index: 4

Type: MEM\_DRAM

Base Address: 0x3000000000

Address Size: 0x20000

Bank Used: No

Name: PLRAM[1]

Index: 5

Type: MEM\_DRAM

Base Address: 0x3000200000

Address Size: 0x20000

Bank Used: No

Name: PLRAM[2]

Index: 6

Type: MEM\_DRAM

Base Address: 0x3000400000

Address Size: 0x20000

Bank Used: No

==============================================================================

Kernel: rtl\_kernel\_wizard\_0

Definition

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Signature: rtl\_kernel\_wizard\_0 (uint scalar00, int\* axi00\_ptr0)

Ports

-----

Port: s\_axi\_control

Mode: slave

Range (bytes): 0x1000

Data Width: 32 bits

Port Type: addressable

Port: m00\_axi

Mode: master

Range (bytes): 0xFFFFFFFFFFFFFFFF

Data Width: 512 bits

Port Type: addressable

--------------------------

Instance: vinc0

Base Address: 0x1e00000

Argument: scalar00

Register Offset: 0x010

Port: s\_axi\_control

Memory: <not applicable>

Argument: axi00\_ptr0

Register Offset: 0x018

Port: m00\_axi

Memory: bank3 (MEM\_DDR4)

==============================================================================

Generated By

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Command: v++

Version: 2020.2 - 2020-11-18-05:13:29 (SW BUILD: 0)

Command Line: v++ --config /iu\_home/iu7158/workspace/Alveo\_lab1\_kernels/src/vitis\_rtl\_kernel/rtl\_kernel\_wizard\_0/myconf.cfg --connectivity.nk rtl\_kernel\_wizard\_0:1:vinc0 --connectivity.slr vinc0:SLR2 --connectivity.sp vinc0.m00\_axi:DDR[3] --input\_files /iu\_home/iu7158/workspace/Alveo\_lab1\_kernels/src/vitis\_rtl\_kernel/rtl\_kernel\_wizard\_0/rtl\_kernel\_wizard\_0.xo --link --optimize 0 --output /iu\_home/iu7158/workspace/Alveo\_lab1\_kernels/src/vitis\_rtl\_kernel/rtl\_kernel\_wizard\_0/vinc.xclbin --platform xilinx\_u200\_xdma\_201830\_2 --report\_level 0 --target hw --vivado.prop run.impl\_1.STEPS.OPT\_DESIGN.ARGS.DIRECTIVE=Explore --vivado.prop run.impl\_1.STEPS.PLACE\_DESIGN.ARGS.DIRECTIVE=Explore --vivado.prop run.impl\_1.STEPS.PHYS\_OPT\_DESIGN.IS\_ENABLED=true --vivado.prop run.impl\_1.STEPS.PHYS\_OPT\_DESIGN.ARGS.DIRECTIVE=AggressiveExplore --vivado.prop run.impl\_1.STEPS.ROUTE\_DESIGN.ARGS.DIRECTIVE=Explore

Options: --config /iu\_home/iu7158/workspace/Alveo\_lab1\_kernels/src/vitis\_rtl\_kernel/rtl\_kernel\_wizard\_0/myconf.cfg

--connectivity.nk rtl\_kernel\_wizard\_0:1:vinc0

--connectivity.slr vinc0:SLR2

--connectivity.sp vinc0.m00\_axi:DDR[3]

--input\_files /iu\_home/iu7158/workspace/Alveo\_lab1\_kernels/src/vitis\_rtl\_kernel/rtl\_kernel\_wizard\_0/rtl\_kernel\_wizard\_0.xo

--link

--optimize 0

--output /iu\_home/iu7158/workspace/Alveo\_lab1\_kernels/src/vitis\_rtl\_kernel/rtl\_kernel\_wizard\_0/vinc.xclbin

--platform xilinx\_u200\_xdma\_201830\_2

--report\_level 0

--target hw

--vivado.prop run.impl\_1.STEPS.OPT\_DESIGN.ARGS.DIRECTIVE=Explore

--vivado.prop run.impl\_1.STEPS.PLACE\_DESIGN.ARGS.DIRECTIVE=Explore

--vivado.prop run.impl\_1.STEPS.PHYS\_OPT\_DESIGN.IS\_ENABLED=true

--vivado.prop run.impl\_1.STEPS.PHYS\_OPT\_DESIGN.ARGS.DIRECTIVE=AggressiveExplore

--vivado.prop run.impl\_1.STEPS.ROUTE\_DESIGN.ARGS.DIRECTIVE=Explore

==============================================================================

User Added Key Value Pairs

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<empty>

==============================================================================

# Содержание v++\_vinc.log

INFO: [v++ 60-1306] Additional information associated with this v++ link can be found at:

Reports: /iu\_home/iu7158/\_x/reports/link

Log files: /iu\_home/iu7158/\_x/logs/link

INFO: [v++ 60-1548] Creating build summary session with primary output /iu\_home/iu7158/workspace/Alveo\_lab1\_kernels/src/vitis\_rtl\_kernel/rtl\_kernel\_wizard\_0/vinc.xclbin.link\_summary, at Mon Dec 20 21:26:52 2021

INFO: [v++ 60-1316] Initiating connection to rulecheck server, at Mon Dec 20 21:26:53 2021

INFO: [v++ 60-1315] Creating rulecheck session with output '/iu\_home/iu7158/\_x/reports/link/v++\_link\_vinc\_guidance.html', at Mon Dec 20 21:27:11 2021

INFO: [v++ 60-895] Target platform: /opt/xilinx/platforms/xilinx\_u200\_xdma\_201830\_2/xilinx\_u200\_xdma\_201830\_2.xpfm

INFO: [v++ 60-1578] This platform contains Device Support Archive '/opt/xilinx/platforms/xilinx\_u200\_xdma\_201830\_2/hw/xilinx\_u200\_xdma\_201830\_2.dsa'

INFO: [v++ 74-74] Compiler Version string: 2020.2

INFO: [v++ 60-1302] Platform 'xilinx\_u200\_xdma\_201830\_2.xpfm' has been explicitly enabled for this release.

INFO: [v++ 60-629] Linking for hardware target

INFO: [v++ 60-423] Target device: xilinx\_u200\_xdma\_201830\_2

INFO: [v++ 60-1332] Run 'run\_link' status: Not started

INFO: [v++ 60-1443] [21:28:14] Run run\_link: Step system\_link: Started

INFO: [v++ 60-1453] Command Line: system\_link --xo /iu\_home/iu7158/workspace/Alveo\_lab1\_kernels/src/vitis\_rtl\_kernel/rtl\_kernel\_wizard\_0/rtl\_kernel\_wizard\_0.xo --config /iu\_home/iu7158/\_x/link/int/syslinkConfig.ini --xpfm /opt/xilinx/platforms/xilinx\_u200\_xdma\_201830\_2/xilinx\_u200\_xdma\_201830\_2.xpfm --target hw --output\_dir /iu\_home/iu7158/\_x/link/int --temp\_dir /iu\_home/iu7158/\_x/link/sys\_link

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7158/\_x/link/run\_link

INFO: [SYSTEM\_LINK 60-1316] Initiating connection to rulecheck server, at Mon Dec 20 21:28:28 2021

INFO: [SYSTEM\_LINK 82-70] Extracting xo v3 file /iu\_home/iu7158/workspace/Alveo\_lab1\_kernels/src/vitis\_rtl\_kernel/rtl\_kernel\_wizard\_0/rtl\_kernel\_wizard\_0.xo

INFO: [SYSTEM\_LINK 82-53] Creating IP database /iu\_home/iu7158/\_x/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml

INFO: [SYSTEM\_LINK 82-38] [21:28:37] build\_xd\_ip\_db started: /data/Xilinx/Vitis/2020.2/bin/build\_xd\_ip\_db -ip\_search 0 -sds-pf /iu\_home/iu7158/\_x/link/sys\_link/xilinx\_u200\_xdma\_201830\_2.hpfm -clkid 0 -ip /iu\_home/iu7158/\_x/link/sys\_link/iprepo/mycompany\_com\_kernel\_rtl\_kernel\_wizard\_0\_1\_0,rtl\_kernel\_wizard\_0 -o /iu\_home/iu7158/\_x/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml

INFO: [SYSTEM\_LINK 82-37] [21:29:14] build\_xd\_ip\_db finished successfully

Time (s): cpu = 00:00:26 ; elapsed = 00:00:37 . Memory (MB): peak = 1557.895 ; gain = 0.000 ; free physical = 126921 ; free virtual = 184943

INFO: [SYSTEM\_LINK 82-51] Create system connectivity graph

INFO: [SYSTEM\_LINK 82-102] Applying explicit connections to the system connectivity graph: /iu\_home/iu7158/\_x/link/sys\_link/cfgraph/cfgen\_cfgraph.xml

INFO: [SYSTEM\_LINK 82-38] [21:29:14] cfgen started: /data/Xilinx/Vitis/2020.2/bin/cfgen -nk rtl\_kernel\_wizard\_0:1:vinc0 -slr vinc0:SLR2 -sp vinc0.m00\_axi:DDR[3] -dmclkid 0 -r /iu\_home/iu7158/\_x/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml -o /iu\_home/iu7158/\_x/link/sys\_link/cfgraph/cfgen\_cfgraph.xml

INFO: [CFGEN 83-0] Kernel Specs:

INFO: [CFGEN 83-0] kernel: rtl\_kernel\_wizard\_0, num: 1 {vinc0}

INFO: [CFGEN 83-0] Port Specs:

INFO: [CFGEN 83-0] kernel: vinc0, k\_port: m00\_axi, sptag: DDR[3]

INFO: [CFGEN 83-0] SLR Specs:

INFO: [CFGEN 83-0] instance: vinc0, SLR: SLR2

INFO: [CFGEN 83-2228] Creating mapping for argument vinc0.axi00\_ptr0 to DDR[3] for directive vinc0.m00\_axi:DDR[3]

INFO: [SYSTEM\_LINK 82-37] [21:29:39] cfgen finished successfully

Time (s): cpu = 00:00:23 ; elapsed = 00:00:25 . Memory (MB): peak = 1557.895 ; gain = 0.000 ; free physical = 127057 ; free virtual = 185099

INFO: [SYSTEM\_LINK 82-52] Create top-level block diagram

INFO: [SYSTEM\_LINK 82-38] [21:29:39] cf2bd started: /data/Xilinx/Vitis/2020.2/bin/cf2bd --linux --trace\_buffer 1024 --input\_file /iu\_home/iu7158/\_x/link/sys\_link/cfgraph/cfgen\_cfgraph.xml --ip\_db /iu\_home/iu7158/\_x/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml --cf\_name dr --working\_dir /iu\_home/iu7158/\_x/link/sys\_link/\_sysl/.xsd --temp\_dir /iu\_home/iu7158/\_x/link/sys\_link --output\_dir /iu\_home/iu7158/\_x/link/int --target\_bd pfm\_dynamic.bd

INFO: [CF2BD 82-31] Launching cf2xd: cf2xd -linux -trace-buffer 1024 -i /iu\_home/iu7158/\_x/link/sys\_link/cfgraph/cfgen\_cfgraph.xml -r /iu\_home/iu7158/\_x/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml -o dr.xml

INFO: [CF2BD 82-28] cf2xd finished successfully

INFO: [CF2BD 82-31] Launching cf\_xsd: cf\_xsd -disable-address-gen -bd pfm\_dynamic.bd -dn dr -dp /iu\_home/iu7158/\_x/link/sys\_link/\_sysl/.xsd

INFO: [CF2BD 82-28] cf\_xsd finished successfully

INFO: [SYSTEM\_LINK 82-37] [21:29:54] cf2bd finished successfully

Time (s): cpu = 00:00:11 ; elapsed = 00:00:15 . Memory (MB): peak = 1557.895 ; gain = 0.000 ; free physical = 127369 ; free virtual = 185420

INFO: [v++ 60-1441] [21:29:55] Run run\_link: Step system\_link: Completed

Time (s): cpu = 00:01:18 ; elapsed = 00:01:41 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 127395 ; free virtual = 185442

INFO: [v++ 60-1443] [21:29:55] Run run\_link: Step cf2sw: Started

INFO: [v++ 60-1453] Command Line: cf2sw -sdsl /iu\_home/iu7158/\_x/link/int/sdsl.dat -rtd /iu\_home/iu7158/\_x/link/int/cf2sw.rtd -nofilter /iu\_home/iu7158/\_x/link/int/cf2sw\_full.rtd -xclbin /iu\_home/iu7158/\_x/link/int/xclbin\_orig.xml -o /iu\_home/iu7158/\_x/link/int/xclbin\_orig.1.xml

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7158/\_x/link/run\_link

INFO: [v++ 60-1441] [21:30:11] Run run\_link: Step cf2sw: Completed

Time (s): cpu = 00:00:14 ; elapsed = 00:00:16 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 127526 ; free virtual = 185572

INFO: [v++ 60-1443] [21:30:11] Run run\_link: Step rtd2\_system\_diagram: Started

INFO: [v++ 60-1453] Command Line: rtd2SystemDiagram

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7158/\_x/link/run\_link

INFO: [v++ 60-1441] [21:30:21] Run run\_link: Step rtd2\_system\_diagram: Completed

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:10 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 127541 ; free virtual = 185570

INFO: [v++ 60-1443] [21:30:21] Run run\_link: Step vpl: Started

INFO: [v++ 60-1453] Command Line: vpl -t hw -f xilinx\_u200\_xdma\_201830\_2 --remote\_ip\_cache /iu\_home/iu7158/.ipcache --output\_dir /iu\_home/iu7158/\_x/link/int --log\_dir /iu\_home/iu7158/\_x/logs/link --report\_dir /iu\_home/iu7158/\_x/reports/link --config /iu\_home/iu7158/\_x/link/int/vplConfig.ini -k /iu\_home/iu7158/\_x/link/int/kernel\_info.dat --webtalk\_flag Vitis --temp\_dir /iu\_home/iu7158/\_x/link --no-info --iprepo /iu\_home/iu7158/\_x/link/int/xo/ip\_repo/mycompany\_com\_kernel\_rtl\_kernel\_wizard\_0\_1\_0 --messageDb /iu\_home/iu7158/\_x/link/run\_link/vpl.pb /iu\_home/iu7158/\_x/link/int/dr.bd.tcl

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7158/\_x/link/run\_link

\*\*\*\*\*\* vpl v2020.2 (64-bit)

\*\*\*\* SW Build (by xbuild) on 2020-11-18-05:13:29

\*\* Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.

INFO: [VPL 60-839] Read in kernel information from file '/iu\_home/iu7158/\_x/link/int/kernel\_info.dat'.

INFO: [VPL 74-74] Compiler Version string: 2020.2

INFO: [VPL 60-423] Target device: xilinx\_u200\_xdma\_201830\_2

INFO: [VPL 60-1032] Extracting hardware platform to /iu\_home/iu7158/\_x/link/vivado/vpl/.local/hw\_platform

WARNING: /data/Xilinx/Vitis/2020.2/tps/lnx64/jre9.0.4 does not exist.

[21:40:19] Run vpl: Step create\_project: Started

Creating Vivado project.

[21:40:45] Run vpl: Step create\_project: Completed

[21:40:45] Run vpl: Step create\_bd: Started

[21:44:27] Run vpl: Step create\_bd: RUNNING...

[21:50:38] Run vpl: Step create\_bd: RUNNING...

[21:54:07] Run vpl: Step create\_bd: RUNNING...

[21:58:50] Run vpl: Step create\_bd: RUNNING...

[22:01:24] Run vpl: Step create\_bd: RUNNING...

[22:03:10] Run vpl: Step create\_bd: Completed

[22:03:10] Run vpl: Step update\_bd: Started

[22:03:14] Run vpl: Step update\_bd: Completed

[22:03:14] Run vpl: Step generate\_target: Started

[22:06:46] Run vpl: Step generate\_target: RUNNING...

[22:09:35] Run vpl: Step generate\_target: RUNNING...

[22:14:07] Run vpl: Step generate\_target: RUNNING...

[22:16:22] Run vpl: Step generate\_target: RUNNING...

[22:17:19] Run vpl: Step generate\_target: Completed

[22:17:19] Run vpl: Step config\_hw\_runs: Started

[22:20:01] Run vpl: Step config\_hw\_runs: Completed

[22:20:01] Run vpl: Step synth: Started

[22:23:31] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[22:24:42] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[22:26:18] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[22:27:44] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[22:28:52] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[22:30:06] Block-level synthesis in progress, 4 of 66 jobs complete, 4 jobs running.

[22:31:32] Block-level synthesis in progress, 6 of 66 jobs complete, 7 jobs running.

[22:33:12] Block-level synthesis in progress, 10 of 66 jobs complete, 4 jobs running.

[22:34:26] Block-level synthesis in progress, 11 of 66 jobs complete, 7 jobs running.

[22:35:52] Block-level synthesis in progress, 13 of 66 jobs complete, 6 jobs running.

[22:36:40] Block-level synthesis in progress, 13 of 66 jobs complete, 8 jobs running.

[22:37:37] Block-level synthesis in progress, 14 of 66 jobs complete, 7 jobs running.

[22:38:34] Block-level synthesis in progress, 15 of 66 jobs complete, 7 jobs running.

[22:39:27] Block-level synthesis in progress, 17 of 66 jobs complete, 5 jobs running.

[22:40:44] Block-level synthesis in progress, 17 of 66 jobs complete, 8 jobs running.

[22:41:25] Block-level synthesis in progress, 19 of 66 jobs complete, 6 jobs running.

[22:42:24] Block-level synthesis in progress, 19 of 66 jobs complete, 8 jobs running.

[22:44:23] Block-level synthesis in progress, 21 of 66 jobs complete, 6 jobs running.

[22:45:42] Block-level synthesis in progress, 21 of 66 jobs complete, 8 jobs running.

[22:47:01] Block-level synthesis in progress, 23 of 66 jobs complete, 7 jobs running.

[22:48:12] Block-level synthesis in progress, 26 of 66 jobs complete, 5 jobs running.

[22:49:21] Block-level synthesis in progress, 27 of 66 jobs complete, 7 jobs running.

[22:50:50] Block-level synthesis in progress, 29 of 66 jobs complete, 6 jobs running.

[22:52:04] Block-level synthesis in progress, 30 of 66 jobs complete, 7 jobs running.

[22:53:10] Block-level synthesis in progress, 32 of 66 jobs complete, 6 jobs running.

[22:54:27] Block-level synthesis in progress, 32 of 66 jobs complete, 8 jobs running.

[22:55:24] Block-level synthesis in progress, 33 of 66 jobs complete, 7 jobs running.

[22:56:03] Block-level synthesis in progress, 34 of 66 jobs complete, 6 jobs running.

[22:57:01] Block-level synthesis in progress, 36 of 66 jobs complete, 5 jobs running.

[22:57:43] Block-level synthesis in progress, 37 of 66 jobs complete, 6 jobs running.

[22:58:34] Block-level synthesis in progress, 38 of 66 jobs complete, 7 jobs running.

[22:59:15] Block-level synthesis in progress, 38 of 66 jobs complete, 7 jobs running.

[23:00:10] Block-level synthesis in progress, 40 of 66 jobs complete, 6 jobs running.

[23:00:52] Block-level synthesis in progress, 41 of 66 jobs complete, 6 jobs running.

[23:02:00] Block-level synthesis in progress, 43 of 66 jobs complete, 6 jobs running.

[23:03:14] Block-level synthesis in progress, 43 of 66 jobs complete, 8 jobs running.

[23:04:36] Block-level synthesis in progress, 43 of 66 jobs complete, 8 jobs running.

[23:05:11] Block-level synthesis in progress, 43 of 66 jobs complete, 8 jobs running.

[23:06:12] Block-level synthesis in progress, 46 of 66 jobs complete, 5 jobs running.

[23:07:19] Block-level synthesis in progress, 46 of 66 jobs complete, 8 jobs running.

[23:08:10] Block-level synthesis in progress, 47 of 66 jobs complete, 7 jobs running.

[23:08:59] Block-level synthesis in progress, 49 of 66 jobs complete, 5 jobs running.

[23:09:45] Block-level synthesis in progress, 49 of 66 jobs complete, 7 jobs running.

[23:10:29] Block-level synthesis in progress, 50 of 66 jobs complete, 7 jobs running.

[23:11:14] Block-level synthesis in progress, 50 of 66 jobs complete, 8 jobs running.

[23:11:59] Block-level synthesis in progress, 50 of 66 jobs complete, 8 jobs running.

[23:12:41] Block-level synthesis in progress, 51 of 66 jobs complete, 7 jobs running.

[23:13:33] Block-level synthesis in progress, 52 of 66 jobs complete, 7 jobs running.

[23:14:14] Block-level synthesis in progress, 53 of 66 jobs complete, 7 jobs running.

[23:15:07] Block-level synthesis in progress, 53 of 66 jobs complete, 8 jobs running.

[23:16:05] Block-level synthesis in progress, 54 of 66 jobs complete, 7 jobs running.

[23:16:45] Block-level synthesis in progress, 55 of 66 jobs complete, 6 jobs running.

[23:17:34] Block-level synthesis in progress, 56 of 66 jobs complete, 7 jobs running.

[23:19:43] Block-level synthesis in progress, 57 of 66 jobs complete, 7 jobs running.

[23:21:42] Block-level synthesis in progress, 60 of 66 jobs complete, 5 jobs running.

[23:23:18] Block-level synthesis in progress, 61 of 66 jobs complete, 4 jobs running.

[23:24:34] Block-level synthesis in progress, 61 of 66 jobs complete, 4 jobs running.

[23:26:03] Block-level synthesis in progress, 61 of 66 jobs complete, 4 jobs running.

[23:27:12] Block-level synthesis in progress, 61 of 66 jobs complete, 4 jobs running.

[23:28:02] Block-level synthesis in progress, 62 of 66 jobs complete, 3 jobs running.

[23:28:44] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[23:29:36] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[23:30:25] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[23:31:42] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[23:32:44] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[23:33:32] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[23:34:28] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[23:35:07] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[23:36:02] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[23:36:46] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[23:37:39] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[23:38:24] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[23:39:20] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[23:40:02] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[23:40:58] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[23:41:43] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:42:34] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:43:12] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:44:00] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:44:39] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:45:32] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:46:13] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:47:13] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:47:53] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:48:49] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:49:29] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:50:20] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:51:07] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:52:01] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:52:38] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:53:34] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:54:19] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:55:11] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:55:51] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:57:08] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:58:11] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[23:58:59] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[00:00:05] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[00:01:17] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[00:02:20] Block-level synthesis in progress, 65 of 66 jobs complete, 0 jobs running.

[00:03:47] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[00:05:21] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[00:06:46] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[00:07:57] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[00:09:00] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[00:10:02] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[00:10:42] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[00:11:30] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[00:12:13] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[00:13:07] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[00:13:48] Block-level synthesis in progress, 66 of 66 jobs complete, 0 jobs running.

[00:14:45] Top-level synthesis in progress.

[00:15:27] Top-level synthesis in progress.

[00:16:23] Top-level synthesis in progress.

[00:17:03] Top-level synthesis in progress.

[00:17:55] Top-level synthesis in progress.

[00:18:35] Top-level synthesis in progress.

[00:19:25] Top-level synthesis in progress.

[00:20:10] Top-level synthesis in progress.

[00:20:53] Top-level synthesis in progress.

[00:21:32] Top-level synthesis in progress.

[00:22:27] Top-level synthesis in progress.

[00:23:06] Top-level synthesis in progress.

[00:24:01] Top-level synthesis in progress.

[00:25:03] Run vpl: Step synth: Completed

[00:25:03] Run vpl: Step impl: Started

[01:19:17] Finished 2nd of 6 tasks (FPGA linking synthesized kernels to platform). Elapsed time: 03h 48m 45s

[01:19:17] Starting logic optimization..

[01:25:40] Phase 1 Generate And Synthesize MIG Cores

[02:00:09] Phase 2 Generate And Synthesize Debug Cores

[02:25:21] Phase 3 Retarget

[02:28:04] Phase 4 Constant propagation

[02:29:25] Phase 5 Sweep

[02:35:31] Phase 6 BUFG optimization

[02:36:59] Phase 7 Shift Register Optimization

[02:38:25] Phase 8 Post Processing Netlist

[02:54:06] Finished 3rd of 6 tasks (FPGA logic optimization). Elapsed time: 01h 34m 48s

[02:54:06] Starting logic placement..

[02:59:36] Phase 1 Placer Initialization

[02:59:36] Phase 1.1 Placer Initialization Netlist Sorting

[03:13:34] Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

[03:23:46] Phase 1.3 Build Placer Netlist Model

[03:36:57] Phase 1.4 Constrain Clocks/Macros

[03:38:16] Phase 2 Global Placement

[03:38:16] Phase 2.1 Floorplanning

[03:42:17] Phase 2.1.1 Partition Driven Placement

[03:42:17] Phase 2.1.1.1 PBP: Partition Driven Placement

[03:44:17] Phase 2.1.1.2 PBP: Clock Region Placement

[03:49:07] Phase 2.1.1.3 PBP: Compute Congestion

[03:49:07] Phase 2.1.1.4 PBP: UpdateTiming

[03:51:59] Phase 2.1.1.5 PBP: Add part constraints

[03:52:40] Phase 2.2 Update Timing before SLR Path Opt

[03:52:40] Phase 2.3 Global Placement Core

[04:26:49] Phase 2.3.1 Physical Synthesis In Placer

[04:39:47] Phase 3 Detail Placement

[04:39:47] Phase 3.1 Commit Multi Column Macros

[04:40:25] Phase 3.2 Commit Most Macros & LUTRAMs

[04:46:00] Phase 3.3 Small Shape DP

[04:46:00] Phase 3.3.1 Small Shape Clustering

[04:48:51] Phase 3.3.2 Flow Legalize Slice Clusters

[04:48:51] Phase 3.3.3 Slice Area Swap

[04:53:39] Phase 3.4 Place Remaining

[04:54:19] Phase 3.5 Re-assign LUT pins

[04:56:24] Phase 3.6 Pipeline Register Optimization

[04:56:24] Phase 3.7 Fast Optimization

[05:01:01] Phase 4 Post Placement Optimization and Clean-Up

[05:01:01] Phase 4.1 Post Commit Optimization

[05:11:20] Phase 4.1.1 Post Placement Optimization

[05:12:02] Phase 4.1.1.1 BUFG Insertion

[05:12:02] Phase 1 Physical Synthesis Initialization

[05:14:46] Phase 4.1.1.2 BUFG Replication

[05:19:58] Phase 4.1.1.3 Replication

[05:26:33] Phase 4.2 Post Placement Cleanup

[05:27:55] Phase 4.3 Placer Reporting

[05:27:55] Phase 4.3.1 Print Estimated Congestion

[05:29:17] Phase 4.4 Final Placement Cleanup

[06:36:34] Finished 4th of 6 tasks (FPGA logic placement). Elapsed time: 03h 42m 28s

[06:36:34] Starting logic routing..

[06:42:45] Phase 1 Build RT Design

[06:54:11] Phase 2 Router Initialization

[06:54:11] Phase 2.1 Fix Topology Constraints

[06:54:53] Phase 2.2 Pre Route Cleanup

[06:55:32] Phase 2.3 Global Clock Net Routing

[06:57:34] Phase 2.4 Update Timing

[07:10:38] Phase 2.5 Update Timing for Bus Skew

[07:10:38] Phase 2.5.1 Update Timing

[07:15:25] Phase 3 Initial Routing

[07:15:25] Phase 3.1 Global Routing

[07:20:54] Phase 4 Rip-up And Reroute

[07:20:54] Phase 4.1 Global Iteration 0

[07:43:48] Phase 4.2 Global Iteration 1

[07:48:33] Phase 4.3 Global Iteration 2

[07:53:55] Phase 5 Delay and Skew Optimization

[07:53:55] Phase 5.1 Delay CleanUp

[07:53:55] Phase 5.1.1 Update Timing

[08:00:06] Phase 5.2 Clock Skew Optimization

[08:00:06] Phase 6 Post Hold Fix

[08:00:06] Phase 6.1 Hold Fix Iter

[08:00:06] Phase 6.1.1 Update Timing

[08:04:49] Phase 7 Route finalize

[08:05:29] Phase 8 Verifying routed nets

[08:06:10] Phase 9 Depositing Routes

[08:09:38] Phase 10 Route finalize

[08:10:17] Phase 11 Post Router Timing

[08:16:28] Finished 5th of 6 tasks (FPGA routing). Elapsed time: 01h 39m 53s

[08:16:28] Starting bitstream generation..

[10:02:34] Creating bitmap...

[10:48:29] Writing bitstream ./pfm\_top\_i\_dynamic\_region\_my\_rm\_partial.bit...

[10:48:29] Finished 6th of 6 tasks (FPGA bitstream generation). Elapsed time: 02h 32m 01s

[10:52:50] Run vpl: Step impl: Completed

[10:52:58] Run vpl: FINISHED. Run Status: impl Complete!

INFO: [v++ 60-1441] [10:53:26] Run run\_link: Step vpl: Completed

Time (s): cpu = 00:49:34 ; elapsed = 13:23:05 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 79863 ; free virtual = 180402

INFO: [v++ 60-1443] [10:53:26] Run run\_link: Step rtdgen: Started

INFO: [v++ 60-1453] Command Line: rtdgen

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7158/\_x/link/run\_link

INFO: [v++ 60-991] clock name 'clkwiz\_kernel\_clk\_out1' (clock ID '0') is being mapped to clock name 'DATA\_CLK' in the xclbin

INFO: [v++ 60-991] clock name 'clkwiz\_kernel2\_clk\_out1' (clock ID '1') is being mapped to clock name 'KERNEL\_CLK' in the xclbin

INFO: [v++ 60-1230] The compiler selected the following frequencies for the runtime controllable kernel clock(s) and scalable system clock(s): Kernel (DATA) clock: clkwiz\_kernel\_clk\_out1 = 300, Kernel (KERNEL) clock: clkwiz\_kernel2\_clk\_out1 = 500

INFO: [v++ 60-1453] Command Line: cf2sw -a /iu\_home/iu7158/\_x/link/int/address\_map.xml -sdsl /iu\_home/iu7158/\_x/link/int/sdsl.dat -xclbin /iu\_home/iu7158/\_x/link/int/xclbin\_orig.xml -rtd /iu\_home/iu7158/\_x/link/int/vinc.rtd -o /iu\_home/iu7158/\_x/link/int/vinc.xml

INFO: [v++ 60-1652] Cf2sw returned exit code: 0

INFO: [v++ 60-2311] HPISystemDiagram::writeSystemDiagramAfterRunningVivado, rtdInputFilePath: /iu\_home/iu7158/\_x/link/int/vinc.rtd

INFO: [v++ 60-2312] HPISystemDiagram::writeSystemDiagramAfterRunningVivado, systemDiagramOutputFilePath: /iu\_home/iu7158/\_x/link/int/systemDiagramModelSlrBaseAddress.json

INFO: [v++ 60-1618] Launching

INFO: [v++ 60-1441] [10:53:38] Run run\_link: Step rtdgen: Completed

Time (s): cpu = 00:00:11 ; elapsed = 00:00:12 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 79774 ; free virtual = 180314

INFO: [v++ 60-1443] [10:53:38] Run run\_link: Step xclbinutil: Started

INFO: [v++ 60-1453] Command Line: xclbinutil --add-section DEBUG\_IP\_LAYOUT:JSON:/iu\_home/iu7158/\_x/link/int/debug\_ip\_layout.rtd --add-section BITSTREAM:RAW:/iu\_home/iu7158/\_x/link/int/partial.bit --force --target hw --key-value SYS:dfx\_enable:true --add-section :JSON:/iu\_home/iu7158/\_x/link/int/vinc.rtd --append-section :JSON:/iu\_home/iu7158/\_x/link/int/appendSection.rtd --add-section CLOCK\_FREQ\_TOPOLOGY:JSON:/iu\_home/iu7158/\_x/link/int/vinc\_xml.rtd --add-section BUILD\_METADATA:JSON:/iu\_home/iu7158/\_x/link/int/vinc\_build.rtd --add-section EMBEDDED\_METADATA:RAW:/iu\_home/iu7158/\_x/link/int/vinc.xml --add-section SYSTEM\_METADATA:RAW:/iu\_home/iu7158/\_x/link/int/systemDiagramModelSlrBaseAddress.json --output /iu\_home/iu7158/workspace/Alveo\_lab1\_kernels/src/vitis\_rtl\_kernel/rtl\_kernel\_wizard\_0/vinc.xclbin

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7158/\_x/link/run\_link

XRT Build Version: 2.8.743 (2020.2)

Build Date: 2020-11-16 00:19:11

Hash ID: 77d5484b5c4daa691a7f78235053fb036829b1e9

Creating a default 'in-memory' xclbin image.

Section: 'DEBUG\_IP\_LAYOUT'(9) was successfully added.

Size : 440 bytes

Format : JSON

File : '/iu\_home/iu7158/\_x/link/int/debug\_ip\_layout.rtd'

Section: 'BITSTREAM'(0) was successfully added.

Size : 42510826 bytes

Format : RAW

File : '/iu\_home/iu7158/\_x/link/int/partial.bit'

Section: 'MEM\_TOPOLOGY'(6) was successfully added.

Format : JSON

File : 'mem\_topology'

Section: 'IP\_LAYOUT'(8) was successfully added.

Format : JSON

File : 'ip\_layout'

Section: 'CONNECTIVITY'(7) was successfully added.

Format : JSON

File : 'connectivity'

Section: 'CLOCK\_FREQ\_TOPOLOGY'(11) was successfully added.

Size : 274 bytes

Format : JSON

File : '/iu\_home/iu7158/\_x/link/int/vinc\_xml.rtd'

Section: 'BUILD\_METADATA'(14) was successfully added.

Size : 3174 bytes

Format : JSON

File : '/iu\_home/iu7158/\_x/link/int/vinc\_build.rtd'

Section: 'EMBEDDED\_METADATA'(2) was successfully added.

Size : 2759 bytes

Format : RAW

File : '/iu\_home/iu7158/\_x/link/int/vinc.xml'

Section: 'SYSTEM\_METADATA'(22) was successfully added.

Size : 5871 bytes

Format : RAW

File : '/iu\_home/iu7158/\_x/link/int/systemDiagramModelSlrBaseAddress.json'

Section: 'IP\_LAYOUT'(8) was successfully appended to.

Format : JSON

File : 'ip\_layout'

Successfully wrote (42533519 bytes) to the output file: /iu\_home/iu7158/workspace/Alveo\_lab1\_kernels/src/vitis\_rtl\_kernel/rtl\_kernel\_wizard\_0/vinc.xclbin

Leaving xclbinutil.

INFO: [v++ 60-1441] [10:53:40] Run run\_link: Step xclbinutil: Completed

Time (s): cpu = 00:00:00.50 ; elapsed = 00:00:02 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 79741 ; free virtual = 180361

INFO: [v++ 60-1443] [10:53:40] Run run\_link: Step xclbinutilinfo: Started

INFO: [v++ 60-1453] Command Line: xclbinutil --quiet --force --info /iu\_home/iu7158/workspace/Alveo\_lab1\_kernels/src/vitis\_rtl\_kernel/rtl\_kernel\_wizard\_0/vinc.xclbin.info --input /iu\_home/iu7158/workspace/Alveo\_lab1\_kernels/src/vitis\_rtl\_kernel/rtl\_kernel\_wizard\_0/vinc.xclbin

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7158/\_x/link/run\_link

INFO: [v++ 60-1441] [10:53:43] Run run\_link: Step xclbinutilinfo: Completed

Time (s): cpu = 00:00:02 ; elapsed = 00:00:03 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 79667 ; free virtual = 180288

INFO: [v++ 60-1443] [10:53:43] Run run\_link: Step generate\_sc\_driver: Started

INFO: [v++ 60-1453] Command Line:

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7158/\_x/link/run\_link

INFO: [v++ 60-1441] [10:53:43] Run run\_link: Step generate\_sc\_driver: Completed

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.04 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 79645 ; free virtual = 180266

INFO: [v++ 60-244] Generating system estimate report...

INFO: [v++ 60-1092] Generated system estimate report: /iu\_home/iu7158/\_x/reports/link/system\_estimate\_vinc.xtxt

INFO: [v++ 60-586] Created /iu\_home/iu7158/workspace/Alveo\_lab1\_kernels/src/vitis\_rtl\_kernel/rtl\_kernel\_wizard\_0/vinc.ltx

INFO: [v++ 60-586] Created /iu\_home/iu7158/workspace/Alveo\_lab1\_kernels/src/vitis\_rtl\_kernel/rtl\_kernel\_wizard\_0/vinc.xclbin

INFO: [v++ 60-1307] Run completed. Additional information can be found in:

Guidance: /iu\_home/iu7158/\_x/reports/link/v++\_link\_vinc\_guidance.html

Timing Report: /iu\_home/iu7158/\_x/reports/link/imp/impl\_1\_xilinx\_u200\_xdma\_201830\_2\_bb\_locked\_timing\_summary\_routed.rpt

Vivado Log: /iu\_home/iu7158/\_x/logs/link/vivado.log

Steps Log File: /iu\_home/iu7158/\_x/logs/link/link.steps.log

INFO: [v++ 60-2343] Use the vitis\_analyzer tool to visualize and navigate the relevant reports. Run the following command.

vitis\_analyzer /iu\_home/iu7158/workspace/Alveo\_lab1\_kernels/src/vitis\_rtl\_kernel/rtl\_kernel\_wizard\_0/vinc.xclbin.link\_summary

INFO: [v++ 60-791] Total elapsed time: 13h 27m 17s

INFO: [v++ 60-1653] Closing dispatch client.

# Тестирование

Изменим содержимое файла **host\_example.cpp** таким образом, чтобы выполнялось корректное тестирование функции, предложенной в варианте:

**for** (cl\_uint i = **0**; i < number\_of\_words; i++) {

printf("i=%d, input=%d, output=%d**\n**", i, ((h\_data[i] + **10**) & (**255**<<**8**)), h\_axi00\_ptr0\_output[i]);

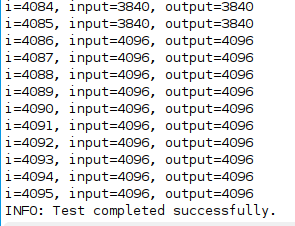
**if** (((h\_data[i] + **10**) & (**255**<<**8**)) != h\_axi00\_ptr0\_output[i]) {

printf("ERROR in rtl\_kernel\_wizard\_0::m00\_axi - array index %d (host addr 0x%03x) - input=%d (0x%x), output=%d (0x%x)**\n**", i, i\***4**, h\_data[i], h\_data[i], h\_axi00\_ptr0\_output[i], h\_axi00\_ptr0\_output[i]);

check\_status = **1**;

}

Далее приведены результаты тестирования.



# Заключение

В ходе лабораторной работы были изучены архитектура гетерогенных вычислительных систем и технологии разработки ускорителей вычислений на базе ПЛИС фирмы Xilinx. Была выполнена генерация ядра ускорителя с последующим синтезом, сборкой и тестированием бинарного модуля ускорителя.