CPT160

Final Assessment

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Contents

Question 1 Bit Masking (2+0.5+1.5 = 4 marks)

1. Make sure that the MSB is set and only this bit is set in the byte.

Reset all bytes with **AND -** mask 00000000, then set the MSB with **OR -** mask 10000000

bit	7	6	5	4	3	2	1	0
A	x	x	x	x	x	x	x	x
M1	0	0	0	0	0	0	0	0
A AND M	0	0	0	0	0	0	0	0
bit	7	6	5	4	3	2	1	0
A	0	0	0	0	0	0	0	0
M2	1	0	0	0	0	0	0	0
(A and M1) or M2	1	0	0	0	0	0	0	0

2. Flip the LSB and bit 6 leaving the other bits untouched.

Flip selected using **XOR** operator mask 01000001

bit	7	6	5	4	3	2	1	0
A	x	x	x	x	x	x	x	x
M	0	1	0	0	0	0	0	1
A XOR M	x	/x	x	x	x	x	x	/x

3. Set bits 3 and 5, all other bits are reset.

Multiple ways to do this could set bit 3 and 5 setting rest to 0 with and operator in 1 go but have chosen to reset all then set with or so the following:
Reset all with **AND** – mask 00000000, Set 3 and 5 with **OR** – mask 00101000

bit	7	6	5	4	3	2	1	0
A	X	x	x	X	x	x	x	x
M1	0	0	0	0	0	0	0	0
A and M1	0	0	0	0	0	0	0	0
bit	7	6	5	4	3	2	1	0
A	0	0	0	0	0	0	0	0
M2	0	0	1	0	1	0	0	0
(A and M1) or M2	0	0	1	0	1	0	0	0

Question 2 Hamming/SECDED codes(1+3 = 4 marks)

1. Yes. An error has occurred because the retrieved code has an odd number of 1's in this case 5.

2.

7	6	5	4	3	2	1	0	Bit no
D4	D3	D2	P3	D1	P2	P1	P0	Data/parity
1	1	0	1	0	0	1	1	Data
1	1	0	1	0	0	1	1	P0
1		0		0		1		P1
1	1			0	0			P2
1	1	0	1					P3

5 ones P0 shows an error
2 ones P1 is Correct
2 ones P2 is Correct
3 ones P3 is Error state

Method 1 Deduction/logic
1, 2, 3, 5, 7 are correct covered by P1 and P2
6 is correct covered by P2

Bit 4 has flipped as only one left out.

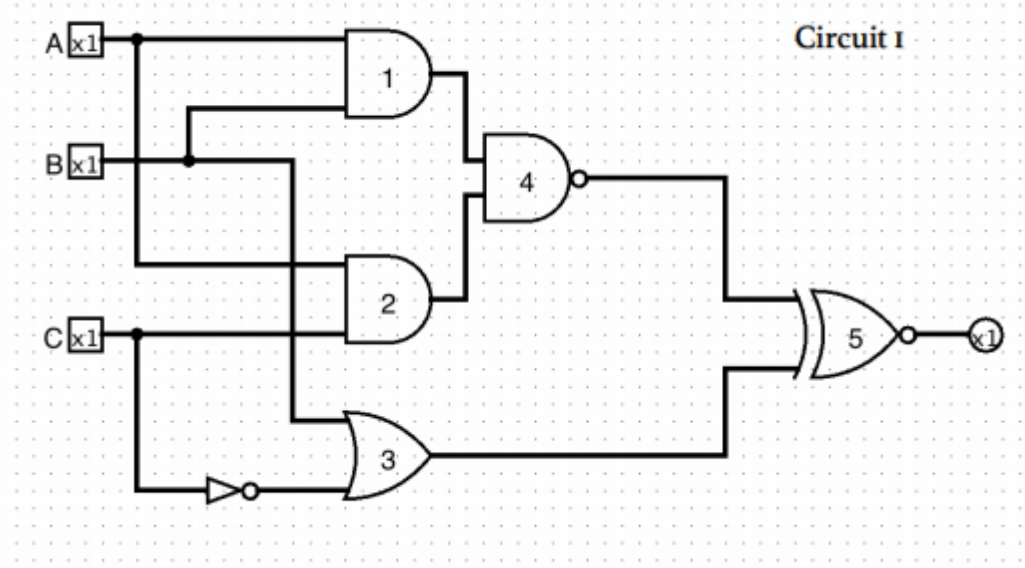
Method 2
P3P2P1 = > 100_2 => 4_{10}

Method 3
P0 + P3 = 0+4 = 4_{10}

Correct data would be **1100 0011**

Question 3 — Logic Circuits and Truth Tables (2+4 = 6 marks)

Solve problems related to the circuit below:



1. Solution

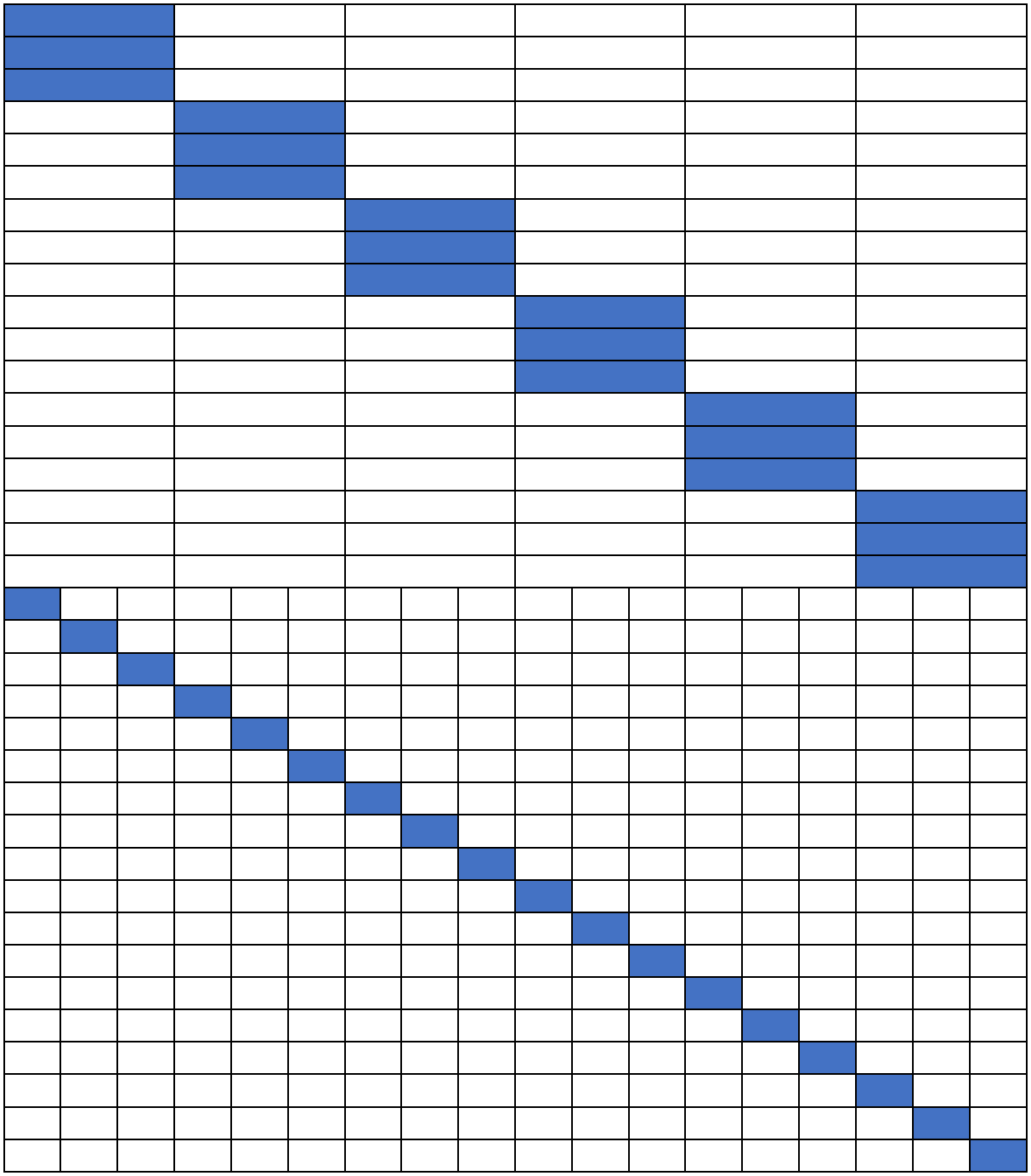
AND gate(1) = (A.B)
AND gate(2) = (A.C)
OR gate(3) = (B+/C)
NAND gate(4) = /((A.B).(A.C))
XNOR gate(5) = /(/((A.B).(A.C))) + (B+/C))

2.

a	b	c	a.b	a.c	a.b.a.c	/a.b.a.c	/c	B+/c	/(/((A.B).(A.C))) + (B+/C))
0	0	0	0	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	0
0	1	0	0	0	0	1	1	1	1
0	1	1	0	0	0	1	0	1	1
1	0	0	0	0	0	1	1	1	1
1	0	1	0	1	0	1	0	0	0
1	1	0	1	0	0	1	1	1	1
1	1	1	1	1	1	0	0	1	1

Question 4 Pipelining (1+1+1+1+1 = 4 marks)

A 6 stage pipeline uses three clock ticks for each stage. A 18 stage pipeline uses one clock tick for every stage.



1. The 6 stage will be full on the 16^{th} tick whereas the 18 stage will be full upon the 18^{th} tick.
2. If determining that the instructions are the stages the 6 stage will be able to complete : 30/3 = 10 instructions
   The 18 stage pipeline will be 30/1 = 30 instructions
3. Advantage of deep pipelining is speed splitting the pipeline into more stages with each stage containing less logic processing can be done faster.
   Disadvantage would be the cost not only the for the hardware but for the running costs (energy consumption)

Question 5 Latency (3 marks)

Calculate the true latency of the following memory module in MHz and CL in ns:

DDR5-6400MHz with CL46

Clock Cycle = 1/(6400000000/2)

= 0.0000000003125 seconds
nanoseconds = 0.0000000003125 * 1000000000
= 0.3125

True latency = clock cycle time * number of clock cycles

= 0.3125 * 46

= 14.375 ns

Question 6 RAID (4 marks)

You are putting together a file server, using an array of 10 consumer grade 400GB hard disks in RAID 1 (mirroring) configuration.

1.Total usuable capacity = (10 * 400)/2

= 2000GB

2. It is called a URE unrecoverable read errors. While rebuilding the data was insufficient for rebuild.

3. RAID 10 would overcome this problem since it is mirror copied the drive replacement is a simple copy over ignoring any URE corruptions. If the new drive were to fail then the full mirror is still there for mirroring resulting in no problems.

Bibliography

Cutress, D., 2021. *Insights into DDR5 Sub-timings and Latencies*. [online] Anandtech.com. Available at: <https://www.anandtech.com/show/16143/insights-into-ddr5-subtimings-and-latencies> [Accessed 30 August 2021].

If a RAID5 system experiences a URE during rebuild, i., 2021. *If a RAID5 system experiences a URE during rebuild, is all the data lost?*. [online] Server Fault. Available at: <https://serverfault.com/questions/937547/if-a-raid5-system-experiences-a-ure-during-rebuild-is-all-the-data-lost> [Accessed 30 August 2021].