# 1. Description

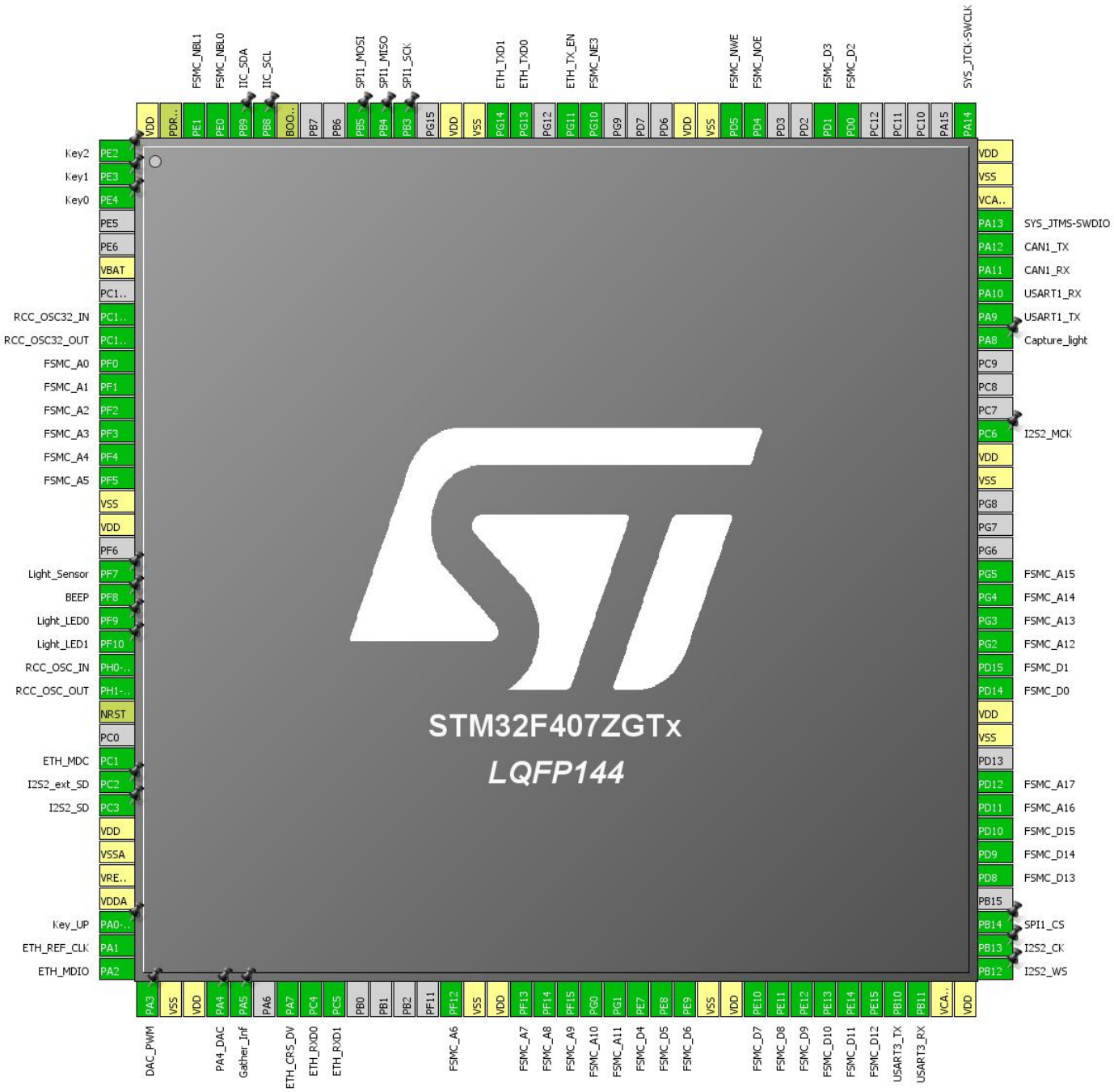
## 1.1. Project

| | |
|---|---|
| Project Name | STM32F407_FreeRTOS |
| Board Name | custom |
| Generated with: | STM32CubeMX 4.27.0 |
| Date | 03/20/2021 |

## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32F4 |
| MCU Line | STM32F407/417 |
| MCU name | STM32F407ZGTx |
| MCU Package | LQFP144 |
| MCU Pin number | 144 |

# 2. Pinout Configuration



# 3. Pins Configuration

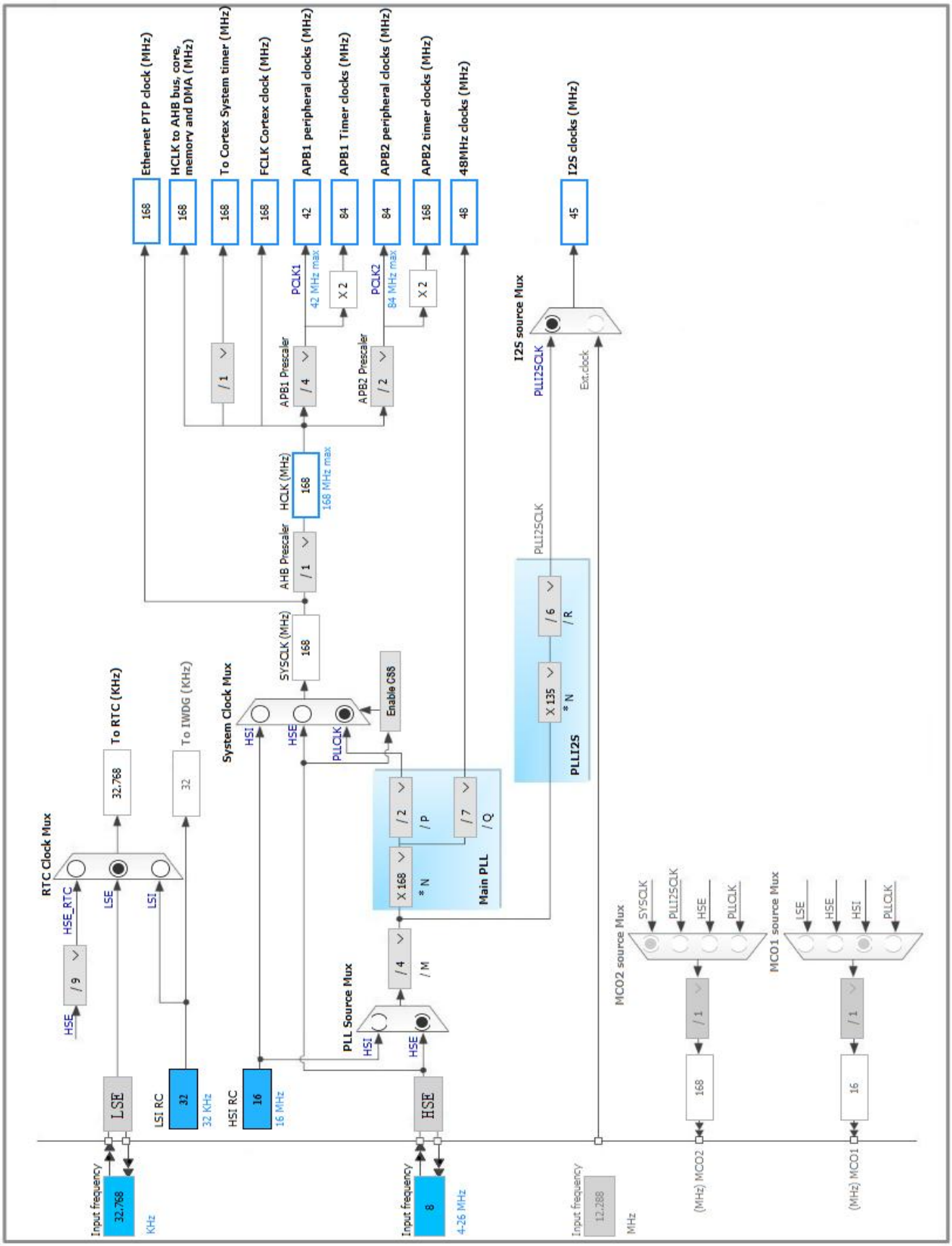
| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 1 | PE2 | I/O | GPIO_EXTI2 | Key2 |
| 2 | PE3 | I/O | GPIO_EXTI3 | Key1 |
| 3 | PE4 | I/O | GPIO_EXTI4 | Key0 |
| 6 | VBAT | Power | | |
| 8 | PC14-OSC32_IN | I/O | RCC_OSC32_IN | |
| 9 | PC15-OSC32_OUT | I/O | RCC_OSC32_OUT | |
| 10 | PF0 | I/O | FSMC_A0 | |
| 11 | PF1 | I/O | FSMC_A1 | |
| 12 | PF2 | I/O | FSMC_A2 | |
| 13 | PF3 | I/O | FSMC_A3 | |
| 14 | PF4 | I/O | FSMC_A4 | |
| 15 | PF5 | I/O | FSMC_A5 | |
| 16 | VSS | Power | | |
| 17 | VDD | Power | | |
| 19 | PF7 | I/O | GPIO_Analog, ADC3_IN5 | Light_Sensor |
| 20 | PF8 * | I/O | GPIO_Output | BEEP |
| 21 | PF9 | I/O | TIM14_CH1 | Light_LED0 |
| 22 | PF10 * | I/O | GPIO_Output | Light_LED1 |
| 23 | PH0-OSC_IN | I/O | RCC_OSC_IN | |
| 24 | PH1-OSC_OUT | I/O | RCC_OSC_OUT | |
| 25 | NRST | Reset | | |
| 27 | PC1 | I/O | ETH_MDC | |
| 28 | PC2 | I/O | I2S2_ext_SD | |
| 29 | PC3 | I/O | I2S2_SD | |
| 30 | VDD | Power | | |
| 31 | VSSA | Power | | |
| 32 | VREF+ | Power | | |
| 33 | VDDA | Power | | |
| 34 | PA0-WKUP | I/O | TIM5_CH1 | Key_UP |
| 35 | PA1 | I/O | ETH_REF_CLK | |
| 36 | PA2 | I/O | ETH_MDIO | |
| 37 | PA3 | I/O | TIM9_CH2 | DAC_PWM |
| 38 | VSS | Power | | |
| 39 | VDD | Power | | |
| 40 | PA4 | I/O | GPIO_Analog, DAC_OUT1 | PA4_DAC |
| 41 | PA5 | I/O | GPIO_Analog, ADC1_IN5 | Gather_Inf |

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 43 | PA7 | I/O | ETH_CRS_DV | |
| 44 | PC4 | I/O | ETH_RXD0 | |
| 45 | PC5 | I/O | ETH_RXD1 | |
| 50 | PF12 | I/O | FSMC_A6 | |
| 51 | VSS | Power | | |
| 52 | VDD | Power | | |
| 53 | PF13 | I/O | FSMC_A7 | |
| 54 | PF14 | I/O | FSMC_A8 | |
| 55 | PF15 | I/O | FSMC_A9 | |
| 56 | PG0 | I/O | FSMC_A10 | |
| 57 | PG1 | I/O | FSMC_A11 | |
| 58 | PE7 | I/O | FSMC_D4 | |
| 59 | PE8 | I/O | FSMC_D5 | |
| 60 | PE9 | I/O | FSMC_D6 | |
| 61 | VSS | Power | | |
| 62 | VDD | Power | | |
| 63 | PE10 | I/O | FSMC_D7 | |
| 64 | PE11 | I/O | FSMC_D8 | |
| 65 | PE12 | I/O | FSMC_D9 | |
| 66 | PE13 | I/O | FSMC_D10 | |
| 67 | PE14 | I/O | FSMC_D11 | |
| 68 | PE15 | I/O | FSMC_D12 | |
| 69 | PB10 | I/O | USART3_TX | USART3_TX |
| 70 | PB11 | I/O | USART3_RX | USART3_RX |
| 71 | VCAP_1 | Power | | |
| 72 | VDD | Power | | |
| 73 | PB12 | I/O | I2S2_WS | |
| 74 | PB13 | I/O | I2S2_CK | |
| 75 | PB14 * | I/O | GPIO_Output | SPI1_CS |
| 77 | PD8 | I/O | FSMC_D13 | |
| 78 | PD9 | I/O | FSMC_D14 | |
| 79 | PD10 | I/O | FSMC_D15 | |
| 80 | PD11 | I/O | FSMC_A16 | |
| 81 | PD12 | I/O | FSMC_A17 | |
| 83 | VSS | Power | | |
| 84 | VDD | Power | | |
| 85 | PD14 | I/O | FSMC_D0 | |
| 86 | PD15 | I/O | FSMC_D1 | |
| 87 | PG2 | I/O | FSMC_A12 | |

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 88 | PG3 | I/O | FSMC_A13 | |
| 89 | PG4 | I/O | FSMC_A14 | |
| 90 | PG5 | I/O | FSMC_A15 | |
| 94 | VSS | Power | | |
| 95 | VDD | Power | | |
| 96 | PC6 | I/O | I2S2_MCK | |
| 100 | PA8 | I/O | TIM1_CH1 | Capture_light |
| 101 | PA9 | I/O | USART1_TX | USART1_TX |
| 102 | PA10 | I/O | USART1_RX | USART1_RX |
| 103 | PA11 | I/O | CAN1_RX | CAN1_RX |
| 104 | PA12 | I/O | CAN1_TX | CAN1_TX |
| 105 | PA13 | I/O | SYS_JTMS-SWDIO | |
| 106 | VCAP_2 | Power | | |
| 107 | VSS | Power | | |
| 108 | VDD | Power | | |
| 109 | PA14 | I/O | SYS_JTCK-SWCLK | |
| 114 | PD0 | I/O | FSMC_D2 | |
| 115 | PD1 | I/O | FSMC_D3 | |
| 118 | PD4 | I/O | FSMC_NOE | |
| 119 | PD5 | I/O | FSMC_NWE | |
| 120 | VSS | Power | | |
| 121 | VDD | Power | | |
| 125 | PG10 | I/O | FSMC_NE3 | |
| 126 | PG11 | I/O | ETH_TX_EN | |
| 128 | PG13 | I/O | ETH_TXD0 | |
| 129 | PG14 | I/O | ETH_TXD1 | |
| 130 | VSS | Power | | |
| 131 | VDD | Power | | |
| 133 | PB3 * | I/O | GPIO_Output | SPI1_SCK |
| 134 | PB4 * | I/O | GPIO_Input | SPI1_MISO |
| 135 | PB5 * | I/O | GPIO_Output | SPI1_MOSI |
| 138 | BOOT0 | Boot | | |
| 139 | PB8 * | I/O | GPIO_Output | IIC_SCL |
| 140 | PB9 * | I/O | GPIO_Output | IIC_SDA |
| 141 | PE0 | I/O | FSMC_NBL0 | |
| 142 | PE1 | I/O | FSMC_NBL1 | |
| 143 | PDR_ON | Reset | | |
| 144 | VDD | Power | | |

* The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 5. IPs and Middleware Configuration

## 5.1. ADC1

**mode: IN5**

### 5.1.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | PCLK2 divided by 4 |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | **Enabled *** |
| Continuous Conversion Mode | **Enabled *** |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | **Enabled *** |
| End Of Conversion Selection | EOC flag at the end of single channel conversion |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | Channel 5 |
| Sampling Time | **480 Cycles *** |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Number Of Conversions | 0 |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## 5.2. ADC3

**mode: IN5**

### 5.2.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | PCLK2 divided by 4 |
| Resolution | |

| | |
|---|---|
| | **10 bits (13 ADC Clock cycles) *** |
| Data Alignment | Right alignment |
| Scan Conversion Mode | **Enabled *** |
| Continuous Conversion Mode | **Enabled *** |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | **Enabled *** |
| End Of Conversion Selection | EOC flag at the end of single channel conversion |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | Channel 5 |
| Sampling Time | **480 Cycles *** |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Number Of Conversions | 0 |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## *5.3. CAN1*

### mode: Mode

### 5.3.1. Parameter Settings:

**Bit Timings Parameters:**

| | |
|---|---|
| Prescaler (for Time Quantum) | **7 *** |
| Time Quantum | **166.66666666666669 *** |
| Time Quanta in Bit Segment 1 | **5 Times *** |
| Time Quanta in Bit Segment 2 | **6 Times *** |
| ReSynchronization Jump Width | 1 Time |

**Basic Parameters:**

| | |
|---|---|
| Time Triggered Communication Mode | Disable |
| Automatic Bus-Off Management | Disable |
| Automatic Wake-Up Mode | Disable |
| No-Automatic Retransmission | **Enable *** |
| Receive Fifo Locked Mode | Disable |
| Transmit Fifo Priority | Disable |

**Advanced Parameters:**

| | |
|---|---|
| Operating Mode | Normal |

## 5.4. DAC

### mode: OUT1 Configuration

### 5.4.1. Parameter Settings:

**DAC Out1 Settings:**

| | |
|---|---|
| Output Buffer | **Disable *** |
| Trigger | None |

## 5.5. ETH

### Mode: RMII

### 5.5.1. Parameter Settings:

**Advanced : Ethernet Media Configuration:**

| | |
|---|---|
| Auto Negotiation | Enabled |

**General : Ethernet Configuration:**

| | |
|---|---|
| Ethernet MAC Address | 00:80:E1:00:00:00 |
| PHY Address | **0 *** |

**Ethernet Basic Configuration:**

| | |
|---|---|
| Rx Mode | Interrupt Mode |
| TX IP Header Checksum Computation | By hardware |

### 5.5.2. Advanced Parameters:

**External PHY Configuration:**

| | |
|---|---|
| PHY | LAN8742A_PHY_ADDRESS |
| PHY Address Value | 0 |
| PHY Reset delay these values are based on a 1 ms Systick interrupt | **0x000000FF *** |
| PHY Configuration delay | **0x00000FFF *** |
| PHY Read TimeOut | **0x0000FFFF *** |
| PHY Write TimeOut | **0x0000FFFF *** |

**Common : External PHY Configuration:**

| | |
|---|---|
| Transceiver Basic Control Register | **0x00 *** |

| | |
|---|---|
| Transceiver Basic Status Register | **0x01 *** |
| PHY Reset | **0x8000 *** |
| Select loop-back mode | **0x4000 *** |
| Set the full-duplex mode at 100 Mb/s | **0x2100 *** |
| Set the half-duplex mode at 100 Mb/s | **0x2000 *** |
| Set the full-duplex mode at 10 Mb/s | **0x0100 *** |
| Set the half-duplex mode at 10 Mb/s | **0x0000 *** |
| Enable auto-negotiation function | **0x1000 *** |
| Restart auto-negotiation function | **0x0200 *** |
| Select the power down mode | **0x0800 *** |
| Isolate PHY from MII | **0x0400 *** |
| Auto-Negotiation process completed | **0x0020 *** |
| Valid link established | **0x0004 *** |
| Jabber condition detected | **0x0002 *** |

**Extended : External PHY Configuration:**

| | |
|---|---|
| PHY special control/status register Offset | **0x1F *** |
| PHY Speed mask | **0x0004 *** |
| PHY Duplex mask | **0x0010 *** |
| PHY Interrupt Source Flag register Offset | **0x000B *** |
| PHY Link down inturrupt | **0x000B *** |

## *5.6. FSMC*

*NOR Flash/PSRAM/SRAM/ROM/LCD 1*

**Chip Select: NE3**

**Memory type: SRAM**

**Address: 18 bits**

**Data: 16 bits**

**Byte enable: set**

### 5.6.1. NOR/PSRAM 1:

**NOR/PSRAM control:**

| | |
|---|---|
| Memory type | SRAM |
| Bank | Bank 1 NOR/PSRAM 3 |
| Write operation | **Enabled *** |
| Extended mode | Disabled |

**NOR/PSRAM timing:**

| | |
|---|---|
| Address setup time in HCLK clock cycles | **0 *** |
| Data setup time in HCLK clock cycles | **6 *** |
| Bus turn around time in HCLK clock cycles | **0 *** |

## 5.7. I2S2

### Mode: Full-Duplex Master
### mode: Master Clock Output
### 5.7.1. Parameter Settings:

**Generic Parameters:**

| | |
|---|---|
| Transmission Mode | Mode Master Transmit |
| Communication Standard | I2S Philips |
| Data and Frame Format | **24 Bits Data on 32 Bits Frame *** |
| Selected Audio Frequency | 8 KHz |
| Real Audio Frequency | **7.99 KHz *** |
| Error between Selected and Real | **-0.12 % *** |

**Clock Parameters:**

| | |
|---|---|
| Clock Source | I2S PLL Clock |
| Clock Polarity | Low |

## 5.8. RCC

### High Speed Clock (HSE): Crystal/Ceramic Resonator
### Low Speed Clock (LSE) : Crystal/Ceramic Resonator
### 5.8.1. Parameter Settings:

**System Parameters:**

| | |
|---|---|
| VDD voltage (V) | 3.3 |
| Instruction Cache | Enabled |
| Prefetch Buffer | Enabled |
| Data Cache | Enabled |
| Flash Latency(WS) | 5 WS (6 CPU cycle) |

**RCC Parameters:**

| | |
|---|---|
| HSI Calibration Value | 16 |
| HSE Startup Timout Value (ms) | 100 |
| LSE Startup Timout Value (ms) | 5000 |

**Power Parameters:**

| | |
|---|---|
| Power Regulatror Voltage Scale | Power Regulator Voltage Scale 1 |

## 5.9. RNG

**mode: Activated**

## 5.10. RTC

**mode: Activate Clock Source**

**mode: Activate Calendar**

**Alarm A: Internal Alarm**

### 5.10.1. Parameter Settings:

**General:**

| | |
|---|---|
| Hour Format | Hourformat 24 |
| Asynchronous Predivider value | 127 |
| Synchronous Predivider value | 255 |

**Calendar Time:**

| | |
|---|---|
| Data Format | BCD data format |
| Hours | **22 *** |
| Minutes | **42 *** |
| Seconds | **55 *** |
| Day Light Saving: value of hour adjustment | Daylightsaving None |
| Store Operation | Storeoperation Reset |

**Calendar Date:**

| | |
|---|---|
| Week Day | **Wednesday *** |
| Month | January |
| Date | **16 *** |
| Year | **21 *** |

**Alarm A:**

| | |
|---|---|
| Hours | **15 *** |
| Minutes | **18 *** |
| Seconds | **23 *** |
| Sub Seconds | 0 |
| Alarm Mask Date Week day | Disable |
| Alarm Mask Hours | Disable |
| Alarm Mask Minutes | Disable |
| Alarm Mask Seconds | Disable |

| | |
|---|---|
| Alarm Sub Second Mask | **SS[14:0] are compared and must match to activate alarm. *** |
| Alarm Date Week Day Sel | **Weekday *** |
| Alarm Week Day | Monday |

## 5.11. SYS

**Debug: Serial Wire**

**Timebase Source: TIM3**

## 5.12. TIM1

**Trigger Source: ITR0**

**Clock Source : Internal Clock**

**Channel1: Input Capture direct mode**

### 5.12.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **179 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **10000 *** |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 8 bits value) | 0 |
| Slave Mode Controller | Slave mode disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

**Input Capture Channel 1:**

| | |
|---|---|
| Polarity Selection | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter (4 bits value) | **0x03 *** |

## 5.13. TIM2

**Trigger Source: ITR0**

**Clock Source : Internal Clock**

### 5.13.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **1 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value ) | **0xFFFFFFFF *** |
| Internal Clock Division (CKD) | No Division |
| Slave Mode Controller | Slave mode disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | **Update Event *** |

## *5.14. TIM4*

**Clock Source : Internal Clock**

### 5.14.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **8400-1 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **1000 *** |
| Internal Clock Division (CKD) | No Division |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

## *5.15. TIM5*

**Trigger Source: ITR0**

**mode: Clock Source**

**Channel1: Input Capture direct mode**

### 5.15.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **84 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value ) | **0xFFFFFFFF *** |
| Internal Clock Division (CKD) | No Division |

| | |
|---|---|
| Slave Mode Controller | Slave mode disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | **Update Event *** |

**Input Capture Channel 1:**

| | |
|---|---|
| Polarity Selection | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter (4 bits value) | 0 |

## *5.16. TIM7*

### mode: Activated

### 5.16.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **84-1 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **1 *** |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

## *5.17. TIM9*

### Channel2: PWM Generation CH2

### 5.17.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **1 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **255 *** |
| Internal Clock Division (CKD) | No Division |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

## 5.18. TIM14

**mode: Activated**

**Channel1: PWM Generation CH1**

### 5.18.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | **42 *** |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | **500 *** |
| Internal Clock Division (CKD) | No Division |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | **Low *** |

## 5.19. USART1

**Mode: Asynchronous**

### 5.19.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |

## 5.20. USART3

**Mode: Asynchronous**

### 5.20.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |

## *5.21. FREERTOS*

### mode: Enabled

### 5.21.1. Config parameters:

**Versions:**

| | |
|---|---|
| FreeRTOS version | 9.0.0 |
| CMSIS-RTOS version | 1.02 |

**Kernel settings:**

| | |
|---|---|
| USE_PREEMPTION | Enabled |
| CPU_CLOCK_HZ | SystemCoreClock |
| TICK_RATE_HZ | 1000 |
| MAX_PRIORITIES | 7 |
| MINIMAL_STACK_SIZE | 128 |
| MAX_TASK_NAME_LEN | 16 |
| USE_16_BIT_TICKS | Disabled |
| IDLE_SHOULD_YIELD | Enabled |
| USE_MUTEXES | Enabled |
| USE_RECURSIVE_MUTEXES | Disabled |
| USE_COUNTING_SEMAPHORES | Disabled |
| QUEUE_REGISTRY_SIZE | 8 |
| USE_APPLICATION_TASK_TAG | Disabled |
| ENABLE_BACKWARD_COMPATIBILITY | Enabled |
| USE_PORT_OPTIMISED_TASK_SELECTION | Enabled |
| USE_TICKLESS_IDLE | Disabled |
| USE_TASK_NOTIFICATIONS | Enabled |

**Memory management settings:**

| | |
|---|---|
| Memory Allocation | Dynamic |
| TOTAL_HEAP_SIZE | 15360 |
| Memory Management scheme | heap_4 |

**Hook function related definitions:**

| | |
|---|---|
| USE_IDLE_HOOK | Disabled |
| USE_TICK_HOOK | Disabled |
| USE_MALLOC_FAILED_HOOK | Disabled |
| USE_DAEMON_TASK_STARTUP_HOOK | Disabled |
| CHECK_FOR_STACK_OVERFLOW | Disabled |

**Run time and task stats gathering related definitions:**

| | |
|---|---|
| GENERATE_RUN_TIME_STATS | Disabled |
| USE_TRACE_FACILITY | Disabled |
| USE_STATS_FORMATTING_FUNCTIONS | Disabled |

**Co-routine related definitions:**

| | |
|---|---|
| USE_CO_ROUTINES | Disabled |
| MAX_CO_ROUTINE_PRIORITIES | 2 |

**Software timer definitions:**

| | |
|---|---|
| USE_TIMERS | Disabled |

**Interrupt nesting behaviour configuration:**

| | |
|---|---|
| LIBRARY_LOWEST_INTERRUPT_PRIORITY | 15 |
| LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY | 5 |

## 5.21.2. Include parameters:

**Include definitions:**

| | |
|---|---|
| vTaskPrioritySet | Enabled |
| uxTaskPriorityGet | Enabled |
| vTaskDelete | Enabled |
| vTaskCleanUpResources | Disabled |
| vTaskSuspend | Enabled |
| vTaskDelayUntil | Disabled |
| vTaskDelay | Enabled |
| xTaskGetSchedulerState | Enabled |
| xTaskResumeFromISR | Enabled |
| xQueueGetMutexHolder | Disabled |
| xSemaphoreGetMutexHolder | Disabled |
| pcTaskGetTaskName | Disabled |
| uxTaskGetStackHighWaterMark | Disabled |
| xTaskGetCurrentTaskHandle | Disabled |
| eTaskGetState | Disabled |
| xEventGroupSetBitFromISR | Disabled |
| xTimerPendFunctionCall | Disabled |
| xTaskAbortDelay | Disabled |
| xTaskGetHandle | Disabled |

## *5.22. LWIP*

**mode: Enabled**

Advanced parameters are not listed except if modified by user.

### 5.22.1. General Settings:

| | |
|---|---|
| **LwIP Version:** | |
| LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **) | 2.0.3 |
| **IPv4 - DHCP Options:** | |
| LWIP_DHCP (DHCP Module) | **Disabled *** |
| **IP Address Settings:** | |
| IP_ADDRESS (IP Address) | **192.168.001.030 *** |
| NETMASK_ADDRESS (Netmask Address) | **255.255.255.000 *** |
| GATEWAY_ADDRESS (Gateway Address) | **192.168.001.001 *** |
| **RTOS Dependency:** | |
| WITH_RTOS (Use FREERTOS ** CubeMX specific **) | Enabled |
| **Protocols Options:** | |
| LWIP_ICMP (ICMP Module Activation) | Enabled |
| LWIP_IGMP (IGMP Module) | Disabled |
| LWIP_DNS (DNS Module) | Disabled |
| LWIP_UDP (UDP Module) | Enabled |
| MEMP_NUM_UDP_PCB (Number of UDP Connections) | 4 |
| LWIP_TCP (TCP Module) | Enabled |
| MEMP_NUM_TCP_PCB (Number of TCP Connections) | 5 |

### 5.22.2. Key Options:

| | |
|---|---|
| **Infrastructure - OS Awarness Option:** | |
| NO_SYS (OS Awarness) | OS Used |
| **Infrastructure - Timers Options:** | |
| LWIP_TIMERS (Use Support For sys_timeout) | Enabled |
| **Infrastructure - Core Locking and MPU Options:** | |
| SYS_LIGHTWEIGHT_PROT (Memory Functions Protection) | Enabled |
| **Infrastructure - Heap and Memory Pools Options:** | |
| MEM_SIZE (Heap Memory Size) | 1600 |
| **Infrastructure - Internal Memory Pool Sizes:** | |
| MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs) | 16 |

| | |
|---|---|
| MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks) | 4 |
| MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections) | 8 |
| MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued) | 16 |
| MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List) | 1 |

**Pbuf Options:**

| | |
|---|---|
| PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool) | 16 |
| PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool) | 592 |

**IPv4 - ARP Options:**

| | |
|---|---|
| LWIP_ARP (ARP Functionality) | Enabled |

**Callback - TCP Options:**

| | |
|---|---|
| TCP_TTL (Number of Time-To-Live Used by TCP Packets) | 255 |
| TCP_WND (TCP Receive Window Maximum Size) | 2144 |
| TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets) | Enabled |
| TCP_MSS (Maximum Segment Size) | 536 |
| TCP_SND_BUF (TCP Sender Buffer Space) | 1072 |
| TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender) | 9 |

**Network Interfaces Options:**

| | |
|---|---|
| LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes) | Disabled |
| LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes) | Disabled |

**NETIF - Loopback Interface Options:**

| | |
|---|---|
| LWIP_NETIF_LOOPBACK (NETIF Loopback) | Disabled |

**Infrastructure - Threading Options:**

| | |
|---|---|
| TCPIP_THREAD_NAME (TCPIP Thread Name) | "tcpip_thread" |
| TCPIP_THREAD_STACKSIZE (TCPIP Thread Stack Size) | 1024 |
| TCPIP_THREAD_PRIO (TCPIP Thread Priority Level) | 3 |
| TCPIP_MBOX_SIZE (TCPIP Mailbox Size) | 6 |
| DEFAULT_THREAD_NAME (Default LwIP Thread Name) | "lwIP" |
| DEFAULT_THREAD_STACKSIZE (Default LwIP Thread Stack Size) | 1024 |
| DEFAULT_THREAD_PRIO (Default LwIP Thread Priority Level) | 3 |
| DEFAULT_RAW_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN Raw) | 0 |
| DEFAULT_TCP_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN TCP) | 6 |
| DEFAULT_ACCEPTMBOX_SIZE (Default Mailbox Size for Incoming Connections) | 6 |

**Thread Safe APIs - Netconn Options:**

| | |
|---|---|
| LWIP_NETCONN (NETCONN API) | Enabled |

**Thread Safe APIs - Socket Options:**

| | |
|---|---|
| LWIP_SOCKET (Socket API) | Enabled |
| LWIP_COMPAT_SOCKETS (BSD-style Socket Functions Names) | 1 |
| LWIP_SOCKET_OFFSET (Socket Offset Number) | 0 |

### 5.22.3. PPP:

**PPP Options:**

| | |
|---|---|
| PPP_SUPPORT (PPP Module) | Disabled |

### 5.22.4. IPv6:

**IPv6 Options:**

| | |
|---|---|
| LWIP_IPV6 (IPv6 Protocol) | Disabled |

### 5.22.5. HTTPD:

**HTTPD Options:**

| | |
|---|---|
| LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **) | Disabled |

### 5.22.6. SNMP:

**SNMP Options:**

| | |
|---|---|
| LWIP_SNMP (LwIP SNMP Agent) | Disabled |

### 5.22.7. SNTP:

**SNTP Options:**

| | |
|---|---|
| LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **) | Disabled |

### 5.22.8. MDNS/TFTP:

**MDNS Options:**

| | |
|---|---|
| LWIP_MDNS (Multicast DNS Support ** CubeMX specific **) | Disabled |

**TFTP Options:**

| | |
|---|---|
| LWIP_TFTP (TFTP Support ** CubeMX specific **) | Disabled |

### 5.22.9. Perf/Checks:

**Sanity Checks:**

| | |
|---|---|
| LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks) | Disabled |
| LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks) | Disabled |

**Performance Options:**

| | |
|---|---|
| LWIP_PERF (Performace Testing for LwIP) | Disabled |

## 5.22.10. Statistics:

### Debug - Statistics Options:

| | |
|---|---|
| LWIP_STATS (Statictics Collection) | Disabled |

## 5.22.11. Checksum:

### Infrastructure - Checksum Options:

| | |
|---|---|
| CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **) | Disabled |
| LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif) | Disabled |
| CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets) | Disabled |
| CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets) | Disabled |
| CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets) | Disabled |
| CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets) | Disabled |
| CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets) | Disabled |
| CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets) | Disabled |
| CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets) | Disabled |
| CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets) | Disabled |
| CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets) | Disabled |
| CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets) | Disabled |

## 5.22.12. Debug:

### LwIP Main Debugging Options:

| | |
|---|---|
| LWIP_DBG_MIN_LEVEL (Minimum Level) | All |

*** User modified value**

# 6. System Configuration

## 6.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| ADC1 | PA5 | ADC1_IN5 | Analog mode | No pull-up and no pull-down | n/a | Gather_Inf |
| ADC3 | PF7 | ADC3_IN5 | Analog mode | No pull-up and no pull-down | n/a | Light_Sensor |
| CAN1 | PA11 | CAN1_RX | Alternate Function Push Pull | **Pull-up *** | **High *** | CAN1_RX |
| | PA12 | CAN1_TX | Alternate Function Push Pull | **Pull-up *** | **High *** | CAN1_TX |
| DAC | PA4 | DAC_OUT1 | Analog mode | No pull-up and no pull-down | n/a | PA4_DAC |
| ETH | PC1 | ETH_MDC | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PA1 | ETH_REF_CLK | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PA2 | ETH_MDIO | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PA7 | ETH_CRS_DV | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PC4 | ETH_RXD0 | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PC5 | ETH_RXD1 | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PG11 | ETH_TX_EN | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PG13 | ETH_TXD0 | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PG14 | ETH_TXD1 | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| FSMC | PF0 | FSMC_A0 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PF1 | FSMC_A1 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PF2 | FSMC_A2 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PF3 | FSMC_A3 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PF4 | FSMC_A4 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PF5 | FSMC_A5 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PF12 | FSMC_A6 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PF13 | FSMC_A7 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PF14 | FSMC_A8 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PF15 | FSMC_A9 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PG0 | FSMC_A10 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | PG1 | FSMC_A11 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PE7 | FSMC_D4 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PE8 | FSMC_D5 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PE9 | FSMC_D6 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PE10 | FSMC_D7 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PE11 | FSMC_D8 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PE12 | FSMC_D9 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PE13 | FSMC_D10 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PE14 | FSMC_D11 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PE15 | FSMC_D12 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PD8 | FSMC_D13 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PD9 | FSMC_D14 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PD10 | FSMC_D15 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PD11 | FSMC_A16 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PD12 | FSMC_A17 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PD14 | FSMC_D0 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PD15 | FSMC_D1 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PG2 | FSMC_A12 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PG3 | FSMC_A13 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PG4 | FSMC_A14 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PG5 | FSMC_A15 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PD0 | FSMC_D2 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PD1 | FSMC_D3 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PD4 | FSMC_NOE | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PD5 | FSMC_NWE | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PG10 | FSMC_NE3 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PE0 | FSMC_NBL0 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| | PE1 | FSMC_NBL1 | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| I2S2 | PC2 | I2S2_ext_SD | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PC3 | I2S2_SD | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PB12 | I2S2_WS | Alternate Function Push Pull | **Pull-up *** | **High *** | |
| | PB13 | I2S2_CK | Alternate Function Push Pull | **Pull-up *** | **High *** | |
| | PC6 | I2S2_MCK | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| RCC | PC14-OSC32_IN | RCC_OSC32_IN | n/a | n/a | n/a | |
| | PC15-OSC32_OUT | RCC_OSC32_OUT | n/a | n/a | n/a | |
| | PH0-OSC_IN | RCC_OSC_IN | n/a | n/a | n/a | |
| | PH1- | RCC_OSC_OUT | n/a | n/a | n/a | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | OSC_OUT | | | | | |
| SYS | PA13 | SYS_JTMS-SWDIO | n/a | n/a | n/a | |
| | PA14 | SYS_JTCK-SWCLK | n/a | n/a | n/a | |
| TIM1 | PA8 | TIM1_CH1 | Alternate Function Push Pull | **Pull-up *** | **High *** | Capture_light |
| TIM5 | PA0-WKUP | TIM5_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | Key_UP |
| TIM9 | PA3 | TIM9_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | DAC_PWM |
| TIM14 | PF9 | TIM14_CH1 | Alternate Function Push Pull | **Pull-down *** | Low | Light_LED0 |
| USART1 | PA9 | USART1_TX | Alternate Function Push Pull | Pull-up | **High *** | USART1_TX |
| | PA10 | USART1_RX | Alternate Function Push Pull | Pull-up | **High *** | USART1_RX |
| USART3 | PB10 | USART3_TX | Alternate Function Push Pull | Pull-up | **High *** | USART3_TX |
| | PB11 | USART3_RX | Alternate Function Push Pull | Pull-up | **High *** | USART3_RX |
| GPIO | PE2 | GPIO_EXTI2 | **External Interrupt Mode with Falling edge trigger detection** | **Pull-up *** | n/a | Key2 |
| | PE3 | GPIO_EXTI3 | **External Interrupt Mode with Falling edge trigger detection** | **Pull-up *** | n/a | Key1 |
| | PE4 | GPIO_EXTI4 | **External Interrupt Mode with Falling edge trigger detection** | **Pull-up *** | n/a | Key0 |
| | PF7 | GPIO_Analog | Analog mode | No pull-up and no pull-down | n/a | Light_Sensor |
| | PF8 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **High *** | BEEP |
| | PF10 | GPIO_Output | Output Push Pull | **Pull-down *** | Low | Light_LED1 |
| | PA4 | GPIO_Analog | Analog mode | No pull-up and no pull-down | n/a | PA4_DAC |
| | PA5 | GPIO_Analog | Analog mode | No pull-up and no pull-down | n/a | Gather_Inf |
| | PB14 | GPIO_Output | Output Push Pull | **Pull-up *** | **High *** | SPI1_CS |
| | PB3 | GPIO_Output | Output Push Pull | **Pull-up *** | **High *** | SPI1_SCK |
| | PB4 | GPIO_Input | Input mode | **Pull-up *** | **n/a** | SPI1_MISO |
| | PB5 | GPIO_Output | Output Push Pull | **Pull-up *** | **High *** | SPI1_MOSI |
| | PB8 | GPIO_Output | Output Push Pull | **Pull-up *** | **High *** | IIC_SCL |
| | PB9 | GPIO_Output | Output Push Pull | **Pull-up *** | **High *** | IIC_SDA |

## 6.2. DMA configuration

| DMA request | Stream | Direction | Priority |
|---|---|---|---|
| DAC1 | DMA1_Stream5 | Memory To Peripheral | Low |
| ADC1 | DMA2_Stream4 | Peripheral To Memory | Low |
| ADC3 | DMA2_Stream0 | Peripheral To Memory | Low |
| SPI2_TX | DMA1_Stream4 | Memory To Peripheral | **High *** |
| I2S2_EXT_RX | DMA1_Stream3 | Peripheral To Memory | **High *** |
| USART1_RX | DMA2_Stream2 | Peripheral To Memory | Low |
| USART3_RX | DMA1_Stream1 | Peripheral To Memory | Low |

### *DAC1: DMA1_Stream5 DMA request Settings:*

| | |
|---|---|
| Mode: | **Circular *** |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | **Word *** |
| Memory Data Width: | **Word *** |

### *ADC1: DMA2_Stream4 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Half Word |
| Memory Data Width: | Half Word |

### *ADC3: DMA2_Stream0 DMA request Settings:*

| | |
|---|---|
| Mode: | **Circular *** |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Half Word |
| Memory Data Width: | Half Word |

### *SPI2_TX: DMA1_Stream4 DMA request Settings:*

| | |
|---|---|
| Mode: | **Circular *** |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | **Half Word *** |
| Memory Data Width: | **Half Word *** |

### *I2S2_EXT_RX: DMA1_Stream3 DMA request Settings:*

| | |
|---|---|
| Mode: | **Circular *** |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | **Half Word *** |
| Memory Data Width: | **Half Word *** |

### *USART1_RX: DMA2_Stream2 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### *USART3_RX: DMA1_Stream1 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

## 6.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 15 | 0 |
| System tick timer | true | 15 | 0 |
| EXTI line2 interrupt | true | 12 | 0 |
| EXTI line3 interrupt | true | 12 | 0 |
| EXTI line4 interrupt | true | 12 | 0 |
| DMA1 stream1 global interrupt | true | 5 | 0 |
| DMA1 stream3 global interrupt | true | 5 | 0 |
| DMA1 stream4 global interrupt | true | 5 | 0 |
| DMA1 stream5 global interrupt | true | 5 | 0 |
| CAN1 RX0 interrupts | true | 5 | 0 |
| TIM1 update interrupt and TIM10 global interrupt | true | 6 | 0 |
| TIM1 capture compare interrupt | true | 6 | 0 |
| TIM2 global interrupt | true | 6 | 0 |
| TIM3 global interrupt | true | 0 | 0 |
| TIM4 global interrupt | true | 7 | 0 |
| USART1 global interrupt | true | 6 | 0 |
| USART3 global interrupt | true | 7 | 0 |
| RTC alarms A and B interrupt through EXTI line 17 | true | 15 | 0 |
| TIM8 trigger and commutation interrupts and TIM14 global interrupt | true | 5 | 0 |
| TIM5 global interrupt | true | 14 | 0 |
| TIM7 global interrupt | true | 5 | 0 |
| DMA2 stream0 global interrupt | true | 5 | 0 |
| DMA2 stream2 global interrupt | true | 5 | 0 |
| DMA2 stream4 global interrupt | true | 5 | 0 |
| Ethernet global interrupt | true | 5 | 0 |
| HASH and RNG global interrupts | true | 15 | 0 |
| PVD interrupt through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| | | | |

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| ADC1, ADC2 and ADC3 global interrupts | unused | | |
| CAN1 TX interrupts | unused | | |
| CAN1 RX1 interrupt | unused | | |
| CAN1 SCE interrupt | unused | | |
| TIM1 break interrupt and TIM9 global interrupt | unused | | |
| TIM1 trigger and commutation interrupts and TIM11 global interrupt | unused | | |
| SPI2 global interrupt | unused | | |
| TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts | unused | | |
| Ethernet wake-up interrupt through EXTI line 19 | unused | | |
| FPU global interrupt | unused | | |

*** User modified value**

# 7. Power Consumption Calculator report

7.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32F4 |
| Line | STM32F407/417 |
| MCU | STM32F407ZGTx |
| Datasheet | 022152_Rev8 |

7.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | 3.3 |

# 8. Software Project

## 8.1. Project Settings

| Name | Value |
|---|---|
| Project Name | STM32F407_FreeRTOS |
| Project Folder | C:\EmbeddedSoftwareWorkSpace\EmbeddedSoftwareDevelop\STM32F407STO |
| Toolchain / IDE | EWARM V8 |
| Firmware Package Name and Version | STM32Cube FW_F4 V1.21.0 |

## 8.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube Firmware Library Package | Copy only the necessary library files |
| Generate peripheral initialization as a pair of '.c/.h' files | Yes |
| Backup previously generated files when re-generating | No |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |

# 9. Software Pack Report