1. Description

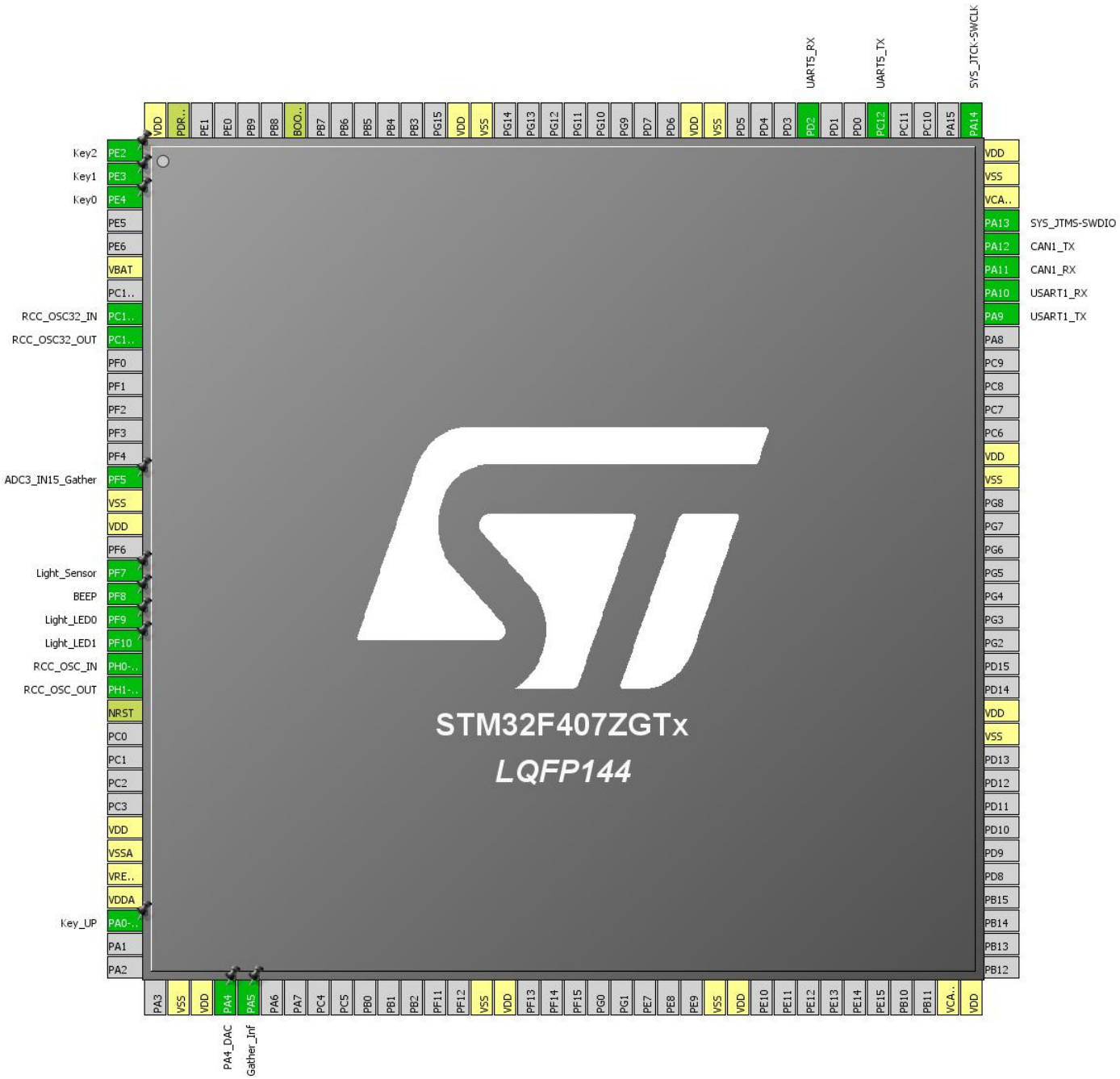
1.1. Project

Project Name	STM32F407_FreeRTOS
Board Name	custom
Generated with:	STM32CubeMX 4.27.0
Date	01/23/2021

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407ZGTx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



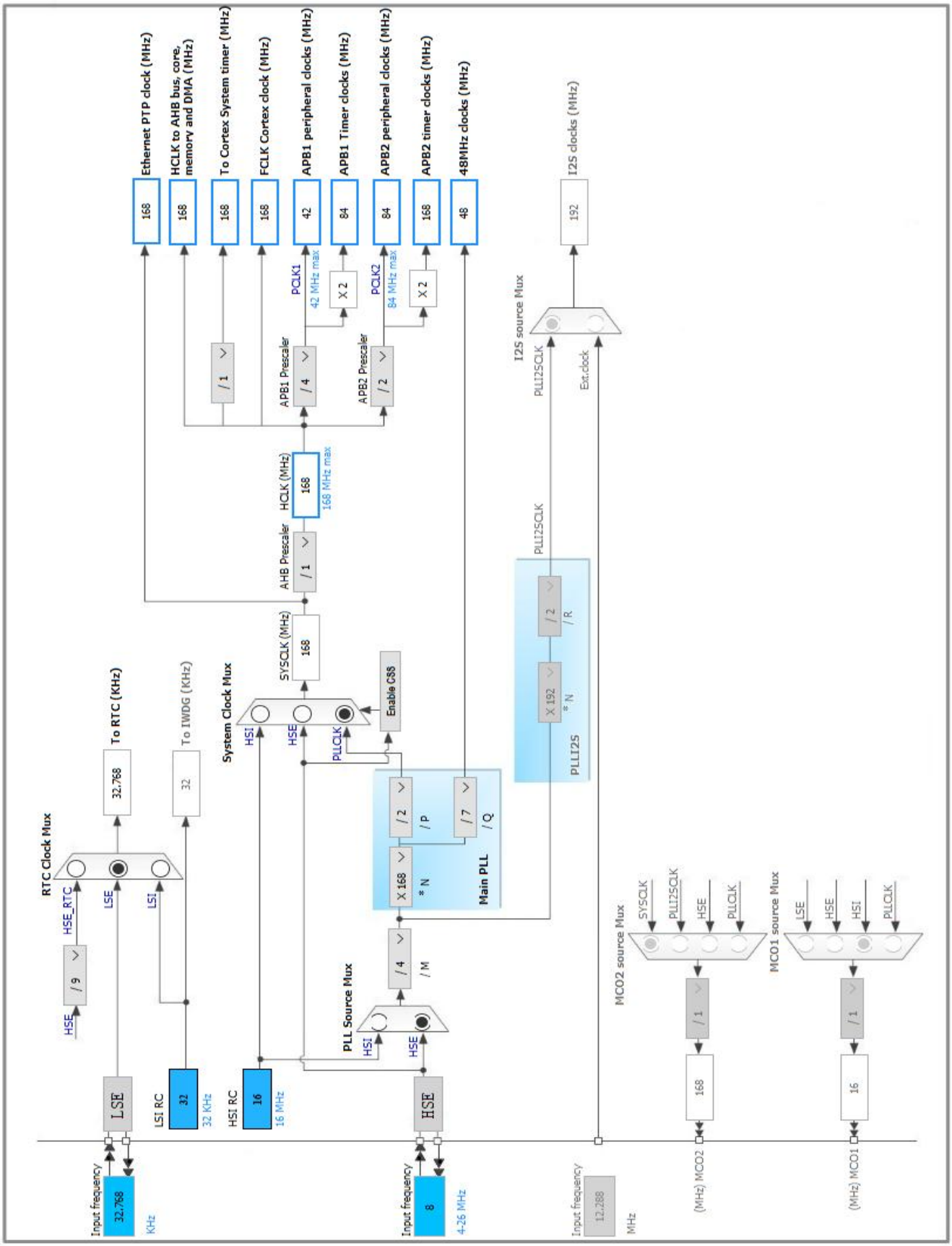
3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	GPIO_EXTI2	Key2
2	PE3	I/O	GPIO_EXTI3	Key1
3	PE4	I/O	GPIO_EXTI4	Key0
6	VBAT	Power		
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
15	PF5	I/O	GPIO_Analog, ADC3_IN15	ADC3_IN15_Gather
16	VSS	Power		
17	VDD	Power		
19	PF7	I/O	GPIO_Analog, ADC3_IN5	Light_Sensor
20	PF8 *	I/O	GPIO_Output	BEEP
21	PF9	I/O	TIM14_CH1	Light_LED0
22	PF10 *	I/O	GPIO_Output	Light_LED1
23	PH0-OSC_IN	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0-WKUP	I/O	TIM5_CH1	Key_UP
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	GPIO_Analog, DAC_OUT1	PA4_DAC
41	PA5	I/O	GPIO_Analog, ADC1_IN5	Gather_Inf
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VCAP_1	Power		
72	VDD	Power		
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDD	Power		
101	PA9	I/O	USART1_TX	USART1_TX

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
102	PA10	I/O	USART1_RX	USART1_RX
103	PA11	I/O	CAN1_RX	CAN1_RX
104	PA12	I/O	CAN1_TX	CAN1_TX
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
113	PC12	I/O	UART5_TX	
116	PD2	I/O	UART5_RX	
120	VSS	Power		
121	VDD	Power		
130	VSS	Power		
131	VDD	Power		
138	BOOT0	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN5

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**Enabled ***
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 5
Sampling Time	**480 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. ADC3

mode: IN5

mode: IN15

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	**2 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 15 ***
Sampling Time	**480 Cycles ***
Rank	**2 ***
Channel	Channel 5
Sampling Time	**480 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.3. CAN1

mode: Mode

5.3.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**7 ***
Time Quantum	**166.66666666666669 ***
Time Quanta in Bit Segment 1	**5 Times ***
Time Quanta in Bit Segment 2	**6 Times ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable

No-Automatic Retransmission	**Enable ***
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

5.4. DAC

mode: OUT1 Configuration

5.4.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	**Disable ***
Trigger	None

5.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

5.6. RNG

mode: Activated

5.7. RTC

mode: Activate Clock Source

mode: Activate Calendar

Alarm A: Internal Alarm

5.7.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	BCD data format
Hours	**22 ***
Minutes	**42 ***
Seconds	**55 ***
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	**Wednesday ***
Month	January
Date	**16 ***
Year	**21 ***

Alarm A:

Hours	**15 ***
Minutes	**18 ***
Seconds	**23 ***
Sub Seconds	0
Alarm Mask Date Week day	Disable
Alarm Mask Hours	Disable
Alarm Mask Minutes	Disable
Alarm Mask Seconds	Disable
Alarm Sub Second Mask	**SS[14:0] are compared and must match to activate alarm. ***
Alarm Date Week Day Sel	**Weekday ***
Alarm Week Day	Monday

5.8. SYS

Debug: Serial Wire

Timebase Source: TIM3

5.9. TIM2

Trigger Source: ITR0

Clock Source : Internal Clock

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**0xFFFFFFFF ***
Internal Clock Division (CKD)	No Division
Slave Mode Controller	Slave mode disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	**Update Event ***

5.10. TIM4

Clock Source : Internal Clock

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**8400-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.11. TIM5

Trigger Source: ITR0

mode: Clock Source

Channel1: Input Capture direct mode

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**84 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**0xFFFFFFFF ***
Internal Clock Division (CKD)	No Division
Slave Mode Controller	Slave mode disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	**Update Event ***

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.12. TIM7

mode: Activated

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**84-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1 ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.13. TIM14

mode: Activated

Channel1: PWM Generation CH1

5.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**42 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**500 ***
Internal Clock Division (CKD)	No Division

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	**Low ***

5.14. UART5

Mode: Asynchronous

5.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.15. USART1

Mode: Asynchronous

5.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.16. FREERTOS

mode: Enabled

5.16.1. Config parameters:

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.16.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA5	ADC1_IN5	Analog mode	No pull-up and no pull-down	n/a	Gather_Inf
ADC3	PF5	ADC3_IN15	Analog mode	No pull-up and no pull-down	n/a	ADC3_IN15_Gather
	PF7	ADC3_IN5	Analog mode	No pull-up and no pull-down	n/a	Light_Sensor
CAN1	PA11	CAN1_RX	Alternate Function Push Pull	**Pull-up ***	**High ***	CAN1_RX
	PA12	CAN1_TX	Alternate Function Push Pull	**Pull-up ***	**High ***	CAN1_TX
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	PA4_DAC
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM5	PA0-WKUP	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	Key_UP
TIM14	PF9	TIM14_CH1	Alternate Function Push Pull	**Pull-down ***	Low	Light_LED0
UART5	PC12	UART5_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PD2	UART5_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**High ***	USART1_TX
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**High ***	USART1_RX
GPIO	PE2	GPIO_EXTI2	**External Interrupt Mode with Falling edge trigger detection**	**Pull-up ***	n/a	Key2
	PE3	GPIO_EXTI3	**External Interrupt Mode with Falling edge trigger detection**	**Pull-up ***	n/a	Key1
	PE4	GPIO_EXTI4	**External Interrupt Mode with Falling**	**Pull-up ***	n/a	Key0

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
			edge trigger detection			
	PF5	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	ADC3_IN15_Gather
	PF7	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	Light_Sensor
	PF8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	BEEP
	PF10	GPIO_Output	Output Push Pull	**Pull-down ***	Low	Light_LED1
	PA4	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	PA4_DAC
	PA5	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	Gather_Inf

6.2. DMA configuration

DMA request	Stream	Direction	Priority
UART5_RX	DMA1_Stream0	Peripheral To Memory	Low
UART5_TX	DMA1_Stream7	Memory To Peripheral	Low
USART1_RX	DMA2_Stream2	Peripheral To Memory	Low
USART1_TX	DMA2_Stream7	Memory To Peripheral	Low
ADC3	DMA2_Stream1	Peripheral To Memory	Low
ADC1	DMA2_Stream0	Peripheral To Memory	Low
DAC1	DMA1_Stream5	Memory To Peripheral	Low

UART5_RX: DMA1_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART5_TX: DMA1_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_RX: DMA2_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_TX: DMA2_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC3: DMA2_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

DAC1: DMA1_Stream5 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
EXTI line2 interrupt	true	12	0
EXTI line3 interrupt	true	12	0
EXTI line4 interrupt	true	12	0
DMA1 stream0 global interrupt	true	5	0
DMA1 stream5 global interrupt	true	5	0
CAN1 RX0 interrupts	true	5	0
TIM2 global interrupt	true	6	0
TIM3 global interrupt	true	0	0
TIM4 global interrupt	true	7	0
USART1 global interrupt	true	6	0
RTC alarms A and B interrupt through EXTI line 17	true	15	0
TIM8 trigger and commutation interrupts and TIM14 global interrupt	true	5	0
DMA1 stream7 global interrupt	true	5	0
TIM5 global interrupt	true	14	0
UART5 global interrupt	true	15	0
TIM7 global interrupt	true	5	0
DMA2 stream0 global interrupt	true	6	0
DMA2 stream1 global interrupt	true	6	0
DMA2 stream2 global interrupt	true	6	0
DMA2 stream7 global interrupt	true	6	0
HASH and RNG global interrupts	true	15	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
CAN1 TX interrupts	unused		
CAN1 RX1 interrupt	unused		
CAN1 SCE interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407ZGTx
Datasheet	022152_Rev8

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	STM32F407_FreeRTOS
Project Folder	C:\EmbeddedSoftwareWorkSpace\EmbeddedSoftwareDevelop\STM32F407STO
Toolchain / IDE	EWARM V8
Firmware Package Name and Version	STM32Cube FW_F4 V1.21.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report