LINEAR TECHNOLOGY

Application Note 41

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Questions and Answers on the SPICE Macromodel Library

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INTRODUCTION

This document is provided to answer some of the potential questions raised about the Linear Technology SPICE macromodel library. It assumes that you have a diskette copy of the library already, and want some background and/or additional information. Those needing a copy of the current SPICE macromodel diskette may obtain one by calling (800) 637-5545. The macromodel library is available on IBM PC format (high density) diskettes, in either 5.25″ or 3.5″ styles. If you should have a question not answered by this text, you may call LTC applications at (408) 432-1900. For more general SPICE questions, references are provided.

GETTING STARTED

Question (1): What hardware and software do I need to get the LTC SPICE model package up and running?

Answer (1): Obviously, you first need an IBM PC compatible computer with a high density drive, either 5.25″ or 3.5″. Beyond that, you will need only a minimal amount of RAM (512k or more). With this SPICE macromodel diskette, we have not just given you a model library, we have also furnished a working demo copy of PSpice™ from MicroSim, right on the diskette with our model software. To run this demo copy of PSpice, there are no minimum CPU speed, display or printer requirements. Unlike the production version, this special version of PSpice does not require a coprocessor to run, so you can see the models at work almost immediately, with no configuration or file editing necessary.

The demo PSpice version will run up to two models at once. To see it operate, all you need to do is slide the diskette into your computer, log onto the A: drive, and type in: "DEMOLTC <Enter>". The rest is all automatic!

Question (2): That sounds a bit too easy. Isn't there some configuration necessary to run SPICE? Also, is there some "on diskette" help available?

Answer (2): To minimize the configuration necessary for PSpice, the graphics display Probe™ comes pre-configured for a "text" style of screen display, one which will display a plot on any monitor. Once you get your feet wet, you will want to edit the Probe configuration file, "PROBE.DEV" to better match your equipment (this file is in the SPICE directory).

Yes, there are two help files on the diskette. One, "README.COM" is in the root directory, and it lists the specific LTC device types modeled. To use it type "README <Enter>", then just follow the on screen prompts. The information can also be printed out, if desired. The second help utility is "README2.COM", and it is in the SPICE directory. It has information on PSpice and Probe in general, and this demo version in particular. From the SPICE directory, type "README2 <Enter>" to use it, and follow the prompts. Note that this help file has the detailed info needed to customize "PROBE.DEV", with an ASCII editor. We recommend printing out the information in both of these help utilities for future reference.

Question (3): Where can I get more information on PSpice and Probe?

Answer (3): The two help utilities mentioned will serve you here, or write or call MicroSim (mentioning this demo diskette) at:

MicroSim Corporation
20 Fairbanks, Irvine, CA 92718
(714) 770-3022

Question (4): Will the devices in this LTC macromodel library run on any version of SPICE? Are they copy protected or encrypted?

Answer (4): You can use the LTC models with other versions of SPICE, either on a PC or another computer system. All of the LTC SPICE model files are furnished in an ASCII file format, which are actually usable on any type of computer; a PC, a workstation and/or mainframes. If you don't intend final use for them on a PC, they can be transferred from the PC environment to a dissimilar system via modem, using an error checking protocol (such as Xmodem or Kermit).

As was noted, the models are in ASCII form, and are designed to be Berkeley SPICE 2G.6 compatible (generic SPICE). They were in fact developed and debugged using PSpice, but other vendors' PC based SPICE implementations can be used with them, and they will also work on workstations and large mainframes (once transferred). So, while we can recommend PSpice as highly useful, the generic nature of our models allows their use on virtually any 2G.6 compatible host.

Since the models are ASCII files, they are easily copied, and we encourage use on diverse systems. Model encryption, in our opinion, is counter-productive to our goals of widespread LTC model use. In fact, it could be said that it is contrary to a "universal" SPICE 2G.6 ASCII file format.

MODEL COVERAGE

Question (5): How many of the LTC linear devices are now included in the SPICE macromodel library, and what device types are covered?

Answer (5): Right now, most of the LTC operational amplifier models are already contained in the library. This collection of 40-odd part numbers includes NPN and PNP bipolar and JFET input amplifier types. There is also an instrumentation amplifier, and it is hoped that more amplifiers will soon follow. Other linear devices (comparators, A/Ds, references, regulators) are not modeled as yet.

MODEL SUPPORT

Question (6): If your models are in fact ASCII files, that means they are easily edited and changed. Does this mean that I can "tweak" a model to suit my own specific needs?

Answer (6): You sure can edit the models, but you'd better understand all the implications of it before doing so! Modifying a model by definition makes it something other than what it was when released. Please note that LTC will only support models in their released form, and at our discretion. Does this then mean that you won't ever be able to make useful model changes? Not really, if you just use common sense, and keep an original reference copy of the model, in "as received" form. Common sense means that you don't change 10 model parameters, then call us up and ask why "our" model doesn't fly. LTC (or any other IC vendor) won't step into such a Pandora's box!

Question (7): What if I really do have a problem with the models? Will I be able to get help from LTC?

Answer (7): Problems using SPICE models will generally fall into one of three types: 1) Problems with the user's system which are hardware and/or software related, 2) Problems of application, that is a circuit application which presents some general modeling difficulty. Or, in some circumstance, 3) A real problem with the model itself. Obviously LTC cannot be responsible for the correct operation of your computer system and application of your software, so we will not become involved with case 1). Case 3), problems which can be directly attributed to an LTC model will be serviced at the discretion of LTC.

Case 2) is the most difficult of all, since it can actually be open-ended, with no practical solution. For example, you may need to simulate a circuit using an LTC model, but some other crucial part is not modeled, say something from another vendor. While we can sympathize with this dilemma, we could not logically be expected to help develop such a model. Due to time and manpower realities, we may not even be able to help develop a new model for one of our own parts (on short notice). More on this and related areas is answered in the next two questions.

Question (8): Are these models guaranteed to run?

Answer (8): Users should bear in mind that software models are at their very best just approximations of the real thing, that is they amount to clever apings of actual ICs. LTC does guarantee (and fully supports) its IC devices, the ones you plug in to do genuine work on your PC boards. By way of contrast, models are software support items, and are supplied on an "as is" basis. With regard to their use and performance, they should never be confused with the performance of the real item. Think about this as in the context of what gets shipped out your door as product, that is real, and measured performance results on it validates your equipment guarantees. Model results will likely mean little or nothing to your customers, since they are much less tangible to your product.

Question (9): What if a model functions, but it simply doesn't reveal everything I want it to?

Answer (9): It is entirely possible that a given model may fall short of specific expectations, especially if they tend towards the unrealistic or the impractical. We don't get paranoid when a real op amp has finite gain as opposed to infinite, we consider the implications in context and proceed from there. It is simply impractical (at least at this point in modeling evolution) to make a macromodel emulate a device's specs with 100% fidelity in all regards, and still remain compact, fast running, and free of convergence problems.

What we have done in developing these models is to take into account all those performance/spec areas we saw as most important, and then pay serious attention to them in the models. Granted, this is a judgement call on our part, but we hope it is a reasonable one. This does not rule out special cases, where a model may be optimized to satisfy a given set of customer requirements, and LTC will respond to these as they arise. And, we will welcome inputs on future models!

PARAMETERS MODELED

Question (10): OK then, what are the specific performance areas and specifications which these models do cover?

Answer (10): The LTC op amp macromodels simulate a number of performance areas and specs, as noted in Table 1. We have chosen typical parameters from the device datasheet in generating these models, and room temperature operation.

Table 1.

SPECIFICATION	MODELED?	MODELING ACCURACY
V_{OS}	Yes	High
I_B/I_{OS}	Yes	High
Gain-bandwidth	Yes	Medium
Phase margin	Yes	Medium
SR	Yes	Medium
AV (dc)	Yes	High
CMRR	Yes	High
PSRR	No	NA
V_{SAT} (+ and −)	Yes	High
I_{SC}	Yes	High
R_{OUT}	Yes	High
I_q	Yes	High
en	No*	NA
in	No*	NA

*The model topology used does not address input stage noise simulation. Use the LTC "NOISE" software instead, which does model the LTC op amps for voltage and current noise (see question 20).

In addition, there are functional areas of performance where modeling attention should be directed for realistic behavior. For example, if an op amp is designed as a single-supply device, then the input/output ranges of the model should include the V^- rail (ground), with good accuracy. If clamping networks are used at the input, then the model should reflect this, and clamp at the same level. If the amplifier is pole-zero compensated, its transient response will not resemble a classic single pole plus parasitic rolloff, and the model should address this. Table 2 summarizes the LTC model characteristics in these functional regards.

Table 2.

CHARACTERISTIC	MODELED?	MODELING ACCURACY
Multiple pole/zero	Yes	Medium
Single supply op.	Yes	High
Common-mode clamps	Yes	Medium
Differential clamps	Yes	Medium

MODEL TOPOLOGY

Question (11): Sometimes it appears that the terms "model" and "macromodel" are being used interchangeably. Is there a difference, and what defines a macromodel?

Answer (11): "Model" is a general term, and a "macromodel" is a specific model form, one which is more compact and efficient. To be historically precise, the op amp macromodel was devised by Boyle[1] originally, and has been used since then. An op amp macromodel differs from a full "device level" model in that key parts of the circuit are defined by the use of synthetic SPICE elements, that is controlled current/voltage sources, etc., along with passive circuit elements such as Rs and Cs, and a minimum number of (simplified) semiconductors. By reducing the number of semiconductor junctions to a minimum, an op amp macromodel can achieve simulation times 5 to 10 times faster than a device level model, and so easily allow multiple amplifier simulations for large systems.

Question (12): This sounds like an area of tradeoff! Certainly a macromodel using synthesized elements cannot perform like a real device level model, can it?

Answer (12): For many aspects of performance, one cannot tell that macromodeling has been used. For any performance aspect with simulation speed as a criterion, a macromodel approach will almost always be faster, and with reasonable fidelity, *when properly executed.* A qualifying note here . . . comparatively speaking, we will rule out a SPICE "ideal" op amp model, which can be built with one or a few controlled sources. We feel this is too far removed from a real IC op amp, as it will be devoid of real bias currents, offset voltages, slew rates, etc.

The most useful macromodel approach is one which carefully balances the mutual goals of reasonable fidelity to the real part, along with a realistic simulation time, and finally the overall vigor or robustness of the model. The importance of the first two of these points cannot be overemphasized in considering the evolution of op amp macromodeling. As a case in point, it is not a widely useful thing to improve say, the fidelity of an op amp's transient response with a complex model which departs from the simplicity and speed advantages of a more basic model. In the extreme, one might find a board's worth of "more sophisticated" op amp models which takes all night to run simulations, or worst yet, won't run at all!

Question (13): What is meant by "won't run at all?" Is that related to the reported convergence problems of SPICE?

Answer (13): Yes, there are macromodel types which have been published which have problems with SPICE convergence for certain types of simulations. In the extreme case, a solution cannot be found and the simulator just quits, reporting an error. "Tweaking" of the simulator defaults may be necessary to make it run, and then slowly. Try a unity-gain follower small signal transient analysis to separate the macromodel wheat-from-chaff, and to see what a "robust" macromodel implies.

To our minds, it is simply not enough that a model yield good fidelity with the electrical results, it should also do so with reasonable speed and not be overly sensitive to system memory, applied signal, biasing, and/or supply voltages. So, we have purposely included a transient test for the LT1007 (one of our more complex models) in our demo to illustrate this point. We will be interested to learn of comparative tests, using other models (see Appendix).

THE BOYLE MODEL AND LTC IMPROVEMENTS

Question (14): We take it then, that your LTC models are based on the Boyle macromodel. Is it true that this model cannot handle differing transistor types, and that it has other serious deficiencies?

Answer (14): Yes, the LTC macromodels are in fact derived from the basic Boyle model. We should hasten at this point to note that this model is apparently little understood in terms of real versus perceived limits! In fact, many Boyle derived models (and we include LTC's here) are related topologically, but have been enhanced in many different and significant ways. Perhaps a fitting analogy is that all present day cars using internal combustion engines are in a sense related to Henry Ford's Model T. This

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Note 1: Boyle, G.R., Cohn, B.M., Pederson, D.O., Solomon, J.E. "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. SC-9, #6, December 1974.

is of course intentionally dramatized to make the following point: Most of us will have no trouble at all appreciating that a basic design concept can be usefully enhanced in many aspects, while still retaining a fundamental lineage.

Yes, the original Boyle model used NPN bipolar input stage transistors, in the context of a 741. But replacing them with PNP types simply changes the connections, not the basic design equations. FET transistors were added to the Boyle model in 1979, in the paper by Krajewska and Holmes,[2] in both JFET and MOSFET form. Anyone implying that a Boyle-based model can't handle a variety of transistor types is confused as to history!

Question (15): But the Boyle model cannot handle multiple poles and zeros, and is therefore not suited for accurate transient response simulations. Some companies have discarded that approach long ago. How can you guys still be using it, with all those problems?

Answer (15): The LTC macromodels were developed with an attitude that transient response fidelity, while important, should not necessarily be achieved at the expense of many other equally critical performance areas. Accordingly, LTC macromodels use extensions to the overall Boyle topology for additional poles and zeros, as opposed to discarding it outright. This technique allows additional control over phase response, while still retaining relative simplicity. The LT1007 demo example cited uses this form of compensation, and the results can be seen in the demo example (see Appendix). This approach does have the virtue of still retaining the overall form of the Boyle topology. While it may be possible to more accurately simulate an OP-27, for example, with up to 10 pole-zero pair networks, a legitimate question arises: Is it worth the substantial overhead of the many additional active stages, for each and every simulation, however trivial? Every element added to a SPICE macromodel extracts some penalty in terms of speed, memory required, or overall model vigor. Carried to the extreme, significantly more complex models may even preclude multiple amplifier simulations, defeating the very purpose of macromodeling.

Question (16): The last statement seems to be a contradiction, as you have added additional networks, diode clamps, and entire circuit sections to model the unique internal features of your op amps. If you question others adding additional stages, how then can you justify it?

Answer (16): The answer lies in exactly how one goes about it! We certainly do recognize the potential penalties these added features can represent to users who simply may not care about a particular detail which they may be simulating. So, we have generally implemented them in ways which allow them to be easily disconnected. For example, the diode clamps at the inputs of the LT1078 series can be disconnected if they get in the way, as can the differential clamps for the LT1007 (and others). In other words, we haven't locked anyone away from stripping the model bare, so to speak, should they so wish. In most instances, a "*" in column one of a line is all that is needed to deactivate it.

Question (17): The Boyle model uses a ground node internally, node zero (node 0). Isn't it true that this creates simulation errors for power supply and load currents?

Answer (17): The model we use does have a node zero internally, which happens to be the default common (ground, or node 0) for SPICE circuits in general. The output signal current of our models therefore flows through this common node, and to/from the common node of the overall circuit in which it is used. Usually this is a common ground between source(s) and the load(s).

In our models (and most others which operate similarly) the actual model output current comes from controlled sources, which are referred to ground (node 0), inside the model. To an extent, this node voltage can be somewhat arbitrary; that is, it is possible for it to be referred to other points, and the model will still operate normally. For example, the "node 0" in single-supply op amps such as the LT1078 series gets tied to V^- in the main circuit, when the device is used in a single-supply mode (since the V^- pin, #4 is tied to ground). All still works OK in this fashion. If the very same model is used with dual supplies, obviously "node 0" gets referred to a level which is intermediate between the two supply levels, such as + 15V and – 15V.

Note 2: Krajewska, G., Holmes, F.E. "Macromodeling of FET/Bipolar Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. SC-14, #6, December 1979.

A better understanding of how this operates can be realized if it is appreciated that the SPICE controlled sources do indeed have two terminal floating outputs, which can be referred to various levels. Thus, the op amp's output (load) current can actually be different from the power supply rail current, for the case where the internal common node (node 0) is not tied to a supply rail.

Is all of this a real problem? It actually becomes more one of bookkeeping, or adding up all the currents properly. We hope it is then not a great one, since the total current drain will still be that in the load, plus the static drain of the op amp itself. We have taken the step of making all the models reflect an internal DC power supply current which is that value typical to their operation (the real LT1007 draws 2.7mA, therefore Iee + Ip totals 2.7mA in the model).

SOME GENERAL SPICE QUESTIONS

Question (18): All of this seems to be implying that SPICE simulations can be quite burdensome, in terms of getting up and running to a point of realizing useful results. What can be said about this aspect to someone just getting started with modeling?

Answer (18): SPICE simulation is unquestionably very involved, and it is also quite demanding of analog circuit skills along with general computer proficiency. It is just as demanding of the computer hardware as well. While you don't need to be a programmer to use SPICE efficiently, well developed computer skills definitely do help. More important to overall effectiveness however is a strong design engineering background, in particular one in analog circuit design.

This should seem obvious, since SPICE is an analog simulator. But, it is being stressed here to make the point that someone proficient in analog design will likely produce quality SPICE results much faster than one equally proficient in digital design, with both starting from zero. Why? Because SPICE has its quirks, which must be dealt with to use it most effectively. By and large, there are often analogs between SPICE software problems and linear circuit problems. Thus, it helps in dealing with these types of problems to be comfortable in "thinking analog." Analog designers also tend to be well-developed in terms of patience, and SPICE if nothing else will be a challenge to one's patience!

These generalizations aside, SPICE will definitely be most demanding of hardware, as the bigger and faster the computer, the more quickly you get your results. The PSpice demo supplied with this macromodel library is quite exceptional in terms of what it does, but this does not change the fact that the full version counterpart is more demanding on the hardware. In the SPICE world, hardware dollars for RAM, coprocessors, and faster CPUs buy overall speed and complex circuit capability.

Question (19): OK, assuming that these general requirements can be met, what other potential bottlenecks lie in the path of my trip towards SPICE bliss?

Answer (19): Given adequate resources in terms of manpower and computer hardware/software, the next fundamental obstacle is the availability and quality of models. One certainly wouldn't want to build up a breadboard circuit faced with the necessity to make all the op amps up from scratch, but that is where you'd stand for a SPICE simulation without adequate models. Even assuming you had the time and manpower resources to make your own models, there is the very real question of their technical sufficiency.

Now, this actually brings us full circle, with the IC manufacturer such as LTC entering the picture as a supplier of op amp models for their catalog of devices. With this circumstance, you, as an IC user, are in the very best position to do useful simulations, since it is in the IC manufacturers interest to supply you with models that reasonably reflect actual device performance. This establishes your confidence in the devices as well as speeding your design towards completion, with a minimum of hassle with models.

Of course, this does not make the modeling problem go completely away, it only lessens it appreciably, with regard to LTC as one vendor. You still need models for all parts of your circuit, beyond the op amps. This will very likely continue to be a serious challenge in the months and years ahead, as more and more vendors become active with modeling support of their devices.

Question (20): The bottom line seems to be that the SPICE user in today's design world has their work really cut out for them. What level of confidence can be expected with SPICE op amp simulations, given typical designs and your models?

Answer (20): SPICE simulation results can and will vary in fidelity with regard to a real live op amp, dependent upon the type of circuit in use. Generally speaking, DC and low frequency AC results are good to excellent, and the models do a nice job with bias currents, offset voltages, and most input related parameters. By contrast, noise is not modeled well at all with the enhanced Boyle topology we employ, but we do provide a useful option here, in the form of the alternative software, Alan Rich's program "NOISE"[3] (available as noted).

The high frequency response of LTC wideband op amps such as the LT1007 and OP-27 is modeled with multiple poles and zeros, which yields a reasonable approximation to the real device's transient response (see demo). It is worthwhile noting that the precise pulse fidelity of a single given sample of a wideband amplifier is in reality a "moving-target." This is because device-to-device production variations can be of the same degree as the errors in their current modeling! Therefore, there is some question as to just what benefit a more precise high frequency model would provide.

The particular performance area of transient response has been and will continue to be one of challenge in terms of better models (without pitfalls). It is also likely to continue as one of controversy, in terms of the best overall solution to the technical challenge.

Note 3: Rich A. "Noise Calculation in Op Amp Circuits," LTC Design Note #15, September, 1988. (Program available on diskette, call (800) 637-5545).

Output stage performance of the LTC models is good to excellent, with accurate current and voltage limits, and good simulation of the small signal characteristics, particularly the single supply devices near the rails.

All-in-all, we feel that this model collection is a quite useful addition to the analog designer's bag of tricks. Like the SPICE program itself, the models are no panacea, and they need to be used carefully and wisely. You will very likely encounter many crossroads with SPICE models, and often be tempted to decide between the lab results and a SPICE simulation . . . which one to believe? Our advice here is to not accept either without first carefully checking, but do be inclined to lean towards the lab performance of the real device, particularly if it passes all the conventional analog bench tests . . . Remember, that is real by default, while SPICE is a mimic by default!

We hope that the LTC models serve you well, and welcome your feedback on them.

SOME GENERAL SPICE REFERENCES

1. Nagel L.W., Pederson, D.O. "Simulation Program with Integrated Circuit Emphasis (SPICE)," University CA @ Berkeley, ERL-M382, 1973.
2. Nagel, L.W. "SPICE2: A Computer Program to Simulate Semiconductor Circuits," University CA @ Berkeley, ERL-M520, 1975.
3. Cohen, E. "Program Reference for SPICE2," University CA @ Berkeley, ERL-M592, 1976.

Available from:

EECS/ERL Industrial Support Office
497 Cory Hall, University CA @ Berkeley
Berkeley, CA 94720

APPENDIX

The LT1007 Op Amp Macromodel Transient Test Demonstration

03/02/90 ★★ Evaluation PSpice (LT 3.06) ★★ 08:41:27

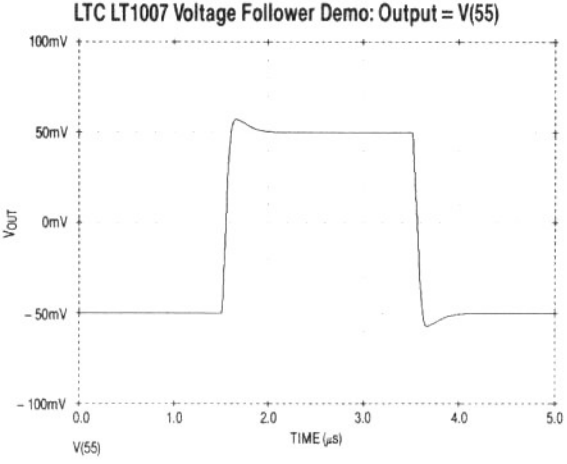
LTC LT1007 VOLTAGE FOLLOWER DEMO: OUTPUT = V(55)

(edited for clarity/brevity; comments italicized)

MATRIX SOLUTION	6.09	4
MATRIX LOAD	8.74	
READIN	2.48	
SETUP	0.05	
DC SWEEP	0.00	0
BIAS POINT	1.98	32
AC and NOISE	0.00	0
TRANSIENT ANALYSIS	22.41	455
OUTPUT	0.22	
TOTAL JOB TIME	26.53	

Shown above are (edited) portions of an actual output file, "DEMO.OUT," as run from files on a released LTC SPICE macromodel diskette. The test is a small signal, voltage follower transient test. The computer used is a 16 megahertz 386 w/387 math coprocessor, and the times shown in the left column reflect operation from a RAM disc. Actual running times for other situations will vary. We invite relative comparisons using other models for this same transient test (edit "DEMO.CIR," to include your comparison model).

Shown below is the LT1007 test waveform simulated in this transient analysis, as seen on the screen.



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