

Step-Down Switching Regulators

Jim Williams

A substantial percentage of regulator requirements involve stepping down the primary voltage. Although linear regulators can do this, they cannot achieve the efficiency of switching based approaches¹. The theory supporting step-down (“buck”) switching regulation is well established, and has been exploited for some time. Convenient, easily applied ICs allowing implementation of practical circuits are, however, relatively new. These devices permit broad application of step-down regulation with minimal complexity and low cost. Additionally, more complex functions incorporating step-down regulation become realizable.

Basic Step Down Circuit

Figure 1 is a conceptual voltage step-down or “buck” circuit. When the switch closes the input voltage appears at the inductor. Current flowing through the inductor-capacitor combination builds over time. When the switch opens current flow ceases and the magnetic field around the inductor collapses. Faraday teaches that the voltage induced by the collapsing magnetic field is opposite to the originally applied voltage. As such, the inductor’s left side heads negative and is clamped by the diode. The capacitors accumulated charge has no discharge path, and a DC potential appears at the output. This DC potential is lower than the input because the inductor limits current during the switch’s on-time. Ideally, there are no dissipative elements in this voltage step-down conversion. Although the output voltage is lower than the input, there is no energy

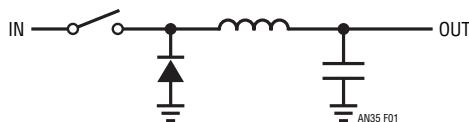


Figure 1. Conceptual Voltage Step-Down (“Buck”) Circuit

lost in this voltage-to-current-to-magnetic field-to-current-to-charge-to-voltage conversion. In practice, the circuit elements have losses, but step-down efficiency is still higher than with inherently dissipative (e.g., voltage divider) approaches. Figure 2 feedback controls the basic circuit to regulate output voltage. In this case switch on-time (e.g., inductor charge time) is varied to maintain the output against changes in input or loading.

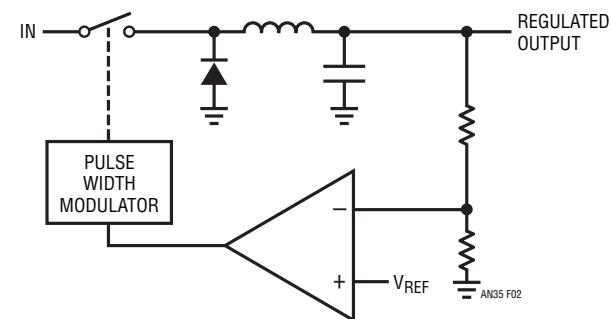


Figure 2. Conceptual Feedback Controlled Step-Down Regulator

Practical Step-Down Switching Regulator

Figure 3, a practical circuit using the LT[®]1074² IC regulator, shows similarities to the conceptual regulator. Some new elements have also appeared. Components at the LT1074’s “V_{COMP}” pin control the IC’s frequency compensation, stabilizing the feedback loop. The feedback resistors are selected to force the “feedback” pin to the device’s internal 2.5V reference value. Figure 4 shows operating waveforms for the regulator at V_{IN} = 28V with a 5V, 1A load.

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Note 1: While linear regulators cannot compete with switchers, they can achieve significantly better efficiencies than generally supposed. See LTC Application Note 32, “High Efficiency Linear Regulators,” for details.

Note 2: See Appendix A for details on this device.

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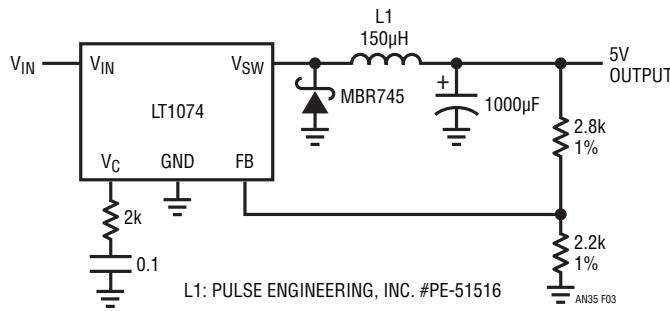


Figure 3. A Practical Step-Down Regulator Using the LT1074

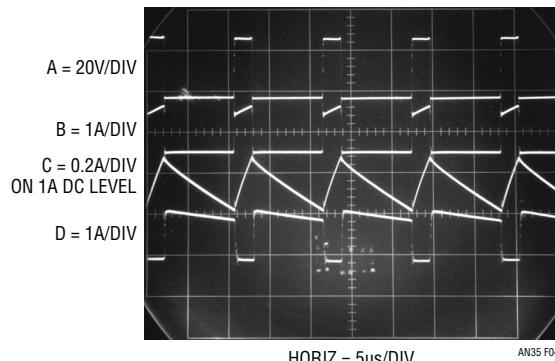


Figure 4. Waveforms for the Step-Down Regulator at $V_{IN} = 28V$ and $V_{OUT} = 5V$ at 1A

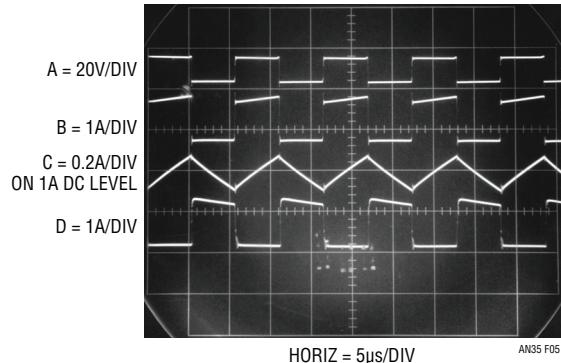


Figure 5. Waveforms for the Step-Down Regulator at $V_{IN} = 12V$ and $V_{OUT} = 5V$ at 1A

Trace A is the V_{SW} pin voltage and Trace B is its current. Inductor current³ appears in Trace C and diode current is Trace D. Examination of the current waveforms allows determination of the V_{SW} and diode path contributions to inductor current. Note that the inductor current's waveform occurs on top of a 1A DC level. Figure 5 shows significant duty cycle changes when V_{IN} is reduced to 12V. The lower input voltage requires longer inductor charge times to maintain the output. The LT1074 controls inductor charge characteristics (see Appendix A for operating details), with resulting waveform shape and time proportioning changes.

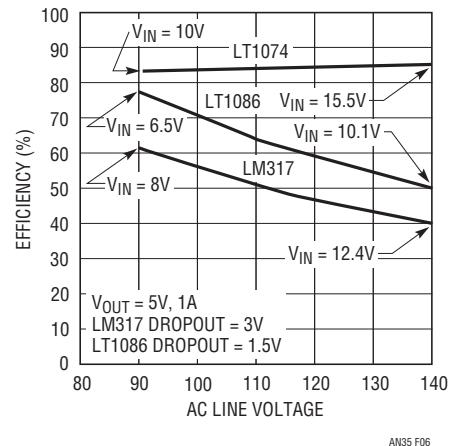


Figure 6. Efficiency vs AC Line Voltage for the LT1074, LT1086 and LM317 Linear Regulators are Shown for Comparison

Figure 6 compares this circuit's efficiency with linear regulators in a common and important situation. Efficient regulation under varying AC line conditions is a frequent requirement. The figure assumes the AC line has been transformed down to acceptable input voltages. The input voltages shown correspond to the AC line voltages given on the horizontal axis. Efficiency for the LM317 and LT1086 linear regulators suffers over the wide input range.

Note 3: Methods for selecting appropriate inductors are discussed in Appendix B.

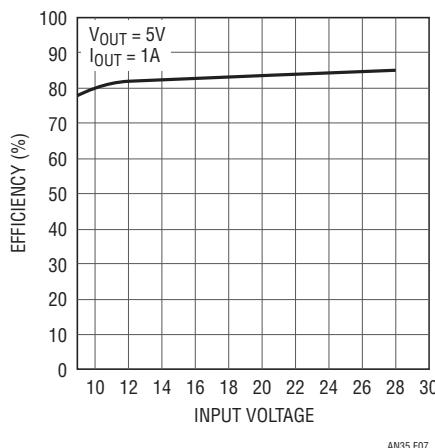


Figure 7. Efficiency Plot for Figure 3. Higher Input Voltages Minimize Effects of Saturation Losses, Resulting in Increased Efficiency

The LT1086 is notably better because its lower dropout voltage cuts dissipation over the range. Switching pre-regulation⁴ can reduce these losses, but cannot equal the LT1074's performance. The plot shows minimum efficiency of 83%, with some improvement over the full AC line excursion. Figure 7 details performance. Efficiency approaches 90% as input voltage rises. This is due to minimization of the effects of fixed diode and LT1074 junction losses as input increases. At low inputs these losses are a higher percentage of available supply, degrading efficiency. Higher inputs make the fixed losses a smaller percentage, improving efficiency. Appendix D presents detail on optimizing circuitry for efficiency.

Dual Output Step-Down Regulator

Figure 8, a logical extension of the basic step-down converter, provides positive and negative outputs. The circuit is essentially identical to Figure 3's basic converter with the addition of a coupled winding to L1. This floating winding's output is rectified, filtered and regulated to a -5V output. The floating bias to the LT1086 positive voltage regulator permits negative outputs by assigning the regulator's output terminal to ground. Negative output power is set by flux pick-up from L1's driven winding. With a 2A load at the +15 output the -5V output can supply over 500mA. Because L1's secondary winding is floating its output may be referred to any point within the breakdown capability of the device. Hence, the secondary output could be 5V or, if stacked on the +15 output, 20V.

Negative Output Regulators

Negative outputs can also be obtained with a simple 2-terminal inductor. Figure 9 demonstrates this by essentially grounding the inductor and steering the catch diodes negative current to the output. A1 facilitates loop closure by providing a scaled inversion of the negative output to the LT1074's feedback pin. The 1% resistors set the scale factor (e.g., output voltage) and the RC network around A1 gives frequency compensation. Waveforms for this circuit are reminiscent of Figure 5, with the exception that diode

Note 4: See Reference 1.

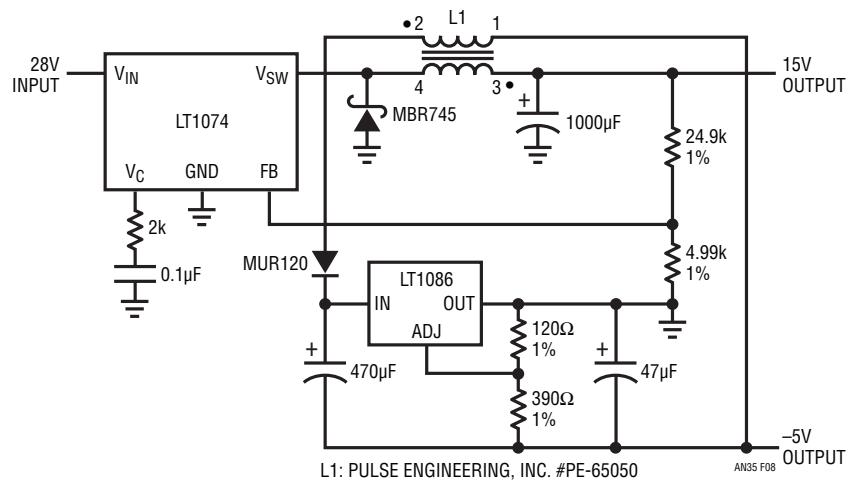


Figure 8. Coupled Inductor Provides Positive and Negative Outputs

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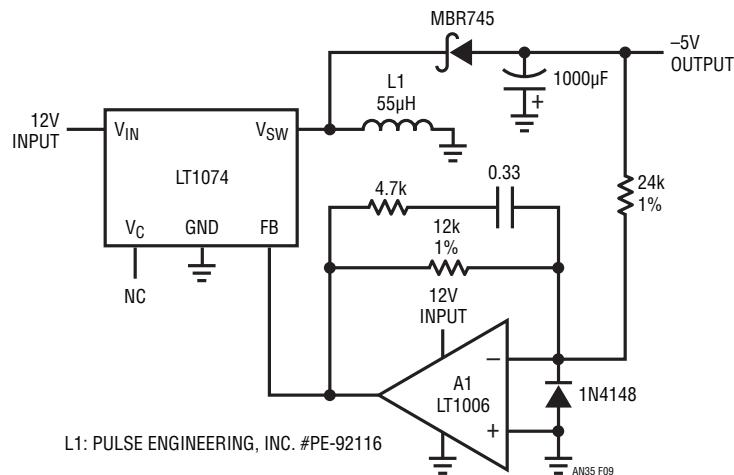


Figure 9. A Negative Output Step-Down Regulator

current (Trace D) is negative. Traces A, B and C are V_{SW} voltage, inductor current and V_{SW} current respectively.

Figure 11, commonly referred to as “Nelson’s Circuit,” provides the same function as the previous circuit, but eliminates the level-shifting op amp. This design accomplishes the level shift by connecting the LT1074’s “ground” pin to the negative output. Feedback is sensed from circuit ground, and the regulator forces its feedback pin 2.5V above its “ground” pin. Circuit ground is common to input and output, making system use easy. Operating waveforms are essentially identical to Figure 10. Advantages of the previous circuit compared to this one are that the LT1074 package can directly contact a grounded heat sink and that control signals may be directly interfaced to the ground referred pins.

The inductor values in both negative output designs are notably lower than in the positive case. This is necessitated

by the reduced loop phase margin of these circuits. Higher inductance values, while preferable for limiting peak current, will cause loop instability or outright oscillation.

Current-Boosted Step-Down Regulator

Figure 12 shows a way to obtain significantly higher output currents by utilizing efficient energy storage in the LT1074 output inductor. This technique increases the duty cycle over the standard step-down regulator allowing more energy to be stored in the inductor. The increased output current is achieved at the expense of higher output voltage ripple.

The operating waveforms for this circuit are shown in Figure 13. The circuit operating characteristics are similar to that of the step-down regulator (Figure 3). During the V_{SW} (Trace A) “on” time the input voltage is applied to one end of the coupled inductor. Current through the V_{SW} pin (Trace B) ramps up almost instantaneously (since inductor current (Trace F) is present) and then slows as energy is stored in the core. The current proceeds into the inductor (Trace D) and finally is delivered to the load. When the V_{SW} pin goes off, current is no longer available to charge the inductor. The magnetic field collapses, causing the V_{SW} pin voltage to go negative. At this point similarity with the basic regulator vanishes. In this modified version the output current (Trace F) receives a boost as the magnetic field collapses. This results when the energy stored in

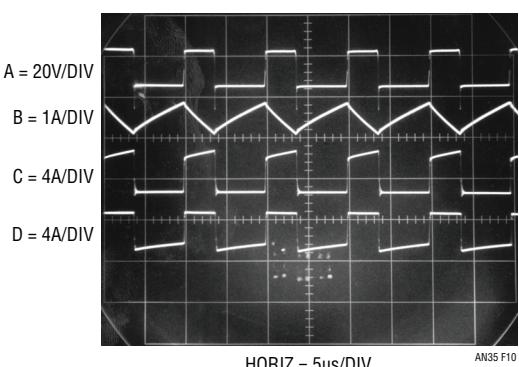


Figure 10. Figure 9's Waveforms

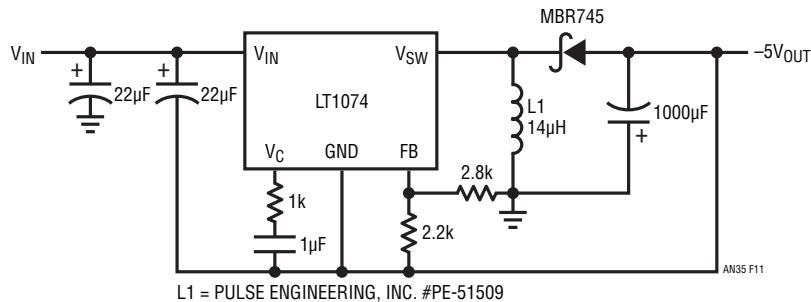


Figure 11. Nelson's Circuit...A (Better) Negative Output Step-Down Regulator

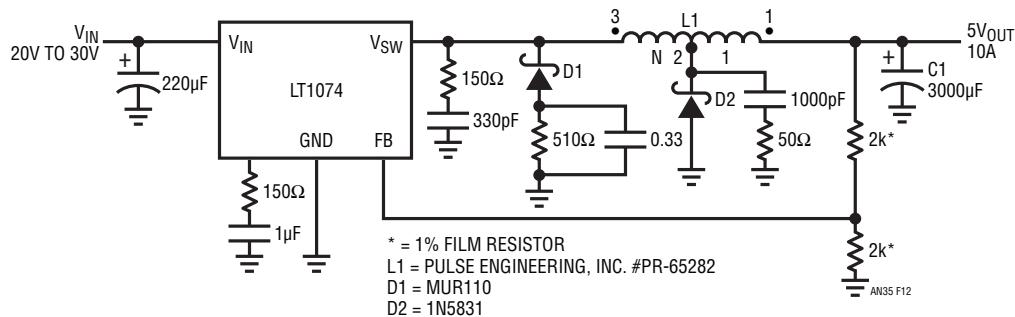


Figure 12. "Current Boosted" Step-Down Regulator. Boost Current is Supplied By Energy Stored in the Tapped Inductor

the core is transferred to the output. This current step circulates through C1 and D2 (Trace E), somewhat increasing output voltage ripple. Not all the energy is transferred to the "1" winding. Current (Trace C) will continue to flow in the "N" winding due to leakage inductance. A snubber network suppresses the effects of this leakage inductance. For lowest snubber losses the specified tapped inductor is bifilar wound for maximum coupling.

Post Regulation-Fixed Case

In most instances the LT1074 output will be applied directly to the load. Those cases requiring faster transient response or reduced noise will benefit from linear post regulation. In Figure 14 a 3-terminal regulator follows the LT1074 output. The LT1074 output is set to provide just enough voltage

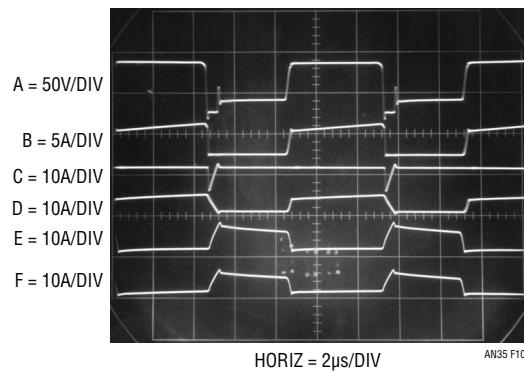


Figure 13. AC Current Flow for the Boosted Regulator

to the LT1084 to maintain regulation. The LT1084's low dropout characteristics combined with a high circuit input voltage minimizes the overall efficiency penalty.

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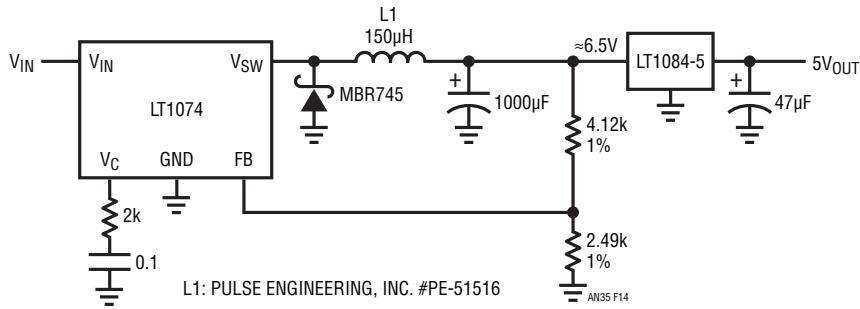


Figure 14. Linear Post-Regulator Improves Noise and Transient Response

Post Regulation-Variable Case

Some situations require variable linear post regulation. Figure 15 does this with little efficiency sacrifice. The LT1085 operates in normal fashion, supplying a variable 1.2V to 28V output. The remainder of the circuit forms a switched mode pre-regulator which maintains a small, fixed voltage across the LT1085 regardless of its output voltage. A1 biases the LT1074 to produce whatever voltage is necessary to maintain the “E diodes” potential across the LT1085. A1’s inputs are balanced when the LT1085 output is “E diodes” above its input. A1 maintains this condition regardless of line, load or output voltage conditions. Thus, good efficiency is maintained over the full range of output voltages. The RC network at A1 compensates the loop. Loop start-up is assured by deliberately introducing a positive offset to A1. This is done by grounding A1’s appropriate balance pin (5), resulting in a positive 6mV offset. This increases amplifier drift, and is normally considered poor practice, but causes no measurable error in this application.

As shown, the circuit cannot produce outputs below the LT1085’s 1.2V reference. Applications requiring output adjustability down to 0V will benefit from option “A” shown on the schematic. This arrangement replaces L1 with L2. L2’s primary performs the same function as L1 and its coupled secondary winding produces a negative bias output ($-V$). The full-wave bridge rectification is necessitated by widely varying duty cycles. A2 and its attendant circuitry replace all components associated with

the LT1085 V_{ADJ} pin. The LT1004 reference terminates the 10k to 250k feedback string at $-1.2V$ with A2 providing buffered drive to the LT1085 V_{ADJ} pin. The negative bias allows regulated LT1085 outputs down to 0V. The $-V$ potential derived from L2’s secondary varies considerably with operating conditions. The high feedback string values and A2’s buffering ensure stable circuit operation for “starved” values of $-V$.

Low Quiescent Current Regulators

Many applications require very wide ranges of power supply output current. Normal conditions require currents in the ampere range, while standby or “sleep” modes draw only microamperes. A typical laptop computer may draw 1 to 2 amperes running while needing only a few hundred microamps for memory when turned off. In theory, any regulator designed for loop stability under no-load conditions will work. In practice, a converter’s relatively large quiescent current may cause unacceptable battery drain during low output current intervals. Figure 16’s simple loop effectively reduces circuit quiescent current from 6mA to only 150 μ A. It does this by utilizing the LT1074’s shutdown pin. When this pin is pulled within 350mV of ground the IC shuts down, pulling only 100 μ A. Comparator C1 combines with the LT1004 reference and Q1 to form a “bang-bang” control loop around the LT1074. The LT1074’s internal feedback amplifier and voltage reference are bypassed by this loop’s operation. When the circuit output (Trace C, Figure 17) falls slightly below 5V C1’s output (Trace A) switches low, turning off Q1 and enabling the

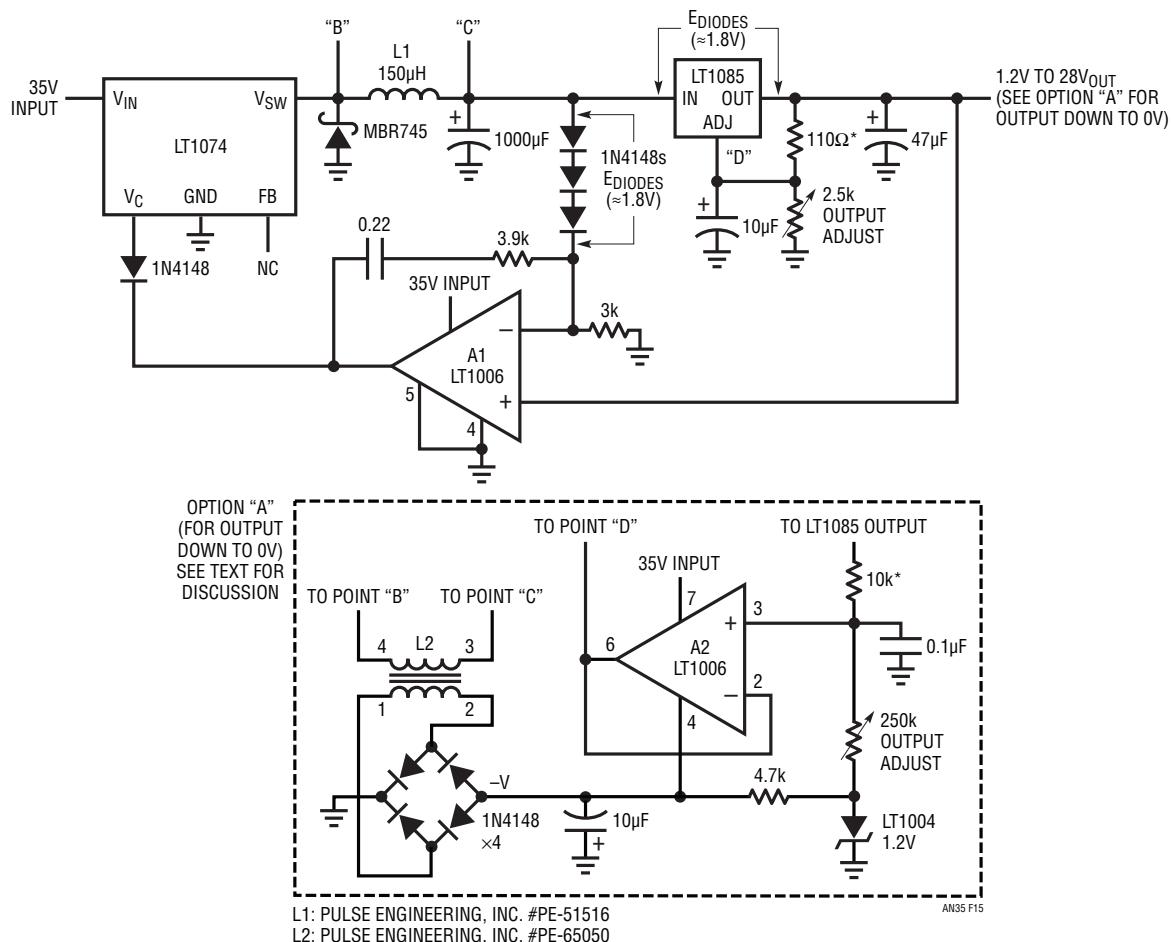


Figure 15. Adjustable Linear Post-Regulator Maintains Efficiency Over Widely Varying Operating Conditions

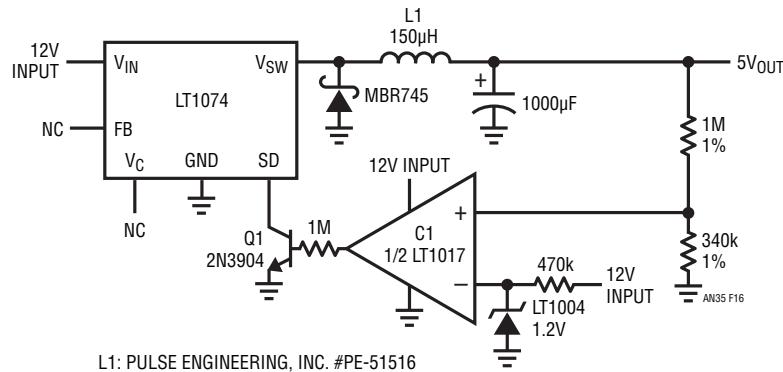


Figure 16. A Simple Loop Reduces Quiescent Current to 150 μ A

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LT1074. The V_{SW} pin (Trace B) pulses at full duty cycle, forcing the output back above 5V. C1 then biases Q1 again, the LT1074 goes into shutdown, and loop action repeats. The frequency of this on-off control action is directly load dependent, with typical repetition rates of 0.2Hz at no load. Short on-times keep duty cycle low, resulting in the small effective quiescent current noted. The on-off operation combines with the LC filtering action in the regulator's V_{SW} line to generate an output hysteresis of about 50mV (again, see Figure 17, Trace C).

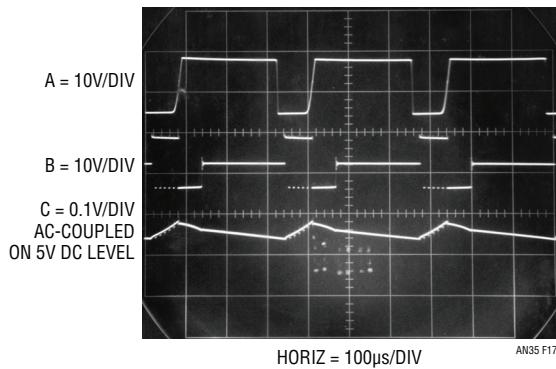


Figure 17. The Low Quiescent Current Loop's Waveforms

The loop performs well, but has two potential drawbacks. At higher output currents the loop oscillates in the 1kHz to 10kHz range, causing audible noise which may be objectionable. This is characteristic of this type of loop, and is the reason that ICs employing gated oscillators invariably produce such noise. Additionally, the control loops operation causes about 50mV of ripple on the output. Ripple frequency ranges from 0.2Hz to 10kHz depending upon input voltage and output current.

Figure 18's more sophisticated circuit eliminates these problems with some increase in complexity. Quiescent current is maintained at 150 μ A. The technique shown is particularly significant, with broad implication in battery powered systems. It is easily applied to a wide variety of regulator requirements, meeting an acknowledged need across a wide spectrum of applications.

Figure 18's signal flow is similar to Figure 16, but additional circuitry appears between the feedback divider and the LT1074. The LT1074's internal feedback amplifier and reference are not used. Figure 19 shows operating

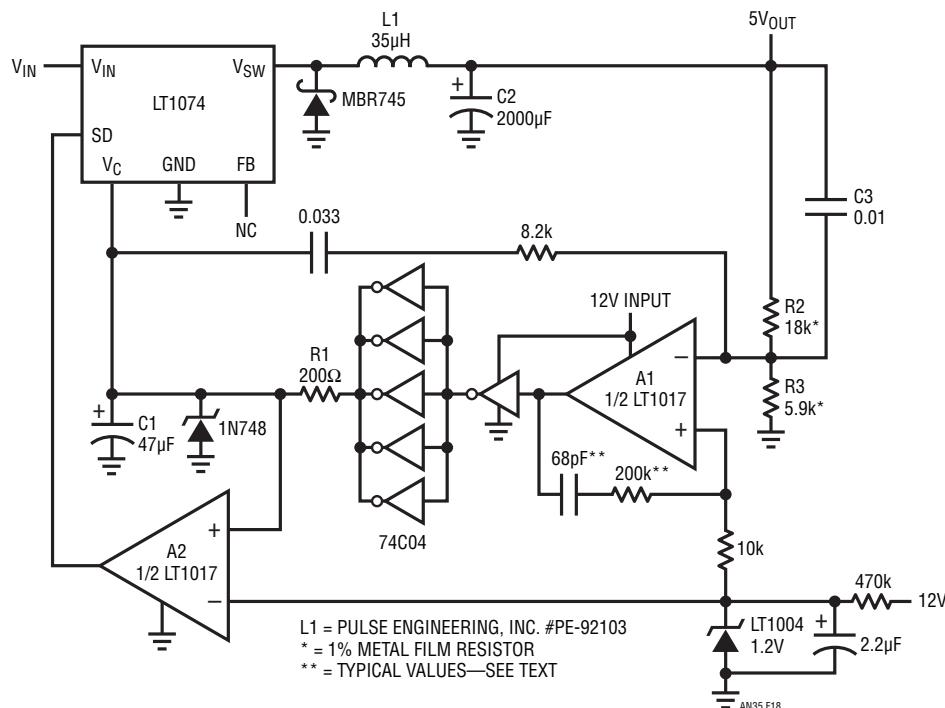


Figure 18. A More Sophisticated Loop Gives Better Regulation While Maintaining 150 μ A Quiescent Current

waveforms under no-load conditions. The output (Trace A) ramps down over a period of seconds. During this time comparator A1's output (Trace B) is low, as are the 74C04 paralleled inverters. This pulls the V_C pin (Trace D) low, forcing the regulator to zero duty cycle. Simultaneously, A2 (Trace C) is low, putting the LT1074 in its 100 μ A shutdown mode. The V_{SW} pin (Trace E) is off, and no inductor current flows. When the output drops about 60mV, A1 triggers and the inverters go high, pulling the V_C pin up and biasing the regulator. The Zener diode prevents V_C pin overdrive. A2 also rises, taking the IC out of shutdown mode. The V_{SW} pin pulses the inductor at the 100kHz clock rate, causing the output to abruptly rise. This action trips A1 low, forcing the V_C pin back low and shutting off V_{SW} pulsing. A2 also goes low, putting the LT1074 into shutdown.

This “bang-bang” control loop keeps the 5V output within the 60mV ramp hysteresis window set by the loop. Note that the loop oscillation period of seconds means the R1-C1

time constant at V_C is not a significant term. Because the LT1074 spends almost all of the time in shutdown, very little quiescent current (150 μ A) is drawn.

Figure 20 shows the same waveforms with the load increased to 2mA. Loop oscillation frequency increases to keep up with the load's sink current demand. Now, the V_C pin waveform (Trace D) begins to take on a filtered appearance. This is due to R1-C1's 10ms time constant. If the load continues to increase, loop oscillation frequency will also increase. The R1-C1 time constant, however, is fixed. Beyond some frequency, R1-C1 must average loop oscillations to DC. At 7mA loading (Figure 21) loop frequency further increases, and the V_C waveform (Trace D) appears heavily filtered.

Figure 22 shows the same circuit points at 2A loading. Note that the V_C pin is at DC, as is the shutdown pin. Repetition rate has increased to the LT1074's 100kHz

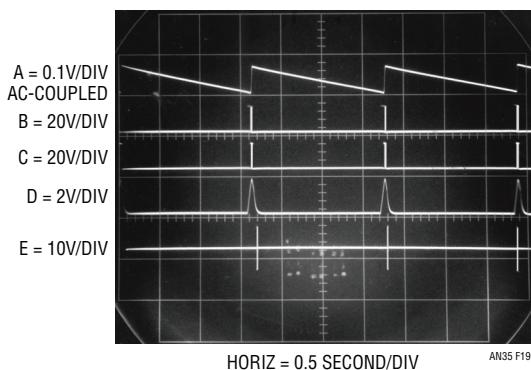


Figure 19. Low Quiescent Current Regulator's Waveforms with No Load (Traces B, C and E Retouched for Clarity)

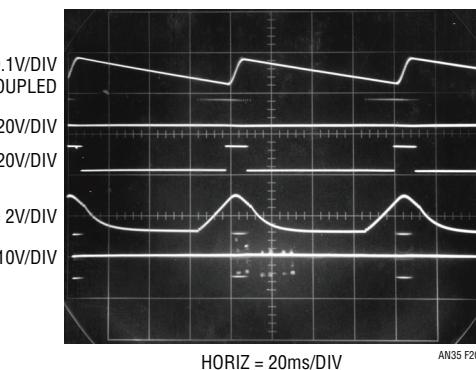


Figure 20. Low Quiescent Current Regulator's Waveforms at 2mA Loading

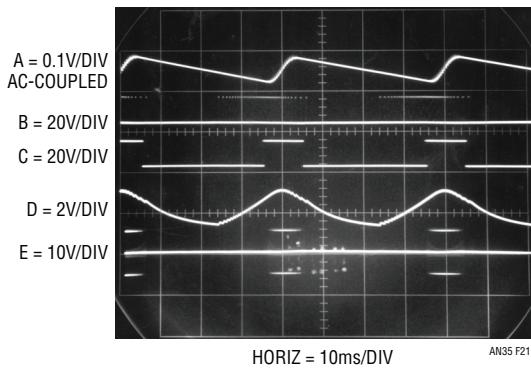


Figure 21. Low Quiescent Current Regulator's Waveforms at 7mA Loading

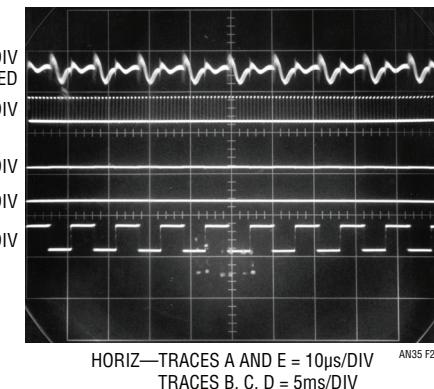


Figure 22. Low Quiescent Current Regulator's Waveforms at 2A Loading

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clock frequency. Figure 23 plots what is occurring, with a pleasant surprise. As output current rises, loop oscillation frequency also rises until about 23Hz. At this point the R1-C1 time constant filters the V_C pin to DC and the LT1074 transitions into “normal” PWM operation. With the V_C pin at DC it is convenient to think of A1 and the inverters as a linear error amplifier with a closed-loop gain set by the R2-R3 feedback divider. In fact, A1 is still duty cycle modulating, but at a rate far above R1-C1’s break frequency. The phase error contributed by C2 (which was selected for low loop frequency at low output currents) is dominated by the R1-C1 roll off and the C3 lead into A1. The loop is stable and responds linearly for all loads beyond 10mA. In this high current region the LT1074 is desirably “fooled” into behaving like a conventional step-down regulator.

A formal stability analysis for this circuit is quite complex, but some simplifications lend insight into loop operation. At 250 μ A loading (20k Ω) C2 and the load form a decay time constant exceeding 30 seconds. This is orders of magnitude larger than R2-C3, R1-C1, or the LT1074’s 100kHz commutation rate. As a result, C2 dominates the loop. Wideband A1 sees phase shifted feedback, and very low frequency oscillations similar to Figure 19’s occur⁵. Although C2’s decay time constant is long, its charge time constant is short because the circuit has low sourcing impedance. This accounts for the ramp nature of the oscillations.

Increased loading reduces the C2-load decay time constant. Figure 23’s plot reflects this. As loading increases,

the loop oscillates at a higher frequency due to C2’s decreased decay time. When the load impedance becomes low enough C2’s decay time constant ceases to dominate the loop. This point is almost entirely determined by R1 and C1. Once R1 and C1 “take over” as the dominant time constant the loop begins to behave like a linear system. In this region (e.g., above about 10mA, per Figure 23) the LT1074 runs continuously at its 100kHz rate. Now, C3 becomes significant, performing as a simple feedback lead⁶ to smooth output response. There is a fundamental trade-off in the selection of the C3 lead value. When the converter is running in its linear region it must dominate the loops time lag generated hysteretic characteristic. As such, it has been chosen for the best compromise between output ripple at high load and loop transient response.

Despite the complex dynamics transient response is quite good. Figure 24 shows performance for a step from no load to 1A. When Trace A goes high a 1A load appears across the output (Trace C). Initially, the output sags almost 200mV due to slow loop response time (the R1-C1 pair delay V_C pin (Trace B) response). When the LT1074 comes on response is reasonably quick and surprisingly well behaved considering circuit dynamics. The multi-time constant recovery⁷ (“rattling” is perhaps more appropriate) is visible in Trace C’s response.

Note 5: Some layouts may require substantial trace area to A1’s inputs. In such cases the optional RC network around A1 ensures clean transitions at A1’s output.

Note 6: “Zero Compensation” for all you technosnobs out there.

Note 7: Once again, “multi-pole settling” for those who adore jargon.

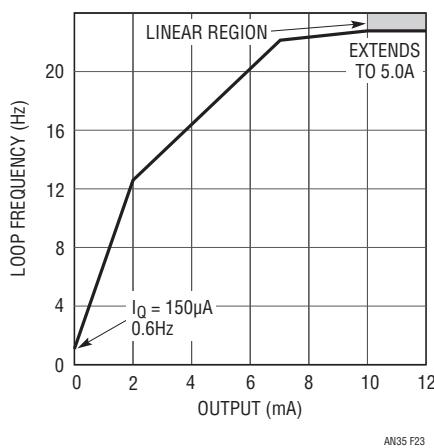


Figure 23. Figure 18’s Loop Frequency vs Output Current.
Note Linear Loop Operation Above 10mA

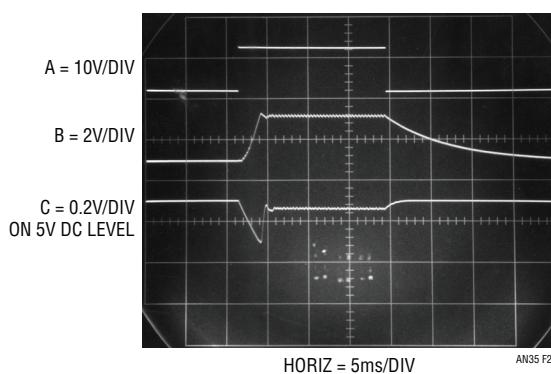
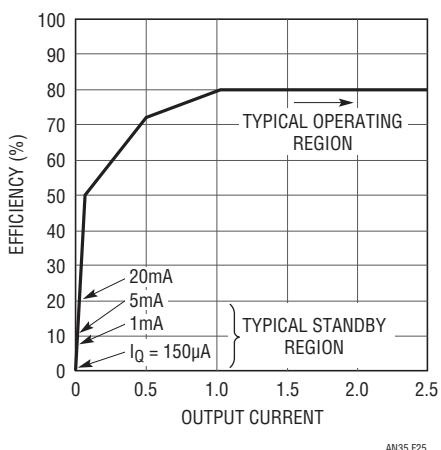


Figure 24. Load Transient Response for Figure 18

Figure 25 plots efficiency versus output current. High power efficiency is similar to standard converters. Low power efficiency is somewhat better, although poor in the lowest ranges. This is not particularly bothersome, as power loss is very small.

The loop provides a controlled, conditional instability instead of the usually more desirable (and often elusive) unconditional stability. This deliberately introduced characteristic dramatically lowers converter quiescent current without sacrificing high power performance.



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Figure 25. Efficiency vs Output Current for Figure 18. Standby Efficiency is Poor, But Power Loss Approaches Battery Self-Discharge

Wide Range, High Power, High Voltage Regulator

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Figure 26 is an example of the LT1074 making a complex function practical. This regulator provides outputs from millivolts to 500V at 100W with 80% efficiency. A1 compares a variable reference voltage with a resistively scaled version of the circuit's output and biases the LT1074 switching regulator configuration. The switcher's DC output drives

a toroidal DC/DC converter comprised of L1, Q1 and Q2. Q1 and Q2 receive out of phase square wave drive from the 74C74 $\div 4$ flip-flop stage and the LT1010 buffers. The flip-flop is clocked from the LT1074 V_{SW} output via the Q3 level shifter. The LT1086 provides 12V power for A1 and the 74C74. A1 biases the LT1074 regulator to produce the DC input at the DC/DC converter required to balance to loop. The converter has a voltage gain of about 20, resulting in high voltage output. This output is resistively divided down, closing the loop at A1's negative input. Frequency compensation for this loop must accommodate the significant phase errors generated by the LT1074 configuration, the DC/DC converter and the output LC filter. The $0.47\mu F$ roll-off term at A1 and the 100Ω - $0.15\mu F$ RC lead network provide the compensation, which is stable for all loads.

Figure 27 gives circuit waveforms at 500V output into a 100W load. Trace A is the LT1074 V_{SW} pin while Trace B is its current. Traces C and D are Q1 and Q2's drain waveforms. The disturbance at the leading edges is due to cross-current conduction, which lasts about 300ns—a small percentage of the cycle. Transistor currents during this interval remain within reasonable values, and no overstress or dissipation problems occur. This effect could be eliminated with non-overlapping drive to Q1 and Q2⁸, although there would be no reliability or significant efficiency gain. The 500kHz ringing on the same waveforms is due to excitation of transformer resonances. These phenomena are not deleterious, although L1's primary RC damper is included to minimize them.

All waveforms are synchronous because the flip-flop drive stage is clocked from the LT1074 V_{SW} output. The LT1074's maximum 95% duty cycle means that the Q1-Q2 switches can never see destructive DC drive. The only condition allowing DC drive occurs when the LT1074 is at zero duty cycle. This case is clearly non-destructive, because L1 receives no power.

Figure 28 shows the same circuit points as Figure 27, but at only 5mV output. Here, the loop restricts drive to the DC/DC converter to small levels. Q1 and Q2 chop just 70mV into L1. At this level L1's output diode drops look large, but loop action forces the desired 0.005V output.

Note 8: For an example of this technique see LTC Application Note 29, Figure 1.

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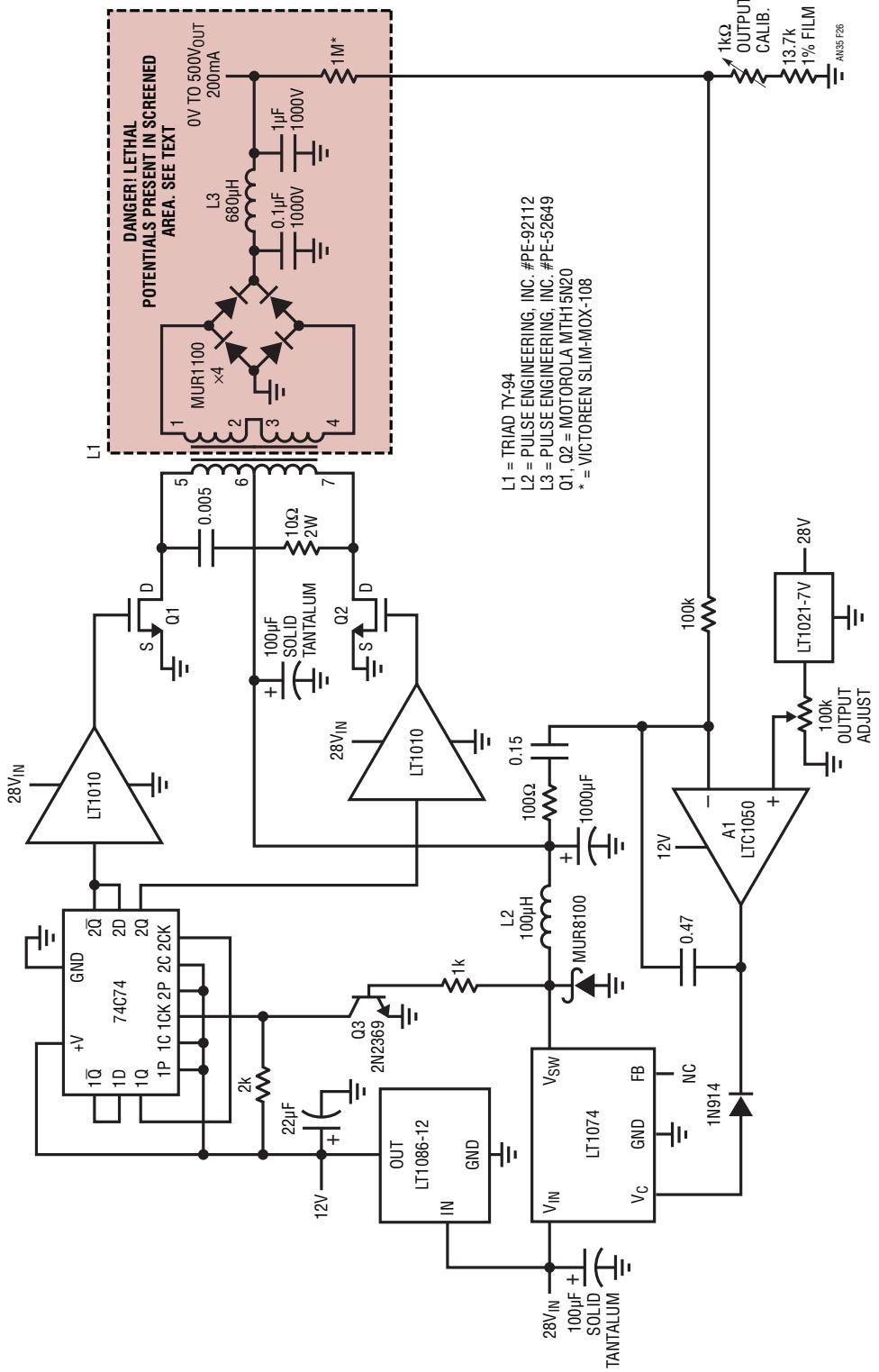


Figure 26. LT1074 Permits High Voltage Output Over 100dB Range with Power and Efficiency.
DANGER! Lethal Potentials Present—See Text

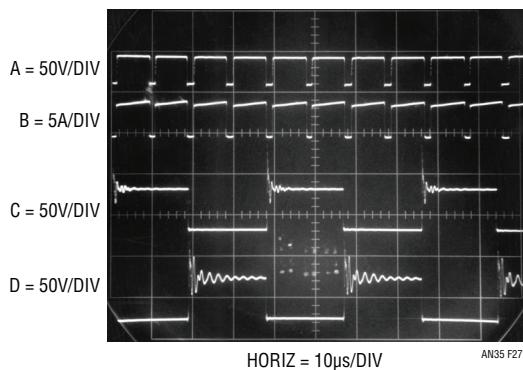


Figure 27. Figure 26's Operating Waveforms at 500V Output into a 100W Load

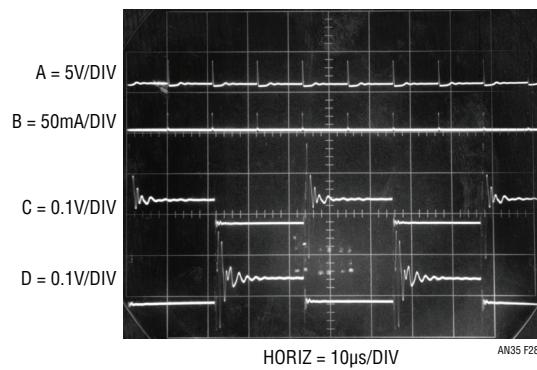


Figure 28. Figure 26's Operating Waveforms at 0.005V Output

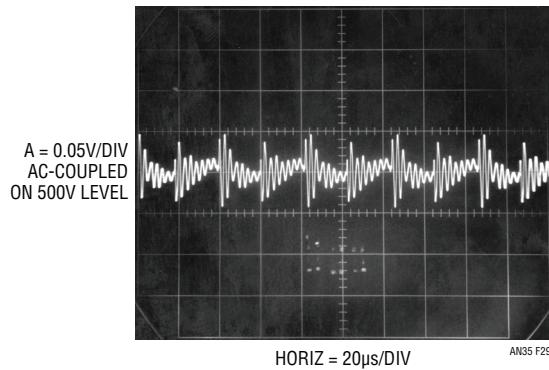


Figure 29. Figure 26's Output Noise at 500V into a 100W Load. Residue is Composed of Q1-Q2 Chopping Artifacts and Transformer Related Ringing. **DANGER!** Lethal Potentials Present—See Text

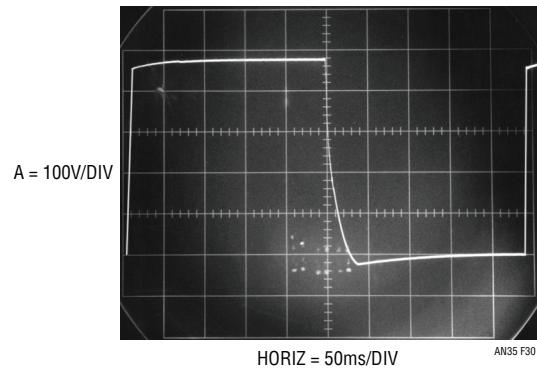


Figure 30. 500V Step Response with 100W Load (Photo Retouched for Clarity). **DANGER!** Lethal Potentials Present—See Text

The LT1074's switched mode drive to L1 maintains high efficiency at high power, despite the circuit's wide output range⁹.

Figure 29 shows output noise at 500V into a 100W load. Q1-Q2 chopping artifacts and transformer related ringing are clearly visible, although limited to about 80mV. The coherent noise characteristic is traceable to the synchronous clocking of Q1 and Q2 by the LT1074.

A 50V to 500V step command into a 100W load produces the response of Figure 30. Loop response on both edges

is clean, with the falling edge slightly underdamped. This slew asymmetry is typical of switching configurations, because the load and output capacitor determine negative slew rate. The wide range of possible loads mandates a compromise when setting frequency compensation. The falling edge could be made critically or even over damped, but response time for other conditions would suffer. The compensation used seems a reasonable compromise.

Note 9: A circuit related to the one presented here appears in the LTC Application Note 18 (Figure 13). Its linear drive to the step-up DC/DC converter forces dissipation, limiting output power to about 15W. Similar restrictions apply to Figure 7 in Application Note 6.

Application Note 35

Regulated Sinewave Output DC/AC Converter

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT, EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS HIGH VOLTAGE POTENTIALS. USE CAUTION.

Figure 31 is another example of the LT1074 permitting the practical implementation of a complex function. It converts a 28V DC input to a regulated 115V_{AC} 400Hz sinewave output with 80% efficiency. Waveform distortion is below 1.6% at 50W output. This design shares similarities with the previous circuit. The LT1074 supplies efficient drive to a high voltage converter despite large line and load variations. An amplifier (A1) controls the input to the high voltage converter via A2 and the LT1074 switching regulator. The high voltage output is divided down and fed back to the amplifier where it is compared to a reference to close a loop. In the previous circuit the output is DC; here the output is AC. As such, A1's reference (Trace A, Figure 32) is an amplitude and frequency stabilized 800Hz half-sine¹⁰. The high voltage converter is driven from a flip-flop clocked by a reference synchronized pulse (negative going excursions just visible in Trace B) via level shift transistor Q3. The reference synchronized pulse occurs at the zero voltage point of the half-sine. The flip-flop outputs (Traces C and D, respectively) drive the Q1 and Q2 gates. RC filters in the gate line retard the drive's slew rate.

A1 biases the LT1074's V_C pin via A2 to produce an 800Hz half-sine signal at L2's center tap (Trace E). Because Q1 and Q2 are synchronously driven with the reference half-sine their drain waveforms (Traces F and G) reveal alternate chopping of complete half cycles. L2 receives balanced drive and its secondary recombines the chopped half-sines into a 115V_{AC} 400Hz sinewave output (Trace H). The diode bridge rectifies L2's output back to an 800Hz half-sine which is fed to A1 via the resistor divider. A1 balances this signal against the reference half-sine to close a loop. Transmitting the 800Hz waveform around the loop requires attention to available bandwidth. The LT1074's 100kHz switching frequency is theoretically high enough to permit this, but the bandwidth attenuation of its output LC filter must be

considered. The unusually low output filter capacitor value allows the necessary frequency response. A1's 330k-0.01μF components combine with the RC lead network across the 16k feedback resistor to stabilize the loop.

A2 closes a local loop around the LT1074 configuration. This is necessary because L2 blocks DC information from being conducted around A1's loop. This is a concern because the waveform presented to L2's primary center tap must have no DC component. DC content at this point will cause waveform distortion, transformer power dissipation or both. The LT1074's V_C pin operates with substantial and uncertain DC bias, making A1's inability to control DC errors unacceptable. A2 corrects this by biasing the LT1074 V_C pin at its DC threshold so that no DC component is presented to L2. A1's output represents the difference between the AC-coupled circuit output and the half-sine reference. A2's output contains this information in addition to DC restoration information. L2 and A1 contribute essentially no DC error, so A2's loop may be closed at the LT1074 configuration's output. A2's feedback capacitor stabilizes this local loop.

The drive to L2 cannot sink current. This means that any residual energy stored in L2 when the drive waveform goes to zero sees no exit path. This is a relatively small effect, but can cause output crossover distortion. The synchronous switch option shown on the schematic provides such a path, and is recommended for lowest output distortion. This optional circuitry is detailed in Appendix E.

Figures 33a and 33b show waveforms in the "turnaround" region of circuit operation. This is the most critical part of the converter, and its characteristics directly determine output waveform purity. Figure 33a (Trace A), a highly amplitude and time expanded version of L2's center tap drive, arrives at OV (upper cross-etched horizontal line) and turns around cleanly. This action is just slightly time skewed from the reference synchronized pulse (Trace B). The aberration on the rising edge is due to the optional synchronous switch's operation. This switch is shorted during the on-time of Trace C's pulse (see Appendix E for operating details of this option). Trace D, Q2's gate drive, aligns with Trace B's pulse. The slew reduction caused by

Note 10: Complete operating details of the half-sine reference generator appear in Appendix E.

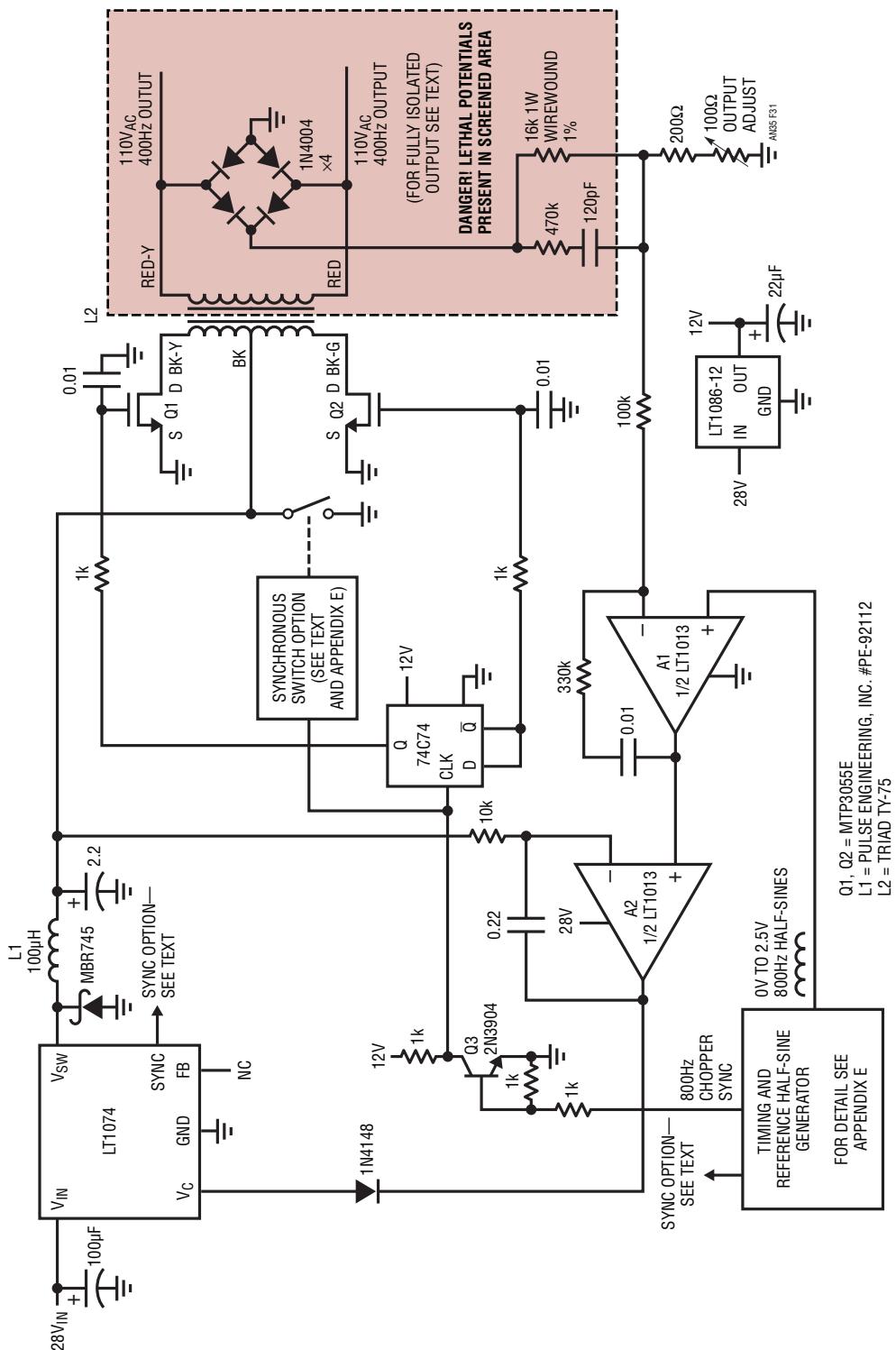


Figure 31. LIT074 Based +28 to 110VAC 400Hz Converter. Sinewave Output Shows Only 1.6% Distortion. **DANGER!** Lethal Potentials Present—See Text

Application Note 35

the 1k-0.01 μ F filter is clearly visible, and contributes to Trace A's low noise turnaround. The LT1074's 100kHz chopping related components are easily observed in Trace A. Waveforms at the next half cycle's zero point (e.g., Q1's gate driven) are identical.

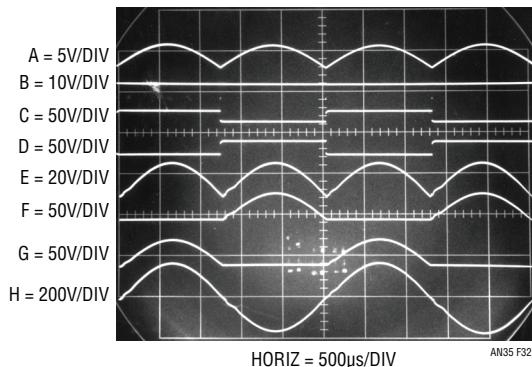


Figure 32. +28 to 110V_{AC}, 400Hz Converter's Waveforms. The Optional Synchronous Switch is Disabled in this Photo, Resulting in Relatively High Crossover Distortion (Trace H). **DANGER! Lethal Potentials Present—See Text**

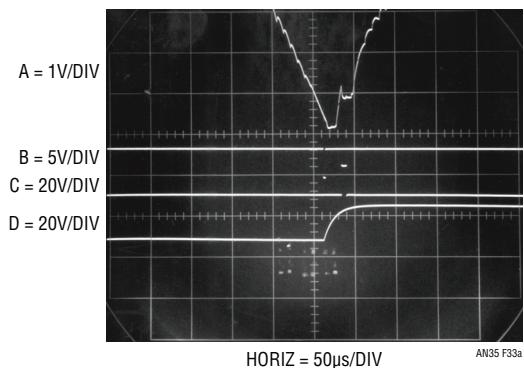


Figure 33a

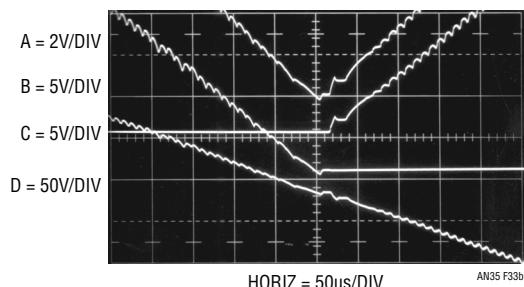


Figure 33b

Figure 33a and 33b. Details of “Turnaround” Sequence. Switching Characteristics Directly Determine Output Crossover Distortion. **DANGER! Lethal Potentials Present—See Text**

Figure 33b shows additional details at highly expanded amplitude and time scales. L2's center tap is Trace A, Q1's drain is Trace B and Q2's drain Trace C. The output sinewave (Trace D) is shown as it crosses through zero.

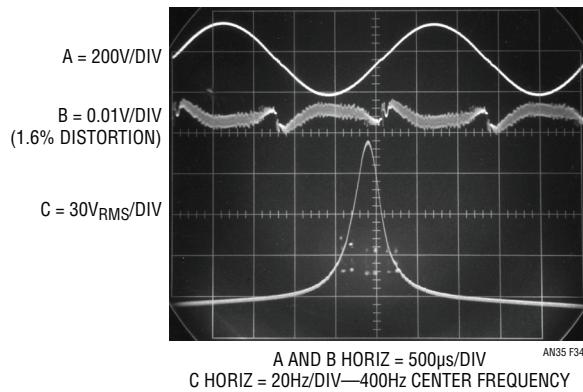


Figure 34. Distortion and Spectral Characteristics for the Sinewave Output Converter. Distortion Trace (B) Shows Crossover Aberrations and the LT1074 Wideband Chopping Residue. The Synchronous Switch Option is Employed in this Photo for Lowest Distortion. **DANGER! Lethal Potentials Present—See Text**

Figure 34 studies waveform purity. Trace A is the sinewave output at 50W loading. Trace B shows distortion products, which are dominated by turnaround related crossover aberrations and LT1074 100kHz chopping residue. Although not strictly necessary, the LT1074's switching can be synchronized to the reference half-sine for coherent noise characteristics. This option is discussed in Appendix E, along with other reference generator details. Trace C is a spectrum analysis centered at 400Hz¹¹. In this photo the optional synchronous switch is used, accounting for improved crossover characteristics over Figure 32.

If a fully floating output is desired the output diode bridge can be isolated by a simple 1:1 ratio transformer. To calibrate this circuit trim the “output adjust” potentiometer for a 115V_{AC} output. Regulation remains within 1% over wide variations of input and load.

¹¹Test equipment aficionados may wish to consider how this picture was taken. Hint: Double exposure techniques were not used. This photograph is a real time, simultaneous display of frequency and time domain information.

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2. Williams, J and Huffman, B., "Some Thoughts on DC/DC Converters," Linear Technology Corporation, Application Note 29.
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Note: *This application note was derived from a manuscript originally prepared for publication in EDN magazine.*

APPENDIX A

Physiology of the LT1074

The LT1074 uses standard (as opposed to current mode) pulse width modulation, with two important differences. First, it is a clocked system with a maximum duty cycle of approximately 95%. This allows a controlled start-up when it is used as a positive-to-negative converter or a negative boost converter. Second, duty cycle is an inverse function of input voltage ($DC \approx 1/V_{IN}$), without any change in error amplifier output. This greatly improves line transient response and ripple rejection, especially for designs which have the control loop over-damped.

Referring to the block diagram, the heart of the LT1074 consists of the oscillator, the error amplifier A1, an analog multiplier, comparator C6, and an RS flip-flop. A complete switching cycle begins with the reset (down ramp) period of the oscillator. During this time ($\approx 0.7\mu s$), the RS flip-flop is set and the switch driver Q104 is kept off via the "and" gate G1. At the end of the reset time, Q104 turns on and drives the output switch Q111, Q112 and Q113. The oscillator ramp starts upward, and when it is equal to the output voltage of the analog multiplier, C6 resets the RS flip-flop, turning off the output switch. Duty cycle is therefore controlled by the output of the multiplier which in turn is controlled by the output of the error amplifier, A1.

A multiplier is used in the LT1074 to provide a perfect "feedforward" function. Conventional switching regulators sometimes use a simple form of feedforward to adjust duty cycle immediately when input voltage changes. This reduces the requirement for voltage swing at the output of the error amplifier as it tries to correct for line variations. Bandwidth of switching regulator error amplifiers must be fairly low to maintain loop stability, so rather large output perturbations occur when the output of the error amplifier must move quickly to correct for line variations. Conventional feedforward schemes typically operate well over a restricted input voltage range or are effective only at certain frequencies. The multiplier technique is very effective over the full range of input voltage and at all frequencies. The basic function is to compensate for the generalized buck regulator transfer function; $V_{OUT} = (V_{IN})^{(DC)}$, where DC = switch duty cycle. This transfer function has two implications. First, it is obvious that to maintain a constant output, duty cycle must change inversely with input voltage. Second, input voltage appears in the loop transfer function, i.e., a fixed variation in duty cycle gives different variations in output voltage depending on input voltage. Loop gain is directly proportional to input voltage,

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and this can cause loop instability or slow loop response if input voltage varies over a wide range. The multiplier takes out all input voltage effects by automatically adjusting loop gain inversely with input voltage. The multiplier output (V_O) is equal to error amplifier output (V_E) divided by input voltage (V_{IN}); $V_O = (V_R) \cdot (V_E)/(V_{IN})$. V_R is a fixed voltage required by all analog multipliers to define multiplier gain. It has an effective value of approximately 20V in the LT1074.

The error amplifier used in the LT1074 is a transconductance type. It has high output impedance ($\approx 500\text{k}\Omega$), so that its AC voltage gain is defined by the impedance of external shunt frequency compensation components (Z_C) and the transconductance (g_m) of the amplifier, $A_V = (g_m)(A_C)$. g_m is $\approx 3500\mu\text{mho}$. The error amplifier has its noninverting input committed to an internal 2.3V reference. The inverting input (fb) is brought out for connection to an external voltage divider that establishes regulator output voltage.

Two other connections are made internally to the fb pin. A window comparator consisting of C4, C5, and some logic provides an “output status” function. It monitors the voltage on the fb pin and gives a “high” output only when the fb voltage is within $\pm 5\%$ of the internal reference voltage. This status output can be used to alert external circuitry that the regulator output is “in” or “out” of regulation. The delay and one-shot circuits ensure that switching EMI will not cause spurious outputs, and that the minimum time for an “out-of-bounds” (low) status output is $\geq 20\mu\text{s}$. Also tied to the fb pin is a frequency shift circuit consisting of R15 and Q36. The base of Q36 is biased at $\approx 1\text{V}$ so that Q36 turns on when the fb pin drops below $\approx 0.6\text{V}$. Current through Q36 smoothly decreases oscillator frequency. This is necessary for maintaining control of current limit at high input voltages. A “dead short” on the output of a switching regulator requires that switch “on” time reduce to $(V_D)/(V_{IN})(f)$, where V_D is the forward voltage of the output catch diode and f is switching frequency. V_D is typically 0.5V for a Schottky catch diode, forcing switch “on” time to shrink to a theoretical $0.1\mu\text{s}$ for a 50V input and 100kHz switching frequency with a shorted output. In practical circuits, effective “on” time can stretch to $0.3\mu\text{s}$ under these conditions due to losses in the inductor wire resistance and switch rise and fall time. The LT1074

cannot reduce switch “on” time to less than $\geq 0.6\mu\text{s}$ in current limit because it has true pulse-by-pulse switch current limiting. The current limit circuitry must sense switch current *after* the switch turns on, and then send a signal to turn the switch off. Minimum time for this signal path is $0.6\mu\text{s}$. Full control of current limit is maintained by reducing switching frequency when the output falls to less than approximately 15% of its regulated value. This has no affect on normal operation and does not change the selection of external components such as the inductor or output capacitor.

True pulse-by-pulse current limiting is performed by comparator C7. It monitors the voltage across sense resistor R52 and resets the RS flip-flop. Current limit threshold is set by the voltage across R47 which in turn is set by the voltage on the I_{LIM} pin. The I_{LIM} voltage is determined by an external resistor or by an internal clamp of 5V if no external resistor is used. To compensate for the temperature coefficient of R47 ($\approx +0.25\%/\text{^\circ C}$), the internal current source I_L has a matching positive temperature coefficient. Its nominal value is $300\mu\text{A}$ at 25°C . Current limit can be set from 1A to 6A with one external resistor between I_{LIM} and ground. If no resistor is used, the I_{LIM} pin will self clamp at $\leq 5\text{V}$ and current limit will be $\approx 6.5\text{A}$. A small pre-bias is added to the negative input of C7 to ensure that current limit will go to zero (no switching) when the I_{LIM} pin is pulled to 0V, either by an external short or via Q11 during undervoltage lockout. Soft-start can be achieved by connecting a capacitor to the I_{LIM} pin. Foldback current limiting can also be implemented by connecting a resistor from I_{LIM} to the regulated output.

Switching frequency of the LT1074 is internally set at 100kHz, but can be increased by connecting a resistor from the frequency pin to ground. This resistor biases on Q79 and feeds extra current into the oscillator. Maximum suggested frequency is 200kHz. A comparator, C3, is also connected to the frequency pin and allows this pin to be used for synchronizing the oscillator to an external clock, even when the pin is also being used to boost oscillator frequency. R35 keeps the frequency pin biased correctly in a no-function state when it is left open and R36 limits Q79 current if the frequency pin is accidentally shorted to ground.

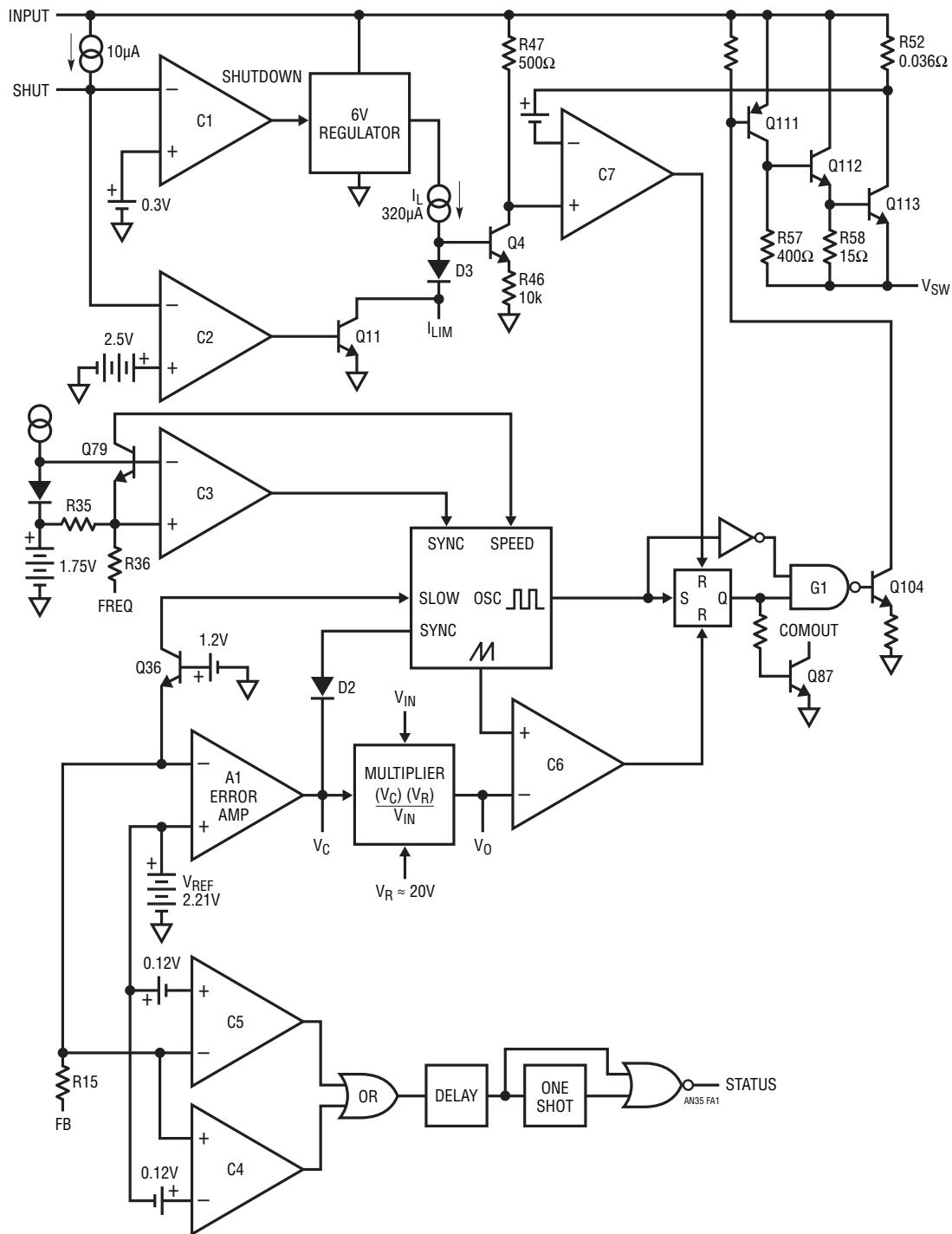


Figure A1. Simplified LT1074 Internal Details

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The shutdown pin on the LT1074 can be used as a logic control of output switching, as an undervoltage lockout, or to put the regulator into complete shutdown with $I_{SUPPLY} \approx 100\mu A$. Comparator C2 has a threshold of 2.5V. It forces the output switch to a 100% "off" condition by pulling the I_{LIM} pin low via Q11. Undervoltage lockout is implemented through C2 by connecting the tap of an input voltage divider to the shutdown pin. Full micropower shutdown of the regulator is achieved by pulling the shutdown pin below the 0.30V threshold of C1. This turns off the chip by shutting down the internal 6V bias supply. An internal 10 μA current source pulls the shutdown pin high (inactive) if it is left open.

The Comout pin is an open-collector NPN whose collector voltage is the complement of the switch output (V_{SW}). Q87 is specified to drive up to 10mA and 30V. It is intended to drive the gate of an external N-channel MOS switch which is in parallel with the catch diode. The MOS switch then acts as a synchronous rectifier, which can significantly improve converter efficiency in low output voltage applications. The Comout pin can also be used to drive the gate of an external P-channel MOS switch in parallel with

the internal bipolar switch to provide ultrahigh efficiency switching at lower input voltages. A slight time-shift in the Comout signal prevents switch overlap problems.

The combination of these features produces a DC/DC converter with the electrical characteristics shown in Figure A2.

PARAMETER	CONDITIONS	UNITS
Input Voltage Range		4.5V to 60V
Output Voltage Range		2.5V to 50V
Output Current Range	Standard Buck Tapped Buck	0A to 5A 0A to 10A
Quiescent Input Current		7mA
Switching Frequency		100kHz to 200kHz
Switch Rise/Fall Times		50ns
Switch Voltage Loss	1A 5A	1.6V 2V
Reference Voltage		2.35V $\pm 1.5\%$
Line/Load Regulation		0.05%
Efficiency	$V_{OUT} = 15V$ $V_{OUT} = 5V$	90% 80%

Figure A2. LT1074 Electrical Characteristics

APPENDIX B

GENERAL CONSIDERATIONS FOR SWITCHING REGULATOR DESIGN

Inductor Selection

Magnetic considerations are easily the most common problem area in switching regulator design. Ninety percent of the difficulties encountered are traceable to the inductive components in the circuit. The overwhelming level of difficulty associated with magnetics mandates a judicious selection process. The most common difficulty is saturation. An inductor is saturated when it cannot hold any more magnetic flux. As an inductor arrives at saturation it begins to look more resistive and less inductive. Under these conditions current flow is limited only by the inductor's DC copper resistance and the source capacity. This is why saturation often results in destructive failures.

While saturation is a prime concern, cost, heating, size, availability and desired performance are also significant. Electromagnetic theory, although applicable to these issues, can be confusing, particularly to the non-specialist.

Practically speaking, an empirical approach is often a good way to address inductor selection. It permits real-time analysis under actual circuit operating conditions using the ultimate simulator—a breadboard. If desired, inductor design theory can be used to augment or confirm experimental results.

Figure B1 shows a typical step-down converter utilizing the LT1074 switching regulator. A simple approach may be employed to determine the appropriate inductor. A very useful tool is the #845 inductor kit¹² shown in Figure B2. This kit provides a broad range of inductors for evaluation in test circuits such as Figure B1.

Note 12: Available from Pulse Engineering, Inc., P.O. Box 12235, San Diego, California 92112, 619-268-2400.

Figure B3 was taken with a $450\mu\text{H}$ value, high core capacity inductor installed. Circuit operating conditions such as input voltage and loading are set at levels appropriate to the intended application. Trace A is the LT1074's V_{SW} pin voltage while Trace B shows its current. When V_{SW} pin voltage is high, inductor current flows. The high inductance means current rises relatively slowly, resulting in the shallow slope observed. Behavior is linear, indicating no saturation problems. In Figure B4, a lower value unit with equivalent core characteristics is tried. Current rise is steeper, but saturation is not encountered. Figure B5's selected inductance is still lower, although core characteristics are similar. Here, the current ramp is quite pronounced, but well controlled. Figure B6 brings some informative surprises. This high value unit, wound on a low capacity core, starts out well but heads rapidly into saturation, and is clearly unsuitable.

The described procedure narrows the inductor choice within a range of devices. Several were seen to produce

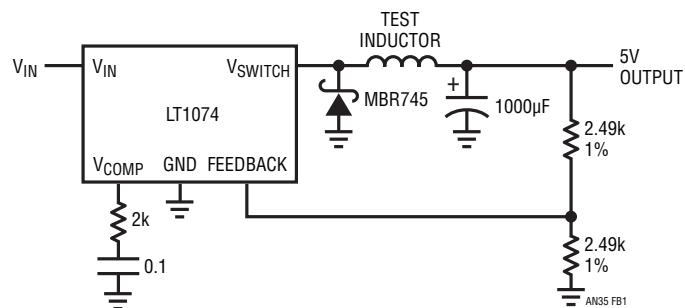


Figure B1. Basic LT1074 Test Circuit

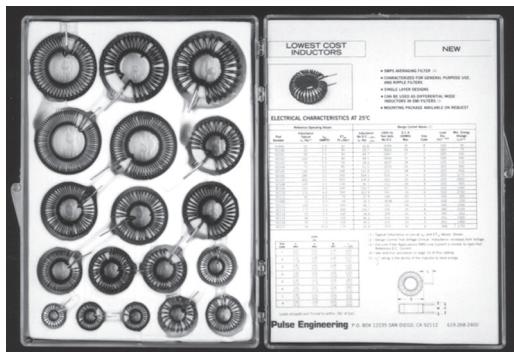


Figure B2. Model 845 Inductor Selection Kit from Pulse Engineering, Inc. Includes 18 Fully Specified Devices

acceptable electrical results, and the "best" unit can be further selected on the basis of cost, size, heating and other parameters. A standard device in the kit may suffice, or a derived version can be supplied by the manufacturer.

Using the standard products in the kit minimizes specification uncertainties, accelerating the dialogue between user and inductor vendor.

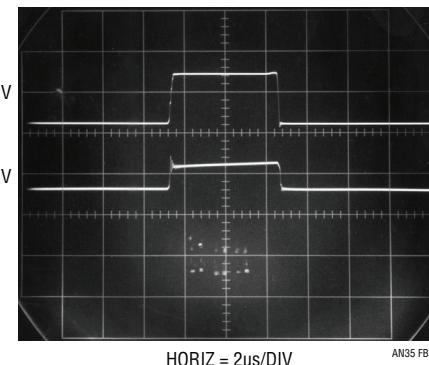


Figure B3. Waveforms for $450\mu\text{H}$, High Capacity Core Unit

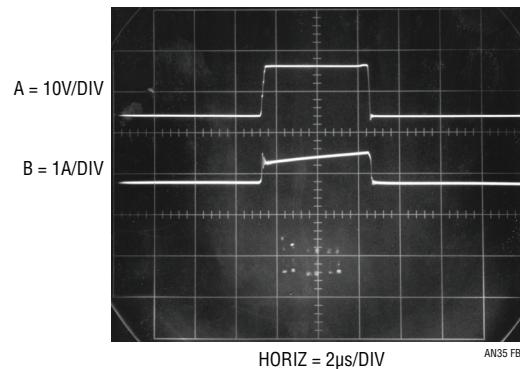


Figure B4. Waveforms for $170\mu\text{H}$, High Capacity Core Unit

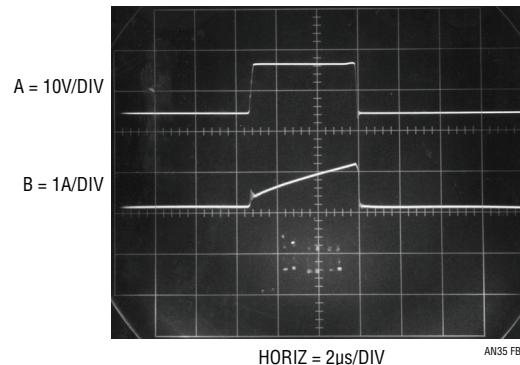


Figure B5. Waveforms for $55\mu\text{H}$, High Capacity Core Unit

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Inductor Selection—Alternate Method

There are alternate inductor selection methods to the one described. One of the most popular is utilized by those devoid of the recommended inductor kit, time or adequate instrumentation. What is usually desired is to get a prototype LT1074 circuit running *NOW*. What is often available is limited to a drawer of inductors (see Figure B7) of unknown or questionable lineage. Selection of an appropriate inductor is (hopefully) made by simply inserting one of these drawer dwellers into an unsuspecting LT1074 circuit. Although this method's theoretical premise is perhaps questionable, its seemingly limitless popularity compels us to address it. We have developed a 2-step procedure for screening inductors of unknown characteristics. Inductors passing both stages of the test have an excellent chance (75%—based on our sample of

randomly selected inductors) of performing adequately in a prototype LT1074 circuit. The only instrumentation required is an ohmmeter and a scale.

Test 1 consists of weighing the candidate inductor. Acceptable limits range between 0.01 and 0.25 pounds. This test is best performed at an Inductor Test Facility (see Figure B8), where precision scales are readily available. To save time the quick checkout line is recommended (but only if you have nine¹³ inductors or less—no cheating).

Figure B9 shows an inductor under test. The 0.13 pound weight indicated by the scale places this unit well within acceptable limits.

Note 13: The maximum permitted number of items in the quick checkout line varies from facility to facility. Please be familiar with and respect local regulations.

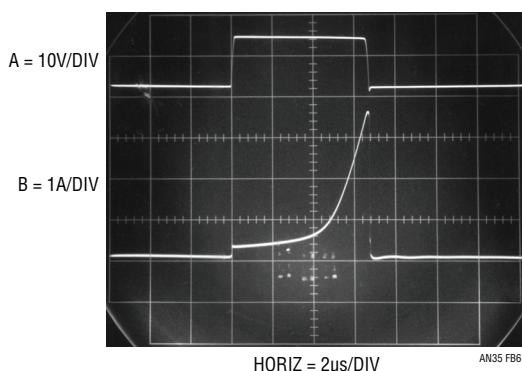


Figure B6. Waveforms for 500 μ H, Low Capacity Core Inductor (Note Saturation Effects)



Figure B8. Typical Inductor Test Facility



Figure B7. "Yeah, We Got Some Inductors in a Drawer. I'm Sure They'll Work..."



Figure B9. Inductor Under Test (Don't Forget to Pick Up a Loaf of Bread and a Dozen Eggs)

The second test involves measuring the inductors DC resistance. Acceptable limits are usually between 0.01Ω and 0.25Ω . Inductors passing both tests will probably function in a prototype LT1074 circuit. Figures B10 and B11 show typical acceptable and unacceptable inductors. Graduates tend to be relatively dense, with (where visible) thick wire. Flunkers are usually less dense, with small (again, where visible) wire sizes.

When using an inductor selected with this method try low power first, then gradually increase loading. Observe inductor and LT1074 heating, making sure their dissipation is reasonable (warm to the touch). Disproportionate increases in heating as load is increased probably indicate inductor saturation. Either reduce the load, or go back to the drawer and try again.

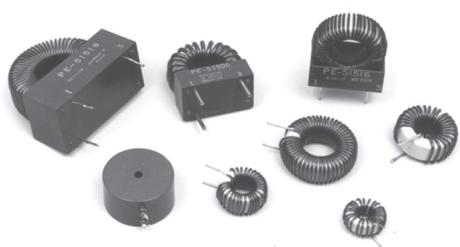


Figure B10. Typical Acceptable Inductors

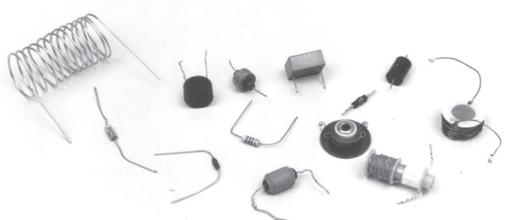


Figure B11. Typical Unacceptable Inductors

While these two tests are somewhat lacking in rigor they do increase the chances of quickly getting a circuit to run with available components. In the longer term, the appropriate inductor can be decided upon and specified.

For the theoretically minded, test 1 grades out inductors which are unlikely to have enough flux storage capability (core mass) to avoid saturation. Test 2 eliminates units with too high a resistance to efficiently support typical LT1074 operating currents. Expanded discussion and design considerations for inductors will be found in Reference 4.

Capacitors

Think about requirements in capacitors. All operating conditions should be accounted for. Voltage rating is the most obvious consideration, but remember to plan for the effects of equivalent series resistance (ESR) and inductance. These specifications can have significant impact on circuit performance. In particular, an output capacitor with high ESR can make loop compensation difficult or decrease efficiency.

Layout

Layout is vital. Don't mix signal, frequency compensation, and feedback returns with high current returns. Arrange the grounding scheme for the best compromise between AC and DC performance. In many cases, a ground plane may help. Account for possible effects of stray inductor-generated flux on other components and plan layout accordingly.

Diodes

Diode breakdown and switching ratings must be thought through. Account for all conditions. Transient events usually cause the most trouble, introducing stresses that are often hard to predict. Study the data sheet breakdown, current capacity, and switching speed ratings carefully. Were these specifications written under the same conditions that your circuit is using the device in? If in doubt, consult the manufacturer.

Switching diodes have two important transient characteristics—reverse recovery time and forward turn-on time.

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Reverse recovery time occurs because the diode stores charge during its forward conducting cycle. This stored charge causes the diode to act as a low impedance conductive element for a short period of time after reverse drive is applied. Reverse recovery time is measured by forward biasing the diode with a specified current, then forcing a second specified current backwards through the diode. The time required for the diode to change from a reverse conducting state to its normal reverse non-conducting state is reverse recovery time. Hard turn-off diodes switch abruptly from one state to the other following reverse recovery time. They therefore dissipate very little power even with moderate reverse recovery times. Soft turn-off diodes have a gradual turn-off characteristic that can cause considerable diode dissipation during the turn-off interval.

Fast diodes can be useless if stray inductance is high in the diode, output capacitor or LT1074 loop. 20-gauge hook-up wire has 30nH/inch inductance. Switching currents on the order of 10^8 A/sec are typical in regulator circuits. They can easily generate volts per inch in wiring. Keep the diode, capacitor and LT1074 input/switch lead lengths *SHORT!*

Frequency Compensation

The basic LT1074 step-down configuration is relatively free of frequency compensation difficulties. The simple RC damper networks shown from the V_C pin to ground will usually suffice. Things become more complex when gain and phase contributing elements are added to the basic loop. In these cases it is often useful to look at the LT1074 as a low bandwidth power stage. The delays are due to the sampled data nature of power delivery (100kHz switching frequency) and the output LC filter. In general, complex loops can be stabilized by limiting the gain bandwidth of the LT1074 below that of the added elements. This is in accordance with well known feedback theory. A discussion of practical techniques for stabilizing such loops, "The Oscillation Problem (Frequency Compensation Without Tears)," appears at the end of LTC Application Note 18. Other pertinent comments appear in the "Frequency Compensation" sections of LTC Application Notes 19 and 25.

APPENDIX C

Techniques and Equipment for Current Measurement

Accurate measurement of current flow under rapidly changing circuit conditions is essential to switching regulator design. In many cases current waveforms contain more valuable information than voltage measurements. The most powerful and convenient current measuring tool is the clip-on current probe. Several types appear in Figure C1. The Tektronix P-6042, shown bottom left, is a Hall effect stabilized current transformer which responds from DC to 50MHz. The more recent Tektronix AM-503 (not shown) has similar specifications. The combination of convenience, broad bandwidth and DC response make Hall effect stabilized current probes the instrument of choice for converter design. The DC response allows determination of DC content in high speed current waveforms. The clip-on probe contains a current transformer and a Hall effect device. The Hall device senses at DC and low frequency while the transformer simultaneously processes high frequency content. Careful roll-off matching allows

a composite output with no peaking or response aberrations at the two sensors bandwidth crossover. Sensitivity ranges from fractions of a millampere to amperes and is switch selectable.

Transformer based clip-on current probes are also available. These types lack the DC response of their Hall effect augmented cousins, but are still quite useful. The Tektronix type 131 (and the more modern 134) responds from hundreds of hertz to about 40MHz. AC current probes (type 131 appears in C1, upper left) are as convenient to use as Hall types, but cannot respond at low frequency. AC current probes are also available with a simple termination (left foreground, Figure C1). These types are more difficult to use than the actively terminated models (e.g., type 131 shown) because of complex gain switching. Their low frequency limitations are also poorer, although their high frequency response exceeds 100MHz.

A final form of AC current probe is the simple transformer shown in Figure C1's foreground. These are not clip-on devices, and usually have significant performance limitations compared to the instruments discussed. However, they are inexpensive and can provide meaningful measurement results when used according to manufacturers' recommendations. In use, the conductor is threaded through the opening provided and the signal monitored at the output pins.

Figure C1 also shows a wide ranging DC clip-on current probe. The Hewlett-Packard 428B (upper right) responds from DC to only 400Hz, but features 3% accuracy over a 100 μ A to 10A range. This instrument obviously cannot discern high speed events, but is invaluable for determining overall efficiency and quiescent current.



Figure C1. Various Current Probe Types Provide Different Capabilities. Selection Criteria is Application Dependent

A great strength of the probes described is that they take a fully floating measurement. The extraction of current information by magnetic connection eliminates common mode voltage considerations. Additionally, the clip-on convenience makes the probes as easy to use as a standard voltage mode probe. As good as they are, current probes have limitations and characteristics which must be remembered to avoid unpleasant surprises. At high currents, probe saturation limits may be encountered. Resultant CRT waveforms will be corrupted, rendering the measurement useless and confusing the unwary. For Hall types, measurement below a few hundred microamperes is limited by noise, which is much more obvious on the display. Keep in mind that current probes have different signal transit delay times than voltage probes or dissimilar current probes. At high sweep speeds this effect shows up

in multi-trace displays as time skewing between individual channels. The current probes transit time delay can be mentally factored in to reduce error when interpreting the display. Note that active probes have the longest signal transit times, on the order of 25ns.

The AC probes low frequency bandwidth restriction must be kept in mind when interpreting CRT displays. Figure C2 clearly demonstrates this by showing the AC probes inability to follow low frequency. Similarly, remember that the probe's stated bandpass is a -3dB figure, meaning signal information is not entirely present in the display at this frequency. When working in regions approaching either end of the probe bandpass consider that displayed information may be distorted or incomplete.

There are other ways, albeit less convenient and desirable than clip-on current probes, to measure wideband current signals. Ohm explains that measuring voltage across a resistor gives current. Current shunts (Figure C3 foreground) are low value (for LT1074 circuits 0.1 Ω to

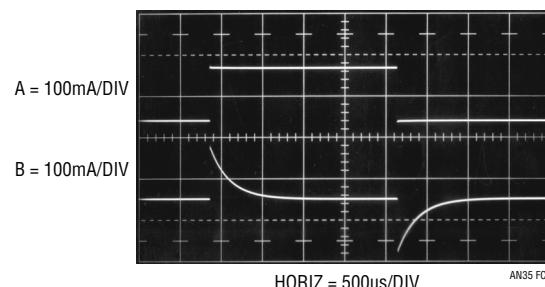


Figure C2. Hall Stabilized (Trace A) and Transformer (Trace B) Based Current Probes Responding to Low Frequency



Figure C3. Typical Current Shunts and an “Isolated” Probe

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0.01Ω is typical) resistors with four terminal connections for accurate measurement. In theory, measuring voltage across a current shunt should yield accurate information. In practice, common mode voltages introduce measurement difficulties, particularly at speed. Making this measurement requires an isolated probe or a high speed differential plug-in. The Signal Acquisition Technologies SL-10 (Figure C3) has 10MHz bandwidth, a galvanically floating input and 600V common mode capability. This probe allows any oscilloscope to take a floating measurement across a shunt.

Differential oscilloscope plug-ins, while not galvanically floating, can measure across a shunt. Tektronix types W, 1A5 and 7A13 have 1mV sensitivity with up to 100MHz bandwidth and excellent common mode rejection. Types 1A7 and 7A22 have $10\mu V$ sensitivity, although bandwidth is limited to 1MHz. All differential plug-ins have bandwidth and/or common mode voltage restrictions that vary with sensitivity. These trade-offs must be reviewed when selecting the optimal shunt value for a particular measurement. In general the smallest practical shunt value is desirable. This minimizes the inserted resistances parasitic effects on circuit operation.

APPENDIX D

Optimizing Switching Regulators for Efficiency

Squeezing the utmost efficiency out of a switching regulator is a complex, demanding design task. Efficiency exceeding 80% to 85% requires some combination of finesse, witchcraft and just plain luck. Interaction of electrical and magnetic terms produces subtle effects which influence efficiency. A detailed, generalized method for obtaining maximum converter efficiency is not readily described but some guidelines are possible.

Losses fall into several loose categories including junction, ohmic, drive, switching, and magnetic losses.

Semiconductor junctions produce losses. Diode drops increase with operating current and can be quite costly in low voltage output converters. A 700mV drop in a 5V output converter introduces more than 10% loss. Schottky devices will cut this nearly in half, but loss is still appreciable. Germanium (rarely used) is lower still, but switching losses negate the low DC drop at high speeds. In very low power converters Germanium's reverse leakage may be equally oppressive. Synchronously switched rectification is more complex, but can sometimes simulate a more efficient diode (see LTC Application Note 29, Figure 32). The LT1074's "Com Out" pin is intended to drive external synchronous switches. See Appendix A for details.

When evaluating synchronous rectification schemes remember to include both AC and DC drive losses in efficiency estimates. DC losses include base or gate current in

addition to DC consumption in any driver stage. AC losses might include the effects of gate (or base) capacitance, transition region dissipation (the switch spends some time in its linear region) and power lost due to timing skew between drive and actual switch action.

The LT1074's output switch is composed of a PNP driving a power NPN (Figure D1). The switch drop can reach 2V at high currents. This will usually be the major loss in the circuit. Its effect on efficiency can be mitigated by using the highest possible input voltage. Text Figure 7 shows 5V regulator efficiency improving almost 10% for higher input voltages. Higher output voltages will further minimize the switch losses.

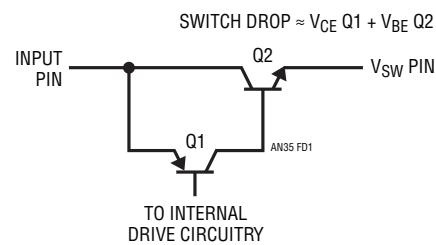


Figure D1. Simplified LT1074 Output Switch

Actual losses caused by switch saturation effects and diode drops are sometimes difficult to ascertain. Changing duty cycles and time variant currents make determination tricky. One simple way to make relative loss judgments is to measure device temperature rise. Appropriate tools here

include thermal probes and (at low voltages) the perhaps more readily available human finger. At lower power (e.g., less dissipation, even though loss percentage may be as great) this technique is less effective. Sometimes deliberately adding a known loss to the component in question and noting efficiency change allows loss determination.

Ohmic losses in conductors are usually only significant at higher currents. "Hidden" ohmic losses include socket and connector contact resistance and equivalent series resistance (ESR) in capacitors. ESR generally drops with capacitor value and rises with operating frequency, and should be specified on the capacitor data sheet. Consider the copper resistance of inductive components. It is often necessary to evaluate trade-offs of an inductor's copper resistance versus magnetic characteristics.

Switching losses occur when the LT1074 spends significant amounts of time in its linear region relative to operating frequency. At higher switching frequencies transition times can become a substantial loss source. The LT1074's 100kHz preset switching frequency is a good compromise (for this device) and changes should be carefully considered. Raising the switching frequency to gain some desired benefit necessitates consideration of increased LT1074 losses. 200kHz is the maximum practical operating frequency.

Magnetics design also influences efficiency. Design of inductive components is well beyond the scope of this appended section, but issues include core material selection, wire type, winding techniques, size, operating frequency current levels, temperature and other issues. Some of these topics are discussed in LTC Application Note 19,

but there is no substitute for access to a skilled magnetics specialist. Fortunately, the other categories mentioned usually dominate losses, allowing good efficiencies to be obtained with standard magnetics. Custom magnetics are usually only employed after circuit losses have been reduced to lowest practical levels.

A Special Circuit

In cases where input voltage must be low, but may float, Figure D2's circuit may be preferable to an LT1074 based approach. This circuit uses the LT1070, a common emitter output device. With the emitter connected to the ground pin this device's (LT1070 operating details are available in its data sheet, and in LTC Application Notes 19, 25 and 29) switch loss is significantly lower than the LT1074's. Although intended for voltage step-up in flyback configurations the LT1070 can be arranged to perform the step-down function. The advantage is the efficiency gain due to the reduced switch loss. The circuit's primary restriction is that the input must float with respect to the output. Q1 performs a level shift to get the feedback information referenced to the LT1070 "ground" pin, which floats with the input. The LT1070 is effectively "fooled" and behaves like a flyback regulator. It is oblivious to the fact that the overall function is step down, because the floating input is driven to the output potential. The negative side of the output filter capacitor is connected to the ground (\ominus) of the powered system, and the LT1070 input rail becomes the 5V output. Other voltages are obtainable by altering the 3.9k – 1.1k feedback ratio. Efficiency approaches 85%.

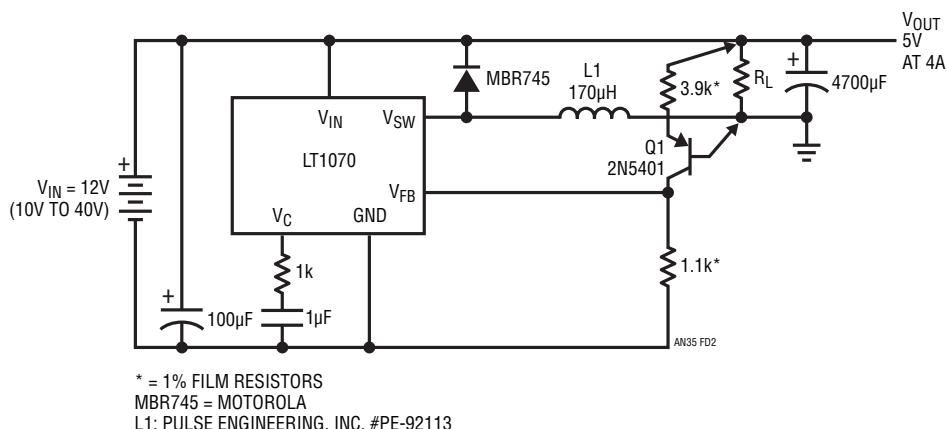


Figure D2. Floating Input Buck Regulator

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APPENDIX E

A Half-Sine Reference Generator

Text Figure 31's half-sine reference must be amplitude and frequency stabilized to a fairly high degree. It is not unreasonable to expect a 115V_{AC} 400Hz source to be within 1V and 0.1Hz. Additionally, Figure 31's reference requires a half-sine, as opposed to the more normal full-sine. These requirements are achievable by classical analog techniques, but a digital approach eases complexity with no performance trade-off¹⁴. Figure E3 shows such an approach. C1 forms a 1.024MHz crystal oscillator which is divided down by the 7490. The 7490's differentiated $\div 10$ output becomes the LT1074's 102.4kHz sync. option output. The 7490's $\div 5$ output (204.8kHz) is fed to the 74191 counters. These counters parallel load a 2716 EPROM which is programmed to produce an 8-bit (256 states) digitally coded half-sine. The program, developed by Sean Gold and Guy M. Hoover, appears in Figure E1.

The 2716's parallel output is fed to an 8-bit DAC, which produces 800Hz 2.5V (peak) half-sines.

Those wishing to utilize this reference for full-sines will find the appropriate software in Figure E2.

Figure E3 also shows the synchronous switch option discussed in the text. The 74C122 monostable forms a simple delayed pulse generator which drives the Q4 switch. The 20 μ s delay and 6 μ s pulse width set at the 74C122 were empirically determined to produce lowest overall crossover distortion in Figure 31's output.

Note 14: The sinewave is probably the paramount expression of the analog world. The Old Man Himself, George A. Philbrick, once elegantly discussed analog functions as "those which are continuous in excursion and time." He might have viewed digital production of a sinewave with considerable suspicion, or simply labeled it blasphemous. Such are the wages of progress.

Line	10801	Column	Wrap	APL2/PC												
				GNCODES												
00	03	06	09	00	10	13	16	19	1C	1F	22	26	29	2C	2F	
32	35	38	3B	3E	41	44	47	4A	4D	50	53	56	59	5C	5F	
62	65	68	6B	6D	70	73	76	79	7B	7E	81	84	86	89	8C	
8E	91	93	96	98	9B	9D	A0	A2	A5	A7	A9	AC	AE	B0	B3	
85	87	89	8B	8E	C0	C2	C4	C6	C8	CA	CB	CD	CF	D1	D3	
D5	D6	D8	DA	DB	D0	DE	E0	E1	E3	E4	E6	E7	E8	EA	EB	
EC	ED	EE	EF	F1	F2	F3	F4	F5	F6	F7	F8	F9	F9	FA		
FA	FB	FB	FC	FD	FD	FE	FE	FE	FF							
FF	FF	FF	FF	FF	FE	FE	FE	FE	FD	FD	FC	FB	FA	F9	F7	F6
FA	F9	F8	F8	F7	F6	F5	F4	F3	F3	F2	F1	EF	EE	ED	EC	
EB	EA	E8	E7	E6	E4	E3	E1	E0*	OE	DD	DB	DA	D8	D6	D5	
D3	D1	CF	CD	CB	CA	C8	C6	C4	C2	C0	BE	BB	B9	B7	B5	
B3	B0	AE	AC	A9	A7	A5	A2	A0	9D	9B	98	96	93	91	8E	
8C	89	86	84	81	7E	7B	79	76	73	70	6D	6B	68	65	62	
5F	5C	59	56	53	50	4D	4A	47	44	41	3E	3B	38	35	32	
2F	2C	29	26	22	1F	1C	19	16	13	10	00	09	06	03	00	

Figure E1. Half-Sine Software Code for the 2716 EPROM

Line	10736	Column	Wrap	APL2/PC											
				GNCODES											
FF	FF	FF	FE	FE	FE	FD	FD	FC	FB	FA	F9	F9	F7	F6	
F5	F4	F3	F1	F0	EE	ED	EB	E9	E8	E6	E4	E2	E0	OE	DC
D9	D7	D5	D2	D0	CE	C8	C9	C6	C3	C1	BE	BB	BB	B6	B3
B0	AD	AA	A7	A4	A1	9E	9B	98	95	92	8E	88	88	85	82
7F	7C	78	75	72	6F	6C	69	66	63	60	5D	5A	57	54	51
4E	4B	48	45	42	40	3D	3A	3B	35	33	30	2E	2B	29	27
25	22	20	1E	1C	1A	1B	17	15	13	11	10	0E	0D	0C	0A
09	08	07	06	05	04	03	03	02	02	01	01	00	00	00	00
00	00	00	00	01	01	02	02	03	03	04	05	06	07	08	09
0A	0C	0D	0E	10	11	13	15	17	18	1A	1C	1E	20	22	25
27	29	2B	2E	30	33	35	38	3A	3D	40	42	45	48	4B	4E
S1	S4	S7	SA	SD	60	63	66	69	6C	72	75	78	7C	7F	
82	85	88	8B	8E	92	95	98	9B	9E	A1	A4	A7	AA	AD	B0
B3	B6	B8	BB	BE	C1	C3	C6	C9	CB	CE	D0	D2	D5	D7	D9
DC	DE	E0	E2	E4	E6	E8	E9	E8	ED	EE	F0	F1	F3	F4	F5
F6	F7	F9	FA	FB	FC	FD	FO	FE	FF						

Figure E2. Full-Sine Software Code for the 2716 EPROM (Bonus)

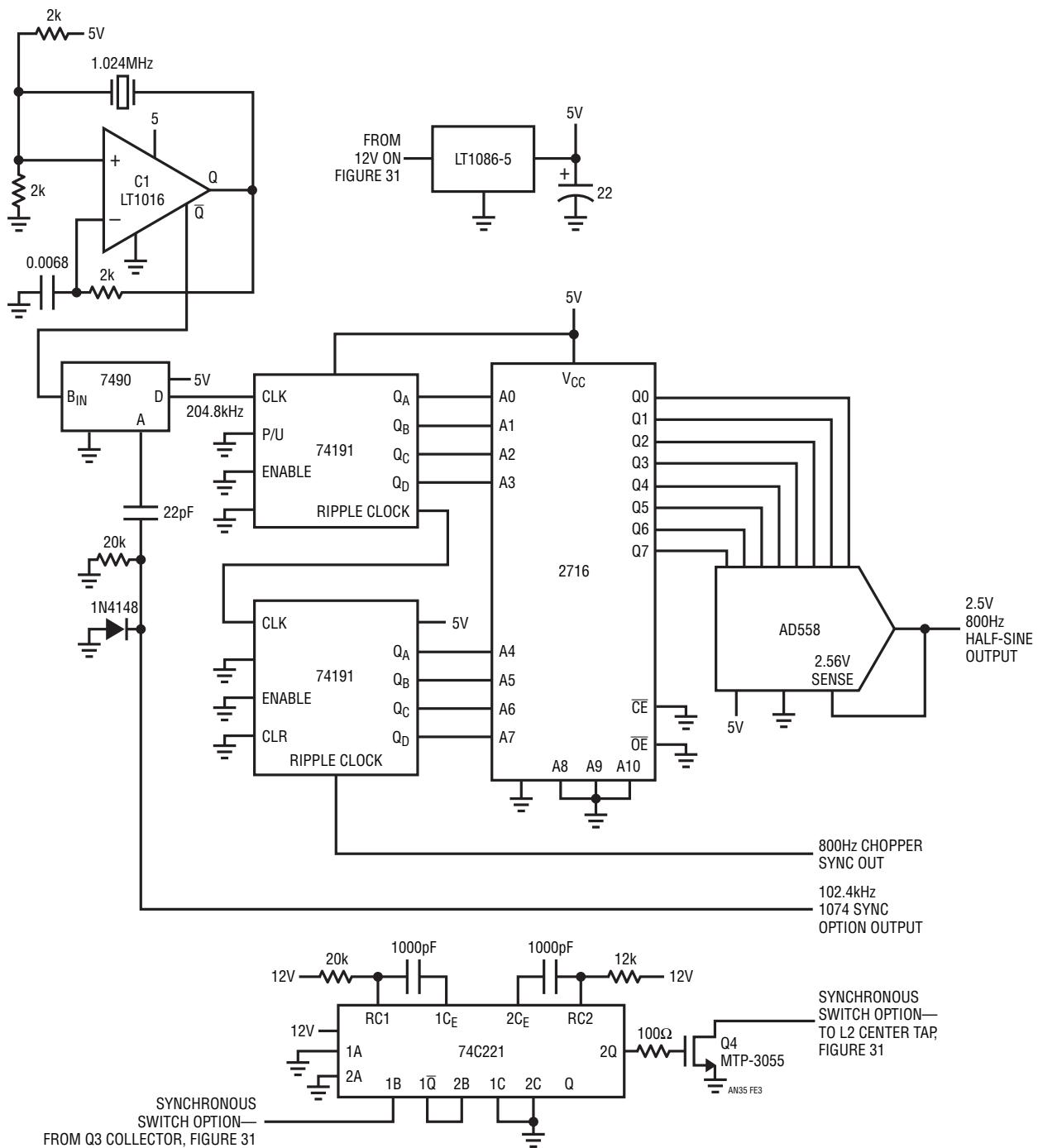


Figure E3. Timing and Reference Half-Sine Generator for Figure 31

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APPENDIX F

The Magnetics Issue

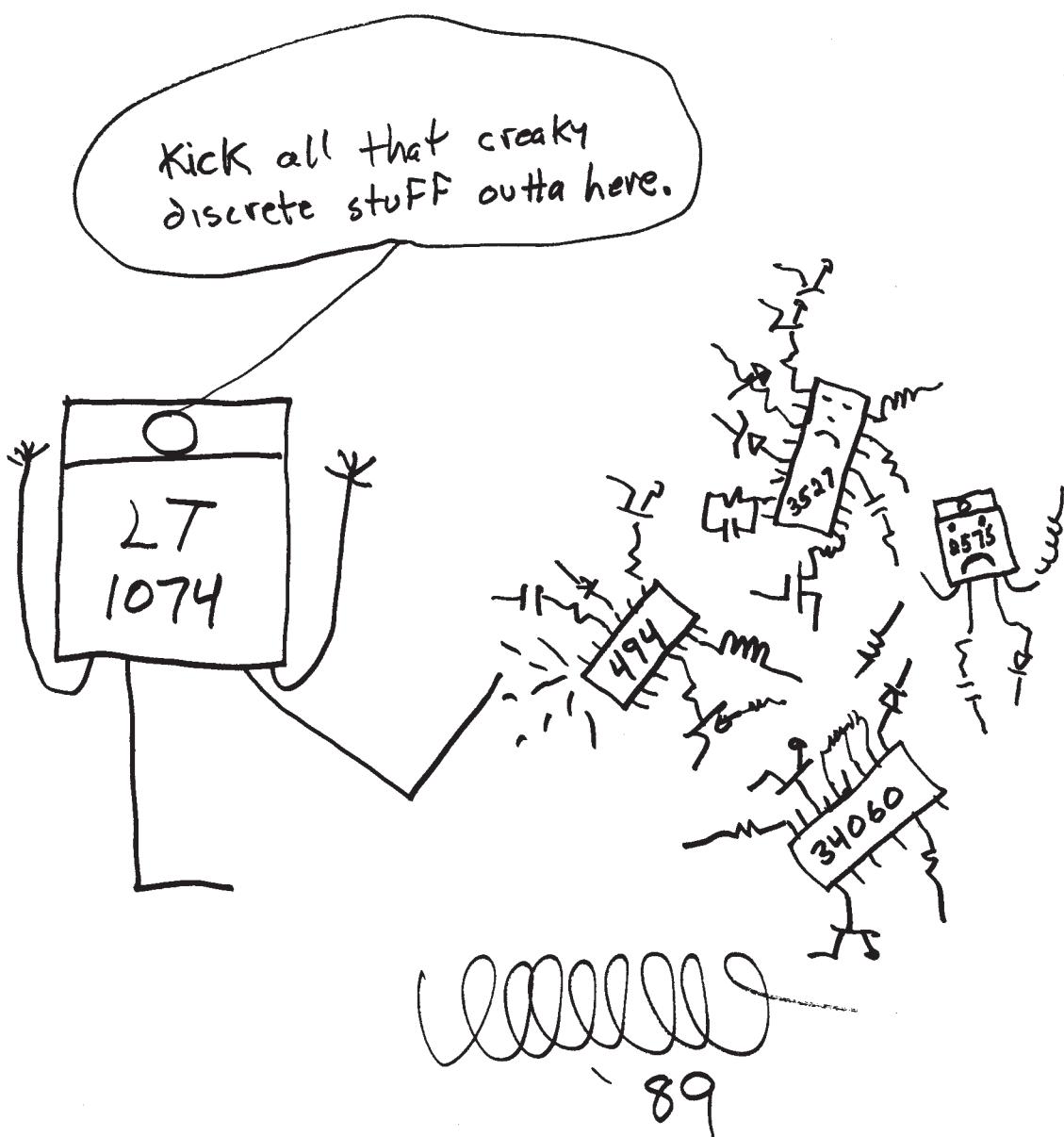
Magnetics is probably the most formidable issue in converter design. Design and construction of suitable magnetics is a difficult task, particularly for the non-specialist. It is our experience that the majority of converter design problems are associated with magnetics requirements. This consideration is accented by the fact that most converters are employed by non-specialists. As a purveyor of switching power ICs we incur responsibility towards addressing the magnetics issue (our publicly spirited attitude is, admittedly, capitalistically polluted). As such, it is LTC's policy to use off-the-shelf magnetics in our circuits. In some cases, available magnetics serve a particular design. In other situations the magnetics have been specially designed, assigned a part number and made available as standard product.

In many circumstances a standard product is suitable for production. Other cases may require modifications or changes which the manufacturer can provide or advise on. Hopefully, this approach serves the needs of all concerned.

Recommended magnetics manufacturers include the following;

Pulse Engineering, Inc
P.O. Box 12235
7250 Convoy Court
San Diego, California 92112
619-268-2400

Coiltronics
984 Southwest 13th Court
Pompano Beach, FL 33069
305-781-8900



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