Linear Circuits for Digital Systems
Some Affable Analogs for Digital Devotees

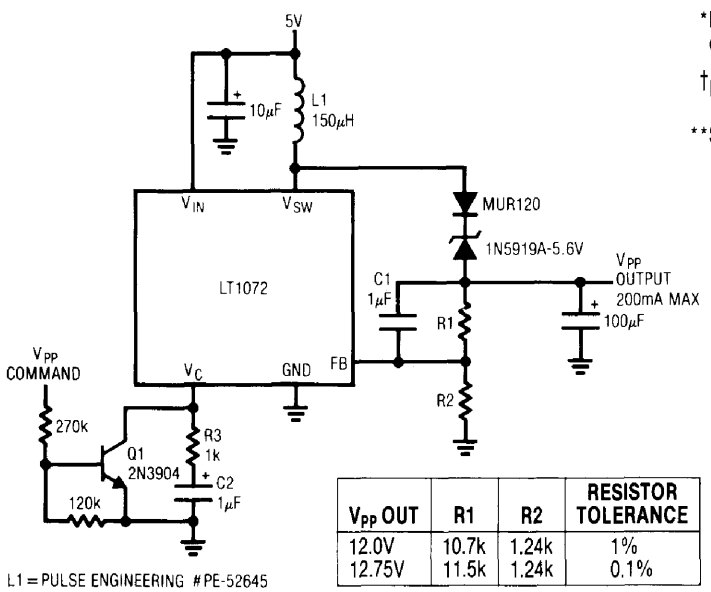
Jim Williams

The pristine, regimented symmetry of digital circuit boards is occasionally interrupted by an irregular huddle of linear components. These aberrants are tolerated because they perform a variety of ancillary tasks necessary to keep the digital system running. While I certainly wouldn't wish lifetime employment on a digital circuit board to anyone*, the reality is that the need exists. Power control, clock circuits and memory management are areas where linear circuits are needed in digital systems. Recently introduced flash memories offer a good example of linear circuits supporting a predominantly digital function. Flash memory adds electrical chip-erase and reprogramming to conventional EPROM capability. A full chip erasure takes 1 second with 100μs byte-program times and 4 seconds for full chip programming. These features make flash memories an attractive non-volatile memory option. Additional information on these devices appears in Appendix A, "A Primer on Flash Memory," guest written by Saul Zales of Intel Corporation.

These devices require carefully controlled, high voltage programming power. A typical unit, the Intel 28F010 1 megabit flash memory, specifies V_{PP} ($V_{PROGRAM\ POWER}$) pulses of 12V ± 0.6V or 12.75V ± 0.2V, depending on part type. V_{PP} excursions beyond 14V (for 20ns or longer) will destroy the ETOX† process based device. Reliably generating such pulses in a 5V powered digital system involves several analog issues. High voltage must be derived and controlled within the tight tolerances noted (see Appendix B for an expanded discussion of this topic). Additionally, it is desirable to control the high voltage pulses from a 5V logic command.

Basic Flash Memory Programming Voltage Supply

Figure 1's circuit meets almost all flash memory V_{PP} requirements. When the V_{PP} command goes low (Trace A, Figure 2) the LT1072** switching regulator drives L1, producing high voltage. DC feedback occurs via R1 and R2,



L1 = PULSE ENGINEERING #PE-52645

V_{PP} OUT	R1	R2	RESISTOR TOLERANCE
12.0V	10.7k	1.24k	1%
12.75V	11.5k	1.24k	0.1%

Figure 1. Basic Flash Memory V_{PP} Programming Voltage Supply

*I suppose it's not all that bad. Some of my best friends are digital circuits. If I had a daughter, I'd even consider letting her go out with one.

†ETOX is a trademark of Intel Corporation.

**See Appendix C and References for detailed information on the LT1072.

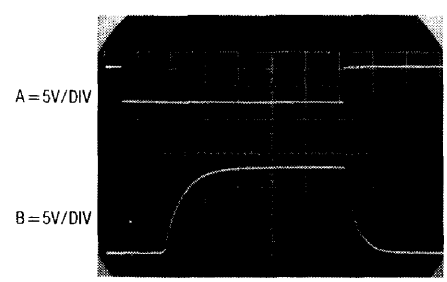


Figure 2. Waveforms for Basic Flash Programming Supply

with AC roll-off controlled by C1 and R3-C2. The result is a smoothly rising V_{PP} (Trace B) which settles to the required value. The specified R1 values allow either 12.0V or 12.75V outputs. The 5.6V zener permits the output to return to 0V when the V_{PP} command goes high. It may be deleted in cases where a 4.5V minimum output is acceptable or desirable (see Intel 28F010 datasheet). Precision resistors combine with the LT1072's tight internal reference to eliminate circuit trimming requirements. Alternately, 1% resistors and a trimmer may be used. Additionally, this circuit will not spuriously overshoot during power-up or down, preventing memory destruction. Figure 3's table details circuit changes permitting higher power outputs. The synchronous switch option can be used to eliminate the zener and its attendant power dissipation.

High Repetition Rate V_{PP} Programming Supplies

Figure 1's repetition rate is limited because the regulator must fully rise and settle for each V_{PP} command. Figure 4's circuit serves special cases which require higher repetition rate. Here, the switching regulator runs continuously, with the V_{PP} generated by the A1-A2 loop. If desired, the V_{PP} lock line can be driven, shutting down the regulator to preclude any possibility of inadvertent V_{PP} outputs. When V_{PP} lock goes low (Trace A, Figure 5) the LT1072 loop comes on (Trace B), stabilizing at about 17V. 2 pole compensation ensures a clean rise time. Pulling the V_{PP} command line low causes the 74C04 (Trace C) to bias the LT1004 reference. The LT1004 clamps at 1.23V with A1 and A2 giving a scaled output (Trace D). The 680pF capacitor controls loop slewing, eliminating overshoots. Figure 6 details the V_{PP} output. Trace A is the 74C04 output, with Trace B showing clean V_{PP} characteristics.

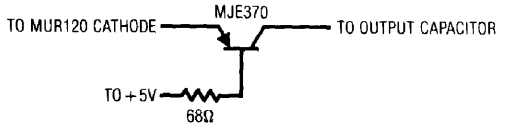
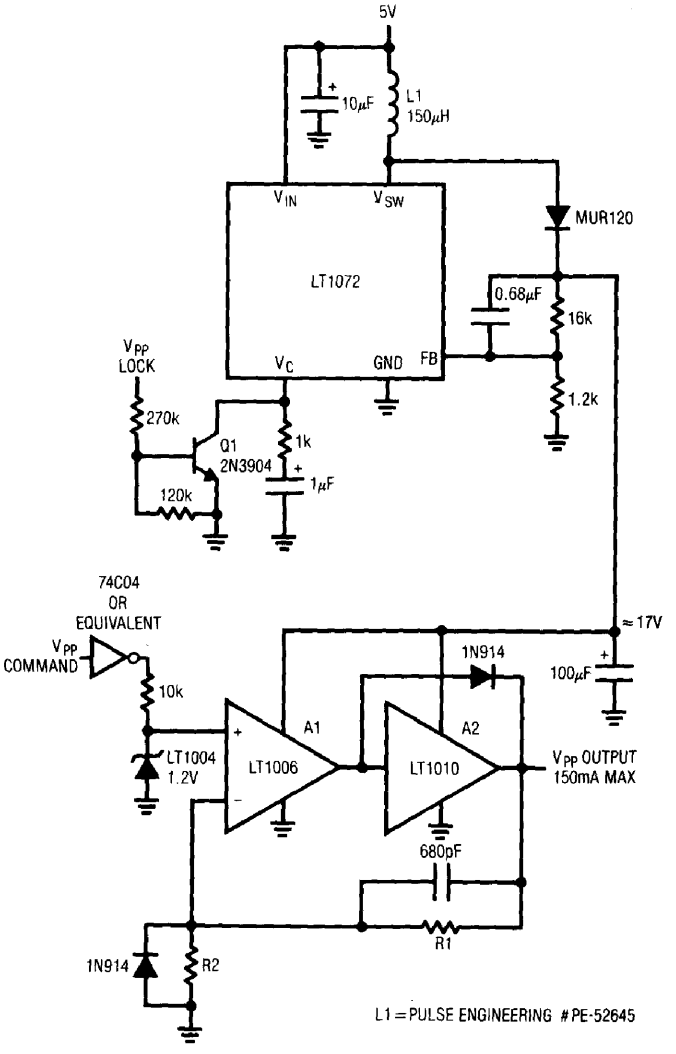


Figure 3. Synchronous Switch Option

Power Options for Basic V_{PP} Pulse Generator

OUTPUT CURRENT	C_{OUT}	REGULATOR	INDUCTOR	ZENER
400mA	200µF	LT1071	PE-52645	1N5339A or Synchronous Switch Option
800mA	400µF	LT1070	PE-51516	1N5339A or Synchronous Switch Option

Note: Assume each 28F010 device requires 30mA of V_{PP} current.



V_{PP} OUT	R1	R2	RESISTOR TOLERANCE
12.0V	10.7k	1.24k	1%
12.75V	11.5k	1.24k	0.1%

Figure 4. High Repetition Rate V_{PP} Programming Supply

As in Figure 1, spurious V_{PP} outputs are suppressed during power-up or down. The LT1010 provides 150mA drive (5 28F010's) and short circuit protection. The diode path around the LT1010 prevents destructive overshoot when the circuit is recovering from output shorts. The diode at A1's input clips excessive negative voltages due to the 680pF unit's differentiated response. Figure 7's circuit is similar to Figure 4's, except that the LT1010 has been replaced with a discrete power output stage, Q2-Q3. Q3 furnishes up to 800mA (26 28F010 memories), with Q2 used for current limiting. The feedback values have been increased, preventing Q2's collector current from causing excessive heating in the grounded resistor. This could occur during prolonged short circuit conditons. The feedback capacitor is re-established accordingly. The circuit's AC dynamics, including a glitchless short circuit recovery, are identical to Figure 4.

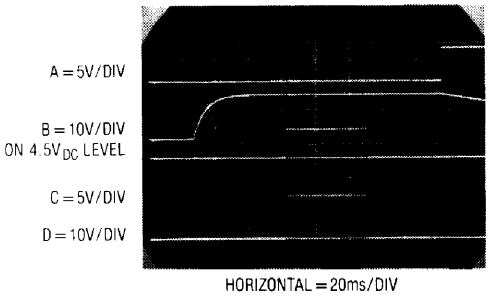


Figure 5. Operating Details of High Repetition Rate Flash Memory Programming Supply

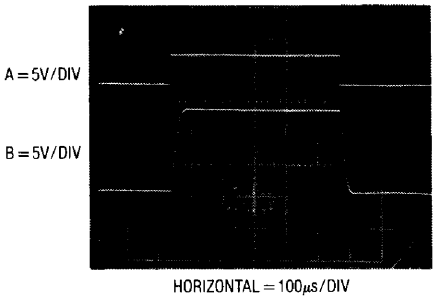
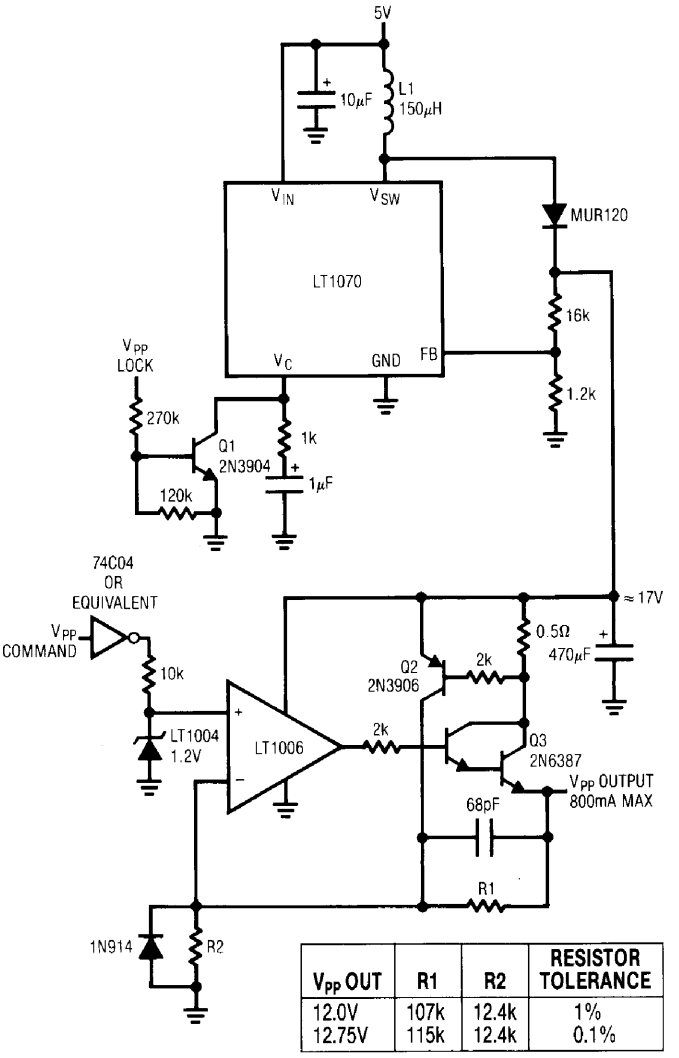


Figure 6. Expanded Scale Display of Figure 4's V_{PP} Output. Controlled Rise Time Eliminates Overshoots

In some systems high voltage is already available. In such cases the LT1070/72 circuitry may be deleted from Figures 4 and 7.

A good question might be: "Why not set the switching regulator output voltage at the desired V_{PP} level and use a simple low resistance FET or bipolar switch?". In theory, this approach will work. In practice, transmission line effects in printed circuit trace runs may cause memory destroying overshoots. Appendix B, "Preventing Memory Destruction," details this phenomenon.



V_{PP} OUT	R1	R2	RESISTOR TOLERANCE
12.0V	107k	12.4k	1%
12.75V	115k	12.4k	0.1%

L1 = PULSE ENGINEERING # PE-51516

Figure 7. High Power, High Repetition Rate V_{PP} Pulse Generator

V_{PP} Handshake Circuit

Both V_{PP} circuits shown require a small waiting period for the regulator to settle before proceeding with a V_{PP} operation. In almost all circumstances this is acceptable, but some situations may require verification that V_{PP} is within tolerance before pulsing begins. Figure 8's circuit, used in conjunction with either V_{PP} circuit, gives a handshake output when V_{PP} has settled. This simple circuit works by comparing the V_{PP} output against the known LT1004 reference voltage. The resistor values given allow for possible variations in V_{PP} voltage due to component tolerance stack-up. When this circuit is in use, the output of the V_{PP} generator circuit should be set within 0.4% of nominal value. This can be done by trimming, or using 0.05% resistors in place of the 0.1% units specified.

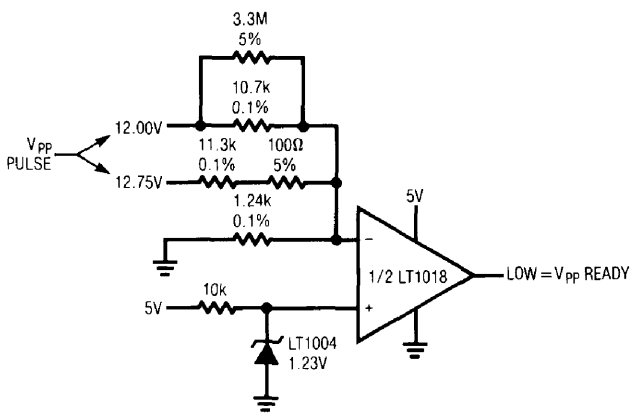


Figure 8. V_{PP} Handshake Circuit

EEPROM V_{PP} Pulse Generator

EEPROMs do not offer the advantages of flash memories, but are sometimes used. Their V_{PP} pulse requirements have commonalities with flash types. The 2816 specifies 21V ± 1V V_{PP} amplitude with a maximum allowable voltage of 22.5. A special EEPROM stipulation is that the V_{PP} pulse must have a 600µs rise time. Figure 9's circuit meets these requirements. The LT1072 generates the high voltage while A1 and A2 form the actual V_{PP} pulse. With the Erase/Write lock line low (Trace A, Figure 10), the LT1072 is in standby; no high voltage is produced and there is no circuit activity. Under these conditions the V_{PP} output line is pulled towards +5V via the 1N914 diode (see 2816 datasheet for details). When the Erase/Write lock line (Trace A, Figure 10) goes high, the regulator output (Trace C) builds smoothly and regulates at 25V. The 2 pole LT1072 compensation allows the regulator output to rise relatively quickly. When the V_{PP} command line (Trace B) is pulsed high, the LT1004 reference clamps at 1.23V and the RC network delivers a 600µs edge to A1's input. A1 combines with power buffer A2 and the feedback resistors to produce a 21V pulse at the V_{PP} output (Trace D). Trace E is a time and amplitude expanded version of this pulse. The 600µs RC rise time condition is met, with the 21V amplitude assured by the LT1004 reference and closed loop operation. When the V_{PP} command goes low, the V_{PP} output returns cleanly to 4.5 V. The diode path speeds recovery of the 0.005µF capacitor at A1's input. A2 provides a 150mA (ten 2816 EEPROMs) output with short circuit protection. As in Figure 4, a diode path around the LT1010 prevents overshoot when the circuit is recovering from output shorts. When the Erase/Write lock line returns low, the regulator output decays towards zero. As with the other V_{PP} circuits, this design does not produce undesired outputs during power-up or down.

5V Powered 4-20mA Current Loop Generator

Figure 11's circuit also employs voltage step-up, but for a different purpose. Transmission of industry standard 4-20mA current loop signals to valves and other actuators is a common requirement. Resistive line losses and actuator impedances require current transmitters to be able to force a compliance voltage of at least 20V. Because of this, 5V powered systems usually cannot meet current loop transmitter requirements, but Figure 11 shows a way to do this. This 5V powered circuit utilizes a servo controlled DC-DC converter to generate the compliance voltage necessary for loop current requirements. It will drive 4-20mA into loads as high as 2200Ω (44V compliance) and is inherently short circuit protected. Its digital inputs permit easy interface to digital systems.

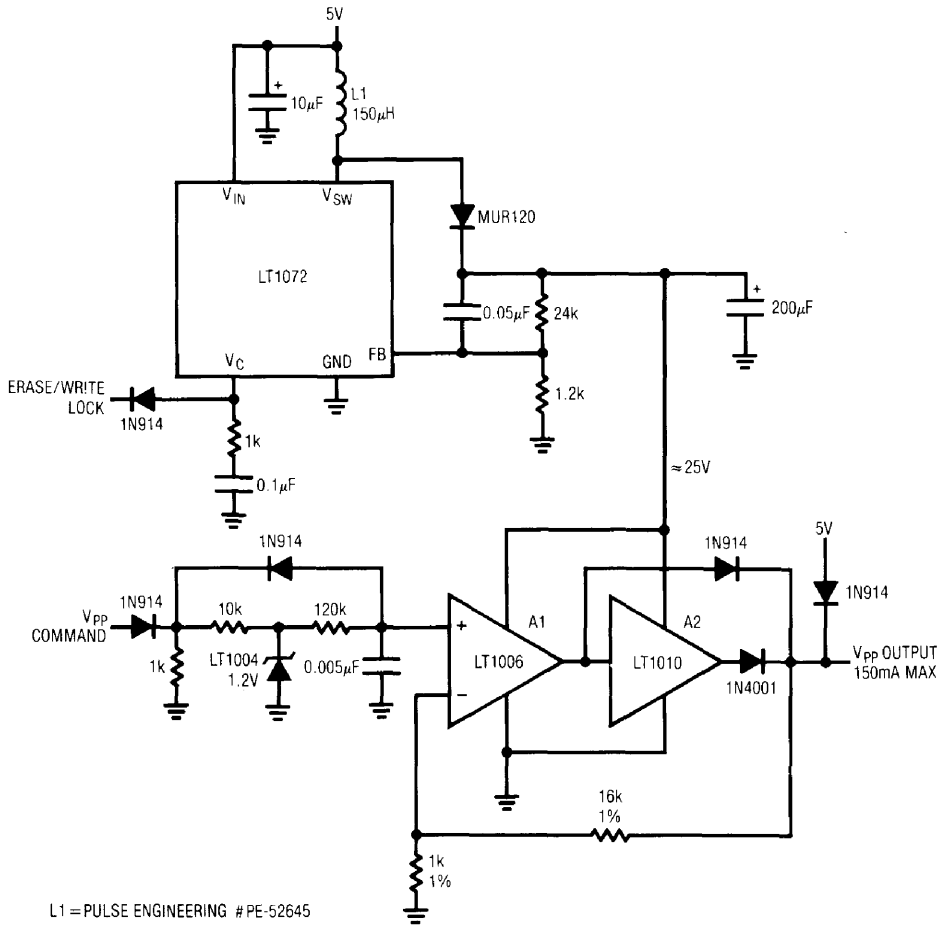


Figure 9. EEPROM V_{PP} Pulse Generator

The AD558 8 bit D→A converter receives the circuit's digital inputs, producing a 2.56V full-scale output. A1's positive input voltage is determined by the D→A output and the 4mA trim network output. A1's output biases the LT1072's V_C pin. This forces the switching regulator to run at the output voltage necessary to balance A1's inputs. The feedback path for this action is through the load, across the 75Ω resistor and back to A1's negative input. The 240Ω-0.05μF combination stabilizes the loop. The 7.5V zener permits regulator output down to 0V. The resistors connected to the LT1072's feedback (FB) pin prevent circuit output from running away in the event the load opens up. Normally, A1 controls the loop, forcing the LT1072 to produce the voltage required to maintain the D→A directed current through the load. If the load opens, A1 receives no feedback, but the FB pin becomes active at 1.2V, forcing the loop to close locally around the LT1072. In this fashion the circuit automatically crosses over from a current to a voltage regulator, preventing excessive output voltages from occurring.

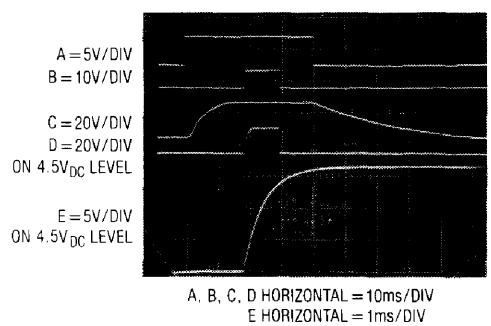


Figure 10. EEPROM Pulse Generator Waveforms

Figure 12 details LT1072 operation under normal conditions. Trace A is V_{SWITCH} pin voltage, while Trace B indicates its current. Trace C, the MUR120 diode current, clearly shows the switched packets of energy delivered to the 22μF output capacitor. The resultant output ripple voltage (Trace D) measures only 25mV at the load.

Figure 13 catches circuit output at the instant a load open has occurred. Normal current mode operation ceases just past the third vertical division. The "+" output line heads positive until the LT1072 FB pin rises to 1.2V. At this point (just past the 6th vertical division), the LT1072's internal feedback amplifier activates, causing local loop closure and regulating the output at about 57V. The non-linear slew characteristic is due to A1's feedback capacitor restrained response. Once A1's output rails, slew increases to a limit imposed by L1, the 22μF output capacitor and the LT1072's 40kHz switching rate.

To trim this circuit, connect any load below 2kΩ and set all DAC bits low. Adjust the 4mA trim for 0.300V across the 75Ω resistor. Next, put all DAC bits high and set the 20mA trim for 1.500V across the 75Ω resistor. Repeat this procedure until both points are fixed.

AC Line Dropout Detector

Digital systems driven from the AC line often require power dropout detection. Fast AC line dropout detection allows a memory store command to be issued before DC

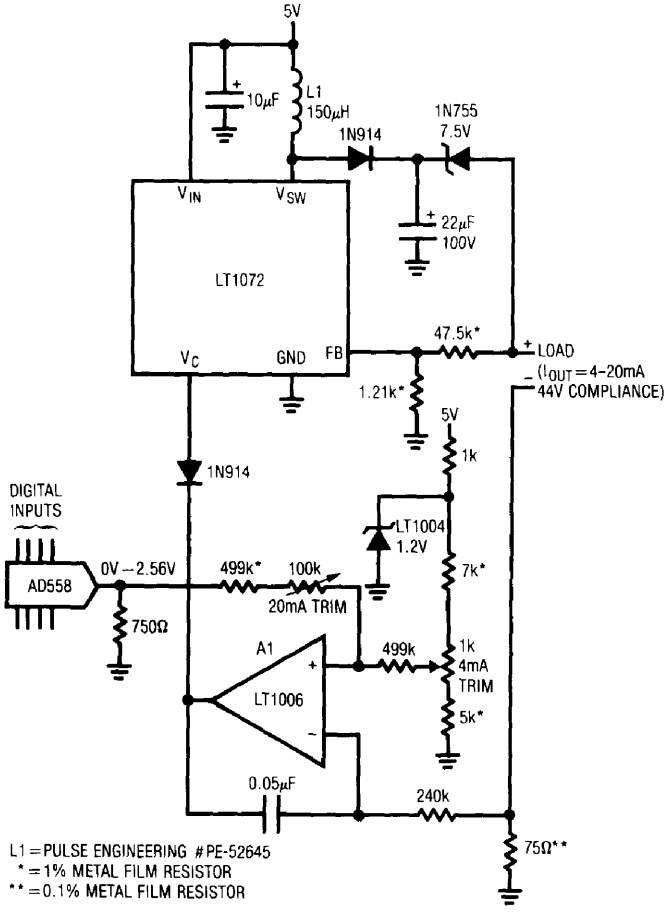


Figure 11. 5V Powered, Digitally Controlled 4-20mA Current Loop Generator

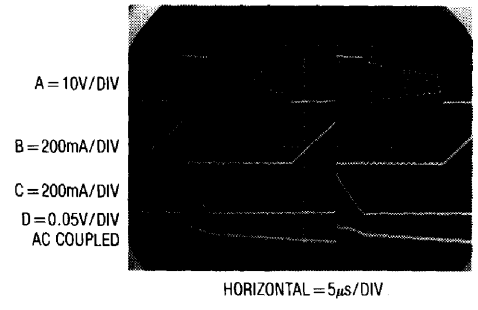


Figure 12. Figure 11's Waveforms

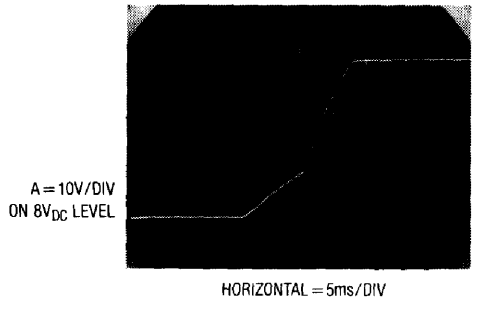


Figure 13. Open Load Characteristics for Figure 11's Current Source. LT1072 Crosses over into Constant Voltage Mode at 57V

power falls. Figure 14's circuit detects AC dropout by connecting an optoisolator across the power transformer's rectified secondary. Normally, the AC line (Trace A, Figure 15) turns on the LED every 8ms (1/2 cycle of the line), causing the output transistor to reset the 0.01μF capacitor (Trace B). When the line drops out, the capacitor charges via the 33k resistor. The resultant ramp voltage is compared by C1A to a +5V supply derived reference. In this case, the 2k-3k resistors bias C1A to go low (Trace C) within one cycle of AC line dropout. Typically, the DC regulator will supply 50ms-100ms of hold-up before it begins to sag. This hold-up period, which should be verified in any individual application, permits adequate time to execute a memory store operation. C1B serves as a final warning that power failure is imminent. It goes low when the 5V regulator input drops below the threshold set by the selected resistor shown on the schematic. This value should be chosen so that C1B trips when the regulator input approaches its specified dropout voltage.

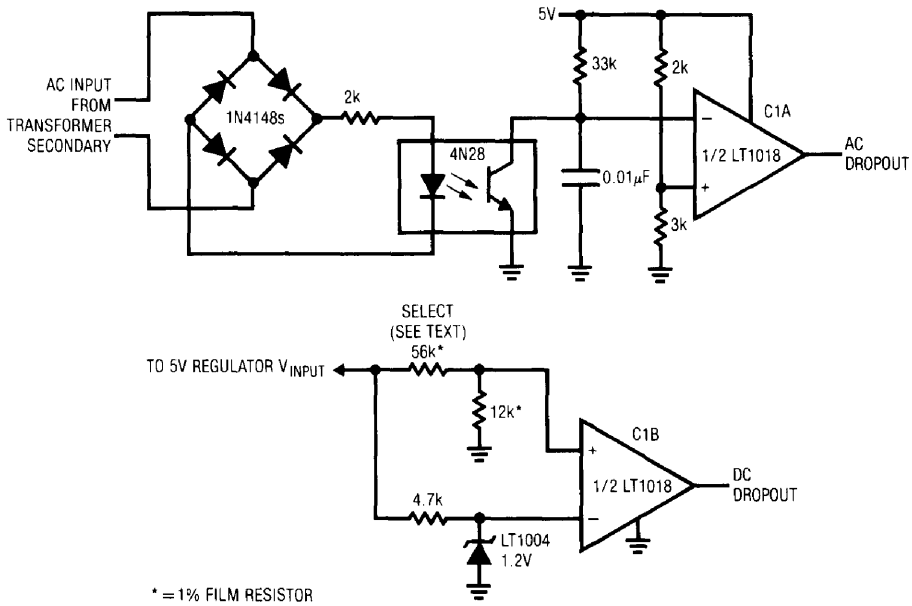


Figure 14. AC-DC Dropout Detector

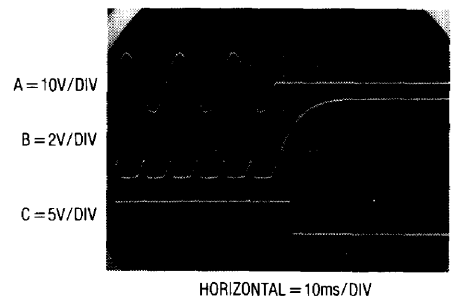


Figure 15. AC Line Dropout Detector Operates within a Half Cycle

Memory Save Circuit

Figure 16 is another circuit for saving memory contents when power goes down. This DC sensing circuit is useful where AC line dropout detection is not feasible. It functions by utilizing the different dropout voltages of two regulators. In operation, the LT1086 supplies 5V power to the main system, while the LT1020 drives the memory section. When input power, which could be from a battery or filter capacitor, falls (Trace A, Figure 17) the LT1086 drops out first (Trace B). This is detected by the LT1020's onboard auxiliary comparator, which goes low (Trace C). This alerts the memory section to store data. The LT1020 regulator output (Trace D) maintains memory power for additional time due to its extremely low dropout characteristics. It finally begins to fall about 50ms after the memory store command. The optional connections shown allow extended hold up times.

Overvoltage Protection Circuit

Figure 18's circuit represents the other extreme in power supply protection. It prevents system damage due to overvoltage produced by regulator failure. If the regulator fails in a way which effectively connects the raw DC supply to the 5V rail, overvoltage will occur. This failure mode is possible if the pass transistor shorts or the feedback loop opens up. C1A compares the 5V supply (Trace A, Figure 19) to the LT1004 reference via a resistive divider. If the supply rises beyond 5.5V (rise starts just past the first vertical division), C1A's output goes high (Trace B), turning on the SCR via Q1. SCR current (Trace C) peaks at almost 6A as it "crowbars" the supply, blowing the downstream fuse. C1B simultaneously pulls the supply feedback node low, ensuring minimum pass transistor on-resistance if the overvoltage is due to feedback or error amplifier malfunction. About 5μs elapses from the time the supply peaks (5.5V) until it begins to shut down. In this case the maximum overvoltage is 5.7V. The 4.3k-1.2k resistor string ratio can be altered for different trip values, and the optional filter used to suppress transients. Note that the LT1018's 1.2V minimum supply voltage combines with the diode in the SCR's gate to eliminate false tripping on power-up.

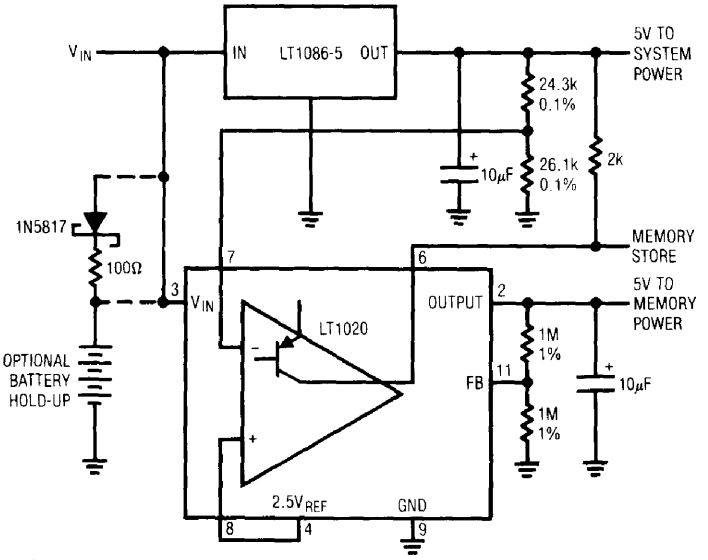


Figure 16. Memory-Save-On-Power Down

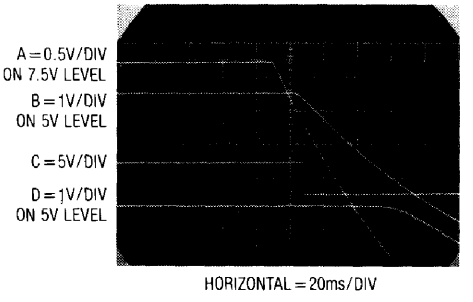


Figure 17. Differential Dropout Between Regulators Provides a Memory Store Pulse and Power Hold-Up

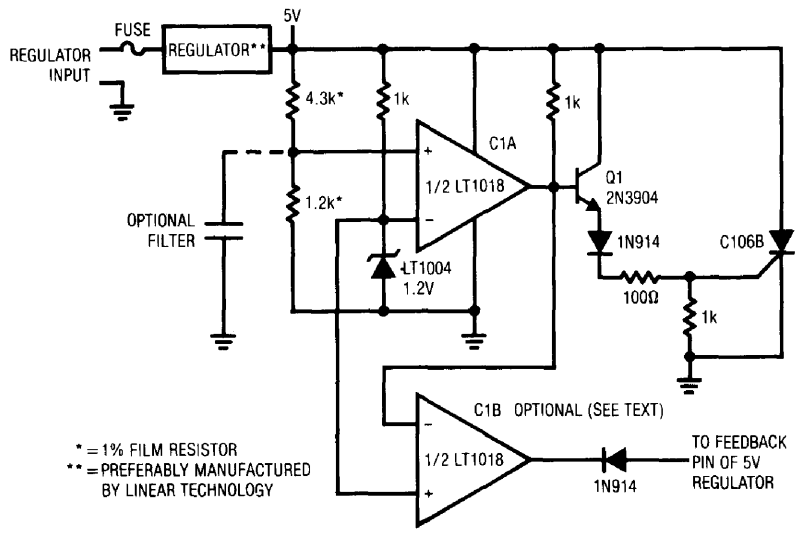


Figure 18. "Crowbar" Overvoltage Protection Circuit

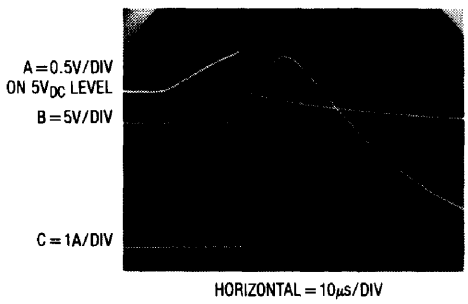


Figure 19. "Crowbar" Stops Overvoltage in 5μs

Power-On-Reset Generator

Another power related requirement involves generating a system reset pulse after supply turn-on. When supply power is applied to Figure 20, the 5V rail comes up (Trace A, Figure 21). The LT1004 clamps at 1.2V and C1A's positive input (Trace B) ramps at a time constant determined by the 0.5% resistors and the 0.1μF capacitor. When C1A's positive input ramps beyond the LT1004 potential, its output goes high, delivering a differentiated pulse to C1B's negative input (Trace C). C1B's output (Trace D) goes low for a period determined by the 0.01μF-680k differentiator. This pulse is used for system reset. The 1N914 gives quick reset for the 0.1μF delay capacitor and the Schottky diode clip's differentiator caused negative voltages at C1B's input. The turn-on threshold, in this case 4.8V, is set by the ratio of the 0.5% resistors. The output pulse delay time is controlled by the 0.1μF unit, which may be varied. Similarly, the RC combination at C1B sets output pulse width, and may be varied. The LT1018's 1.2V minimum supply voltage prevents spurious output during supply power-up.

"Watchdog" Timer Circuit

Figure 22's circuit is not for power supply management, but serves to prevent lock-up in processor based systems. This can occur if the system misses an instruction due to transient hardware or software events. Such a processor hang-up will usually cause predictable cessation of pulse events somewhere in the system. This circuit issues a reset command in response to such a cessation. In normal operation, a pulse train (Trace A, Figure 23) appears at the circuit input, causing C1A's output (Trace B) to pulse low. The diode path discharges the 0.01μF capacitor (Trace C) each time C1A's output goes low. Interruption of the input pulse train (after the 7th vertical division) allows the capacitor to charge beyond C1B's threshold, triggering it low. This pulse can be used to reset the system. C1B's negative input RC values may be adjusted to accommodate various input pulse train repetition rates.

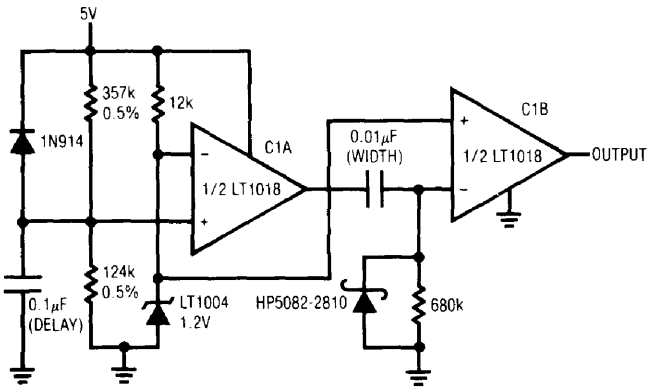


Figure 20. Power-On-Reset Pulse Generator

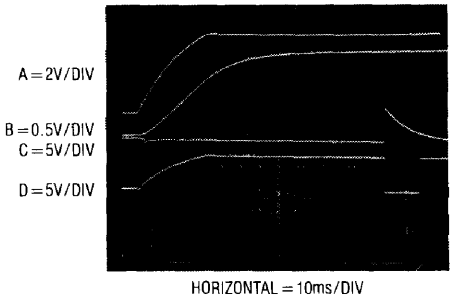


Figure 21. Power-On-Reset Pulse is Generated after Supply Stabilizes

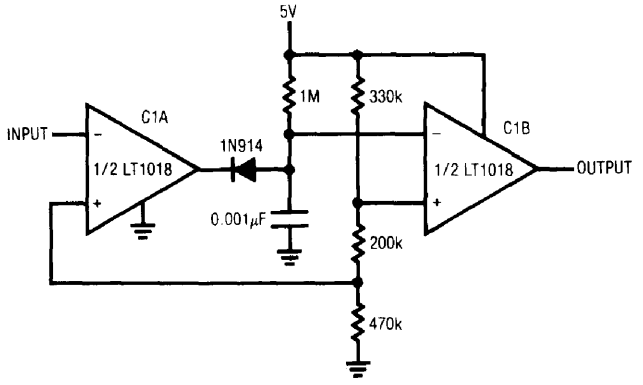


Figure 22. "Watchdog" Timer Circuit

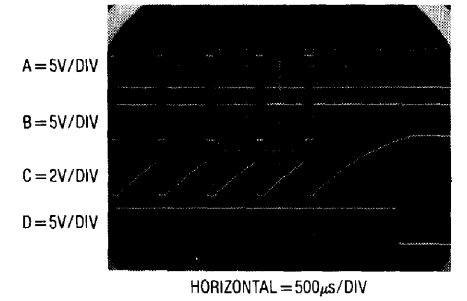
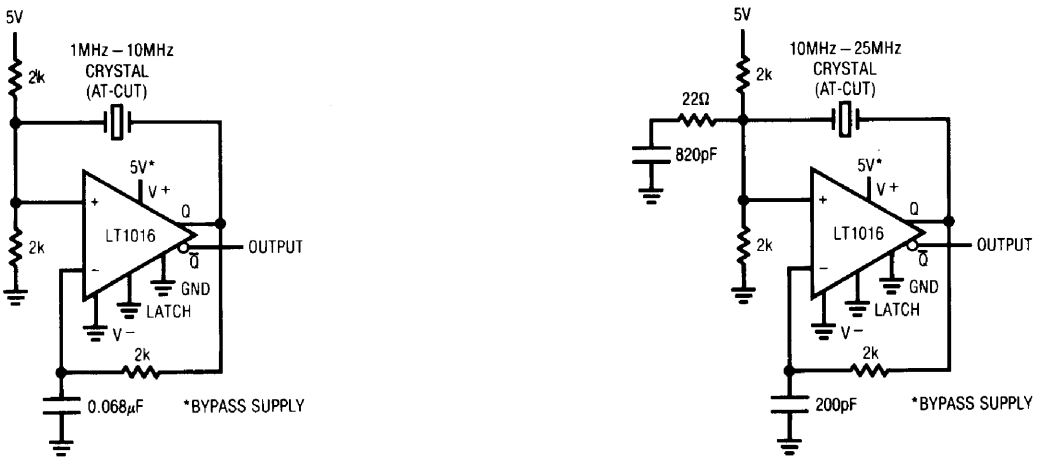


Figure 23. "Watchdog" Drops Low (Trace D) when Pulse Train Ceases

Clock Circuits

Almost all digital systems require a clock source. Generating accurate and reliable clock pulses usually involves quartz based circuits. Figure 24's two circuits cover a 1MHz-25MHz range. In Figure 24A, the LT1016 comparator is set up with DC negative feedback. The 2k resistors set the common-mode level at the device's positive input. Without the crystal, the circuit may be considered as a very wideband (50GHz GBW) amplifier biased at 2.5V. With the crystal inserted, positive feedback occurs and oscillation commences. Figure 24A is useful with AT-cut fundamental mode crystals up to 10MHz. Figure 24B is similar, but supports oscillation frequencies to 25MHz. Above 10MHz, AT-cut crystals operate in overtone mode. Because of this, oscillation can occur at multiples of the desired frequency. The damper network rolls off gain at high frequency, ensuring proper operation.

Figure 25's circuit is also similar, but optimized for lower frequency crystals. C1A is the oscillator, with C1B and Q1 used as a sink-source buffer if desired. These circuits also operate with lower cost and lower performance ceramic resonators substituted for the crystal.



A. 1MHz-10MHz Circuit

B. 10MHz-25MHz Circuit

Figure 24. Crystal Oscillator Clock Circuits

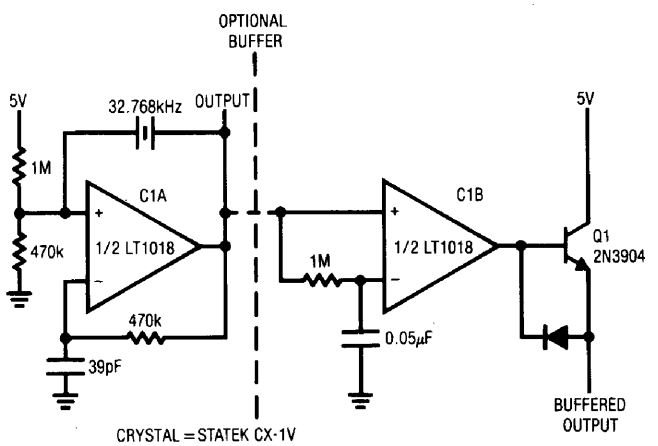


Figure 25. Low Frequency Crystal Oscillator Clock

High Noise Immunity Line Synchronous Clock

Although crystal based circuits are universally applied, they cannot serve all clock requirements. As an example, many systems require a reliable 60Hz line synchronous clock. Zero crossing detectors or simple voltage level detectors are often employed, but have poor noise rejection characteristics. The key to achieving a good line clock under adverse conditions is to design a circuit which takes advantage of the narrow bandwidth of the 60Hz fundamental. Approaches utilizing wide gain-bandwidth, even if hysteresis is applied, invite trouble with noise. Figure 26 shows a line synchronous clock which will not lose lock under noisy line conditions. The basic RC multivibrator is tuned to free run near 60Hz, but the AC-line-derived synchronizing input forces the oscillator to lock to the line. The circuit derives its noise rejection from the integrator characteristics of the RC network. As Figure 27 shows, noise and fast spiking on the 60Hz input (Trace A, Figure 27) has little effect on the capacitor's charging characteristics (Trace B) and the circuit's output (Trace C) is stable.

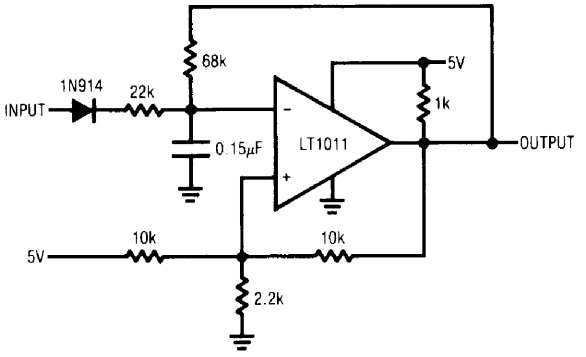


Figure 26. High Noise Immunity Line Synchronization Circuit

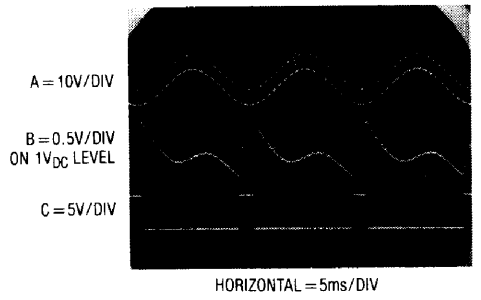


Figure 27. Line Synchronization is Maintained Despite Noisy Input

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Note: *This application note was derived from a manuscript originally prepared for publication in EDN magazine.*

APPENDIX A
A Primer on Flash Memory

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Intel Corporation

High integration, supported by dense memory, is the key to compact, reliable firmware-based equipment. These products often need post-sales update service for the latest software revisions. While providing high density, EPROMs are costly to update. Equipment must be dismantled, either to UV-erase and then reprogram the EPROMs or to replace them with new ones. This takes at least 15 minutes of a technician's time. Double that if you wait for UV erasure. In contrast, flash memories allow reprogramming "in-system" — in seconds. They are not discarded as EPROMs often are. The simplicity and speed of the update process yields even bigger savings. Thus, flash memory technology dramatically reduces firmware update costs in EPROM applications.

Non-volatile memory history illustrates flash memory technology's utility. EPROM gave users more control over their code than with ROM by moving the memory coding operation from component purchasing to factory assembly. Similarly, flash technology extends this flexibility. In the factory, it allows multiple test code programming during a single board-testing step. Testing enhances product quality while reducing rework and warrenty repair costs.

Beyond the factory, flash technology provides the highest level of code management functionality. Though E²PROM has more functions, its characteristics best suit parameter, as opposed to code, storage. Parameters need to be rewritten individually in real time, that is, while the system is on-line, in normal operation. Parameters also require less memory than code. E²PROM trades off density for the byte-alterable functionality needed for parameter storage.

In contrast, flash memories ideally match embedded code needs. Even if only one line of code needs modification, an entirely new microcomputer program results. Software updates are done as a complete copy for simple code verification. This ensures error-free updating. Flash memory technology mirrors this process with its full-chip erase characteristics in a few seconds of off-line system time.

This framework for delineating non-volatile memory roles is summarized in Figure A1. ROM, EPROM, and flash memory handle large amounts of code, which is installed or modified (excepting ROM) off-line, along an 'increasing flexibility' scale. E²PROM handles smaller amounts of on-line-modified parameters.

The most powerful reprogramming method is In-System Write (ISW). ISW eliminates external programming equipment altogether. It facilitates updates through an existing data communication channel, such as a modem. ISW utilizes the embedded, local CPU for the flash memory device reprogramming 'intelligence,' taking advantage of the off-line nature of updates. The only new requirement for ISW is providing a local programming power supply (V_{PP}), either 12.0V or 12.75V, depending on device specifications. Intel's command register architecture drives reprogramming control: 1) without extra device pins, 2) from a fixed V_{PP} supply, and 3) using standard system read and write timings (though some operations require millisecond-range durations, they are initiated and terminated with standard memory interface timings). See Figure A2 for system block diagram.

Reliability

Intel's ETOX flash memory devices endure up to 10,000 reprogramming cycles, just like E²PROM , yet with EPROM-like quality. The cycling advantage over E²PROM is derived partly from lower-voltage operation. This reduces the electric field intensity across the tunnel oxide by about 2 megavolts per centimeter. Each MV/cm electric field reduction increases the device reliability lifetime by at least one thousand (and as much as ten million) times.

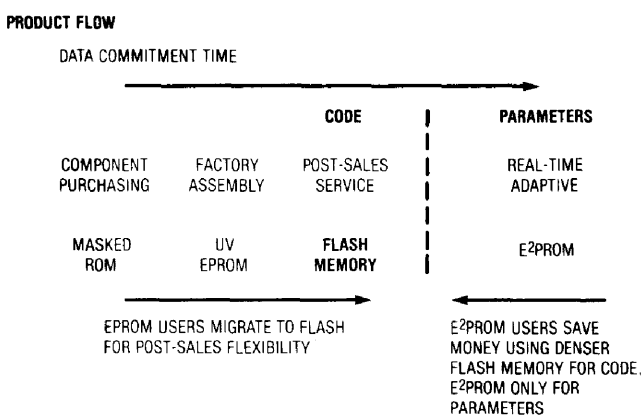


Figure A1. Non-Volatile Memory Flexibility Spectrum

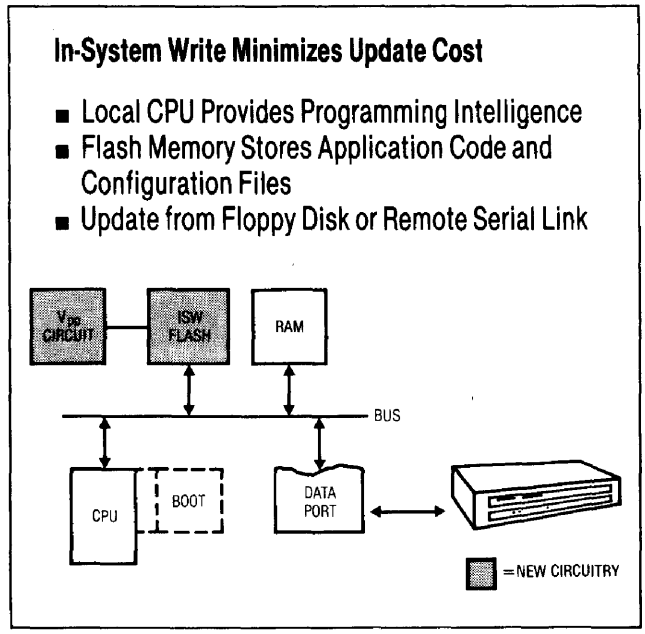


Figure A2. In-System Write

The common-source approach for erasure is another key contributor. Unlike other E²PROM and flash technologies, ETOX technology uses separate junctions for program and erase which yields: 1) much lower oxide stress, and 2) the ability to optimize the manufacturing process for both program and erase performance and durability. Finally, cycling and overall reliability of ETOX technology-based products is enhanced by the tunnel oxide process employed.

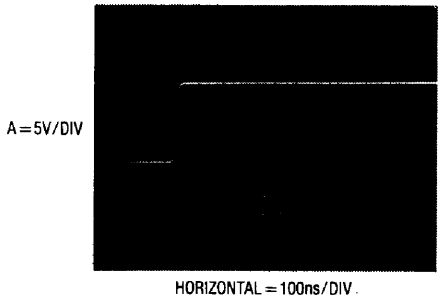
Intel specifies flash memory endurance to be less than 0.01% failures over 100 cycles and 0.1% for 10,000 cycles. In contrast, E²PROMs typically specify 5% failure rates for 10,000 cycles. Lifetime reliability testing of the data retention shows that ETOX technology meets or exceeds EPROM reliability.

APPENDIX B
Preventing Memory Destruction

The 12V or 12.75V V_{PP} supplies used with flash memories seem uncomfortably close to the devices 14V breakdown limit. In actuality, the precautions required are similar to overvoltage considerations for 5V rails. Excursions beyond 14V for durations longer than 20ns exceed the chip's absolute maximum rating. As such, the design of V_{PP} generating circuitry requires care to avoid seemingly mysterious memory failures. Although this section uses the 28F010 flash memory as an example, the considerations are generally applicable to other type devices (e.g., 2816).

In theory, a simple low loss transistor switching a low impedance power supply will work. In practice, this is a hazardous approach. Figure B1 shows an ideal V_{PP} pulse produced by simple transistor switching from a power supply. Settling to the desired V_{PP} level occurs quickly, with no overshoots or abberations. Figure B2 shows *the same output* measured at the memory pins after a printed circuit trace run. The PC trace looks like an unterminated transmission line with ill-defined characteristics. Reflections occur, causing ringing which exceeds 20V. This is well beyond specified destructive levels, and almost guarantees chip failures. Similar overshooting on the falling edge can cause equally destructive negative voltages to appear at the memory pins.

These effects demonstrate the necessity for rise time control. The controlled edge times of the text's closed loop circuits eliminate this problem. Some other features of these circuits make them attractive. Short circuit protection is obviously desirable to protect the V_{PP} generator.



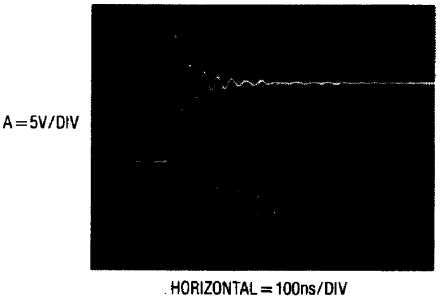


Figure B1. An "Ideal" Flash Memory V_{PP} Output ..... Figure B2. Rings at Destructive Voltages After a PC Trace Run

More subtly, it also protects the memory. In an unprotected V_{PP} generator, the pass switch may fail in a shorted condition. This will cause the memory to see destructive overvoltage and fail. The short circuit protection must be designed so that it does not cause overshoots when operating or recovering from overload. For example, removing A2's shunt diode path in text Figure 4 causes dangerous overshoots on short circuit recovery. Figure B3 shows V_{PP} output recovery with the diode removed. In Figure B4, the diode is installed and recovery is benign. Similar considerations apply on power-up and down. The V_{PP} generator must not produce spurious outputs during power application or removal. In the text circuits, this is facilitated by employing circuit techniques and ICs which operate down to low voltages. This makes V_{PP} outputs predictable and controllable during transient supply conditions.

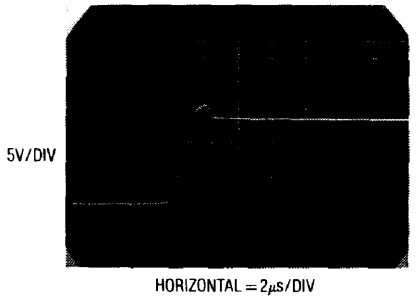


Figure B3.

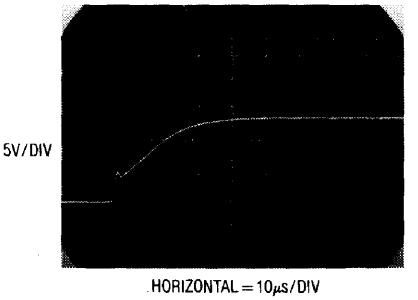


Figure B4.

Short Circuit Recovery for Poorly (Figure B3) and Properly (Figure B4) Designed Connections. Figure B3's Overshoot on Recovery Can Cause Memory Chip Failures

APPENDIX C
Physiology of the LT1070/LT1071/LT1072

The LT1070 series is a family of current-mode switchers with switch duty cycle directly controlled by switch current rather that by output voltage. Referring to Figure C1, the switch is turned on at the start of each oscillator cycle. It is turned off when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage-sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short circuit conditions. A low dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1070. This low dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns on the output switch via the logic and driver circuitry. Special adaptive antisaturation circuitry detects onset of saturation in the power switch and adjusts drive current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, is programs the LT1070 to disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1070 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer-coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1070 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft-starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor-coupled external clamp will provide soft-start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1070 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown with only 50μA supply current for shutdown circuitry biasing. For more details, see Linear Technology Application Note AN-19, pages 4-8.

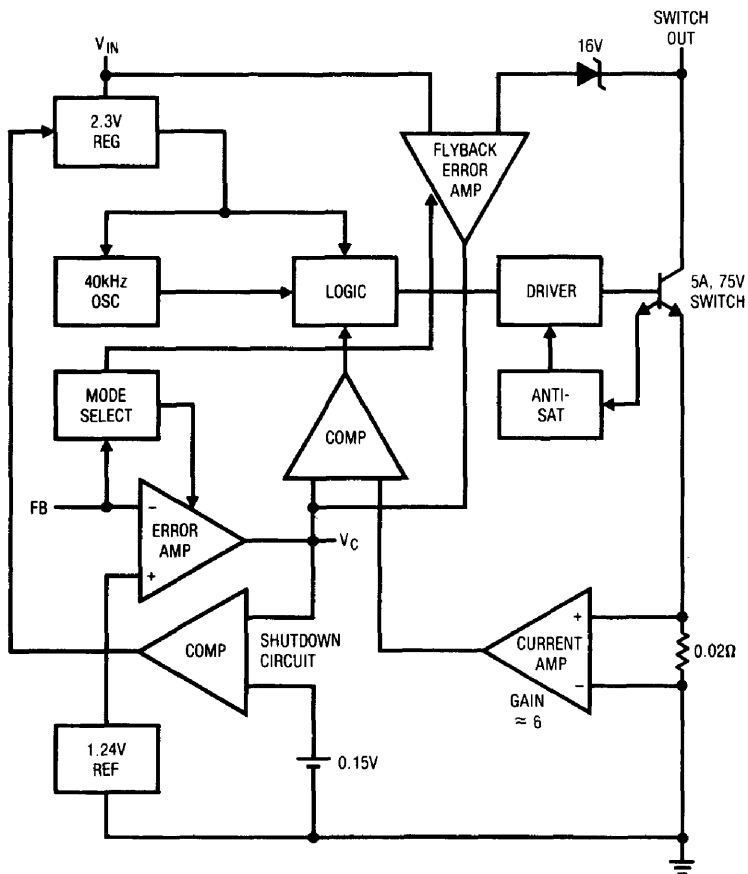


Figure C1. LT1070 Internal Details