

Hardware Engineer's Guide

Power

| Power Supply | Description | Advantages | Disadvantages |
|--------------------|---|---|--|
| LDO | Linear Drop Voltage Drops excess voltage as heat | Low noise Simple design Fast transients | Low efficiency Significant power loss Heat |
| BUCK | Higher input to lower output | High efficiency Low heat | Requires ex. components Complex layout |
| BOOST | Lower input to Higher output | Efficient Wide input range | Higher output ripple Potential instability |
| BUCK-BOOST | Step Up or Step Down | Efficient Wide input range | Higher output ripple Potential instability |
| FLYBACK | Stepping up/down using transformer | Provides isolation Cost-effective for LP | Higher ripple Lower efficiency |
| SEPIC | Single-Ended PRI Inductor Converter Step-up/down with inductor | No polarity inversion Continuous output | More complex Requires multiple L/C |
| CHARGE PUMP | Uses capacitors for conversion | Simple No inductor needed | Low current capability Limited efficiency |

| Known Problem | Reason | Mitigation |
|------------------------------------|--|---|
| Switching Losses | Reduces efficiency in high frequency | Use MOSFETs with low RDS-on FET Optimize switching frequency |
| Conduction Losses | Heat dissipation in resistive elements | Use thick traces Low ESR components |
| Inductor/Transformer Losses | Core losses at high frequencies | Use high-efficiency ferrite cores |
| Ripple & Noise | Affects system performance | Use proper filtering |

Tips and Know How's

- **Component Selection:** Choose low ESR capacitors, high-efficiency inductors, and low RDS-on MOSFETs
- **Thermal Management:** Ensure proper heatsinking and airflow for heat dissipation in high-power designs.
- **Layout Considerations:** Keep high-current traces short and thick, minimize loop areas, use ground planes
- **Power Sequencing:** Design startup sequence where needed (e.g. FPGA or complex chipset)
- **EMI & Noise Control:** Place bulk capacitors near power inputs, use snubbers or FB where necessary

Efficiency

Efficiency is calculated as:

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} \times 100\%$$

P_{out} = Output Power (Watts)

P_{in} = Input Power (Watts)

Example:

A buck converter takes 12V input at 2A and converts it to 5V output at 4A.

$$P_{\text{in}} = 12V \times 2A = 24W$$

$$P_{\text{out}} = 5V \times 4A = 20W$$

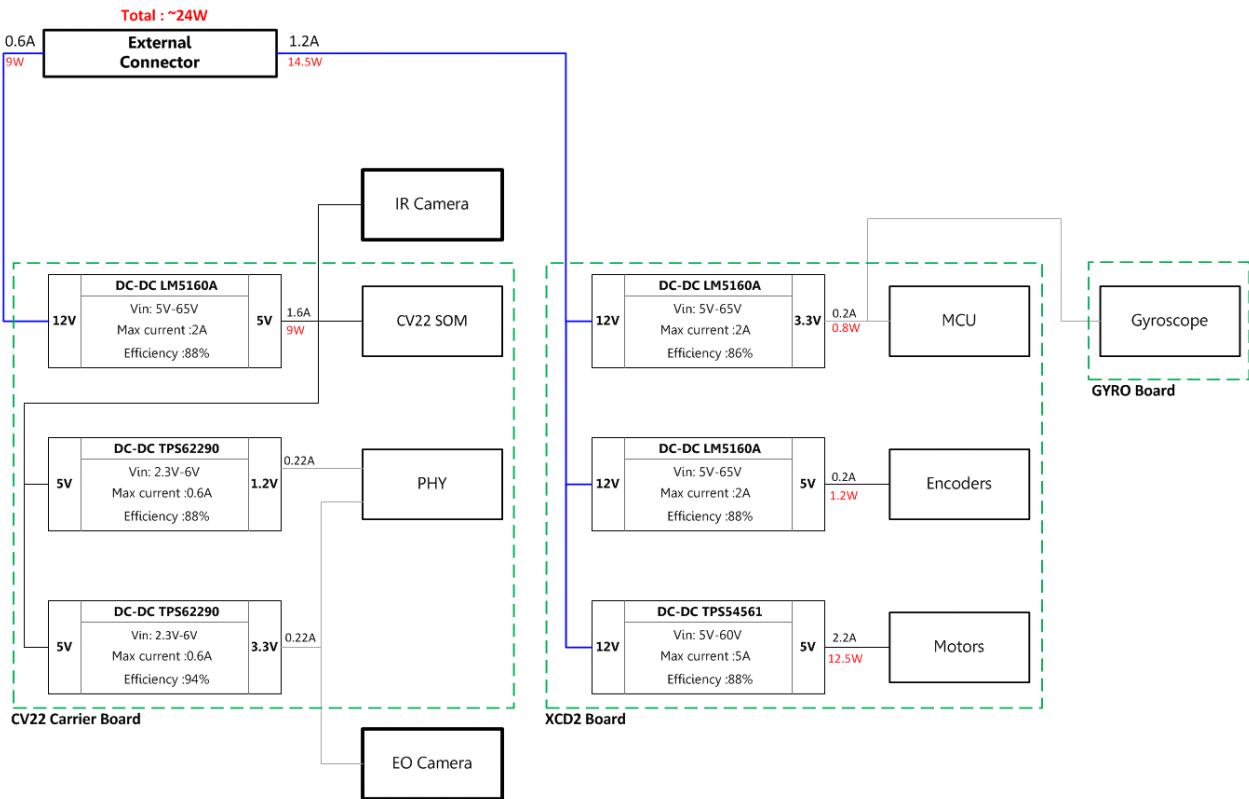
$$\eta = \frac{20}{24} \times 100 = 83.3\%$$

Common Mistakes

- **Using LDOs for large voltage drops** – Use Switching Regulators Instead
- **Long high-current traces** - Use wider traces or dedicated power planes
- **Placing decoupling caps too far from ICs** - Place capacitors as close to pins as possible
- **Ignoring thermal vias on power components** - Add thermal vias under power ICs
- **Not considering inrush current** - Use soft-start circuits or inrush limiters

Power Tree

See the Following Example of Creating Power tree and keeping all data on the diagram:



Each Power Supply block should contain:

- 1) Supply Manufacturer Name
- 2) Input Voltage
- 3) Input Range
- 4) Output Voltage
- 5) Max Output current
- 6) Efficiency

Recommendations for clarity:

- 1) Segregate each board (see green dotted line)
- 2) Add Power values where it matters (in red line)
- 3) Each Load in its own block
- 4) Mark main routes (like the blue lines)

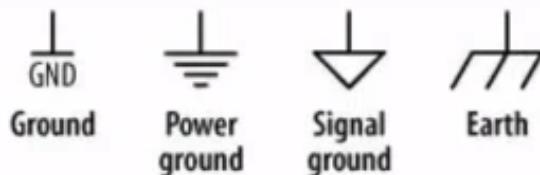
Ground

What is Ground?

- Not always 0V — ground = reference point, not absolute voltage.
- It can be analog, digital, chassis, earth, or even floating depending on context.
- Purpose: Return path for current, noise shielding, safety, EMI control.

Grounding Types:

- Power Ground:** Return path for power circuits. May carry high current = noise source.
- Analog Ground (AGND):** Clean return path for sensitive analog signals (op-amps, ADCs).
- Digital Ground (DGND):** Noisy path from LOGIC circuits and switching devices.
- Chassis Ground:** Connected to enclosure, used for shielding & ESD path.
- Earth Ground:** Physical ground (rod in earth), for safety in AC/mains systems.



Ground Plane

- Solid Ground Plane:** Ideal. Continuous copper area, low impedance, uniform return path.
- Split Ground Planes:** Used to isolate analog and digital noise.
Must be done right — no signal trace should cross the split, or return current takes wild paths
- Stitched Grounds:** Use ground vias/fences/stitching caps between zones (AGND ↔ DGND) for controlled return paths.
- Star Grounding:** All grounds converge at one central point. Great for analog audio/power, but rare in dense PCBs.
- Ground Flooding:** Pour copper everywhere, stitch to GND — improves EMI, reduces impedance, lowers voltage drop.

Standards and Compliance

- IPC-2221:** Generic PCB design guide (stackups, grounding, spacing).
- IEC 61000-4-x:** EMC immunity standards (ESD, EFT, Surge).
- MIL-STD-464, MIL-STD-461:** Military EMI/grounding specs.
- UL/CE/FCC:** all have grounding clauses for safety and EMI.

Practical Techniques

Return Path Awareness

- The Current always takes lowest impedance path, not shortest distance.
- High-speed signals create loop areas → EMI sources.
- Always route return-path below the signal trace (via solid GND plane).
- No ground breaks under differential or fast digital lines.

Faraday Cage and Shielding:

- Faraday Cage = enclosure tied to chassis/earth GND, blocks external fields.
- Works best when 360° shielded and grounded at single point.
- Cables must be shielded and tied to GND at one end (or both if differential).

ESD and Safety Grounding

- Protective Earth (PE): Mandatory in AC designs.
- Connect all metal cases/panels to PE.
- Use TVS diodes, MOVs, gas discharge tubes on GND entry points for protection.
- Grounded mats, wrist straps for ESD-safe assembly zones.

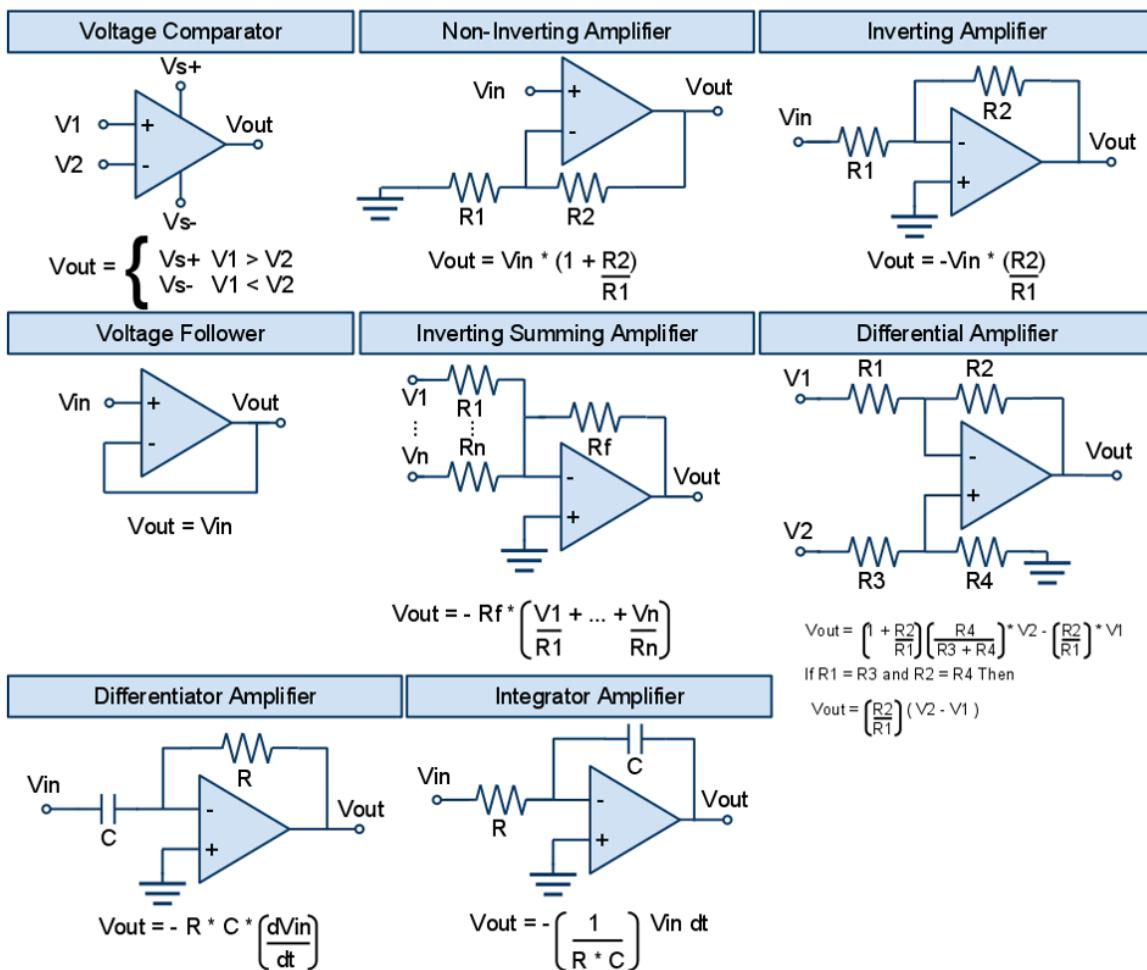
Grounding Know-Hows People Overlook:

- GND vias should be abundant and close to signal vias.
- Capacitive decoupling to GND doesn't help if GND return path sucks.
- Don't put noisy circuits over sensitive GND areas (e.g., high current switching over analog return).
- Isolated ground planes for high-voltage or isolated sections (use optos, transformers).
- High-current power GND return should be separated from signal GND near source.
- Don't let differential pair return currents split across multiple GND paths.

Operational Amplifiers

OPAMPS Types

- Comparator** – good for implementing thresholds
- Non-Inverting Amplifier** – When phase must remain the same
- Inverting Amplifier** – Very common, Inverting the signal and amplifying the voltage
- Voltage Follower (Buffer)** – Used for Impedance matching, Signal Isolation (no gain)
- Summing Amplifier** – Used for Control systems (PID), Audio Mixing, Modulation
- Differential Amplifier** – Common for signal integrity or Current Sensors
- Differentiator** – Edge Detection, Noise Filter
- Integrator** – Mainly used for Filters and Oscillators



OPAMP Characteristics

- **High Input Impedance:** Low current flows into the input terminals
- **Low Output Impedance:** Can drive loads without resistance
- **High Gain:** Amplifies small differences in input voltages
- **Low Offset Voltage:** Low inherent voltage difference between inputs without a signal
- **High Bandwidth:** Capable of amplifying signals across a wide range of frequencies
- **Low Noise:** Low unwanted electrical noise

Important Parameters

Gain-Bandwidth Product (GBP)

Defines the relationship between gain and bandwidth.

Op-amp with a high GBP can handle higher frequencies at lower gains.

Slew Rate

The rate at which the output can change.

Critical for high-speed applications like fast signal processing.

Offset Voltage

A small voltage difference that appears even when both inputs are at the same potential.

It should ideally be zero.

Common-Mode Rejection Ratio (CMRR)

The ability of an op-amp to reject common-mode signals (signals that are the same on both inputs).

In simple terms, CMRR tells you how well the op-amp ignores noise that affects both inputs equally.

Supply Range

Voltage supply that the OPAMP can handle. Usually symmetrical (e.g. $\pm 15V$)

The term "*Rail-to-Rail*" defines the ability to deliver output voltages as close as possible to supply.

Recommendations:

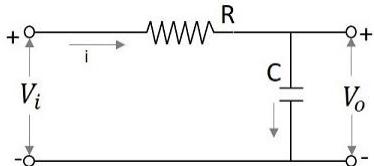
- 1) Stabilizing Feedback - Use negative feedback to maintain stability and control the gain
- 2) Saturation Avoidance - Ensure the input is within the range to prevent output saturation
- 3) Impedance Matching – Use buffers when impedance matching is critical
- 4) Bandwidth Consideration - Check the BW, higher gain typically reduces bandwidth
- 5) When designing an amplifier use Simulations such as LT-SPICE before implementation

Filters

Analog Filter Types

Low-Pass Filter (LPF)

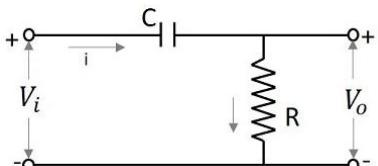
- Description: Allows low frequencies to pass while attenuating higher frequencies.
- Application: Removing high-frequency noise from audio signals or power supplies.



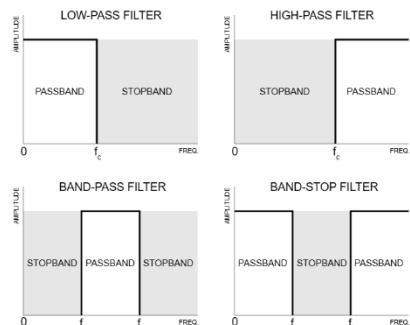
$$f_c = \frac{1}{2\pi RC}$$

High-Pass Filter (HPF)

- Description: Allows high frequencies to pass while blocking lower frequencies.
- Application: Removing low-frequency noise or DC offset in signals.

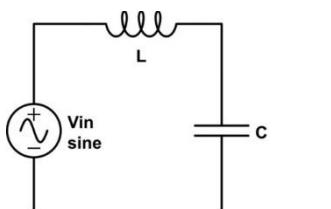


$$f_c = \frac{1}{2\pi RC}$$



Band-Pass Filter (BPF)

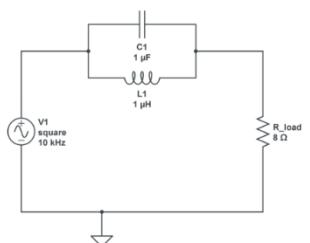
- Description: Allows frequencies within a specific range to pass
- Application: Isolating a specific frequency range



$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad Q = \frac{R}{\sqrt{L/C}} \quad \text{BW} = \frac{f_0}{Q}$$

Band-Stop Filter (BSF)

- Description: Blocks a specific range of frequencies, allowing frequencies outside this range to pass.
- Application: Removing unwanted frequencies, such as 50/60 Hz power-line hum.



$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad Q = \frac{R}{\sqrt{L/C}} \quad \text{BW} = \frac{f_0}{Q}$$

Filter Building Blocks

Resistors (R)

- Resistors are commonly used in RC filters.
- They limit current and control time constants.
- In **passive filters**, resistors are key in defining the filter's behavior.

Capacitors (C)

- Capacitors store energy and block DC signals.
- Capacitors determine the frequency response and control the phase.

Inductors (L)

- Inductors resist changes in current and store energy in a magnetic field.
- In LC circuits, inductors help define the frequency response.
- Inductors are used in band-pass, band-stop, and resonant filters.

Operational Amplifiers (Op-Amps)

- OPAMPS are used in **active filters** to provide gain and improve performance.
- They help achieve sharp cutoffs, low power loss, and high precision in filters.
- Op-amps are common in high-pass, low-pass, and active band-pass filters.

Filter Characteristics

Flatness

The filter should ideally have a flat response in the passband, meaning that all frequencies pass through without attenuation.

Steepness of Cutoff

The steeper the cutoff slope, the sharper the filter. Steeper slopes are desirable in applications that need clear separation of frequency bands.

Phase Response

Filters also affect the phase of signals, particularly in analog filters. The phase shift at various frequencies must be considered in applications like audio or communications.

Group Delay

Group delay refers to the time delay experienced by different frequency components of a signal. A good filter should have constant group delay across the passband to avoid distortion.

Communication

Communication Types

Table of common communication:

| Protocol | Max Rate | Wiring | Type | Problems |
|-----------------|----------------------------------|--------------------------------|---|--|
| 1-Wire | 142 kbps | 2 (CAN H, CAN L) | Asynchronous Serial Daisy Chain | Very limited BW Not common PU Res. dependency |
| UART | 1 Mbps | 2 (TX, RX) | Asynchronous Serial Point to Point | Limited BW Distance issues |
| I2C | 3.4 Mbps | 2 (SCL, SDA) | Synchronous Serial "Star" – Multi Slave | Limited BW Distance issues PU Res. dependency |
| SPI | 50 Mbps | 4 (MISO, MOSI, SCLK, CS) | Synchronous Serial "Star" – Multi Slaves | Limited devices Extra CS for each slave |
| Ethernet | 100 Gbps | 4 (TX, RX, GND) | AC Coupled Diff. BUS | Requires infrastructure costlier setup |
| MIPI | 16 Gbps | 2/4 Diff (n x DATA + CLOCK) * | AC Coupled Diff. Point to Point | Limited range complex wiring setup |
| HDMI | 6 GPbs | 4 Diff (TMDS DATA + CLOCK) * | AC Coupled Diff. Point to Point | Point-to-Point (No Multi) Signal Integrity and Loss |
| USB | 10 Gbps | 5 (VBUS, GND, D+, D-, OTG) | AC Coupled Diff. BUS | Distance issues |
| PCIe | 32 Gbps (3 rd Gen) | N x Diff (DATA) N: 1,4,8,16 | AC Coupled Diff. Point to Point | Requires termination Fairly slow |

*HDMI and MIPI have more signals running (e.g. CEC for HDMI or I2C control for MIPI)

Communication Topologies

- **Open drain** saves power, avoids contention in multi-device buses, PU needed (e.g. I2C)
- **Push-pull** faster rise/fall times, better for high-speed signals (e.g. SPI)
- **Differential Pair** must-have for high-speed or noisy environments (MIPI/USB/HDMI)
- **Tri-state** enables multiple devices on shared lines (e.g., SPI MISO).
- **AC coupling** (serial cap) blocks DC and increases integrity (e.g. HDMI/USB/ETH)

Communication Requiring Impedance Matching

- RF Coaxial (Analog/Digital): **50Ω or 75Ω**
- Ethernet (Twisted Pair): **100Ω**
- USB (1.1 / 2.0 / 3.0): **90Ω differential**
- HDMI: **100Ω differential**
- DisplayPort: **100Ω differential**
- LVDS (Low Voltage Differential Signaling): **100Ω differential**
- CAN Bus: **120Ω**
- RS-485 / RS-422: **120Ω**
- PCI Express (PCIe): **85Ω differential**
- SATA: **100Ω differential**
- Thunderbolt: **85Ω or 100Ω differential**
- SPI (over long distances): **~50Ω**
- I²C (over long distances): **~100Ω differential**
- SerDes Interfaces: **100Ω differential**

Terms and Definitions:

| Topology Point-to-point Bus Ring Star Mesh | Security Encryption Secure handshake | Power Consumption LP communication Sleep/Wake modes Energy harvesting PoE | Bus Arbitration Shared buses Address methods Priority access timing |
|--|--|--|---|
| Power Integrity Decoupling PDN noise coupling | Timing & Latency Propagation delay Setup/hold time Data throughput Latency tradeoff | Physical Layer Cable types Trace impedance Stack up PCB layout | Buffering & Drive Fan-out Bus drivers transceivers repeaters |
| Voltage Levels CMOS/LVDS/CML Differential swing | Error Detection CRC, Parity bits Hamming code FEC | Synchronization Clock/Data recovery Skew & delay PLLs, DLLs | Data Encoding NRZ 8b/10b PAM/PSK AM/FM/QAM |
| Transmission Modes Single-ended Differential Serial vs Parallel Half/ Full duplex | Noise & Interference EMI/EMC Differential noise Shielding tech. Filtering | Signal Integrity Crosstalk Reflections Ground bounce Jitter | Bandwidth & Data Rate BW limitations Nyquist theorem Shannon limit Over/Under sample |

Signal Integrity

Differential Pair Design Rules

| Parameter | Target Value / Rule |
|--------------------------|--|
| Intra-pair Length Match | ≤ 5 mils (preferably <2 mils for >5 Gbps) |
| Inter-pair Length Match | $\leq 25-50$ mils (depends on protocol/speed) |
| Impedance (Z_{diff}) | 90Ω or $100\Omega \pm 10\%$ |
| Spacing (S) | $S \approx W$ (Trace Width) for 100Ω pairs |
| Routing Style | Route pairs together, same length, same path |

Impedance Guidelines

| Structure | Target Z_0 | Notes |
|------------|--------------|---|
| Microstrip | 50Ω | Top layer, air/dielectric above |
| Strip Line | 50Ω | Between two GND planes, better shielding |
| Diff Pair | 100Ω | Two 50Ω traces spaced for differential |

Layer Stack Up Best Practice

L1 (Top) Low-speed signals, reference GND below

L2 Solid GND plane

L3 High-speed SERDES signals

L4 Power plane

L5 More SERDES or clock signals

L6 GND plane

L7/L8 Mixed/Low-speed or GND

*Route high-speed lanes between **GND layers**

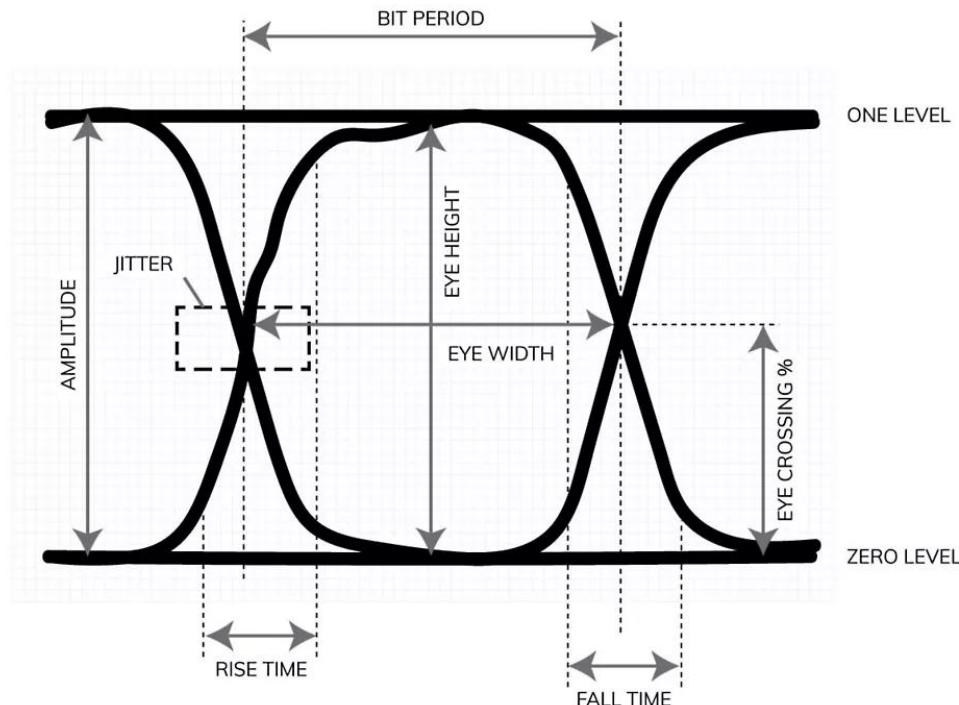
Via & Return Path Design

| Guideline | Description |
|----------------------------------|--|
| Minimize signal vias | Each via adds parasitic inductance/stubs |
| Use ground stitching vias | Next to diff pairs to maintain return path |
| Avoid plane splits under routing | Causes impedance discontinuities + reflections |
| Back drill long unused via stubs | Especially at >6Gbps |

General Routing Tips:

- 1) Keep diff pairs close & parallel
- 2) Avoid sharp angles (use 45° or curves)
- 3) Avoid length tuning meanders unless needed — only on one side
- 4) Avoid changing layers — if unavoidable, match via stubs
- 5) Place AC/DC terminations close to RX/driver
- 6) Use ground shielding lanes for isolation

Eye Diagram:



Terminology & Design Tips

Impedance Matching

Goal: Prevent signal reflections.

Sources of mismatch: Transmission line impedance \neq source or load impedance.

Fixes: Use proper termination resistors or adjust the trace width.

Crosstalk

Goal: Minimize interference between adjacent traces.

Near-end Crosstalk (NEXT): Interference close to the source.

Far-end Crosstalk (FEXT): Interference at the receiving end.

Fixes: Increase trace spacing, use ground planes, or shield sensitive traces.

Jitter

Goal: Maintain timing accuracy.

Sources: Clock skew, power noise, and thermal fluctuations.

Fixes: Use proper clock distribution, reduce noise, and maintain consistent voltage levels.

Eye Diagrams

Goal: Visualize signal quality over time.

Opening: Wide eye opening = good signal quality

Closeness: A narrowed eye opening = signal degradation

Fixes: Improve PCB design, reduce reflections, optimize clocking.

Signal Reflection

Goal: Avoid bounced signals that interfere with the incoming signal.

Sources: Impedance mismatch between transmission line and load.

Fixes: Use proper termination or controlled impedance traces.

PCB Layout

Goal: Optimize routing to maintain signal integrity.

Key Considerations:

- Trace width and length.
- Minimize via use to reduce inductance.
- Keep ground planes continuous.

Fixes: Route high-speed signals with controlled impedance, minimize trace length.

Terminology & Design Tips (continue)

Power Delivery Noise

Goal: Ensure clean power to components.

Causes: Switching noise, power supply ripple.

Fixes: Use decoupling capacitors, proper power plane layout, and low-pass filters.

Differential Signaling

Goal: Improve noise immunity.

What it is: Signals are transmitted as a pair of complementary signals (positive and negative).

Benefits: Reduces susceptibility to common-mode noise.

Examples: LVDS, RS-485.

Skew

Goal: Keep the signal in sync.

What it is: Difference in arrival times of signals at different points.

Fixes: Properly match the lengths of signal traces and adjust timing.

Signal-to-Noise Ratio (SNR)

Goal: Maximize the quality of the signal.

What it is: The ratio of the signal power to noise power.

Fixes: Increase signal strength, reduce noise sources.

Bandwidth Limitation

Goal: Ensure signal fidelity over long distances.

What it is: Limits on how much data can be transmitted without distortion.

Fixes: Use higher-quality traces, reduce distance, and adjust data rates.

Termination

Goal: Prevent reflections and signal degradation.

Series Termination: Placed near the driver.

Parallel Termination: Placed at the receiver end.

Fixes: Use the right termination technique for your application.

Voltage Standing Wave Ratio (VSWR)

Goal: Measure how well the transmission line is matched to the load.

What it tells you: A high VSWR indicates poor matching and signal reflection.

Fixes: Use impedance matching techniques to improve.

SERDES

What is SERDES?

SERDES is a technology used to convert parallel data into serial data (serialization) for transmission and then convert it back into parallel data (deserialization) on the receiving end.

The Purpose is to Optimize high-speed communication over a single lane, reducing pin count and power consumption.

SERDES Data Rates:

- 1) **Low-Speed**: Around 1-3 Gbps (USB 2.0, SATA I).
- 2) **Mid-Speed**: Around 6-12 Gbps (PCIe 3.0, SATA III).
- 3) **High-Speed**: 25-50 Gbps and beyond (PCIe 5.0/6.0, 100G Ethernet, DisplayPort 2.0).

HW Components:

- 1) **Serializer** - parallel into serial. Takes data bits and combines them into a single stream
- 2) **Deserializer** - serial into parallel. Reconstructs the serialized data into parallel format
- 3) **Clocking** - SERDES systems use a clock (often differential) to sync data
- 4) **Transceivers** - Combine both Serializer and Deserializer in a single unit.

SW/FW Components:

- 1) **FPGAs/ASICs** - Used to implement SERDES systems in hardware
- 2) **Driver Software** - Manages SERDES chip initialization, error correction, and data flow.
- 3) **Protocol Handling** - Software protocols interface with SERDES to ensure proper trans.

Applications:

- 1) **Data Centers**: Connecting high-speed servers and storage devices
- 2) **Networking**: Fiber optics, Ethernet, and 5G backhaul communications.
- 3) **Consumer Electronics**: Display interfaces (e.g., HDMI) for high-bandwidth video/audio.
- 4) **Automotive**: For communication between different modules in cars
- 5) **Telecommunications**: For high-speed transmission in optical networks.

Key SERDES Vendors:

- 1) **Xilinx**: Offers SERDES blocks in their FPGAs for high-speed communication.
- 2) **Intel (Altera)**: Provides SERDES solutions for networking, data centers
- 3) **Broadcom**: Known for high-performance networking and storage chips using SERDES.
- 4) **Texas Instruments**: Offers integrated SERDES solutions in all fields (e.g. industrial)

Protocols using SERDES

PCI Express (PCIe): Used in computers between peripherals like GPUs, storage devices, etc.

Gigabit Ethernet: Used in networking for data transmission at gigabit speeds.

Serial ATA (SATA): Used for connecting storage devices like SSDs and HDDs.

USB 3.x: Used for communication between USB devices.

DisplayPort / HDMI: Used for video/audio transmission in consumer electronics

SAS (Serial Attached SCSI): Used data transfer between servers and storage devices

SERDES vs Parallel Communication

Parallel:

Pros: High-speed, multiple bits transferred at once.

Cons: Requires many pins, higher power consumption, and more complex routing.

SERDES:

Pros: Reduced pin count, lower power consumption, and suitable for long-distance

Cons: Serial transmission requires clock synchronization.

Problems and issues:

- 1) **Signal Integrity Issues**: High-speed signals are susceptible to noise, reflections
- 2) **Clock Skew**: Discrepancies in the clock signals can lead to synchronization problems.
- 3) **Electromagnetic Interference (EMI)**: High-speed signals can generate EMI
- 4) **Data Alignment**: Ensuring that data is correctly aligned after deserialization
- 5) **Power Consumption**: SERDES can be power-hungry, especially in high-speed systems.

Design Challenges:

- 1) **PCB Routing**: High-speed signals need to be routed carefully to avoid signal degradation.
- 2) **Power Delivery**: Ensuring stable power delivery for high-speed circuits.
- 3) **Thermal Management**: High-speed SERDES circuits generate significant heat.
- 4) **Clock Generation and Distribution**: A clean clock signal is critical for data integrity

IMUs

What is MEMS IMU?

Definition: MEMS based Inertial Measurement Unit = a sensor system that measures:

- Acceleration (Linear) → **Accelerometer**
- Angular Velocity (Rotation) → **Gyroscope**
- Magnetic Field → **Magnetometer**

Purpose: Estimate orientation, position, and movement — without relying on external references

Core Sensors Inside:

| Sensor | Measures | Unit | Axis |
|---------------|--------------------------|-----------------------|-------|
| Accelerometer | Linear acceleration | m/s ² or g | X Y Z |
| Gyroscope | Angular velocity | °/s or rad/s | X Y Z |
| Magnetometer | Magnetic field (heading) | µT (microtesla) | X Y Z |

IMU Types

| Type | Components | Typical Use |
|---------|-----------------------------------|--------------------------------------|
| 3-DOF | Accel only / Gyro only | Basic tilt/motion sensing |
| 6-DOF | Accel + Gyro | Orientation, attitude estimation |
| 9-DOF | Accel + Gyro + Magnetometer | Full orientation (yaw, pitch, roll) |
| 10-DOF+ | 9-DOF + Barometer/Pressure sensor | Advanced applications (e.g., drones) |

Most common Applications

Drones
 Mobile phones
 Robotics
 VR/AR headsets
 Automotive (ABS, ESC)
 Navigation systems (INS)
 Gait analysis / Wearables
 Gaming controllers
 Cameras (image stabilization)

IMU Design

Hardware Interface:

- I2C / SPI / UART → Digital data output (slave)
- Voltage Levels: 3.3V or 1.8V logic
- Sampling Rates: Up to 32kHz
- Resolution: 8-bit to 20-bit depending on model
- Low current devices
- Hardware Interrupts (depends on IMUs)

Software interface:

- Sensor Fusion Algorithms: Combine multiple sensor outputs to reduce drift & noise.
- IMU to Orientation Estimation: Gives Roll, Pitch, Yaw
- Dead Reckoning: Estimating position over time using IMU
- Rotation Matrix
- Filtering Output Data
- Supporting Internal Features (Filters, Offsets, Temperature etc.)

Features & Data (depends on IMU)

- Raw data format: 2's complement, 8-bit or 16-bit
- Interrupt pins for motion detection, FIFO full, orientation change
- Timestamping is often needed to match sensor data precisely to system time
- Sensor Bandwidth consideration
- Freefall detection
- Resolution selection (e.g. 1g/2g etc.)
- Motion tracker

Advanced Use Cases

- **IMU + GPS** → Sensor fusion for outdoor navigation
- **IMU + Visual SLAM** → Inside-out tracking in robotics/AR
- **IMU + Machine Learning** → Activity recognition, gesture control
- **IMU + Gimbal Systems** → Vibration rejection and motion tracking

IMU Common Problems

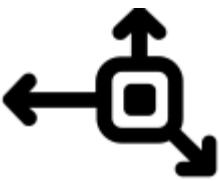
| Issue | Cause | Effect |
|-----------------------|---|---------------------------------|
| Drift | Gyro integration error over time | Wrong orientation |
| Bias/Offset | Sensor zero-point error | Wrong data even at rest |
| Noise | Electrical/thermal fluctuations | Jittery signal |
| Vibration Sensitivity | External mechanical noise | Corrupted motion data |
| Magnetic Interference | Nearby current loops, motors, metal objects | Wrong heading from magnetometer |
| Temperature Drift | Sensor readings change with temperature | Inconsistent measurements |
| AXIS Crosstalk | IMU is not mounted properly | X AXIS parts are shown |

Validation tests for IMU:

- 1) Bias Test
- 2) Drift Test
- 3) Step Response Test
- 4) Magnetic Reliability Test
- 5) Repeatability Test
- 6) Thermal Drift Test
- 7) Cross-Axis Coupling Test
- 8) Vibration Robustness Test
- 9) Power-On Consistency Test

Real World Tips:

- 1) Always calibrate bias/offset on startup (and Production)
- 2) Mount the IMU close to Center of Gravity to reduce error
- 3) Use soft foam damping to reduce vibration
- 4) Avoid placing IMU near power lines/motors
- 5) Log raw data — fusion later can be improved offline
- 6) Mechanical PCB guidelines are critical in IMU boards
- 7) Use Internal Filters and features to get max accuracy



Product Development Stages

| STAGE | PURPOSE | DELIVERABLES | AVOID |
|-----------------|---|--|--|
| KICK OFF | Initial requirements Feasibility and Expectations Scope and high-level design | Project goals and requirements Initial feasibility study Preliminary timeline and budget Team allocation | Lack of clarity in requirements Poor feasibility assessment |
| PDR | Preliminary Design Review High-level architecture Feasibility validation Concepts VS Requirements | System architecture High-level block diagrams Initial risk assessment Interface definitions Preliminary BOM | Missing interfaces overlooking dependencies Undefined risks |
| CDR | Critical Design Review Finalized design before prototype Ensure all details are validated | Schematic and layout finalization Power and thermal analysis Firmware/software architecture Compliance check Updated BOM | Design errors caught late Regulatory compliance issues |
| BRING UP | First prototype tested Focus on debugging and validating | First PCB assembly Power-up Signal integrity Firmware boot Debug and rework plan | PCB re-spins Unexpected thermal issues EMI issues |
| V&V | Verification & Validation Ensures design meets SPEC Verification: Testing against SPEC Validation: Functionality Testing | Functional testing Environmental and stress testing Compliance and certification Reliability testing | Failing compliance tests Design flaws |
| NPI | New Product Introduction Transition from R&D to production Ensuring manufacturing | Manufacturing test plans Yield and production QC Cost optimization Supply chain readiness | Production yield issues Component shortages |
| PROD | Full-scale manufacturing Long-term product maintenance | Production ramp-up Field support and bug fixes Cost and quality improvements | Supply chain disruptions Needed firmware support Needed HW support |

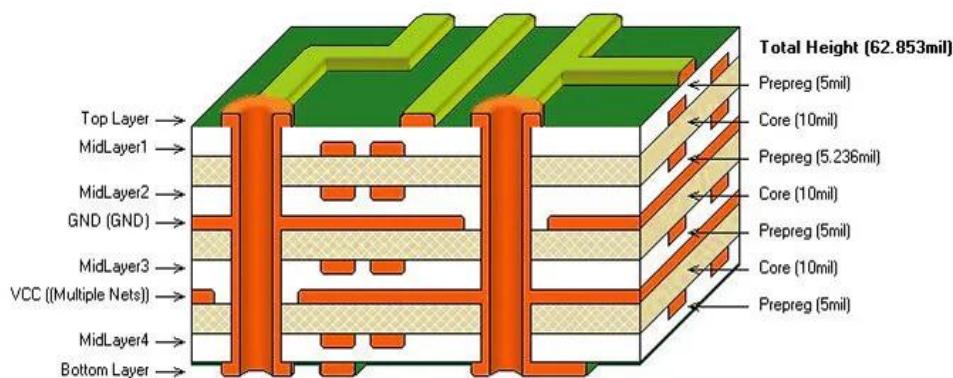
PCB

Printed Circuit Board Production Stages

| | |
|---------------------|--|
| SPECs | Layers, signals, current, mechanicals |
| Stack Up | Define copper thickness, dielectric, impedance control |
| DRC | Apply spacing, trace width, via rules |
| Routing | High-current paths, signals, diff pairs, impedance match |
| Grounding | Plan returns, pour strategy, stitching vias |
| Final Checks | ERC, DRC, netlist, mechanical fit |
| Production | Export Gerbers, drill files, pick & place, BOM |

| Thickness | Max current |
|-----------|-------------|
| ~0.7 mil | ~0.5A |
| ~1.4 mil | ~1A |
| ~2.8 mil | ~2A |

| Via Type | Description | Notes |
|-------------------|------------------|--------------------------|
| Thru-Hole | Standard drill | Cheapest |
| Blind Via | Surface to inner | Cost↑ |
| Buried Via | Inner to inner | Complex |
| Micro-via | Laser drilled | Used in BGA, HDI |
| Via-in-pad | Via inside pad | Needs filled/plugged via |



Design Consideration

Design for Testability:

- Test Points where it matters
- Route Rail lines (voltage) to ADC or MCU for later probing
- Design Current Sensors in main traces
- Create back doors to components or devices on board that you want direct access during debug
- Use indications (LEDs, GPIOs etc.)
- Use JTAG for debug in MCU – Make the connection accessible (not just for programming)
- USB to PC is always recommended in multi-discipline devices
- Leave Spare pins and lines for example GPIOs from MCU ending with via
- When using UART or USB, make a cross wire (TX/RX) option via NC resistors

High Speed Consideration:

| Factor | Tip |
|-----------------------|--------------------------------|
| Trace Length Matching | <50ps skew for diff pairs |
| Avoid Stubs | Route clean, no dead ends |
| Min Via Count | Each via = discontinuity |
| Short Return Path | Return must follow signal path |
| Guard Traces | Optional for noise shielding |

Real World Tips:

- 1) Always route high current paths **short & thick**
- 2) Differential signals should have **tight coupling** (closer spacing = better)
- 3) Clock, USB, CAN, Ethernet → impedance-controlled traces
- 4) Decoupling caps **close as hell** to IC pins
- 5) Avoid **90° angles** – use **2x45°** or arcs (RF boards especially)
- 6) Keep analog/digital **separate routing paths**
- 7) Place test points early
- 8) Add **fiducials** for pick & place
- 9) Thermal reliefs in copper pours (important for soldering)
- 10) Document **stack up & impedance targets in Fab notes**

Deliverables to Manufacturer:

- 1) Gerber (RS-274X)
- 2) Drill Files (Excelon)
- 3) Assembly Drawing
- 4) Component Placement
- 5) BOM
- 6) Pick & Place (XY)
- 7) Stack Up Info

Assembly

Assembly Considerations

Key Considerations for Footprints:

- 1) **Component Manufacturer Specs:** Always refer to the manufacturer's Datasheet for accurate footprint dimensions. Different manufacturers might have slightly different specs for the same component type.
- 2) **Standardization:** Use standard libraries for widely used components (like resistors, capacitors, ICs) to avoid errors.
- 3) **Pad Design:** Ensure the pads are designed for the right soldering process (e.g., wave soldering, hand soldering, or reflow soldering). This includes the correct pad size and spacing between them.
- 4) **Clearance:** Make sure there's enough clearance around each component to allow for soldering tools and avoid thermal damage during reflow.

Design Tips:

- Use IPC-2221 standards for footprint creation.
- If the footprint is too small, it can result in poor solder joints or even short circuits.
- If it's too large, it can cause alignment issues during assembly.

Pick And Place

Pick-and-place machines are used for the automatic placement of components onto a PCB. These machines pick up components (usually SMDs) and place them at the correct location on the PCB based on data from the assembly files.

Key Points to Ensure Efficient Pick-and-Place:

- 1) **Accurate Placement:** The placement data for each component (often in the form of centroid files) must match the footprint precisely.
- 2) **Component Orientation:** Proper orientation information should be provided in the placement files. For example, ICs and polarized components (like capacitors and diodes) need specific orientation information.
- 3) **No Misalignment:** Misalignment can lead to non-functioning circuits or failed solder joints. Ensuring the machine has accurate data will avoid this.
- 4) **Component Size:** Ensure the component size is compatible with the machine's pickup heads. If the components are too large or too small, this can lead to misplacement or even damage to the component.

Connector common mistakes

Connectors often present unique challenges during assembly due to their size, orientation, and tight tolerances.

Common Connector Assembly Issues:

- 1) **Wrong Orientation:** Connectors, particularly polarized connectors, need to be placed with correct orientation. If reversed, it could lead to connection issues or damage to the connector or other parts of the system.
- 2) **Misalignment:** Connectors have very precise pin-to-hole alignment requirements. Misalignment during the placement can cause poor solder joints, leading to failure in the connection.
- 3) **Different Pin Types:** Some connectors have through-hole pins, while others are surface-mount. Ensure that the correct type is selected for the corresponding assembly method.
- 4) **Over- or Under-Board Protrusion:** Check that connectors do not protrude too far from the PCB (they may not fit within the enclosure) or too little (they may not make a reliable connection).

Mitigation:

- Choose connectors including indicators or marks to show orientation (like, dot, or triangle).
- Use custom fixtures to guide connector placement during assembly to ensure proper orientation.

Conformal Coating

Conformal coating is a protective layer applied over the PCB to shield it from environmental factors like moisture, dust, and chemicals. It's especially important in harsh environments or when the PCB will be exposed to extreme conditions.

Conformal Coating Options:

- 1) Acrylic Coating: Provides a good balance of flexibility and moisture protection.
- 2) Silicone Coating: Provides high temperature stability and vibration resistance.
- 3) Polyurethane Coating: Offers better chemical resistance but is more rigid.
- 4) Epoxy Coating: Gives the best protection but is quite rigid and difficult to remove.

Key Considerations for Conformal Coating:

- Component Accessibility: Ensure that sensitive components like connectors, buttons, or test points are masked off before applying the coating.
- Thickness Control: Too thick a coating can insulate signals or interfere with component connections.
- Coating Method: Common methods include spray, dip, or brush coating. Each has its advantages depending on the type of board and coating used.

Footprint Types

TQFP: flat IC with leads on 4 sides, fine pitch (0.4–0.8mm), used in MCUs and logic ICs.

QFN: no-lead square package with pads underneath, compact, good thermal performance, 0.4–0.65mm pitch.

BGA: ball grid under the chip, high pin count (100+), excellent for high-speed ICs, needs X-ray inspection.

LGA: flat pads instead of balls (like BGA), ideal for sockets or direct board contact, used in RF modules and CPUs.

SOIC: dual-inline gull-wing leads, easy to solder, 1.27mm pitch, used in op-amps and logic chips.

SSOP/TSOP: smaller versions of SOIC with tighter pitch (0.5–0.65mm), used in EEPROMs and analog ICs.

DIP: through-hole dual-row pins, 2.54mm pitch, great for prototyping, used in older or hobbyist designs.

TO-220: power transistor package with large tab for heatsink, 3-pin, used for regulators and MOSFETs.

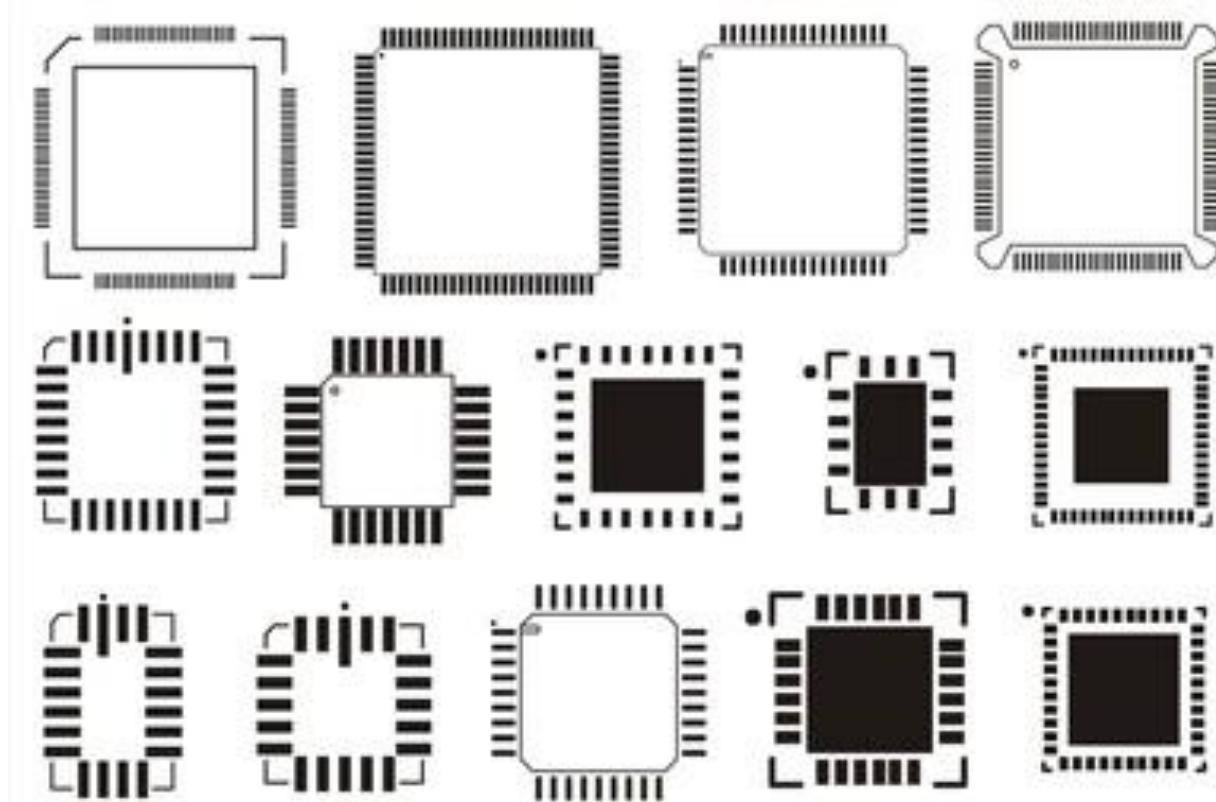
TO-92: small through-hole transistor package, 3-pin, used for BJTs and sensors.

SOT-23: small (2.9x1.3mm), common 3–6 pin SMT transistor/regulator package, easy to solder.

SOT-223: mid-sized (6.7x3.5mm), better thermal dissipation, 3–4 pin, often for LDOs and MOSFETs.

SOT-89: compact SMT power transistor, 3-pin, higher power than SOT-23, still hand-solderable.

DFN/SON: very compact no-lead SMT package (2x2mm to 5x5mm), pads on underside



Validation & Verification

Validation is a critical stage in development process. This stage must be considered in early stages of the product to make sure that the infrastructure needed is included (e.g. Design **Built in Test** Module with all required HW supporting it). Validation should be carried out against SPEC making sure that the product meets the requirements, and it works as intended.

Validation of all aspects

Schematic Validation

Cross-check part numbers, pinouts, power rails, polarities.

Verify decoupling caps near every IC, resistor values, net names.

Validate pull-ups/pull-downs, analog filtering, unused pins termination.

Check IC enable logic, reset circuit, power sequencing.

PCB DRC & ERC Validation

Run all Design Rule Checks: clearance, width, via aspect ratio, annular ring.

Check electrical rules: floating nets, unconnected pins, hidden labels.

Validate net continuity manually for critical paths (e.g. clocks, power, analog).

Review ground plane integrity, return path, split plane violations.

Check thermal reliefs, copper balancing, impedance mismatch.

Footprint Validation

Match every footprint pad spacing, outline, height, pin 1 marking.

Print 1:1 scale on paper, test real components.

Validate keep outs, fiducials, silkscreen markings, pin orientation.

Double-check polarized caps, LEDs, connectors, switch orientation.

Mechanical Validation

Check mounting holes, enclosure fit, connector clearance.

3D step model integration with mechanical CAD.

Confirm heatsink clearance, board warpage risks.

Verify penalization rules if needed.

Electrical Validation

Power ON test: check rail voltages, ripple, sequencing.

Load test: check regulator performance, heat dissipation.

Signal test: measure clocks, data buses, analog voltages.

Oscilloscope + multimeter sweep for sanity check.

Current consumption vs design estimate → early red flag for wrong logic or floating pins.

Validate the design in all aspects(continue)

Functional Validation

MCU boots? I/O works? Analog section behaves?
Validate firmware + hardware handshake, USB, SPI, UART, etc.
Validate all sensor inputs, signal conditioning, interface logic.
Check LEDs, buttons, relays, output drivers, etc.

Thermal Validation

Run thermal camera or IR scan after full load.
Validate heatsinks, airflow, junction temp vs spec.
Watch out for thermal coupling between hot and sensitive zones (e.g. analog next to MOSFETs).

EMI/ESD Validation

Inject ESD: simulate real-world finger zaps ($\pm 2\text{--}8\text{kV}$).
Check susceptibility to radiated or conducted noise.
Validate TVS, GND shielding, filtering caps.
Run in noisy environments (motor noise, USB plug/unplug, nearby WiFi devices).

Signal Integrity Validation

Scope the high-speed traces, clock edges, ringing, reflections.
Measure diff pair skew, impedance mismatch, crosstalk.
Validate signal eye diagram if relevant.
Run loopback tests, jitter tests, and simulate degraded cables.

Software/Firmware Validation

Test full code stack with all hardware peripherals.
Test firmware fail-safe, watchdog, power recovery.
Validate sleep modes, GPIO configurations, sensor comms.
Log edge cases → brownouts, timing drifts, startup behavior.

Corner Case Validation

Run board cold start at -20°C , hot run at $+70^\circ\text{C}$.
Test under-voltage, brownout, overload, overclocked SPI, broken cable scenarios.
Simulate partial shorts, remove connector mid-run, etc.

Assembly/Manufacturing Validation

Do a trial run: 1–5 pcs assembled manually or by pick & place.
Check component orientation, reverse polarity risk.
Validate DFM/DFT readiness: test pads, access for probes, test jigs.