Poster: Delay-Constrained Input-Queued Switch

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ABSTRACT

We study delay-constrained input-queued switches where each packet has a deadline that will expire if it is not delivered before its deadline. Such a new scenario is motivated by the proliferation of real-time applications in multimedia communication systems, tactile Internet, networked controlled systems, and cyber-physical systems. One fundamental problem centering around the performance metric of *timely throughput* is how to characterize the capacity region. In this work, for the frame-synchronized traffic pattern, we characterize the capacity region by a polynomial number of linear constraints.

CCS CONCEPTS

• **Networks** → **Bridges and switches**; **Packet scheduling**; • **Mathematics of computing** → *Combinatorial optimization*;

KEYWORDS

Input-Queued Switch, Delay-Constrained Traffic, Capacity Region

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1 INTRODUCTION

Switches, which interconnect multiple devices, are the core of communication networks. The input-queued switch using virtual output queueing is most widely used among all types of switches, which we call *input-queued switch* for the sake of convenience. Most existing works on input-queued switches consider *delay-unconstrained* traffic where packets can be kept in the virtual output queues forever. McKeown et al. in [6] characterized the capacity region for independent, identically distributed (i.i.d.) arrivals and further proved that the maximum-weight-matching scheduling policy is throughput-optimal in that it can support any feasible throughput requirements in the capacity region. Dai et al. in [2] extended these results to arbitrary delay-unconstrained arrivals.

However, nowadays with the proliferation of real-time applications, the communication networks need to support more and more *delay-constrained* traffic. Typical examples include multimedia communication systems such as real-time streaming and video conferencing, tactile Internet, networked controlled systems (NCSs) such as remote control of unmanned aerial vehicles (UAVs), and cyber-physical systems (CPSs) such as medical tele-operations, X-by-wire vehilces/avionics, factory automation, and robotic collaboration [3–5]. In such applications, each packet has a hard deadline: if it is not delivered before its deadline, its validity will expire and it will be removed from the system. In addition, throughput (which is termed timely throughput in the delay-constrained scenario [3, 4]) is also important to such applications.

Since switches are the core of communication networks, how to support delay-constrained traffic in switches becomes critical. There are some existing works that investigate how to design real-time input-queued switch. Chang et al. in [1] proposed two scheduling policies under which the delivery delay of packets is upper bounded by a finite value. Kang et al. in [5] aimed to deliver *all* packets and minimize the maximum delivery delay among all packets. Thus, they do not directly guarantee the delivery of delay-constrained traffics where hard deadlines are predetermined by the applications; and they do not allow any packet loss. Instead, in this work, we consider how to deliver delay-constrained traffic and focus on the performance metric of timely throughput. One fundamental problem for delay-constrained input-queued switches is how to characterize the capacity region in terms of timely throughput of all input-output pairs. The capacity region serves as the foundation to evaluate the performance of any scheduling policy. We prove that for the *frame-synchronized traffic pattern* [3, 4], we can characterize the capacity region with only a polynomial number of linear constraints (see (2)).

2 MODEL, PROBLEM, AND RESULT

Input-Queued Switch. We consider an $N \times N$ input-queued switch using virtual output queueing. Each input I_i has N virtual output queues (VOQs), denoted as $\mathrm{VOQ}(i,j), \forall j \in [N]$

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where we define $[N] \triangleq \{1, 2, \cdots, N\}$. VOQ$(i, j)$ contains all packets from input I_i to output O_j.

Traffic Pattern. We consider a time-slotted system and a *frame-synchronized* traffic pattern [3, 4]: staring from slot 1, there is an incoming packet for each VOQ every T slots and the deadline of any packet is also T slots. We call T the frame length. If a packet is delivered before its deadline, it contributes to the throughput; otherwise, the packet is useless and will be removed from the system.

Scheduling Algorithm/Policy. In each slot, the switch fabric can transmit some packets from the inputs to the outputs. In this paper, we use the most common crossbar switch fabric. Due to the physical limitations of crossbar switch fabric, each input can transmit at most one packet per slot and each output can receive at most one packet per slot. This is also known as the crossbar constraints. Then the (deterministic) decision in each slot is to select a set of pairs satisfying the crossbar constraints. The decision could also be randomized in the sense that it could randomly choose a choice among multiple choices. A scheduling algorithm/policy is the set of (possibly randomized) decisions at all slots.

Problem Statement. For a scheduling policy π, we define the *timely throughput* [3, 4] from I_i to O_j as

$$R^{\pi}_{i,j} \triangleq \liminf_{t\to\infty} \frac{\mathbb{E}\left[\sum_{\tau=1}^{t} D^{\pi}_{i,j,\tau}\right]}{t}, \forall i, j \in [N] \tag{1}$$

where $D^{\pi}_{i,j,\tau} = 1$ if a packet is delivered from input I_i to output O_j at slot τ under scheduling policy π and $D^{\pi}_{i,j,\tau} = 0$ otherwise. A rate matrix $\mathbf{R} = (R_{i,j})$ is *feasible* if there exists a scheduling policy such that the timely throughput from input I_i to output O_j is at least $R_{i,j}$ for all $i, j \in [N]$. We then define the *capacity region* $\mathcal{R}(T)$ as the set of all feasible rate matrices with frame length T. One timely-throughput-centric fundamental problem is how to characterize the capacity region $\mathcal{R}(T)$. It is important because it serves as the foundation to evaluate any scheduling policy.

Main Result. By exploiting our problem's combinatorial features, we derive a characterization of the capacity region of our delay-constrained input-queued switch in terms of $2N^2 + 2N$ linear constraints.

THEOREM 2.1. *The capacity region $\mathcal{R}(T)$ is the set of all rate matrices $\mathbf{R} = (R_{i,j})$ satisfying the following linear inequalities:*

$$\sum_{i=1}^{N} R_{i,j} \le 1, \forall j \in [N] \tag{2a}$$

$$\sum_{j=1}^{N} R_{i,j} \le 1, \forall i \in [N] \tag{2b}$$

$$R_{i,j} \in [0, 1/T], \forall i, j \in [N] \tag{2c}$$

3 SIMULATION

We simulate a 3×3 switch and vary the frame length T from 1 to 5. Since it is difficult to visualize the capacity region (of dimension $3 \times 3 = 9$), we solve instead the network-utility maximization problem with a linear utility function $U_{i,j}(R_{i,j}) = w_{i,j} R_{i,j}$ for each VOQ(i, j), i.e., we solve the linear program $\max_{\mathbf{R}\in\mathcal{R}(T)} \sum_{i,j\in[N]} w_{i,j} R_{i,j}$. We randomly pick a weight matrix, which is realized as

$$\mathbf{w} = (w_{i,j}) = \begin{pmatrix} 0.70 & 0.84 & 0.54 \\ 0.51 & 0.92 & 0.44 \\ 0.10 & 0.30 & 0.28 \end{pmatrix}.$$

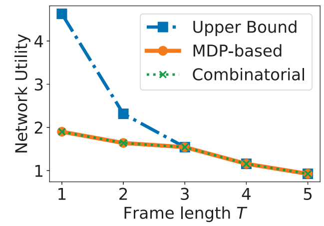

Figure 1: Capacity region characterization.

Note that we can also adopt the Markov Decision Process (MDP) theory in [3] to characterize our capacity region, whose downside is that it has an exponential number of linear inequalities. We call it MDP-based approach and call our characterization (2) the combinatorial approach. We show the achieved maximum network utility under two characterizations in Fig. 1. We can see that both approaches result in the same maximum network utility. We remark that such a result holds for all our randomly generated weighted matrices. In addition, since each VOQ has only 1 packet every T slots, the timely throughput of any VOQ is upper bounded by $1/T$ and we thus plot the utility upper bound $\sum_{i,j\in[N]} w_{i,j}/T$ in Fig. 1. We can see that when $T \ge N = 3$, the achieved maximum network utility attains the upper bound. Such a result can be verified by Theorem 2.1.

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