Appendix F: Design Process Drawings and Sketches

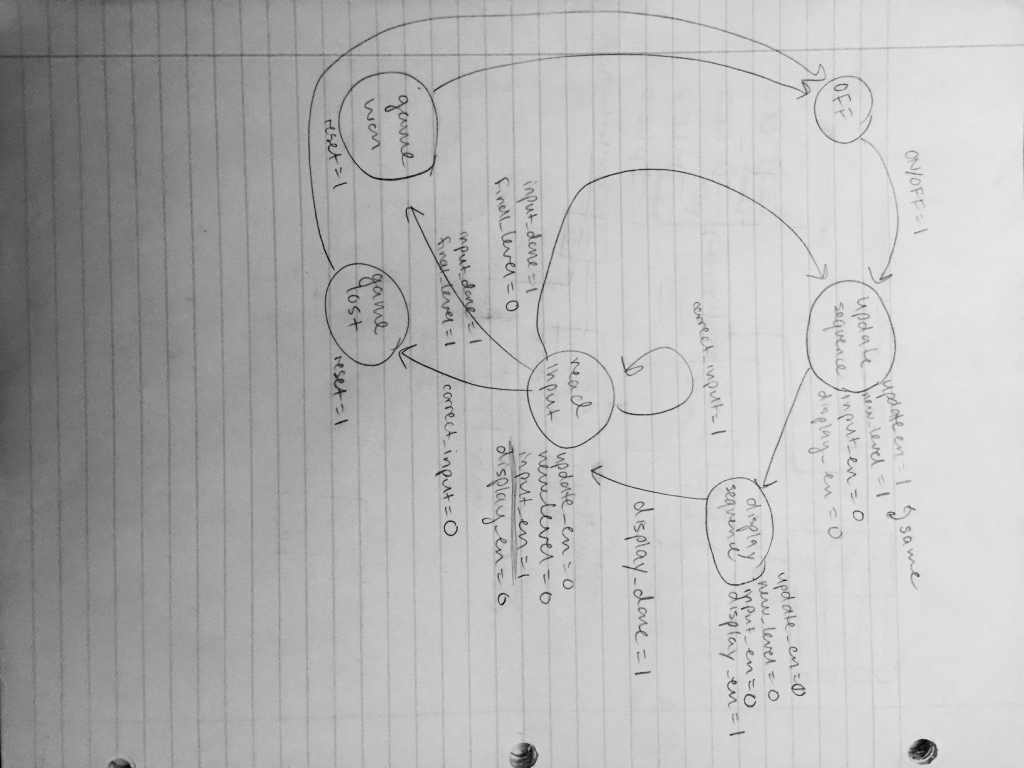


Figure 1. Original state machine diagram

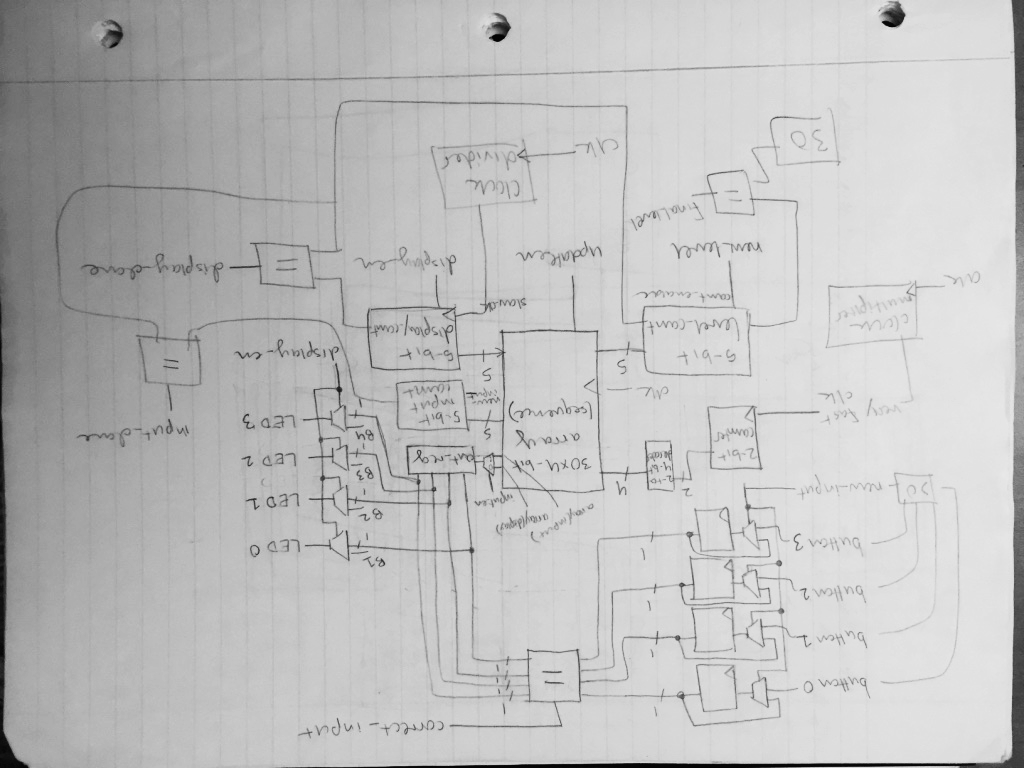


Figure 2. Original datapath diagram

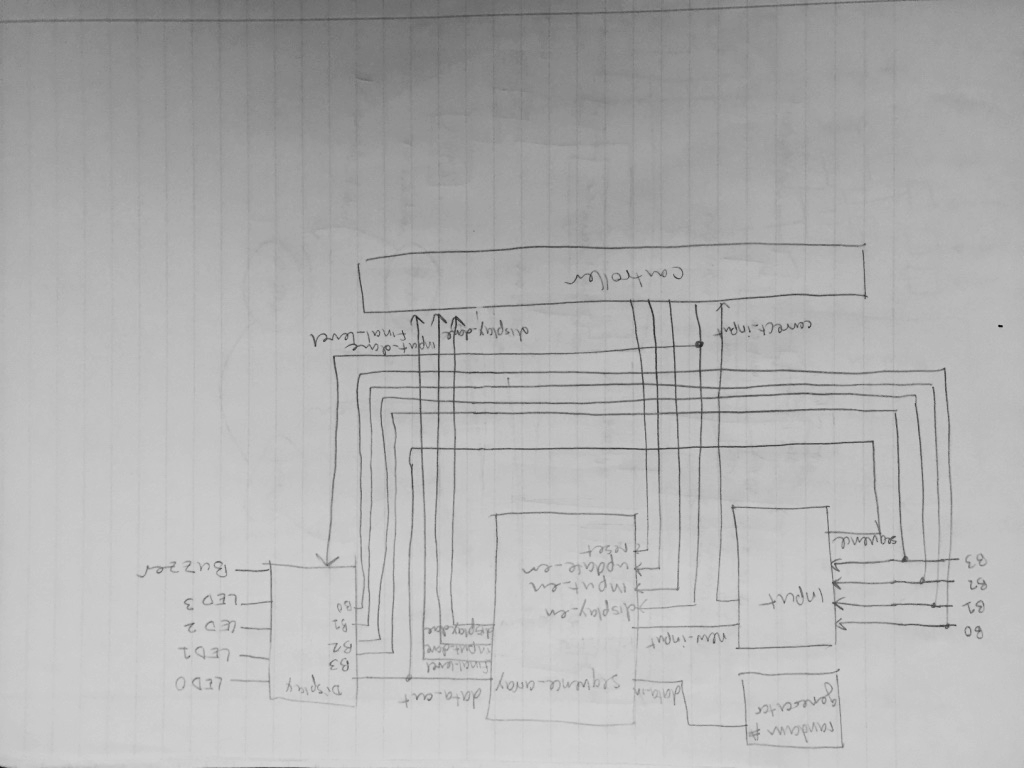


Figure 3. Original module-split design



Figure 4. Iteration on top-level design (top), plan for Input Module (bottom)

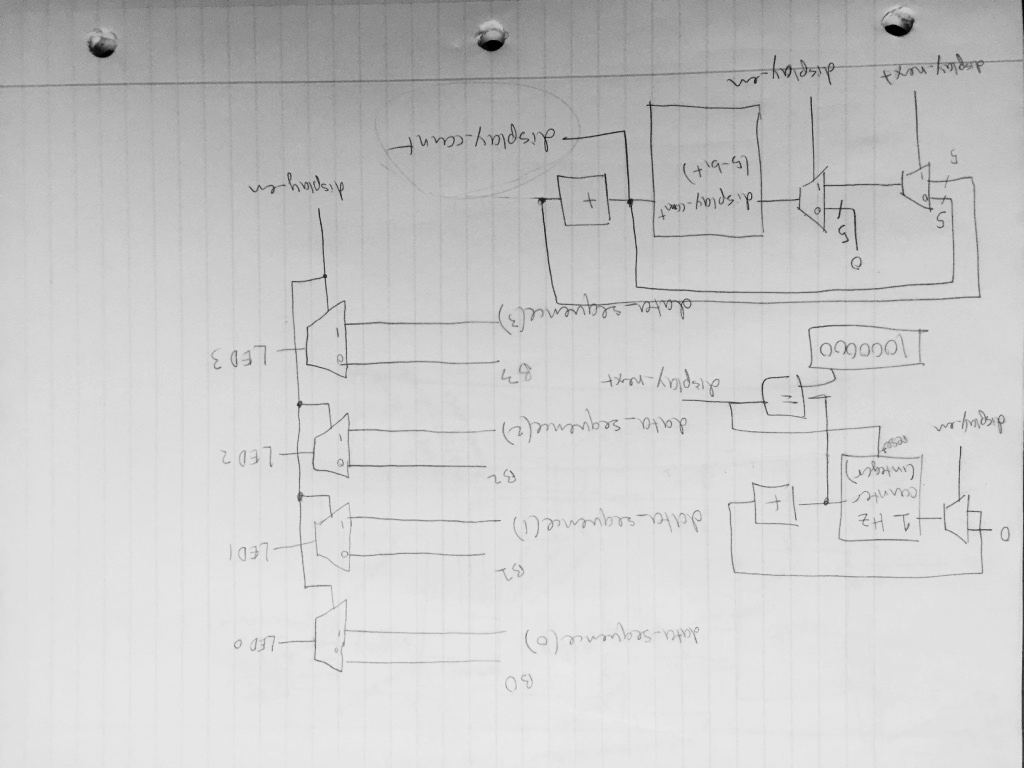


Figure 5. Original plan for Display Module datapath

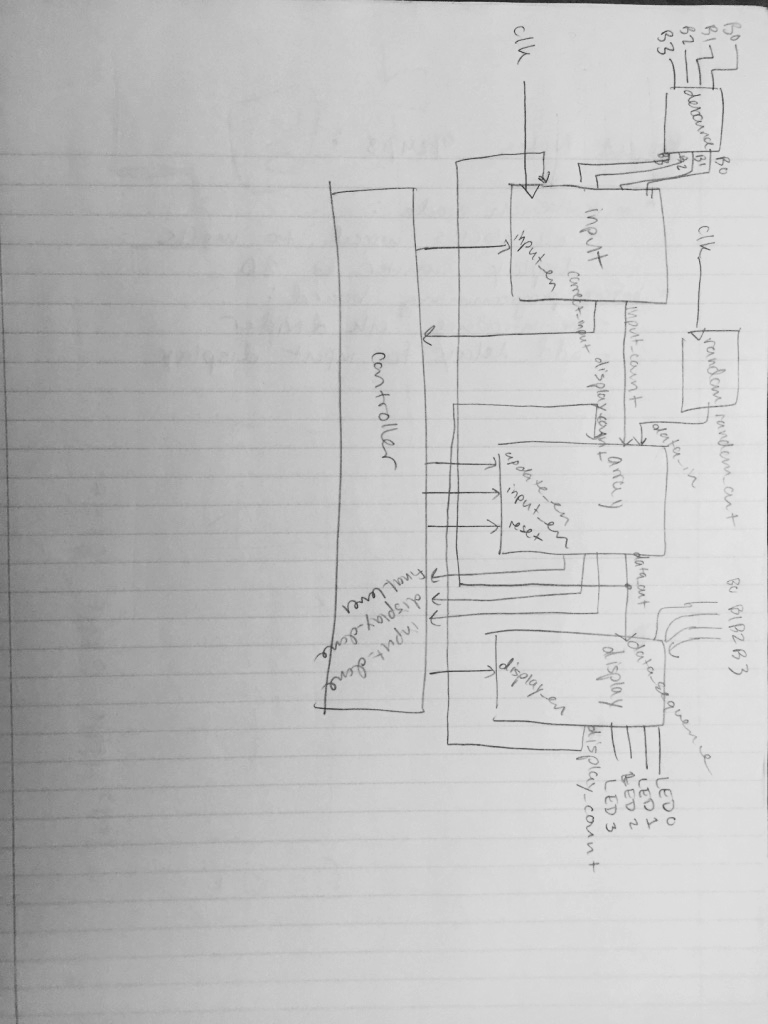


Figure 6. Iteration on top-level design

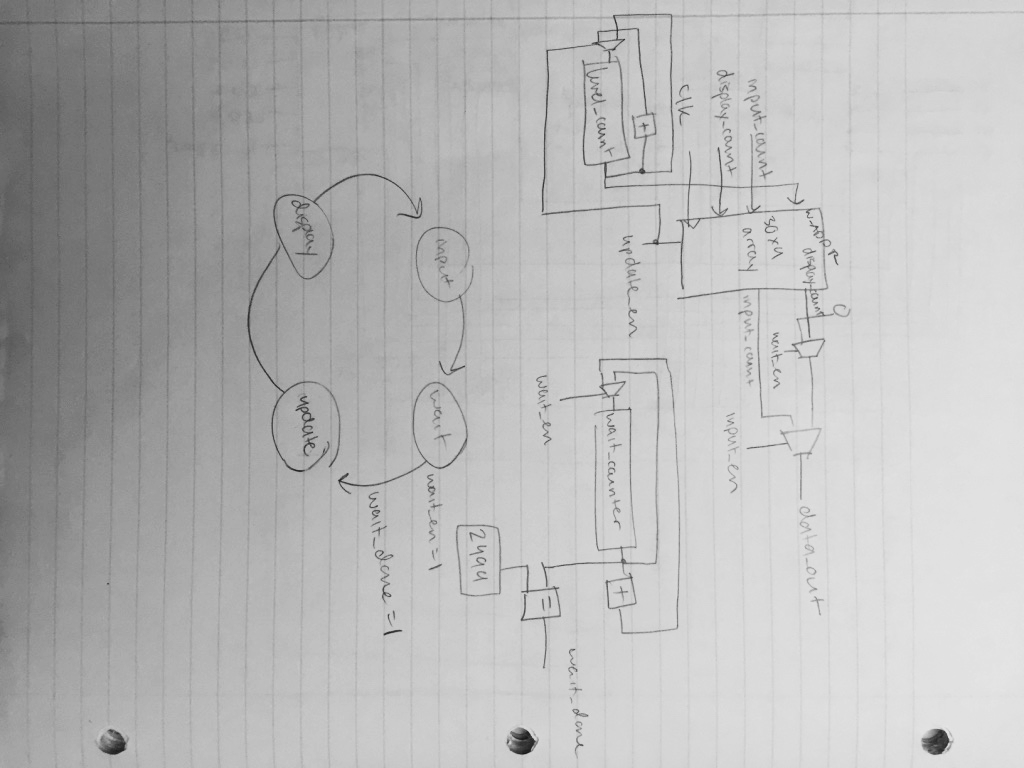


Figure 7. Plan for ‘waiting’ state (state diagram and datapath integration)

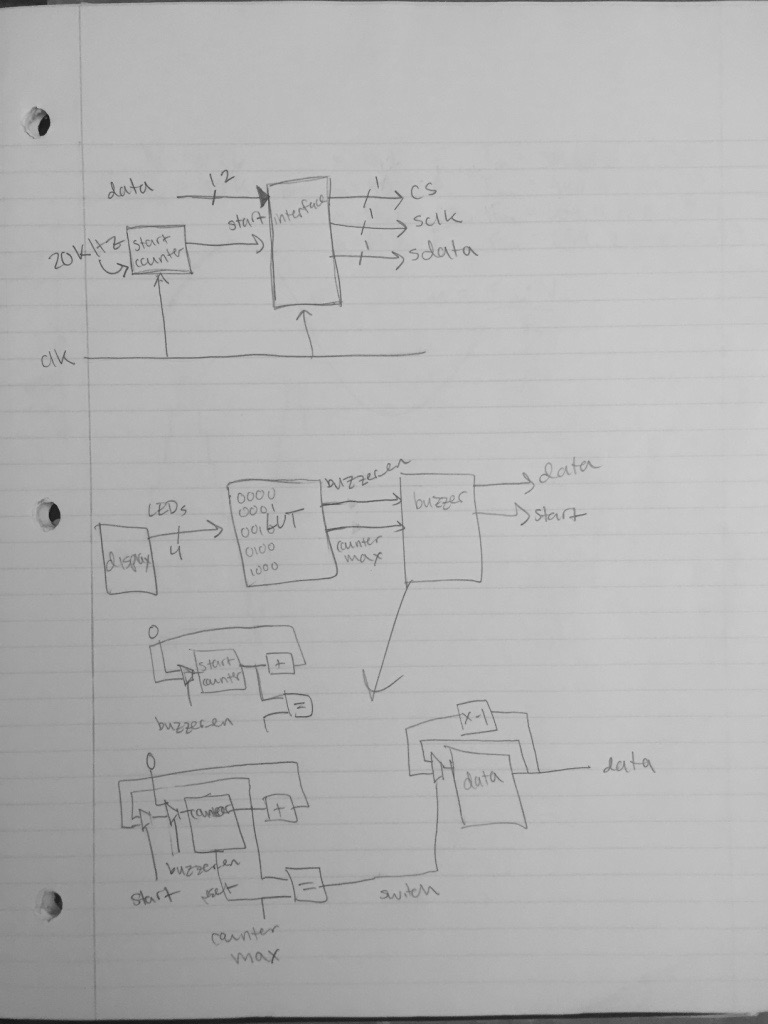


Figure 8. Plan for buzzer functionality

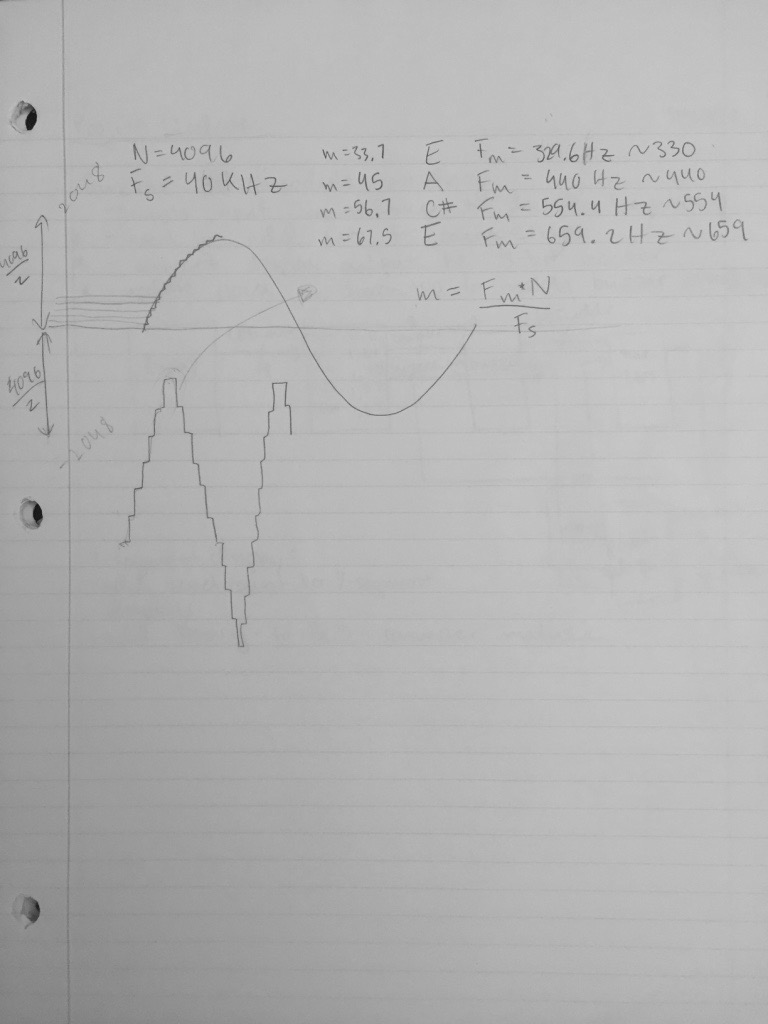


Figure 9. Calculations of counter step-sizes to achieve desired frequency

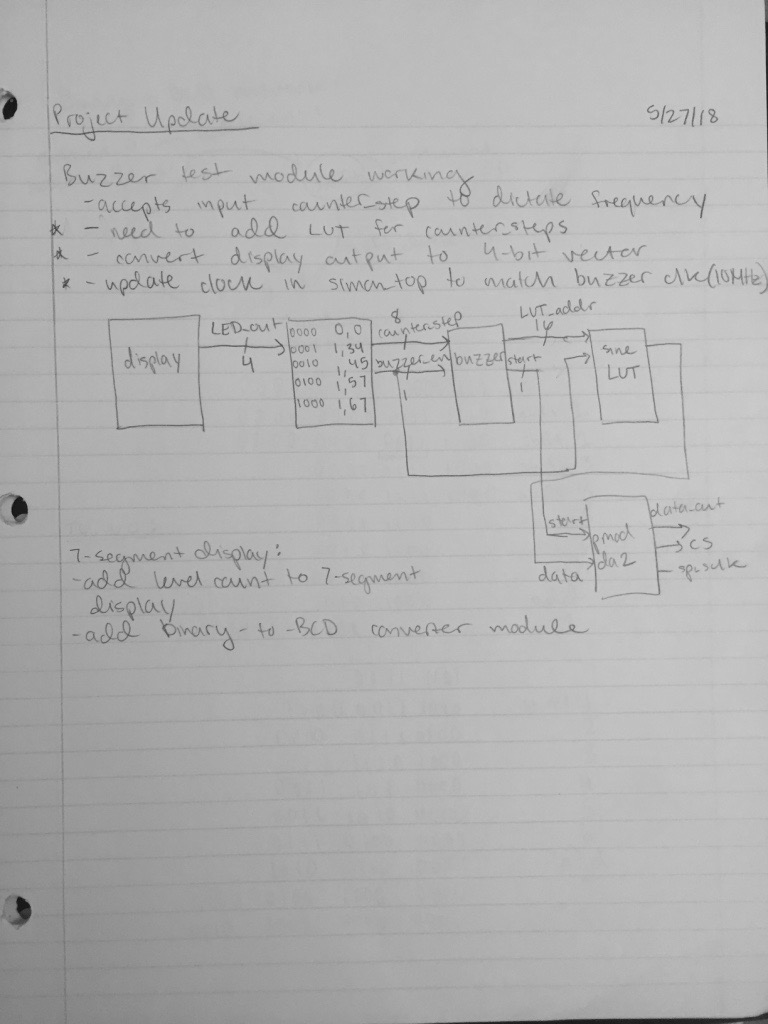


Figure 10. Integration plan for Buzzer Module