CUSTOMER APPROVAL SHEET

Company Name

MODEL	A030JTN01.2
CUSTOMER	Title :
APPROVED	Name :

■ APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 1.0)

☐ APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.___)

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☐ CUSTOMER REMARK :

AUO PM :

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Product Specification

3.0″ COLOR TFT-LCD MODULE

Model Name :	**A030JTN01.2**
Planned Lifetime:	**From 2011/Dec To 2012/Dec**
Phase-out Control:	**From 2013/Jan To 2013/Jun**
EOL Schedule:	**2013/Jun**

< > Preliminary Specification

< ◆ > Final Specification

Note: The content of this specification is subject to change without prior notice.

Record of Revision

Version	Revise Date	Page	Content
1.0	2012/01/30		First version

Contents

Precaution in Design

1. Notice

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(2) The application examples in these specification sheets are provided to explain the representative applications of the device and are not intended to guarantee any industrial property right or other rights or license you to use them. AUO assumes no responsibility for any problems related to any industrial property right of a third party resulting from the use of the device.

(3) The device listed in these specification sheets was designed and manufactured for use in Telecommunication equipment (terminals)

(4) In case of using the device for applications such as control and safety equipment for transportation (aircraft, trains, automobiles, etc.), rescue and security equipment and various safety related equipment which require higher reliability and safety, take into consideration that appropriate measures such as fail-safe functions and redundant system design should be taken.

(5) Do not use the device for equipment that requires an extreme level of reliability, such as aerospace applications, telecommunication equipment (trunk lines), nuclear power control equipment and medical or other equipment for life support.

(6) AUO assumes no responsibility for any damage resulting from the use of the device which does not comply with the
instructions and the precautions specified in these specification sheets.

(7) Contact and consult with a AUO sales representative for any questions about this device.

. Operating Precautions

(1) Since front polarizer is easily damaged, please be cautious and not to scratch it.

(2) Be sure to turn off power supply when inserting or disconnecting from input connector.

(3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

(4) When the panel surface is soiled, wipe it with absorbent cotton or soft cloth.

(5) Since the panel is made of glass, it may be broken or cracked if dropped or bumped on hard surface.

(6) Do not open nor modify the module assembly.

(7) Do not press the reflector sheet at the back of the module to any direction.

(8) In case if a module has to be put back into the packing container slot after it was taken out from the container, do not press the center of the LED light bar edge. Instead, press at the far ends of the LED light bar edge softly. Otherwise the TFT Module may be damaged.

2. For Handing And System Design

(1) Do not scratch the surface of the polarizer film as it is easily damaged.

(2) If the cleaning of the surface of the LCD panel is necessary, wipe it swiftly with cotton or other soft cloth. Do not use organic solvent as it damages polarizer.

(3) Water droplets on polarizer must be wiped off immediately as they may cause color changes, or other defects if remained for a long time.

(4) Since this LCD panel is made of glass, dropping the module or banging it against hard objects may cause cracks or fragmentation.

(5) Certain materials such as epoxy resin (amine' s hardener) or silicone adhesive agent (de-alcohol or de-oxym) emits gas to which polarizer reacts (color change). Check carefully that gas from materials used in system housing or packaging do not hurt polarizer.

(6) Liquid crystal material will freeze below specified storage temperature range and it will not get back to normal quality even after temperature comes back within specified temperature range. Liquid crystal material will become isotropic above specified temperature range and may not get back to normal quality. Keep the LCD module always within specified temperature range.

(7) Do not expose LCD module to the direct sunlight or to strong ultraviolet light for long time.

(8) If the LCD driver IC (COG) is exposed to light, normal operation may be impeded. It is necessary to design so that the light is shut off when the LCD module is mounted.

(9) Do not disassemble the LCD module as it may cause permanent damage.

(10) As this LCD module contains components sensitive to electrostatic discharge, be sure to follow the instructions in below.

① Operators

Operators must wear anti-static wears to prevent electrostatic charge up to and discharge from human body.

② Equipment and containers

Process equipment such as conveyer, soldering iron, working bench and containers may possibly generate electrostatic charge up and discharge. Equipment must be grounded through 100Mohms resistance. Use ion blower.

③ GND

To avoid ESD (Electro Static Discharge) damage, be sure to ground yourself before handling TFT-LCD Module.

④Humidity

Proper humidity of working room may reduce the risk of electrostatic charge up and discharge. Humidity should be kept over 50% all the time.

⑤Transportation/storage

Storage materials must be anti-static to prevent causing electrostatic discharge.

⑥Others

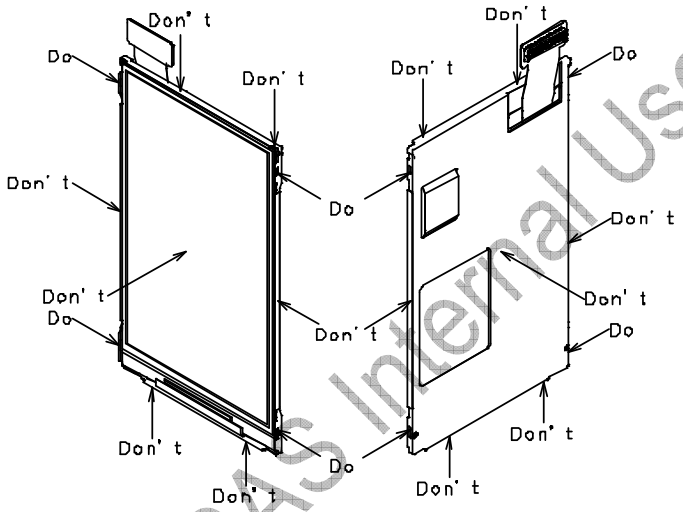
Protective film is attached on the surface of LCD panel to prevent scratches or other damages. When removing this protective film, remove it slowly under proper anti-ESD control such as ion blower.

(11) Hold LCD very carefully when placing LCD module into the system housing. Do not apply excessive stress or pressure to LCD module. Do not to use chloroprene rubber as it may affect on the reliability of the electrical interconnection.

(12) Do not hold or touch LCD panel to flex interconnection area as it may be damaged.

(13) As the binding material between LCD panel and flex connector mentioned in 12) contains an organic material, any type of organic solvents are not allowed to be used. Direct contact by fingers is also prohibited.

(14) When carrying the LCD module, place it on the tray to protect from mechanical damage. It is recommended to use the conductive trays to protect the CMOS components from electrostatic discharge. When holding the module, hold the Plastic Frame of LCD module so that the panel, COG and other electric parts are not damaged.



(15) Place a protective cover on the LCD module to protect the glass panel from mechanical damages.

(16) LCD panel is susceptible to mechanical stress and even the slightest stress will cause a color change in background. So make sure the LCD panel is placed on flat plane without any continuous twisting, bending or pushing stress.

(17) Protective film is placed onto the surface of LCD panel when it is shipped from factory. Make sure to peel it off before assembling the LCD module into the system. Be very careful not to damage LCD module by electrostatic discharge when peeling off this protective film. Ion blower and ground strap are recommended.

(18) Make sure the mechanical design of the system in which the LCD module will be assembled matches specified viewing angle of this LCD module.

(19) This LCD module does not contain nor use any ODS (1,1,1-Trichloroethane, CCL4) in all materials used, in all production processes.

3. For Operating LCD Module

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) At the shipment, adjust the contrast of each LCD module with electric volume. LCD contrast may vary from panel to panel depending on variation of LCD power voltage from system.

(3) As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 ˚C and it becomes stable.

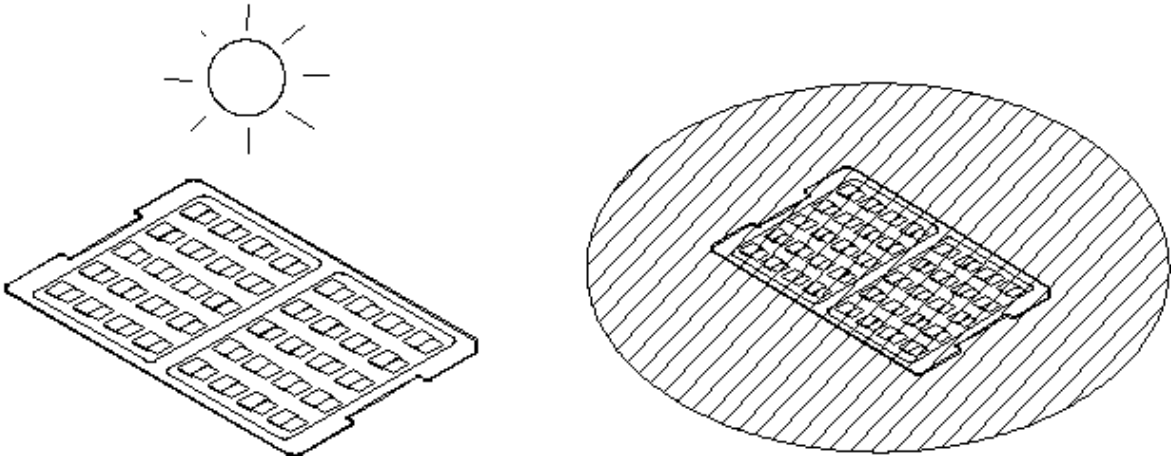
4. Precaution for Storage

(1) Do not expose the LCD module to direct sunlight or strong ultraviolet light for long periods. Store in a dark place.

(2) The liquid crystal material will solidify if stored below the rated storage temperature and will become an isotropic liquid if stored above the rated storage temperature, and may not retain its original properties. Only store the module at normal temperature and humidity (25±5˚C,60±10%RH) in order to avoid exposing the front polarizer to chronic humidity.

(3) Keeping Method

DON'T DO



a. Don't keeping under the direct sunlight. b. Keeping in the tray under the dark place.

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) Be sure to prevent light striking the chip surface.

5. Other Notice

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) As electrical impedance of power supply lines (VCC-GND) are low when LCD module is working, place the de-coupling capacitor near by LCD module as close as possible.

(3) Reset signal must be sent after power on to initialize LSI. LSI does not function properly until initialize it by reset signal.

(4) Generally, at power on, in order not to apply DC charge directly to LCD panel, supply logic voltage first and initialize LSI logic function including polarity alternation. Then supply voltage for LCD bias. At power off, in order not to apply DC charge directly to LCD panel, execute Power OFF sequence and Discharge command.

(5) Don’ t touch to FPC surface, exposed IC chip, electric parts and other parts, to any electric, metallic materials.

(6) No bromide specific fire-retardant material is used in this module.

(7) Do not display still picture on the display over 2 hours as this will damage the liquid crystal.

6. Precaution for Discarding Liquid Crystal Modules

COG: After removing the LSI from the liquid crystal panel, dispose of it in a similar way to circuit boards from electronic devices.

LCD panel: Dispose of as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances.

A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution（dot）	960(W) x 480(H)	
2	Active area（mm）	60 x 45	
3	Screen size（inch）	2.95 (Diagonal)	
4	Dot pitch（um）	62.5x 93.75	
5	Color configuration	R, G, B delta	
6	Overall dimension（mm）	70.2 x 51.4 x 2.2	Note 1
7	Weight（g）	18	
8	Panel surface treatment	Hard Coating	

Note 1: Refer to F. Outline Dimension

B. Electrical specifications

1. Pin assignment

Pin no	Symbol	I/O	Description	Remark
1	VDD	P	Voltage input pin for analog power	
2	GND	P	Ground	
3	GND	P	Ground	
4	GRB	I	Global reset pin	
5	STB	I	Standby setting. It should be connected to VDDIO in normal operation	
6	CS	I	Chip select pin of SPI interface	
7	SDA	I	Data input pin of SPI mode	
8	SCL	I	Clock input pin of SPI mode	
9	VDDIO	P	Voltage input pin for digital power	
10	VDD_18V	C	Connect capacitor	
11	DCLK	I	Data-clock and oscillator source	
12	VSYNC	I	Vertical synchronizing signal	
13	HSYNC	I	Horizontal synchronizing signal	
14	D15	I	Data signal (MSB)	
15	D14	I	Data signal	
16	D13	I	Data signal	
17	D12	I	Data signal	
18	D11	I	Data signal	
19	D10	I	Data signal	
20	D09	I	Data signal	
21	D08	I	Data signal (LSB)	
22	D07	I	Data signal (MSB)	
23	D06	I	Data signal	
24	D05	I	Data signal	
25	D04	I	Data signal	
26	D03	I	Data signal	
27	D02	I	Data signal	
28	D01	I	Data signal	
29	D00	I	Data signal (LSB)	
30	VCOMH	C	Connect capacitor	
31	VCOML	C	Connect capacitor	

32	VCL	C	Connect capacitor	
33	C3N	C	Connect capacitor	
34	C3P	C	Connect capacitor	
35	VDD2	C	Connect capacitor	
36	C1P	C	Connect capacitor	
37	C1N	C	Connect capacitor	
38	C2P	C	Connect capacitor	
39	C2N	C	Connect capacitor	
40	C4P	C	Connect capacitor	
41	C4N	C	Connect capacitor	
42	VGH	C	Connect capacitor	
43	C5P	C	Connect capacitor	
44	C5N	C	Connect capacitor	
45	VGL	C	Connect capacitor	
46	VLED+	P	LED backlight anode	
47	VLED-	P	LED backlight cathode	

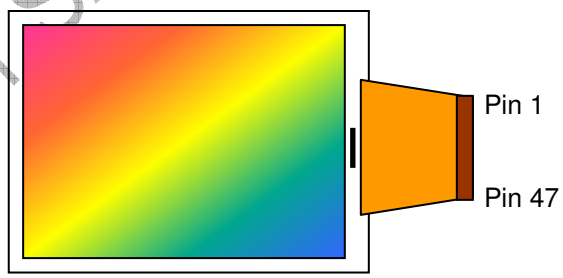
I：Input, O：Output, C：Capacitor, P：Power

Note1:D[15:08]:8-bit C date of YUV input when YUV-16bit timing.

Note2:D[07:00]:8-bit Y date of YUV input when YUV-16bit timing.

D[07:00]:serial 8-bit data input when YUV 320 8-bit or UPS051 timing.

Note3: Definition of scanning direction, Refer to figure as below：



2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Supply Voltage	VDD	GND=0V	-0.3	6.0		
Supply Voltage	VDDIO	GND=0V	-0.3	6.0	V	

Note 1: Functional operation should be restricted under ambient temperature (25°C).

Note 2: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

3. Electrical characteristics

3.1 Recommended operating conditions (GND=0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
		VDD	3.0	3.3	3.6	V	
		VDDIO	3.0	3.3	3.6		
Input Signal	H Level	V_{IH}	0.7* VDDIO	-	VDDIO	V	
	L Level	V_{IL}	GND	-	0.3* VDDIO	V	

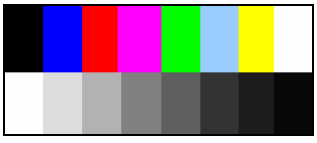
3.2 Electrical characteristics (GND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input Current for V_{VDD}	I_{VDD}	V_{VDD}=3.3V	-	14	18	mA	Note 1
	$I_{VDD(STANDBY)}$		-	50	100	uA	
Input Current for V_{VDDIO}	I_{VDDIO}	V_{VDDIO}=3.3V	-	0.5	1	mA	Note 1
	$I_{VDDIO(STANDBY)}$		-	20	50	uA	
DC-DC voltage	V_{GH}	V_{DD}=3.3V	13	14	15	V	Note 2
	V_{GL}	V_{DD}=3.3V	-10	-9	-8	V	Note 2
VCOM voltage	V_{CAC}	-	4.8	5.4	6	Vp-p	AC component, Note 3

Note 1: Test Condition: 8colorbar+Grayscale pattern, UPS051 mode, Frame rate: 60Hz, other registers are default setting.

Note 2: V_{GH} and V_{GL} are output voltages of integrated LCD driver IC.

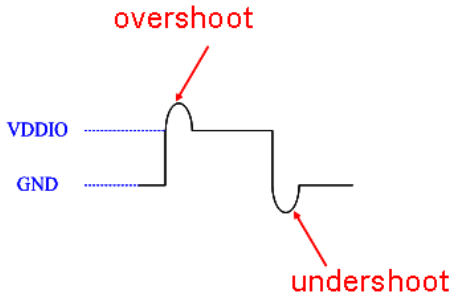
Note 3: The brightness of LCD panel could be adjusted by the adjustment of the AC component of VCOM.



3.2 Digital input signal overshoot and undershoot limitation

The digital input signal overshoot and undershoot voltage should keep under VDDIO+0.3V and over GND-0.3V.

Symbol	Overshoot	Undershoot
D0-D15	< VDDIO+0.3V	> GND-0.3V
DCLK		
HSYNC		
VSYNC		
SCL		
SDA		
CS		
GRB		
STB		



3.3 Recommended Capacitance Values of External Capacitor

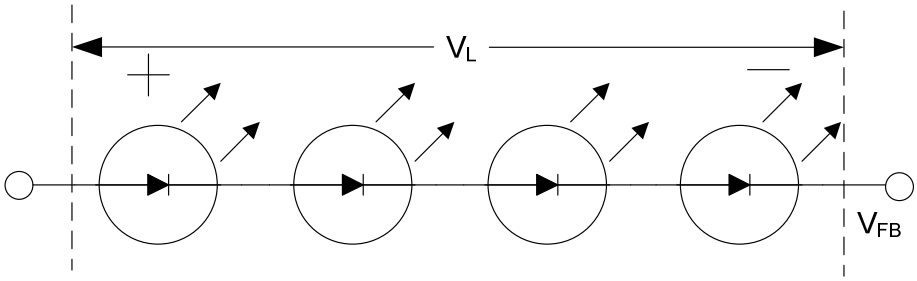
The recommended capacitance values of the external capacitor are shown below. These values should be finally determined only after performing sufficient evaluation on the module.

Pin name	Recommended value of capacitors (μF)	Withstanding voltage (V)
VGH	1 to 2.2	25
VGL	1 to 2.2	16
VDD	1 to 2.2	6.3
VDDIO	1 to 2.2	6.3
VDD_18V	1 to 2.2	6.3
VDD2	1 to 4.7	10
VCL	1 to 2.2	10
VCOMH	1 to 4.7	10
VCOML	1 to 4.7	10
C1P,C1N	1	6.3
C2P,C2N	1	6.3
C3P,C3N	1	10
C4P,C4N	1	16
C5P,C5N	1	16

3.4 Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current			25	27.5	mA	
LED voltage	V_L		12.8	14	V	4 LED's
Feedback voltage	V_{FB}				V	

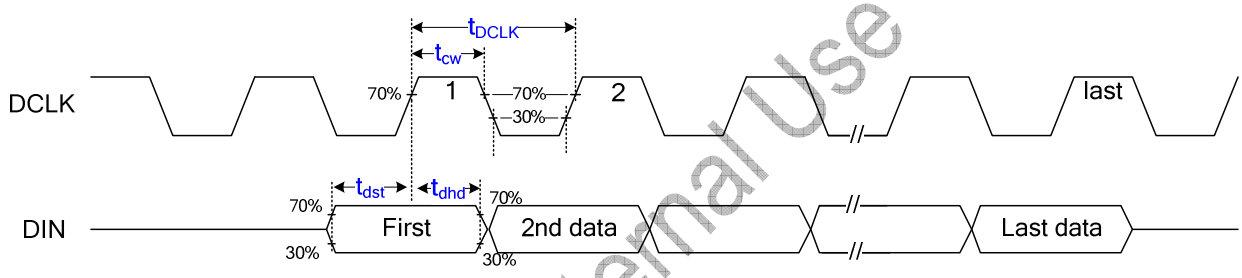
Note1: To consider Backlight driver and feedback resistor tolerance.

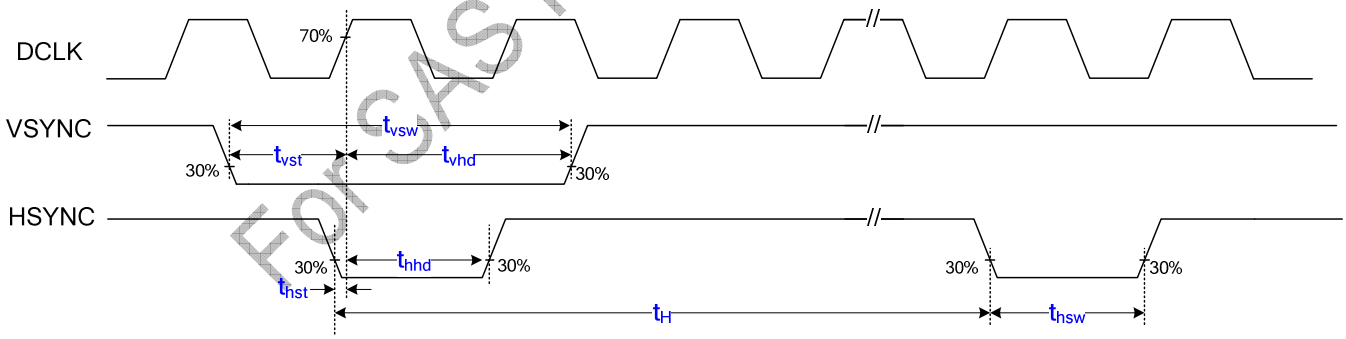


4. Input timing AC characteristic

(VDD=3.0 ~3.6V, AGND=GND=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK duty cycle	Tcw	40	50	60	%	
VSYNC setup time	Tvst	8	-	-	ns	
VSYNC hold time	Tvhd	8	-	-	ns	
HSYNC setup time	Thst	8	-	-	ns	
HSYNC hold time	Thhd	8	-	-	ns	
Data setup time	Tdst	8	-	-	ns	
Data hold time	Tdhd	8	-	-	ns	





t_H means: HSYNC period

5. Input timing format

5.1 UPS051 timing conditions (Refer to Fig.1 Fig.2 Fig.3)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency		$1/t_{DCLK}$	30	33	36	MHz	
HSYNC	Period	t_H	1004	1048	1399	t_{DCLK}	
	Display period	t_{hd}	960			t_{DCLK}	
	Back porch	t_{hbp}	20	40	255	t_{DCLK}	Note 1
	Front porch	t_{hfp}	24	48	96	t_{DCLK}	
	Pulse width	t_{hsw}	1	20	t_{hbp} -1	t_{DCLK}	
VSYNC	Period	t_V	485	525	576	t_H	
	Display period	t_{vd}	480			t_H	
	Back porch	t_{vbp}	3	27	31	t_H	Note 2
	Front porch	t_{vfp}	2	18	66	t_H	
	Pulse width	t_{vsw}	$1t_{DCLK}$	$1t_{DCLK}$	$6t_H$		

Note 1: The t_{hbp} time is adjustable by setting register HBLK; requirement of minimum blanking time and minimum front porch time must be satisfied.

Note 2: The t_{vbp} time is adjustable by setting register VBLK. UPS051 accepts both interlace and non-interlace vertical input timing.

Fig.1 UPS051 Input Horizontal Timing Chart

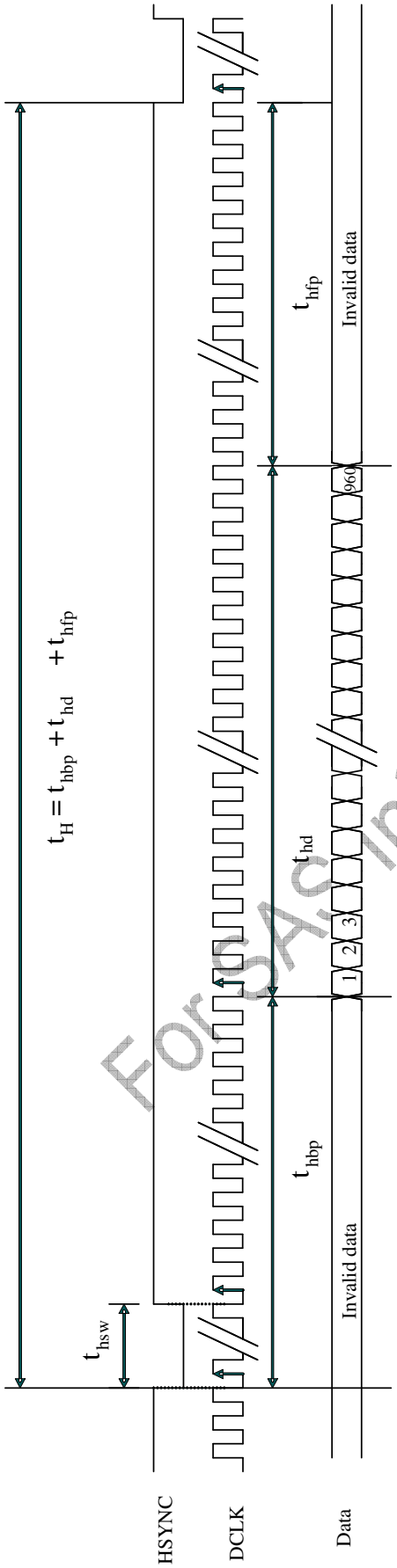
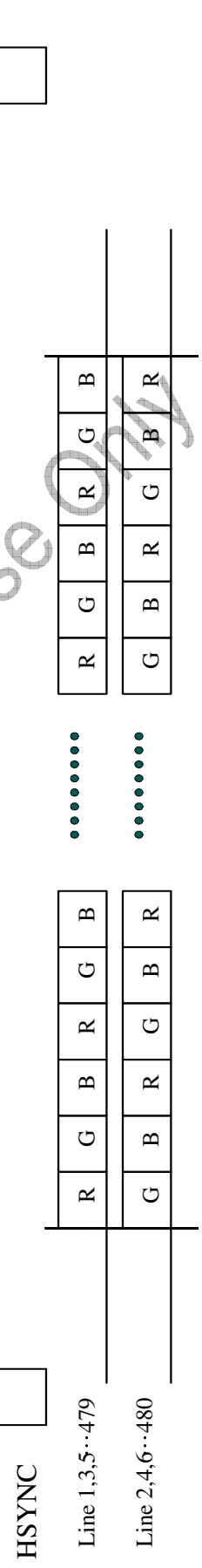


Fig.2 UPS051 Input Horizontal Data Sequence



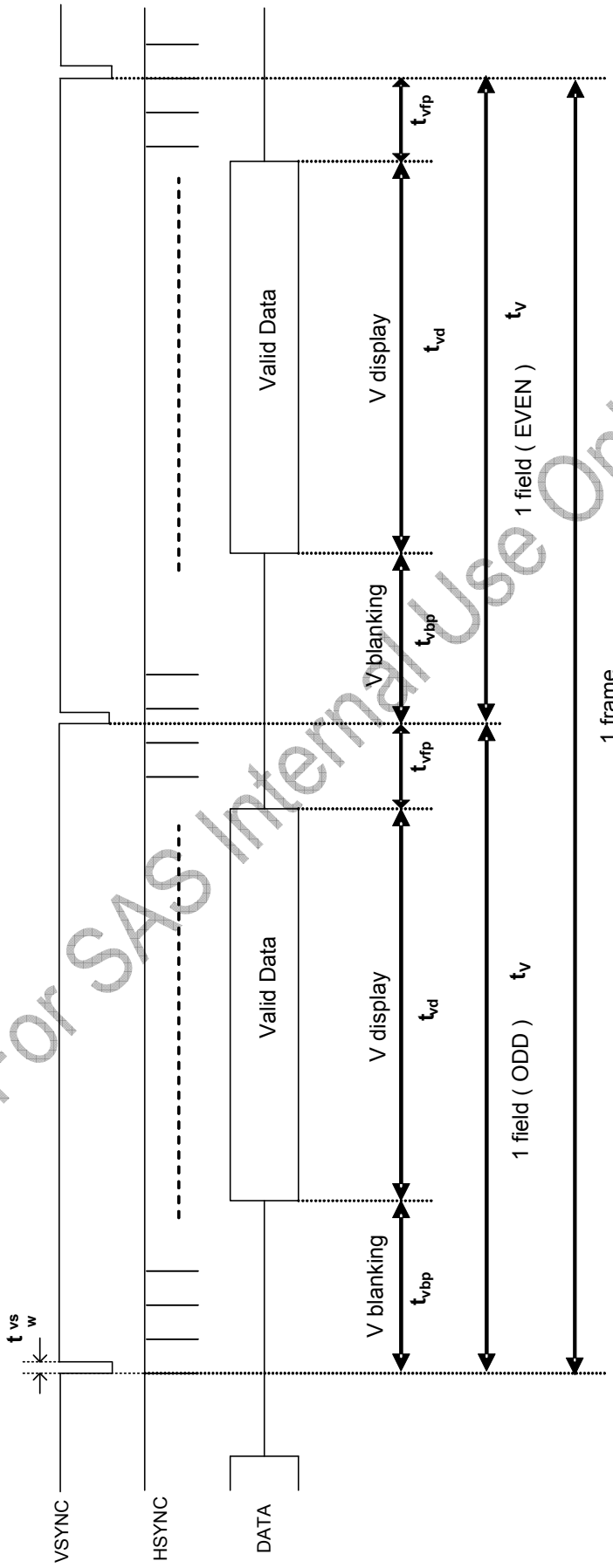


Fig.3 UPS051 Input Vertical Timing Chart

5.2 YUV 320 8-bit serial mode (Refer to Fig.4 Fig.5)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency		$1/t_{DCLK}$	23	24.5	25	MHz	
HSYNC	Period	t_H	710	780	877	t_{DCLK}	
	Display period	t_{hd}	640			t_{DCLK}	
	Back porch	t_{hbp}	20	40	127	t_{DCLK}	Note 1
	Front porch	t_{hfp}	50	100	110	t_{DCLK}	
	Pulse width	t_{hsw}	1	1	t_{hbp} -1	t_{DCLK}	
VSYNC	Period	t_V	485	525	576	t_H	
	Display period	t_{vd}	480			t_H	
	Back porch	t_{vbp}	3	27	31	t_H	Note 2
	Front porch	t_{vfp}	2	18	66	t_H	
	Pulse width	t_{vsw}	$1t_{DCLK}$	$1t_{DCLK}$	$6t_H$		

Note 1: The t_{hbp} time is adjustable by setting register HBLK; requirement of minimum blanking time and minimum front porch time must be satisfied.

Note 2: The t_{vbp} time is adjustable by setting register VBLK.

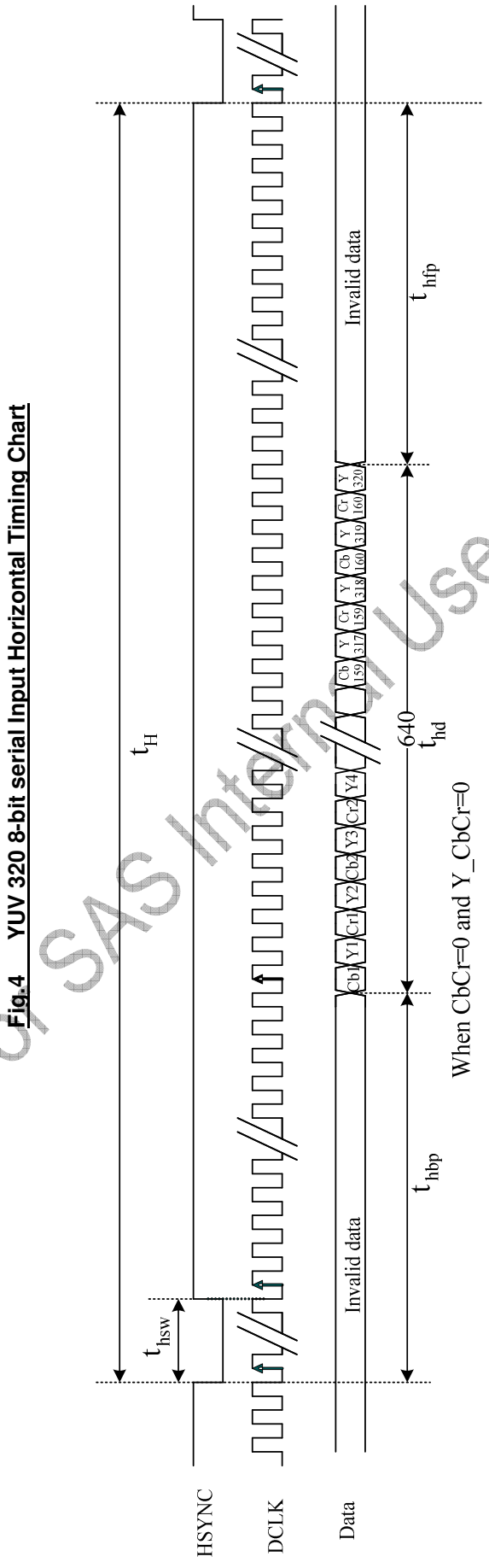


Fig.4 YUV 320 8-bit serial Input Horizontal Timing Chart

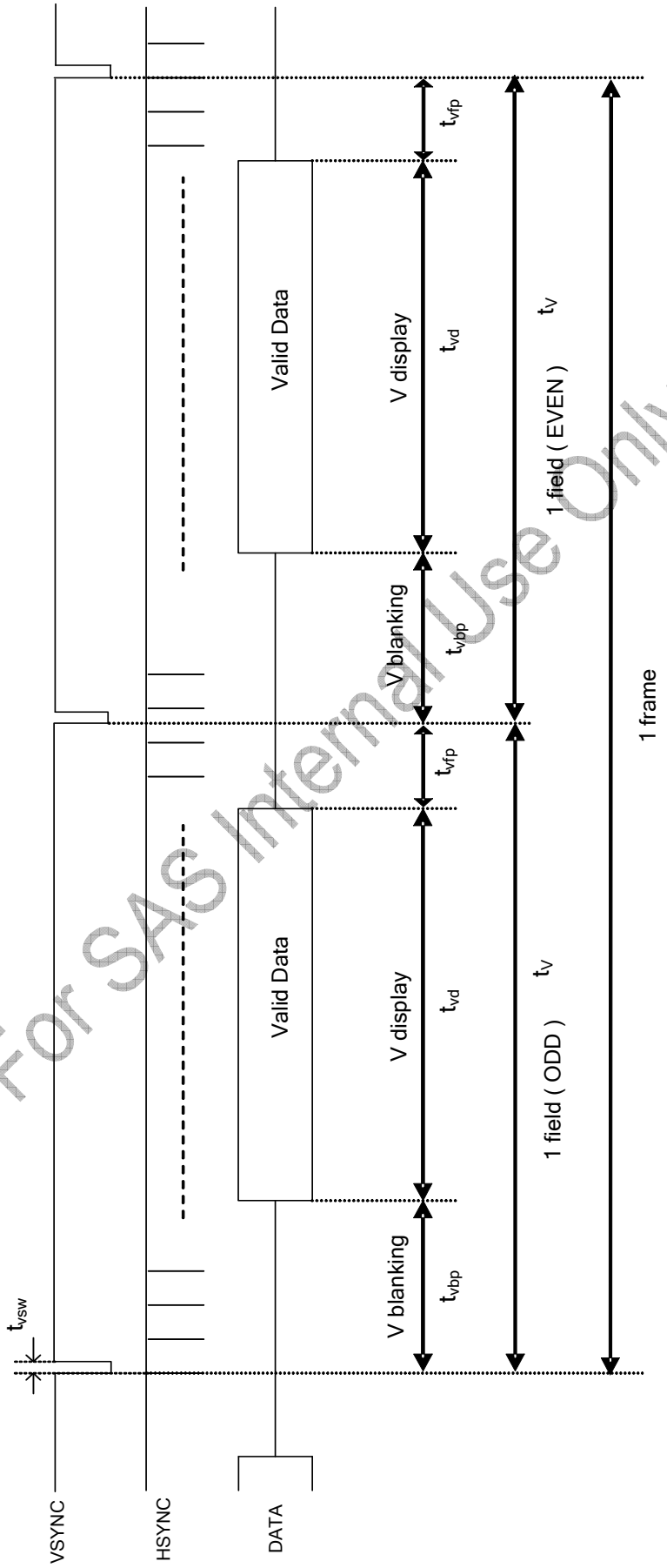


Fig.5 YUV 320 8-bit serial Input Vertical Timing Chart

5.3 YUV 320 16-bit parallel mode(Refer to Fig.6 Fig.7)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency		$1/t_{DCLK}$	10	12	14	MHz	
HSYNC	Period	t_H	351	381	388	t_{DCLK}	
	Display period	t_{hd}	320			t_{DCLK}	
	Back porch	t_{hbp}	20	40	45	t_{DCLK}	
	Front porch	t_{hfp}	11	21	23	t_{DCLK}	
	Pulse width	t_{hsw}	1	20	t_{hbp} -1	t_{DCLK}	
VSYNC	Period	t_V	485	525	576	t_H	
	Display period	t_{vd}	480			t_H	
	Back porch	t_{vbp}	3	27	31	t_H	
	Front porch	t_{vfp}	2	18	66	t_H	
	Pulse width	t_{vsw}	$1t_{DCLK}$	$1t_{DCLK}$	$6t_H$		

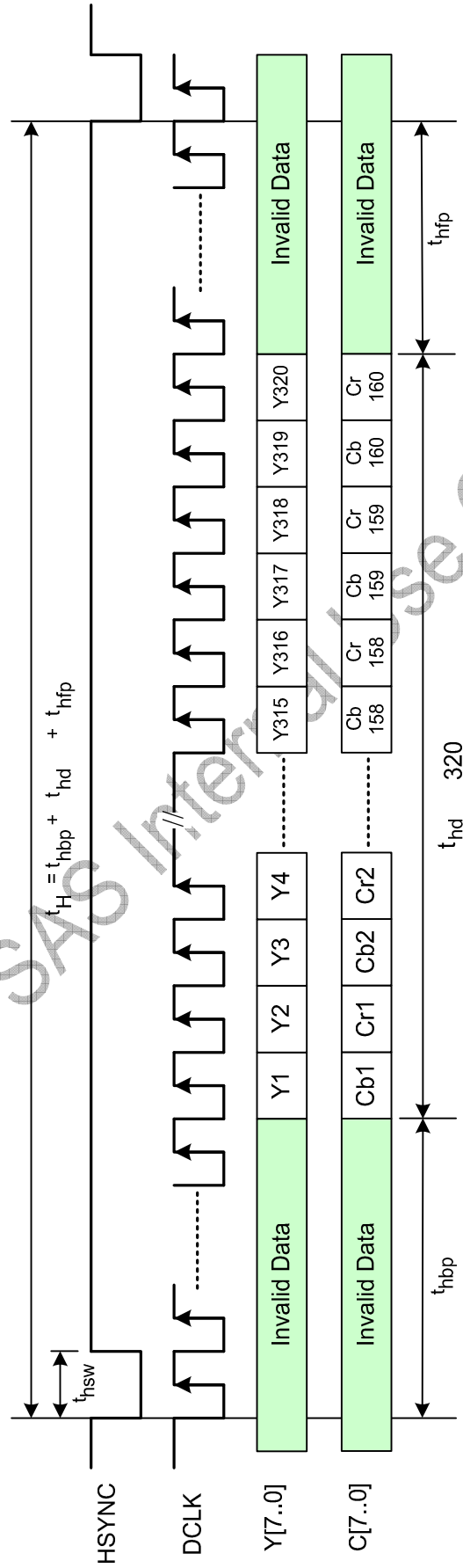


Fig.6 YUV 320 16-bit Input Horizontal Timing Chart

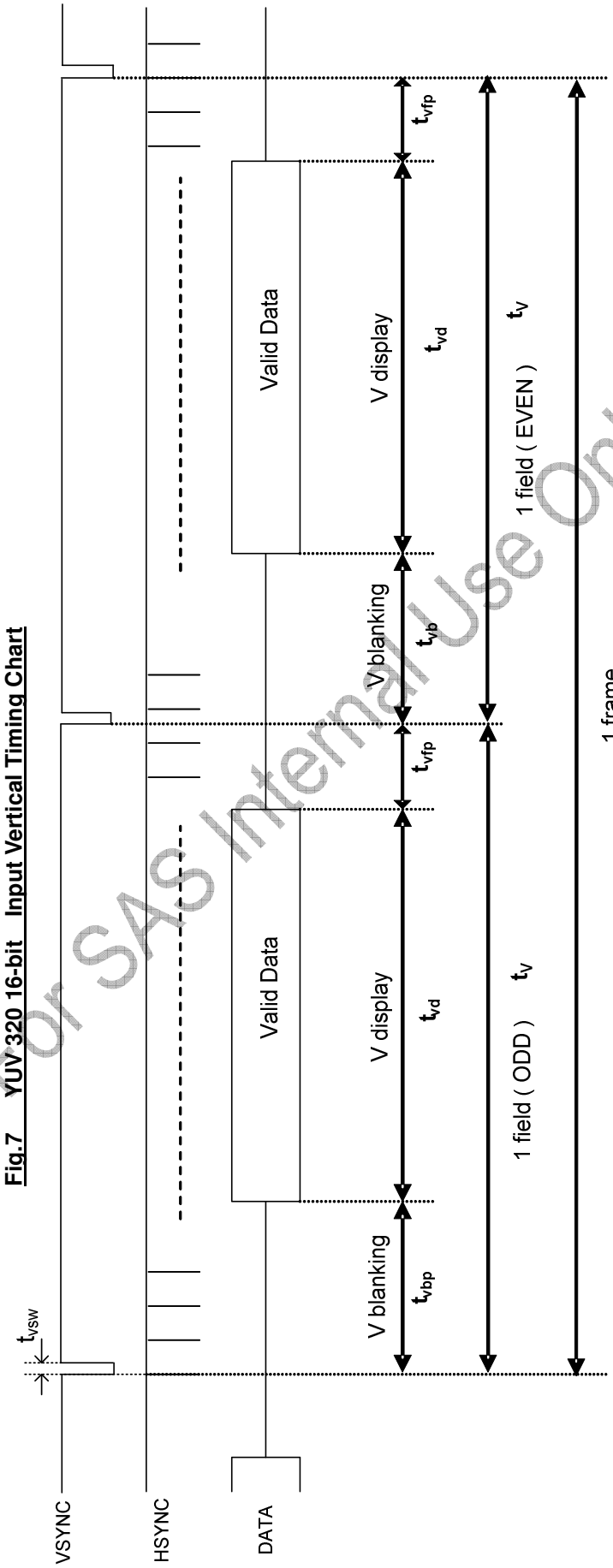


Fig.7 YUV 320 16-bit Input Vertical Timing Chart

5.4 YUV 640 16-bit parallel mode(Refer to Fig.8 Fig.10)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency		$1/t_{DCLK}$	23	24.5	25	MHz	
HSYNC	Period	t_H	710	780	877	t_{DCLK}	
	Display period	t_{hd}	640			t_{DCLK}	
	Back porch	t_{hbp}	20	40	127	t_{DCLK}	Note 1
	Front porch	t_{hfp}	50	100	110	t_{DCLK}	
	Pulse width	t_{hsw}	1	1	t_{hbp} -1	t_{DCLK}	
VSYNC	Period	t_V	485	525	576	t_H	
	Display period	t_{vd}	480			t_H	
	Back porch	t_{vbp}	3	27	31	t_H	Note 2
	Front porch	t_{vfp}	2	18	66	t_H	
	Pulse width	t_{vsw}	$1t_{DCLK}$	$1t_{DCLK}$	$6t_H$		

5.5 YUV 720 16-bit parallel mode(Refer to Fig.9 Fig.10)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency		$1/t_{DCLK}$	25	27	28	MHz	
HSYNC	Period	t_H	789	858	954	t_{DCLK}	
	Display period	t_{hd}	720			t_{DCLK}	
	Back porch	t_{hbp}	40	40	127	t_{DCLK}	
	Front porch	t_{hfp}	49	98	107	t_{DCLK}	
	Pulse width	t_{hsw}	1	1	t_{hbp} -1	t_{DCLK}	
VSYNC	Period	t_V	485	525	576	t_H	
	Display period	t_{vd}	480			t_H	
	Back porch	t_{vbp}	3	27	31	t_H	
	Front porch	t_{vfp}	2	18	66	t_H	
	Pulse width	t_{vsw}	$1t_{DCLK}$	$1t_{DCLK}$	$6t_H$		

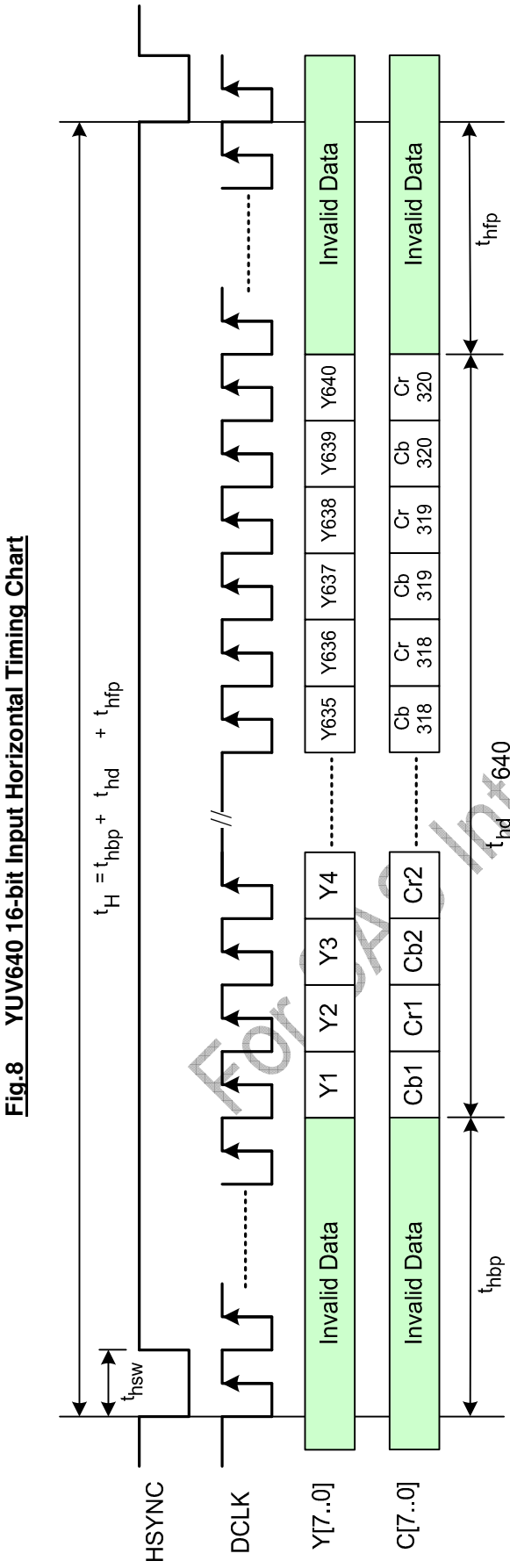


Fig.8 YUV640 16-bit Input Horizontal Timing Chart

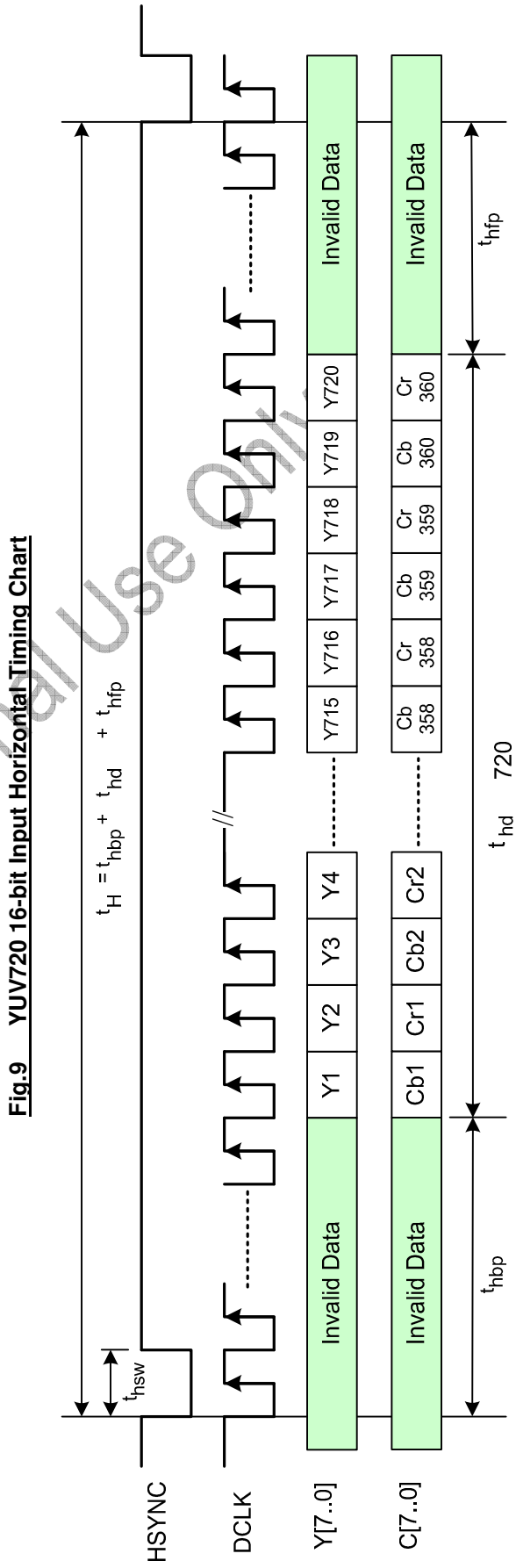


Fig.9 YUV720 16-bit Input Horizontal Timing Chart

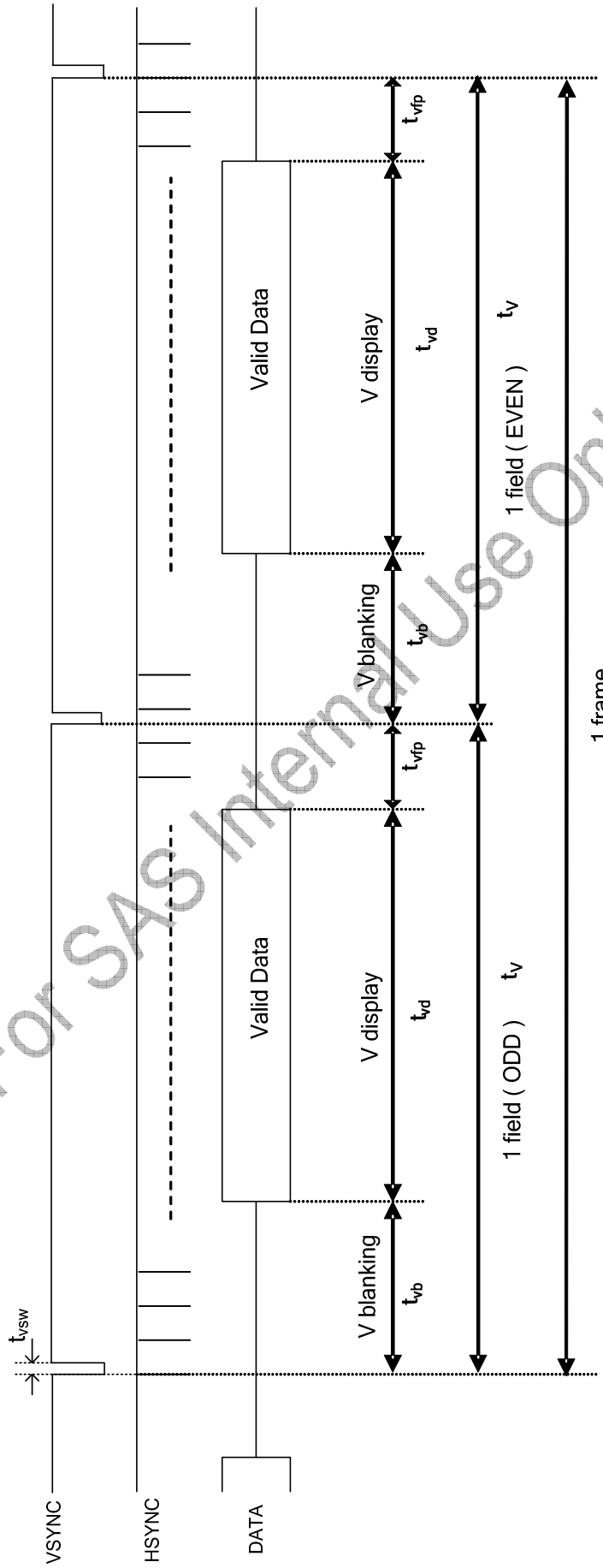


Fig.10 YUV640/YUV720 16 bit parallel Input Vertical Timing Chart

5.6 YUV 320 to RGB conversion

$R2n\text{-}1 = 1.164*(Y_{2n-1} - 16) + 1.596*(C_{rn} - 128)$

$R2n = 1.164*(Y_{2n} - 16) + 1.596*(C_{rn} - 128)$

$G2n\text{-}1 = 1.164*(Y_{2n-1} - 16) - 0.813*(C_{rn} - 128) - 0.391*(C_{bn} - 128)$

$G2n = 1.164*(Y_{2n} - 16) - 0.813*(C_{rn} - 128) - 0.391*(C_{bn} - 128)$

$B2n\text{-}1 = 1.164*(Y_{2n-1} - 16)+ 2.017*(C_{bn} - 128)$

$B2n = 1.164*(Y_{2n} - 16) + 2.017*(C_{bn} - 128)$

Where Y : 16~235 Cr : 16~240 Cb : 16~240

5.7 YUV 720/YUV 640 to RGB conversion

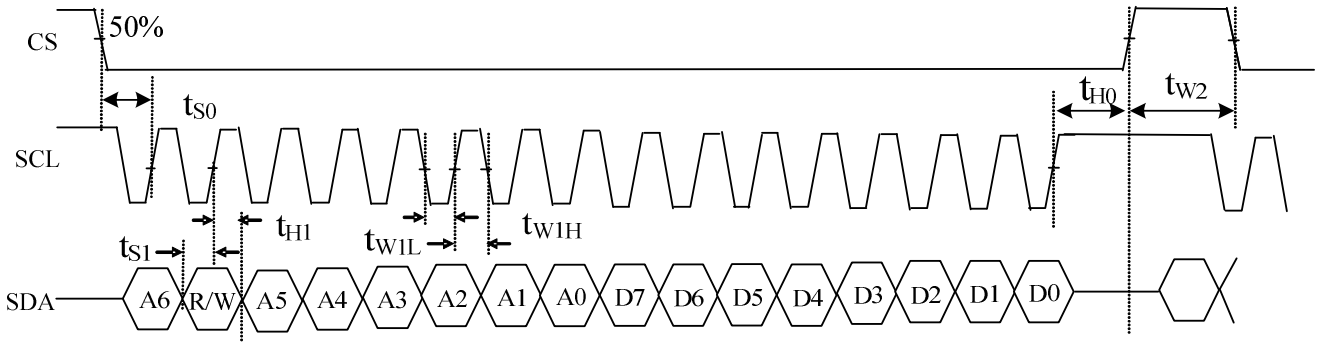
$R_n=1.164*[(Y_{2n-1} + Y_{2n})/2\text{-}16] + 1.596*(C_{rn} -128)$

$G_n=1.164*[(Y_{2n-1}+ Y_{2n})/2\text{-}16] - 0.813*(C_{rn} -128) - 0.392*(C_{bn} -128)$

$B_n=1.164*[(Y_{2n-1}+ Y_{2n})/2\text{-}16] + 2.017*(C_{bn} -128)$

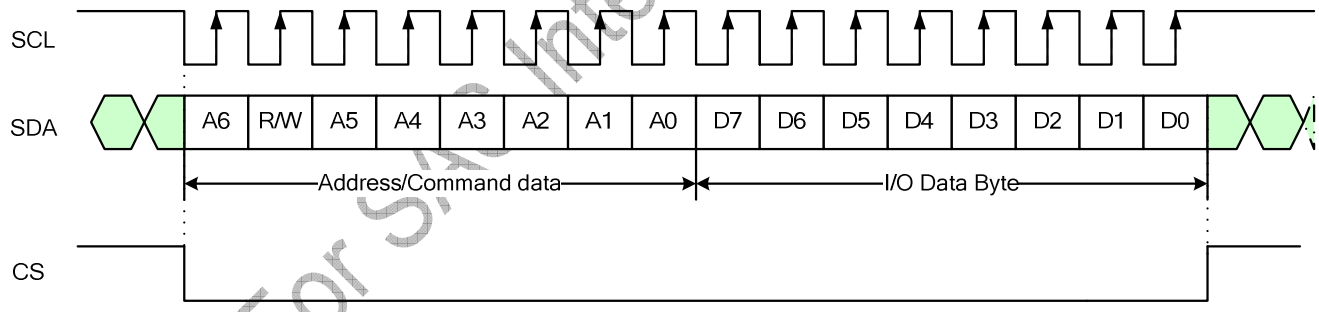
Where Y:16~235 C_r:16~240 C_b:16~240

6. Serial control interface AC characteristic



Item	Symbol	Min	Typical	Max	Unit
CS input setup Time	t_{S0}	50	-	-	ns
Serial data input setup Time	t_{S1}	50	-	-	ns
CS input hold Time	t_{H0}	50	-	-	ns
Serial data input hold Time	t_{H1}	50	-	-	ns
SCL pulse low width	t_{W1L}	50	-	-	ns
SCL pulse high width	t_{W1H}	50	-	-	ns
CS pulse high width	t_{W2}	400	-	-	ns

6.1 Timing chart



1. Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.
2. Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.
3. The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.
4. If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.
5. If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data after the falling edge of CS pulse are valid data.
6. Serial block operates with the SCL clock.
7. Serial data can be accepted in the standby (power save) mode.

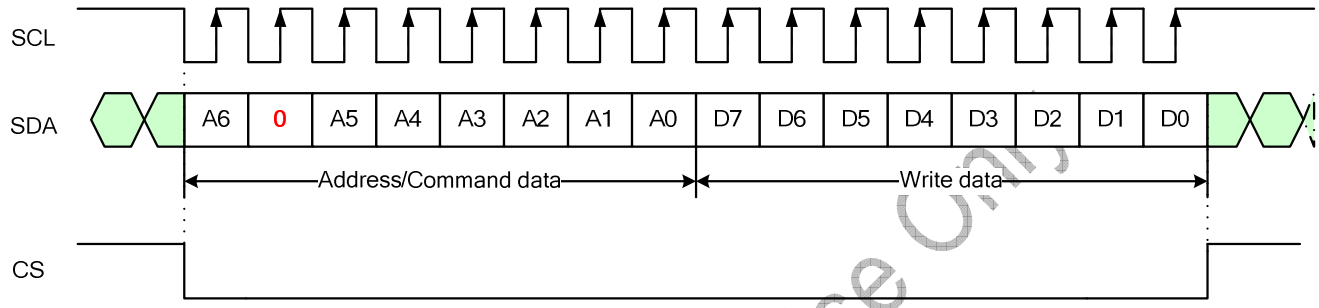
6.2 The configuration of serial data at SDA terminal is at below

MSB LSB

A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Address	R/W	Address						DATA							

R/W: Establishes the Read mode when set to '1', and the Write mode when set to '0'.

Write Mode:



6.3 Register table

No.	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	Y_CbCr (0)	x	x	x	x	x	x	x
R3	0	0	0	0	0	0	1	1	Brightness (40h)							
R4	0	0	0	0	0	1	0	0	x	SEL (000)			x	x	VDIR (1)	HDIR (1)
R5	0	0	0	0	0	1	0	1	x	GRB (1)	PFM_DUTY (011)			SHDB2 (1)	SHDB1 (1)	STB (0)
R6	0	0	0	0	0	1	1	0	HBLK_EN (0)	LED_Current (00)	VBLK (1Bh)					
R7	0	0	0	0	0	1	1	1	HBLK(28h)							
R8	0	0	0	0	1	0	0	0	BL_DRV(00)		DRV_FREQ (00)		x	x	x	x
R12	0	0	0	0	1	1	0	0	x	x	x	CbCr(0)	x	Vdpol(1)	Hdpol(1)	DCLKpol(0)
R13	0	0	0	0	1	1	0	1	CONTRAST_RGB(40h)							
R14	0	0	0	0	1	1	1	0	x	SUB_CONTRAST_R(40h)						
R15	0	0	0	0	1	1	1	1	x	SUB_BRIGHTNESS_R(40h)						
R16	0	0	0	1	0	0	0	0	x	SUB_CONTRAST_B(40h)						
R17	0	0	0	1	0	0	0	1	x	SUB_BRIGHTNESS_B(40h)						
R21	0	0	0	1	0	1	0	1	LED_ON_CYCLE(0111)				LED_ON_RATIO(1111)			
R27	0	0	0	1	1	0	1	1	VCOM_SEL(0)	VCOMH(3Ch)						
R28	0	0	0	1	1	1	0	0	x	VCOML(47h)						

Note: 1. “x” => please set to ‘0’.

6.4 Register description

R0:

No.	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
R0	0	0	0	0	0	0	0	0	Y_CbCr(0)	x	x	x	x	x	x	x

Y_CbCr: Y & CbCr exchange position (only valid for 8-bit input YUV)

	CbCr(R12[4])='0' (Default)	CbCr(R12[4])='1'
Y_CbCr='0' (Default)	Cb1 Y1 Cr1 Y2 Cb2 Y3 Cr2 Y4	Cr1 Y1 Cb1 Y2 Cr2 Y3 Cb2 Y4
Y_CbCr='1'	Y1 Cb1 Y2 Cr1 Y3 Cb2 Y4 Cr2	Y1 Cr1 Y2 Cb1 Y3 Cr2 Y4 Cb2

R3:

No.	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
R3	0	0	0	0	0	0	1	1	Brightness (40h)							

BRIGHTNESS: RGB bright level setting, setting accuracy: 1 step / bit

D7 ~ D0	Brightness gain
00h	Dark (-64)
40h(Default)	Center (0) (Default)
FFh	Bright (+191)

R4:

No.	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R4	0	0	0	0	0	1	0	0	x	SEL(000)			x	x	VDIR(1)	HDIR(1)

HDIR: Horizontal scan direction setting

HDIR	Function
0	Right to left scan
1	Left to right scan (Default)

VDIR: Vertical scan direction setting

VDIR	Function
0	Down to up scan
1	Up to down scan (Default)

SEL: Input data timing format selection

SEL			INPUT TIMING FORMAT
D6	D5	D4	
0	0	0	UPS051 (Default)
0	1	0	YUV 320 8-bit
0	1	1	YUV 320 16-bit
1	0	X	YUV 640 16-bit
1	1	X	YUV 720 16-bit

R5:

No	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R5	0	0	0	0	0	1	0	1	x	GRB(1)	PFM_DUTY(011)			SHDB2(1)	SHDB1(1)	STB(0)

STB: Standby (Power saving) mode setting

STB	Function
0	Standby mode (Default)
1	Normal operation

SHDB1: Shut down for back light power converter

SHDB1	Function
0	The back light power converter is off
1	The back light power converter is controlled by power on/off sequence (Default)

SHDB2: Shut down for VGH/VGL charge pump

SHDB2	Function
0	VGH/VGL charge pump is always off
1	VGH/VGL charge pump is controlled by power on/off sequence (Default)

PFM_DUTY: PFM duty cycle selection for back light power converter

PFM_DUTY			Function
D5	D4	D3	PFM duty cycle
0	0	0	93%
0	0	1	95%
0	1	0	65%
0	1	1	70%(Default)
1	0	0	75%
1	0	1	80%
1	1	0	85%
1	1	1	90%

GRB: Register reset setting

GRB	Function
0	Reset all registers to default value
1	Normal operation (Default)

When this command is sent to driver ic,it will be executed immediately

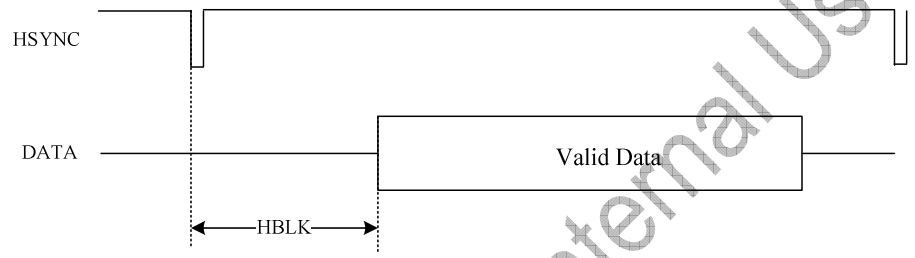
R6 & R7:

No	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R6	0	0	0	0	0	1	1	0	HBLK_EN(0)	LED_Current(00)		VBLK(1Bh)				
R7	0	0	0	0	0	1	1	1	HBLK(28h)							

HBLK_EN & HBLK: Horizontal blanking setting

HBLK_EN	HBLK(D7~D0)	HBLK	Unit	Remark
x	14h	20	DCLK(*)	UPS051
x	28h	40(Default)		
x	FFh	255		
0	-	40(fixed)	DCLK(*)	YUV320,YUV640, YUV720
1	14h ~ FFh	20 ~ 127	DCLK(*)	

*The frequency of DCLK is different under different input timing.



LED_CURRENT: adjust LED current

DC-DC feedback voltage

D6	D5	Feedback Threshold voltage
0	0	0.6V(20mA) (default)
0	1	0.75V(25mA)
1	0	0.45V(15mA)
1	1	0.3V(10mA)

R8:

No.	Register address								MSB		Register data					LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R8	0	0	0	0	1	0	0	0	BL_DRV(00)		DRV_FREQ(00)		x	x	x	x

DRV_FREQ: DRV signal frequency setting

DRV_FREQ		DRV signal frequency
D5	D4	
0	0	DCLK / 64 **(Default)**
0	1	DCLK / 64 / 2
1	0	DCLK / 64 / 3
1	1	DCLK / 64 / 4

BL_DRV: Backlight driving capability setting

D7	D6	BL_DRV capability
0	0	Normal capability (Default)
0	1	2 times the Normal capability
1	0	4 times the Normal capability
1	1	8 times the Normal capability

R12:

No.	Register address								MSB			Register data				LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R12	0	0	0	0	1	1	0	0	x	x	x	CbCr(0)	x	Vdpol(1)	Hdpol(1)	DCLKpol(0)

DCLKpol: DCLK polarity selection

DCLKpol	Function
0	Positive polarity (Default)
1	Negative polarity

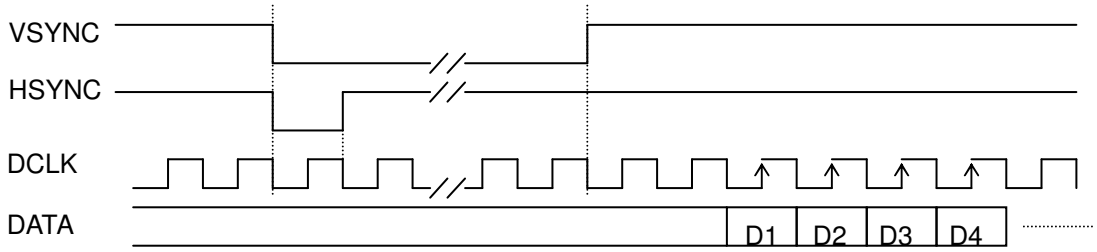
HDpol: HSYNC polarity selection

HDpol	Function
0	Positive polarity
1	Negative polarity (Default)

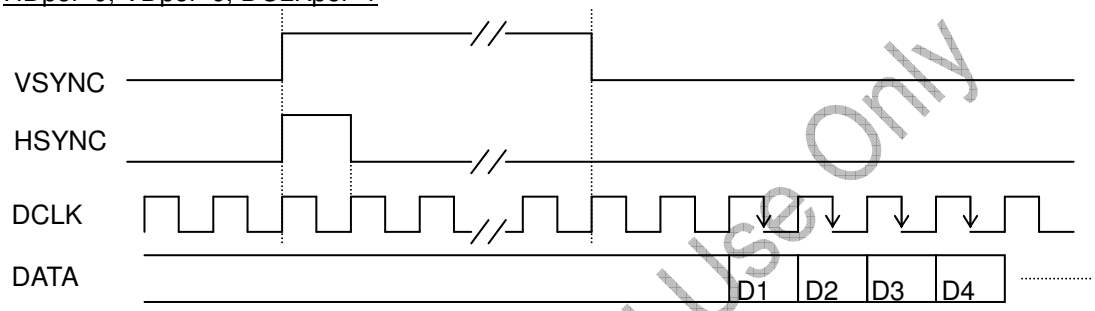
VDpol: VSYNC polarity selection

VDpol	Function
0	Positive polarity
1	Negative polarity (Default)

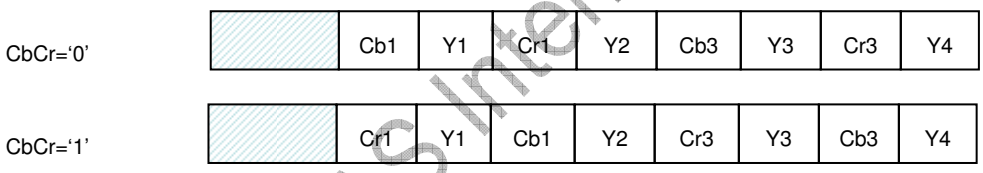
HDpol=1, VDpol=1, DCLKpol=0



HDpol=0, VDpol=0, DCLKpol=1



CbCr: Cb & Cr exchange position, (Please refer to the table of R0(Y_CbCr) for detail description)



R13:

No.	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R13	0	0	0	0	1	1	0	1	CONTRAST_RGB(40h)							

CONTRAST_RGB: RGB contrast level setting, the gain changes (1/64) / bit

D7 ~ D0	Contrast gain
00h	0
40h	1(Default)
FFh	3.984

R14~R17:

No.	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R14	0	0	0	0	1	1	1	0	x	SUB-CONTRAST_R(40h)						
R16	0	0	0	1	0	0	0	0	X	SUB-CONTRAST_B(40h)						

SUB-CONTRAST: R/B sub-contrast level setting, the gain changes (1/256) / bit

D6 ~ D0	Brightness gain
00h	0.75
40h	1(Default)
7Fh	1.246

No.	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R15	0	0	0	0	1	1	1	1	X	SUB-BRIGHTNESS_R(40h)						
R17	0	0	0	1	0	0	0	1	X	SUB-BRIGHTNESS_B(40h)						

SUB-BRIGHTNESS: R/B sub-bright level setting, setting accuracy : 1 step / bit

D6 ~ D0	Brightness gain
00h	Dark (-64)
40h	Center (0)(Default)
7Fh	Bright (+63)

R21:

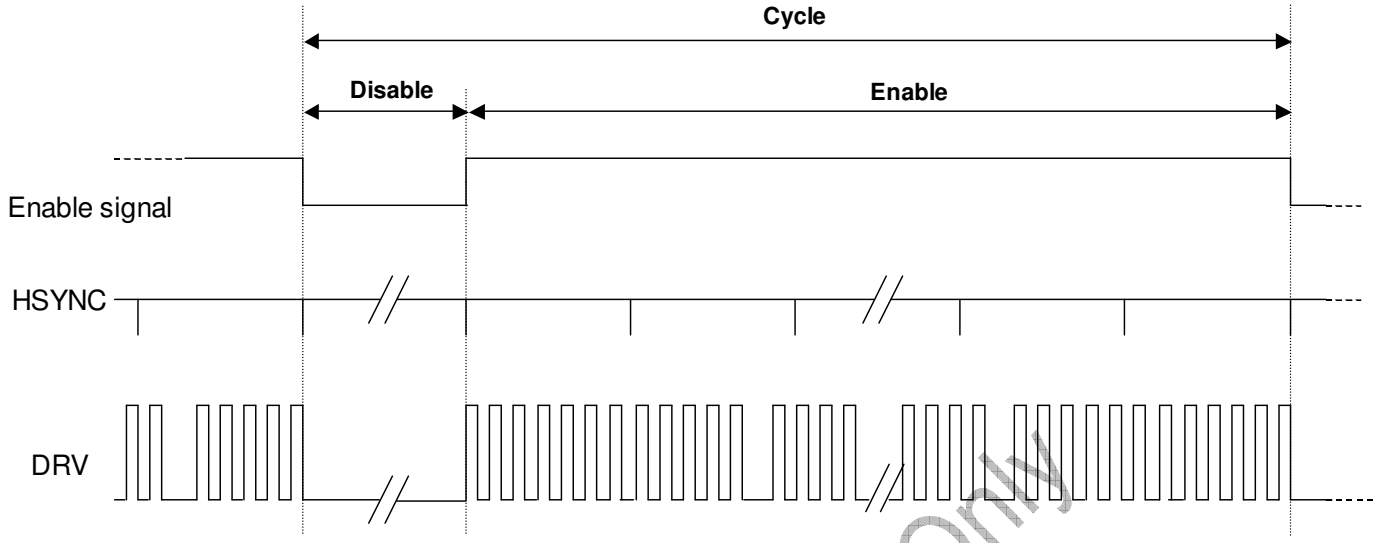
No.	Register address								MSB Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R21	0	0	0	1	0	1	0	1	LED_ON_CYCLE (0111)				LED_ON_RATIO (1111)			

LED_ON_RATIO: Set the active ratio of enable signal, and we can use it to adjust brightness of the LEDs.

LED_ON_RATIO				Value
D3	D2	D1	D0	
0	0	0	0	1/16
0	0	0	1	2/16
0	0	1	0	3/16
0	0	1	1	4/16
0	1	0	0	5/16
0	1	0	1	6/16
0	1	1	0	7/16
0	1	1	1	8/16
1	0	0	0	9/16
1	0	0	1	10/16
1	0	1	0	11/16
1	0	1	1	12/16
1	1	0	0	13/16
1	1	0	1	14/16
1	1	1	0	15/16
1	1	1	1	16/16(Default)

LED_ON_CYCLE : Set the cycle of enable signal , and we can use it to adjust brightness of the LEDs.

LED_ON_CYCLE				Value
D7	D6	D5	D4	
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8(Default)
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16



$16 * LED\_ON\_CYCLE = LED\_ON\_CYCLE * (LED\_ON\_RATIO * 16) + LED\_ON\_CYCLE * (16 - LED\_ON\_RATIO * 16)$

(Cycle) **(Enable)** **(Disable)** Unit : HSYNC

for example:
LED_ON_RATIO is **"1001"**, and LED_ON_CYCLE is **"0111"**, then:
Cycle = 16 * **8** = 128(HSYNC)
Enable = **8** * ((**10**/**16**) * 16) = 80(HSYNC)
Disable = **8** * (16-(**10**/**16**) * 16) = 48(HSYNC) ➔62.5% on

R27

No.	Register address								MSB Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R22	0	0	0	1	1	0	1	1	VCOMH_SEL(0)	VCOMH(3Ch)						

R27[7]-VCOMH_SEL=0 (for LOW VCOMH)

R27[6:0]-VCOMH:VCOMH level adjustment(1 step:20mv)

VCOMH level	(Unit:V)
00h	1.5v
…	step:20mV
3Ch(Default)	2.7(Default)
…	…
7Bh	3.96V
7Ch	3.97V
7Dh	3.98V
7Eh	4.00V
7Fh	4.02V

R27[7]-VCOMH_SEL=1 (for High VCOMH)

VCOMH level	(Unit:V)
00h	2.68v
…	step:20mV
7Bh	5.12V
7Ch	5.14V
7Dh	5.16V
7Eh	5.18V
7Fh	5.2V

R28

No.	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R22	0	0	0	1	1	1	0	0	x	VCOML(47h)						

R28[6:0]-VCOML:VCOML level adjustment(1 step:20mv)

VCOMH level	(Unit:V)
00h	-0.1V
01h	-0.12V
02h	-0.14V
03h	-0.15V
04h	-0.16V
…	step:20mV
47h	-1.5V(Default)
…	…
7Fh	-2V

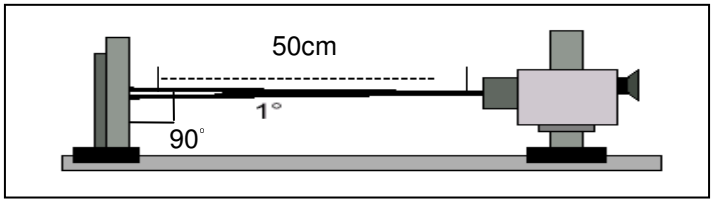
C. Optical specification (Note 1, Note 2, Note 3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time							Note 4
Rise	Tr	θ =0°	-	10	40	ms	
Fall	Tf		-	25	50	ms	
Contrast ratio	CR	At optimized viewing angle	400	700	-		Note 5
Viewing angle							Note 6
Top	φ_T	CR≧10	40	50	-	deg.	
Bottom	φ_B		50	60	-		
Left	φ_L		50	60	-		
Right	φ_R		50	60	-		
Brightness *	Y_L	θ =0°	400	550	-	cd/m^2	Note 7,8
Luminance Uniformity			70	75		%	Note 9
Color Chromaticity	x	θ =0°	0.252	0.302	0.352		
	y	θ =0°	0.274	0.324	0.374		
	Rx	θ =0°	0.521	0.571	0.621		
	Ry	θ =0°	0.286	0.336	0.386		
	Gx	θ =0°	0.287	0.337	0.387		
	Gy	θ =0°	0.500	0.550	0.600		
	Bx	θ =0°	0.103	0.153	0.203		
	By	θ =0°	0.075	0.125	0.175		

Note 1. Ambient temperature =25℃.

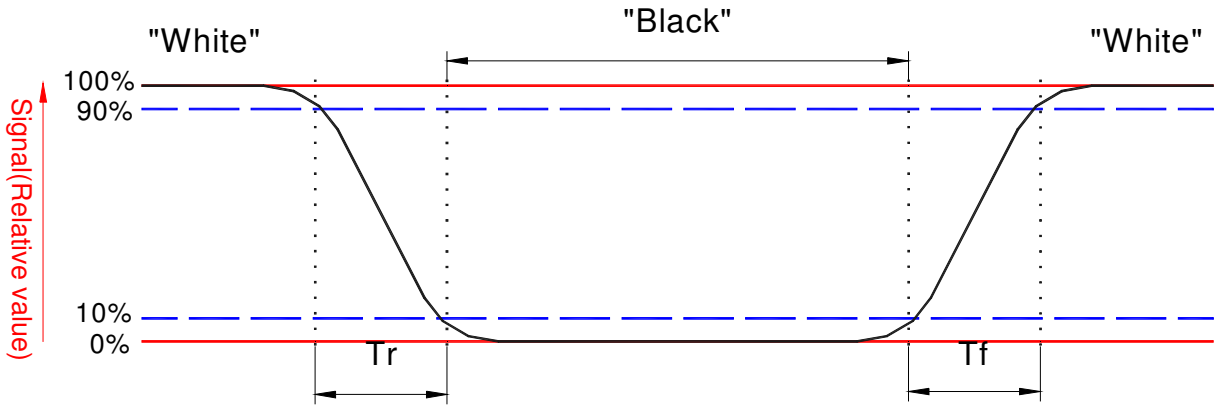
Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-5A, after 10 minutes operation.



Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



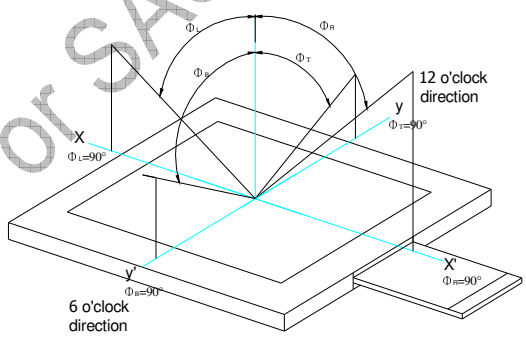
Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

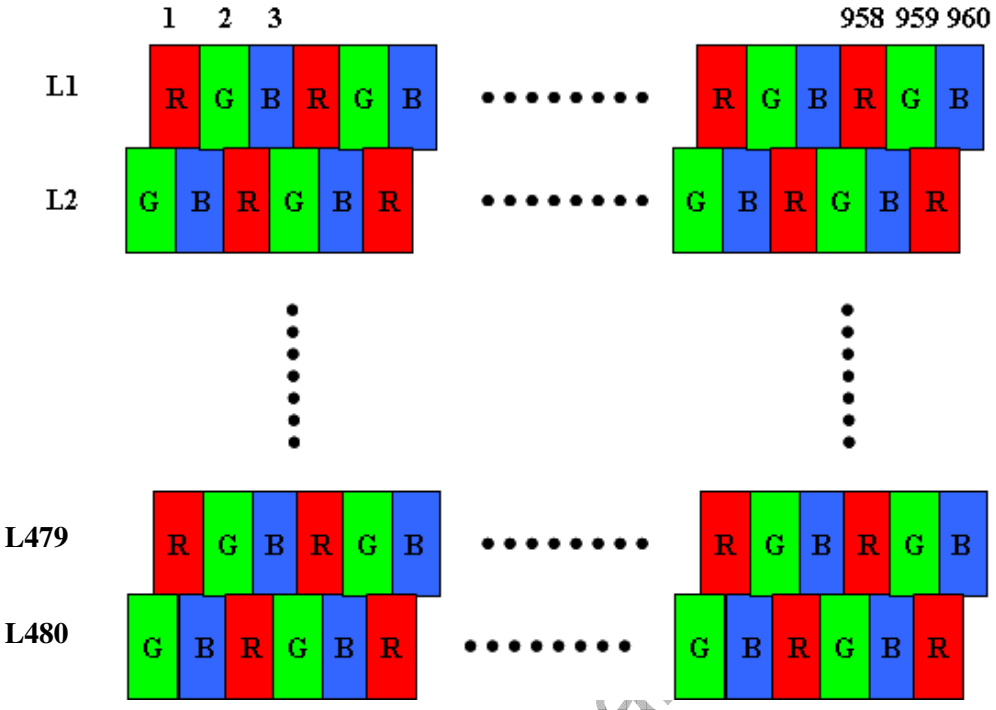
Note 6. Definition of viewing angle:

Refer to figure as below.



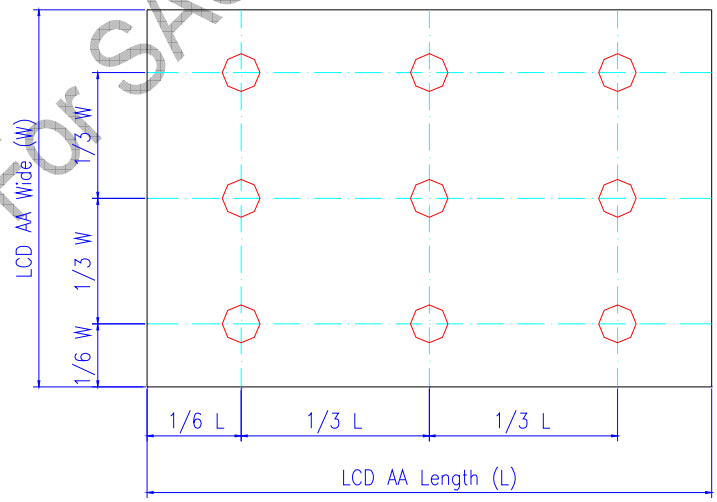
Note 7. Measured at the center area of the panel in gray level 255.

Note 8. Color Filter Arrangement



Note 9. Definition of luminance uniformity

$$\text{Luminance Uniformity} = \frac{\text{Min. Brightness of nine point}}{\text{Max. Brightness of nine point}}$$



D. Reliability test items

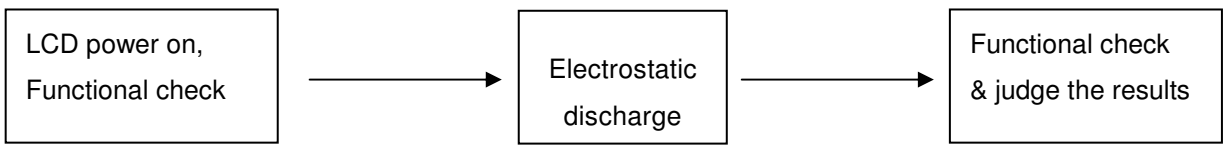
No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 70℃ 240Hrs	Note 1
2	Low temperature storage	Ta= -25℃ 240Hrs	
3	High temperature operation	Ta= 60℃ 240Hrs	
4	Low temperature operation	Ta= -10℃ 240Hrs	
5	High temperature and high humidity	Ta= 60℃. 90% RH 240Hrs	Operation
6	Heat shock	-25℃~60℃/50 cycle 2Hrs/cycle	Non-operation
7	Electrostatic discharge	Air-mode : +/- 8kV Contact-mode : +/- 4kV	Note.2, Note 3
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
9	Mechanical shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
10	Vibration (with carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note 1. (for test item 1 to 6) Ta: Ambient temperature

Note 2. (for test item 1 to 6) Test method: check with recovery time 2hrs in the laboratory environment

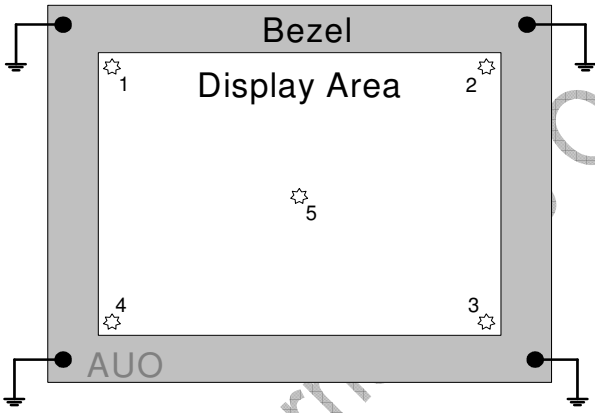
Note 3. Judged by the on/off testing results of AUO's standard w/o functional fail.

Note 4. ESD Testing Flow as the below



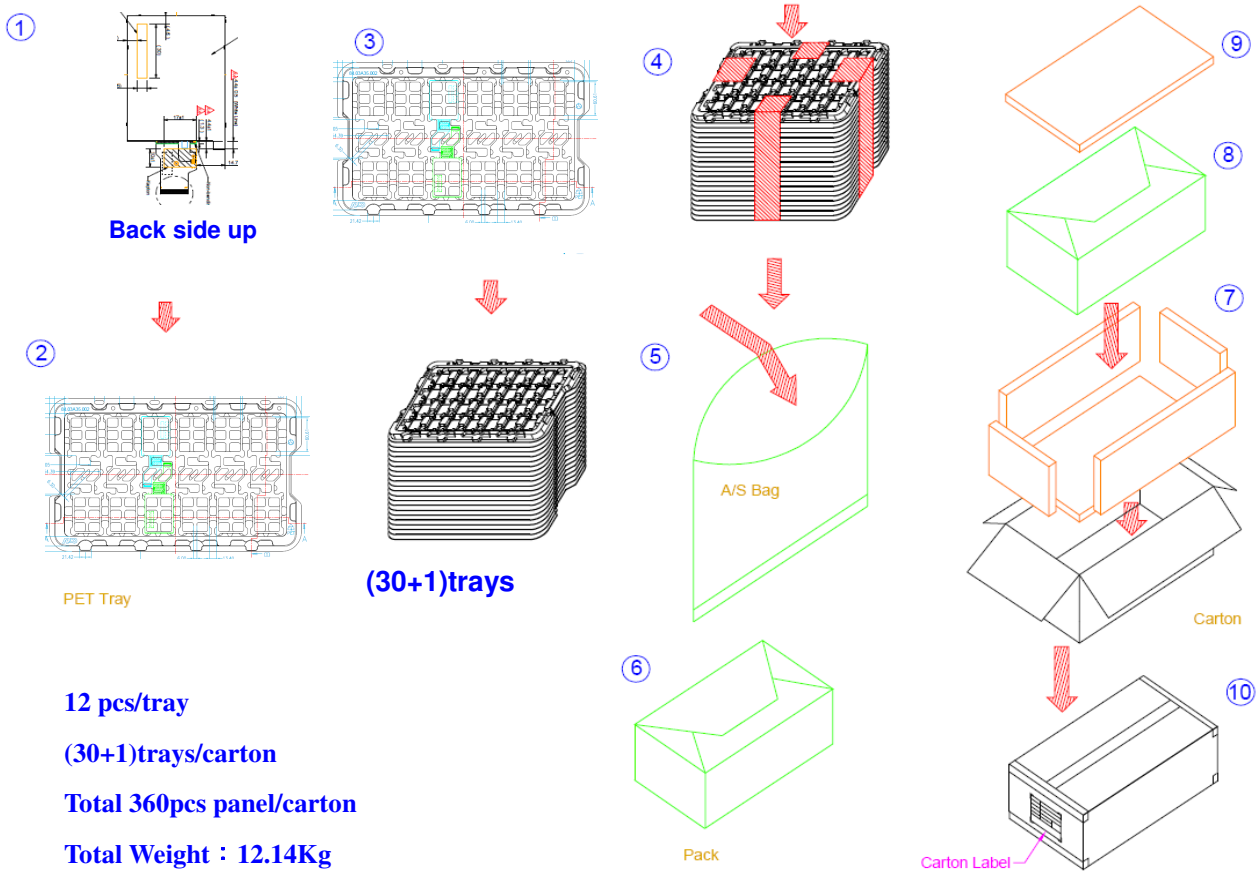
Note 5. ESD testing method.

1. Ambient: 24~26℃, 56~65%RH
2. Instruments:NoisekenESS-2000,
3. Operation System: “CX40FL-B” and adapter “A030JTN01.1”
4. Test Mode: Operating mode, test pattern: colorbar+8Gray scale
5. Test Method:
   a. Contact Discharge:, 150pF(330Ω) 1sec, 5 points, 10 times/point
   b. Air Discharge:, 150pF(330Ω) 1sec, 5 points, 10 times/point
6. Test point:



7. The metal casing is connected to power supply ground (0V) at four corners.
8. All register commands are repeating transfer.

E. Packing form



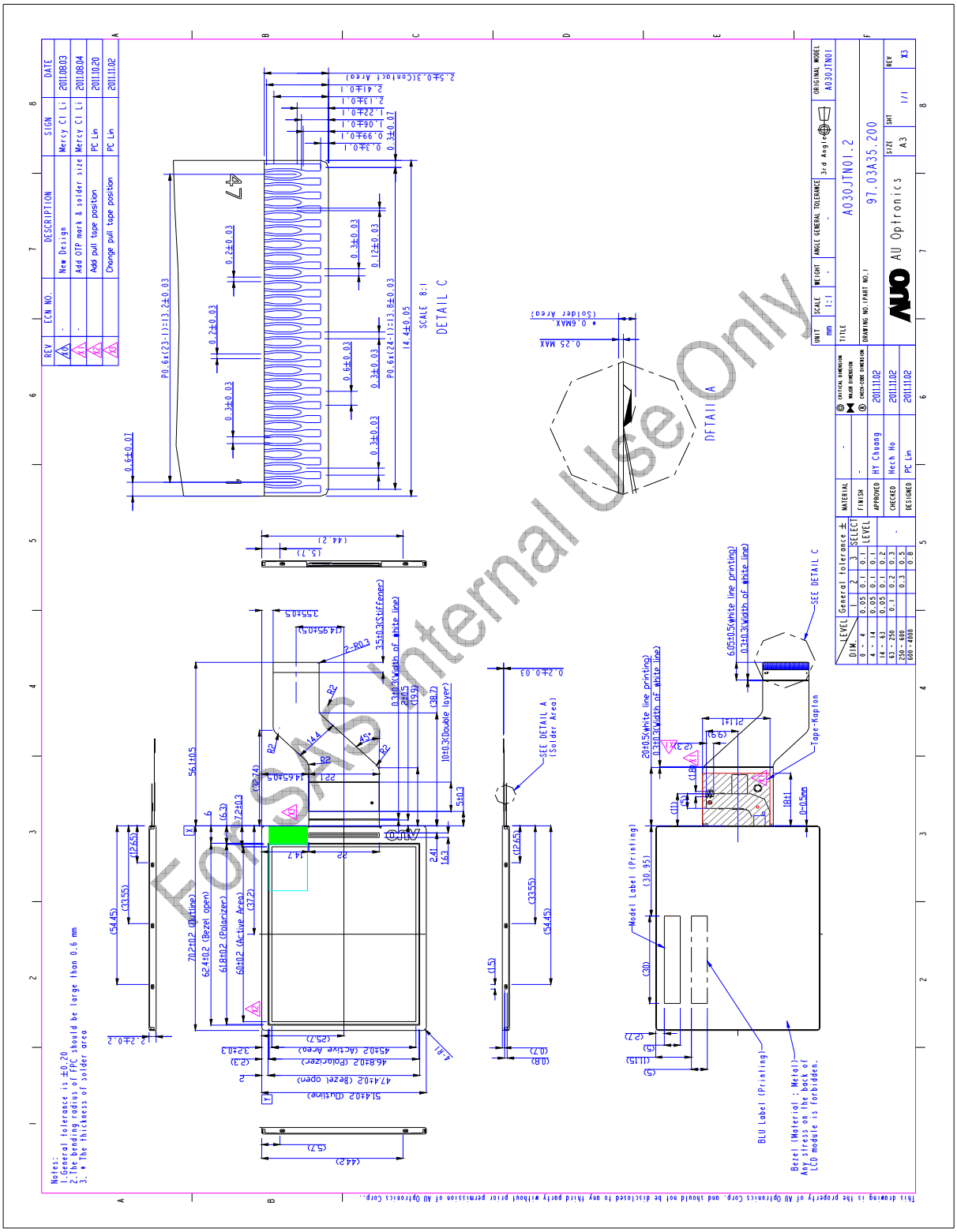
12 pcs/tray

(30+1)trays/carton

Total 360pcs panel/carton

Total Weight：12.14Kg

F. Dimension



Note: OTP land and BL Soldering are insulated by the Kapton tape

G. Application note

1. Input Data Timing

In UPS051 input format, the conversion of image data to display dots is controled by the user.

For UPS051 timing, the module accpet one dot video data at the rising edge of DCLK, and display them one dot by one dot. Therefore the input data timing is different according to different panel resolutions and scan directions. Refer to the AC Timing of UPS051 part, you can use the typ. value for a typical case.

Because of delta color filter arrangement, the RGB data sequence for even and odd lines are different based on scan direction. For the RGB sequence, see Fig. 11.

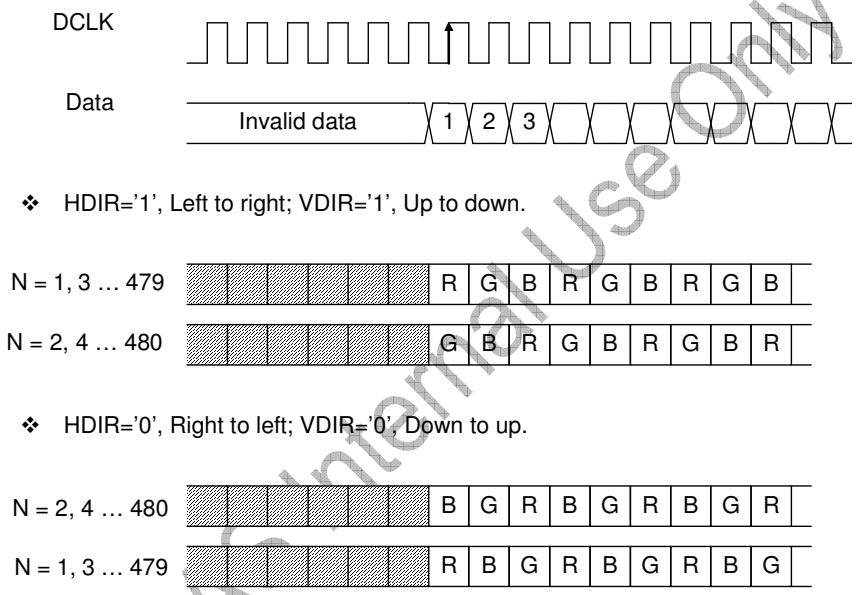


Fig. 11 UPS051 Input RGB sequence

For the color filter arrangement, see Fig. 12.

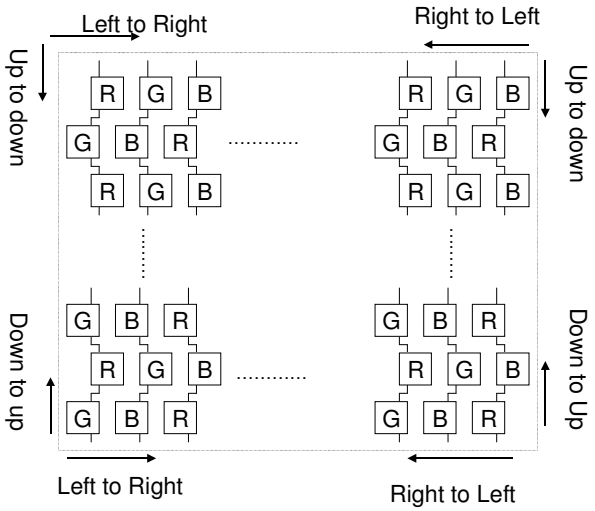
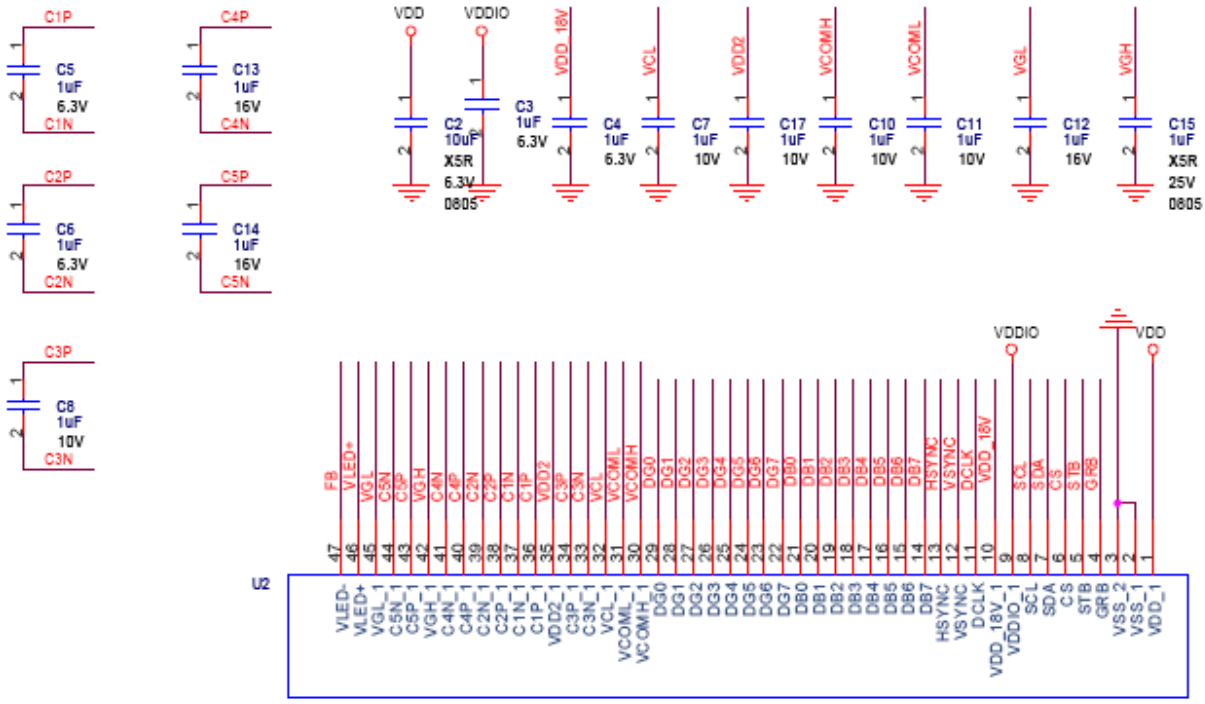


Fig. 12 Color filter arrangement

2. Application circuit

2.1 With external LED driver circuit



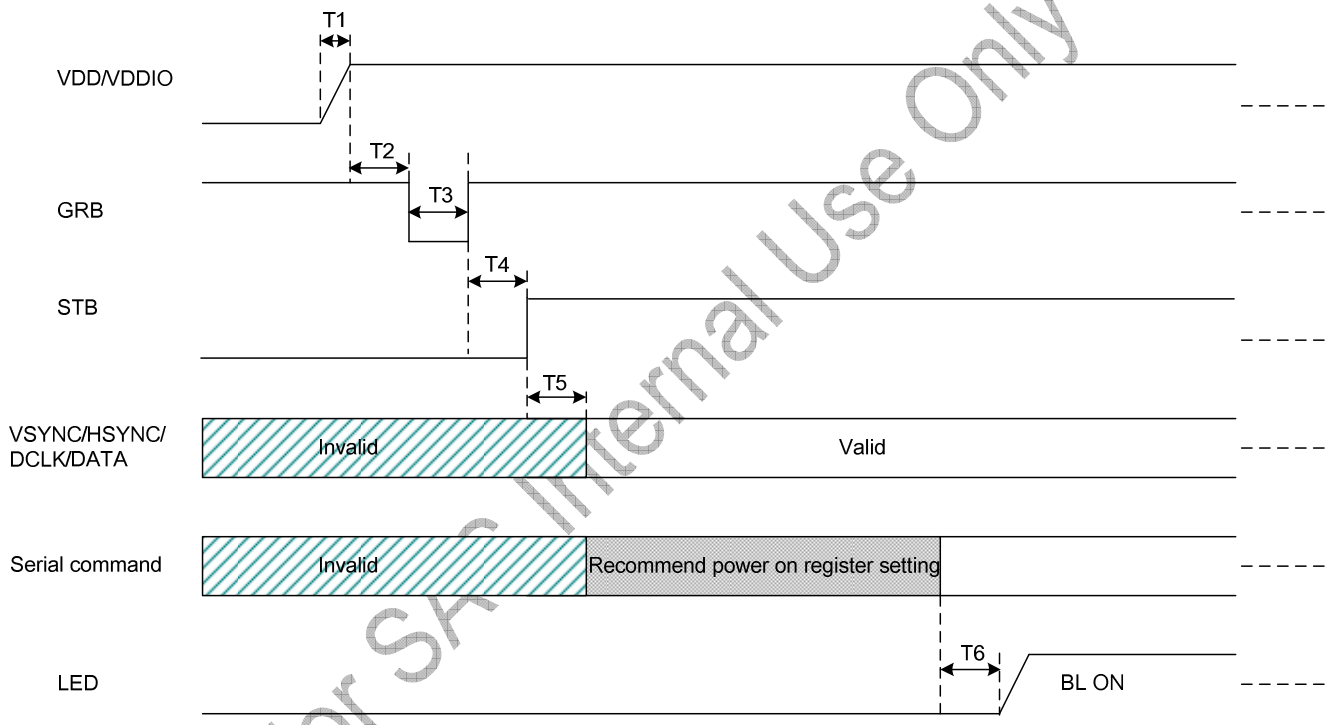
Note1: Use external LED driver must set R5[1](SHDB1)= ‘0’.

3. Power on/off sequence

The register setting of standby mode disabling / enabling is used to control the build-in power on / off sequence.

3.1 Power on (Standby Disabling)

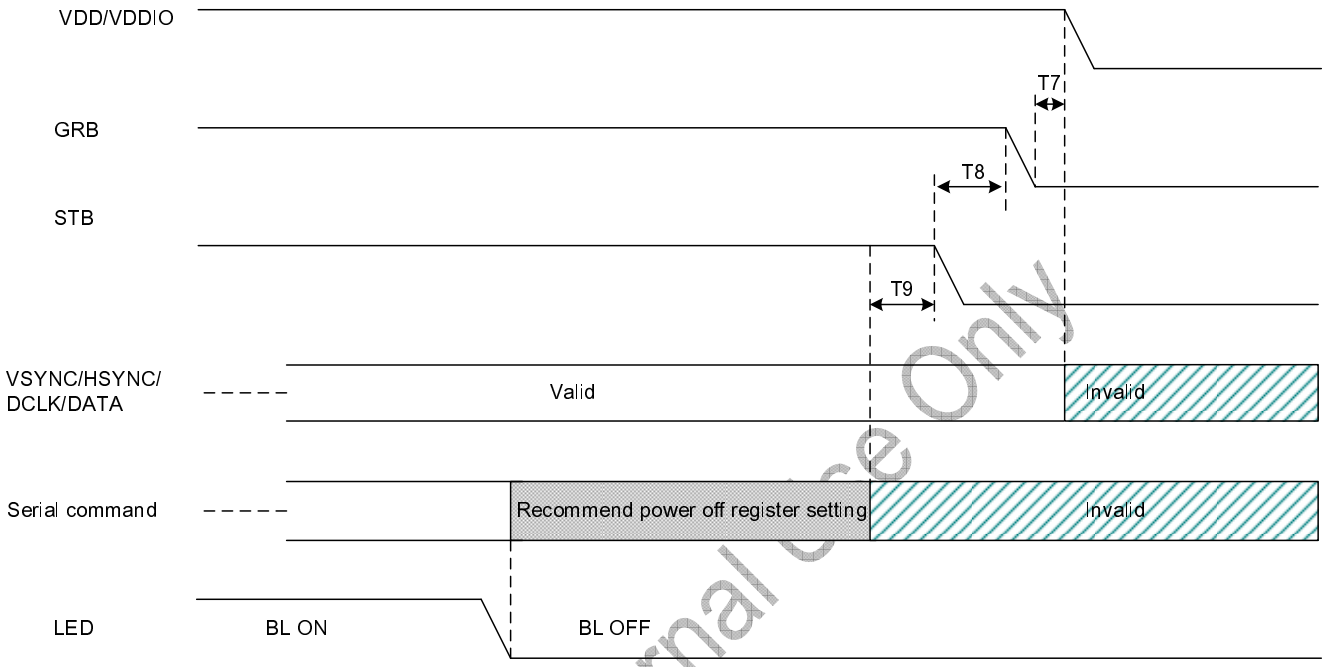
After VDD power on, VSYNC/HSYNC/DCLK/DATA can be input, and serial control interface is also operational. The LCD driver is in default standby mode after VDD power-on, and setting register STB to '1' to disable the standby mode is required for normal operation. When the standby mode is disabled, a build-in power on sequence is started.



T1> 10 us, T2> 1 ms, T3> 100 us, T4> 2 ms, T5> 2 ms, T6> 170 ms

3.2 Power off (Standby Enabling)

When the register STB is set to '0' to enable standby mode, a build-in power off sequence is started.



T7> 1 ms, T8> 120 ms, T9> 1 ms

4. Recommended power on/off serial command settings

a. Recommended Power On Register Setting with external LED driver

Number	Command(Binary)
1	00000101 00110100
Delay 3ms	
2	00000101 01110100
3	10010101 00000000
4	00011011 10111001
5	00011100 01001011
6	10011010 00000000
7	00000101 01110101

b. Recommended Power Off Register Setting

Number	Command(Binary)
1	00000101 01110000

Note: The recommended power on/ power off serial command setting needed to be applied into system