



**SPECIFICATION  
FOR  
M+CTP Module  
KD024QVRMA038-C009A**

MODULE:	KD024QVRMA038-C009A
CUSTOMER:	

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Long Time supply支持小量  
NO MOQ品种齐全  
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## Revision History

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### \* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 2.4''TFT-LCD contains 240X320 pixels, and can display up to 65K/262K colors.

### \* Features

- Low Input Voltage: 3.3V(TYP)
- Display Colors of TFT LCD: 65K/262K colors
- TFT Interface: 8/9/16/18Bit MCU Interface
  - 3/4SPI+16/18Bit RGB Interface
  - 3-line/4-line Serial Interface

CTP Interface: IIC

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	36.72(H) *48.96(V) (2.4inch )	mm	-
CTP View area	37.32(H)*49.56(V)	mm	
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	240(RGB)*320	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.153 (H) x 0.153 (V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ST7789V	-	-
CTP Driver IC	FT6336G		
Display mode	Transflective /Normally Black	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

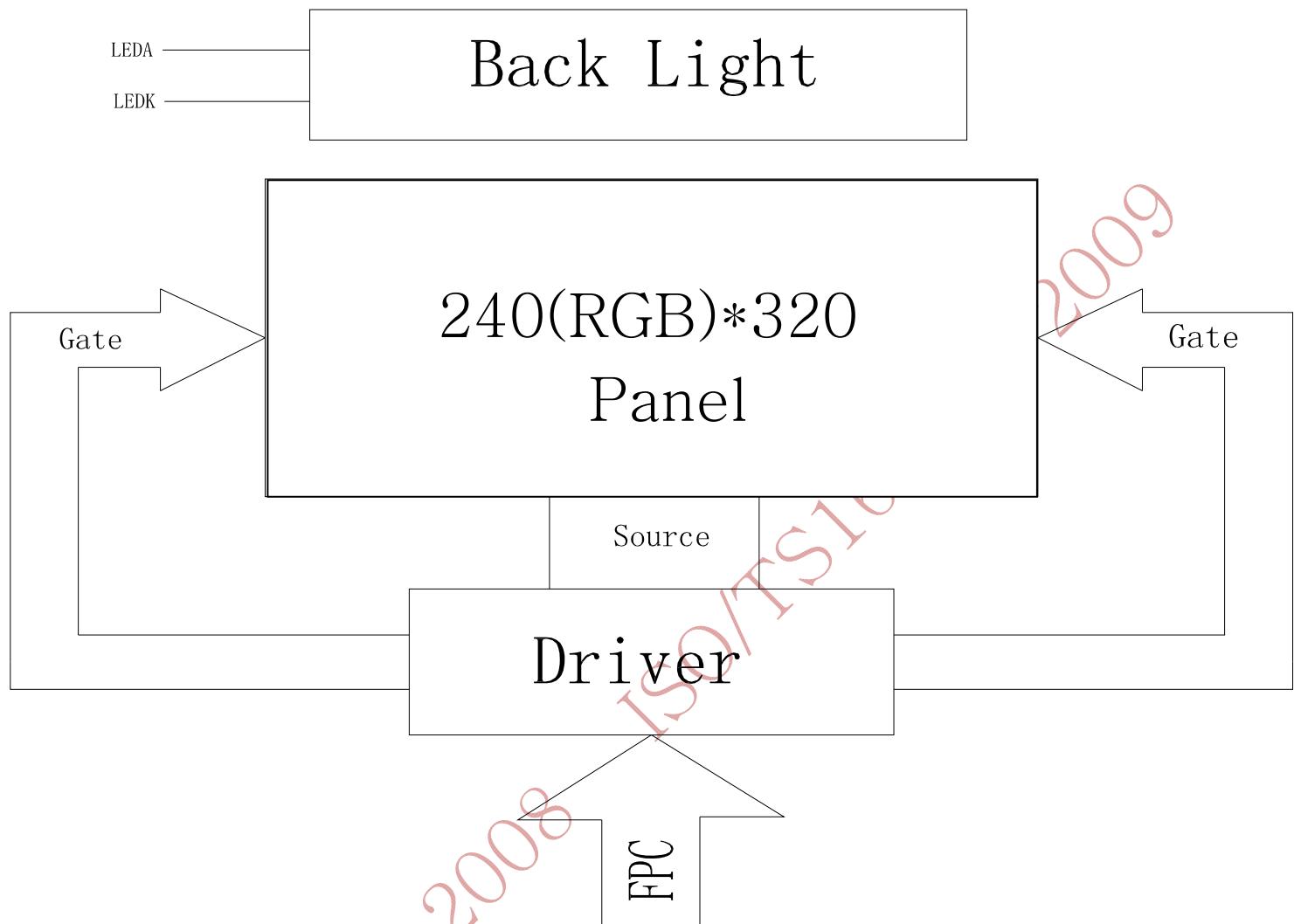
### \* Mechanical Information

Item	Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	42.92		mm	-
	Vertical(V)	60.26		mm	-
	Depth(D)	4.20		mm	-
Weight		TBD		g	-

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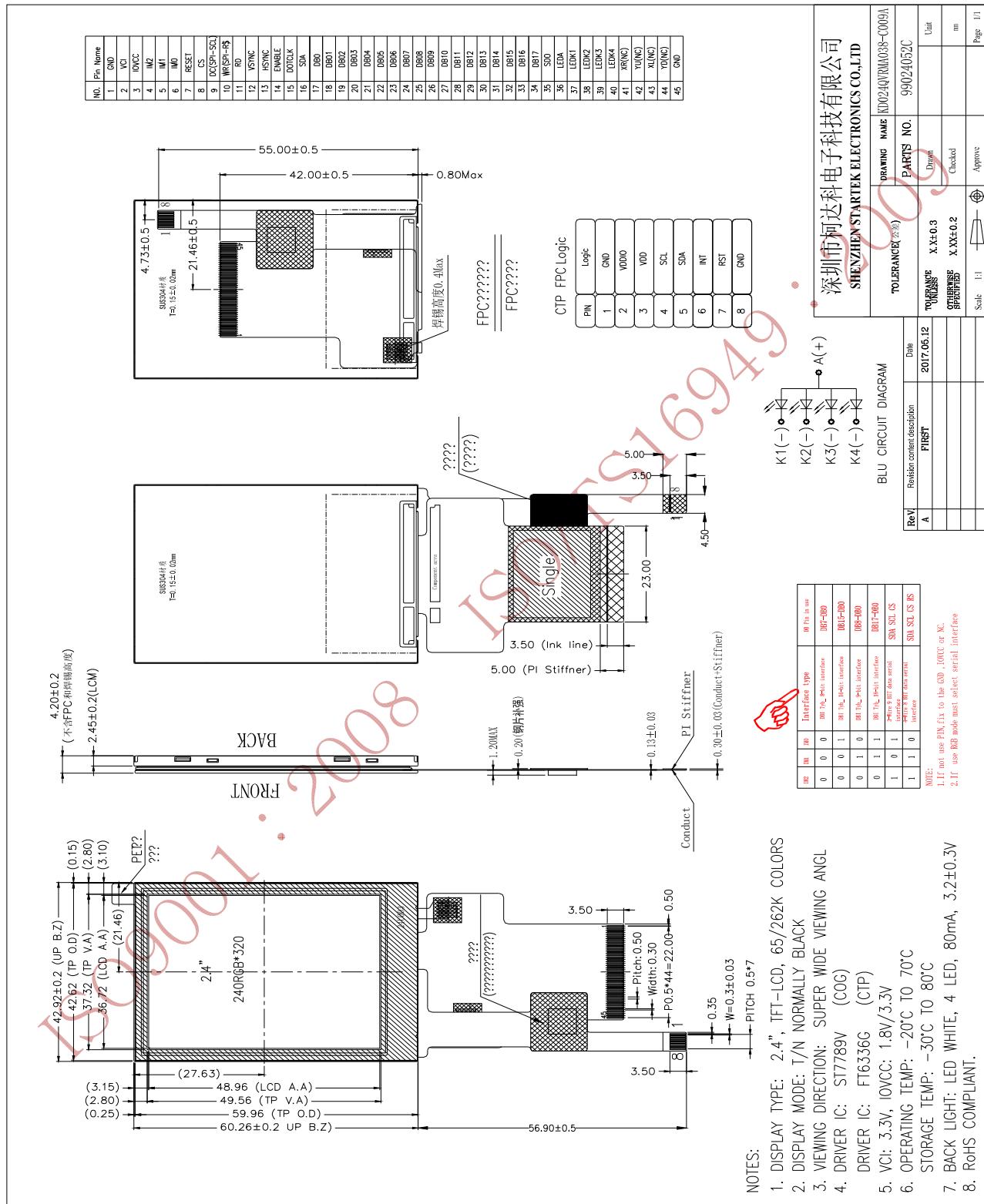


## 1. Block Diagram





## 2. Outline dimension





### 3. Input terminal Pin Assignment

#### 3.1 TFT

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VCI	Supply voltage(3.3V).	P
3	IOVCC	Supply voltage(1.65-3.3V).	P
4	IM2	MPU Parallel interface bus and serial interface select If use RGB Interface must select serial interface.	I
5	IM1		I
6	IM0	Fix this pin at VCI and GND.	I
7	RESET	This signal will reset the device and must be applied to properly initialize the chip.	I
8	CS	Chip select input pin ("Low" enable). fix this pin at VCI or GND when not in use.	I
9	DC(SPI-SCL)	-Display data/command selection pin in parallel interface. -This pin is used to be serial interface clock. DC='1': display data or parameter. DC='0': command data. -If not used, please fix this pin at VDDI or DGND.	I
10	WR(SPI-RS)	-Write enable in MCU parallel interface. - Display data/command selection pin in 4-line serial interface. - Second Data lane in 2 data lane serial interface. -If not used, please fix this pin at VDDI or DGND.	I
11	RD	Serves as a read signal and MCU read data at the rising edge. fix this pin at VCI or GND when not in use.	I
12	VSYNC	Frame synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
13	HSYNC	Line synchronizing signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
14	ENABLE	Data enable signal for RGB interface operation. fix this pin at VCI or GND when not in use.	I
15	DOTCLK	Dot clock signal for RGB interface operation. Fix this pin at VCI or GND when not in use.	I

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16	SDA	Serial input signal. The data is latched on the rising edge of the SCL signal. fix this pin at VCI or GND when not in use.	I
17-34	DB0-DB17	18-bit parallel bi-directional data bus for MCU system and RGB interface mode . Fix to GND level when not in use	I/O
35	SDO	SPI interface output pin. -The data is output on the falling edge of the SCL signal. -If not used, let this pin open.	O
36	LEDA	Anode pin of backlight	P
37	LEDK1	Cathode pin OF backlight	P
38	LEDK2	Cathode pin OF backlight	P
39	LEDK3	Cathode pin OF backlight	P
40	LEDK4	Cathode pin OF backlight	P
41	XR(NC)	Touch panel Right Glass Terminal	A/D
42	YU(NC)	Touch panel Bottom Film Terminal	A/D
43	XL(NC)	Touch panel LIFT Glass Terminal	A/D
44	YD(NC)	Touch panel Top Film Terminal	A/D
45	GND	Ground.	P

### 3.2 CTP

No.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	VDDIO	Supply voltage.	P
3	VDD	Supply voltage.	P
4	SCL	I2C clock input.	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host.	I
7	RST	External Reset, Low is active.	I
8	GND	Ground.	P

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## 4. LCD Optical Characteristics

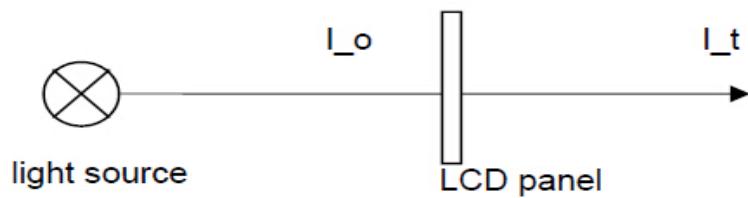
### 4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	$\Theta=0$	--	300	--		
Response time	Rising	$T_{R+F}$	Normal viewing angle	--	25	--	msec	ISO9001:2008
	Falling							
Color Filter Chromacity	White	$W_X$	CR>10	0.250	0.290	0.330		ISO9001:2008
		$W_Y$		0.278	0.318	0.358		
	Red	$R_X$		0.451	0.471	0.491		
		$R_Y$		0.299	0.319	0.339		
	Green	$G_X$		0.299	0.319	0.339		
		$G_Y$		0.495	0.515	0.535		
	Blue	$B_X$		0.147	0.167	0.187		
		$B_Y$		0.106	0.126	0.146		
Viewing angle	Hor.	$\Theta_L$		--	80	--		ISO9001:2008
		$\Theta_R$		--	80	--		
	Ver.	$\Theta_U$		--	80	--		
		$\Theta_D$		--	80	--		
Option View Direction		...	ALL					



### [1] Transmittance (T%)

The transmittance of the panel including polarizers is measured with electrical driving.



The Transmittance is defined as:

$$Tr = \frac{I_t}{I_o} \times 100\%$$

here,

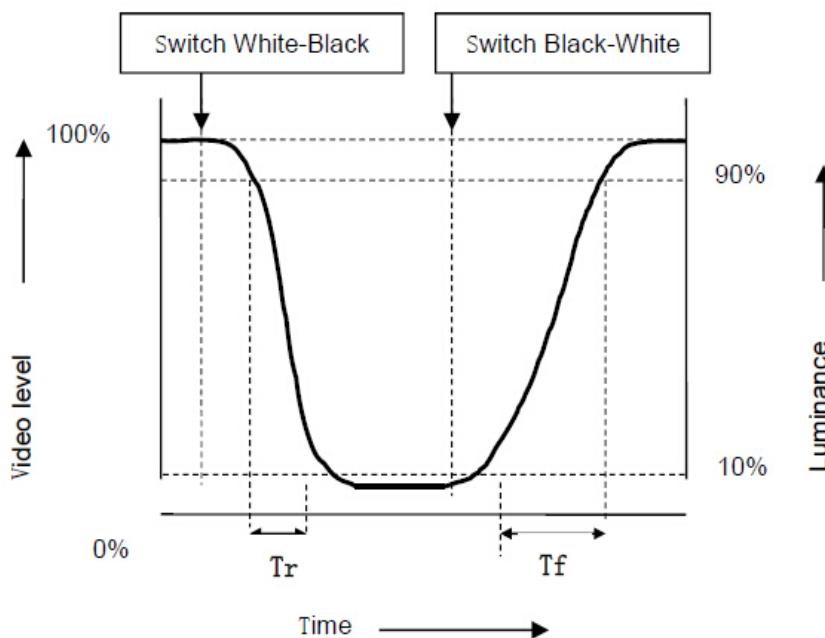
$I_o$ : the brightness of the light source.

$I_t$  : the brightness after panel transmission.



### [2] Response Time(Tr、 Tf)

The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



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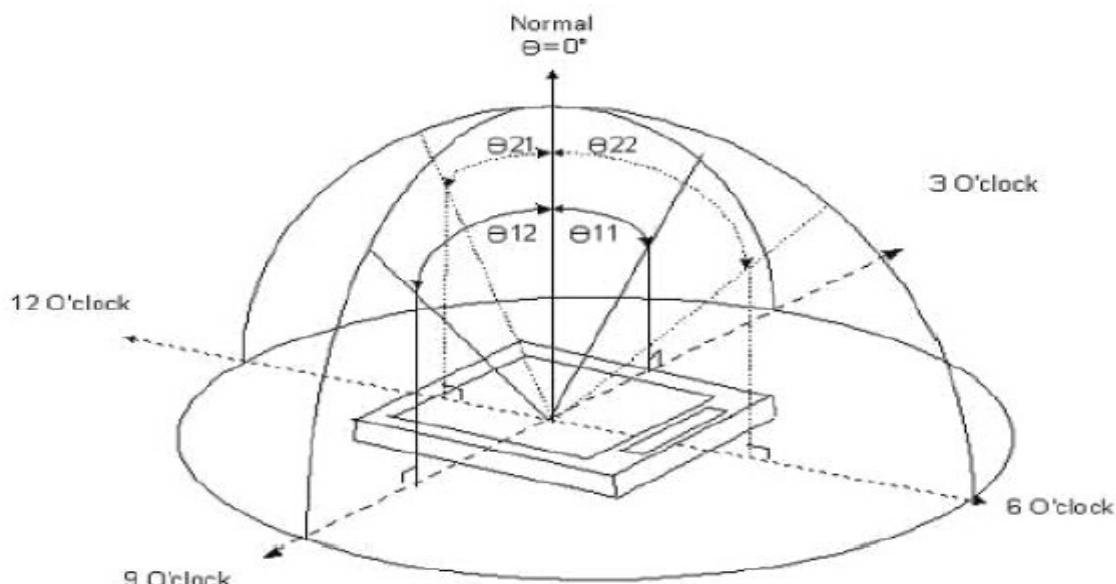
### [3] Contrast ratio (Cr)

The contrast ratio (Cr), measured on a module, is the ratio between the luminance ( $L_w$ ) in a full white area ( $R=G=B=1$ ) and the luminance ( $L_d$ ) in a dark area ( $R=G=B=0$ ):

$$Cr = \frac{L_w}{L_d}$$

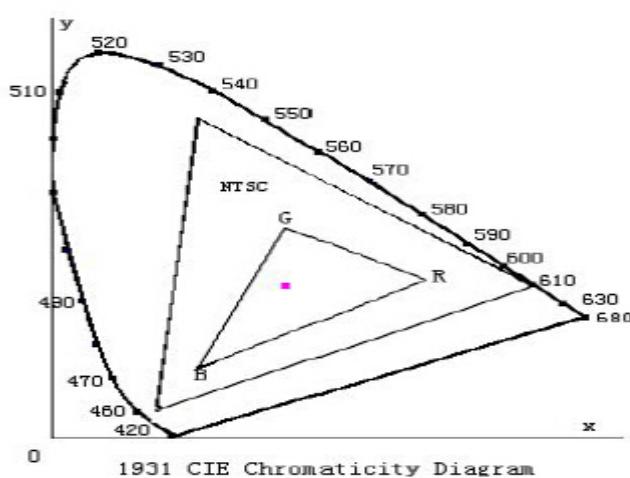
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### [4] Viewing angle diagram



### [5] Definition of color gamut

Measuring machine:CFT-01. NTSC'S Primaries: R(x,y,Y)、G(x,y,Y)、B(x,y,Y).



**Fig. 1931 CIE chromaticity diagram**

$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

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## 5. Electrical Characteristics

### 5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	V <sub>C1</sub>	-0.3	4.6	V
Digital Interface Supply Voltage	V <sub>IOVCC</sub>	-0.3	4.6	
Operating temperature	T <sub>OP</sub>	-20	+70	°C
Storage temperature	T <sub>ST</sub>	-30	+80	°C

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

### 5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	V <sub>C1</sub>	2.4	2.75	3.3	V	
Digital Interface Supply Voltage	V <sub>IOVCC</sub>	1.65	1.8	3.3		
Normal mode Current consumption	I <sub>DD</sub>	--	10.2	--	mA	
Level input voltage	V <sub>IH</sub>	0.7V <sub>DIO</sub>		V <sub>DIO</sub>	V	
	V <sub>IL</sub>	GND		0.3V <sub>DIO</sub>	V	
Level output voltage	V <sub>OH</sub>	0.8V <sub>DIO</sub>		V <sub>DIO</sub>	V	
	V <sub>OL</sub>	GND		0.2V <sub>DIO</sub>	V	

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### 5.3 LED Backlight Characteristics

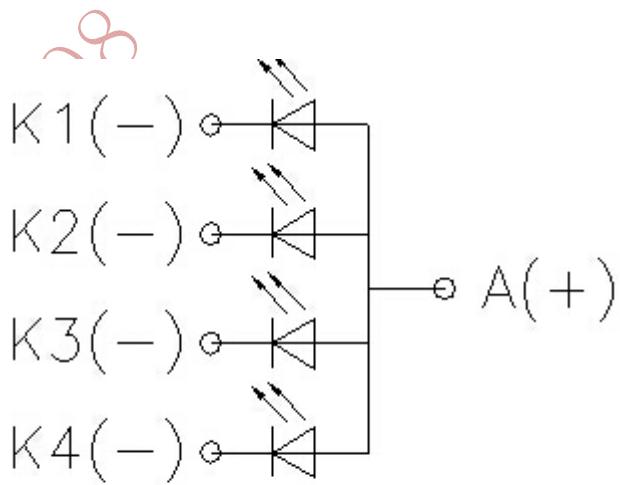
The back-light system is edge-lighting type with 4 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I <sub>F</sub>	60	80	--	mA	
Forward Voltage	V <sub>F</sub>	--	3.2	--	V	
LCM Luminance	L <sub>v</sub>	100	150	--	cd/m <sup>2</sup>	Note3
SLED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	Avg	80	--	--	%	Note3

SNote (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

T<sub>a</sub>=25±3 °C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at T<sub>a</sub>=25°C and IL=80mA. The LED lifetime could be decreased if operating IL is larger than 80mA. The constant current driving method is suggested.

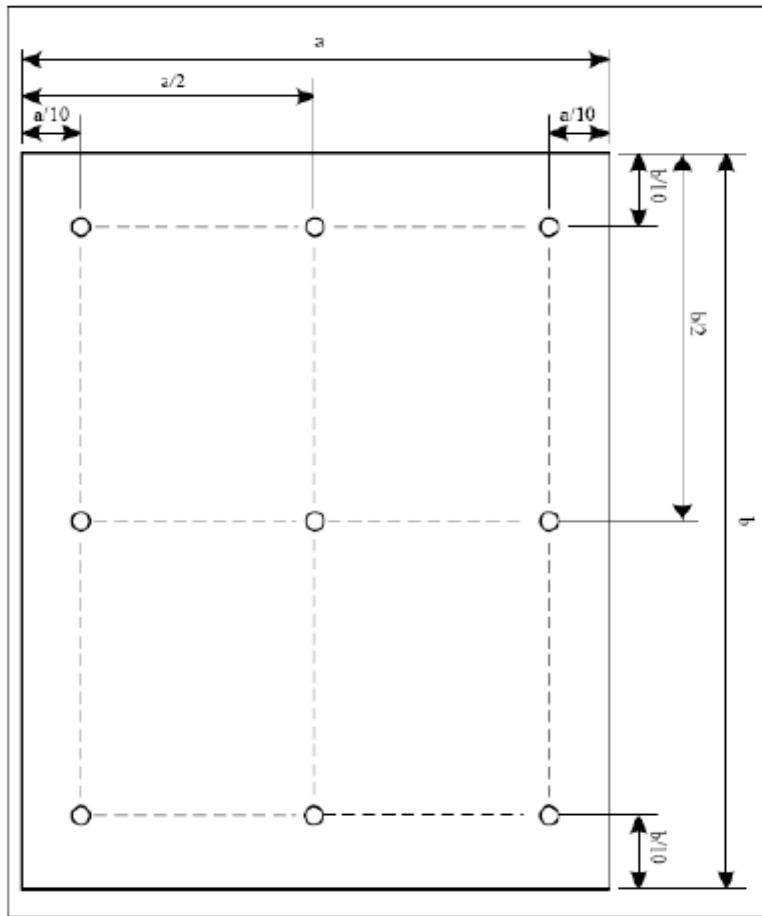


BLU CIRCUIT DIAGRAM

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NOTE 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

ISO9001

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## 6. AC Characteristic

### 6.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

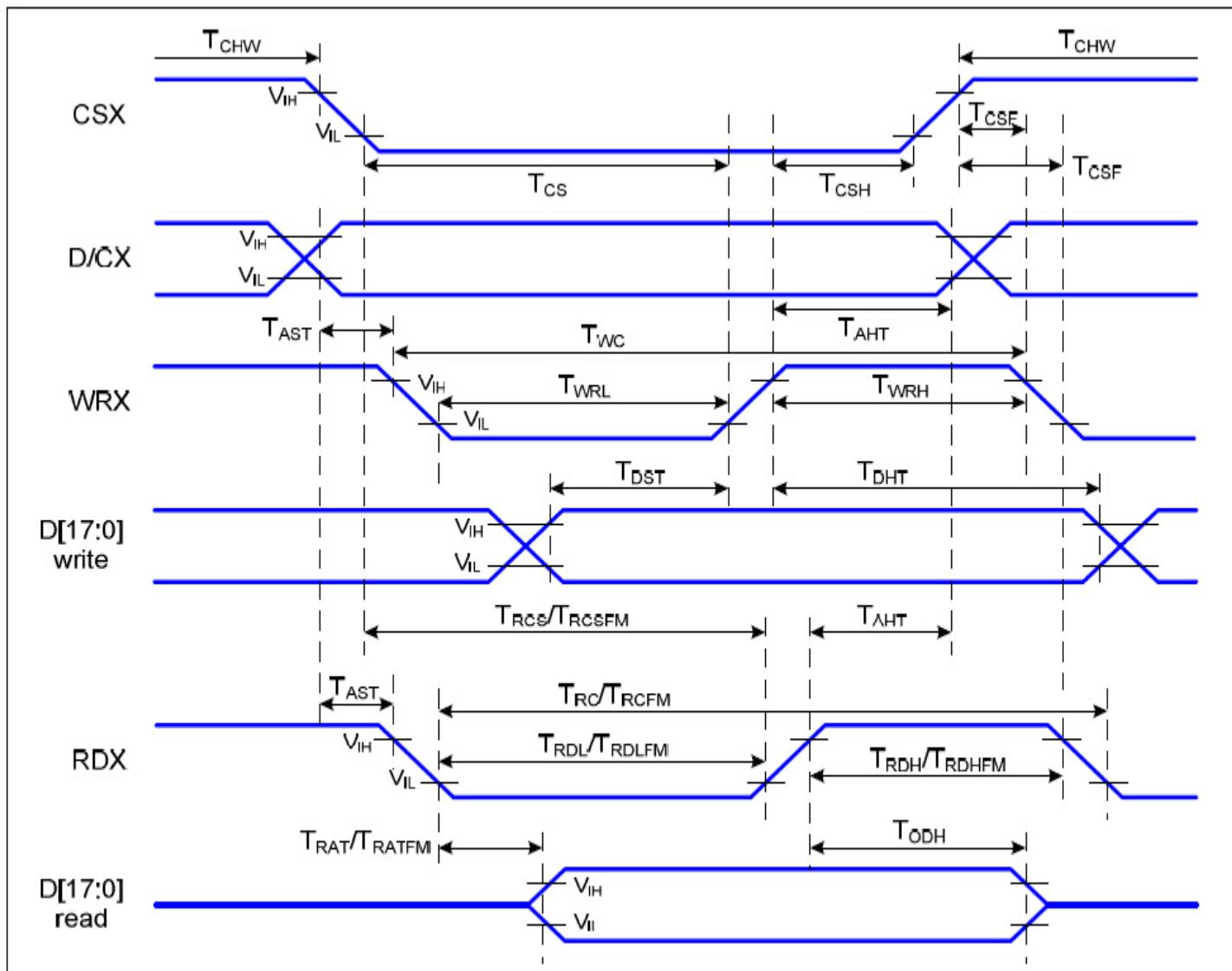


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

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Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T <sub>AST</sub>	Address setup time	0		ns	-
	T <sub>AHT</sub>	Address hold time (Write/Read)	10		ns	
CSX	T <sub>CHW</sub>	Chip select "H" pulse width	0		ns	-
	T <sub>CS</sub>	Chip select setup time (Write)	15		ns	
	T <sub>RCS</sub>	Chip select setup time (Read ID)	45		ns	
	T <sub>RCSFM</sub>	Chip select setup time (Read FM)	355		ns	
	T <sub>CSF</sub>	Chip select wait time (Write/Read)	10		ns	
	T <sub>CSH</sub>	Chip select hold time	10		ns	
WRX	T <sub>WC</sub>	Write cycle	66		ns	-
	T <sub>WRH</sub>	Control pulse "H" duration	15		ns	
	T <sub>WRL</sub>	Control pulse "L" duration	15		ns	
RDX (ID)	T <sub>RC</sub>	Read cycle (ID)	160		ns	When read ID data
	T <sub>RDH</sub>	Control pulse "H" duration (ID)	90		ns	
	T <sub>RDL</sub>	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T <sub>RCFM</sub>	Read cycle (FM)	450		ns	When read from frame memory
	T <sub>RDHFM</sub>	Control pulse "H" duration (FM)	90		ns	
	T <sub>RDLFM</sub>	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T <sub>DST</sub>	Data setup time	10		ns	For CL=30pF

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$T_{DHT}$	Data hold time	10		ns	
$T_{RAT}$	Read access time (ID)		40	ns	
$T_{RATFM}$	Read access time (FM)		340	ns	
$T_{ODH}$	Output disable time	20	80	ns	

Table 4 8080 Parallel Interface Characteristics

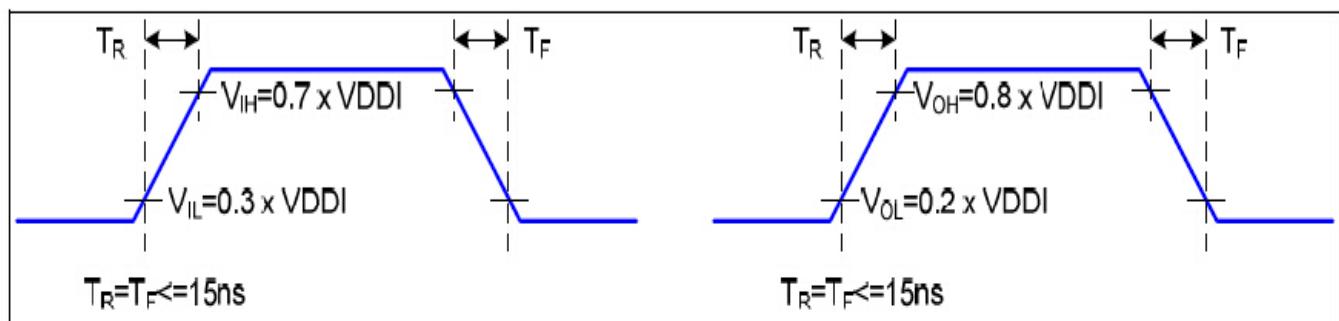


Figure 2 Rising and Falling Timing for I/O Signal

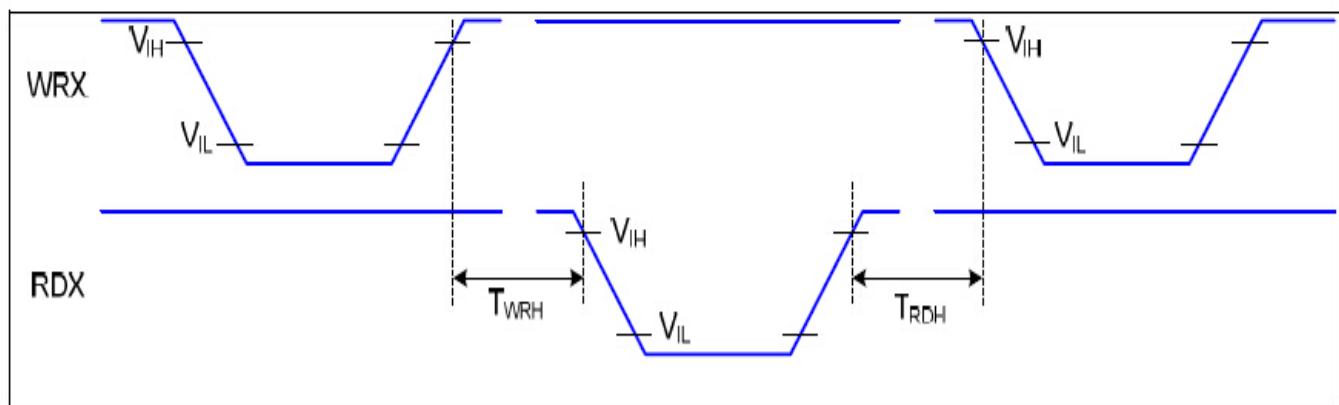


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time ( $T_r$ ,  $T_f$ ) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

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## 6.2 Serial Interface Characteristics (3-line serial)

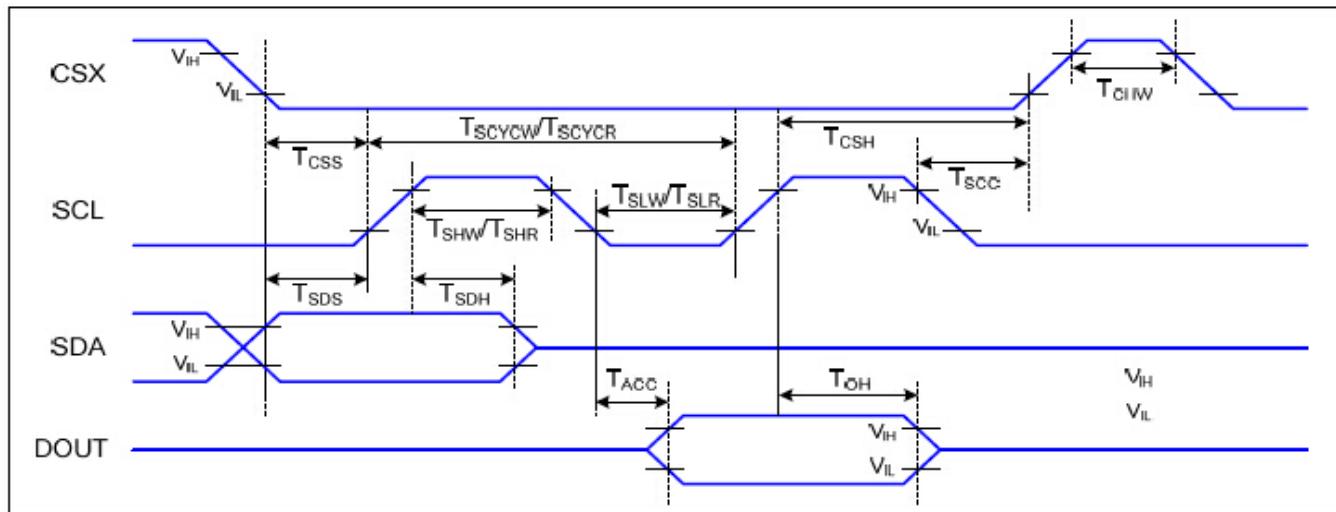


Figure 4 3-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25°C

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T <sub>CSS</sub>	Chip select setup time (write)	15		ns	
	T <sub>CSH</sub>	Chip select hold time (write)	15		ns	
	T <sub>CSS</sub>	Chip select setup time (read)	60		ns	
	T <sub>SCC</sub>	Chip select hold time (read)	65		ns	
	T <sub>CHW</sub>	Chip select "H" pulse width	40		ns	
SCL	T <sub>SCYCW</sub>	Serial clock cycle (Write)	66		ns	
	T <sub>SHW</sub>	SCL "H" pulse width (Write)	15		ns	
	T <sub>SLW</sub>	SCL "L" pulse width (Write)	15		ns	
	T <sub>SCYCR</sub>	Serial clock cycle (Read)	150		ns	
	T <sub>SHR</sub>	SCL "H" pulse width (Read)	60		ns	
	T <sub>SLR</sub>	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T <sub>SDS</sub>	Data setup time	10		ns	
	T <sub>SDH</sub>	Data hold time	10		ns	
DOUT	T <sub>ACC</sub>	Access time	10	50	ns	For maximum CL=30pF
	T <sub>OH</sub>	Output disable time	15	50	ns	For minimum CL=8pF

Table 5 3-line serial Interface Characteristics

Note : The rising time and falling time ( $T_r$ ,  $T_f$ ) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

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### 6.3 Serial Interface Characteristics (4-line serial)

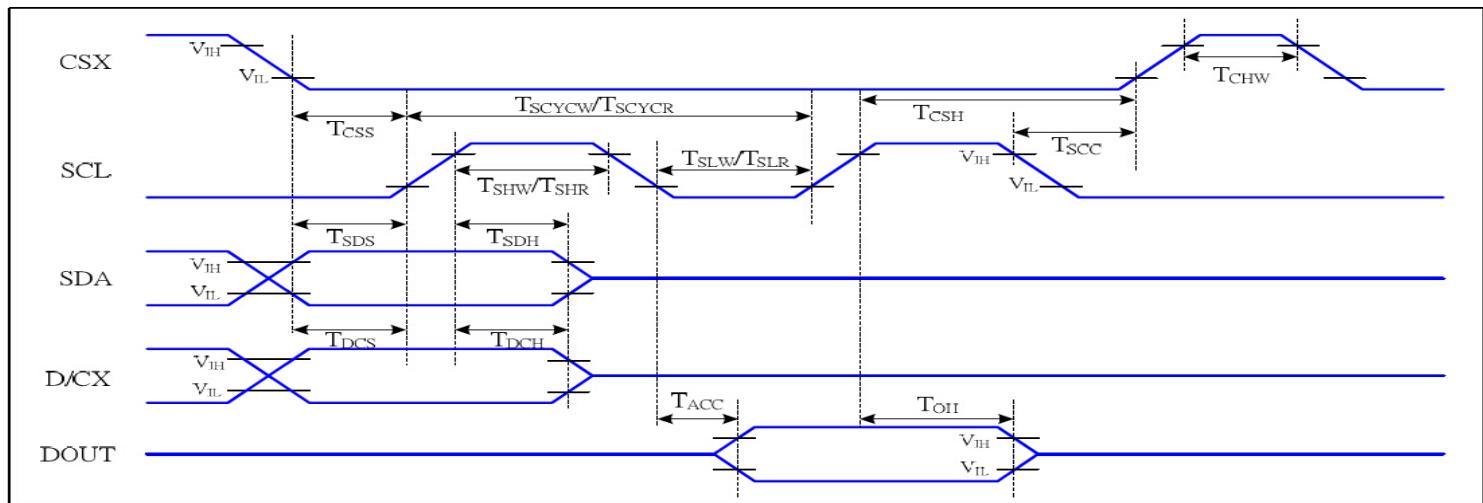


Figure 5 4-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25°C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T <sub>css</sub>	Chip select setup time (write)	15		ns	
	T <sub>csy</sub>	Chip select hold time (write)	15		ns	
	T <sub>css</sub>	Chip select setup time (read)	60		ns	
	T <sub>scc</sub>	Chip select hold time (read)	65		ns	
	T <sub>ch</sub>	Chip select "H" pulse width	40		ns	
SCL	T <sub>scycw</sub>	Serial clock cycle (Write)	66		ns	-write command & data ram
	T <sub>shw</sub>	SCL "H" pulse width (Write)	15		ns	
	T <sub>slw</sub>	SCL "L" pulse width (Write)	15		ns	
	T <sub>scyrcr</sub>	Serial clock cycle (Read)	150		ns	-read command & data ram
	T <sub>shr</sub>	SCL "H" pulse width (Read)	60		ns	
	T <sub>slr</sub>	SCL "L" pulse width (Read)	60		ns	
D/CX	T <sub>dcs</sub>	D/CX setup time	10		ns	
	T <sub>dch</sub>	D/CX hold time	10		ns	
SDA (DIN)	T <sub>sds</sub>	Data setup time	10		ns	
	T <sub>sdh</sub>	Data hold time	10		ns	
DOUT	T <sub>acc</sub>	Access time	10	50	ns	For maximum CL=30pF For minimum CL=8pF
	T <sub>oh</sub>	Output disable time	15	50	ns	

Table 6 4-line serial Interface Characteristics

Note : The rising time and falling time ( $T_r$ ,  $T_f$ ) of input signal are specified at 15 ns or less. Logic high and low levels are specified as

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## 6.4 RGB Interface Characteristics

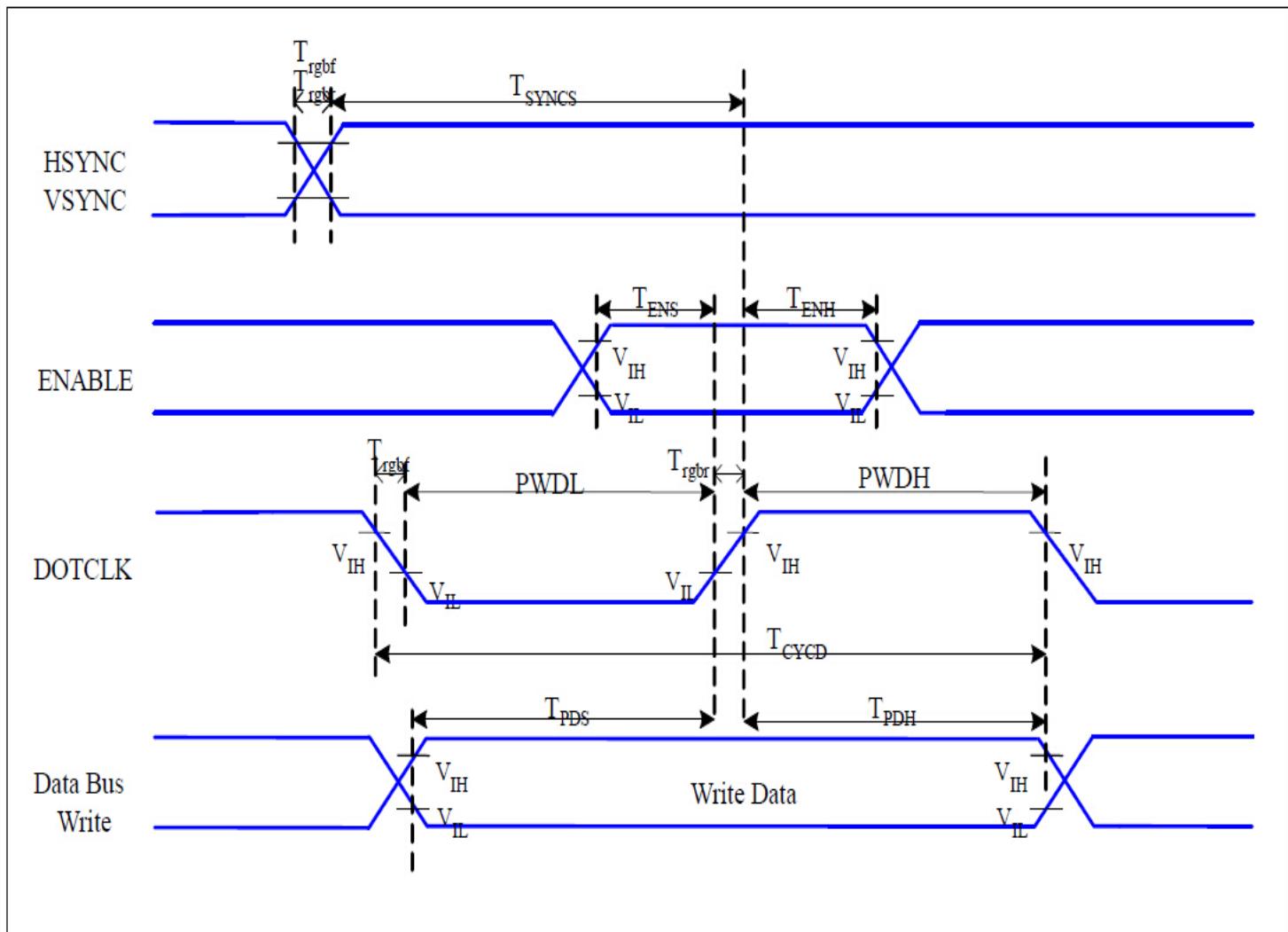


Figure 6 RGB Interface Timing Characteristics



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25°C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
H SYNC, V SYNC	T <sub>SYNCS</sub>	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T <sub>ENS</sub>	Enable Setup Time	25	-	ns	
	T <sub>ENH</sub>	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T <sub>CYCD</sub>	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T <sub>PDS</sub>	PD Data Setup Time	50	-	ns	
	T <sub>PDH</sub>	PD Data Hold Time	50	-	ns	

Table 7 18/16 Bits RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
H SYNC, V SYNC	T <sub>SYNCS</sub>	VSYNC, HSYNC Setup Time	25	-	ns	
ENABLE	T <sub>ENS</sub>	Enable Setup Time	25	-	ns	

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	T <sub>ENH</sub>	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	25	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	25	-	ns	
	T <sub>CYCD</sub>	DOTCLK Cycle Time	55	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	10	ns	
DB	T <sub>PDS</sub>	PD Data Setup Time	25	-	ns	
	T <sub>PDH</sub>	PD Data Hold Time	25	-	ns	

Table 8 6 Bits RGB Interface Timing Characteristics

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## 6.5 Reset Timing

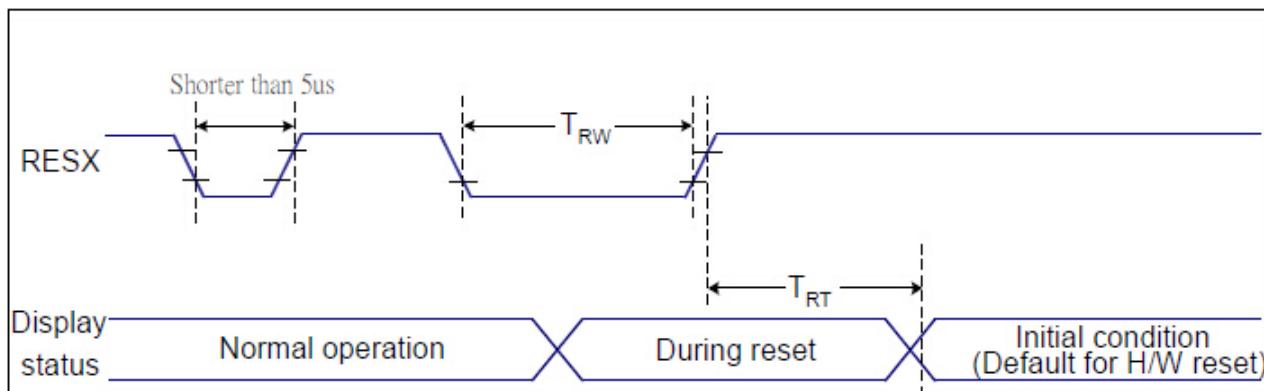


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25°C

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5) 120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

### Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time ( $t_{RT}$ ) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:

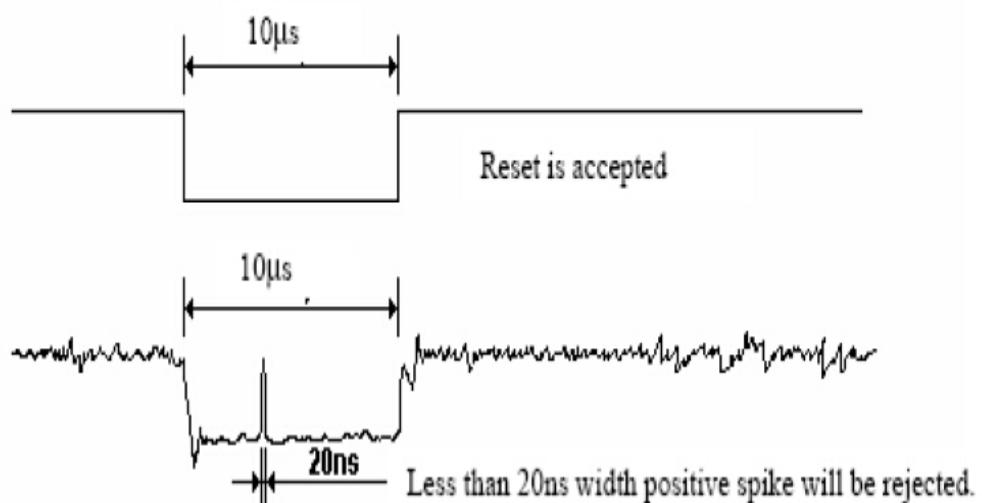
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长期供货  
Long Time supply

支持小量  
NO MOQ

品种齐全  
In Full Range



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

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## 7. CTP Specification

### 7.1 Electrical Characteristics

#### 7.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	-0.3	3.6	V	1
I/O Digital Voltage	VDDIO	1.8	3.6	V	1
Operating temperature	T <sub>OP</sub>	-20	+70	°C	-
Storage temperature	T <sub>ST</sub>	-30	+80	°C	-

#### NOTES:

- If used beyond the absolute maximum ratings, FT6336G may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

#### 7.1.2 DC Electrical Characteristics (Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Digital supply voltage	VDD		2.8	3.3	3.6	V	
I/O Digital supply voltage	VDDIO		1.8	3.3	3.6	V	
Normal operation mode Current consumption	I <sub>op</sub>		-	4	-	mA	
Monitor mode Current consumption	I <sub>mon</sub>	VDD=2.8V Ta=25°C MCLK=17.5Mhz	-	1.5	-	mA	
Sleep mode Current consumption	I <sub>slp</sub>			50		uA	
Level input voltage	V <sub>IH</sub>		0.7V <sub>DDIO</sub>	-	V <sub>DDIO</sub>	V	
	V <sub>IL</sub>		-0.3	-	0.3V <sub>DDIO</sub>	V	
Level output voltage	V <sub>OH</sub>	I <sub>OH</sub> =-0.1mA	0.7V <sub>DDIO</sub>	-	-	V	
	V <sub>OL</sub>	I <sub>OH</sub> =0.1mA	-	-	0.3V <sub>DDIO</sub>	V	

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## 7.2 AC Characteristics

**Table 4-1 AC Characteristics of Oscillators**

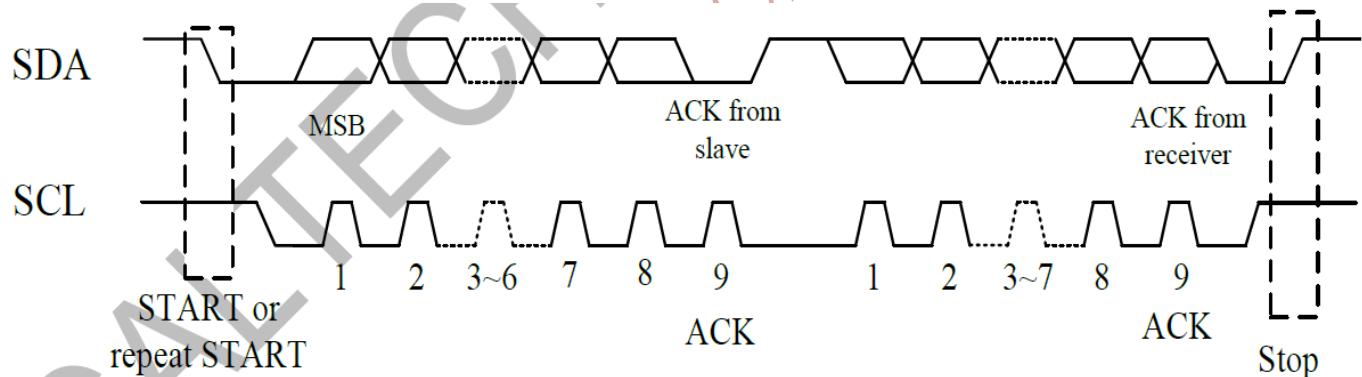
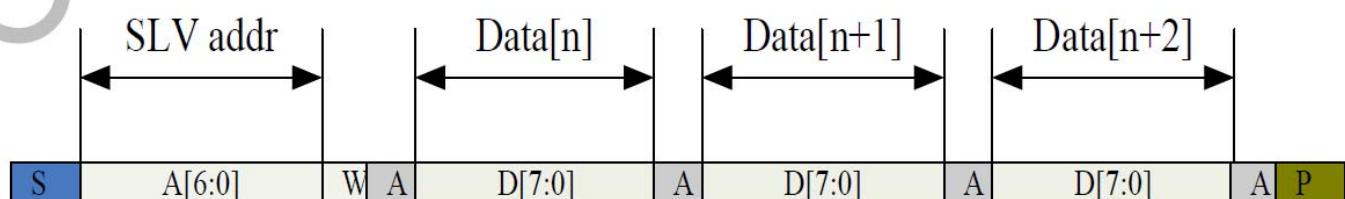
Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
OSC clock 1	fosc1	VDDA= 2.8V; Ta=25°C	34.65	35	35.35	MHz	

**Table 4-2 AC Characteristics of sensor**

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
Sensor acceptable clock	ftx	VDDA= 2.8V; Ta=25°C	0	100	300	KHz	
Sensor output rise time	Ttxr	VDDA= 2.8V; Ta=25°C	-	100	-	nS	
Sensor output fall time	Ttxf	VDDA= 2.8V; Ta=25°C	-	80	-	nS	
Sensor input voltage	Trxi	VDDA= 2.8V; Ta=25°C	-	5	-	V	

### 7.2.1 I2C Interface

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure4-1:

**Figure 4-1 I2C Serial Data Transfer Format****Figure 4-2 I2C master write, slave read**

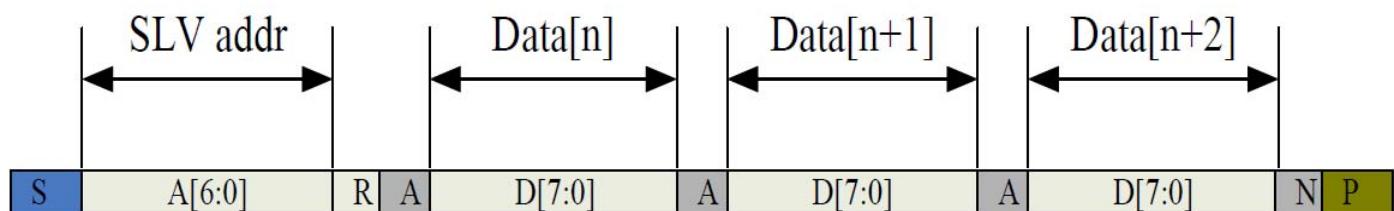


Figure 4-3 I2C master read, slave write

Table4-3 lists the meanings of the mnemonics used in the above figures.

Table 4-3 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table4-4.

Table 4-4 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup Time for STOP condition	4.0	\	us



## 8. LCD Module Out-Going Quality Level

### 8.1 VISUAL & FUNCTION INSPECTION STANDARD

#### 8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

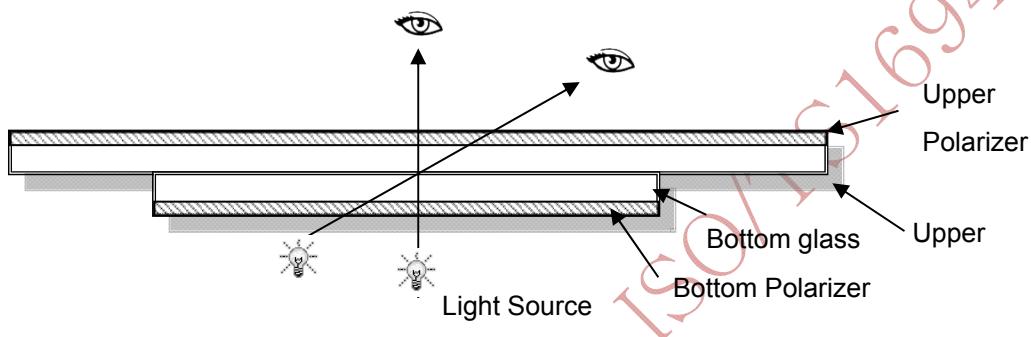
Temperature :  $25 \pm 5^\circ\text{C}$

Humidity :  $65\% \pm 10\%\text{RH}$

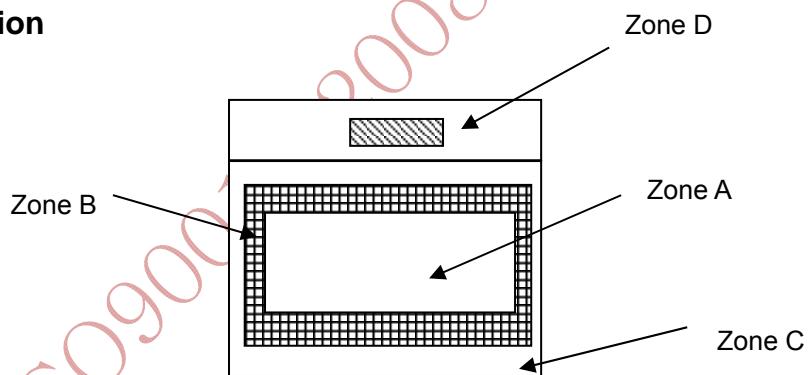
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



#### 8.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D : IC Bonding Area

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

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### 8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

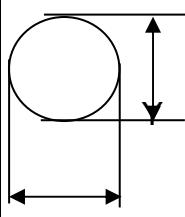
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	Minor
4	Color tone	Color unevenness, refer to limited sample	
5	Spot Line defect	Light dot, Dim spot, Polarizer Bubble ; Polarizer accidented spot.	
6	Soldering appearance	Good soldering , Peeling off is not allowed.	
7	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	



## 8.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken  NOTE: X: Length Y: Width Z: Height L: Length of ITO, T: Height of LCD	(1) The edge of LCD broken	<table border="1"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td><math>\leq 3.0\text{mm}</math></td> <td>&lt;Inner border line of the seal</td> <td><math>\leq T</math></td> </tr> </table>	X	Y	Z	$\leq 3.0\text{mm}$	<Inner border line of the seal	$\leq T$
X	Y	Z						
$\leq 3.0\text{mm}$	<Inner border line of the seal	$\leq T$						
	(2)LCD corner broken	<table border="1"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td><math>\leq 3.0\text{mm}</math></td> <td><math>\leq L</math></td> <td><math>\leq T</math></td> </tr> </table>	X	Y	Z	$\leq 3.0\text{mm}$	$\leq L$	$\leq T$
X	Y	Z						
$\leq 3.0\text{mm}$	$\leq L$	$\leq T$						
	(3) LCD crack	<p>Crack Not allowed</p>						



ISO9001:2000				
2.0				
 $X$ $\Phi = (X+Y)/2$				



3.0	Line defect (LCD/TP /Polarizer backlight black/white line, scratch, stain)	Width(mm) Length(m m)	Acceptable Qty		
			A	B	C
		Φ≤0.05	Ignore	Ignore	
		0.05<W≤0.06	L≤3.0	N≤2	
		0.07<W≤0.08	L≤2.0	N≤1	
0.08<W			Define as spot defect		

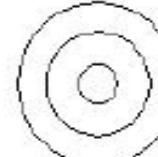
4.0	Electronic Components SMT	Not allow missing parts , solderless connection , cold solder joint , mismatch , The positive and negative polarity opposite
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5.0	Display color& Brightness	1. Color : Measuring the color coordinates, The measurement standard according to the datasheet or samples. 2. Brightness : Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.
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6.0	RTP Related	TP film • bubble/ accidented spot	Size Φ(mm)	Acceptable Qty			
				A	B	C	
			Φ≤0.1	Ignore		Ignore	
			0.1<Φ≤0.2	3 (distance $\geq$ 10mm)			
			0.25<Φ≤0.3	2			
			Φ>0.35	0			



TP film scratch	Width(mm)	Length(mm)	Acceptable Qty						
			A	B	C				
		$\Phi \leq 0.05$	Ignore	Ignore	Ignore				
			$L \leq 3.0$	$N \leq 2$					
			$L \leq 2.0$	$N \leq 1$					
		$0.08 < W$	Define as spot defect						
Assembly deflection	beyond the edge of backlight $\leq 0.2\text{mm}$								
Bulge (undulation included)	The ITO film plumped below $0.40\text{mm}$ , it's ok.								
Newton Ring	 $<0.4\text{mm}$								
	<p>Newton Ring area <math>&gt; 1/3</math> TP area NG</p> <p>Newton Ring area <math>\leq 1/3</math> TP area OK</p>								
	 1. 规律性								
			 2. 非规律性						
			 似牛顿环						



		TP corner broken X : length Y : width Z : height	<table border="1"> <tr><th>X</th><th>Y</th><th>Z</th></tr> <tr><td>X≤3mm</td><td>Y≤3mm</td><td>Z&lt;COVER thickness</td></tr> </table> <p>*</p> <p>*Circuitry broken is not allowed.</p>	X	Y	Z	X≤3mm	Y≤3mm	Z<COVER thickness	
X	Y	Z								
X≤3mm	Y≤3mm	Z<COVER thickness								
		TP edge broken X : length Y : width Z : height	<table border="1"> <tr><th>X</th><th>Y</th><th>Z</th></tr> <tr><td>X≤4mm</td><td>Y≤2mm</td><td>Z&lt;COVER thickness</td></tr> </table> <p>* Circuitry broken is not allowed.</p>	X	Y	Z	X≤4mm	Y≤2mm	Z<COVER thickness	
X	Y	Z								
X≤4mm	Y≤2mm	Z<COVER thickness								

Criteria ( functional items )

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed



## 9. Reliability Test Result

### 9.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20°C, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70°C 90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20°C ↔ 70°C, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80°C, 96HR	3ea	pass	-
Low Temperature Storage test	-30°C, 96HR	3ea	pass	-
ESD test	150pF, 330Ω, ±6KV(Contact)/± 8KV(Air), 5 points/panel, 10 times/point	3ea	pass	
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66cm(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

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## 10. Cautions and Handling Precautions

### 10.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.  
Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.  
If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.  
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.
- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

### 10.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.  
It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%.
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.  
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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## 11. Packing

----TBD-----

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