GC9308

a-Si TFT LCD Single Chip Driver 320RGBx240 Resolution and 262K color

Rev.1.0 Preliminary

2019-2-20

GENERATION REVISION HISTORY

REV.	EFFECTIVE DATE	DESCRIPTION OF CHANGES	PREPARED BY
1.0	2019-2-20	New Created	Aaron

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1. Introduction

GC9308 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 320RGBx240 dots, comprising a 960-channel source driver, a 240-channel gate driver, 172,800 bytes GRAM for graphic display data of 320RGBx240 dots, and power supply circuit.

GC9308 supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

GC9308 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the GC9308 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

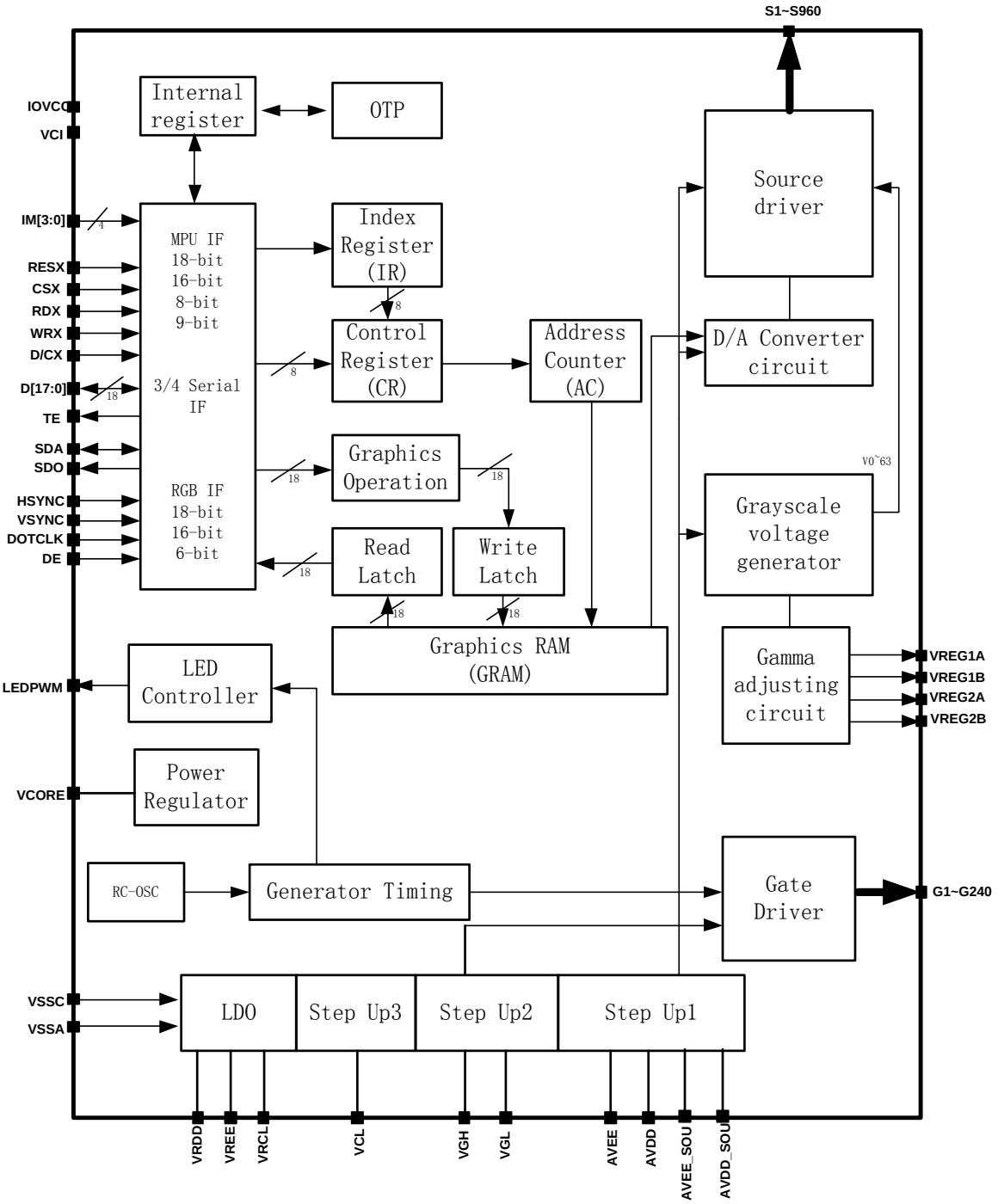
2. Features

- No need for external electronic component
- Display resolution: [320xRGB](H) x 240(V)
- Output:
  - 960 source outputs
  - 240 gate outputs
- a-TFT LCD driver with on-chip full display RAM: 172,800 bytes
- System Interface
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-I /8080-II series MCU
  - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
  - 8-bits, 9-bits 24bit Serial Peripheral Interface (SPI) and 2 data lane SPI
- Display mode:
  - Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
  - Reduce color mode (Idle mode ON): 8-color
- Power saving mode:
  - Sleep mode
- On chip functions:
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Dot/column inversion
- Low -power consumption architecture
  - Low operating power supplies:
    - IOVCC = 1.65V ~ 3.3V (logic)
    - VCI = 2.5V ~ 3.3V (analog)
- LCD Voltage drive:
  - Source/Gamma power supply voltage
    - AVDD - GND = 6.5V ~7.5V
    - AVEE - GND = -5.5V ~ -4.5V
    - VCL - GND = -3.0V ~ -1.5V
  - Gate driver output voltage
    - VGH - GND = 10.0V ~ 12.0V
    - VGL - GND = -11.0V ~ -9.0V
    - VGH - VGL ≦23V
- Operate temperature range: -40℃to 80℃
- a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Block Diagram

3.1. Block diagram

Figure1



3.2. Pin Description

Table 1.

Power Supply Pins			
Pin Name	I/O	Type	Descriptions
IOVCC	I	Digital Power	Low voltage power supply for interface logic circuits(1.65~3.3V)
VCI	I	Analog Power	High voltage power supply for analog circuit blocks(2.5~3.3V)
VCORE	O	Digital Power	Regulated Low voltage level for interface circuits Don't apply any external power to this pad
VSSA	I	Analog Ground	System ground level for analog circuit blocks Connect to VSSA on the FPC to prevent noise.
VSSC	I	Digital Ground	System ground level for Digital circuit blocks Connect to VSSC on the FPC to prevent noise.

Table 2

<table>
<tr><th colspan="4">Interface Logic Signals</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>(IOVCC/GND)</td><td>
-Select the MCU interface mode
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MCU-Interface</th><th colspan="2">Pins in use</th></tr>
<tr><th>Register</th><th>GRAM</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>8080 MCU 8-bit bus interface I</td><td>D[7:0]</td><td>D[7:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>8080 MCU16-bit bus interface I</td><td>D[7:0]</td><td>D[15:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>8080 MCU 9-bit bus interface I</td><td>D[7:0]</td><td>D[8:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>8080 MCU18-bit bus interface I</td><td>D[7:0]</td><td>D[17:0]</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>3-wire 9-bit data serial interface I</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>2 data line serial interface I</td><td colspan="2">SDA: In/OUT
DCX:In</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>4-wire 8-bit data serial interface I</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 16-bit bus interface II</td><td>D[8:1]</td><td>D[17:10] ,D[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 8-bit bus interface II</td><td>D[17:10]</td><td>D[17:10]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 18-bit bus interface II</td><td>D[8:1]</td><td>D[17:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 9-bit bus interface II</td><td>D[17:10]</td><td>D[17:9]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface II</td><td colspan="2">SDI:In
SDO:Out</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>4-wire 8-bit data serial interface II</td><td colspan="2">SDI:In
SDO:Out</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>3wires 24-bit data serial interface (ID0)</td><td colspan="2">SDI, SDO, SCL, CSX</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>3wires 24-bit data serial interface (ID1)</td><td colspan="2">SDI, SDO, SCL, CSX</td></tr>
</table>
MPU Parallel interface bus and serial interface select
If use RGB Interface must select serial interface.
Fix this pin at IOVCC or GND.
</td></tr>
</table>

RESX	I	MCU (IOVCC/GND)	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
CSX	I	MCU (IOVCC/GND)	Chip select input pin("Low" enable). This pin can be permanently fixed "Low" in MPU interface mode only.
D/CX (SCL)	I	MCU (IOVCC/GND)	This pin is used to select "Data or Command" in the parallel interface When DCX='1', data is selected. When DCX='0', command is selected. This pin is used serial interface clock in 3-wire 9-bit/3-wire 24-bit / 4-wire 8-bit serial data interface. If not used, this pin should be connected to IOVCC or GND.
RDX	I	MCU (IOVCC/GND)	8080-I/8080-II system (RDX): Serves as a read signal and MCU read data at the rising edge. Fix to IOVCC level when not in use
WRX (D/CX)	I	MCU (IOVCC/GND)	8080-I/8080-II system (WRX): Serves as a write signal and writes data at the rising edge. 4-line system (D/CX): Serves as command or parameter select. 2 lane mode serial interface: Serves as the second SDA Fix to IOVCC level when not in use.
D[17:0]	I/O	MCU (IOVCC/GND)	18-bit parallel bi-directional data bus for MCU system and RGB interface mode Fix to VSS level when not in use
SDI/SDA	I/O	MCU (IOVCC/GND)	When IM[3]:Low, Serial in/out signal in 3-wire 9-bit/4-wire 8-bit serial data interface. When IM[3]:High, Serial input signal in 3-wire 9-bit/4-wire 8-bit serial data interface. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at IOVCC or GND.
SDO	O	MCU (IOVCC/GND)	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin
TE	O	MCU (IOVCC/GND)	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
DOTCLK	I	MCU (IOVCC/GND)	Dot clock signal for RGB interface operation. Fix to IOVCC or VSSC level when not in use.
VSYNC	I	MCU (IOVCC/GND)	Frame synchronizing signal for RGB interface operation. Fix to IOVCC or VSSC level when not in use.

HSYNC	I	MCU (IOVCC/ GND)	Line synchronizing signal for RGB interface operation. Fix to IOVCC or VSSC level when not in use.
DE	I	MCU (IOVCC/ GND)	Data enable signal for RGB interface operation. Fix to IOVCC or GND level when not in use.

Note:

1. If CSX is connected to GND in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.

2. When CSX='1', there is no influence to the parallel and serial interface.

Table 3

LCD Driver Input/Output Pins			
Pin Name	I/O	Type	Descriptions
S960~S1	O	Source	Source output signals.. Leave the pin to open when not in use.
G240~G1	O	Gate	Gate output signals. Leave the pin to open when not in use.
VRDD	O	Power	Power supply for AVDD
VREE	O	Power	Power supply for AVEE
VRCL	O	Power	Power supply for VCL.
AVDD	O	Power	Output voltage of 1st step up circuit(3*VRDD).Input voltage to 2nd step up circuit. Generated power output pad for source driver block.
AVEE	O	Power	Output voltage of 1st step up circuit(-2*VREE).Input voltage to 2nd step up circuit. Generated power output pad for source driver block.
VGH	O	Power	Power supply for the gate driver(Positive).
VGL	O	Power	Power supply for the gate driver(Negative).
VCL	O	Power	Power supply for VGH and VGL. VCL=0~-VCI
VREG1A	O	Ref	internal generated stable power for source driver unit VREG1A is the highest positive grayscale reference voltage of source driver
VREG1B	O	Ref	internal generated stable power for source driver unit VREG1B is the lowest positive grayscale reference voltage of source driver
VREG2A	O	Ref	internal generated stable power for source driver unit VREG2A is the highest negative grayscale reference voltage of source driver
VREG2B	O	Ref	internal generated stable power for source driver unit VREG2B is the highest negative grayscale reference voltage of source driver
LEDPWM	O	Dig IO	Output pin for PWM(Pulse width Modulation) signal of LED driving. If not used,open this pad.

Table 4

Test Pins			
Pin Name	I/O	Type	Descriptions
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation ,leave these pads open.

Liquid crystal power supply specifications Table

Table 5

No.	Item		Description
1	TFT Source Driver		960 pins (320*RGB)
2	TFT Gate Driver		240 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1~S960	V0~V63 grayscales
		G1~G240	VGH-VGL
5	Input Voltage	IOVCC	1.65~3.30V
		VCI	2.50~3.30V
6	Liquid Crystal Drive Voltages	AVDD	6.5~7.5V
		AVEE	-5.5V~-4.5V
		VGH	10.0~12.0V
		VGL	-11.0~--9.0V
		VCL	-3.0~-1.5V
		VGH-VGL	Max.23.0V
7	Internal Step-up Circuits	AVDD	VCI*3
		AVEE	VCI*-2
		VGH	VCI*5
		VGL	VCI*-5
		VCL	VCI*-1

3.3. PAD coordinates

No	Name	X-axis	Y-axis	Width	Hight	No	Name	X-axis	Y-axis	Width	Hight	No	Name	X-axis	Y-axis	Width	Hight
1	VCOM	-8989	-244	24	69	91	DUMMY	-5389	-244	24	69	181	DB<3>	-1789	-244	24	69
2	VCOM	-8949	-244	24	69	92	DUMMY	-5349	-244	24	69	182	DB<3>	-1749	-244	24	69
3	VCOM	-8909	-244	24	69	93	VSYNC	-5309	-244	24	69	183	DB<2>	-1709	-244	24	69
4	VCOM	-8869	-244	24	69	94	HSYNC	-5269	-244	24	69	184	DB<2>	-1669	-244	24	69
5	DUMMY	-8829	-244	24	69	95	DOTCLK	-5229	-244	24	69	185	DB<1>	-1629	-244	24	69
6	VREE	-8789	-244	24	69	96	ENABLE	-5189	-244	24	69	186	DB<1>	-1589	-244	24	69
7	AVEE	-8749	-244	24	69	97	VSSB	-5149	-244	24	69	187	DB<0>	-1549	-244	24	69
8	AVEE	-8709	-244	24	69	98	DUMMY	-5109	-244	24	69	188	DB<0>	-1509	-244	24	69
9	AVEE	-8669	-244	24	69	99	DUMMY	-5069	-244	24	69	189	VDDI	-1469	-244	24	69
10	AVEE	-8629	-244	24	69	100	DUMMY	-5029	-244	24	69	190	DUMMY	-1429	-244	24	69
11	AVEE	-8589	-244	24	69	101	DUMMY	-4989	-244	24	69	191	VSSB	-1389	-244	24	69
12	AVEE	-8549	-244	24	69	102	DUMMY	-4949	-244	24	69	192	VSSB	-1349	-244	24	69
13	AVEE	-8509	-244	24	69	103	DUMMY	-4909	-244	24	69	193	VSSB	-1309	-244	24	69
14	AVEE	-8469	-244	24	69	104	DUMMY	-4869	-244	24	69	194	VSSB	-1269	-244	24	69
15	VSSB	-8429	-244	24	69	105	DUMMY	-4829	-244	24	69	195	VPP	-1229	-244	24	69
16	VSSB	-8389	-244	24	69	106	VSSB	-4789	-244	24	69	196	VPP	-1189	-244	24	69
17	VSSB	-8349	-244	24	69	107	VSSB	-4749	-244	24	69	197	VPP	-1149	-244	24	69
18	VSSB	-8309	-244	24	69	108	VSSB	-4709	-244	24	69	198	RESET	-1109	-244	24	69
19	VSSB	-8269	-244	24	69	109	VSSB	-4669	-244	24	69	199	VDDI	-1069	-244	24	69
20	VSSB	-8229	-244	24	69	110	DUMMY	-4629	-244	24	69	200	VDDI	-1029	-244	24	69
21	VSSB	-8189	-244	24	69	111	DUMMY	-4589	-244	24	69	201	VDDI	-989	-244	24	69
22	VSSB	-8149	-244	24	69	112	DUMMY	-4549	-244	24	69	202	VDDI	-949	-244	24	69
23	VSSB	-8109	-244	24	69	113	VSSB	-4509	-244	24	69	203	VDDB	-909	-244	24	69
24	VSSB	-8069	-244	24	69	114	DUMMY	-4469	-244	24	69	204	VDDB	-869	-244	24	69
25	VSSB	-8029	-244	24	69	115	DUMMY	-4429	-244	24	69	205	VDDB	-829	-244	24	69
26	VSSB	-7989	-244	24	69	116	DUMMY	-4389	-244	24	69	206	VDDB	-789	-244	24	69
27	VSSB	-7949	-244	24	69	117	VSSB	-4349	-244	24	69	207	TE	-749	-244	24	69
28	VSSB	-7909	-244	24	69	118	DUMMY	-4309	-244	24	69	208	TE	-709	-244	24	69
29	VSSB	-7869	-244	24	69	119	DUMMY	-4269	-244	24	69	209	BC	-669	-244	24	69
30	VSSB	-7829	-244	24	69	120	DUMMY	-4229	-244	24	69	210	BC	-629	-244	24	69
31	VSSB	-7789	-244	24	69	121	VSSB	-4189	-244	24	69	211	DUMMY	-589	-244	24	69
32	VSSB	-7749	-244	24	69	122	DUMMY	-4149	-244	24	69	212	VSSB	-549	-244	24	69
33	VSSB	-7709	-244	24	69	123	DUMMY	-4109	-244	24	69	213	OSC_TEST	-509	-244	24	69
34	VSSB	-7669	-244	24	69	124	DUMMY	-4069	-244	24	69	214	OSC_TEST	-469	-244	24	69
35	VSSB	-7629	-244	24	69	125	VSSB	-4029	-244	24	69	215	OSC_IN	-429	-244	24	69
36	VSSB	-7589	-244	24	69	126	DUMMY	-3989	-244	24	69	216	OSC_IN	-389	-244	24	69
37	VSSB	-7549	-244	24	69	127	DUMMY	-3949	-244	24	69	217	DUMMY	-349	-244	24	69
38	VSSB	-7509	-244	24	69	128	VSSB	-3909	-244	24	69	218	DUMMY	-309	-244	24	69
39	VDDI	-7469	-244	24	69	129	DUMMY	-3869	-244	24	69	219	DUMMY	309	-244	24	69
40	VDDI	-7429	-244	24	69	130	VDDI	-3829	-244	24	69	220	DUMMY	349	-244	24	69
41	VDDI	-7389	-244	24	69	131	DUMMY	-3789	-244	24	69	221	DUMMY	389	-244	24	69
42	VDDI	-7349	-244	24	69	132	VSSB	-3749	-244	24	69	222	DUMMY	429	-244	24	69
43	VDDI	-7309	-244	24	69	133	DUMMY	-3709	-244	24	69	223	DUMMY	469	-244	24	69
44	VDDI	-7269	-244	24	69	134	DUMMY	-3669	-244	24	69	224	DUMMY	509	-244	24	69
45	VDDI	-7229	-244	24	69	135	DUMMY	-3629	-244	24	69	225	DUMMY	549	-244	24	69
46	VDDI	-7189	-244	24	69	136	DUMMY	-3589	-244	24	69	226	DUMMY	589	-244	24	69
47	VDDI	-7149	-244	24	69	137	DUMMY	-3549	-244	24	69	227	DUMMY	629	-244	24	69
48	VDDI	-7109	-244	24	69	138	DUMMY	-3509	-244	24	69	228	DUMMY	669	-244	24	69
49	VDDSF	-7069	-244	24	69	139	DUMMY	-3469	-244	24	69	229	DUMMY	709	-244	24	69
50	VSSB	-7029	-244	24	69	140	DUMMY	-3429	-244	24	69	230	DUMMY	749	-244	24	69
51	IM<3>	-6989	-244	24	69	141	DUMMY	-3389	-244	24	69	231	REF_LDO_TEST	789	-244	24	69
52	VDDI	-6949	-244	24	69	142	VDDI	-3349	-244	24	69	232	REF_LDO_TEST	829	-244	24	69
53	IM<2>	-6909	-244	24	69	143	VDDI	-3309	-244	24	69	233	REF_LDO_TEST	869	-244	24	69
54	VSSB	-6869	-244	24	69	144	VDDI	-3269	-244	24	69	234	REF_LDO_TEST	909	-244	24	69
55	IM<1>	-6829	-244	24	69	145	VDDI	-3229	-244	24	69	235	REF_LDO_TEST	949	-244	24	69
56	VDDI	-6789	-244	24	69	146	RD	-3189	-244	24	69	236	DUMMY	989	-244	24	69
57	IM<0>	-6749	-244	24	69	147	WR	-3149	-244	24	69	237	DUMMY	1029	-244	24	69
58	VSSB	-6709	-244	24	69	148	DC	-3109	-244	24	69	238	DUMMY	1069	-244	24	69
59	VSSB	-6669	-244	24	69	149	CS	-3069	-244	24	69	239	DUMMY	1109	-244	24	69
60	DUMMY	-6629	-244	24	69	150	VSSB	-3029	-244	24	69	240	DUMMY	1149	-244	24	69
61	DUMMY	-6589	-244	24	69	151	DB<17>	-2989	-244	24	69	241	VSSR	1189	-244	24	69
62	DUMMY	-6549	-244	24	69	152	DB<17>	-2949	-244	24	69	242	VSSR	1229	-244	24	69
63	DUMMY	-6509	-244	24	69	153	DB<16>	-2909	-244	24	69	243	VSSR	1269	-244	24	69
64	DUMMY	-6469	-244	24	69	154	DB<16>	-2869	-244	24	69	244	VSSR	1309	-244	24	69
65	VSSB	-6429	-244	24	69	155	DB<15>	-2829	-244	24	69	245	VSSR	1349	-244	24	69
66	DUMMY	-6389	-244	24	69	156	DB<15>	-2789	-244	24	69	246	VSSR	1389	-244	24	69
67	VDDI	-6349	-244	24	69	157	DB<14>	-2749	-244	24	69	247	VSSR	1429	-244	24	69
68	DUMMY	-6309	-244	24	69	158	DB<14>	-2709	-244	24	69	248	VSSR	1469	-244	24	69
69	DUMMY	-6269	-244	24	69	159	DB<13>	-2669	-244	24	69	249	VSSR	1509	-244	24	69
70	DUMMY	-6229	-244	24	69	160	DB<13>	-2629	-244	24	69	250	VSSR	1549	-244	24	69
71	DUMMY	-6189	-244	24	69	161	DB<12>	-2589	-244	24	69	251	VSSR	1589	-244	24	69
72	DUMMY	-6149	-244	24	69	162	DB<12>	-2549	-244	24	69	252	VSSR	1629	-244	24	69
73	DUMMY	-6109	-244	24	69	163	VSSB	-2509	-244	24	69	253	GVDDN	1669	-244	24	69
74	DUMMY	-6069	-244	24	69	164	DB<11>	-2469	-244	24	69	254	GVDDN	1709	-244	24	69
75	DUMMY	-6029	-244	24	69	165	DB<11>	-2429	-244	24	69	255	VSSB	1749	-244	24	69
76	DUMMY	-5989	-244	24	69	166	DB<10>	-2389	-244	24	69	256	VSSB	1789	-244	24	69
77	DUMMY	-5949	-244	24	69	167	DB<10>	-2349	-244	24	69	257	VSSB	1829	-244	24	69
78	DUMMY	-5909	-244	24	69	168	DB<9>	-2309	-244	24	69	258	VSSB	1869	-244	24	69
79	DUMMY	-5869	-244	24	69	169	DB<9>	-2269	-244	24	69	259	VSSB	1909	-244	24	69
80	DUMMY	-5829	-244	24	69	170	DB<8>	-2229	-244	24	69	260	VSSB	1949	-244	24	69
81	DUMMY	-5789	-244	24	69	171	DB<8>	-2189	-244	24	69	261	VSSB	1989	-244	24	69
82	DUMMY	-5749	-244	24	69	172	DB<7>	-2149	-244	24	69	262	VSSB	2029	-244	24	69
83	VSSB	-5709	-244	24	69	173	DB<7>	-2109	-244	24	69	263	VSSB	2069	-244	24	69
84	DUMMY	-5669	-244	24	69	174	DB<6>	-2069	-244	24	69	264	VSSB	2109	-244	24	69
85	VDDI	-5629	-244	24	69	175	DB<6>	-2029	-244	24	69	265	VSSB	2149	-244	24	69
86	DUMMY	-5589	-244	24	69	176	VSSB	-1989	-244	24	69	266	VSSB	2189	-244	24	69
87	DUMMY	-5549	-244	24	69	177	DB<5>	-1949	-244	24	69	267	VSSB	2229	-244	24	69
88	SDA	-5509	-244	24	69	178	DB<5>	-1909	-244	24	69	268	DUMMY	2269	-244	24	69
89	SDO	-5469	-244	24	69	179	DB<4>	-1869	-244	24	69	269	DUMMY	2309	-244	24	69
90	SDO	-5429	-244	24	69	180	DB<4>	-1829	-244	24	69	270	DUMMY	2349	-244	24	69

No	Name	X-axis	Y-axis	Width	Hight	No	Name	X-axis	Y-axis	Width	Hight	No	Name	X-axis	Y-axis	Width	Hight
271	DUMMY	2389	-244	24	69	361	VDDB	5989	-244	24	69	451	G<216>	8811	234.5	14	90
272	DUMMY	2429	-244	24	69	362	VDDB	6029	-244	24	69	452	G<214>	8795	108.5	14	90
273	DUMMY	2469	-244	24	69	363	VDDB	6069	-244	24	69	453	G<212>	8779	234.5	14	90
274	DUMMY	2509	-244	24	69	364	VDDB	6109	-244	24	69	454	G<210>	8763	108.5	14	90
275	DUMMY	2549	-244	24	69	365	VDDB	6149	-244	24	69	455	G<208>	8747	234.5	14	90
276	DUMMY	2589	-244	24	69	366	DUMMY	6189	-244	24	69	456	G<206>	8731	108.5	14	90
277	DUMMY	2629	-244	24	69	367	BVDD	6229	-244	24	69	457	G<204>	8715	234.5	14	90
278	DUMMY	2669	-244	24	69	368	BVDD	6269	-244	24	69	458	G<202>	8699	108.5	14	90
279	DUMMY	2709	-244	24	69	369	BVDD	6309	-244	24	69	459	G<200>	8683	234.5	14	90
280	DUMMY	2749	-244	24	69	370	BVDD	6349	-244	24	69	460	G<198>	8667	108.5	14	90
281	GVDDP	2789	-244	24	69	371	BVDD	6389	-244	24	69	461	G<196>	8651	234.5	14	90
282	GVDDP	2829	-244	24	69	372	BVDD	6429	-244	24	69	462	G<194>	8635	108.5	14	90
283	DUMMY	2869	-244	24	69	373	BVDD	6469	-244	24	69	463	G<192>	8619	234.5	14	90
284	DUMMY	2909	-244	24	69	374	BVDD	6509	-244	24	69	464	G<190>	8603	108.5	14	90
285	DUMMY	2949	-244	24	69	375	VGL	6549	-244	24	69	465	G<188>	8587	234.5	14	90
286	DUMMY	2989	-244	24	69	376	VGL	6589	-244	24	69	466	G<186>	8571	108.5	14	90
287	DUMMY	3029	-244	24	69	377	VGL	6629	-244	24	69	467	G<184>	8555	234.5	14	90
288	AVDD	3069	-244	24	69	378	VGL	6669	-244	24	69	468	G<182>	8539	108.5	14	90
289	AVDD	3109	-244	24	69	379	VGL	6709	-244	24	69	469	G<180>	8523	234.5	14	90
290	AVDD	3149	-244	24	69	380	VGL	6749	-244	24	69	470	G<178>	8507	108.5	14	90
291	AVDD	3189	-244	24	69	381	VGL	6789	-244	24	69	471	G<176>	8491	234.5	14	90
292	AVDD	3229	-244	24	69	382	VGL	6829	-244	24	69	472	G<174>	8475	108.5	14	90
293	AVDD	3269	-244	24	69	383	VRDD	6869	-244	24	69	473	G<172>	8459	234.5	14	90
294	VREG_VREF	3309	-244	24	69	384	VRDD	6909	-244	24	69	474	G<170>	8443	108.5	14	90
295	VREG_VREF	3349	-244	24	69	385	VRDD	6949	-244	24	69	475	G<168>	8427	234.5	14	90
296	VREG_VREF	3389	-244	24	69	386	VRDD	6989	-244	24	69	476	G<166>	8411	108.5	14	90
297	VREG_VREF	3429	-244	24	69	387	VRDD	7029	-244	24	69	477	G<164>	8395	234.5	14	90
298	VREG_VREF	3469	-244	24	69	388	VRDD	7069	-244	24	69	478	G<162>	8379	108.5	14	90
299	VREG_VREF	3509	-244	24	69	389	VRDD	7109	-244	24	69	479	G<160>	8363	234.5	14	90
300	VREG1A	3549	-244	24	69	390	VRDD	7149	-244	24	69	480	G<158>	8347	108.5	14	90
301	VREG1A	3589	-244	24	69	391	VRDD	7189	-244	24	69	481	G<156>	8331	234.5	14	90
302	VREG1A	3629	-244	24	69	392	VRDD	7229	-244	24	69	482	G<154>	8315	108.5	14	90
303	VREG1A	3669	-244	24	69	393	VRDD	7269	-244	24	69	483	G<152>	8299	234.5	14	90
304	VREG1A	3709	-244	24	69	394	VRDD	7309	-244	24	69	484	G<150>	8283	108.5	14	90
305	VREG1A	3749	-244	24	69	395	VCL	7349	-244	24	69	485	G<148>	8267	234.5	14	90
306	DUMMY	3789	-244	24	69	396	VCL	7389	-244	24	69	486	G<146>	8251	108.5	14	90
307	DUMMY	3829	-244	24	69	397	VCL	7429	-244	24	69	487	G<144>	8235	234.5	14	90
308	DUMMY	3869	-244	24	69	398	VCL	7469	-244	24	69	488	G<142>	8219	108.5	14	90
309	DUMMY	3909	-244	24	69	399	VCL	7509	-244	24	69	489	G<140>	8203	234.5	14	90
310	DUMMY	3949	-244	24	69	400	VCL	7549	-244	24	69	490	G<138>	8187	108.5	14	90
311	DVDD	3989	-244	24	69	401	VCL	7589	-244	24	69	491	G<136>	8171	234.5	14	90
312	DVDD	4029	-244	24	69	402	VCL	7629	-244	24	69	492	G<134>	8155	108.5	14	90
313	DVDD	4069	-244	24	69	403	VCL	7669	-244	24	69	493	G<132>	8139	234.5	14	90
314	DVDD	4109	-244	24	69	404	VCL	7709	-244	24	69	494	G<130>	8123	108.5	14	90
315	DVDD	4149	-244	24	69	405	VCL	7749	-244	24	69	495	G<128>	8107	234.5	14	90
316	DVDD	4189	-244	24	69	406	VCL	7789	-244	24	69	496	G<126>	8091	108.5	14	90
317	DUMMY	4229	-244	24	69	407	VRCL	7829	-244	24	69	497	G<124>	8075	234.5	14	90
318	DUMMY	4269	-244	24	69	408	VRCL	7869	-244	24	69	498	G<122>	8059	108.5	14	90
319	DUMMY	4309	-244	24	69	409	VRCL	7909	-244	24	69	499	G<120>	8043	234.5	14	90
320	DUMMY	4349	-244	24	69	410	VRCL	7949	-244	24	69	500	G<118>	8027	108.5	14	90
321	DUMMY	4389	-244	24	69	411	VRCL	7989	-244	24	69	501	G<116>	8011	234.5	14	90
322	DUMMY	4429	-244	24	69	412	VRCL	8029	-244	24	69	502	G<114>	7995	108.5	14	90
323	DUMMY	4469	-244	24	69	413	VRCL	8069	-244	24	69	503	G<112>	7979	234.5	14	90
324	DUMMY	4509	-244	24	69	414	VRCL	8109	-244	24	69	504	G<110>	7963	108.5	14	90
325	DUMMY	4549	-244	24	69	415	VRCL	8149	-244	24	69	505	G<108>	7947	234.5	14	90
326	DUMMY	4589	-244	24	69	416	VRCL	8189	-244	24	69	506	G<106>	7931	108.5	14	90
327	DUMMY	4629	-244	24	69	417	VRCL	8229	-244	24	69	507	G<104>	7915	234.5	14	90
328	DUMMY	4669	-244	24	69	418	VRCL	8269	-244	24	69	508	G<102>	7899	108.5	14	90
329	DUMMY	4709	-244	24	69	419	VGH	8309	-244	24	69	509	G<100>	7883	234.5	14	90
330	DUMMY	4749	-244	24	69	420	VGH	8349	-244	24	69	510	G<98>	7867	108.5	14	90
331	DUMMY	4789	-244	24	69	421	VGH	8389	-244	24	69	511	G<96>	7851	234.5	14	90
332	DUMMY	4829	-244	24	69	422	VGH	8429	-244	24	69	512	G<94>	7835	108.5	14	90
333	DUMMY	4869	-244	24	69	423	VGH	8469	-244	24	69	513	G<92>	7819	234.5	14	90
334	DUMMY	4909	-244	24	69	424	VGH	8509	-244	24	69	514	G<90>	7803	108.5	14	90
335	DUMMY	4949	-244	24	69	425	VGH	8549	-244	24	69	515	G<88>	7787	234.5	14	90
336	DUMMY	4989	-244	24	69	426	VGH	8589	-244	24	69	516	G<86>	7771	108.5	14	90
337	DUMMY	5029	-244	24	69	427	VGH	8629	-244	24	69	517	G<84>	7755	234.5	14	90
338	DUMMY	5069	-244	24	69	428	VGH	8669	-244	24	69	518	G<82>	7739	108.5	14	90
339	DUMMY	5109	-244	24	69	429	VGH	8709	-244	24	69	519	G<80>	7723	234.5	14	90
340	DUMMY	5149	-244	24	69	430	VGH	8749	-244	24	69	520	G<78>	7707	108.5	14	90
341	DUMMY	5189	-244	24	69	431	DUMMY	8789	-244	24	69	521	G<76>	7691	234.5	14	90
342	DUMMY	5229	-244	24	69	432	DUMMY	8829	-244	24	69	522	G<74>	7675	108.5	14	90
343	DUMMY	5269	-244	24	69	433	VCOM	8869	-244	24	69	523	G<72>	7659	234.5	14	90
344	DUMMY	5309	-244	24	69	434	VCOM	8909	-244	24	69	524	G<70>	7643	108.5	14	90
345	DUMMY	5349	-244	24	69	435	VCOM	8949	-244	24	69	525	G<68>	7627	234.5	14	90
346	DUMMY	5389	-244	24	69	436	VCOM	8989	-244	24	69	526	G<66>	7611	108.5	14	90
347	BVEE	5429	-244	24	69	437	DUMMY	9035	234.5	14	90	527	G<64>	7595	234.5	14	90
348	BVEE	5469	-244	24	69	438	DUMMY	9019	108.5	14	90	528	G<62>	7579	108.5	14	90
349	BVEE	5509	-244	24	69	439	G<240>	9003	234.5	14	90	529	G<60>	7563	234.5	14	90
350	BVEE	5549	-244	24	69	440	G<238>	8987	108.5	14	90	530	G<58>	7547	108.5	14	90
351	BVEE	5589	-244	24	69	441	G<236>	8971	234.5	14	90	531	G<56>	7531	234.5	14	90
352	BVEE	5629	-244	24	69	442	G<234>	8955	108.5	14	90	532	G<54>	7515	108.5	14	90
353	BVEE	5669	-244	24	69	443	G<232>	8939	234.5	14	90	533	G<52>	7499	234.5	14	90
354	BVEE	5709	-244	24	69	444	G<230>	8923	108.5	14	90	534	G<50>	7483	108.5	14	90
355	BVEE	5749	-244	24	69	445	G<228>	8907	234.5	14	90	535	G<48>	7467	234.5	14	90
356	BVEE	5789	-244	24	69	446	G<226>	8891	108.5	14	90	536	G<46>	7451	108.5	14	90
357	DUMMY	5829	-244	24	69	447	G<224>	8875	234.5	14	90	537	G<44>	7435	234.5	14	90
358	DUMMY	5869	-244	24	69	448	G<222>	8859	108.5	14	90	538	G<42>	7419	108.5	14	90
359	DUMMY	5909	-244	24	69	449	G<220>	8843	234.5	14	90	539	G<40>	7403	234.5	14	90
360	VDDB	5949	-244	24	69	450	G<218>	8827	108.5	14	90	540	G<38>	7387	108.5	14	90

No	Name	X-axis	Y-axis	Width	Hight	No	Name	X-axis	Y-axis	Width	Hight	No	Name	X-axis	Y-axis	Width	Hight
541	G<36>	7371	234.5	14	90	631	S<892>	6071	234.5	14	90	721	S<802>	4811	234.5	14	90
542	G<34>	7355	108.5	14	90	632	S<891>	6057	108.5	14	90	722	S<801>	4797	108.5	14	90
543	G<32>	7339	234.5	14	90	633	S<890>	6043	234.5	14	90	723	S<800>	4783	234.5	14	90
544	G<30>	7323	108.5	14	90	634	S<889>	6029	108.5	14	90	724	S<799>	4769	108.5	14	90
545	G<28>	7307	234.5	14	90	635	S<888>	6015	234.5	14	90	725	S<798>	4755	234.5	14	90
546	G<26>	7291	108.5	14	90	636	S<887>	6001	108.5	14	90	726	S<797>	4741	108.5	14	90
547	G<24>	7275	234.5	14	90	637	S<886>	5987	234.5	14	90	727	S<796>	4727	234.5	14	90
548	G<22>	7259	108.5	14	90	638	S<885>	5973	108.5	14	90	728	S<795>	4713	108.5	14	90
549	G<20>	7243	234.5	14	90	639	S<884>	5959	234.5	14	90	729	S<794>	4699	234.5	14	90
550	G<18>	7227	108.5	14	90	640	S<883>	5945	108.5	14	90	730	S<793>	4685	108.5	14	90
551	G<16>	7211	234.5	14	90	641	S<882>	5931	234.5	14	90	731	S<792>	4671	234.5	14	90
552	G<14>	7195	108.5	14	90	642	S<881>	5917	108.5	14	90	732	S<791>	4657	108.5	14	90
553	G<12>	7179	234.5	14	90	643	S<880>	5903	234.5	14	90	733	S<790>	4643	234.5	14	90
554	G<10>	7163	108.5	14	90	644	S<879>	5889	108.5	14	90	734	S<789>	4629	108.5	14	90
555	G<8>	7147	234.5	14	90	645	S<878>	5875	234.5	14	90	735	S<788>	4615	234.5	14	90
556	G<6>	7131	108.5	14	90	646	S<877>	5861	108.5	14	90	736	S<787>	4601	108.5	14	90
557	G<4>	7115	234.5	14	90	647	S<876>	5847	234.5	14	90	737	S<786>	4587	234.5	14	90
558	G<2>	7099	108.5	14	90	648	S<875>	5833	108.5	14	90	738	S<785>	4573	108.5	14	90
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897	S<626>	2347	234.5	14	90	987	S<536>	1087	234.5	14	90	1077	S<470>	-457	108.5	14	90
898	S<625>	2333	108.5	14	90	988	S<535>	1073	108.5	14	90	1078	S<469>	-471	234.5	14	90
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1087	S<460>	-597	108.5	14	90	1177	S<370>	-1857	108.5	14	90	1267	S<280>	-3117	108.5	14	90
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1169	S<378>	-1745	108.5	14	90	1259	S<288>	-3005	108.5	14	90	1349	S<198>	-4265	108.5	14	90
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No	Name	X-axis	Y-axis	Width	Hight	No	Name	X-axis	Y-axis	Width	Hight	No	Name	X-axis	Y-axis	Width	Hight
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1352	S<195>	-4307	234.5	14	90	1442	S<105>	-5567	234.5	14	90	1532	S<15>	-6827	234.5	14	90
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1361	S<186>	-4433	108.5	14	90	1451	S<96>	-5693	108.5	14	90	1541	S<6>	-6953	108.5	14	90
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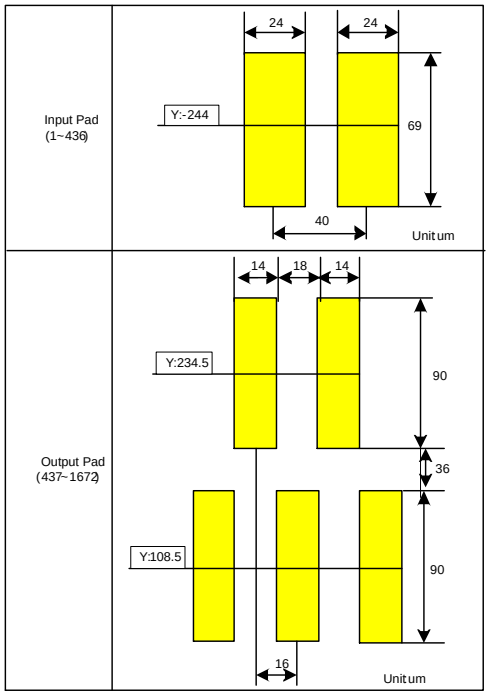
1372	S<175>	-4587	234.5	14	90	1462	S<85>	-5847	234.5	14	90	1552	G<3>	-7115	234.5	14	90
1373	S<174>	-4601	108.5	14	90	1463	S<84>	-5861	108.5	14	90	1553	G<5>	-7131	108.5	14	90
1374	S<173>	-4615	234.5	14	90	1464	S<83>	-5875	234.5	14	90	1554	G<7>	-7147	234.5	14	90
1375	S<172>	-4629	108.5	14	90	1465	S<82>	-5889	108.5	14	90	1555	G<9>	-7163	108.5	14	90
1376	S<171>	-4643	234.5	14	90	1466	S<81>	-5903	234.5	14	90	1556	G<11>	-7179	234.5	14	90
1377	S<170>	-4657	108.5	14	90	1467	S<80>	-5917	108.5	14	90	1557	G<13>	-7195	108.5	14	90
1378	S<169>	-4671	234.5	14	90	1468	S<79>	-5931	234.5	14	90	1558	G<15>	-7211	234.5	14	90
1379	S<168>	-4685	108.5	14	90	1469	S<78>	-5945	108.5	14	90	1559	G<17>	-7227	108.5	14	90
1380	S<167>	-4699	234.5	14	90	1470	S<77>	-5959	234.5	14	90	1560	G<19>	-7243	234.5	14	90
1381	S<166>	-4713	108.5	14	90	1471	S<76>	-5973	108.5	14	90	1561	G<21>	-7259	108.5	14	90
1382	S<165>	-4727	234.5	14	90	1472	S<75>	-5987	234.5	14	90	1562	G<23>	-7275	234.5	14	90
1383	S<164>	-4741	108.5	14	90	1473	S<74>	-6001	108.5	14	90	1563	G<25>	-7291	108.5	14	90
1384	S<163>	-4755	234.5	14	90	1474	S<73>	-6015	234.5	14	90	1564	G<27>	-7307	234.5	14	90
1385	S<162>	-4769	108.5	14	90	1475	S<72>	-6029	108.5	14	90	1565	G<29>	-7323	108.5	14	90
1386	S<161>	-4783	234.5	14	90	1476	S<71>	-6043	234.5	14	90	1566	G<31>	-7339	234.5	14	90
1387	S<160>	-4797	108.5	14	90	1477	S<70>	-6057	108.5	14	90	1567	G<33>	-7355	108.5	14	90
1388	S<159>	-4811	234.5	14	90	1478	S<69>	-6071	234.5	14	90	1568	G<35>	-7371	234.5	14	90
1389	S<158>	-4825	108.5	14	90	1479	S<68>	-6085	108.5	14	90	1569	G<37>	-7387	108.5	14	90
1390	S<157>	-4839	234.5	14	90	1480	S<67>	-6099	234.5	14	90	1570	G<39>	-7403	234.5	14	90
1391	S<156>	-4853	108.5	14	90	1481	S<66>	-6113	108.5	14	90	1571	G<41>	-7419	108.5	14	90
1392	S<155>	-4867	234.5	14	90	1482	S<65>	-6127	234.5	14	90	1572	G<43>	-7435	234.5	14	90
1393	S<154>	-4881	108.5	14	90	1483	S<64>	-6141	108.5	14	90	1573	G<45>	-7451	108.5	14	90
1394	S<153>	-4895	234.5	14	90	1484	S<63>	-6155	234.5	14	90	1574	G<47>	-7467	234.5	14	90
1395	S<152>	-4909	108.5	14	90	1485	S<62>	-6169	108.5	14	90	1575	G<49>	-7483	108.5	14	90
1396	S<151>	-4923	234.5	14	90	1486	S<61>	-6183	234.5	14	90	1576	G<51>	-7499	234.5	14	90
1397	S<150>	-4937	108.5	14	90	1487	S<60>	-6197	108.5	14	90	1577	G<53>	-7515	108.5	14	90
1398	S<149>	-4951	234.5	14	90	1488	S<59>	-6211	234.5	14	90	1578	G<55>	-7531	234.5	14	90
1399	S<148>	-4965	108.5	14	90	1489	S<58>	-6225	108.5	14	90	1579	G<57>	-7547	108.5	14	90
1400	S<147>	-4979	234.5	14	90	1490	S<57>	-6239	234.5	14	90	1580	G<59>	-7563	234.5	14	90
1401	S<146>	-4993	108.5	14	90	1491	S<56>	-6253	108.5	14	90	1581	G<61>	-7579	108.5	14	90
1402	S<145>	-5007	234.5	14	90	1492	S<55>	-6267	234.5	14	90	1582	G<63>	-7595	234.5	14	90
1403	S<144>	-5021	108.5	14	90	1493	S<54>	-6281	108.5	14	90	1583	G<65>	-7611	108.5	14	90
1404	S<143>	-5035	234.5	14	90	1494	S<53>	-6295	234.5	14	90	1584	G<67>	-7627	234.5	14	90
1405	S<142>	-5049	108.5	14	90	1495	S<52>	-6309	108.5	14	90	1585	G<69>	-7643	108.5	14	90
1406	S<141>	-5063	234.5	14	90	1496	S<51>	-6323	234.5	14	90	1586	G<71>	-7659	234.5	14	90
1407	S<140>	-5077	108.5	14	90	1497	S<50>	-6337	108.5	14	90	1587	G<73>	-7675	108.5	14	90
1408	S<139>	-5091	234.5	14	90	1498	S<49>	-6351	234.5	14	90	1588	G<75>	-7691	234.5	14	90
1409	S<138>	-5105	108.5	14	90	1499	S<48>	-6365	108.5	14	90	1589	G<77>	-7707	108.5	14	90
1410	S<137>	-5119	234.5	14	90	1500	S<47>	-6379	234.5	14	90	1590	G<79>	-7723	234.5	14	90
1411	S<136>	-5133	108.5	14	90	1501	S<46>	-6393	108.5	14	90	1591	G<81>	-7739	108.5	14	90
1412	S<135>	-5147	234.5	14	90	1502	S<45>	-6407	234.5	14	90	1592	G<83>	-7755	234.5	14	90
1413	S<134>	-5161	108.5	14	90	1503	S<44>	-6421	108.5	14	90	1593	G<85>	-7771	108.5	14	90
1414	S<133>	-5175	234.5	14	90	1504	S<43>	-6435	234.5	14	90	1594	G<87>	-7787	234.5	14	90
1415	S<132>	-5189	108.5	14	90	1505	S<42>	-6449	108.5	14	90	1595	G<89>	-7803	108.5	14	90
1416	S<131>	-5203	234.5	14	90	1506	S<41>	-6463	234.5	14	90	1596	G<91>	-7819	234.5	14	90
1417	S<130>	-5217	108.5	14	90	1507	S<40>	-6477	108.5	14	90	1597	G<93>	-7835	108.5	14	90
1418	S<129>	-5231	234.5	14	90	1508	S<39>	-6491	234.5	14	90	1598	G<95>	-7851	234.5	14	90
1419	S<128>	-5245	108.5	14	90	1509	S<38>	-6505	108.5	14	90	1599	G<97>	-7867	108.5	14	90
1420	S<127>	-5259	234.5	14	90	1510	S<37>	-6519	234.5	14	90	1600	G<99>	-7883	234.5	14	90
1421	S<126>	-5273	108.5	14	90	1511	S<36>	-6533	108.5	14	90	1601	G<101>	-7899	108.5	14	90
1422	S<125>	-5287	234.5	14	90	1512	S<35>	-6547	234.5	14	90	1602	G<103>	-7915	234.5	14	90
1423	S<124>	-5301	108.5	14	90	1513	S<34>	-6561	108.5	14	90	1603	G<105>	-7931	108.5	14	90
1424	S<123>	-5315	234.5	14	90	1514	S<33>	-6575	234.5	14	90	1604	G<107>	-7947	234.5	14	90
1425	S<122>	-5329	108.5	14	90	1515	S<32>	-6589	108.5	14	90	1605	G<109>	-7963	108.5	14	90
1426	S<121>	-5343	234.5	14	90	1516	S<31>	-6603	234.5	14	90	1606	G<111>	-7979	234.5	14	90
1427	S<120>	-5357	108.5	14	90	1517	S<30>	-6617	108.5	14	90	1607	G<113>	-7995	108.5	14	90
1428	S<119>	-5371	234.5	14	90	1518	S<29>	-6631	234.5	14	90	1608	G<115>	-8011	234.5	14	90
1429	S<118>	-5385	108.5	14	90	1519	S<28>	-6645	108.5	14	90	1609	G<117>	-8027	108.5	14	90
1430	S<117>	-5399	234.5	14	90	1520	S<27>	-6659	234.5	14	90	1610	G<119>	-8043	234.5	14	90
1431	S<116>	-5413	108.5	14	90	1521	S<26>	-6673	108.5	14	90	1611	G<121>	-8059	108.5	14	90
1432	S<115>	-5427	234.5	14	90	1522	S<25>	-6687	234.5	14	90	1612	G<123>	-8075	234.5	14	90
1433	S<114>	-5441	108.5	14	90	1523	S<24>	-6701	108.5	14	90	1613	G<125>	-8091	108.5	14	90
1434	S<113>	-5455	234.5	14	90	1524	S<23>	-6715	234.5	14	90	1614	G<127>	-8107	234.5	14	90
1435	S<112>	-5469	108.5	14	90	1525	S<22>	-6729	108.5	14	90	1615	G<129>	-8123	108.5	14	90
1436	S<111>	-5483	234.5	14	90	1526	S<21>	-6743	234.5	14	90	1616	G<131>	-8139	234.5	14	90
1437	S<110>	-5497	108.5	14	90	1527	S<20>	-6757	108.5	14	90	1617	G<133>	-8155	108.5	14	90
1438	S<109>	-5511	234.5	14	90	1528	S<19>	-6771	234.5	14	90	1618	G<135>	-8171	234.5	14	90
1439	S<108>	-5525	108.5	14	90	1529	S<18>	-6785	108.5	14	90	1619	G<137>	-8187	108.5	14	90
1440	S<107>	-5539	234.5	14	90	1530	S<17>	-6799	234.5	14	90	1620	G<139>	-8203	234.5	14	90

No	Name	X-axis	Y-axis	Width	Hight
1621	G<141>	-8219	108.5	14	90
1622	G<143>	-8235	234.5	14	90
1623	G<145>	-8251	108.5	14	90
1624	G<147>	-8267	234.5	14	90
1625	G<149>	-8283	108.5	14	90
1626	G<151>	-8299	234.5	14	90
1627	G<153>	-8315	108.5	14	90
1628	G<155>	-8331	234.5	14	90
1629	G<157>	-8347	108.5	14	90
1630	G<159>	-8363	234.5	14	90
1631	G<161>	-8379	108.5	14	90
1632	G<163>	-8395	234.5	14	90
1633	G<165>	-8411	108.5	14	90
1634	G<167>	-8427	234.5	14	90
1635	G<169>	-8443	108.5	14	90
1636	G<171>	-8459	234.5	14	90
1637	G<173>	-8475	108.5	14	90
1638	G<175>	-8491	234.5	14	90
1639	G<177>	-8507	108.5	14	90
1640	G<179>	-8523	234.5	14	90
1641	G<181>	-8539	108.5	14	90
1642	G<183>	-8555	234.5	14	90
1643	G<185>	-8571	108.5	14	90
1644	G<187>	-8587	234.5	14	90
1645	G<189>	-8603	108.5	14	90
1646	G<191>	-8619	234.5	14	90
1647	G<193>	-8635	108.5	14	90
1648	G<195>	-8651	234.5	14	90
1649	G<197>	-8667	108.5	14	90
1650	G<199>	-8683	234.5	14	90
1651	G<201>	-8699	108.5	14	90
1652	G<203>	-8715	234.5	14	90
1653	G<205>	-8731	108.5	14	90
1654	G<207>	-8747	234.5	14	90
1655	G<209>	-8763	108.5	14	90
1656	G<211>	-8779	234.5	14	90
1657	G<213>	-8795	108.5	14	90
1658	G<215>	-8811	234.5	14	90
1659	G<217>	-8827	108.5	14	90
1660	G<219>	-8843	234.5	14	90
1661	G<221>	-8859	108.5	14	90
1662	G<223>	-8875	234.5	14	90
1663	G<225>	-8891	108.5	14	90
1664	G<227>	-8907	234.5	14	90
1665	G<229>	-8923	108.5	14	90
1666	G<231>	-8939	234.5	14	90
1667	G<233>	-8955	108.5	14	90
1668	G<235>	-8971	234.5	14	90
1669	G<237>	-8987	108.5	14	90
1670	G<239>	-9003	234.5	14	90
1671	DUMMY	-9019	108.5	14	90
1672	DUMMY	-9035	234.5	14	90

Name	X-axis	Y-axis
left mark	-9200	226.5
right mark	9200	226.5

BUMP Size



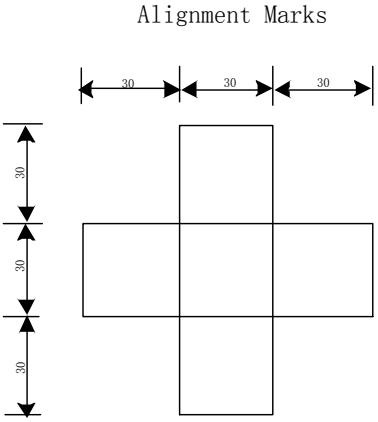
Chip Size: 18620um x 653um

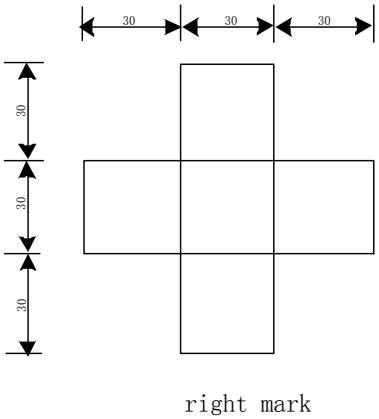
Chip thickness 250um(typ.)

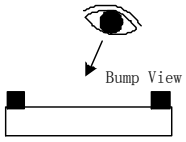
Pad Location: Pad Center

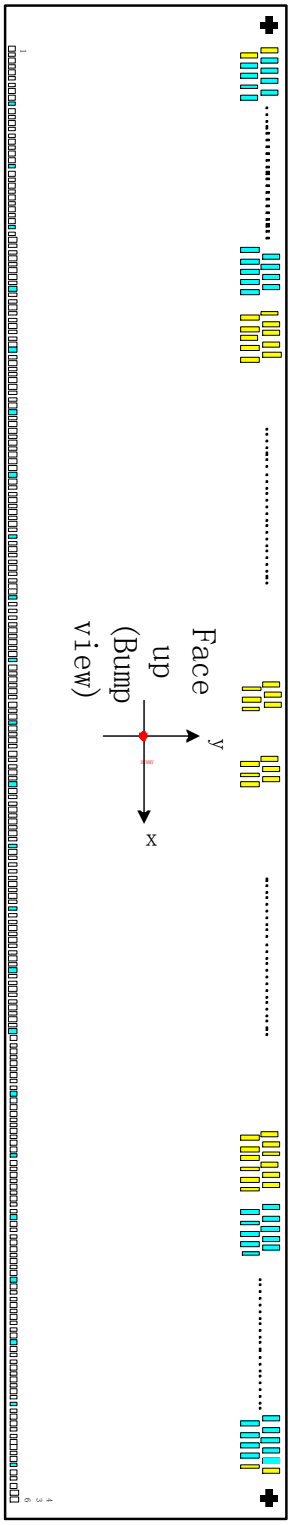
Coordinate Origin Chip center

Au bump height 9um(typ.)









4. Interface setting

4.1. MCU interfaces

GC9308 provides the 8-/9-/16-/18-bit parallel system interface for 8080-I /8080- II series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit formal per pixel color order is selected by DBI [2:0] 3-bits of 3Ah register.

4.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

Table 6

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	1	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX
0	1	1	0	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0],WRX,RDX,CSX,D/CX
0	1	0	1	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0],WRX,RDX,CSX,D/CX
0	1	1	1	8080 MCU 18-bit bus interface I	D[7:0]	D[17:0],WRX,RDX,CSX,D/CX
1	1	0	1	3-wire 9-bit data serial interface I	SCL,SDA,CSX	
				2 data lane serial interface I	SCL,SDA,CSX,D/CX	
1	1	1	1	4-wire 8-bit data serial interface I	SCL,SDA,D/CX,CSX	
0	0	1	0	8080 MCU 16-bit bus interface II	D[8:1]	D[17:10],D[8:1],WRX,RDX,CSX,D/CX
0	0	0	0	8080 MCU 8-bit bus interface II	D[17:10]	D[17:10],WRX,RDX,CSX,D/CX
0	0	1	1	8080 MCU 18-bit bus interface II	D[8:1]	D[17:0],WRX,RDX,CSX,D/CX
0	0	0	1	8080 MCU 9-bit bus interface II	D[17:10]	D[17:9],WRX,RDX,CSX,D/CX
1	0	0	1	3-wire 9-bit data serial interface II	SCL,SDI,SDO,CSX	
1	0	1	1	4-wire 8-bit data serial interface II	SCL,SDI,SDO,D/CX,CSX	
1	0	0	0	3-wire 9-bit data serial interface II	SCL,SDI,SDO,CSX	
1	1	1	0	4-wire 8-bit data serial interface II	SCL,SDI,SDO,CSX	

4.1.2. 8080-I Series Parallel Interface

GC9308 can be accessed via 8-/9-/16-/18-bit MCU 8080-I series parallel interface. The chip select CSX (active low) is used to enable or disable GC9308 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

GC9308 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D[17:0] bits are commands.

The 8080-I series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-I Interface selection is done when IM3 pin is low state (VSSC level). Interface bus width can be selected by IM [2:0] bits.
The selection of 8080-I series parallel interface is shown as the table in the following.

Table 7

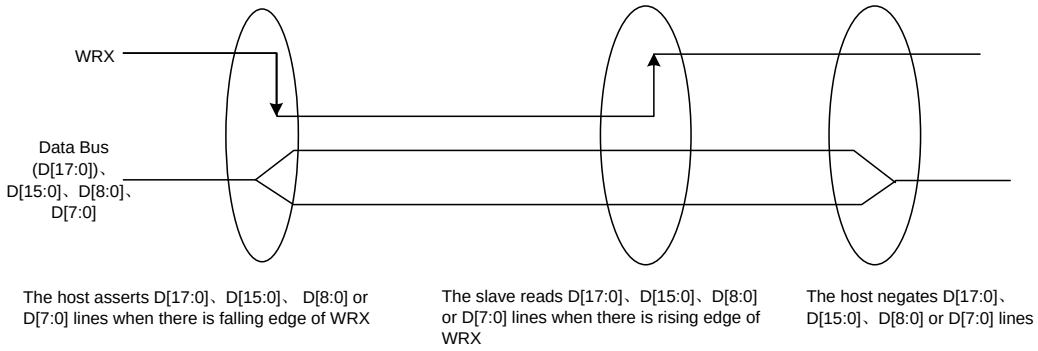
IM3	IM2	IM1	IM0	MCU-Interface	CSX	WRX	RDX	D/CX	Function
0	1	0	0	8080 MCU 8-bit bus interface I	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	1	0	8080 MCU 16-bit bus interface I	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	0	1	8080 MCU 9-bit bus interface I	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	1	1	8080 MCU 18-bit bus interface I	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

4.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is SRAM data or command's parameter.

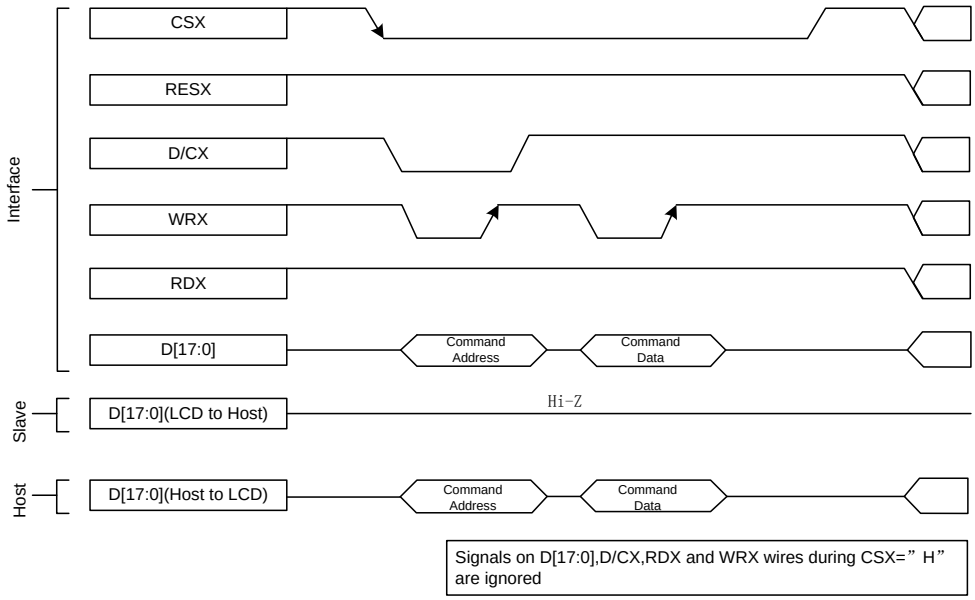
The following figure shows a write cycle for the 8080-I MCU interface.

Figure 2.



Note: WRX is an unsynchronized signal (It can be stopped)

Figure 3.

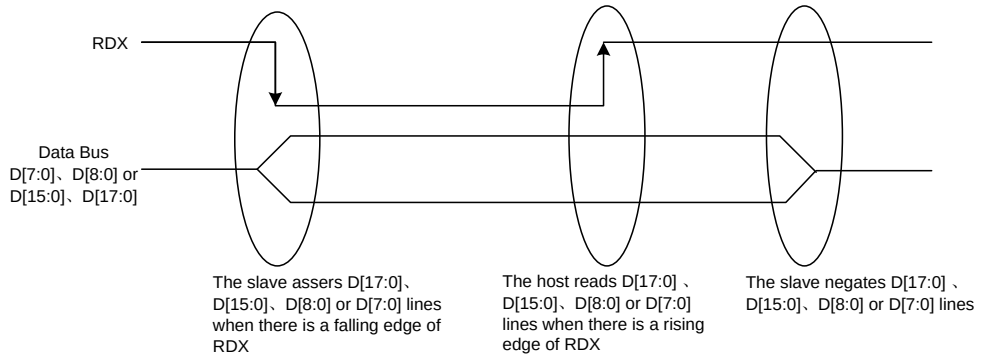


4.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle, while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

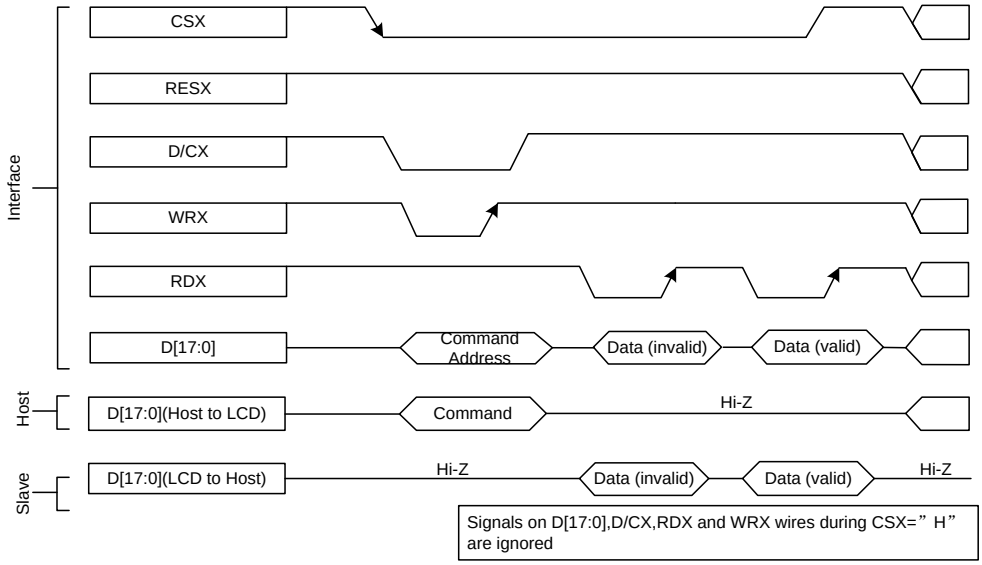
The following figure shows the read cycle for the 8080-I MCU interface.

Figure 4.



Note: RDX is an unsynchronized signal (It can be stopped).

Figure 5.



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

4.1.5. 8080-Ⅱ Series Parallel Interface

GC9308 can be accessed via 8-/9-/16-/18-bit MCU 8080-Ⅱ series parallel interface. The chip select CSX (active low) is used to enable or disable GC9308 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

GC9308 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D[17:0] bits are commands.

The 8080-II series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-II Interface selection is done when IM3 pin is high state (IOVCC level). Interface bus width can be selected by IM [2:0] bits.

The selection of 8080-II series parallel interface is shown as the table in the following.

Table 8

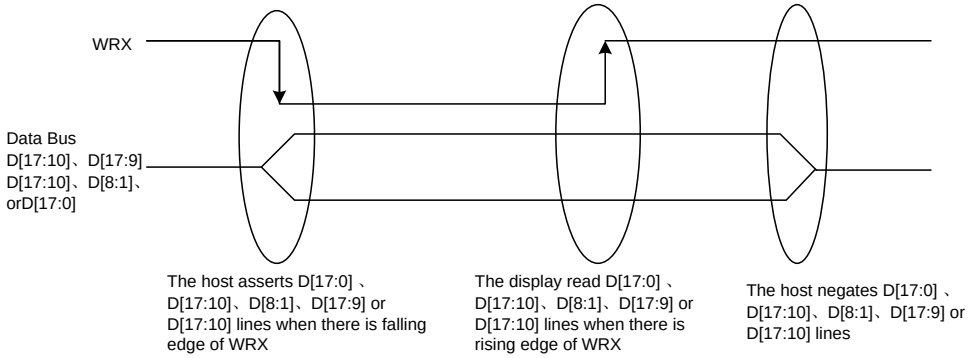
IM3	IM2	IM1	IM0	MCU-Interface	CSX	WRX	RDX	D/CX	Function
0	0	1	0	8080 MCU 16-bit bus interface II	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	0	0	8080 MCU 8-bit bus interface II	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	1	1	8080 MCU 18-bit bus interface II	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	0	1	8080 MCU 9-bit bus interface II	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

4.1.6. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

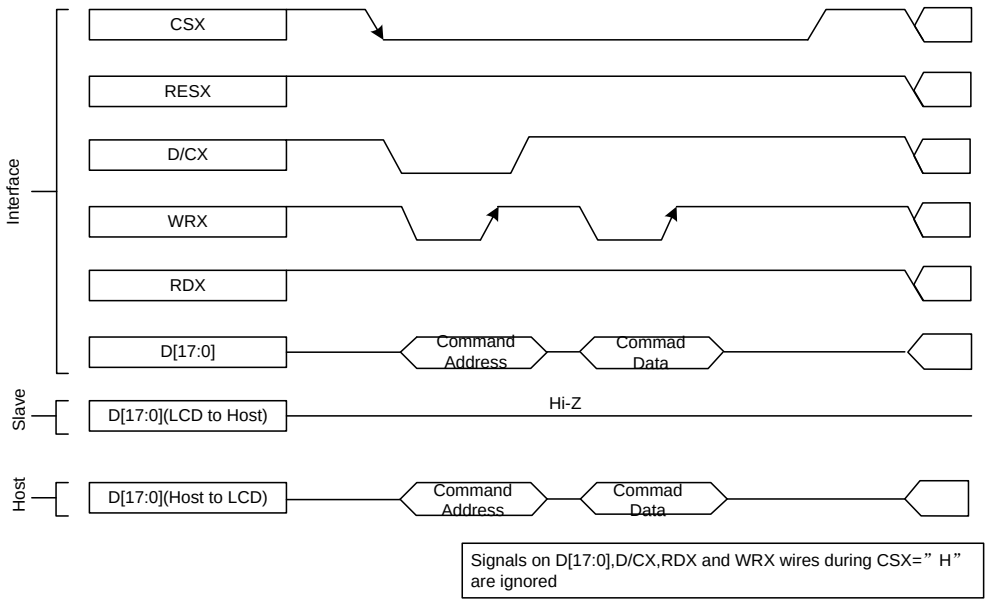
The following figure shows a write cycle for the 8080-II MCU interface.

Figure 6.



Note: WRX is an unsynchronized signal (It can be stopped)

Figure 7.

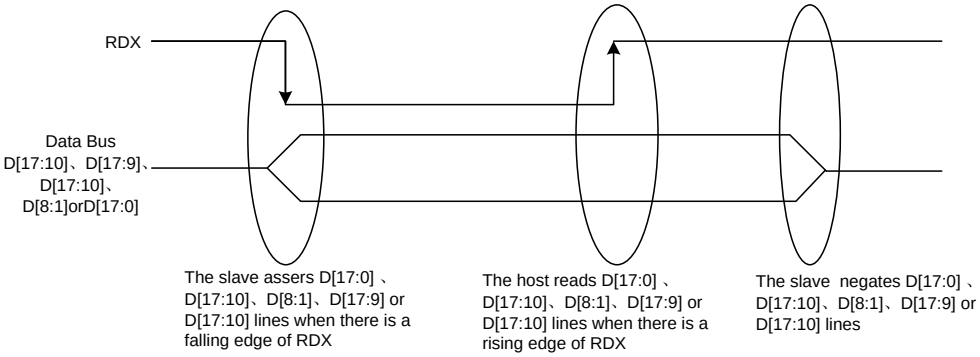


4.1.7. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

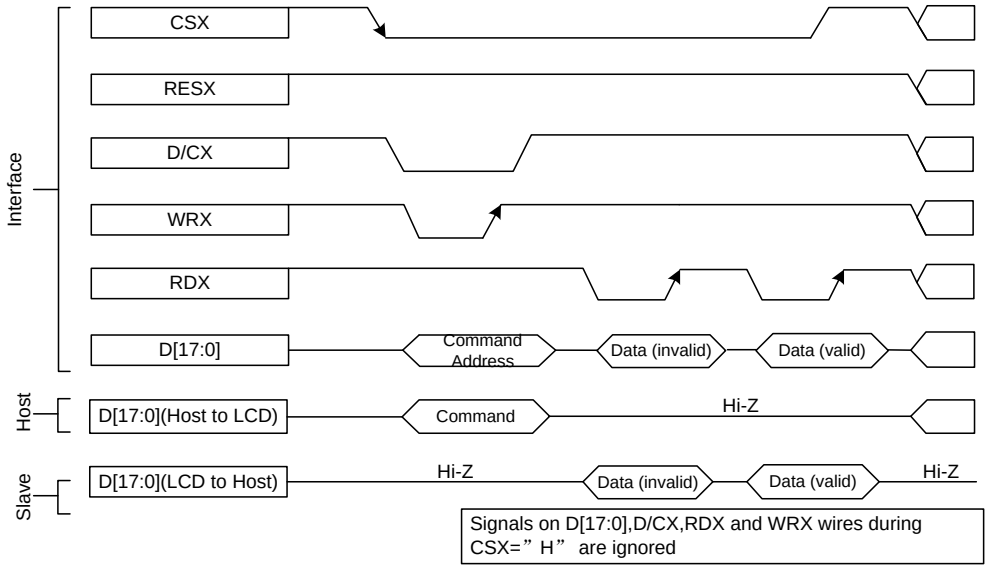
The following figure shows the read cycle for the 8080-II MCU interface.

Figure 8.



Note: RDX is an unsynchronized signal (It can be stopped).

Figure 9.



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

4.1.8. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

Table 8.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
1	1	0	1	3-line serial interface	“L”	-	↑	Read/Write command, parameter or display data.
1	1	1	1	4-line serial interface	“L”	"H/L"	↑	Read/Write command, parameter or display data.
1	0	0	1	3-line serial interface	“L”	-	↑	Read/Write command, parameter or display data.
1	0	1	1	4-line serial interface	“L”	"H/L"	↑	Read/Write command, parameter or display data.

GC9308 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and GC9308. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO). The 4-line serial mode consists of the Data/ Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

4.1.9. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to GC9308. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is “low”, the transmission byte is interpreted as a command byte. If the D/CX bit is “high”, the transmission byte is stored as the display data RAM(Memory write command),or command register as parameter.

Any instruction can be sent in any order to GC9308 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

Figure 10.

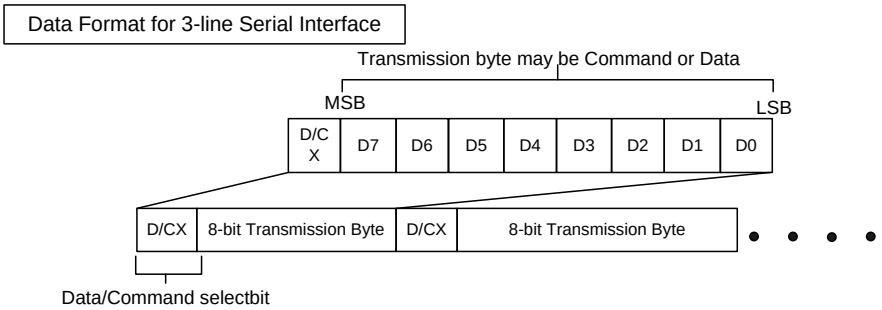
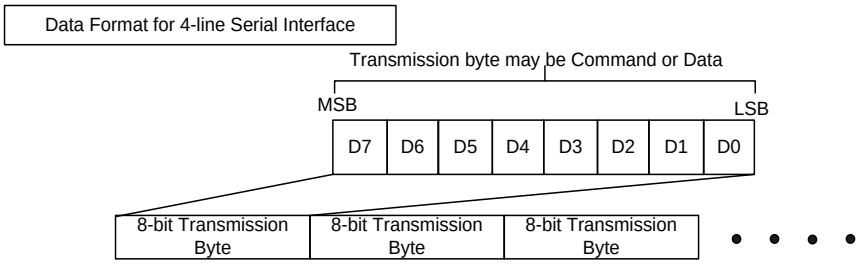


Figure11.



Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by GC9308 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

Figure 12.

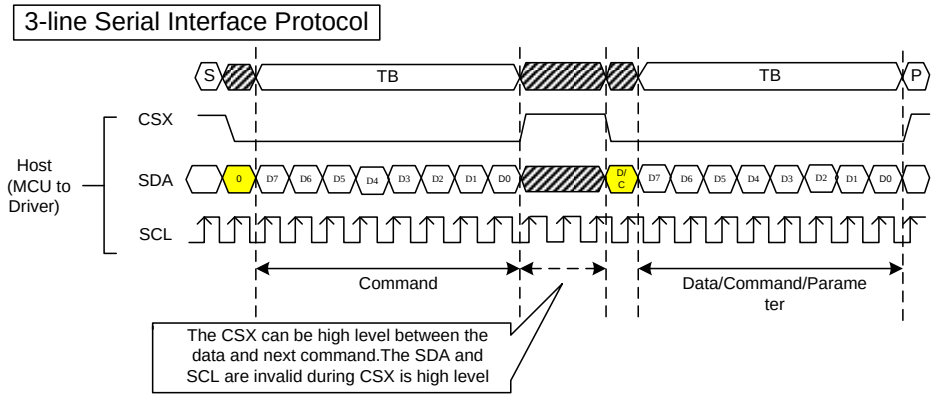
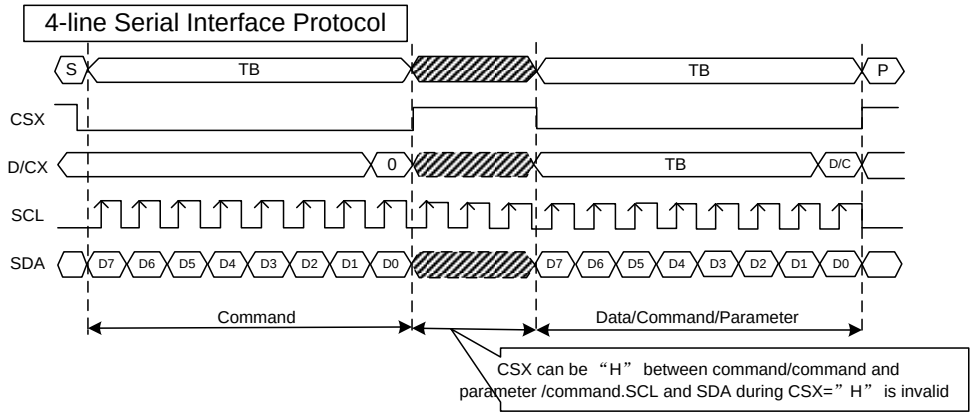


Figure 13.



4.1.10. Read Cycle Sequence

The read mode of interface means that the host reads register's parameter from GC9308. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. GC9308 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

Figure 14.

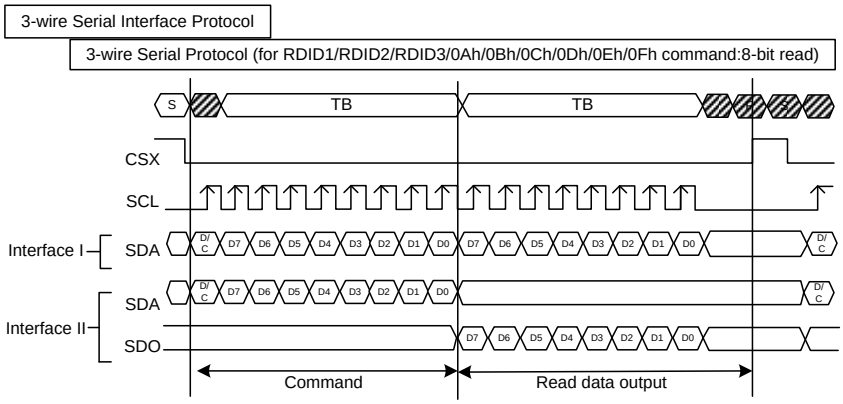


Figure 15.

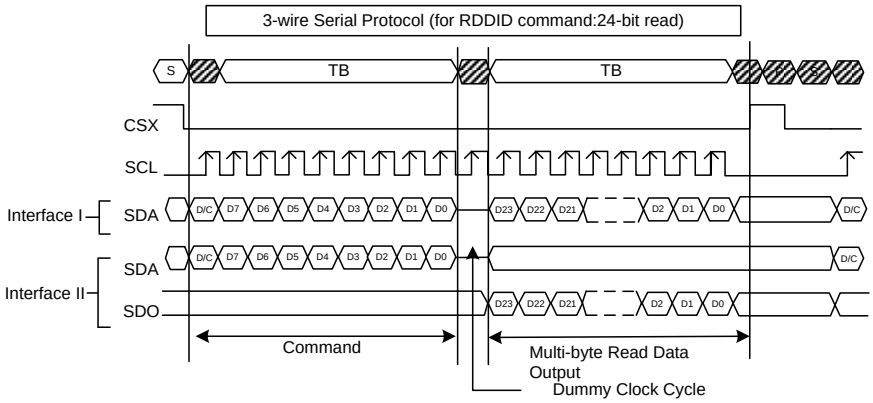


Figure 16.

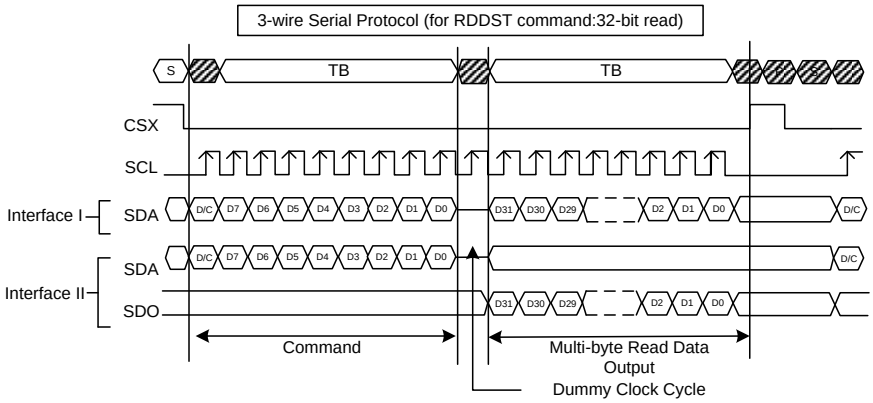


Figure 17.

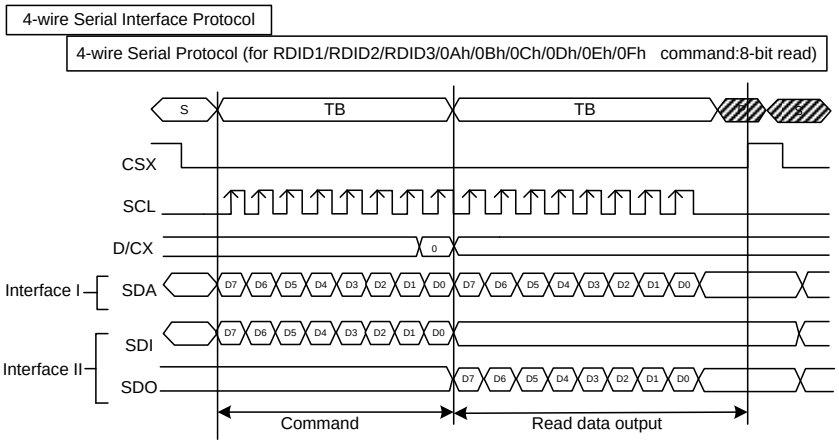


Figure 18.

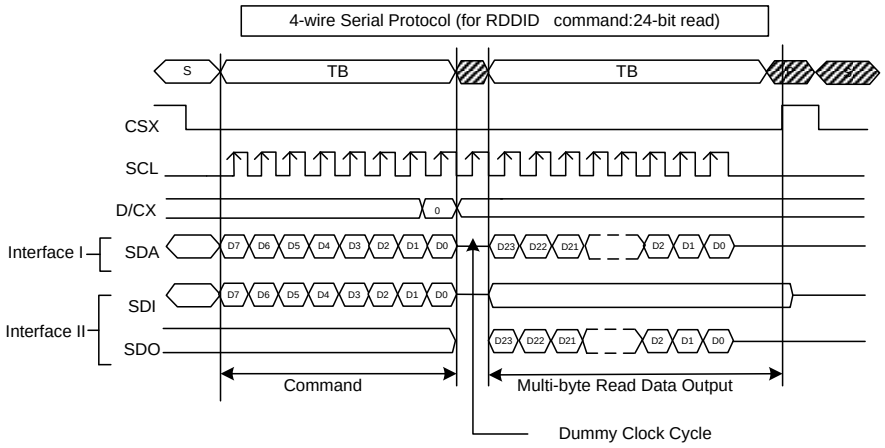
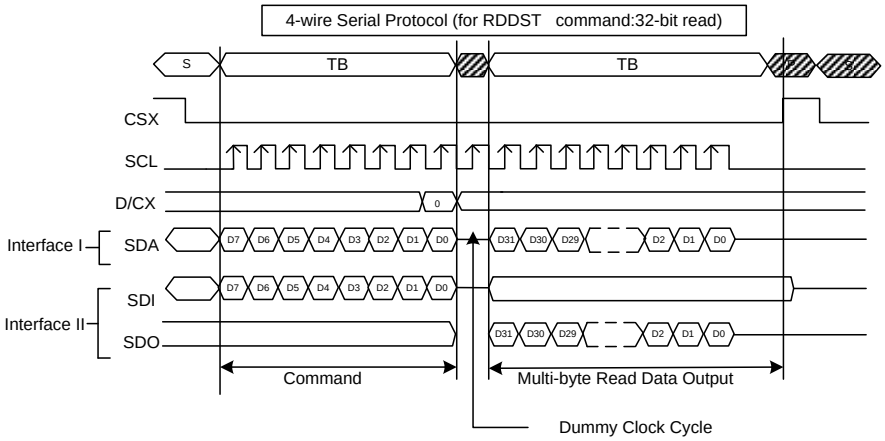


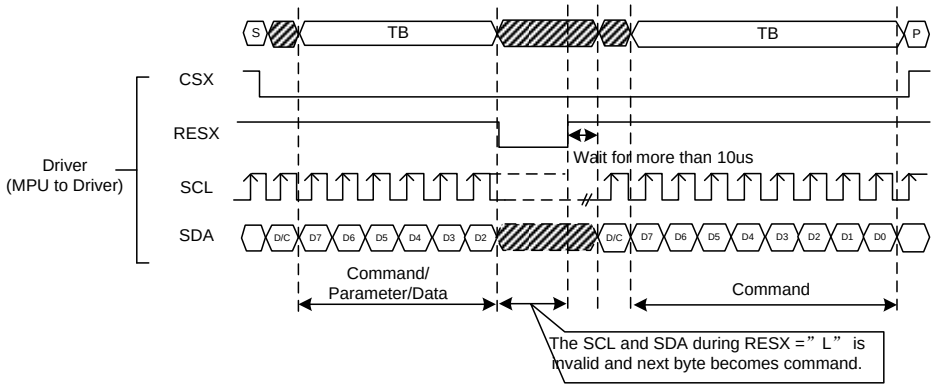
Figure 19.



4.1.11. Data Transfer Break and Recovery

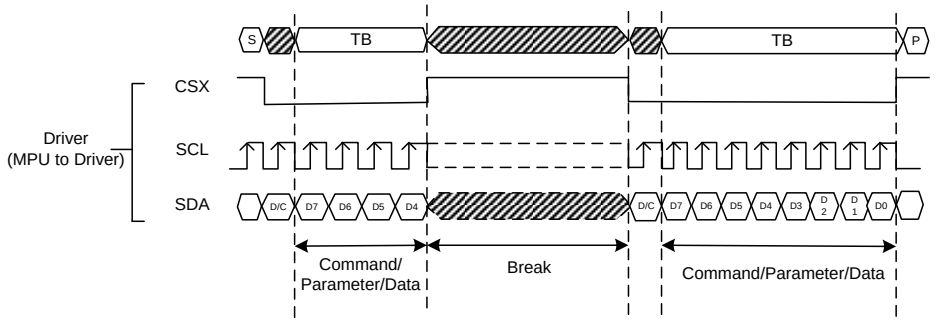
If there is a break in data transmission by RESX pulse, while transferring a command or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.

Figure 20.



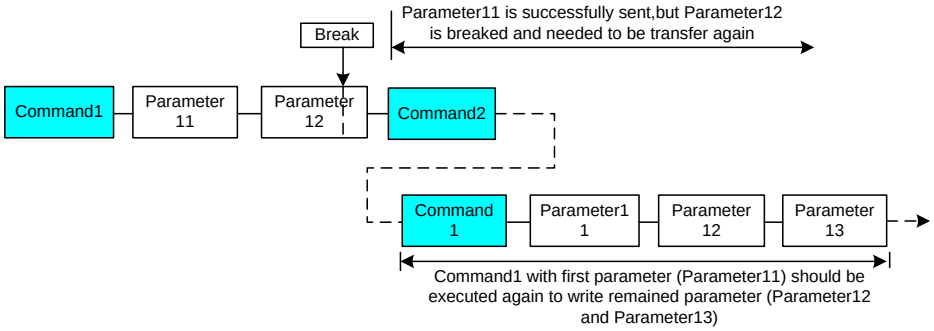
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.

Figure 21.



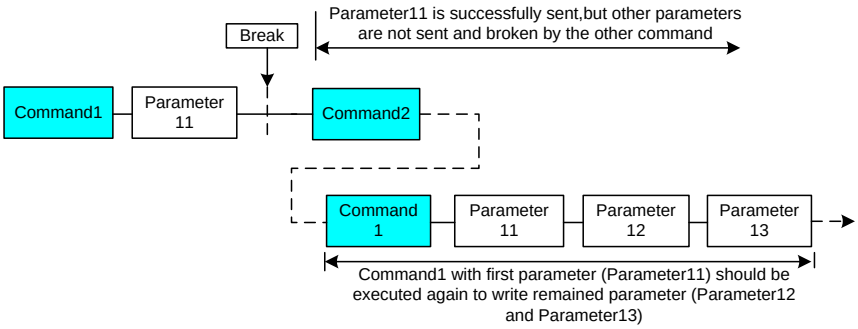
If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

Figure 22.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

Figure 23.

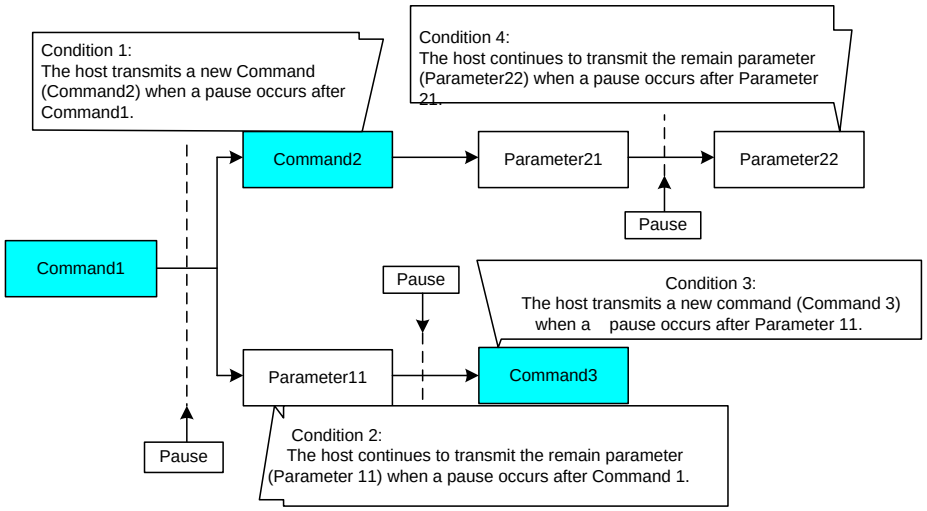


4.1.12. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then GC9308 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters(if appropriate) or a new command when the chip select pin is next enabled as shown below.

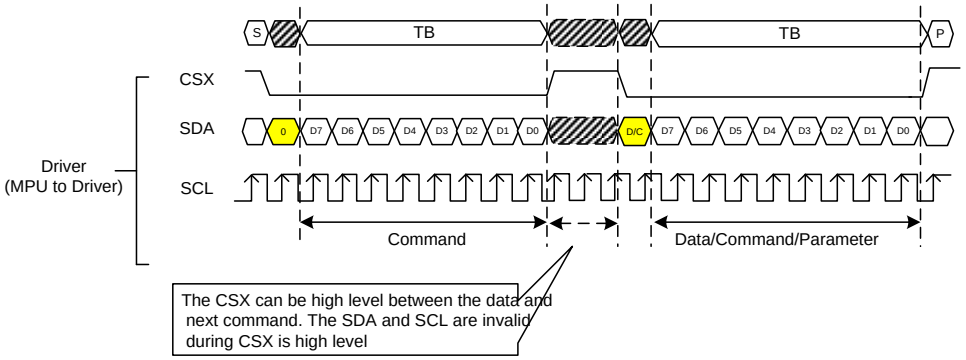
This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

Figure 24.



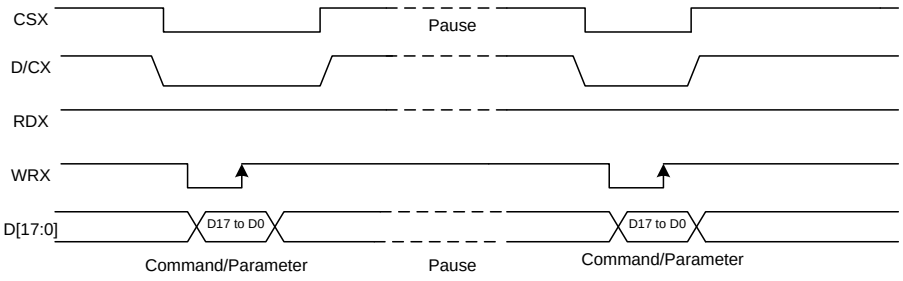
4.1.13. Serial Interface Pause (3_wire)

Figure 25.



4.1.14. Parallel Interface Pause

Figure 26.



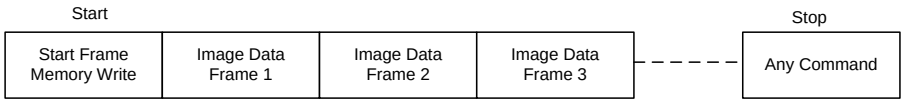
4.1.15. Data Transfer Mode

GC9308 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

4.1.16. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.

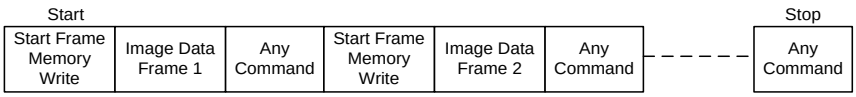
Figure 27.



4.1.17. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.

Figure 28.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.
Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

4.2. RGB Interface

4.2.1. RGB Interface Selection

GC9308 has two kinds of RGB interface and these interfaces can be selected by RCM [1:0] bits. When RCM [1:0] bits are set to “10”, the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM [1:0] bits are set to “11”, the SYNC mode is selected which utilizes which utilizes VSYNC, HSYNC,DOTCLK, D [17:0] pins. Using RGB interface must selection serial interface.
GC9308 supports several pixel formats that can be selected by RIM bit of F6h command. The selection of a given interfaces is done by setting RCM [1:0] as show in the following table.

Table 9

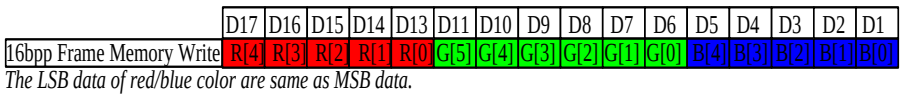
RCM[1:0]		RIM	DPI[1:0]			RGB interface Mode	RGB Mode	Used Pins
1	0	0	1	1	0	18-bit RGB interface (262K colors)	DE Mode Valid data is determined by the DE signal	VSYNC,HSYNC,DE,DOTCLK, D[17:0]
1	0	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC,HSYNC,DE,DOTCLK, D[17:13] & D[11:1]
1	0	1	-			6-bit RGB interface (262K colors)		VSYNC,HSYNC,DE,DOTCLK, D[5:0]
1	1	0	1	1	0	18-bit RGB interface (262K colors)	SYNC Mode In SYNC mode, DE signal is ignored;blanking porch is determined by B5h command	VSYNC,HSYNC,DOTCLK, D[17:0]
1	1	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC,HSYNC,DOTCLK, D[17:13] & D[11:1]
1	1	1	-			6-bit RGB interface (262K colors)		VSYNC,HSYNC,DOTCLK, D[5:0]

18-bit data bus interface (D[17:0] is used) , RIM=0

Figure 29.

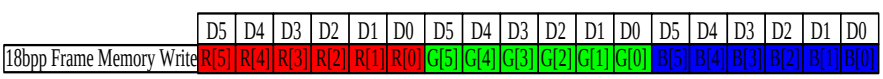
16-bit data bus interface (D[17:13] & D[11:1] is used) , DPI[2:0] = 101, and RIM=0

Figure 30.



6-bit data bus interface (D[5:0] is used) , RIM=1

Figure 31.



Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and

D[17:0] states when there is a rising edge of the DOTCLK. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= ’0’ (low) and there is a rising edge of DOTCLK). D [17:0] can be ‘0’ (low) or ‘1’ (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data in inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.

Figure32.

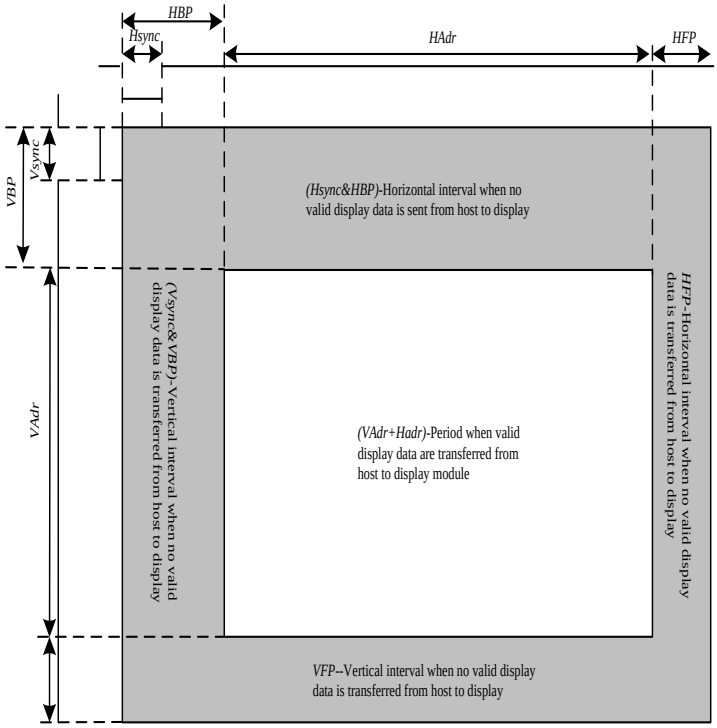


Table 10.

Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	320	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	240	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Notes:

1. Vertical period (one frame) shall be equal to the sum of VBP + VAdr + VFP.

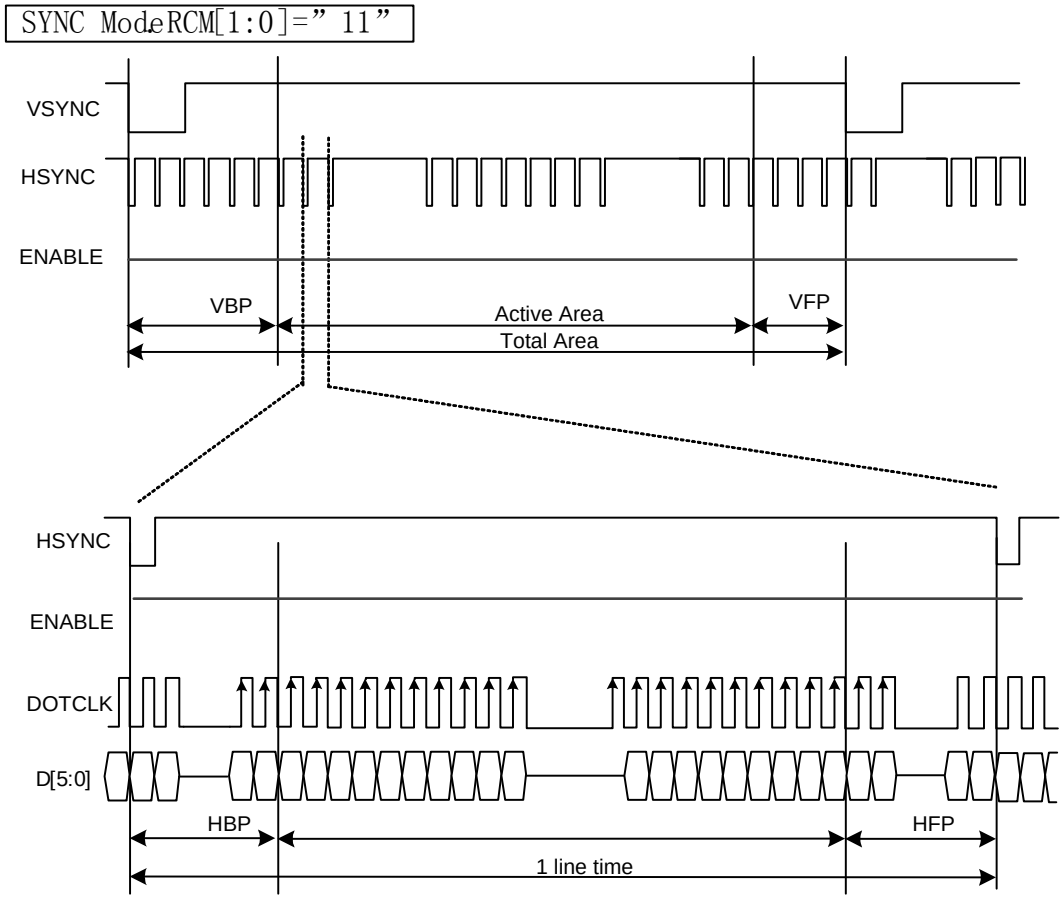
2. Horizontal period (one line) shall be equal to the sum of HBP + HAdr + HFP.

3. Control signals Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

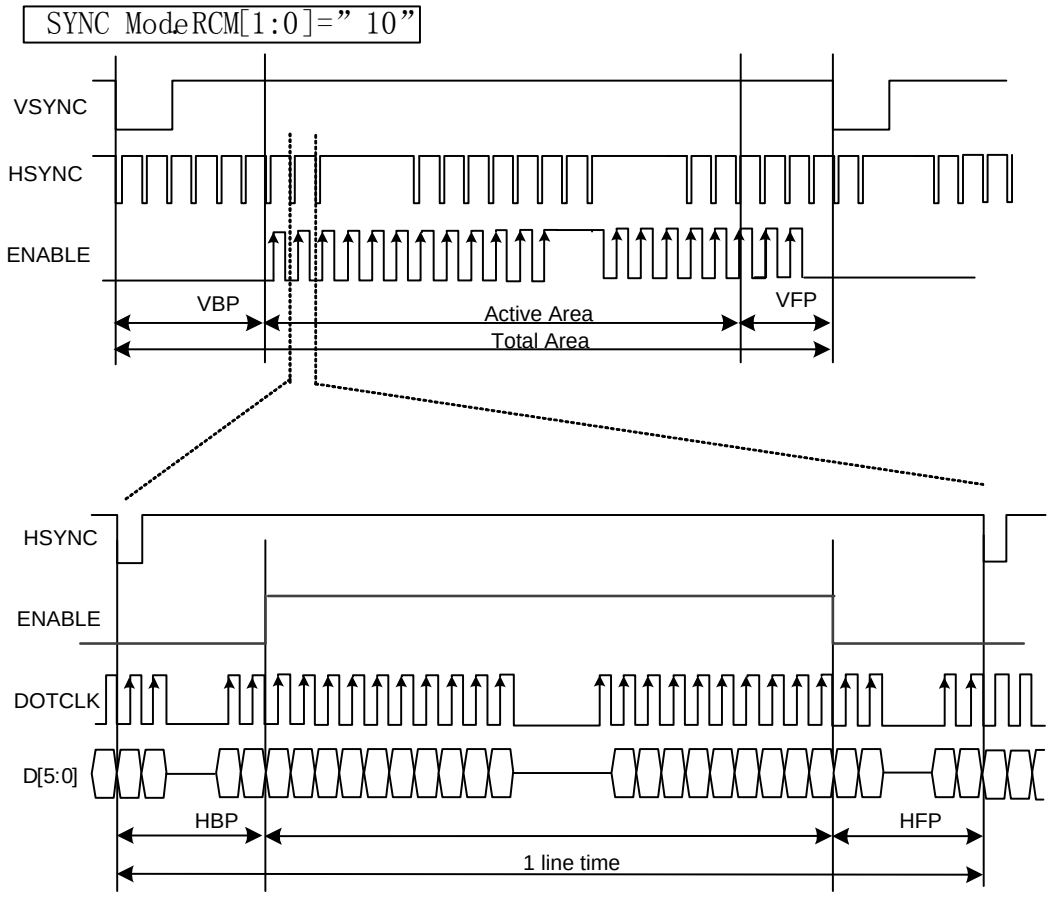
4.2.2. RGB Interface Timing

The timing chart of 18/16-bit RGB interface mode1 and mode 2 is shown as below.

Figure33.



Mode1 RGB SYNC mode



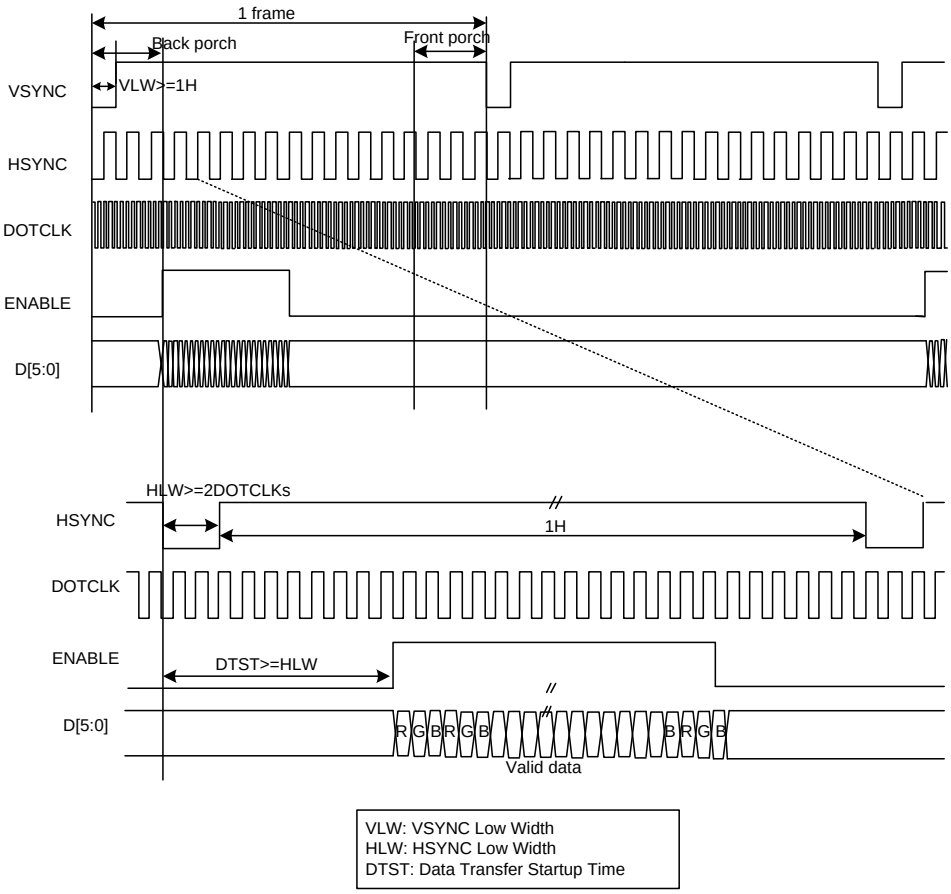
Mode2 RGB SYNC+DE mode

Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

The timing chart of 6-bit RGB interface mode is shown as below:

Figure34.



Note 1: 6-bit RGB interface mode only used in the DE interface.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

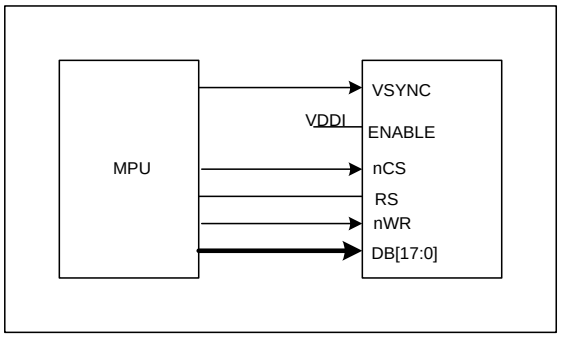
Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.

Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.

4.3. VSYNC Interface

GC9308 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the 8080-Ⅰ/8080-Ⅱ system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = “10” and RM = “0”.

Figure35.



Note 1:In the VSYNC mode,the pin ENABLE should connect to IOVCC.

In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.

Figure36.

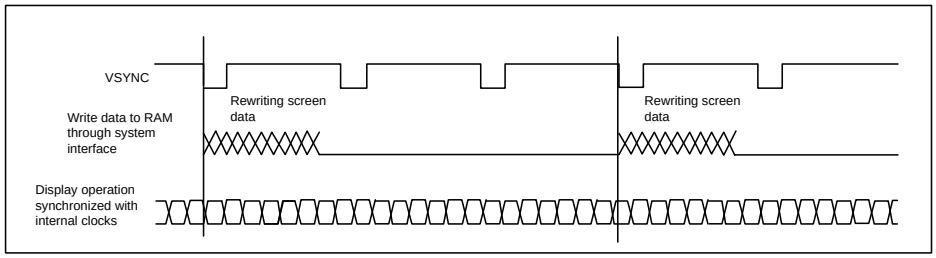
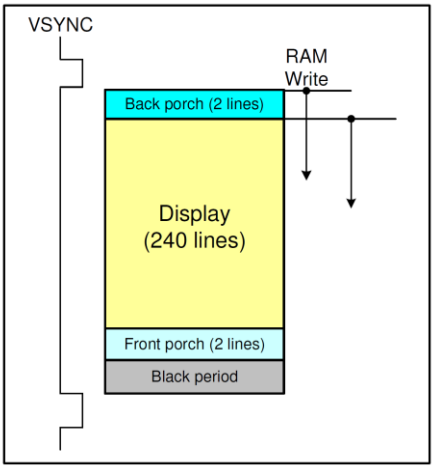


Figure37.



Notes in using the VSYNC interface

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into

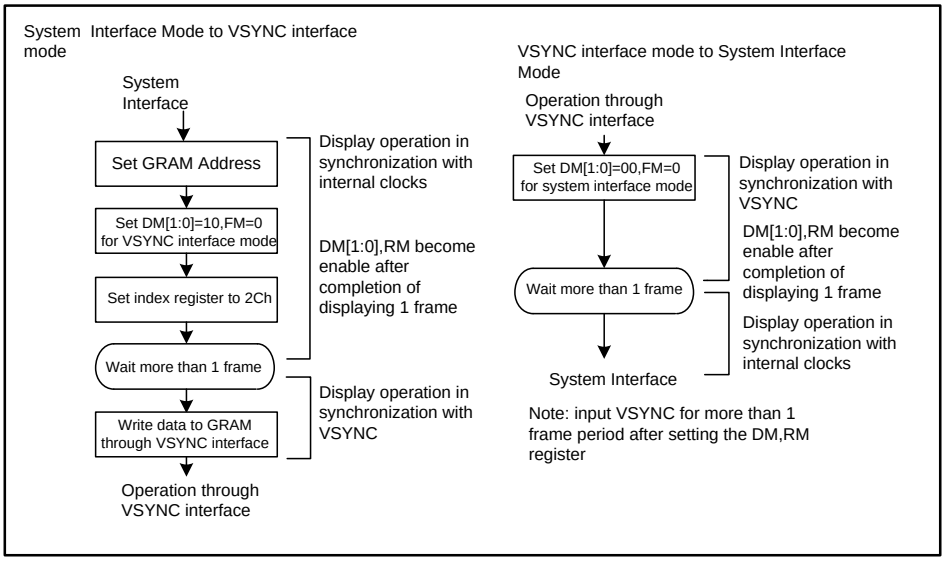
consideration.

2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.

3. When switching from the internal clock operation mode (DM[1:0] = “00”) to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.

4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.

Figure38.



4.4. Display Data RAM (DDRAM)

GC9308 has an integrated 320x240x18-bit graphic type static RAM. This 172,800-byte memory allows storing a 320xRGBx240 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

4.5. Display Data Format

GC9308 supplies 18-/16-/9-/8-bit parallel MCU interface with 8080-Ⅰ/8080-Ⅱ series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

4.5.1. 3-line Serial Interface

The 3-line/9-bit serial bus interface of GC9308 can be used by setting external pin as IM [3:0] to “1101” for serial interface. The shown figure is the example of 3-line SPI interface.

Figure39.

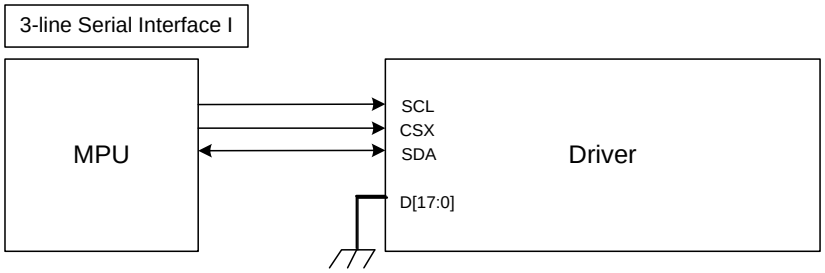
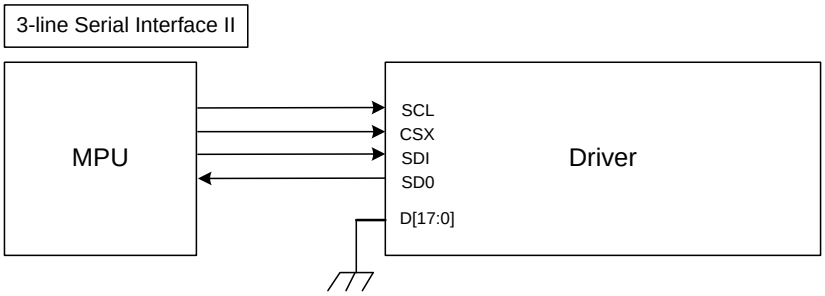


Figure40.



In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

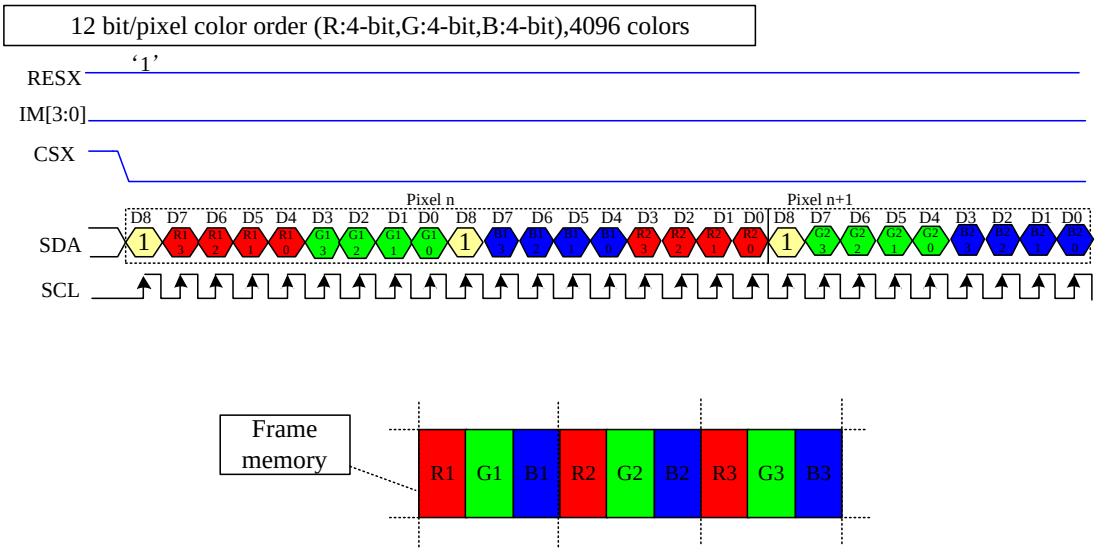
-4k colors, RGB 4, 4, 4 -bits input.

-65k colors, RGB 5, 6, 5 -bits input

-262k colors, RGB 6, 6, 6 -bits input.

1)4K-Colors:12-bit/pixel(RGB 4, 4, 4 -bits input).

Figure41.



Note 1: The pixel data with 12-bit color depth information.

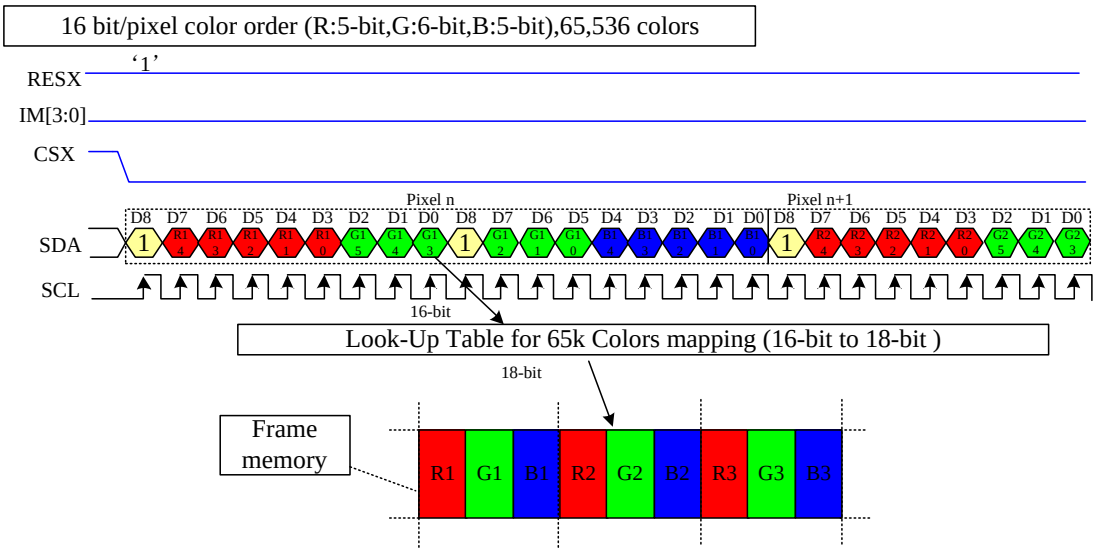
Note 2: The most significant bits are: Rx3, Gx3 and Bx3.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

2)65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

Figure41.



Note 1: The pixel data with 16-bit color depth information.

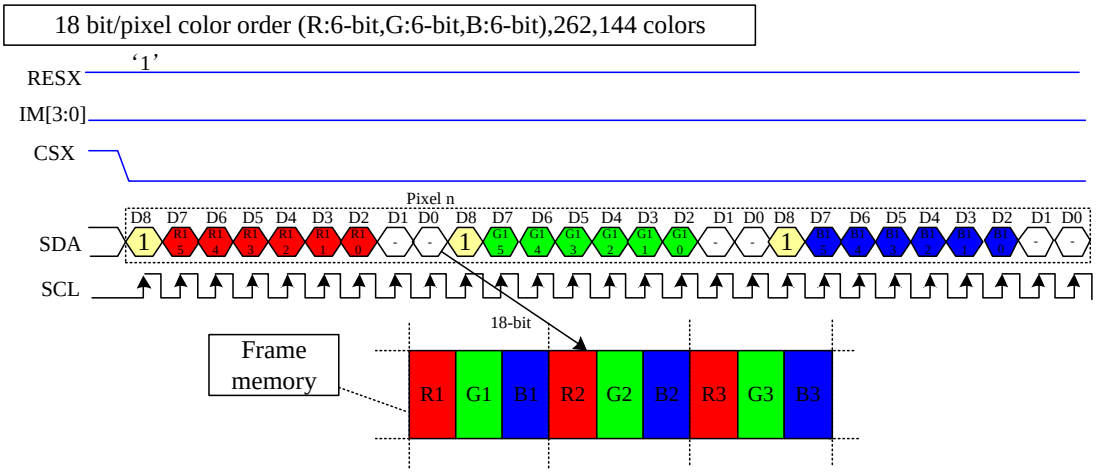
Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

3)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

Figure42.



Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care - Can be set "0" or "1".

4.5.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of GC9308 can be used by setting external pin as IM [3:0] to “1111” for serial interface . The shown figure is the example of 4-line SPI interface.

Figure43.

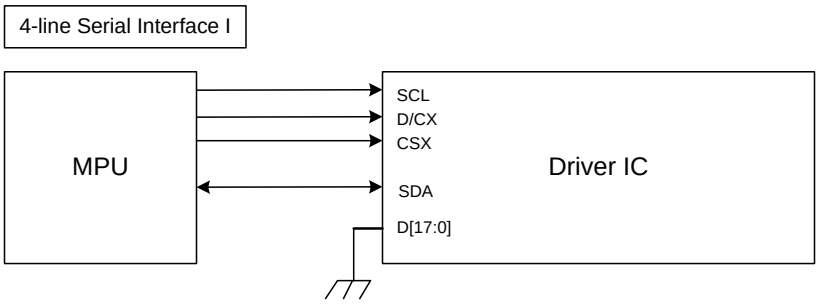
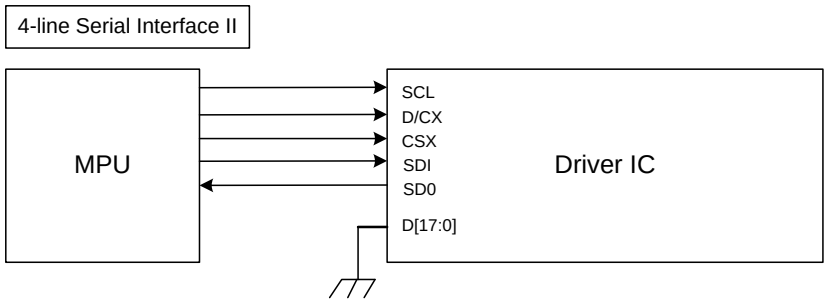


Figure44.



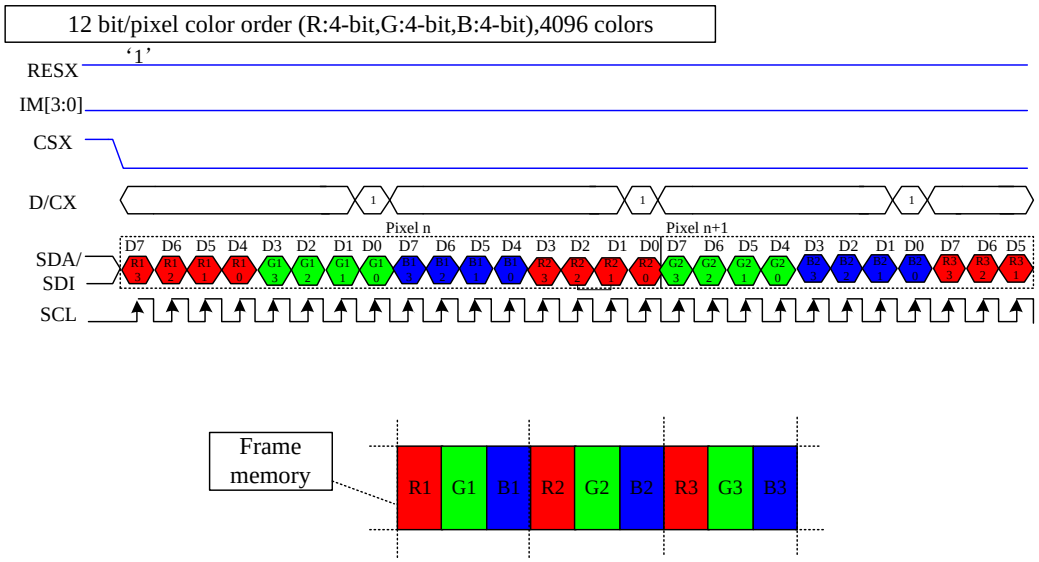
In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-4k colors, RGB 4, 4, 4 -bits input.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.

Figure44.



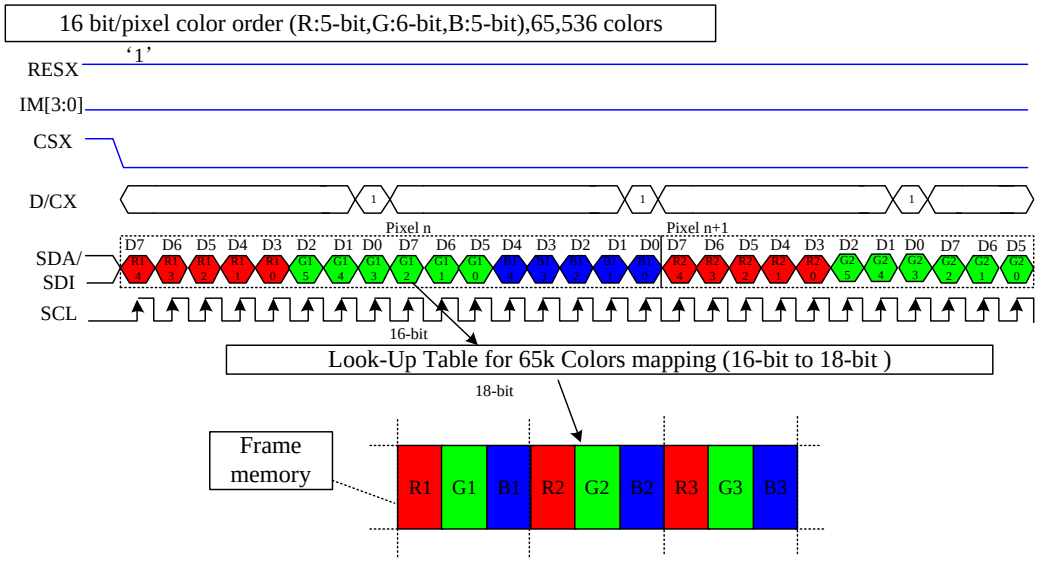
Note 1: The pixel data with 12-bit color depth information.

Note 2: The most significant bits are: Rx3, Gx3 and Bx3.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

Figure45.



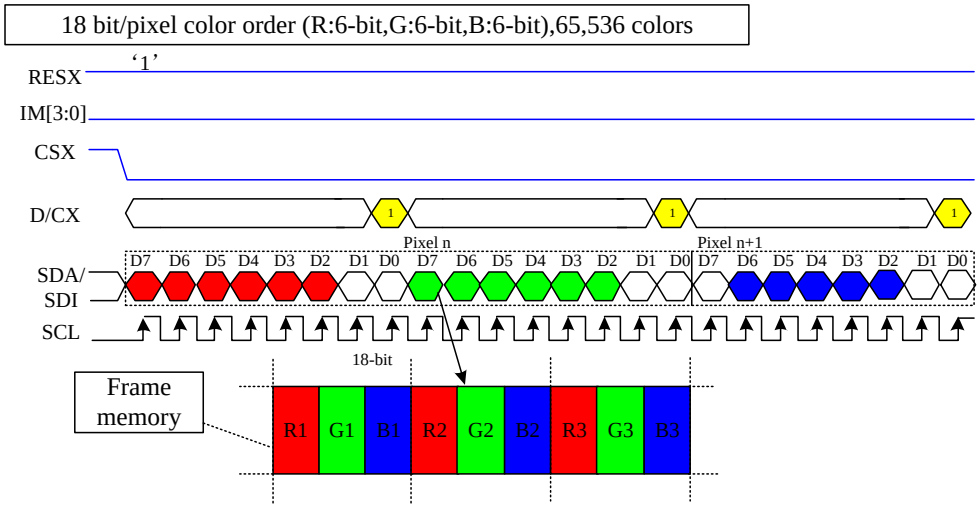
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

Figure46.



Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

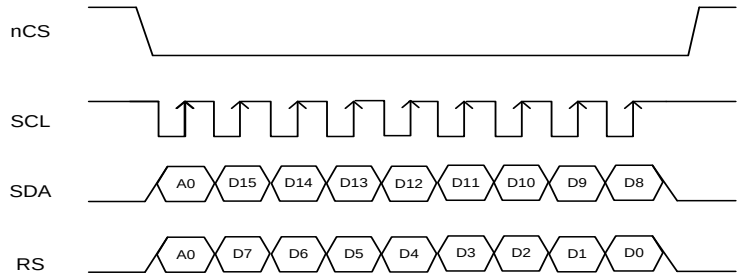
4.5.3. 2-data-line mode

This mode is active when 2data_en (E9h[3]) set to “1” in 3-wire. Only frame pixle data write transitions are sent in 2-data-line mode, register write/read is still sent in 3-wire.

The chip-select nCS (active low) enables and disables the serial interface. SCL is the serial data clock. SDA and DCX are serial data lines.

Serial data must be input to SDA in the sequence A0, D15 to D10 and DCX in the sequence A0, D7 to D0. The GC9308 reads the data at the rising edge of SCL signal. The first bit of serial data A0 is data/command flag. It must be set to "1", D15 to D0 bits are display RAM data.

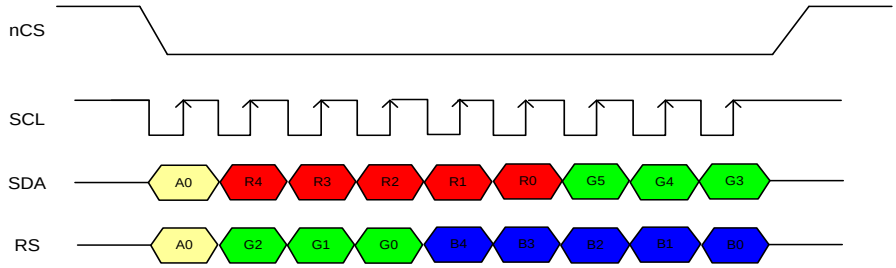
Figure47.



Five data formats are supported in 2-data-line mode, which is indicated by 2data_mdt (E9h[2:0]) .

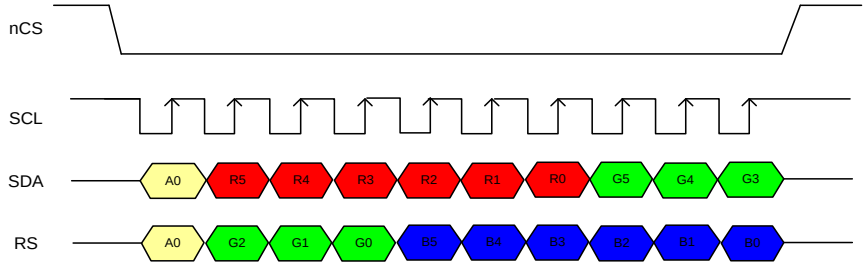
1)RGB565 1pixel/transition(65K color,2data_mdt[2:0]=’000’)

Figure48.



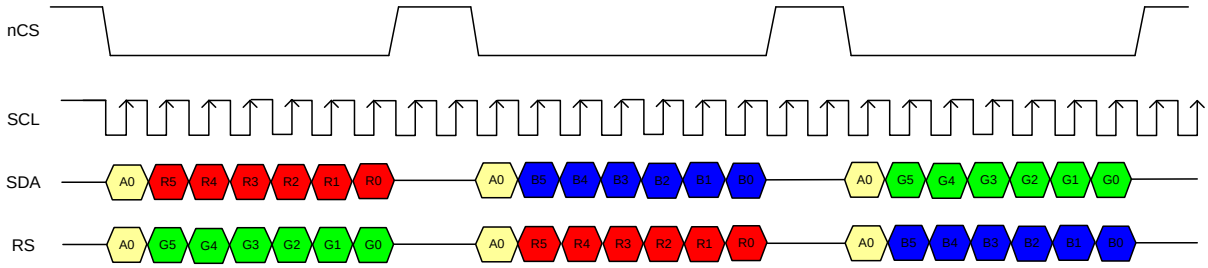
2)RGB666 1pixel/transition(262K color,2data_mdt[2:0]=’001’)

Figure49.



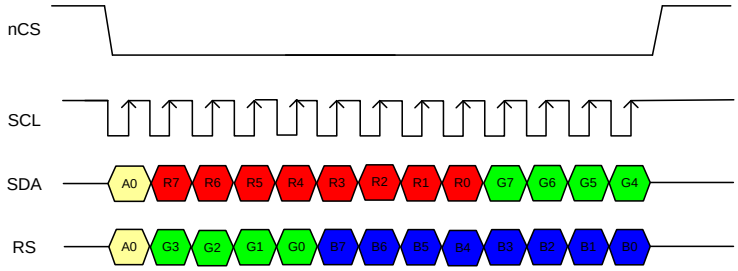
3)RGB666 2/3pixel/transition(262K color,2data_mdt[2:0]=’010’)

Figure50.



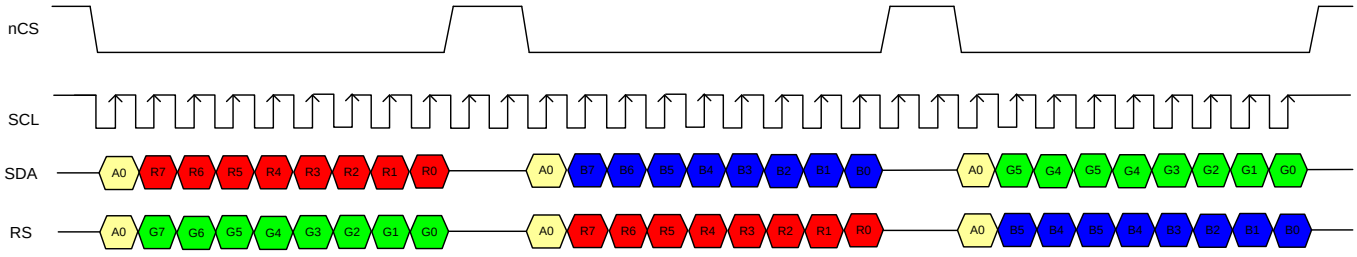
4)RGB888 1pixel/transition(4M color,2data_mdt[2:0]=’100’)

Figure51.



5)RGB888 2/3pixel/transition(4M color,2data_mdt[2:0]=’110’)

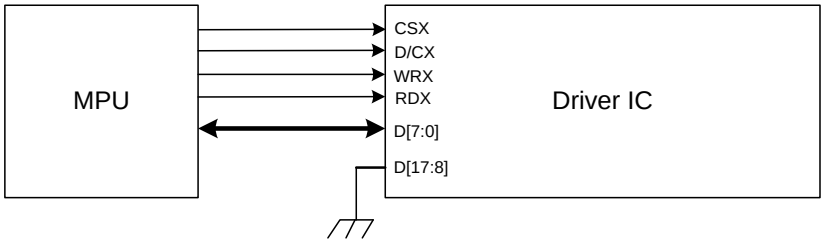
Figure52.



4.5.4. 8-bit Parallel MCU Interface

The 8080-Ⅰsystem 8-bit parallel bus interface of GC9308 can be used by setting external pin as IM [3:0] to“0000”.The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.

Figure53.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

Table 11.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

2) 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

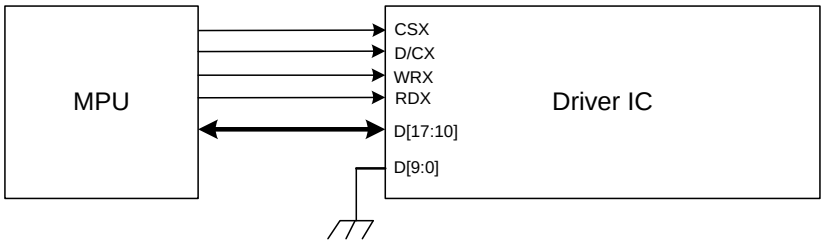
One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Table12.

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

The 8080-II system 8-bit parallel bus interface of GC9308 can be used by settings as IM [3:0] =”1001”. The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.

Figure54.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

Table13.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D16	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D15	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D14	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D13	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D12	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D11	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D10	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

2) 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to“110”.

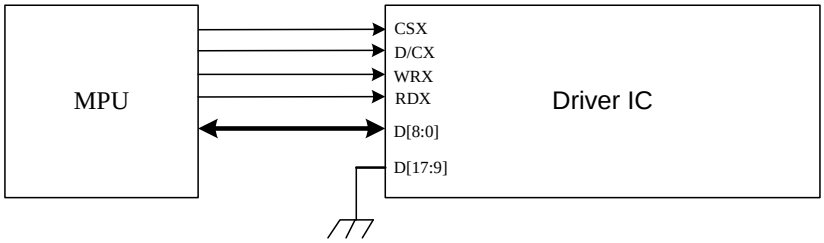
Table14.

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D17	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D16	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D15	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D14	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D13	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D12	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D11	C1				…			
D10	C0				…			

4.5.5. 9-bit Parallel MCU Interface

The 8080-I system 9-bit parallel bus interface of GC9308 can be selected by setting hardware pin IM [3:0] to "0010". The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.

Figure55.



1)262K-Colors,:18-bit/pixel(RGB 6, 6, 6 -bits input).

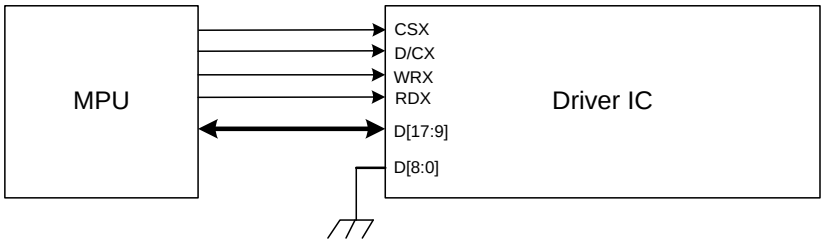
There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

Table15.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D8		0R5	0G2	1R5	1G2	…	238R5	238G2	239R5	239G2
D7	C7	0R4	0G1	1R4	1G1	…	238R4	238G1	239R4	239G1
D6	C6	0R3	0G0	1R3	1G0	…	238R3	238G0	239R3	239G0
D5	C5	0R2	0B5	1R2	1B5	…	238R2	238B5	239R2	239B5
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

The 8080- Ⅱ system 9-bit parallel bus interface of GC9308 can be selected by setting hardware pin IM [3:0] to "1011". The following shown figure is the example of interface with 8080- MCU system interface.

Figure56.



1)262K-Colors,:18-bit/pixel(RGB 6, 6, 6 -bits input).

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

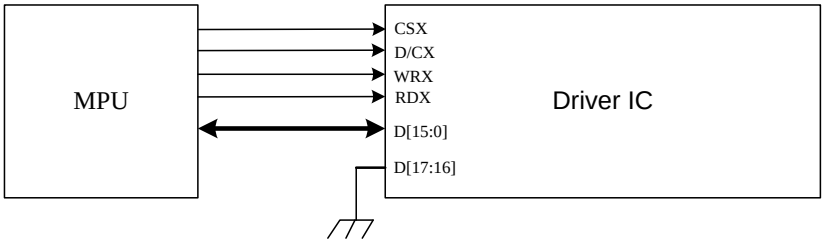
Table16.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R5	0G2	1R5	1G2	…	238R5	238G2	239R5	239G2
D16	C6	0R4	0G1	1R4	1G1	…	238R4	238G1	239R4	239G1
D15	C5	0R3	0G0	1R3	1G0	…	238R3	238G0	239R3	239G0
D14	C4	0R2	0B5	1R2	1B5	…	238R2	238B5	239R2	239B5
D13	C3	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D12	C2	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D11	C1	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D10	C0	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

4.5.6. 16-bit Parallel MCU Interface

The 8080-Ⅰsystem 16-bit parallel bus interface of GC9308 can be selected by setting hardware pin IM[3:0] to "0001".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.

Figure57.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1)65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Table17.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8		0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "110".

1)MDT[1:0]="00"

Table18.

Count	0	1	2	3	…	358	359	360
D/CX	0	1	1	1	…	1	1	1
D15		0R5	0B5	1G5	…	238R5	238B5	239G5
D14		0R4	0B4	1G4	…	238R4	238B4	239G4
D13		0R3	0B3	1G3	…	238R3	238B3	239G3
D12		0R2	0B2	1G2	…	238R2	238B2	239G2
D11		0R1	0B1	1G1	…	238R1	238B1	239G1
D10		0R0	0B0	1G0	…	238R0	238B0	239G0
D9								
D8								
D7	C7	0G5	1R5	1B5	…	238G5	239R5	239B5
D6	C6	0G4	1R4	1B4	…	238G4	239R4	239B4
D5	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
D4	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
D3	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
D2	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
D1	C1							
D0	C0							

2)MDT[1:0]=“01”

Table19.

Count	0	1	2	3		…	477	478	479	480
D/CX	0	1	1	1		…	1	1	1	1
D15		0R5	0B5	1R5	1B5	…	238R5	238B5	239R5	239B5
D14		0R4	0B4	1R4	1B4	…	238R4	238B4	239R4	239B4
D13		0R3	0B3	1R3	1B3	…	238R3	238B3	239R3	239B3
D12		0R2	0B2	1R2	1B2	…	238R2	238B2	239R2	239B2
D11		0R1	0B1	1R1	1B1	…	238R1	238B1	239R1	239B1
D10		0R0	0B0	1R0	1B0	…	238R0	238B0	239R0	239B0
D9						…				
D8						…				
D7	C7	0G5		1G5		…	238G5		239G5	
D6	C6	0G4		1G4		…	238G4		239G4	
D5	C5	0G3		1G3		…	238G3		239G3	
D4	C4	0G2		1G2		…	238G2		239G2	
D3	C3	0G1		1G1		…	238G1		239G1	
D2	C2	0G0		1G0		…	238G0		239G0	
D1	C1					…				
D0	C0					…				

3)MDT[1:0]=“10”

Table20.

Count	0	1	2	3		…	477	478	479	480
D/CX	0	1	1	1		…	1	1	1	1
D15		0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D14		0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0
D13		0R3		1R3		…	238R3		239R3	
D12		0R2		1R2		…	238R2		239R2	
D11		0R1		1R1		…	238R1		239R1	
D10		0R0		1R0		…	238R0		239R0	
D9		0G5		1G5		…	238G5		239G5	
D8		0G4		1G4		…	238G4		239G4	
D7	C7	0G3		1G3		…	238G3		239G3	
D6	C6	0G2		1G2		…	238G2		239G2	
D5	C5	0G1		1G1		…	238G1		239G1	
D4	C4	0G0		1G0		…	238G0		239G0	
D3	C3	0B5		1B5		…	238B5		239B5	
D2	C2	0B4		1B4		…	238B4		239B4	
D1	C1	0B3		1B3		…	238B3		239B3	
D0	C0	0B2		1B2		…	238B2		239B2	

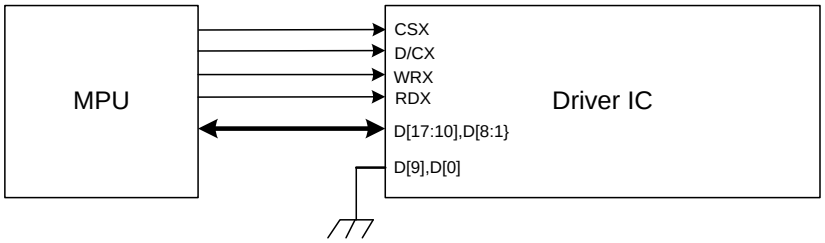
4)MDT[1:0]=“11”

Table21.

Count	0	1	2	3		…	477	478	479	480
D/CX	0	1	1	1		…	1	1	1	1
D15			0R3		1R3	…		238R3		239R3
D14			0R2		1R2	…		238R2		239R2
D13			0R1		1R1	…		238R1		239R1
D12			0R0		1R0	…		238R0		239R0
D11			0G5		1G5	…		238G5		239G5
D10			0G4		1G4	…		238G4		239G4
D9			0G3		1G3	…		238G3		239G3
D8			0G2		1G2	…		238G2		239G2
D7	C7		0G1		1G1	…		238G1		239G1
D6	C6		0G0		1G0	…		238G0		239G0
D5	C5		0B5		1B5	…		238B5		239B5
D4	C4		0B4		1B4	…		238B4		239B4
D3	C3		0B3		1B3	…		238B3		239B3
D2	C2		0B2		1B2	…		238B2		239B2
D1	C1	0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D0	C0	0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0

The 8080-II system 16-bit parallel bus interface of GC9308 can be selected by settings IM [3:0] =”1000”. The following shown figure is the example of interface with 8080- MCU system interface.

Figure58.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Table22.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R4	1R4	2R4	…	237R4	238R4	239R4
D16		0R3	1R3	2R3	…	237R3	238R3	239R3
D15		0R2	1R2	2R2	…	237R2	238R2	239R2
D14		0R1	1R1	2R1	…	237R1	238R1	239R1
D13		0R0	1R0	2R0	…	237R0	238R0	239R0
D12		0G5	1G5	2G5	…	237G5	238G5	239G5
D11		0G4	1G4	2G4	…	237G4	238G4	239G4
D10		0G3	1G3	2G3	…	237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D4	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D3	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D2	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D1	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "110".

1)MDT[1:0]=00

Table23.

Count	0	1	2	3	…	358	359	360
D/CX	0	1	1	1	…	1	1	1
D17		0R5	0B5	1G5	…	238R5	238B5	239G5
D16		0R4	0B4	1G4	…	238R4	238B4	239G4
D15		0R3	0B3	1G3	…	238R3	238B3	239G3
D14		0R2	0B2	1G2	…	238R2	238B2	239G2

D13		0R1	0B1	1G1	…	238R1	238B1	239G1
D12		0R0	0B0	1G0	…	238R0	238B0	239G0
D11								
D10								
D8	C7	0G5	1R5	1B5	…	238G5	239R5	239B5
D7	C6	0G4	1R4	1B4	…	238G4	239R4	239B4
D6	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
D5	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
D4	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
D3	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
D2	C1							
D1	C0							

2)MDT[1:0]=01

Table24.

Count	0	1	2	3		…	477	478	479	480
D/CX	0	1	1	1		…	1	1	1	1
D17		0R5	0B5	1R5	1B5	…	238R5	238B5	239R5	239B5
D16		0R4	0B4	1R4	1B4	…	238R4	238B4	239R4	239B4
D15		0R3	0B3	1R3	1B3	…	238R3	238B3	239R3	239B3
D14		0R2	0B2	1R2	1B2	…	238R2	238B2	239R2	239B2
D13		0R1	0B1	1R1	1B1	…	238R1	238B1	239R1	239B1
D12		0R0	0B0	1R0	1B0	…	238R0	238B0	239R0	239B0
D11						…				
D10						…				
D8	C7	0G5		1G5		…	238G5		239G5	
D7	C6	0G4		1G4		…	238G4		239G4	
D6	C5	0G3		1G3		…	238G3		239G3	
D5	C4	0G2		1G2		…	238G2		239G2	
D4	C3	0G1		1G1		…	238G1		239G1	
D3	C2	0G0		1G0		…	238G0		239G0	
D2	C1					…				
D1	C0					…				

3)MDT[1:0]=10

Table25.

Count	0	1	2	3		…	477	478	479	480
D/CX	0	1	1	1		…	1	1	1	1
D17		0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D16		0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0
D15		0R3		1R3		…	238R3		239R3	
D14		0R2		1R2		…	238R2		239R2	
D13		0R1		1R1		…	238R1		239R1	
D12		0R0		1R0		…	238R0		239R0	
D11		0G5		1G5		…	238G5		239G5	
D10		0G4		1G4		…	238G4		239G4	
D8	C7	0G3		1G3		…	238G3		239G3	
D7	C6	0G2		1G2		…	238G2		239G2	
D6	C5	0G1		1G1		…	238G1		239G1	
D5	C4	0G0		1G0		…	238G0		239G0	
D4	C3	0B5		1B5		…	238B5		239B5	
D3	C2	0B4		1B4		…	238B4		239B4	
D2	C1	0B3		1B3		…	238B3		239B3	
D1	C0	0B2		1B2		…	238B2		239B2	

4)MDT[1:0]=11

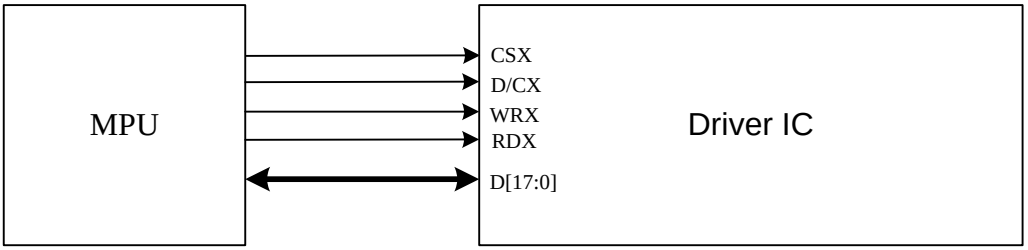
Table26.

Count	0	1	2	3		…	477	478	479	480
D/CX	0	1	1	1		…	1	1	1	1
D17			0R3		1R3	…		238R3		239R3
D16			0R2		1R2	…		238R2		239R2
D15			0R1		1R1	…		238R1		239R1
D14			0R0		1R0	…		238R0		239R0
D13			0G5		1G5	…		238G5		239G5
D12			0G4		1G4	…		238G4		239G4
D11			0G3		1G3	…		238G3		239G3
D10			0G2		1G2	…		238G2		239G2
D8	C7		0G1		1G1	…		238G1		239G1
D7	C6		0G0		1G0	…		238G0		239G0
D6	C5		0B5		1B5	…		238B5		239B5
D5	C4		0B4		1B4	…		238B4		239B4
D4	C3		0B3		1B3	…		238B3		239B3
D3	C2		0B2		1B2	…		238B2		239B2
D2	C1	0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D1	C0	0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0

4.5.7. 18-bit Parallel MCU Interface

The 8080-I system 18-bit parallel bus interface of GC9308 can be selected by setting hardware pin IM[3:0] to "0011".The following shown figure is the example of interface with 8080-I MCU system interface.

Figure58.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Table27.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8		0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

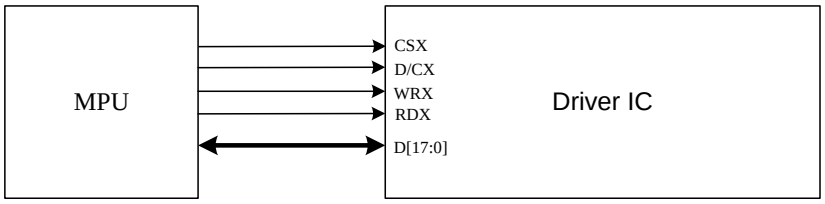
One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "110".

Table28.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	237R5	238R5	239R5
D16		0R4	1R4	2R4	…	237R4	238R4	239R4
D15		0R3	1R3	2R3	…	237R3	238R3	239R3
D14		0R2	1R2	2R2	…	237R2	238R2	239R2
D13		0R1	1R1	2R1	…	237R1	238R1	239R1
D12		0R0	1R0	2R0	…	237R0	238R0	239R0
D11		0G5	1G5	2G5	…	237G5	238G5	239G5
D10		0G4	1G4	2G4	…	237G4	238G4	239G4
D9		0G3	1G3	2G3	…	237G3	238G3	239G3
D8		0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C7	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C6	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C5	0B5	1B5	2B5	…	237B5	238B5	239B5
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

The 8080-II system 18-bit parallel bus interface mode can be selected by settings IM [3:0] =”1010”. The following shown figure is the example of interface with 8080- MCU system interface.

Figure59.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1)65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “101”.

Table29.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8	C7	0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C6	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C5	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C4	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C3	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C2	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C1	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C0	0B1	1B1	2B1	…	237B1	238B1	239B1
D0		0B0	1B0	2B0	…	237B0	238B0	239B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Table30.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	237R5	238R5	239R5
D16		0R4	1R4	2R4	…	237R4	238R4	239R4
D15		0R3	1R3	2R3	…	237R3	238R3	239R3
D14		0R2	1R2	2R2	…	237R2	238R2	239R2
D13		0R1	1R1	2R1	…	237R1	238R1	239R1
D12		0R0	1R0	2R0	…	237R0	238R0	239R0
D11		0G5	1G5	2G5	…	237G5	238G5	239G5
D10		0G4	1G4	2G4	…	237G4	238G4	239G4
D9		0G3	1G3	2G3	…	237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C4	0B5	1B5	2B5	…	237B5	238B5	239B5

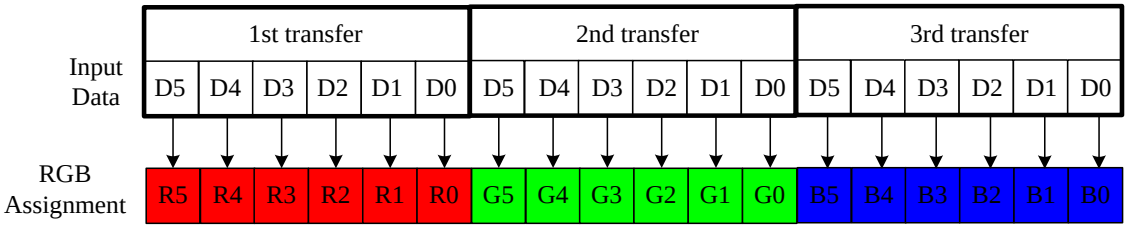
D4	**C3**	**0B4**	**1B4**	**2B4**	**…**	**237B4**	**238B4**	**239B4**
D3	**C2**	**0B3**	**1B3**	**2B3**	**…**	**237B3**	**238B3**	**239B3**
D2	**C1**	**0B2**	**1B2**	**2B2**	**…**	**237B2**	**238B2**	**239B2**
D1	**C0**	**0B1**	**1B1**	**2B1**	**…**	**237B1**	**238B1**	**239B1**
D0		**0B0**	**1B0**	**2B0**	**…**	**237B0**	**238B0**	**239B0**

4.5.8. 6-bit Parallel RGB Interface

The 6-bit RGB interface is selected by setting the RIM bit to “1”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (D [5:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. the valid display data is inputted in pixel unit via D [5:0] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.

1)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

Figure60.



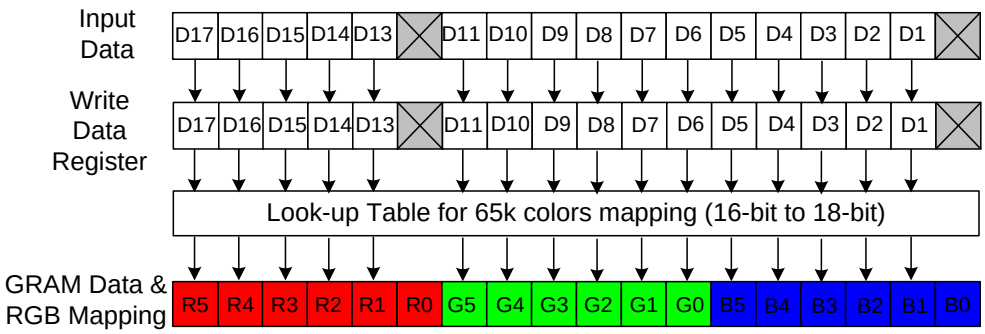
GC9308 has data transfer counters to count the first, second, third data transfer in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK).Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

4.5.9. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to “101”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D[17:13] & D[11:0]) according to the data enable signal (DE). The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D[17:13] & D[11:0] according to the VFP/VBP and HFP/HBP settings. The unused D12 and D0 pins must be connected to GND for ensure normally operation. Registers can be set by the SPI system interface.

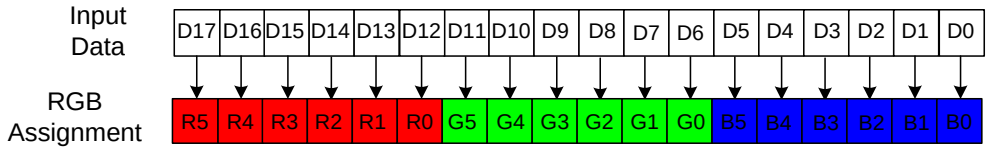
Figure62.



4.5.10. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D[17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the SPI system interface.

Figure63.



5. Function Description

5.1. Display data GRAM mapping

The display data RAM stores display dots and consists of 1,382,400 bits (320x18x240 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **SC, EC** bits and **SP, EP** bits, it is possible to access the GRAM by setting RAMWR or RAMRD commands from start positions of the window address.

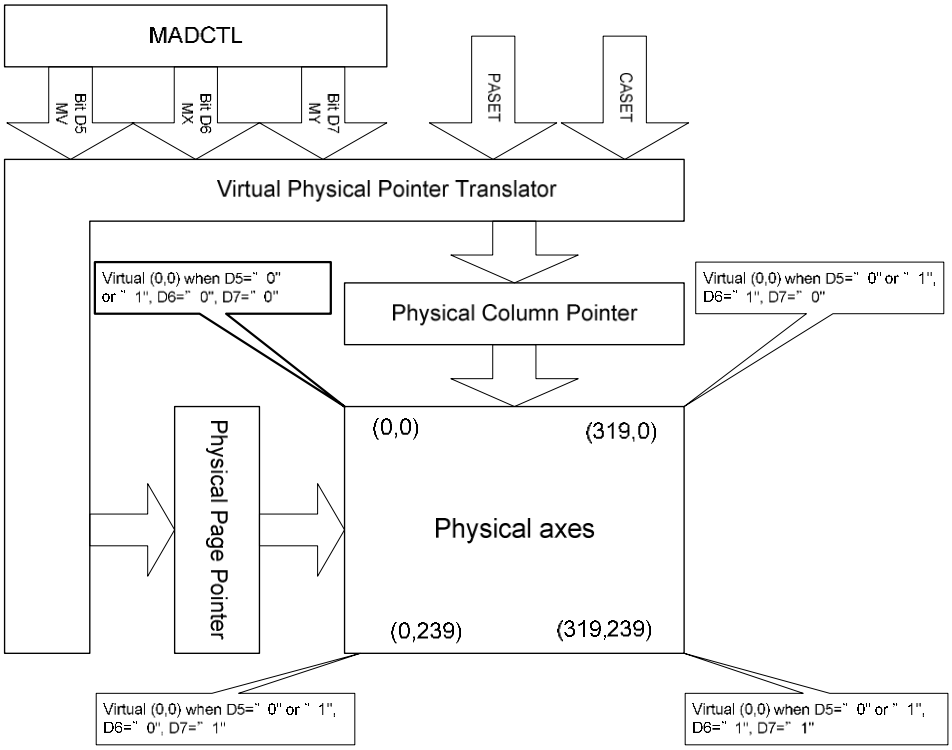
GRAM address for display panel position as shown in the following table

Table31.

(00,00)h	(00,01)h	…… …	(00, 13D)h	(00, 13E)h	(00,13F)h
(01,00)h	(01,01)h	…… …	(01, 13D)h	(01, 13E)h	(01, 13F)h
(02,00)h	(02,01)h	…… …	(02, 13D)h	(02, 13E)h	(02, 13F)h
(03,00)h	(03,01)h	…… …	(03, 13D)h	(03, 13E)h	(03, 13F)h
. . .	. . .	. . .	. . .	. . .	. . .
(ED,00)h	(ED,01)h	…… …	(ED, 13D)h	(ED, 13E)h	(ED, 13F)h
(EE,00)h	(EE,01)h	…… …	(EE, 13D)h	(EE, 13E)h	(EE, 13F)h
(EF,00)h	(EF,01)h	…… …	(EF, 13D)h	(EF, 13E)h	(EF, 13F)h

5.2. MCU to memory write/read direction

The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, Bits D5, D6, and D7 as described below.

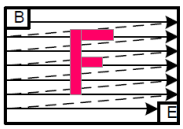
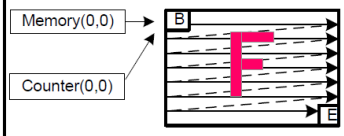
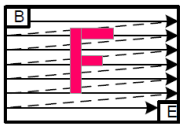
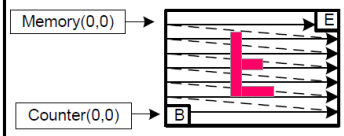
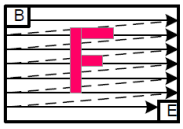
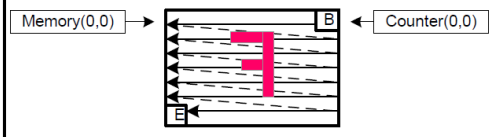
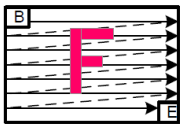
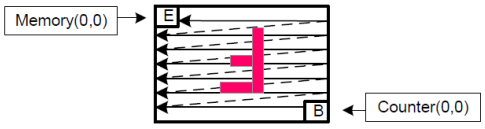
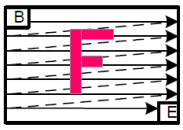
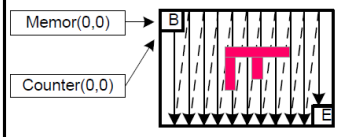
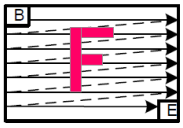
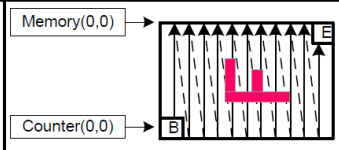
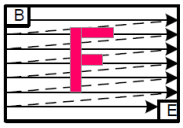
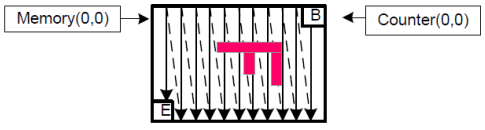
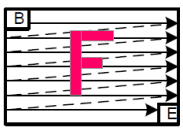
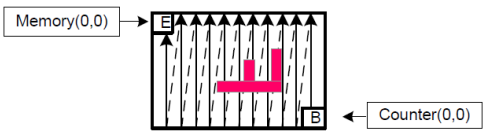


D5	D6	D7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (239-Physical Page Pointer)
0	1	0	Direct to (319-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (319-Physical Column Pointer)	Direct to (239-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (239-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (319-Physical Column Pointer)
1	1	1	Direct to (239-Physical Page Pointer)	Direct to (319-Physical Column Pointer)

Condition	Column Counter	Page counter
When RAMWR/RAMRD command is accepted	Return to “Start column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column values is large than “End Column”	Return to “Start column”	Increment by 1
The Page counter is large than “End Page”	Return to “Start column”	Return to “Start Page”

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data Direction	MADCTR Parameter			Image in the Memory (MCU)	Image in the Driver (Frame Memory)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

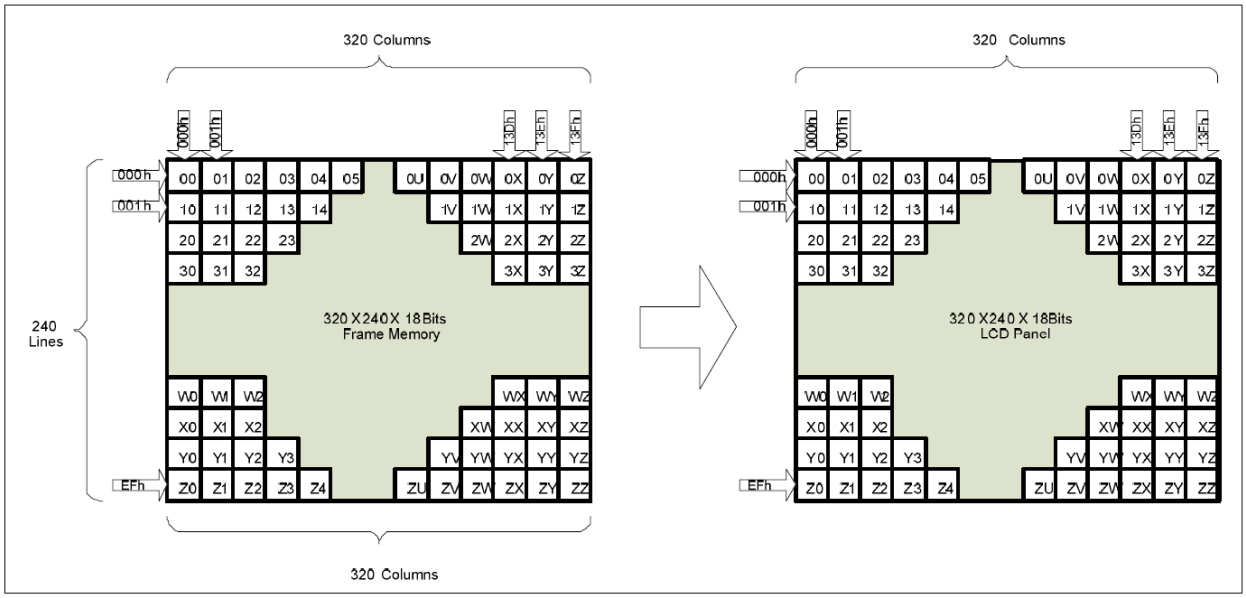
5.3. GRAM to display address mapping

By setting the **SS**, the relation between the source output channel and the GRAM address can be changed as reverse display. By setting the **GS** , the relation between the gate output channel and the GRAM address can be changed as reverse display. By setting the **BGR**, the relation between the source output channel and the <R>, <G>, <B> dot allocation can be reversed for different LCD color filter arrangement.

The following Tables show relations among the GRAM data allocation, the source output channel, and the R, G, B dot allocation.

GRAM X address and display panel position:

GC9308 supports three kinds of display mode: one is Normal Display Mode, the other is Partial Display Mode, and Scrolling Display Mode.

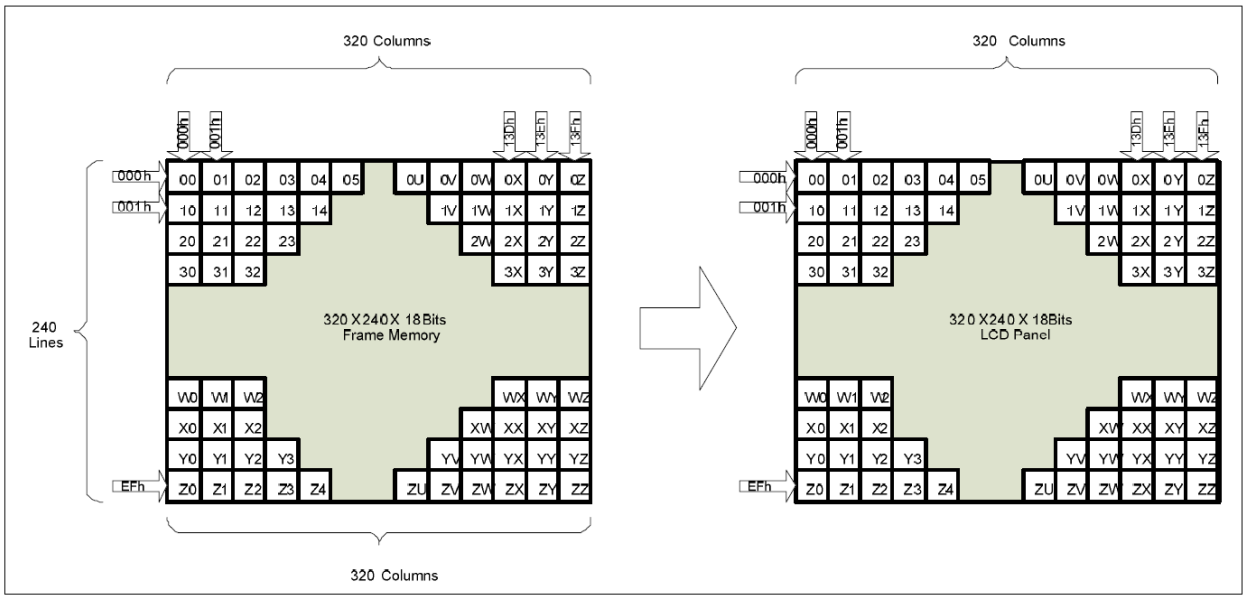


5.3.1. Normal display on or partial mode on, vertical scroll off

In this mode, content of the frame memory within an area where column pointer is 0000h to 013Fh and page pointer is 0000h to 00EFh is displayed.

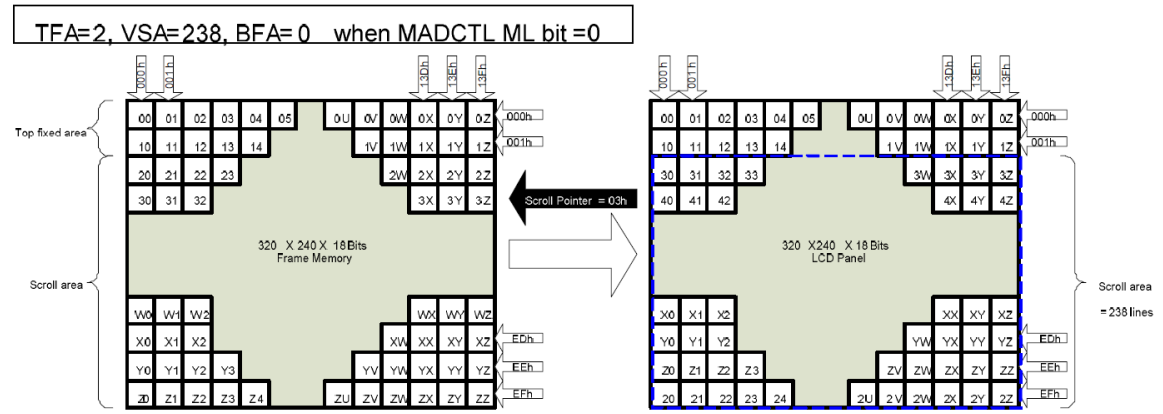
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0)

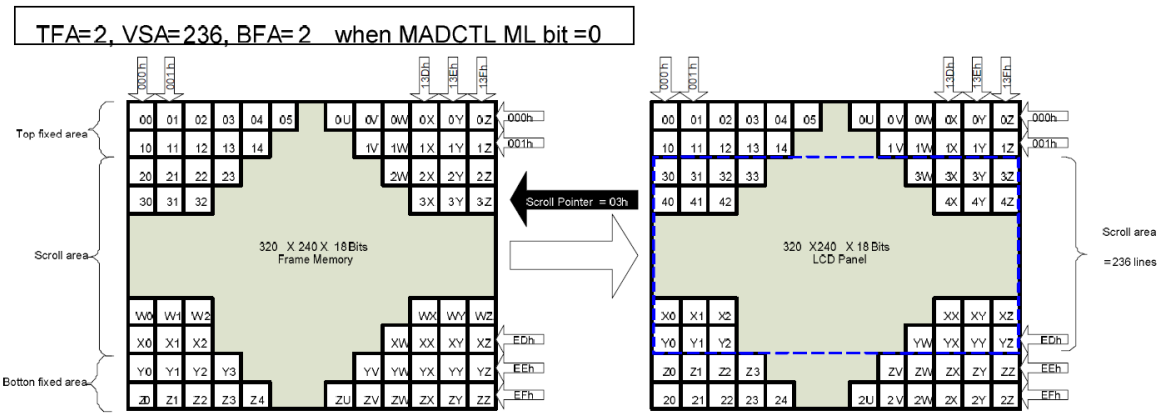
Figure66.

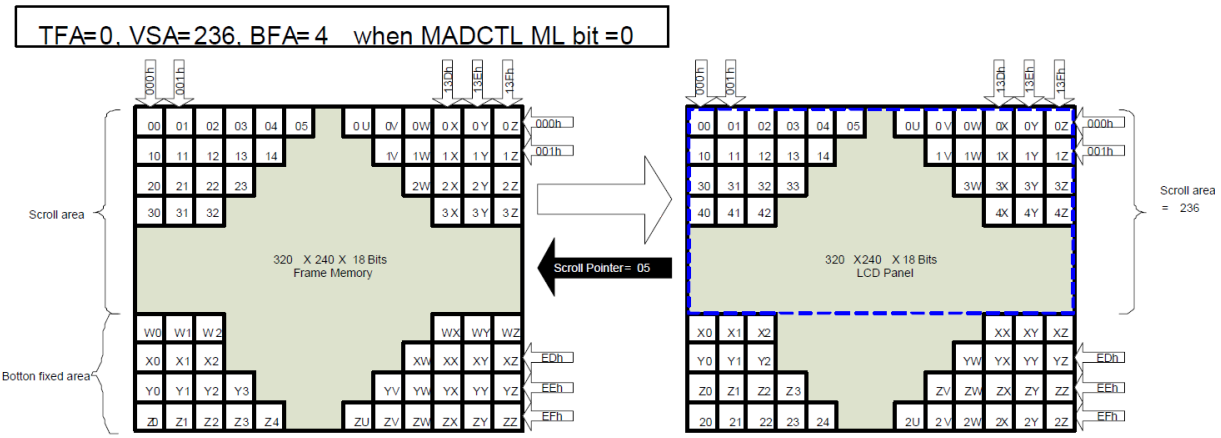


5.3.2. Vertical scroll display mode

When setting R37h, the scrolling display mode is active, and the vertical scrolling display is specified by **TFA, VSA ,BFA** bits (R33h) and **VSP** bits (R37h).







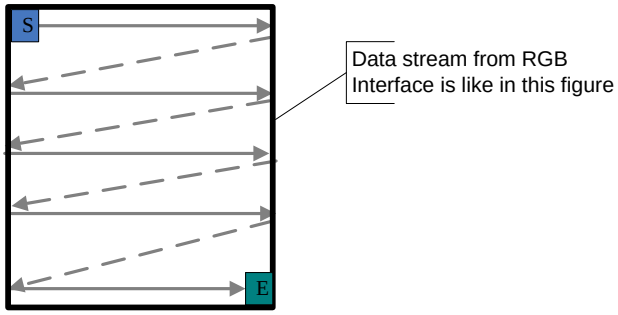
Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) ≠ 240, Scrolling Mode is undefined.

5.3.3. Updating order on display active area in RGB interface mode

There is defined different kind of updating orders for display in RGB interface mode (**RCM [1:0]** =’1x’).

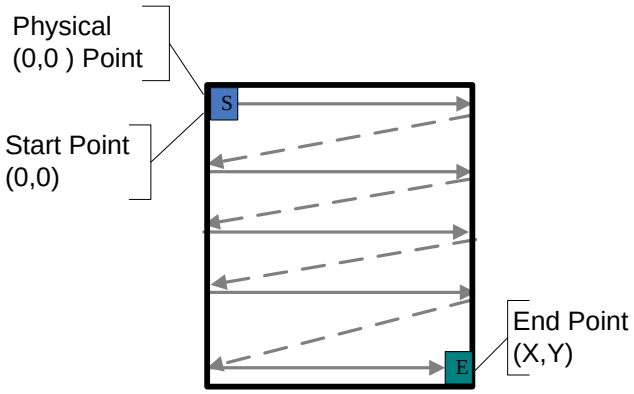
These updating are controlled by **MY** and **MX** bits. Data streaming direction from the host to the display is described in the following figure.

Figure74.



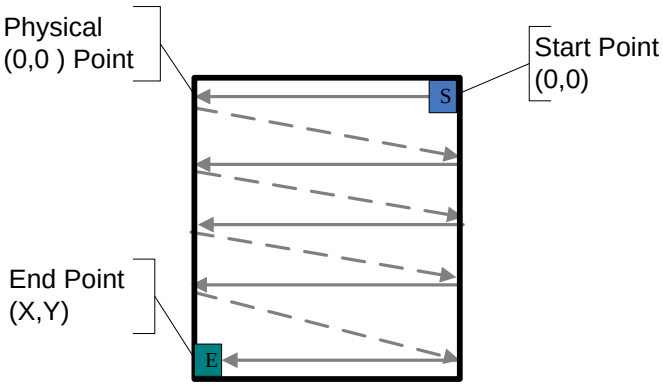
Updating order when MY = ‘0’ and MX = ‘0’

Figure75.



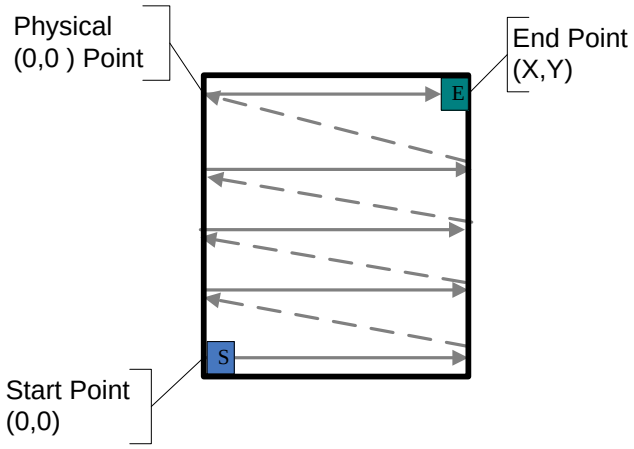
Updating order when MY = ‘0’ and MX = ‘1’

Figure76.



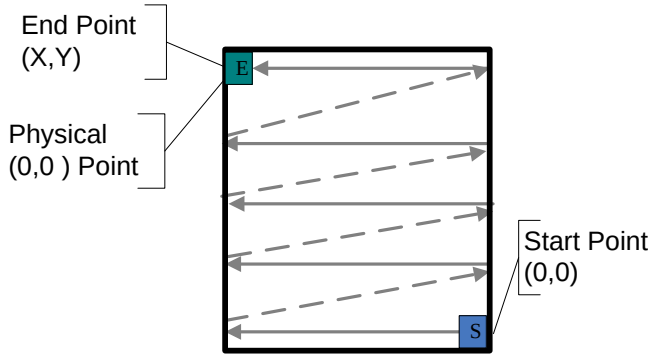
Updating order when MY = ‘1’ and MX = ‘0’

Figure77.



Updating order when MY = '1' and MX = '1'

Figure78.



Rules for updating order on display active area in RGB interface display mode:

Table37.

Condition	Horizontal Counter	Vertical Counter
An active VS signal is received	Return to 0	Return to 0
Single Pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The Horizontal counter value is larger than X and the Vertical counter value is larger than Y	Return to 0 "Start Column"	Return to "Start Page"

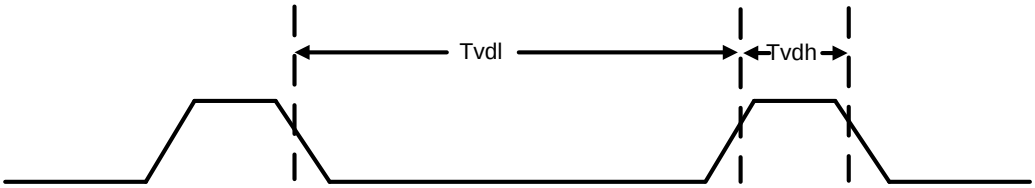
Note: Pixel order is RGB on the display.

5.4. Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

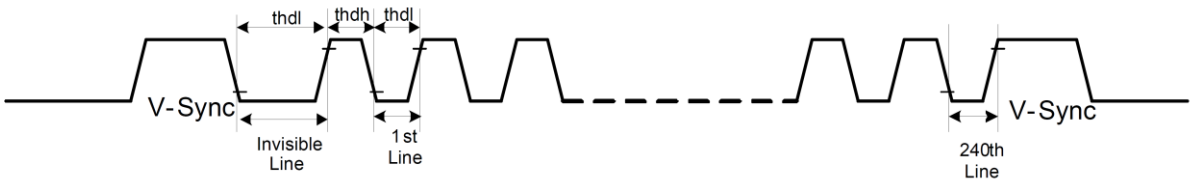
5.4.1. Tearing effect line modes

Mode 1, The Tearing Effect Output signal consists of V-Blanking Information only:
Figure79.



tVdh= The LCD display is not updated from the Frame Memory
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 240 H-sync pulses per field.
Figure80.

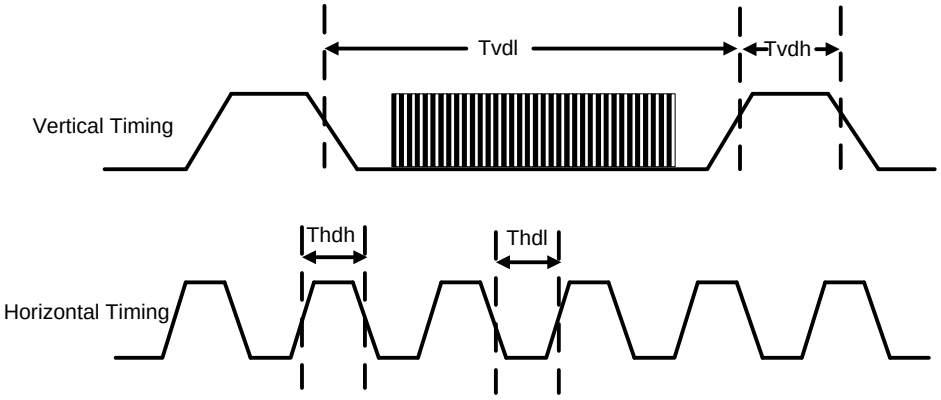


thdh= The LCD display is not updated from the Frame Memory
thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

5.4.2. Tearing effect line timing

The Tearing Effect signal is described below.

Figure81.



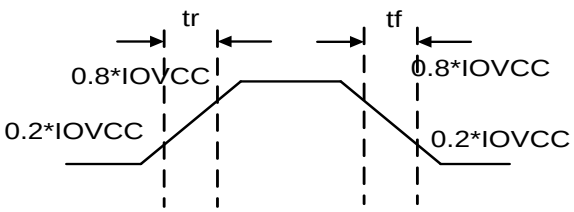
Idle Mode Off (Frame Rate = 60 Hz)

Table38.

Symbol	Parameter	Spec.			Description
		Min.	Max.	Unit	
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

Note: Idle Mode Off (Frame Rate = 60 Hz) ,The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

Figure82.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

5.5. Source driver

The GC9308 contains a 960 channels of source driver (S1~S960) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 960 channels and generates corresponding
gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

5.6. Gate driver

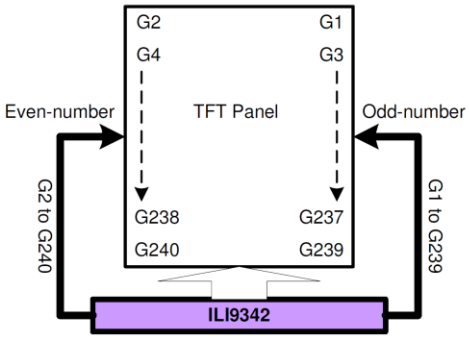
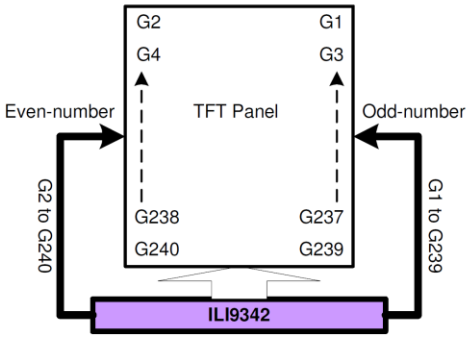
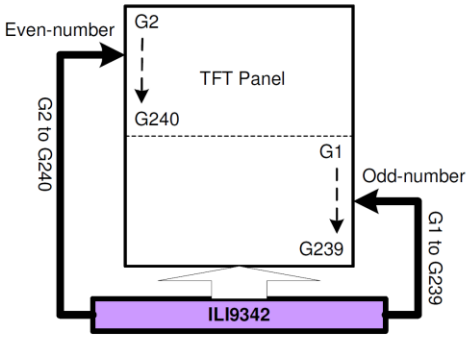
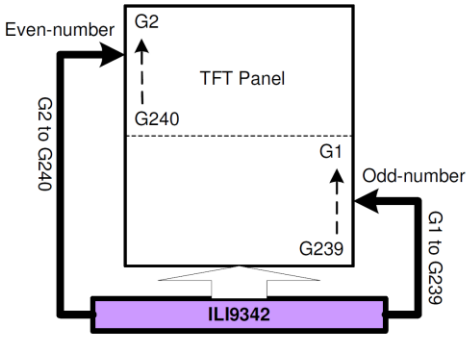
The GC9308 contains a 240 gate channels of gate driver (G1~G240) which is usedfor driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

5.7. Scan mode setting

GS: Sets the direction of scan by the gate driver, The scan direction determined by GS = 0 can be reversed by setting GS = 1.

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

Table39.

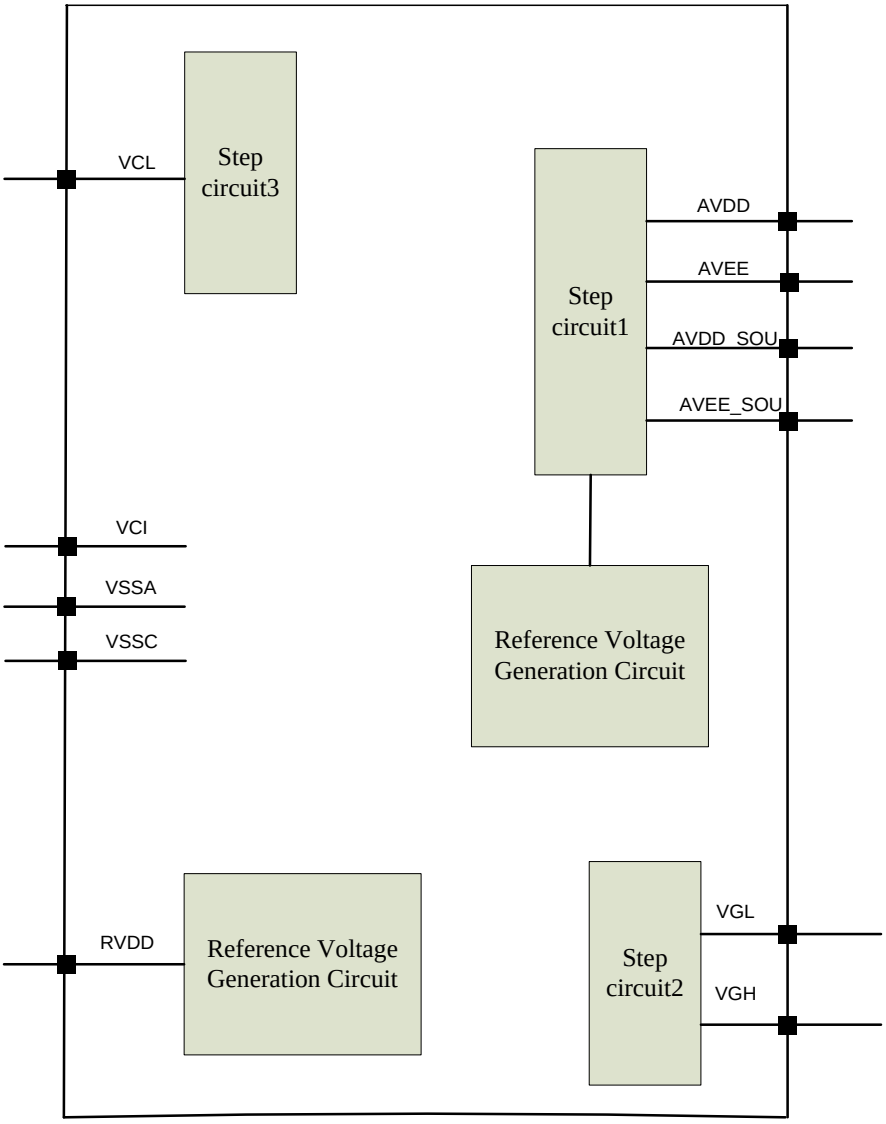
SM	GS	Scan Direction	Gate Output Sequence
0	0		G1→G2→G3→G4→ …… ….→G237→G238→G239→G240
0	1		G240→G239->G238→G237→…… …. →G4→G3→G2→G1
1	0		G1→G3→……..→G237→G239→ G2→G4→……→G238→G240
1	1		G240→G238→……..→G4→G2→ G239→G237→……→G3→G1

5.8. LCD power generation circuit

5.8.1. Power supply circuit

The power circuit of GC9308 is used to generate supply voltages for LCD panel driving.

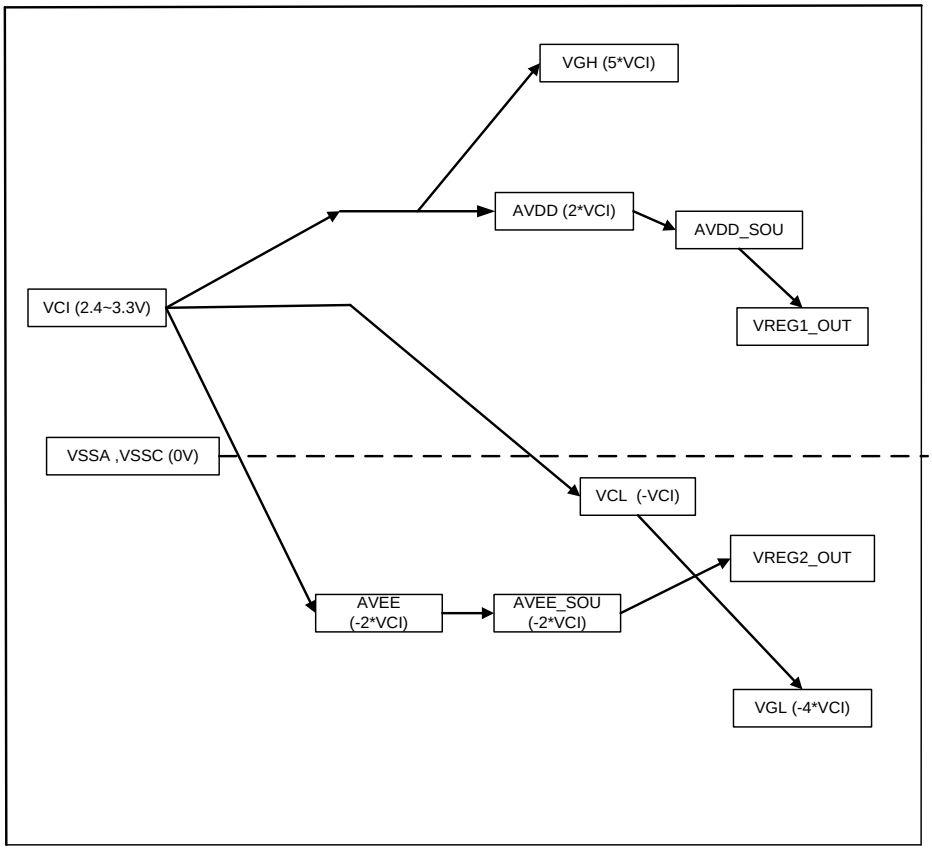
Figure83.



5.8.2. LCD power generation scheme

The boost voltage generated is shown as below.

Figure84.



LCD power generation scheme

5.9. Gamma Correction

GC9308 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make GC9308 available with liquid crystal panels of various characteristics.

Figure85.

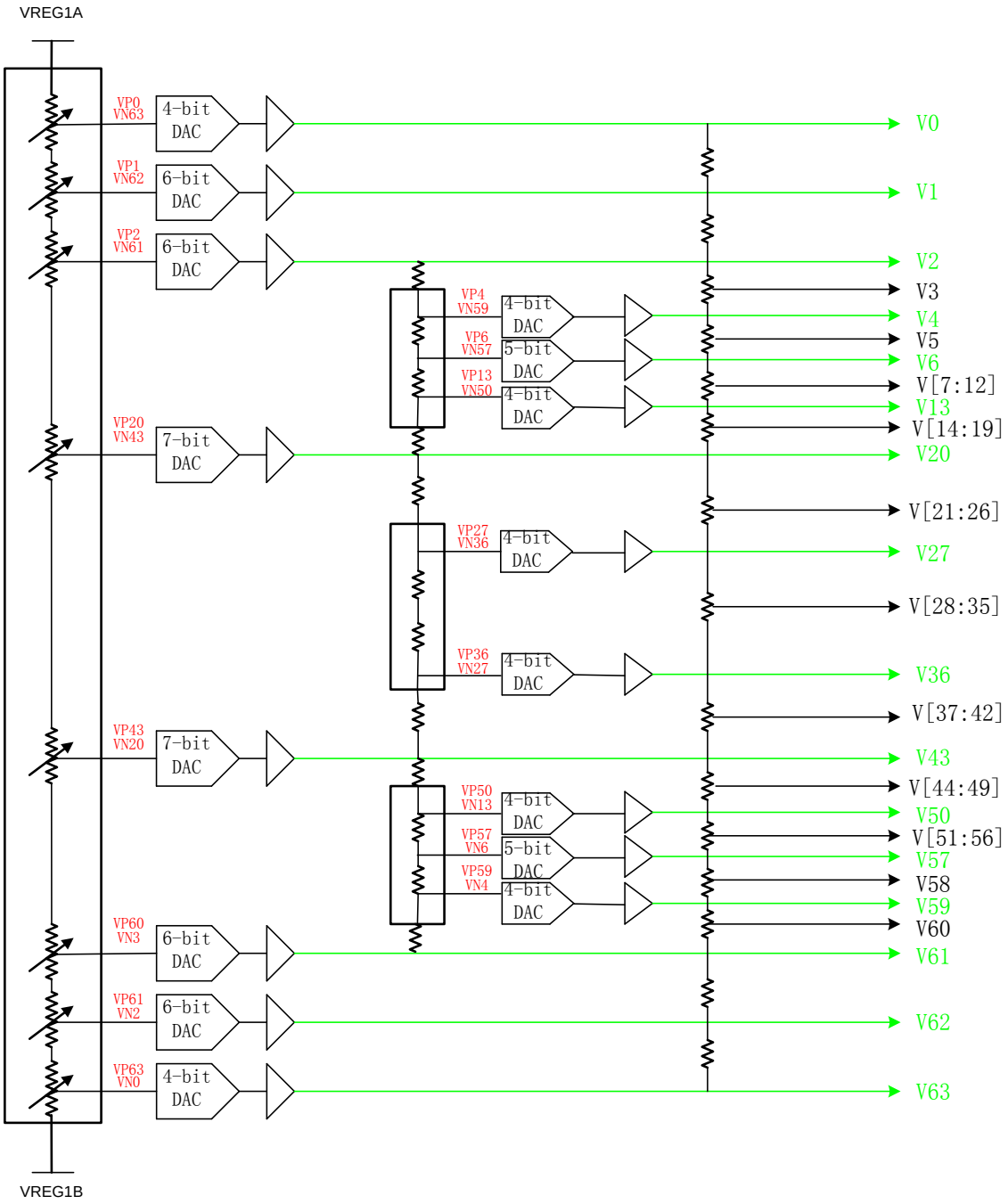
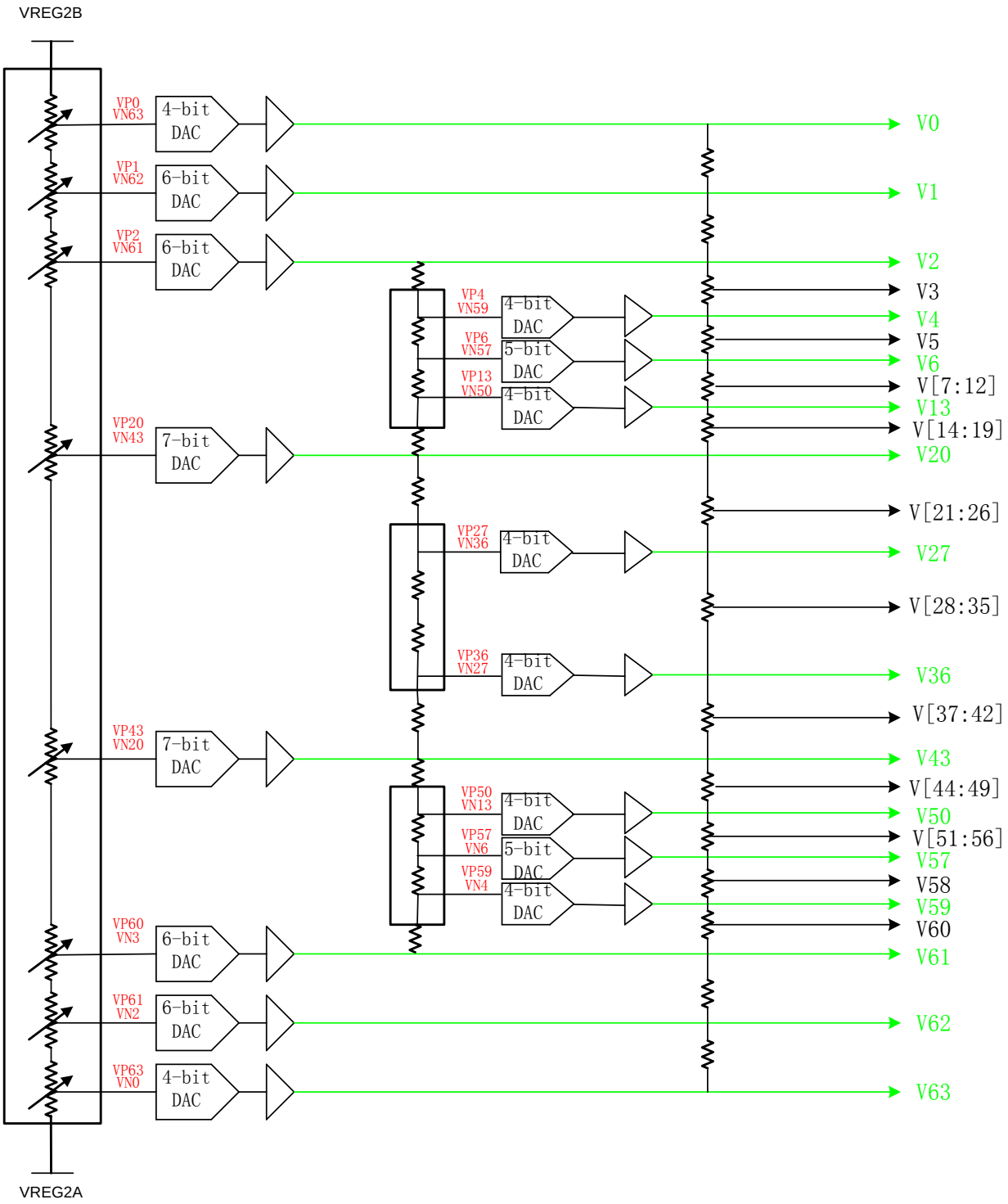
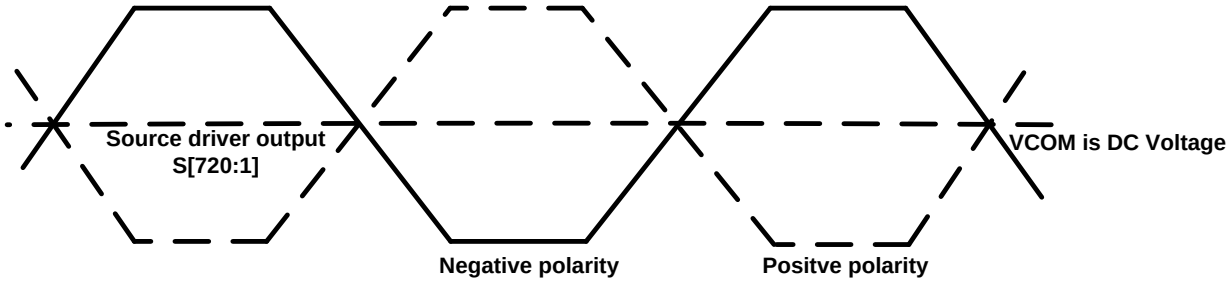


Figure86.



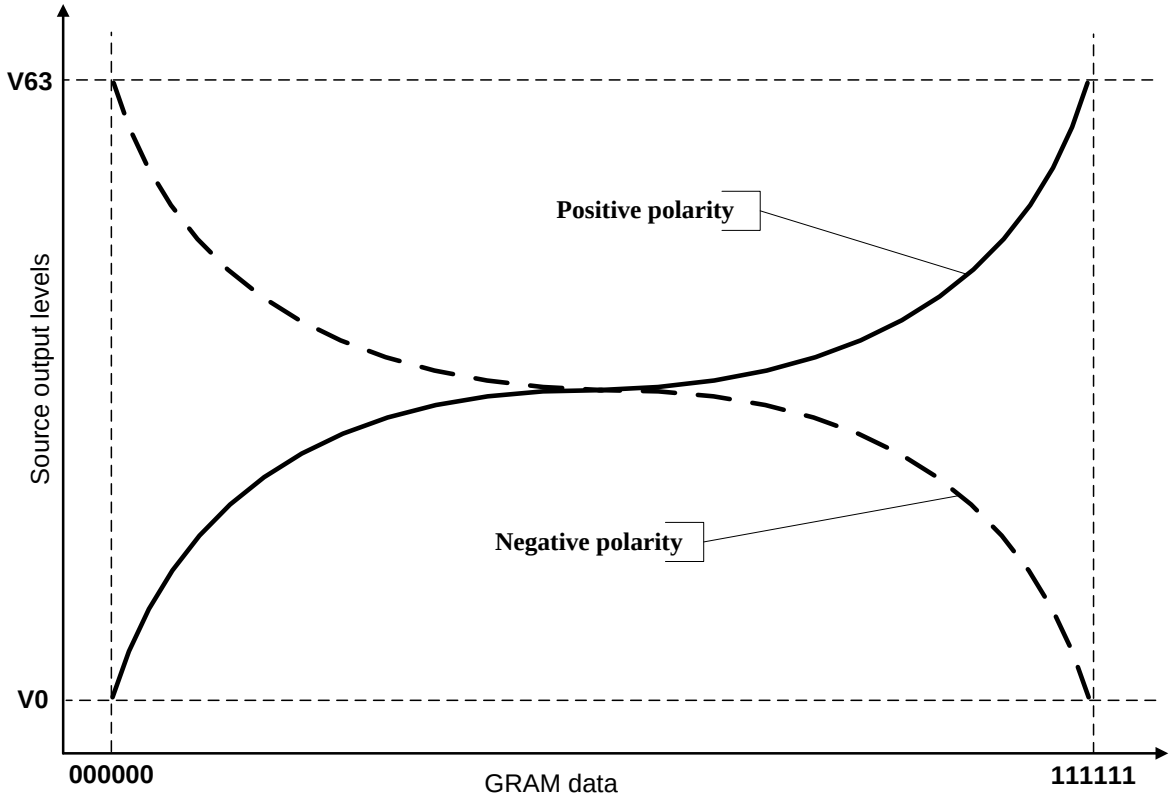
Grayscale Voltage Generation

Figure87.Dot inversion



Relationship between Source Output and VCOM

Figure88.



5.10. Power Level Definition

5.10.1. Power Levels

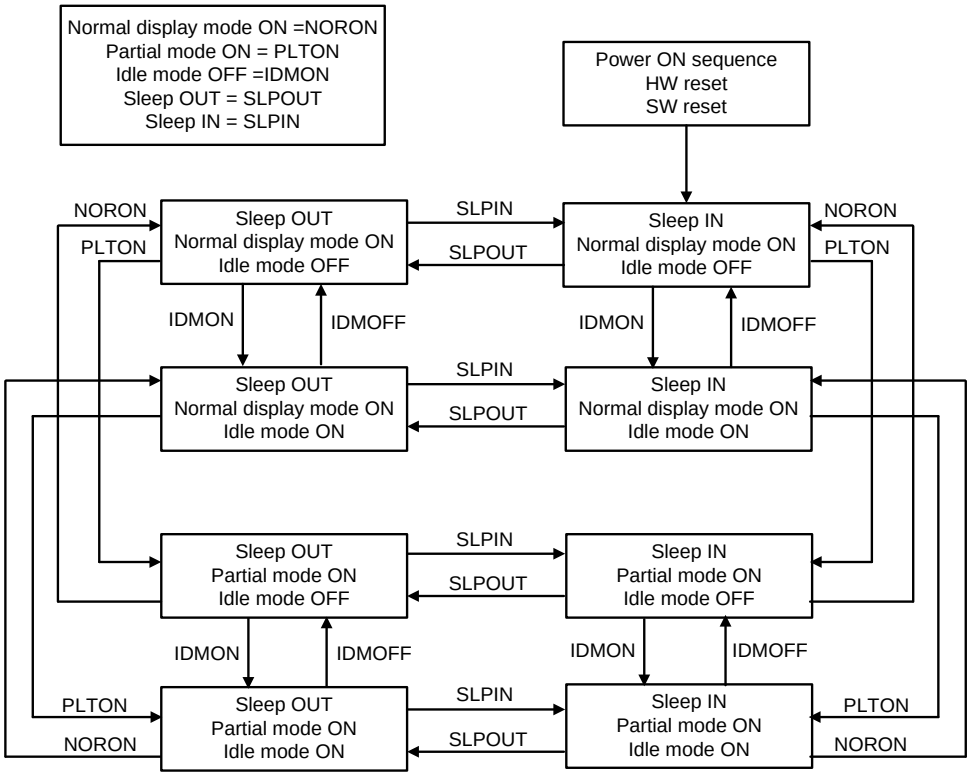
6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with IOVCC power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VCI and IOVCC are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

5.10.2. Power Flow Chart

Figure89.



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

5.10.3.Brightness control block

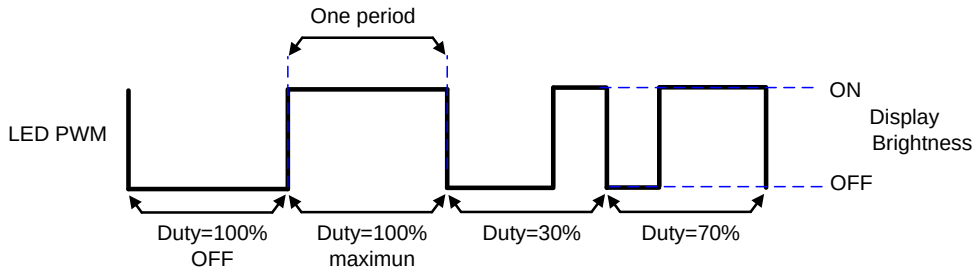
There is an external output signal from brightness block, LEDPWM to control the LED driver IC in order to control display brightness.

There are resister bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The LEDPWM duty is calculated as DBV[7:0]/255 x period (affected by OSC frequency).

For example: LEDPWM period = 3ms, and DBV[7:0] = '200DEC'. Then LEDPWM duty = 200 / 255=78.1%.

Correspond to the LEDPWM period = 3 ms, the high-level of LEDPWM (high effective) = 2.344ms, and the low-level of LEDPWM = 0.656ms.

Figure90.



LEDPWM output duty

5.11. Input/output pin state

5.11.1. Output pins

Table40.

Output or Bi-directional pins	After Power On	After Hardware Reset
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)
SDA	High-Z (Inactive)	High-Z (Inactive)
SDO	High-Z (Inactive)	High-Z (Inactive)
TE	Low	Low
LEDPWM	Low	Low

Characteristics of output pins

5.11.2. Input pins

Table41.

Input pins	During Power On Process	After Power On	After Hardware Reset	During Power Off Process
RESX	Input valid	Input valid	Input valid	Input valid
CSX	Input invalid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input invalid
SDA	Input invalid	Input valid	Input valid	Input invalid
VSYNC	Input invalid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input valid	Input valid	Input invalid
DE	Input invalid	Input valid	Input valid	Input invalid
DOTCLK	Input invalid	Input valid	Input valid	Input invalid
D[17:0]	Input invalid	Input valid	Input valid	Input invalid
IM[3:0]	Input invalid	Input valid	Input valid	Input invalid

Characteristics of input pins

6. Command

6.1. Command List

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Read Display Identification Information 2	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID_1[7:0]								00
	1	↑	1	XX	ID_2[7:0]								93
	1	↑	1	XX	ID_3[7:0]								08
Read Display Status	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[31:25]							X	00
	1	↑	1	XX	X	D[22:20]			D[19:16]				61
	1	↑	1	XX	X	X	X	X	X	D[10:8]			00
	1	↑	1	XX	D[7:5]			X	X	X	X	X	00
Enter Sleep Mode	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Display OFF	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	XX	SC[15:8]								00
	1	1	↑	XX	SC[7:0]								00
	1	1	↑	XX	EC[15:8]								01
	1	1	↑	XX	EC[7:0]								3Fh
Page Address Set	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	XX	SP[15:8]								00
	1	1	↑	XX	SP[7:0]								00
	1	1	↑	XX	EP[15:8]								00h

	1	1	↑	XX	EP[7:0]								EFh
Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	D[17:0]									XX
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XX	SR[15:8]								00
	1	1	↑	XX	SR[7:0]								00
	1	1	↑	XX	ER[15:8]								00
	1	1	↑	XX	ER[7:0]								EF
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XX	TFA[15:8]								00
	1	1	↑	XX	TFA[7:0]								00
	1	1	↑	XX	VSA[15:8]								00
	1	1	↑	XX	VSA[7:0]								F0
Tearing Effect Line OFF	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
	1	1	↑	XX	X	X	X	X	X	X	X	M	00
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	X	X	00
Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XX	VSP[15:8]								00
	1	1	↑	XX	VSP[7:0]								00
Idle Mode OFF	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Pixel Format Set	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XX	X	DPI[2:0]			X	DBI[2:0]			66
Write Memory Continue	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
	1	1	↑	D[17:0]									XX
Set Tear Scanline	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
	1	1	↑	XX	X	X	X	X	X	X	X	STS[8]	00
	1	1	↑	XX	STS[7:0]								00
Get Scanline	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	X	X	GTS [8]	00
	1	↑	1	XX	GTS[7:0]								00
Write Display Brightness	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
	1	↑	1	XX	DBV[7:0]								00
Write CTRL Display	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
	1	1	↑	XX	X	X	BCTRL	X	DD	BL	X	X	00
Read ID1	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh

	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								00
Read ID2	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								93
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								08

Extended Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RGB Interface Signal Control	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
	1	1	↑	XX	X	RCM[1:0]		X	VSPL	HSPL	DPL	EPL	01
Blanking Porch Control	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
	1	1	↑	XX	0	0	0	0	VFP[3:0]				08
	1	1	↑	XX	0	VBP[6:0]							02
	1	1	↑	XX	0	0	0	HBP[4:0]					14
Display Function Control	0	1	1	XX	1	0	1	1	0	1	1	0	B6
	1	1	1	XX	X	X	X	X	X	X	X	X	00
	1	1	1	XX	X	GS	SS	SM	X	X	X	X	00
	1	1	1	XX	X	X	NL[5:0]						1D
TE Control	0	1	↑	XX	1	0	1	1	1	0	1	0	BAh
	1	1	↑	XX	te_pol	te_width[6:0]							00
Interface Control	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h
	1	1	↑	XX	1	1	0	0	DM[1:0]		RM	RIM	C0

Inter Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Power Criterion Control	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h
	1	1	↑	XX	0	0	0	0	0	0	vcire	0	00
Vcore voltage Control	0	1	↑	XX	1	0	1	0	0	1	1	1	A7h
	1	1	↑	XX	0	1	0	0	vdd_ad[3:0]				48
Vreg1a voltage Control	0	1	↑	XX	1	1	0	0	0	0	1	1	C3h
	1	1	↑	XX	0	vreg1_vbp_d[6:0]							3C
Vreg1b voltage Control	0	1	↑	XX	1	1	0	0	0	1	0	0	C4h
	1	1	↑	XX	0	vreg1_vbn_d[6:0]							3C
Vreg2a voltage Control	0	1	↑	XX	1	1	0	0	1	0	0	1	C9h
	1	1	↑	XX	0	0	vrh[5:0]						28
Frame Rate	0	1	↑	XX	1	0	1	0	1	0	0	0	E8

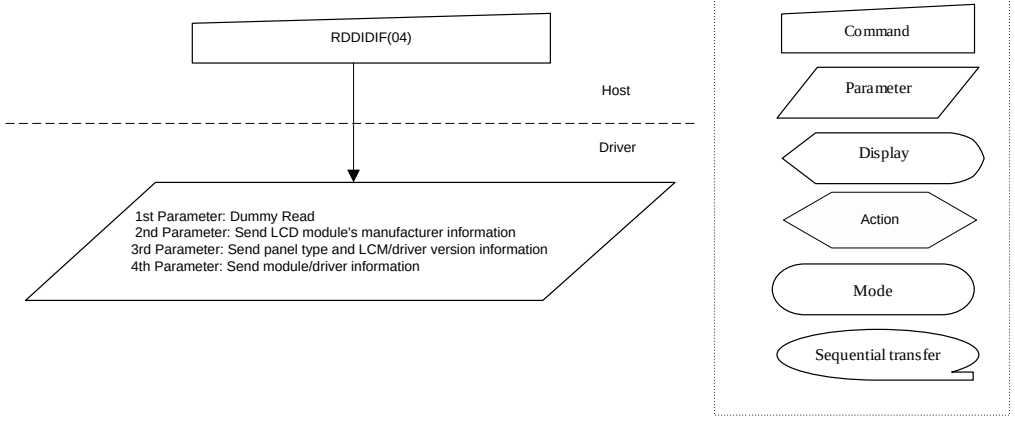
													h
	1	1	↑	XX	0	DINV[2:0]			RTN1[3:0]				11
	1	1	↑	XX	RTN2[7:0]								40
SPI 2data control	0	1	↑	XX	1	1	1	0	1	0	0	1	E9 h
	1	1	↑	XX					2data_ en	2data_mdt			00
Charge Pump Frequent Control	0	1	↑	XX	1	1	1	0	1	1	0	0	EC h
	1	1	↑	XX		avdd_clk_ad[2:0]				avee_clk_ad[2:0]			33
	1	1	↑	XX						vcl_clk_ad[2:0]			02
	1	1	↑	XX	vgh_clk_ad[3:0]				vgl_clk_ad[3:0]				88
Inner register enable 1	0	1	↑	XX	1	1	1	1	1	1	1	0	FE h
Inner register enable 2	0	1	↑	XX	1	1	1	0	1	1	1	1	EF h
SET_GAM MA1	0	1	↑	XX	1	1	1	1	0	0	0	0	F0h
	1	1	↑	XX	dig2gam_ dig2j0_n[1:0]	dig2gam_vr1_n[5:0]							80
	1	1	↑	XX	dig2gam_ dig2j1_n[1:0]	dig2gam_vr2_n[5:0]							03
	1	1	↑	XX	0	0	0	dig2gam_vr4_n[4:0]					08
	1	1	↑	XX	0	0	0	dig2gam_vr6_n[4:0]					06
	1	1	↑	XX	dig2gam_vr0_n[3:0]			dig2gam_vr13_n[3:0]					05
	1	1	↑	XX	0	dig2gam_vr20_n[6:0]							2B
SET_GAM MA2	0	1	↑	XX	1	1	1	1	0	0	0	1	F1h
	1	1	↑	XX	0	dig2gam_vr43_n[6:0]							41
	1	1	↑	XX	dig2gam_vr27_n [2:0]			dig2gam_vr57_n[4:0]					97
	1	1	↑	XX	dig2gam_vr36_n [2:0]			dig2gam_vr59_n[4:0]					98
	1	1	↑	XX	0	0	dig2gam_vr61_n[5:0]						13
	1	1	↑	XX	0	0	dig2gam_vr62_n[5:0]						17
	1	1	↑	XX	dig2gam_vr50_n[3:0]			dig2gam_vr63_n[3:0]					CD
SET_GAM MA3	0	1	↑	XX	1	1	1	1	0	0	1	0	F2h
	1	1	↑	XX	dig2gam_ dig2j0_p[1:0]	dig2gam_vr1_p[5:0]							40

	1	1	↑	XX	dig2gam_dig2j1_p[1:0]		dig2gam_vr2_p[5:0]							03
	1	1	↑	XX	0	0	0	dig2gam_vr4_p[4:0]						08
	1	1	↑	XX	0	0	0	dig2gam_vr6_p[4:0]						0B
	1	1	↑	XX	dig2gam_vr0_p[3:0]				dig2gam_vr13_p[3:0]					08
	1	1	↑	XX	0	dig2gam_vr20_p[6:0]								2E
SET_GAMMA4	0	1	↑	XX	1	1	1	1	0	0	1	1		F3h
	1	1	↑	XX	0	dig2gam_vr43_p[6:0]								3F
	1	1	↑	XX	dig2gam_vr27_p[2:0]			dig2gam_vr57_p[4:0]						98
	1	1	↑	XX	dig2gam_vr36_p[2:0]			dig2gam_vr59_p[4:0]						B4
	1	1	↑	XX	0	0	dig2gam_vr61_p[5:0]							14
	1	1	↑	XX	0	0	dig2gam_vr62_p[5:0]							18
	1	1	↑	XX	dig2gam_vr50_p[3:0]				dig2gam_vr63_p[3:0]					CD

6.2. Description of Level 1 Command

6.2.1. Read display identification information (04h)

<table>
<tr><td>04h</td><td colspan="13">Read display identification information 2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>04h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID_1[7:0]</td><td>00</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID_2[7:0]</td><td>93</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID_3[7:0]</td><td>08</td></tr>
<tr><td>Description</td><td colspan="13">This read byte returns 24 bits display identification information.
The 1st parameter is dummy data.
The 2nd parameter (ID2_1 [7:0]): LCD module’s manufacturer ID.
The 3rd parameter (ID2_2 [7:0]): LCD module/driver version ID.
The 4th parameter (ID2_3 [7:0]): LCD module/driver ID.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>24’h009308</td></tr><tr><td>SW Reset</td><td>24’h009308</td></tr><tr><td>HW Reset</td><td>24’h009308</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"></td></tr>
</table>


RDDIDIF(04)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send LCD module's manufacturer information
3rd Parameter: Send panel type and LCM/driver version information
4th Parameter: Send module/driver information
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.2. Read Display Status (09h)

09h	Read Display Status												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D[31:25]							X	00
3rd Parameter	1	↑	1	XX	0	D[22:20]			D[19:16]				61
4th Parameter	1	↑	1	XX	0	0	0	0	0	D[10:8]			00
5th Parameter	1	↑	1	XX	D[7:5]			0	0	0	0	0	00

Description

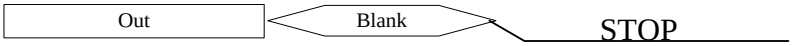
This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Status
D31	Booster voltage status	O	Booster OFF
		1	Booster ON
D30	Row address order	O	Top to Bottom (When MADCTL B7='0')
		1	Bottom to Top (When MADCTL B7='1')
D29	Column address order	O	Left to Right (When MADCTL B6='0').
		1	Right to Left (When MADCTL B6='1').
D28	Row/column exchange	O	Normal Mode (When MADCTL B5='0').
		1	Reverse Mode (When MADCTL B5='1').
D27	Vertical refresh	O	LCD Refresh Top to BoUom (When MADCTL B4='0')
		1	LCD Refresh BoUom to Top (When MADCTL B4='1').
D26	RGB/BGR order	O	RGB (When MADCTL B3='0')
		1	BGR (When MADCTL B3='1')
D25	Horizontal refresh order	O	LCD Refresh Left to Right (When MADCTL B2='0')
		1	LCD Refresh Right to Left (When MADCTL B2='1')
D24	Not used	O	-
D23	Not used	O	-
D22	Interface color pixel format definition	101	16-bit/pixel
D21		110	18-bit/pixel
D20			

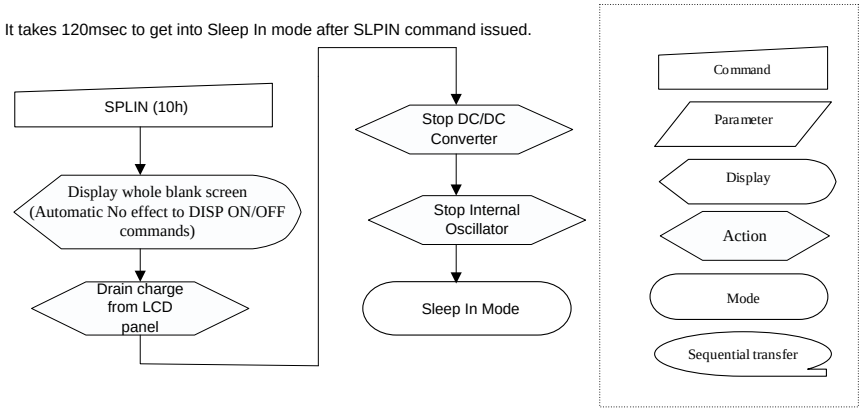
		D19	Idle mode ON/OFF	O	Idle Mode OFF
				1	Idle Mode ON
		D18	Partial mode ON/OFF	O	Partial Mode OFF
				1	Partial Mode ON
		D17	Sleep IN/OUT	O	Sleep IN Mode
				1	Sleep OUT Mode
		D16	Display normal mode ON/OFF	O	Display Normal Mode OFF.
				1	Display Normal Mode ON.
		D15	Vertical scrolling status	O	Scroll OFF
		D14	Not used	O	-
		D13	Inversion status	O	Not defined
		D12	All pixel ON	O	Not defined
		D11	All pixel OFF	O	Not defined
		D10	Display ON/OFF	O	
				1	Display is ON
		D9	Tearing effect line ON/OFF	O	Tearing Effect Line OFF
				1	Tearing Effect ON
		D5	Tearing effect line mode	0	Mode 1, V-Blanking only
				1	Mode 2, both H-Blanking and V-Blanking
		D4	Not used	O	-
		D3	Not used	O	-
		D2	Not used	O	-
		D1	Not used	O	-
		D0	Not used	O	-
Restriction					
Register Availability					

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

6.2.3. Enter Sleep Mode (10h)

<table>
<tr><td>10h</td><td colspan="13">Enter Sleep Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>10h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped
 

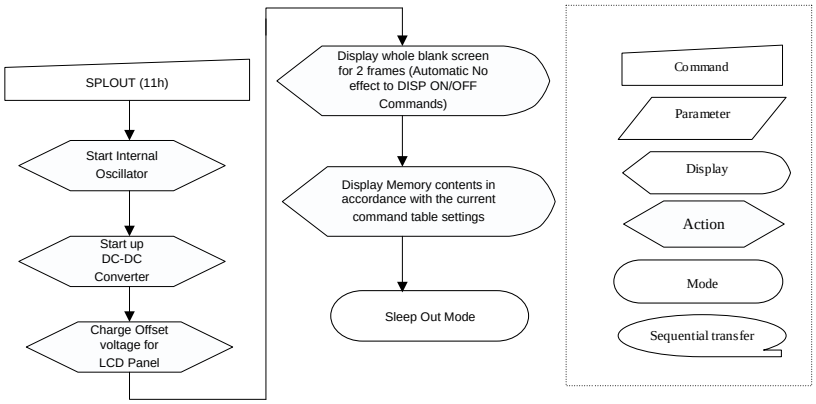
MCU interface and memory are still working and the memory keeps its contents.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>SW Reset</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></table></td></tr>
</table>

Flow Chart	

It takes 120msec to get into Sleep In mode after SLPIN command issued.
SPLIN (10h)
Display whole blank screen (Automatic No effect to DISP ON/OFF commands)
Drain charge from LCD panel
Stop DC/DC Converter
Stop Internal Oscillator
Sleep In Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.4. Sleep Out Mode (11h)

<table>
<tr><td>11h</td><td colspan="13">Sleep Out Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns off sleep mode.
the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits stabilize. The display module loads all display supplier’s factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>SW Reset</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></table></td></tr>
</table>

Flow Chart	

SPLOUT (11h)
Start Internal Oscillator
Start up DC-DC Converter
Charge Offset voltage for LCD Panel
Display whole blank screen for 2 frames (Automatic No effect to DISP ON/OFF Commands)
Display Memory contents in accordance with the current command table settings
Sleep Out Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

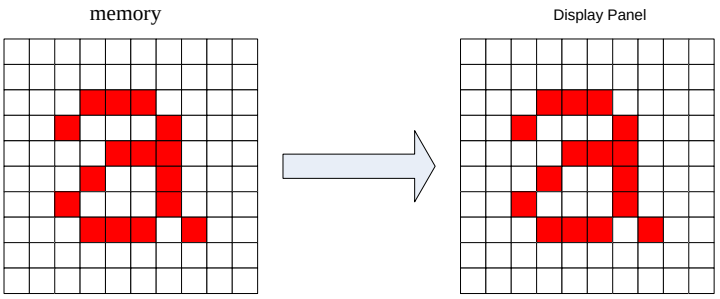
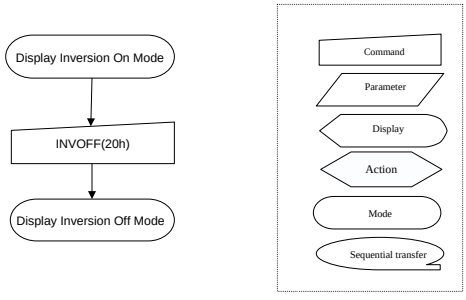
6.2.5. Partial Mode ON (12h)

<table>
<tr><td>12h</td><td colspan="13">Partial Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

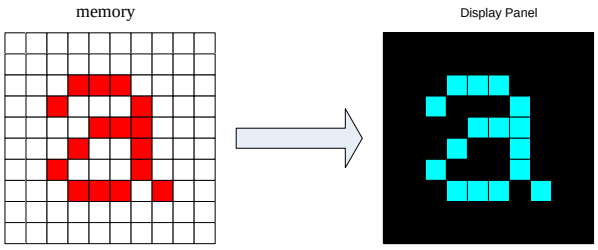
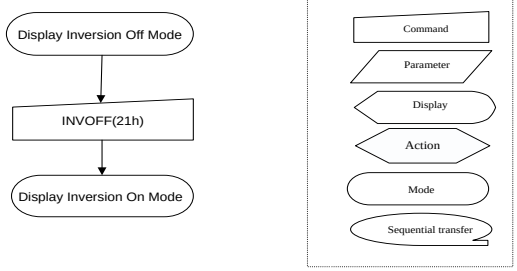
6.2.6. Normal Display Mode ON (13h)

<table>
<tr><td>13h</td><td colspan="13">Normal Display Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the display to normal mode.
Normal display mode on means Partial mode off.
Exit from NORON by the Partial mode On command (12h)
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

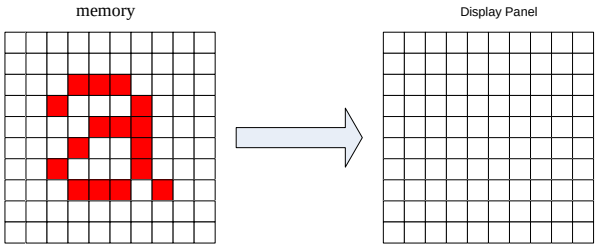
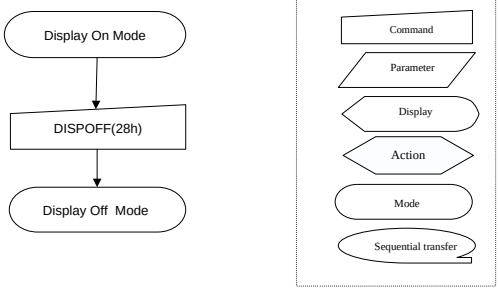
6.2.7. Display Inversion OFF (20h)

<table>
<tr><td>20h</td><td colspan="13">Display Inversion OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>20h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from display inversion mode.
This command makes no change of the content of frame memory.
This command doesn’t change any other status.
 
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module already is inversion OFF mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion OFF</td></tr><tr><td>SW Reset</td><td>Display Inversion OFF</td></tr><tr><td>HW Reset</td><td>Display Inversion OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">  </td></tr>
</table>

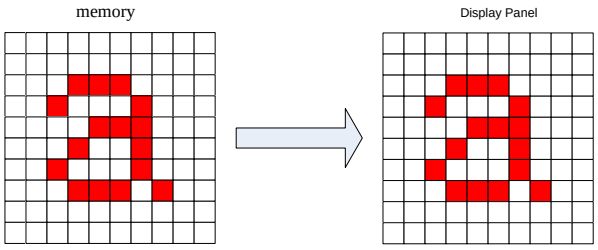
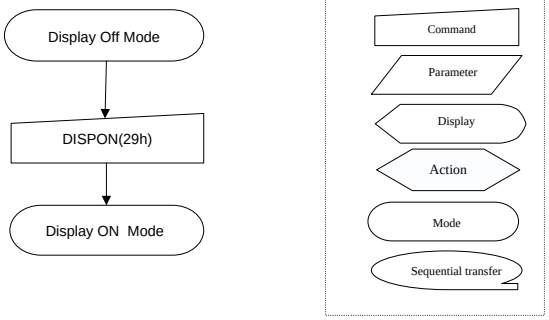
6.2.8. Display Inversion ON (21h)

<table>
<tr><td>21h</td><td colspan="13">Display Inversion ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>21h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into display inversion mode.
This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display.
This command doesn’t change any other status.
To exit Display inversion mode, the Display inversion OFF command (20h) should be written..
 
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module already is inversion ON mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion OFF</td></tr><tr><td>SW Reset</td><td>Display Inversion OFF</td></tr><tr><td>HW Reset</td><td>Display Inversion OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">  </td></tr>
</table>

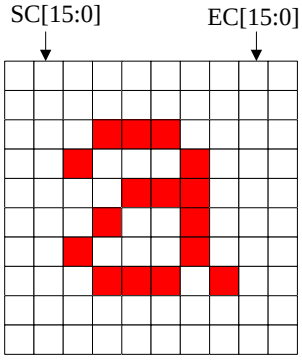
6.2.9. Display OFF (28h)

<table>
<tr><td>28h</td><td colspan="13">Display OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>28h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.
This command makes no change of contents of frame memory.
This command does not change any other status.
There will be no abnormal visible effect on the display.
 
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in display off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display OFF</td></tr><tr><td>SW Reset</td><td>Display OFF</td></tr><tr><td>HW Reset</td><td>Display OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">  </td></tr>
</table>

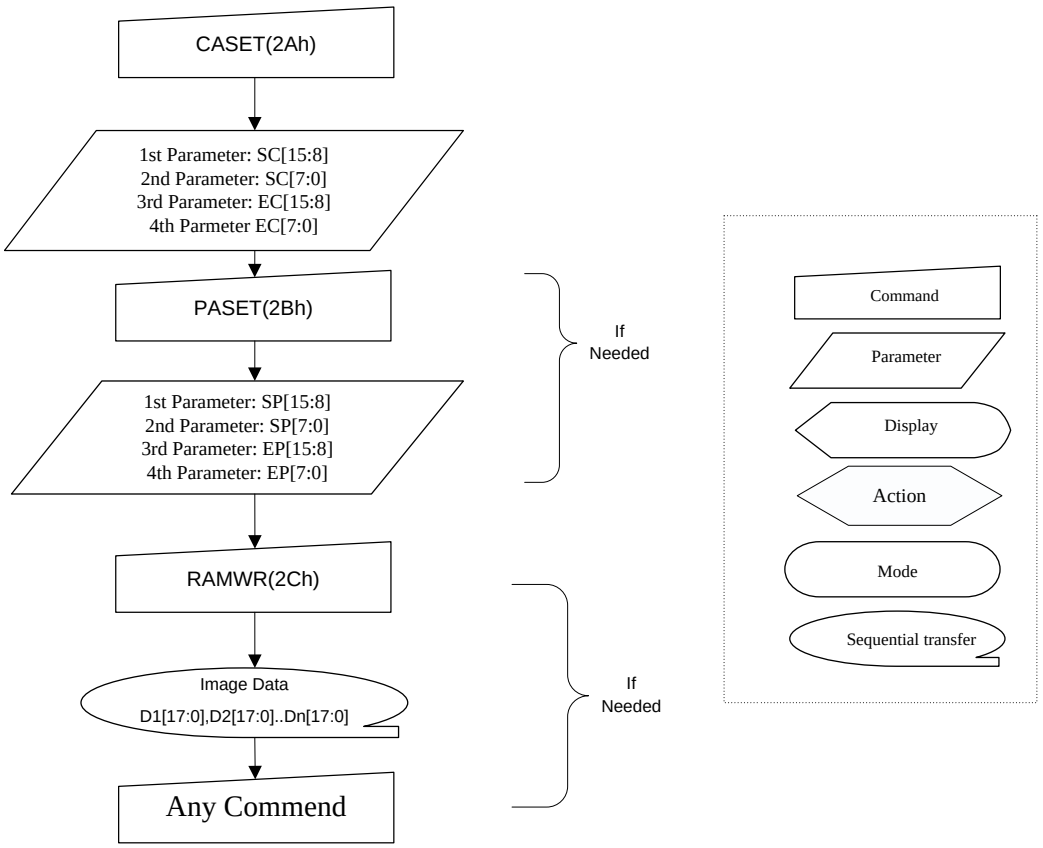
6.2.10. Display ON (29h)

<table>
<tr><td>29h</td><td colspan="13">Display ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.
 
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display OFF</td></tr><tr><td>SW Reset</td><td>Display OFF</td></tr><tr><td>HW Reset</td><td>Display OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">  </td></tr>
</table>

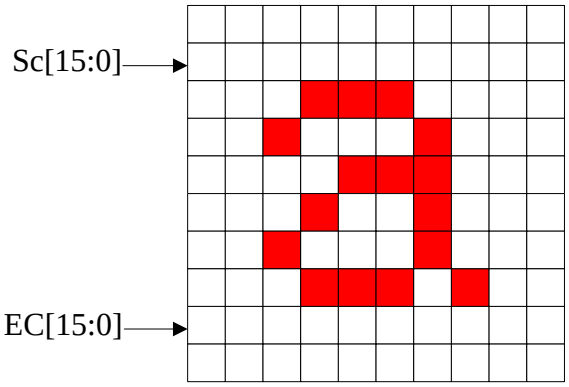
6.2.11. Column Address Set (2Ah)

<table>
<tr><td>2Ah</td><td colspan="13">Column Address Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>2Ah</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SC15</td><td>SC14</td><td>SC13</td><td>SC12</td><td>SC11</td><td>SC10</td><td>SC9</td><td>SC8</td><td rowspan="2">Note1</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SC7</td><td>SC6</td><td>SC5</td><td>SC4</td><td>SC3</td><td>SC2</td><td>SC1</td><td>SC0</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EC15</td><td>EC14</td><td>EC13</td><td>EC12</td><td>EC11</td><td>EC10</td><td>EC9</td><td>EC8</td><td rowspan="2">Note1</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EC7</td><td>EC6</td><td>EC5</td><td>EC4</td><td>EC3</td><td>EC2</td><td>EC1</td><td>EC0</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value
represents one column line in the Frame Memory..
 

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">SC [15:0] always must be equal to or less than EC [15:0].
Note 1: When SC [15:0] or EC [15:0] is greater than 013Fh (When MADCTL’s B5 = 0) or 00EFh (When MADCTL’s B5 = 1), data of out of range will be ignored</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th colspan="2">Default Value</th></tr><tr><td>Power On Sequence</td><td>SC [15:0]=0000h</td><td>EC [15:0]=013Fh</td></tr></table></td></tr>
</table>

	SW Reset	SC [15:0]=0000h	If MADCTL's B5 = 0: EC [15:0]=013Fh
			If MADCTL's B5 = 1: EC [15:0]=00EFh
	HW Reset	SC [15:0]=0000h	EC [15:0]=00EFh
Flow Chart			

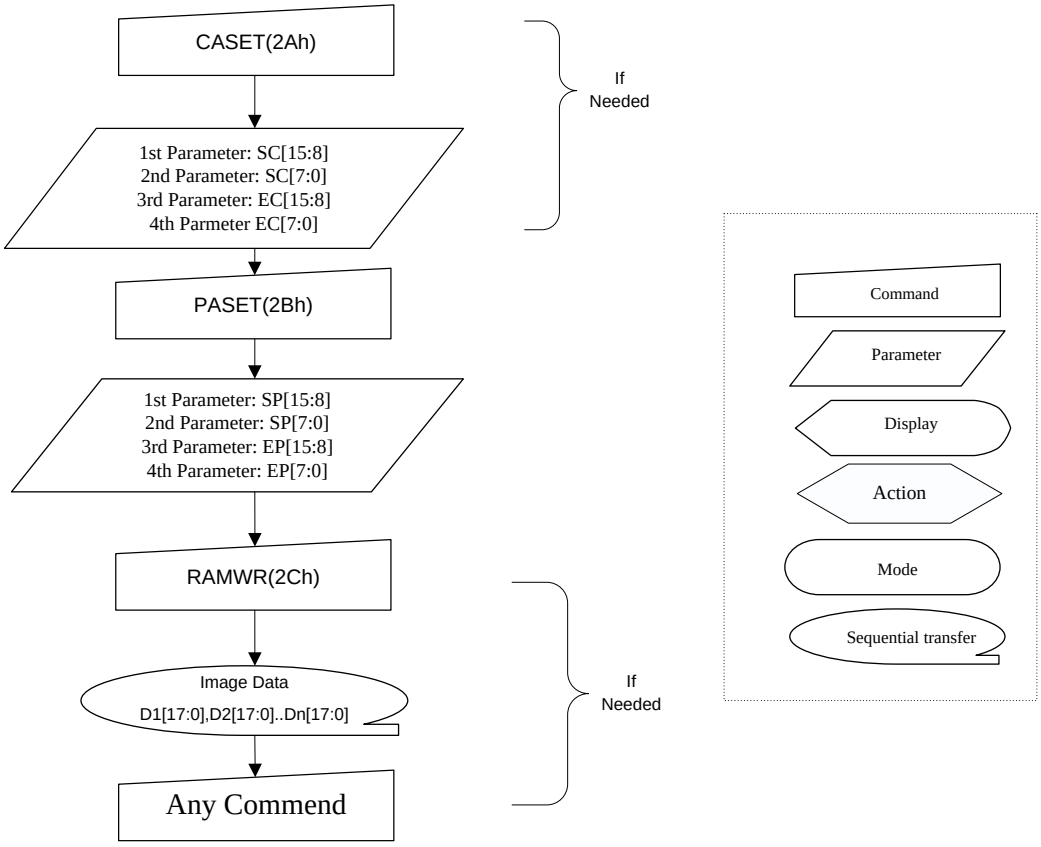
6.2.12. Row Address Set (2Bh)

<table>
<tr><td>2Bh</td><td colspan="13">Row Address Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>2Bh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SP15</td><td>SP14</td><td>SP13</td><td>SP12</td><td>SP11</td><td>SP10</td><td>SP9</td><td>SP8</td><td rowspan="2">Note1</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SP7</td><td>SP6</td><td>SP5</td><td>SP4</td><td>SP3</td><td>SP2</td><td>SP1</td><td>SP0</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EP15</td><td>EP14</td><td>EP13</td><td>EP12</td><td>EP11</td><td>EP10</td><td>EP9</td><td>EP8</td><td rowspan="2">Note1</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EP7</td><td>EP6</td><td>EP5</td><td>EP4</td><td>EP3</td><td>EP2</td><td>EP1</td><td>EP0</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to define area of frame memory where MCU can access. This command makes no change on the
other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value
represents one Page line in the Frame Memory.
 

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">SP [15:0] always must be equal to or less than EP [15:0]
Note 1: When SP [15:0] or EP [15:0] is greater than 00EFh (When MADCTL’s B5 = 0) or 013Fh (When MADCTL’s B5 = 1), data of out of range will be ignored.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"></td></tr>
</table>

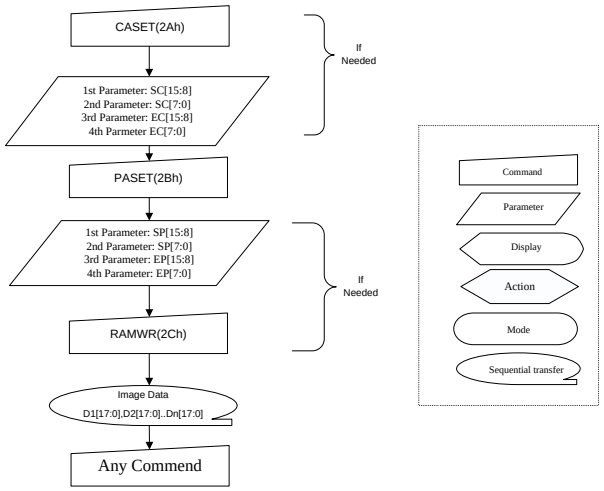
Status	Default Value	
Power On Sequence	SP [15:0]=0000h	EP [15:0]=00EFh
SW Reset	SP [15:0]=0000h	If MADCTL's B5 = 0: EP [15:0]=00EFh
		If MADCTL's B5 = 1: EP [15:0]=013Fh
HW Reset	SP [15:0]=0000h	EP [15:0]=00EFh

Flow Chart

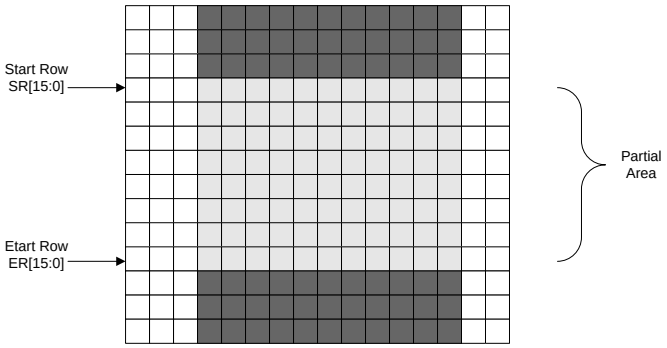
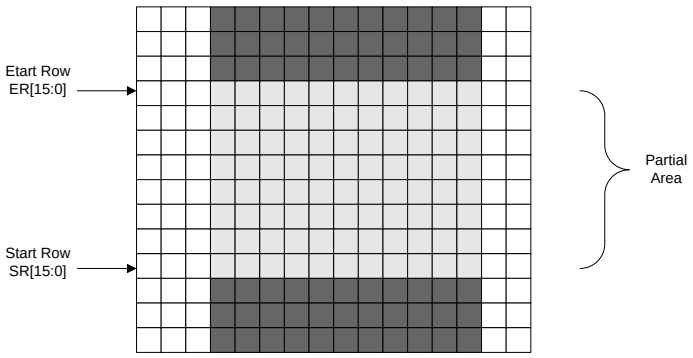


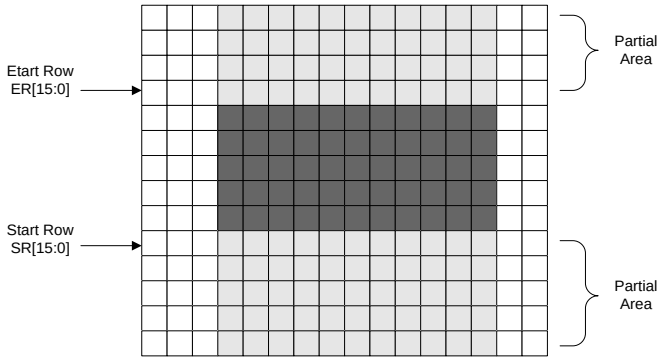
6.2.13. Memory Write (2Ch)

<table>
<tr><td>2Ch</td><td colspan="13">Memory Write</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>2Ch</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="9">D1 [17:0]</td><td>XX</td></tr>
<tr><td>:</td><td>1</td><td>1</td><td>↑</td><td colspan="9">Dx [17:0]</td><td>XX</td></tr>
<tr><td>Nth Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="9">Dn [17:0]</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver
status. When this command is accepted, the column register and the page register are reset to the Start Column/Start
Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] isstored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">In all color modes, there is no restriction on length of parameters.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>SW Reset</td><td rowspan="2">Contents of memory is not cleared</td></tr><tr><td>HW Reset</td></tr></table></td></tr>
</table>

Flow Chart	 CASET(2Ah) 1st Parameter: SC[15:8] 2nd Parameter: SC[7:0] 3rd Parameter: EC[15:8] 4th Parmeter EC[7:0] If Needed PASET(2Bh) 1st Parameter: SP[15:8] 2nd Parameter: SP[7:0] 3rd Parameter: EP[15:8] 4th Parameter: EP[7:0] If Needed RAMWR(2Ch) Image Data D1[17:0],D2[17:0]..Dn[17:0] Any Commend Command Parameter Display Action Mode Sequential transfer

6.2.14. Partial Area (30h)

30h	Partial Area												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2nd Parameter	1	1	↑	XX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3rd Parameter	1	1	↑	XX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	00
4th Parameter	1	1	↑	XX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	EF
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row>Start Row when MADCTL B4=0:-  If End Row>Start Row when MADCTL B4=1:-  If End Row<Start Row when MADCTL B4=0:-												



If End Row = Start Row then the Partial Area will be one row deep.

X = Don't care.

Restriction	SR [15…0] and ER [15…0] cannot be 0000h nor exceed 013Fh.

Register Availability

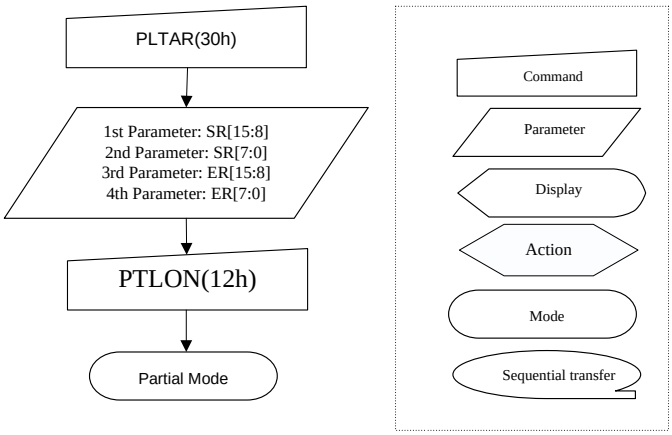
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

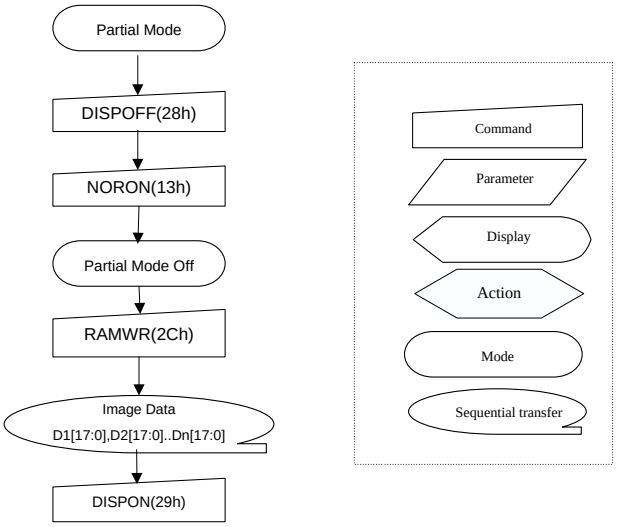
Status	Default Value	
	SR [15:0]	ER [15:0]
Power On Sequence	16'h0000h	16'h00EFh
SW Reset	16'h0000h	16'h00EF h
HW Reset	16'h0000h	16'h00EF h

Flow Chart

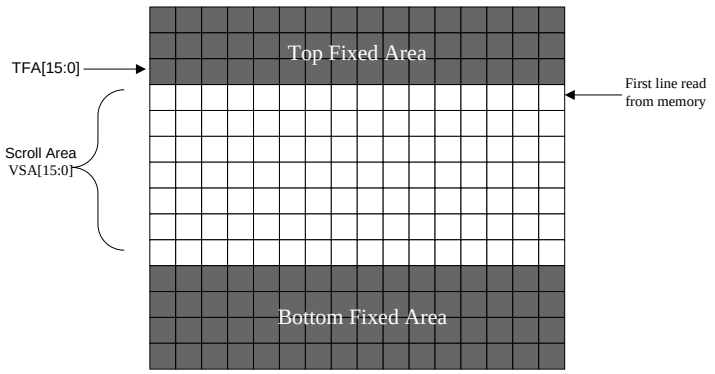
1. To Enter Partial Mode

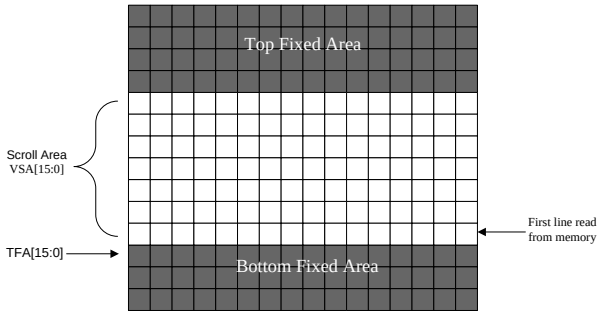


2. To Leave Partial Mode



6.2.15. Vertical Scrolling Definition (33h)

33h	Vertical Scrolling Definition												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1st Parameter	1	1	↑	XX	TFA [15:8]								00
2nd Parameter	1	1	↑	XX	TFA [7:0]								00
3rd Parameter	1	1	↑	XX	VSA [15:8]								00
4th Parameter	1	1	↑	XX	VSA [7:0]								F0
Description	This command defines the Vertical Scrolling Area of the display. When MADCTL B4=0 The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display). The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.  When MADCTL B4=1 The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.												



X = Don’t care.

Restriction

Register Availability

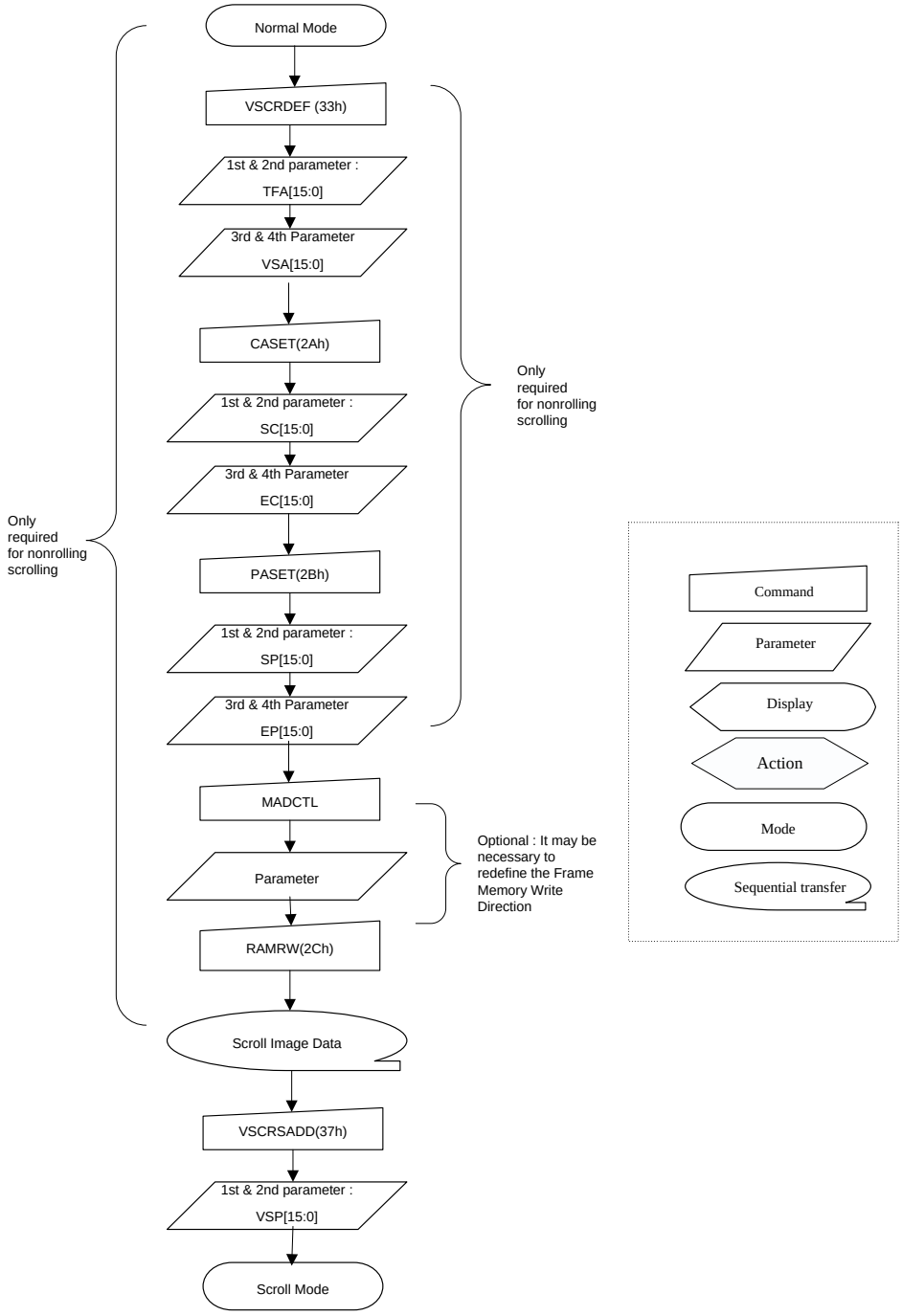
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	TFA [15:0]	VSA [15:0]
Power On Sequence	16’h0000h	16’h00F0h
SW Reset	16’h0000h	16’h00F 0h
HW Reset	16’h0000h	16’h00F 0h

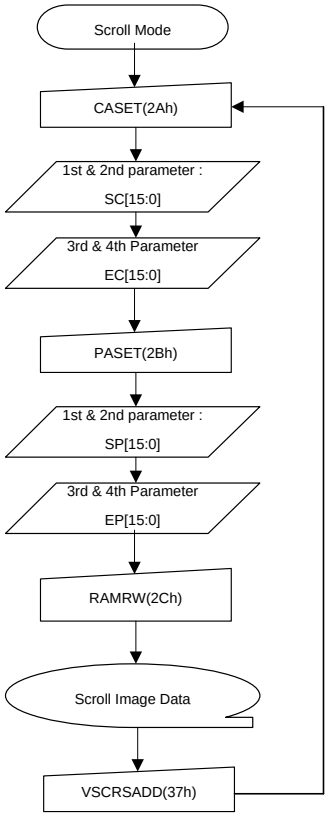
Flow Chart

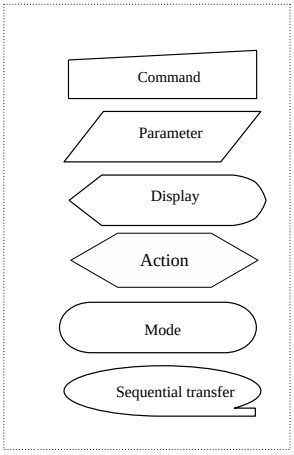
1. To enter Vertical Scroll Mode :



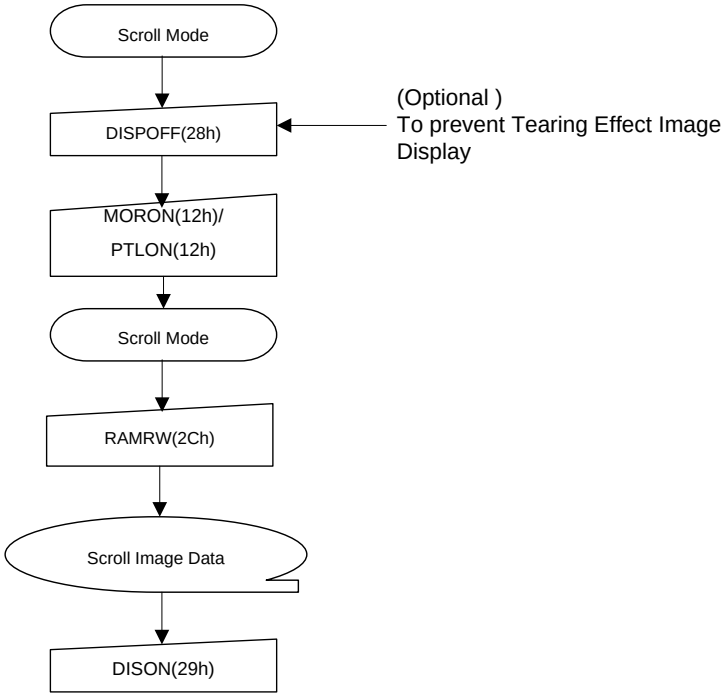
Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.

2.Continuous Scroll :



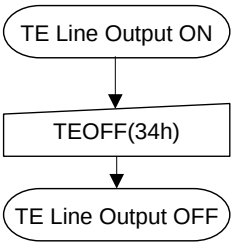


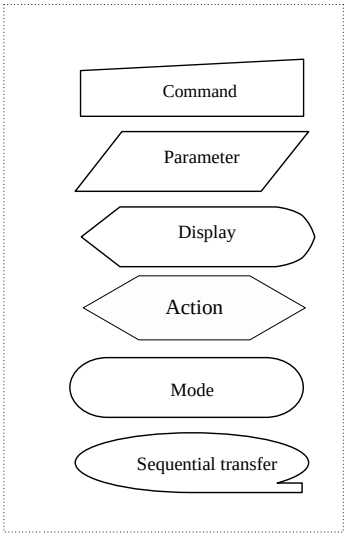
3.To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode ON (13h) and Partial Mode ON (12h) commands.

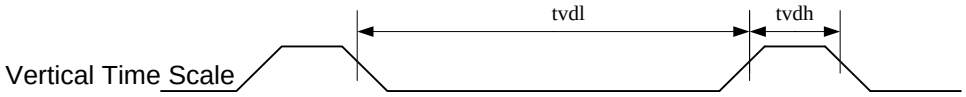
6.2.16. Tearing Effect Line OFF (34h)

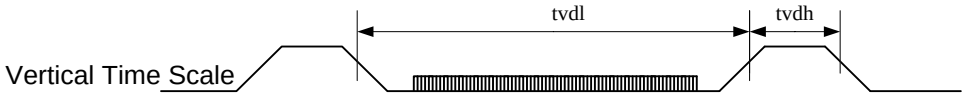
<table>
<tr><td>34h</td><td colspan="13">Tearing Effect Line OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>34h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already OFF.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 


</td></tr>
</table>

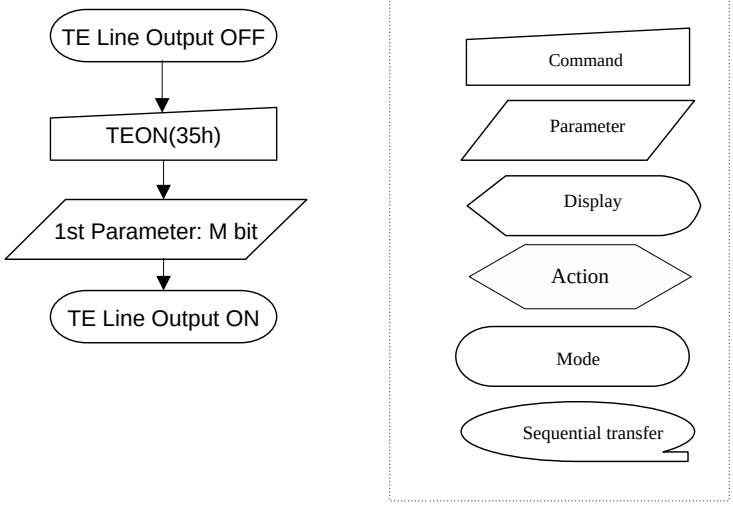
6.2.17. Tearing Effect Line ON (35h)

<table>
<tr><td>35h</td><td colspan="13">Tearing Effect Line ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>35h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>M</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by
changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When M=0:
The Tearing Effect Output line consists of V-Blanking information only:
 

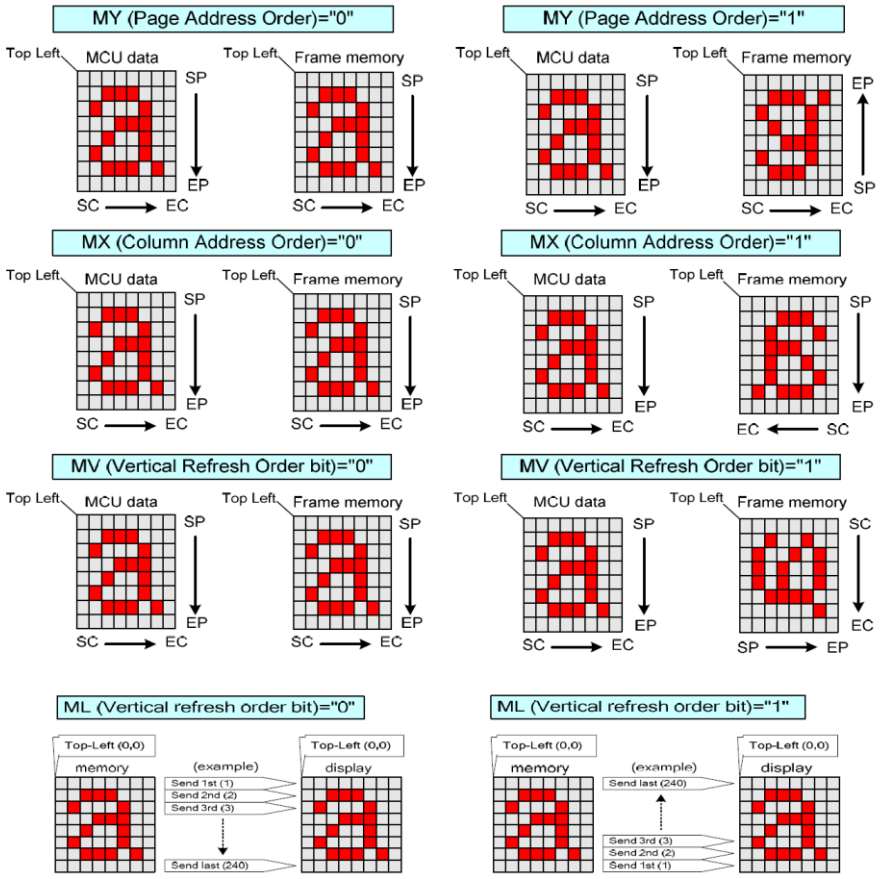
When M=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:
 

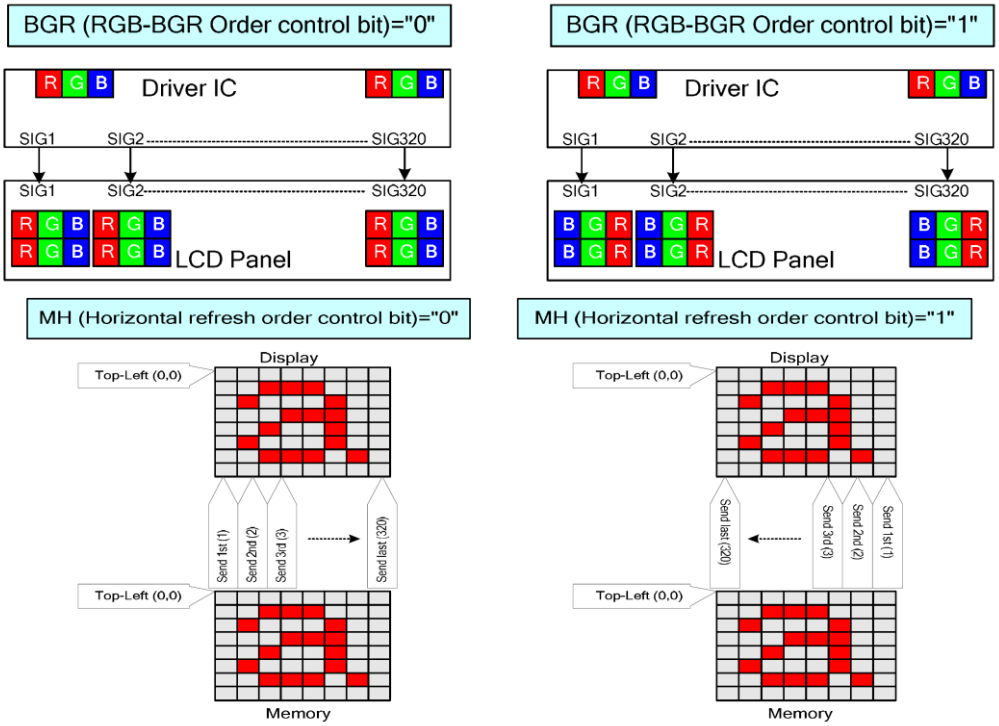
Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
</table>

Flow Chart	

TE Line Output OFF
TEON(35h)
1st Parameter: M bit
TE Line Output ON
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.18. Memory Access Control(36h)

<table>
<tr><td>36h</td><td colspan="13">Tearing Effect Line ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>36h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>MY</td><td>MX</td><td>MV</td><td>ML</td><td>BGR</td><td>MH</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.
<table><tr><th>Bit</th><th>Name</th><th>Description</th></tr><tr><td>MY</td><td>Row Address Order</td><td rowspan="3">These 3 bits control MCU to memory write/read direction.</td></tr><tr><td>MX</td><td>Column Address Order</td></tr><tr><td>MV</td><td>Row / Column Exchange</td></tr><tr><td>ML</td><td>Vertical Refresh Order</td><td>LCD vertical refresh direction control.</td></tr><tr><td>BGR</td><td>RGB-BGR Order</td><td>Color selector switch control
(0=RGB color filter panel, 1=BGR color filter panel)</td></tr><tr><td>MH</td><td>Horizontal Refresh ORDER</td><td>LCD horizontal refreshing direction control.</td></tr></table>Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.
 
</td></tr>
</table>



Note: Top-Left (0,0) means a physical memory location.

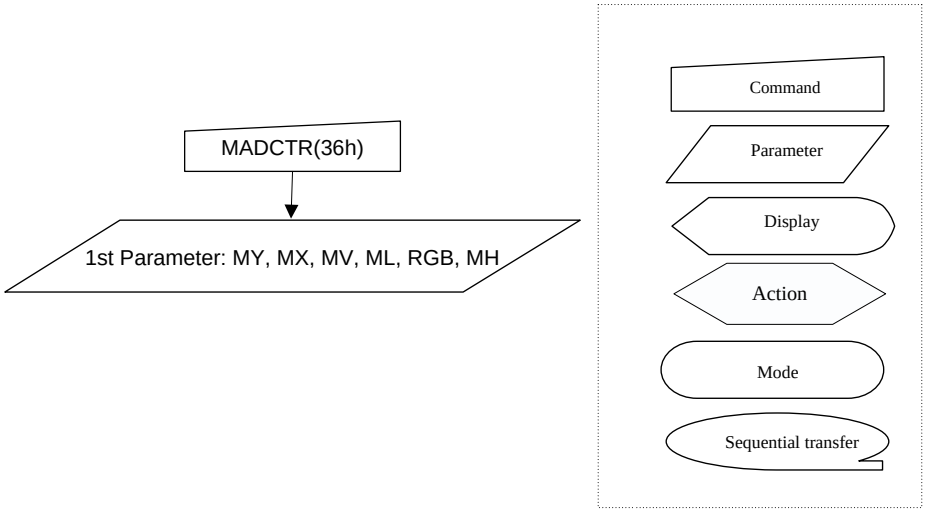
Restriction	This command has no effect when Tearing Effect output is already ON

Register Availability

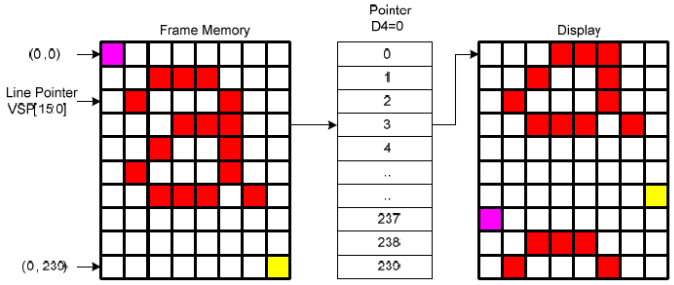
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

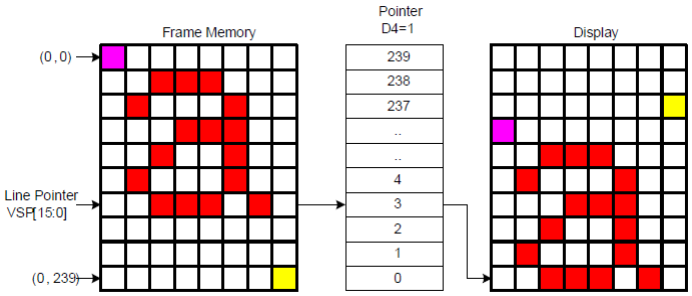
Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	No change
HW Reset	8'h00h

Flow Chart	 MADCTR(36h) 1st Parameter: MY, MX, MV, ML, RGB, MH Command Parameter Display Action Mode Sequential transfer

6.2.19. Vertical Scrolling Start Address (37h)

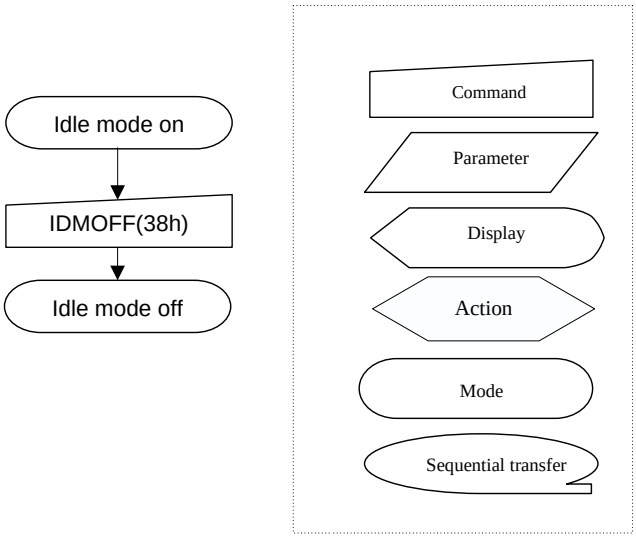
<table>
<tr><td>37h</td><td colspan="13">VSCRSADD (Vertical Scrolling Start Address)</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>37h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">VSP [15:8]</td><td>00</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">VSP [7:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area
and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-
When MADCTL B4=0
Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 240 and VSP=’3’.
 

When MADCTL B4=1
Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 240 and VSP=’3’.
 

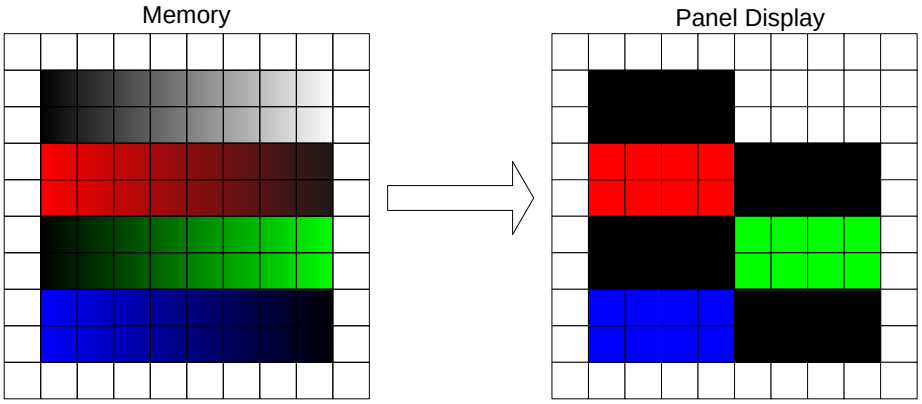
Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.
(2) This command is ignored when the GC9308 enters Partial mode.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already ON</td></tr>
</table>

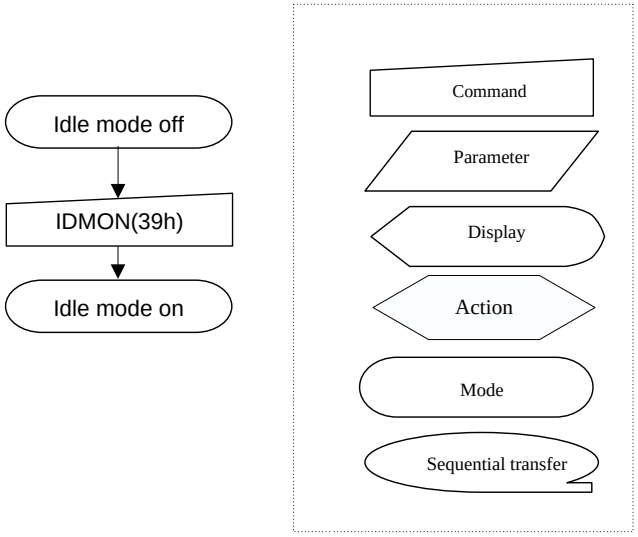
<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VSP [15:0]</th></tr>
<tr><td>Power On Sequence</td><td>16’h0000h</td></tr>
<tr><td>SW Reset</td><td>16’h0000h</td></tr>
<tr><td>HW Reset</td><td>16’h0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

6.2.20. Idle Mode OFF (38h)

<table>
<tr><td>38h</td><td colspan="13">Idle Mode OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>38h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from Idle mode on.
In the idle off mode, LCD can display maximum 262,144 colors.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle mode OFF</td></tr><tr><td>SW Reset</td><td>Idle mode OFF</td></tr><tr><td>HW Reset</td><td>Idle mode OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.21. Idle Mode ON (39h)

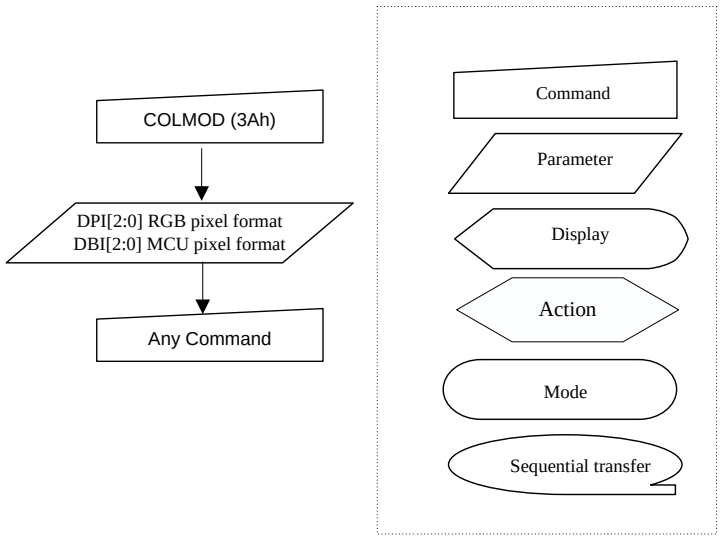
<table>
<tr><td>39h</td><td colspan="13">Idle Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>39h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into Idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
 
<table><tr><td></td><td colspan="3">Memory Contents vs. Display Color</td></tr><tr><td></td><td>R5 R4 R3 R2 R1 R0</td><td>G5 G4 G3 G2 G1 G0</td><td>B5 B4 B3 B2 B1 B0</td></tr><tr><td>Black</td><td>0XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Blue</td><td>0XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Red</td><td>1XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Magenta</td><td>1XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Green</td><td>0XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>Cyan</td><td>0XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr><tr><td>Yellow</td><td>1XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>White</td><td>1XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr></table>X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Idle mode OFF</td></tr>
<tr><td>SW Reset</td><td>Idle mode OFF</td></tr>
<tr><td>HW Reset</td><td>Idle mode OFF</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

6.2.22. COLMOD: Pixel Format Set (3Ah)

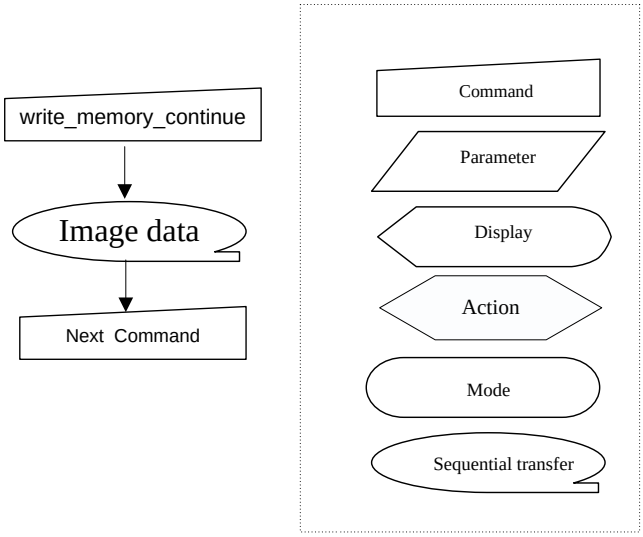
<table>
<tr><td>3Ah</td><td colspan="13">Pixel Format Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3Ah</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td colspan="3">DPI [2:0]</td><td>0</td><td colspan="3">DBI [2:0]</td><td>66</td></tr>
<tr><td>Description</td><td colspan="13">This command sets the pixel format for the RGB image data used by the interface. DPI [2:0] is the pixel format select of RGB interface and DBI [2:0] is the pixel format of MCU interface. If a particular interface, either RGB interface or MCU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below.
<table>
<tr><th colspan="3">DPI [2:0]</th><th>RGB Interface Format</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table>
<table>
<tr><th colspan="3">DBI [2:0]</th><th>MCU Interface Format</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>12 bits / pixel</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table>
If using RGB Interface must selection serial interface.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>DPI [2:0]</th><th>DBI [2:0]</th></tr>
<tr><td>Power On Sequence</td><td>3’b110</td><td>3’b110</td></tr>
<tr><td>SW Reset</td><td>No Change</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>3’b110</td><td>3’b110</td></tr>
</table>
</td></tr>
</table>

Flow Chart	 COLMOD (3Ah) DPI[2:0] RGB pixel format DBI[2:0] MCU pixel format Any Command Command Parameter Display Action Mode Sequential transfer

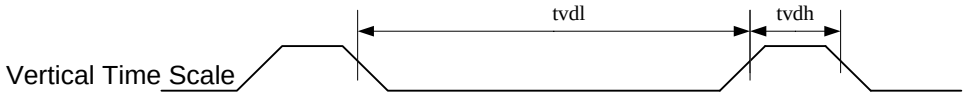
6.2.23. Write Memory Contiue (3Ch)

3Ch	write_memory_continue												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	D1[17..8]	0	0	1	1	1	1	0	0	3Ch
1st Parameter	1	1	↑	Dx[17..8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	0003FF
Xth Parameter	1	1	↑	D1[17..8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	0003FF
Nth Parameter	1	1	↑	Dn[17..8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	0003FF
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. **If set_address_mode B5 = 0:** Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC –SC + 1) * (EP – SP + 1) the extra pixels are ignored. **If set_address_mode B5 = 1:** Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP –SP + 1) the extra pixels are ignored. Sending any other command can stop frame Write. Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored. Frame Memory Access and Interface setting (B3h), WEMODE=1												

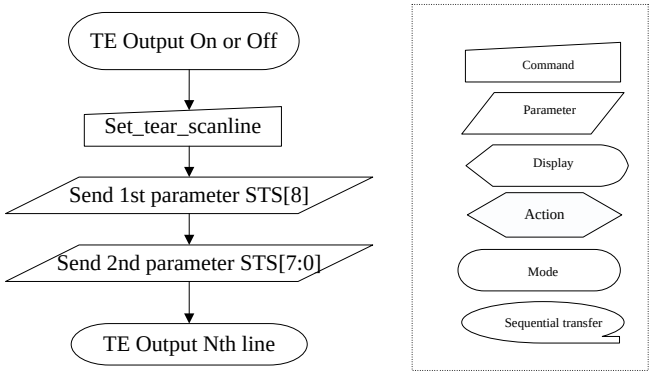
	When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.
Restriction	A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Random value</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>No change</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

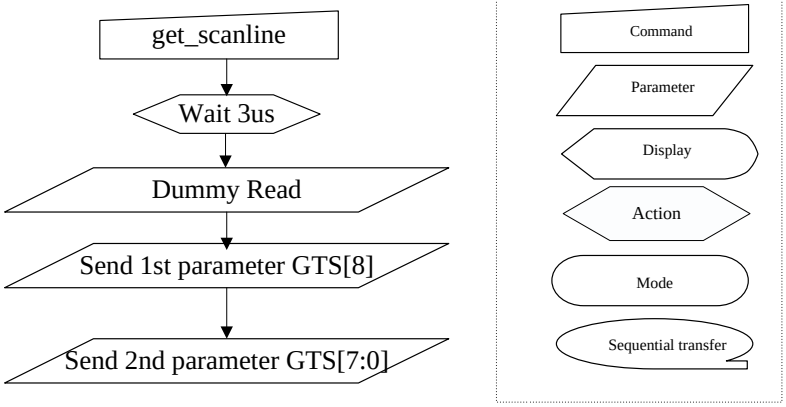
6.2.24. Set_Tear_Scanline (44h)

<table>
<tr><td>44h</td><td colspan="13">Set_Tear_Scanline</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>44h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>STS [8]</td><td>00</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>STS [7]</td><td>STS [6]</td><td>STS [5]</td><td>STS [4]</td><td>STS [3]</td><td>STS [2]</td><td>STS [1]</td><td>STS [0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line equal the value of STS[8:0]
 

Note:that set_tear_scanline with STS is equivalent to set_tear_on with 8+GateN(N=1、2、3...240)
eg:when the STS[8:0]=8,the TE will output at the position of Gate1.
when the STS[8:0]=9,the TE will output at the position of Gate2.
when the STS[8:0]=10,the TE will output at the position of Gate3.
…….
The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>STS [8:0]=0000h</td></tr><tr><td>SW Reset</td><td>STS [8:0]=0000h</td></tr><tr><td>HW Reset</td><td>STS [8:0]=0000h</td></tr></table></td></tr>
</table>

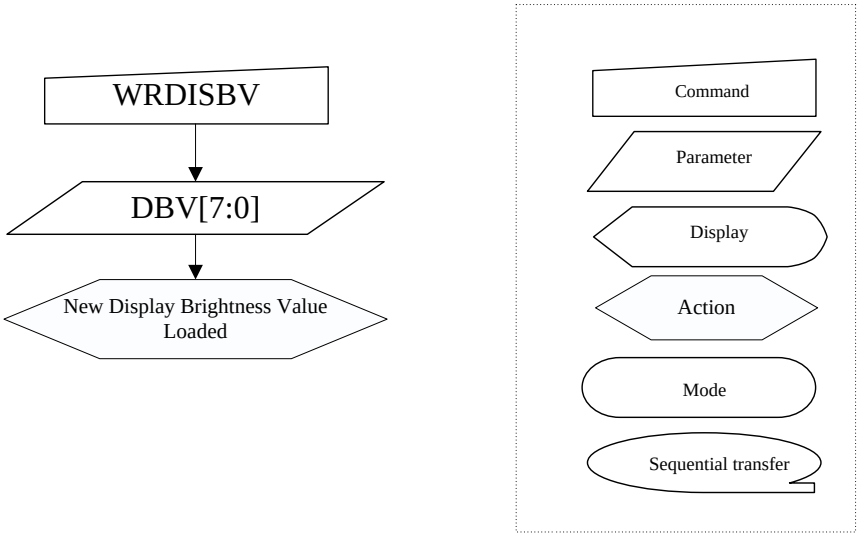
Flow Chart	 TE Output On or Off Set_tear_scanline Send 1st parameter STS[8] Send 2nd parameter STS[7:0] TE Output Nth line Command Parameter Display Action Mode Sequential transfer

6.2.25. Get_Scanline (45h)

<table>
<tr><td>45h</td><td colspan="13">Get_Scanline</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>45h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>GTS [8]</td><td>00</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>GTS [7]</td><td>GTS [6]</td><td>GTS [5]</td><td>GTS [4]</td><td>GTS [3]</td><td>GTS [2]</td><td>GTS [1]</td><td>GTS [0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the setting value of STS[8:0] .
When in Sleep Mode, the value returned by get_scanline is undefined.</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>GTS [9:0]=0000h</td></tr><tr><td>SW Reset</td><td>GTS [9:0]=0000h</td></tr><tr><td>HW Reset</td><td>GTS [9:0]=0000h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

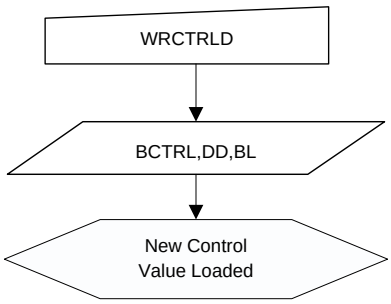
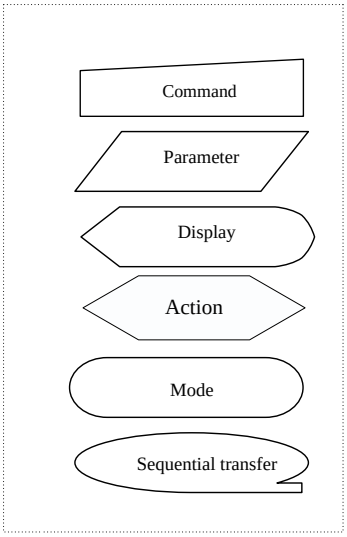
6.2.26. Write Display Brightness (51h)

<table>
<tr><td>51h</td><td colspan="13">Write Display Brightness</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>51h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>DBV[7]</td><td>DBV[6]</td><td>DBV[5]</td><td>DBV[4]</td><td>DBV[3]</td><td>DBV[6]</td><td>DBV[5]</td><td>DBV[4]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to adjust the brightness value of the display.
It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification.
In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>DBV [7:0]= 8’h00</td></tr><tr><td>SW Reset</td><td>DBV [7:0]= 8’h00</td></tr><tr><td>HW Reset</td><td>DBV [7:0]= 8’h00</td></tr></table></td></tr>
</table>

Flow Chart	 WRDISBV DBV[7:0] New Display Brightness Value Loaded Command Parameter Display Action Mode Sequential transfer

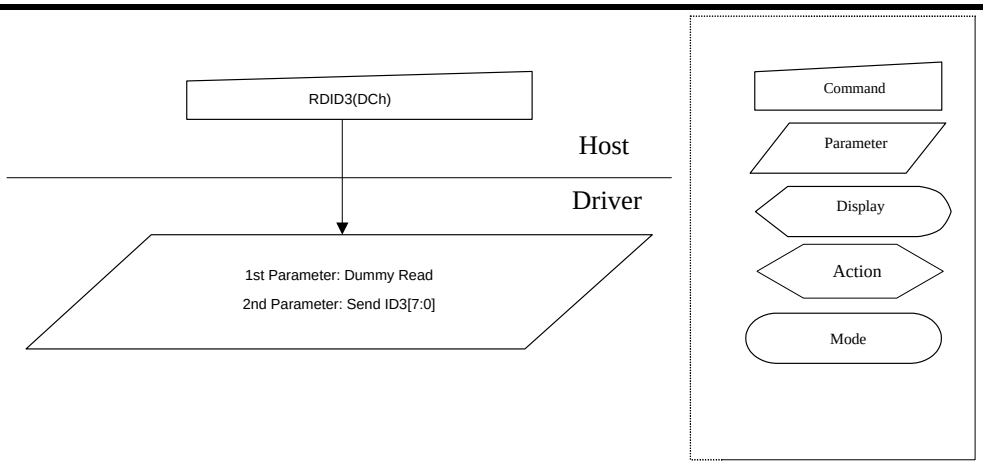
6.2.27. Write CTRL Display (53h)

<table>
<tr><td>53h</td><td colspan="13">Write CTRL Display</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>53h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>BCTRL</td><td>0</td><td>DD</td><td>BL</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to return brightness setting.
BCTRL: Brightness Control Block On/Off,
‘0’ = Off (Brightness registers are 00h)
‘1’ = On (Brightness registers are active, according to the DBV[7..0] parameters.)
DD: Display Dimming
‘0’ = Display Dimming is off
‘1’ = Display Dimming is on
BL: Backlight On/Off
‘0’ = Off (Completely turn off backlight circuit. Control lines must be low.)
‘1’ = On</td></tr>
<tr><td>Restriction</td><td colspan="13">The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter
(= more than 2 RDX cycle) on DBI.
Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>BCTRL</th><th>DD</th><th>BL</th></tr><tr><td>Power On Sequence</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr><tr><td>SW Reset</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr><tr><td>HW Reset</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr></table></td></tr>
</table>

Flow Chart	 WRCTRLD BCTRL,DD,BL New Control Value Loaded  Command Parameter Display Action Mode Sequential transfer

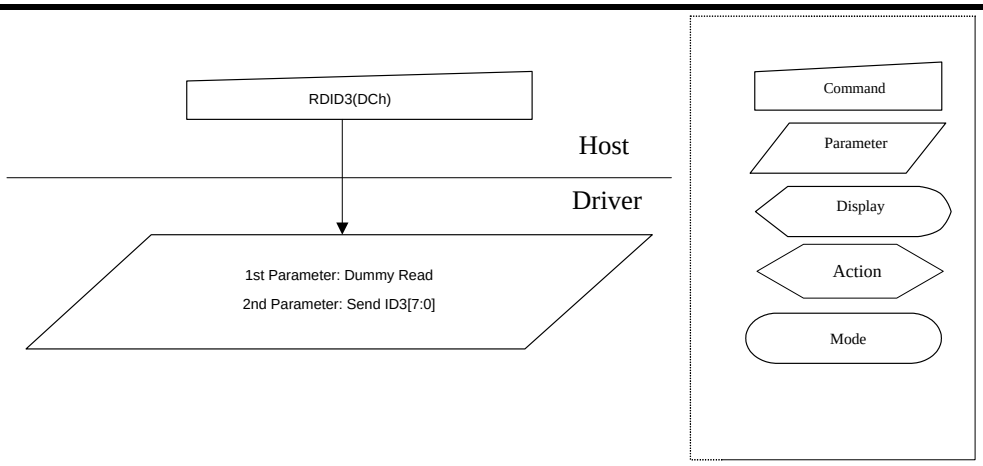
6.2.28. Read ID1 (DAh)

<table>
<tr><td>DCh</td><td colspan="13">Read ID2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>DAh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID3 [7:0]</td><td>Program value</td></tr>
<tr><td>Description</td><td colspan="13">This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User’s agreement) and changes each time a revision is made to the display, material or construction specifications.
The 1st parameter is dummy data.
The 2nd parameter is LCD module/driver version ID
The ID3 can be programmed by MTP function.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value (After MTP program)</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>SW Reset</td><td>8’h00</td></tr><tr><td>HW Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

Flow Chart	 RDID3(DCh) Host Driver 1st Parameter: Dummy Read 2nd Parameter: Send ID3[7:0] Command Parameter Display Action Mode

6.2.29. Read ID2 (DBh)

<table>
<tr><td>DCh</td><td colspan="13">Read ID2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>DBh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID3 [7:0]</td><td>Program value</td></tr>
<tr><td>Description</td><td colspan="13">This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User’s agreement) and changes each time a revision is made to the display, material or construction specifications.
The 1st parameter is dummy data.
The 2nd parameter is LCD module/driver version ID
The ID3 can be programmed by MTP function.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value (After MTP program)</th></tr><tr><td>Power On Sequence</td><td>8’h93</td></tr><tr><td>SW Reset</td><td>8’h93</td></tr><tr><td>HW Reset</td><td>8’h93</td></tr></table></td></tr>
</table>

Flow Chart	 RDID3(DCh) Host Driver 1st Parameter: Dummy Read 2nd Parameter: Send ID3[7:0] Command Parameter Display Action Mode

6.2.30. Read ID3 (DCh)

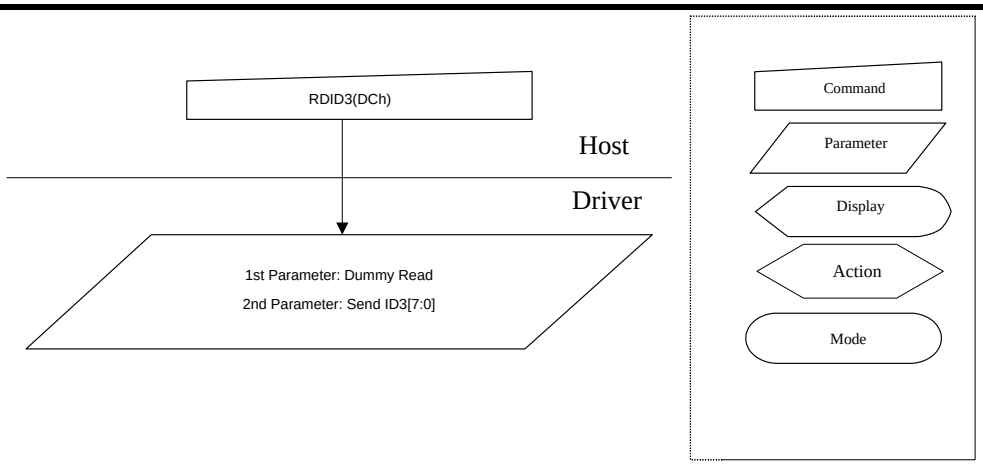
DCh	Read ID2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID3 [7:0]								Program value
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID The ID3 can be programmed by MTP function. X = Don't care												
Restriction	None												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (After MTP program)
Power On Sequence	8'h08
SW Reset	8'h08
HW Reset	8'h08

Flow Chart	 RDID3(DCh) Host Driver 1st Parameter: Dummy Read 2nd Parameter: Send ID3[7:0] Command Parameter Display Action Mode

6.3. Description of Level 2 Command

6.3.1. RGB Interface Signal Control (B0h)

<table>
<tr><td>B0h</td><td colspan="14">RGB Interface Signal Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B0h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>RCM[1]</td><td>RCM[0]</td><td>0</td><td>VSPL</td><td>HSPL</td><td>DPL</td><td>EPL</td><td>01</td></tr>
<tr><td>Description</td><td colspan="14">Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.
EPL: DE polarity (“0”= High enable for RGB interface, “1”= Low enable for RGB interface)
DPL: DOTCLK polarity set (“0”= data fetched at the rising time, “1”= data fetched at the falling time)
HSPL: HSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock)
VSPL: VSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock)
RCM [1:0]: RGB interface selection (refer to the RGB interface section).
<table>
<tr><th colspan="2">RCM[1:0]</th><th>RIM</th><th colspan="3">DPI[1:0]</th><th>RGB interface Mode</th><th>RGB Mode</th><th>Used Pins</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>18-bit RGB interface (262K colors)</td><td rowspan="3">DE Mode
Valid data is determined by the DE signal</td><td>VSYNC,HSYNC,DE, DOTCLK,D[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>16-bit RGB interface (65K colors)</td><td>VSYNC,HSYNC,DE, DOTCLK,D[17:13] & D[11:1]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td colspan="3">-</td><td>6-bit RGB interface (262K colors)</td><td>VSYNC,HSYNC,DE, DOTCLK,D[5:0]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>18-bit RGB interface (262K colors)</td><td rowspan="3">SYNC Mode In SYNC mode, DE signal is ignored; blanking porch is determined by B5h command</td><td>VSYNC,HSYNC,DOTCLK, D[17:0]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>16-bit RGB interface (65K colors)</td><td>VSYNC,HSYNC,DOTCLK, D[17:13] & D[11:1]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td colspan="3">-</td><td>6-bit RGB interface (262K colors)</td><td>VSYNC,HSYNC,DOTCLK, D[5:0]</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="14"></td></tr>
</table>

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	RCM[1:0]	VSPL	HSPL	DPL	EPL
Power On Sequence	2'b00	1'b0	1'b0	1'b0	1'b1
SW Reset	2'b00	1'b0	1'b0	1'b0	1'b1
HW Reset	2'b00	1'b0	1'b0	1'b0	1'b1

HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31
11111	32
HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31

11111	32
HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31
11111	32
HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31
11111	32

6.3.2. Blanking Porch Control (B5h)

B5h	Blanking Porch Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
1st Parameter	1	1	↑	XX	0	0	0	0	VFP [3:0]				08
2nd Parameter	1	1	↑	XX	0	VBP [6:0]							02
3rd Parameter	1	1	↑	XX	0	0	0	HBP [4:0]					14

Description

Note: The Third parameter must write,but it is not valid.

VFP [6:0] / VBP [6:0]: The VFP [6:0] and VBP [6:0] bits specify the line number of vertical front and back porch period respectively.

VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch	VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch
0000000	Setting inhibited	1000000	64
0000001	Setting inhibited	1000001	65
0000010	2	1000010	66
0000011	3	1000011	67
0000100	4	1000100	68
0000101	5	1000101	69
: :	: :	: :	: :
0111101	61	1111101	125
0111110	62	1111110	109.5
0111111	63	1111111	127

Note: VFP + VBP ≦ 254 HSYNC signals

HBP [4:0]: HBP [4:0] bits specify the line number of horizontal back porch period respectively.

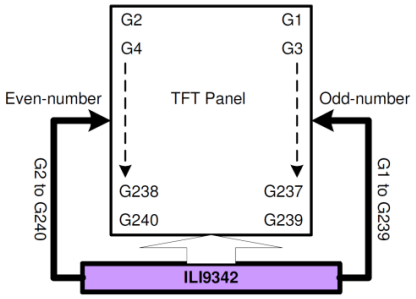
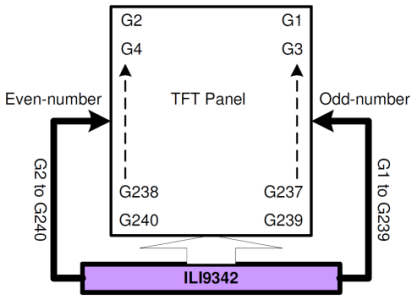
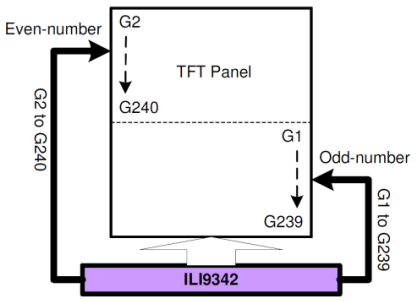
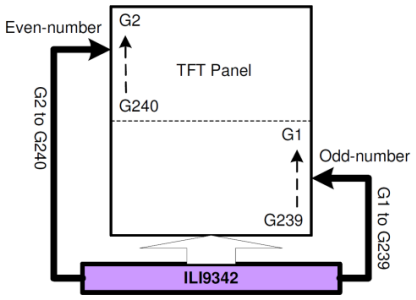
HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31

<table>
<tr><td></td><td>
<table>
<tr><td>11111</td><td>32</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>VFP [6:0]</th><th>VBP [6:0]</th><th>HBP [4:0]</th></tr>
<tr><td>Power On Sequence</td><td>7’h08</td><td>7’h02</td><td>5’h14</td></tr>
<tr><td>SW Reset</td><td>7’h08</td><td>7’h02</td><td>5’h14</td></tr>
<tr><td>HW Reset</td><td>7’h08</td><td>7’h02</td><td>5’h14</td></tr>
</table>
</td></tr>
</table>

6.3.3. Display Function Control (B6h)

<table>
<tr><td>B6h</td><td colspan="13">Display Function Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>B6h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>XX</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>GS</td><td>SS</td><td>SM</td><td colspan="4">X</td><td>00</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td colspan="6">NL [5:0]</td><td>27</td></tr>
<tr><td>Description</td><td colspan="13">
note:the first parameter must write,but it is not valid.
SS: Select the shift direction of outputs from the source driver.
<table>
<tr><th>SS</th><th>Sourc Output Scan Direction</th></tr>
<tr><td>0</td><td>S1 → S960</td></tr>
<tr><td>1</td><td>S960 → S1</td></tr>
</table>
In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, and B dots to the source driver pins.
To assign R, G, B dots to the source driver pins from S1 to S960, set SS = 0.
To assign R, G, B dots to the source driver pins from S960 to S1, set SS = 1.

GS: Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.
<table>
<tr><th>GS</th><th>Gate Output Scan Direction</th></tr>
<tr><td>0</td><td>G1→G240</td></tr>
<tr><td>1</td><td>G240→G1</td></tr>
</table>
SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module
</td></tr>
</table>

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1→G2→G3→G4→ …… ….→G237→G238→G239→G240
0	1		G240→G239->G238→G237→…… …. →G4→G3→G2→G1
1	0		G1→G3→……..→G237→G239→ G2→G4→……→G238→G240
1	1		G240→G238→……..→G4→G2→ G239→G237→……→G3→G1

NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected
by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary
for the size of the liquid crystal panel.

NL [5:0]						LCD Drive Line
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	16 lines
0	0	0	0	1	0	24 lines
0	0	0	0	1	1	32 lines

NL [5:0]						LCD Drive Line
0	1	0	1	0	1	176 lines
0	1	0	1	1	0	184 lines
0	1	0	1	1	1	192 lines
0	1	1	0	0	0	200 lines

		0	0	0	1	0	0	40 lines		0	1	1	0	0	1	208 lines		
		0	0	0	1	0	1	48 lines		0	1	1	0	1	0	216 lines		
		0	0	0	1	1	0	56 lines		0	1	1	0	1	1	224 lines		
		0	0	0	1	1	1	64 lines		0	1	1	1	0	0	232 lines		
		0	0	1	0	0	0	72 lines		0	1	1	1	0	1	240 lines		
		0	0	1	0	0	1	80 lines		Others						Setting prohibited		
		0	0	1	0	1	0	88 lines										
		0	0	1	0	1	1	96 lines										
		0	0	1	1	0	0	104 lines										
		0	0	1	1	0	1	112 lines										
		0	0	1	1	1	0	120 lines										
		0	0	1	1	1	1	128 lines										
		0	1	0	0	0	0	136 lines										
		0	1	0	0	0	1	144 lines										
		0	1	0	0	1	0	152 lines										
		0	1	0	0	1	1	160 lines										

Restriction	EXTC should be high to enable this command

Register Availability

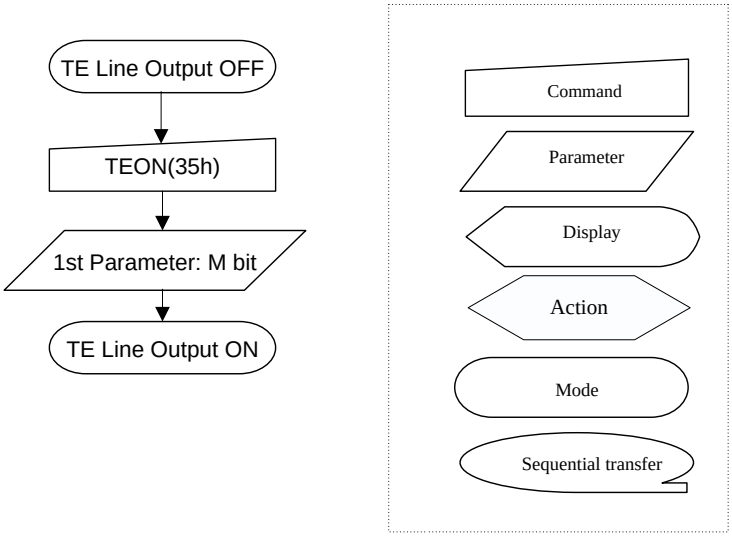
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	-	GS	SS	SM	NL[5:0]
Power On Sequence	-	1’b0	1’b0	1’b0	6’h1D
HW Reset	-	1’b0	1’b0	1’b0	6’h1D

6.3.4. Tearing Effect Control (BAh)

<table>
<tr><td>35h</td><td colspan="13">Tearing Effect Width Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>BAh</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>te_pol</td><td colspan="7">te_width[6:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">te_pol is used to adjust the Tearing Effect output signal pulse polarity.
<table><tr><td>te_pol</td><td>Tearing Effect polarity</td></tr><tr><td>0</td><td>Positive pulse</td></tr><tr><td>1</td><td>negative pulse</td></tr></table>te_width[6:0] is used to adjust the Tearing Effect output signal pulse width with display lines in unit
<table><tr><td>te_width[6:0]</td><td>Tearing Effect width(display line time)</td></tr><tr><td>0</td><td>1line time</td></tr><tr><td>1</td><td>2line time</td></tr><tr><td>…</td><td>…</td></tr><tr><td>N</td><td>N+1 line time</td></tr><tr><td>…</td><td>…</td></tr><tr><td>7f</td><td>128 line time</td></tr></table>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>0x00</td></tr><tr><td>SW Reset</td><td>0x00</td></tr><tr><td>HW Reset</td><td>0x00</td></tr></table></td></tr>
</table>

Flow Chart	

TE Line Output OFF
TEON(35h)
1st Parameter: M bit
TE Line Output ON
Command
Parameter
Display
Action
Mode
Sequential transfer

6.3.5. Interface Control (F6h)

<table>
<tr><td>F6h</td><td colspan="13">Interface Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>F6h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>1</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td colspan="2">DM [1:0]</td><td>RM</td><td>RIM</td><td>C0</td></tr>
<tr><td>Description</td><td colspan="13">
DM [1:0]: Select the display operation mode.
<table>
<tr><th>DM[1]</th><th>DM[0]</th><th>Display Operation Mode</th></tr>
<tr><td>0</td><td>0</td><td>Internal clock operation</td></tr>
<tr><td>0</td><td>1</td><td>RGB Interface Mode</td></tr>
<tr><td>1</td><td>0</td><td>VSYNC interface Mode</td></tr>
<tr><td>1</td><td>1</td><td>Setting disabled</td></tr>
</table>
RM: Select the interface to access the GRAM.
Set RM to “1” when writing display data by the RGB interface.
<table>
<tr><th>RM</th><th>Interface for RAM Access</th></tr>
<tr><td>0</td><td>System interface/VSYNC interface</td></tr>
<tr><td>1</td><td>RGB interface</td></tr>
</table>
RIM: Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.
<table>
<tr><th>RIM</th><th>COLMOD [6:4]</th><th>RGB Interface Mode</th></tr>
<tr><td rowspan="2">0</td><td>110 (262K color)</td><td>18- bit RGB interface (1 transfer/pixel)</td></tr>
<tr><td>101 (65K color)</td><td>16- bit RGB interface (1 transfer/pixel)</td></tr>
<tr><td>1</td><td>(262K color)</td><td>6- bit RGB interface (3 transfer/pixel)</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="13">EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr>
<tr><th>MDT[1:0]</th><th>DM [1:0]</th><th>RM</th><th>RIM</th></tr>
<tr><td>Power On Sequence</td><td>2’b00</td><td>2’b00</td><td>1’b0</td><td>1’b0</td></tr>
<tr><td>SW Reset</td><td>2’b00</td><td>2’b00</td><td>1’b0</td><td>1’b0</td></tr>
<tr><td>HW Reset</td><td>2’b00</td><td>2’b00</td><td>1’b0</td><td>1’b0</td></tr>
</table>
</td></tr>
</table>

6.4. Description of Level 3 Command

6.4.1. Frame Rate (E8h)

<table>
<tr><td>E8h</td><td colspan="13">Frame Rate</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>E8h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="4">DINV[3:0]</td><td colspan="4">RTN1[3:0]</td><td>11</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">RTN2[7:0]</td><td>40</td></tr>
<tr><td>Description</td><td colspan="13">
DINV[3:0] : Set display inversion mode
<table>
<tr><th>DINV[3:0]</th><th>Inversion</th></tr>
<tr><td>0</td><td>column inversion</td></tr>
<tr><td>1</td><td>1 dot inversion</td></tr>
<tr><td>2</td><td>2 dot inversion</td></tr>
<tr><td>3</td><td>4 dot inversion</td></tr>
<tr><td>4</td><td>8 dot inversion</td></tr>
</table>
RTN1[3:0]/RTN2[7:0] :Set the frame rate when the internal resistor is used for oscillator circuit.
Frame Rate = 58.51KHz/(136*(RTN1+4)+RTN2)）
note: set rtn1 =1
<table>
<tr><th>rtn2[7:0]</th><th>TE(Hz)</th><th>rtn2[7:0]</th><th>TE(Hz)</th><th>rtn2[7:0]</th><th>TE(Hz)</th><th>rtn2[7:0]</th><th>TE Hz)</th></tr>
<tr><td>8'd00</td><td>86.04</td><td>8'd10</td><td>84.07</td><td>8'd20</td><td>82.18</td><td>8'd30</td><td>80.37</td></tr>
<tr><td>8'd01</td><td>85.92</td><td>8'd11</td><td>83.95</td><td>8'd21</td><td>82.06</td><td>8'd31</td><td>80.26</td></tr>
<tr><td>8'd02</td><td>85.79</td><td>8'd12</td><td>83.83</td><td>8'd22</td><td>81.95</td><td>8'd32</td><td>80.15</td></tr>
<tr><td>8'd03</td><td>85.67</td><td>8'd13</td><td>83.71</td><td>8'd23</td><td>81.83</td><td>8'd33</td><td>80.04</td></tr>
<tr><td>8'd04</td><td>85.54</td><td>8'd14</td><td>83.59</td><td>8'd24</td><td>81.72</td><td>8'd34</td><td>79.93</td></tr>
<tr><td>8'd05</td><td>85.42</td><td>8'd15</td><td>83.47</td><td>8'd25</td><td>81.6</td><td>8'd35</td><td>79.82</td></tr>
<tr><td>8'd06</td><td>85.29</td><td>8'd16</td><td>83.35</td><td>8'd26</td><td>81.49</td><td>8'd36</td><td>79.71</td></tr>
<tr><td>8'd07</td><td>85.17</td><td>8'd17</td><td>83.23</td><td>8'd27</td><td>81.38</td><td>8'd37</td><td>79.61</td></tr>
<tr><td>8'd08</td><td>85.04</td><td>8'd18</td><td>83.11</td><td>8'd28</td><td>81.26</td><td>8'd38</td><td>79.5</td></tr>
<tr><td>8'd09</td><td>84.92</td><td>8'd19</td><td>82.99</td><td>8'd29</td><td>81.15</td><td>8'd39</td><td>79.39</td></tr>
<tr><td>8'd0A</td><td>84.8</td><td>8'd1A</td><td>82.88</td><td>8'd2A</td><td>81.04</td><td>8'd3A</td><td>79.28</td></tr>
<tr><td>8'd0B</td><td>84.67</td><td>8'd1B</td><td>82.76</td><td>8'd2B</td><td>80.93</td><td>8'd3B</td><td>79.17</td></tr>
<tr><td>8'd0C</td><td>84.55</td><td>8'd1C</td><td>82.64</td><td>8'd2C</td><td>80.81</td><td>8'd3C</td><td>79.07</td></tr>
<tr><td>8'd0D</td><td>84.43</td><td>8'd1D</td><td>82.52</td><td>8'd2D</td><td>80.7</td><td>8'd3D</td><td>78.96</td></tr>
<tr><td>8'd0E</td><td>84.31</td><td>8'd1E</td><td>82.41</td><td>8'd2E</td><td>80.59</td><td>8'd3E</td><td>78.85</td></tr>
<tr><td>8'd0F</td><td>84.19</td><td>8'd1F</td><td>82.29</td><td>8'd2F</td><td>80.48</td><td>8'd3F</td><td>78.75</td></tr>
</table>
</td></tr>
</table>

rtn2[7:0]	TE(Hz)	rtn2[7:0]	TE(Hz)	rtn2[7:0]	TE(Hz)	rtn2[7:0]	TE(Hz)
8'd40	78.64	8'd50	76.99	8'd60	75.4	8'd70	73.88
8'd41	78.54	8'd51	76.89	8'd61	75.3	8'd71	73.78
8'd42	78.43	8'd52	76.78	8'd62	75.21	8'd72	73.69
8'd44	78.33	8'd55	76.68	8'd66	75.11	8'd77	73.6
8'd44	78.22	8'd54	76.58	8'd64	75.01	8'd74	73.51
8'd45	78.12	8'd55	76.48	8'd65	74.92	8'd75	73.41
8'd46	78.01	8'd56	76.38	8'd66	74.82	8'd76	73.32
8'd47	77.91	8'd57	76.28	8'd67	74.73	8'd77	73.23
8'd48	77.81	8'd58	76.18	8'd68	74.63	8'd78	73.14
8'd49	77.7	8'd59	76.09	8'd69	74.54	8'd79	73.05
8'd4A	77.6	8'd5A	75.99	8'd6A	74.44	8'd7A	72.96
8'd4B	77.5	8'd5B	75.89	8'd6B	74.35	8'd7B	72.86
8'd4C	77.39	8'd5C	75.79	8'd6C	74.25	8'd7C	72.77
8'd4D	77.29	8'd5D	75.69	8'd6D	74.16	8'd7D	72.68
8'd4E	77.19	8'd5E	75.59	8'd6E	74.06	8'd7E	72.59
8'd4F	77.09	8'd5F	75.5	8'd6F	73.97	8'd7F	72.5
rtn2[7:0]	TE(Hz)	rtn2[7:0]	TE(Hz)	rtn2[7:0]	TE(Hz)	rtn2[7:0]	TE(Hz)
8'd80	72.41	8'd84	72.06				
8'd81	72.32	8'd85	71.97				
8'd82	72.23	8'd86	71.88				
8'd83	72.15	8'd87	71.79				

note: set rtn2=0x40

rtn1[3:0]	TE(Hz)	rtn1[3:0]	TE(Hz)	rtn1[3:0]	TE(Hz)	rtn1[3:0]	TE(Hz)
8'd00	96.23	8'd04	50.79	8'd08	34.5	8'd0C	26.12
8'd01	78.64	8'd05	45.43	8'd09	31.94	8'd0D	24.63
8'd02	66.49	8'd06	41.09	8'd0A	29.73	8'd0E	23.29
8'd03	57.59	8'd07	37.51	8'd0B	27.81	8'd0F	22.1

Restriction	Inter_command should be set high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	DINV[3:0]	RTN1[3:0]	RTN2[7:0]
Power On Sequence	4’h1	4’h1	8’h40
SW Reset	4’h1	4’h1	8’h40
HW Reset	4’h1	4’h1	8’h40

6.4.2. SPI 2DATA control(E9h)

<table>
<tr><td>E9h</td><td colspan="12">SPI 2DATA control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>E9h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>2data_en</td><td colspan="3">2data_mdt[2:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="12">2DATA_EN: Set 2_data_line mode in 3-wire/4-wire SPI.
2DATA_MDT[2:0] Set pixel data format in 2_data_line mode.

<table><tr><th>2DATA_MDT[2:0]</th><th>Data Format</th></tr><tr><td>000</td><td>65K color 1pixle/transition</td></tr><tr><td>001</td><td>262K color 1pixle/transition</td></tr><tr><td>010</td><td>262K color 2/3pixle/transition</td></tr><tr><td>100</td><td>4M color 1pixle/transition</td></tr><tr><td>110</td><td>4M color 2/3pixle/transition</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="12">Inter command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>2DATA_EN</th><th>2DATA_MDT[2:0]</th></tr><tr><td>Power On Sequence</td><td>1’b0</td><td>3’b000</td></tr><tr><td>SW Reset</td><td>1’b0</td><td>3’b000</td></tr><tr><td>HW Reset</td><td>1’b0</td><td>3’b000</td></tr></table></td></tr>
</table>

6.4.3. Power Control 1 (C1h)

<table>
<tr><td>C1h</td><td colspan="13">Power Control 1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>C1h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>VCIRE</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">VCIRE: Select the external reference voltage Vci or internal reference voltage VCIR.<table><tr><td>VCIRE=0</td><td>Internal reference voltage 2.5V (default)</td></tr><tr><td>VCIRE =1</td><td>External reference voltage Vci</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>VCIRE</th></tr><tr><td>Power On Sequence</td><td>1’b0</td></tr><tr><td>SW Reset</td><td>1’b0</td></tr><tr><td>HW Reset</td><td>1’b0</td></tr></table></td></tr>
</table>

6.4.4. Power Control 2 (C3h)

<table>
<tr><td>C3h</td><td colspan="13">Power Control 2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>C3h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="7">vreg1_vbp_d[6:0]</td><td>3C</td></tr>
<tr><td>Description</td><td colspan="13">Set the voltage level value to output the VREG1A and VREG1B OUT level, which is a reference level for the grayscale voltage level.(Table is valid when vrh=0x28)
VREG1A=(vrh+vbp_d)*0.02+4
VREG1B=vbp_d*0.02+0.3
<table>
<tr><th>vreg1_vbp_d[6:0]</th><th>VREG1A/V</th><th>VREG1B/V</th></tr>
<tr><td>7'h00</td><td>4.8</td><td>0.3</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>N</td><td>(N+40)*0.02+4</td><td>N*0.02+0.3</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>7’h3C</td><td>6</td><td>1.5</td></tr>
<tr><td>…</td><td>…</td><td></td></tr>
<tr><td>7’h7F</td><td>7.34</td><td>2.84</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>vreg1_vbp_d[6:0]</th></tr>
<tr><td>Power On Sequence</td><td>7h3c</td></tr>
<tr><td>SW Reset</td><td>7h3c</td></tr>
<tr><td>HW Reset</td><td>7h3c</td></tr>
</table></td></tr>
</table>

6.4.5. Power Control 3 (C4h)

<table>
<tr><td>C4h</td><td colspan="12">Power Control 3</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>C4h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="7">vreg1_vbn_d[6:0]</td><td>3C</td></tr>
<tr><td>Description</td><td colspan="13">Set the voltage level value to output the VREG2A OUT level, which is a reference level for the grayscale voltage level(Table is valid when vrh=0x28)
VREG2A=(vbn_d-vrh)*0.02-3.4
VREG2B=vbn_d*0.02+0.3
<table>
<tr><th>vreg1_vbn_d[6:0]</th><th>VREG2A/V</th><th>VREG2B/V</th></tr>
<tr><td>7'h00</td><td>-4.2</td><td>0.3</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>N</td><td>N*0.02-4.2</td><td>N*0.02+0.3</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>7’h3C</td><td>-3</td><td>1.5</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>7’h7F</td><td>-1.66</td><td>2.84</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>vreg1_vbn_d[6:0]</th></tr>
<tr><td>Power On Sequence</td><td>7’h3C</td></tr>
<tr><td>SW Reset</td><td>7’h3C</td></tr>
<tr><td>HW Reset</td><td>7’h3C</td></tr>
</table></td></tr>
</table>

6.4.6. Power Control 4 (C9h)

<table>
<tr><td>C9h</td><td colspan="13">Power Control 4</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>C9h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td colspan="6">vrh[5:0]</td><td>28</td></tr>
<tr><td>Description</td><td colspan="13">Set the voltage level value to output the VREG1A OUT level, which is a reference level for the grayscale voltage level. (Table is valid when vbp_d=0x3C and vbn_d=0x3C)
VREG1A=(vrh+vbp_d)*0.02+4
VREG2A=(vbn_d-vrh)*0.02-3.4
<table>
<tr><th>vrh[5:0]</th><th>VREG1A/V</th><th>VREG2A/V</th></tr>
<tr><td>6'h00</td><td>5.2</td><td>-2.2</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>N</td><td>(N+60)*0.02+4</td><td>(100-N)*0.02-4.2</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>6’h28</td><td>6</td><td>-3</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>6’h3F</td><td>6.46</td><td>-3.46</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>vrh[5:0]</th></tr>
<tr><td>Power On Sequence</td><td>6’h28</td></tr>
<tr><td>SW Reset</td><td>6’h28</td></tr>
<tr><td>HW Reset</td><td>6’h28</td></tr>
</table></td></tr>
</table>

6.4.7. Power Control 6 (ECh)

<table>
<tr><td>ECh</td><td colspan="13">Power Control 6</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>ECh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="4">avdd_clk_ad[2:0]</td><td colspan="3">avee_clk_ad[2:0]</td><td>33</td></tr>
<tr><td>2st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td></td><td></td><td></td><td colspan="3">vcl_clk_ad[2:0]</td><td>02</td></tr>
<tr><td>3st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="4">vgh_clk_ad[3:0]</td><td colspan="4">vgl_clk_ad[3:0]</td><td>88</td></tr>
<tr><td>Description</td><td colspan="13">Set the ChargePump frequence output(Fosc is equal to RC oscillator)
<table>
<tr><td colspan="2">vcl_clk_ad[2:0]</td><td colspan="2">vcl_clk(Mhz)</td><td>avee_clk_ad[2:0]</td><td>avee_clk(Mhz)</td><td>avdd_clk_ad[2:0]</td><td>avdd_clk(Mhz)</td></tr>
<tr><td colspan="2">3'h00</td><td colspan="2">Fosc*(3/4)</td><td>3'h00</td><td>Fosc*(2/4)</td><td>3'h00</td><td>Fosc*(2/4)</td></tr>
<tr><td colspan="2">3'h01</td><td colspan="2">Fosc*(4/4)</td><td>3'h01</td><td>Fosc*(3/4)</td><td>3'h01</td><td>Fosc*(3/4)</td></tr>
<tr><td colspan="2">3'h02</td><td colspan="2">Fosc*(5/4)</td><td>3'h02</td><td>Fosc*(4/4)</td><td>3'h02</td><td>Fosc*(4/4)</td></tr>
<tr><td colspan="2">3'h03</td><td colspan="2">Fosc*(6/4)</td><td>3'h03</td><td>Fosc*(5/4)</td><td>3'h03</td><td>Fosc*(5/4)</td></tr>
<tr><td colspan="2">3'h04</td><td colspan="2">Fosc*(7/4)</td><td>3'h04</td><td>Fosc*(6/4)</td><td>3'h04</td><td>Fosc*(6/4)</td></tr>
<tr><td colspan="2">3'h05</td><td colspan="2">Fosc*(8/4)</td><td>3'h05</td><td>Fosc*(7/4)</td><td>3'h05</td><td>Fosc*(7/4)</td></tr>
<tr><td colspan="2">3'h06</td><td colspan="2">Fosc*(9/4)</td><td>3'h06</td><td>Fosc*(8/4)</td><td>3'h06</td><td>Fosc*(8/4)</td></tr>
<tr><td colspan="2">3'h07</td><td colspan="2">Fosc*(10/4)</td><td>3'h07</td><td>Fosc*(9/4)</td><td>3'h07</td><td>Fosc*(9/4)</td></tr>
<tr><td>vgh_clk_ad[3:0]</td><td>vgh_clk(Mhz)</td><td>vgh_clk_ad[3:0]</td><td>vgh_clk(Mhz)</td><td>vgl_clk_ad[3:0]</td><td>vgl_clk(Mhz)</td><td>vgl_clk_ad[3:0]</td><td>vgl_clk(Mhz)</td></tr>
<tr><td>4'h00</td><td>Fosc*(5/4)</td><td>4'h08</td><td>Fosc*(20/4)</td><td>4'h00</td><td>Fosc*(5/4)</td><td>4'h08</td><td>Fosc*(20/4)</td></tr>
<tr><td>4'h01</td><td>Fosc*(6/4)</td><td>4'h09</td><td>Fosc*(22/4)</td><td>4'h01</td><td>Fosc*(6/4)</td><td>4'h09</td><td>Fosc*(22/4)</td></tr>
<tr><td>4'h02</td><td>Fosc*(8/4)</td><td>4'h0a</td><td>Fosc*(24/4)</td><td>4'h02</td><td>Fosc*(8/4)</td><td>4'h0a</td><td>Fosc*(24/4)</td></tr>
<tr><td>4'h03</td><td>Fosc*(10/4)</td><td>4'h0b</td><td>Fosc*(26/4)</td><td>4'h03</td><td>Fosc*(10/4)</td><td>4'h0b</td><td>Fosc*(26/4)</td></tr>
<tr><td>4'h04</td><td>Fosc*(12/4)</td><td>4'h0c</td><td>Fosc*(28/4)</td><td>4'h04</td><td>Fosc*(12/4)</td><td>4'h0c</td><td>Fosc*(28/4)</td></tr>
<tr><td>4'h05</td><td>Fosc*(14/4)</td><td>4'h0d</td><td>Fosc*(30/4)</td><td>4'h05</td><td>Fosc*(14/4)</td><td>4'h0d</td><td>Fosc*(30/4)</td></tr>
<tr><td>4'h06</td><td>Fosc*(16/4)</td><td>4'h0e</td><td>Fosc*(40/4)</td><td>4'h06</td><td>Fosc*(16/4)</td><td>4'h0e</td><td>Fosc*(40/4)</td></tr>
<tr><td>4'h07</td><td>Fosc*(18/4)</td><td>4'h0f</td><td>Fosc*(50/4)</td><td>4'h07</td><td>Fosc*(18/4)</td><td>4'h0f</td><td>Fosc*(50/4)</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
</table>

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

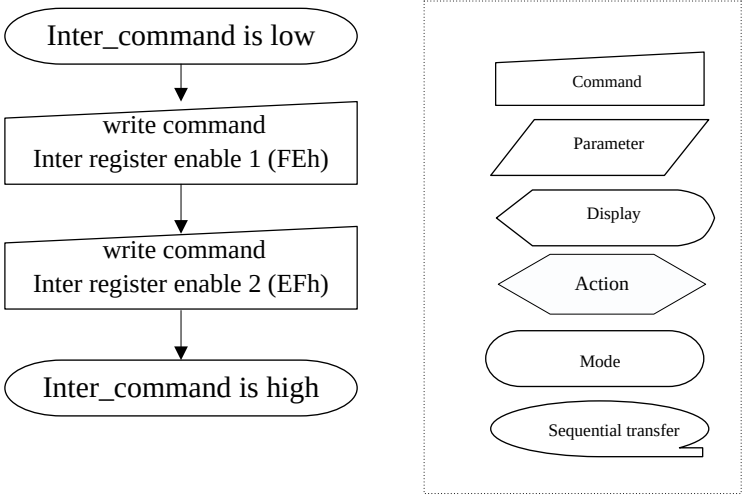
Default

Status	Default Value				
	avdd_clk_ad[2:0]	avee_clk_ad[2:0]	vcl_clk_ad[2:0]	vgh_clk_ad[3:0]	vgl_clk_ad[3:0]
Power On Sequence	3’h3	3’h3	3’h2	4’h8	4’h8
SW Reset	3’h3	3’h3	3’h2	4’h8	4’h8
HW Reset	3’h3	3’h3	3’h2	4’h8	4’h8

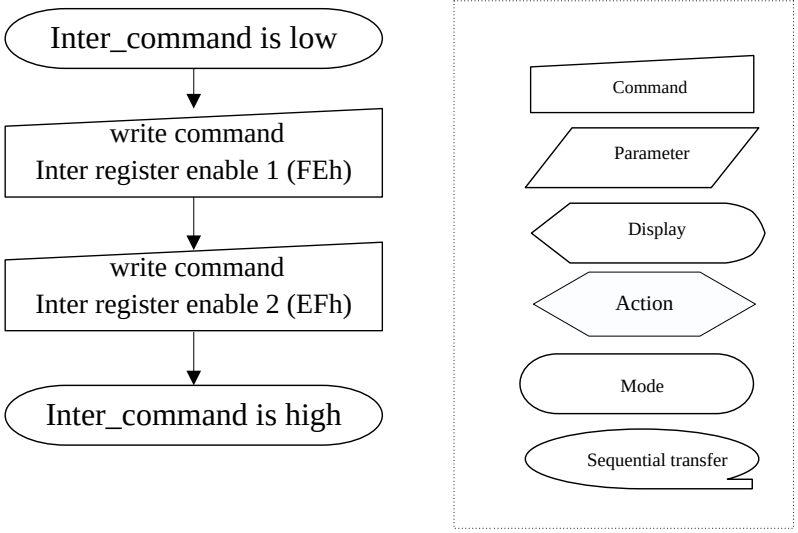
6.4.8. Power Control 7(A7h)

<table>
<tr><td>A7h</td><td colspan="13">Power Control 7</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>A7h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>0</td><td colspan="4">vdd_ad[3:0]</td><td>48</td></tr>
<tr><td>Description</td><td colspan="13">vdd_ad: Set the voltage level value to output the VCORE level,
<table>
<tr><th>vdd_ad[3:0]</th><th>VCORE(V)</th><th>vdd_ad[3:0]</th><th>VCORE(V)</th></tr>
<tr><td>4'h00</td><td>1.483</td><td>4'h08</td><td>1.994</td></tr>
<tr><td>4'h01</td><td>1.545</td><td>4'h09</td><td>2.109</td></tr>
<tr><td>4'h02</td><td>1.590</td><td>4'h0a</td><td>2.193</td></tr>
<tr><td>4'h03</td><td>1.638</td><td>4'h0b</td><td>2.286</td></tr>
<tr><td>4'h04</td><td>1.714</td><td>4'h0c</td><td>2.385</td></tr>
<tr><td>4'h05</td><td>1.279</td><td>4'h0d</td><td>1.713</td></tr>
<tr><td>4'h06</td><td>1.859</td><td>4'h0e</td><td>1.713</td></tr>
<tr><td>4'h07</td><td>1.925</td><td>4'h0f</td><td>1.713</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>vdd_ad[3:0]</th></tr>
<tr><td>Power On Sequence</td><td>4’b48</td></tr>
<tr><td>SW Reset</td><td>4’b48</td></tr>
<tr><td>HW Reset</td><td>4’b48</td></tr>
</table></td></tr>
</table>

6.4.9. Inter Register Enable1(FEh)

<table>
<tr><td>FEh</td><td colspan="13">Inter register enable 1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>FEh</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used for Inter_command controlling.
To set Inter_command high ,you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously.
Once Inter_command is set high, only hardware or software reset can turn it to low.
 
</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13"></td></tr>
</table>

6.4.10. Inter Register Enable2(EFh)

<table>
<tr><td>EFh</td><td colspan="13">Inter register enable 2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>EFh</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used for Inter_command controlling.
To set Inter_command high ,you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously.
Once Inter_command is set high, only hardware or software reset can turn it to low.
 
</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"></td></tr>
</table>

6.4.11. SET_GAMMA1 (F0h)

<table>
<tr><td>F0h</td><td colspan="13">SET_GAMMA1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>F0h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>dig2gam_dig2j0_n[1:0]</td><td colspan="7">dig2gam_vr1_n[5:0]</td><td>80</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>dig2gam_dig2j1_n[1:0]</td><td colspan="7">dig2gam_vr2_n[5:0]</td><td>03</td></tr>
<tr><td>3st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td></td><td colspan="4">dig2gam_vr4_n[4:0]</td><td>08</td></tr>
<tr><td>4nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td></td><td colspan="4">dig2gam_vr6_n[4:0]</td><td>06</td></tr>
<tr><td>5st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="4">dig2gam_vr0_n[3:0]</td><td colspan="4">dig2gam_vr13_n[3:0]</td><td>05</td></tr>
<tr><td>6nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td colspan="8">dig2gam_vr20_n[6:0]</td><td>2B</td></tr>
<tr><td>Description</td><td colspan="13">dig2gam_dig2j0_n[1:0]: γ gradient adjustment register for negative polarity
dig2gam_dig2j1_n[1:0]: γ gradient adjustment register for negative polarity
dig2gam_vr0_n[3:0]: γ gradient adjustment register for negative polarity
dig2gam_vr1_n[5:0]: γ gradient adjustment register for negative polarity
dig2gam_vr2_n[5:0]: γ gradient adjustment register for negative polarity
dig2gam_vr4_n[4:0]: γ gradient adjustment register for negative polarity
dig2gam_vr6_n[4:0]: γ gradient adjustment register for negative polarity
dig2gam_vr13_n[3:0]: γ gradient adjustment register for negative polarity
dig2gam_vr20_n[6:0]: γ gradient adjustment register for negative polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Id e Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

Default		Status	Default Value				
			dig2gam_dig2j0_n[1:0]	dig2gam_dig2j1_n[1:0]	dig2gam_vr0_n[3:0]	dig2gam_vr1_n[5:0]	dig2gam_vr2_n[5:0]	dig2gam_vr4_n[4:0]
		Power On Sequence	2'h02	2'h00	4'h00	6'h00	6'h03	5'h08
		SW Reset	2'h02	2'h00	4'h00	6'h00	6'h03	5'h08
		HW Reset	2'h02	2'h00	4'h00	6'h00	6'h03	5'h08
Default		Status	Default Value				
			dig2gam_vr6_n[4:0]	dig2gam_vr13_n[3:0]	dig2gam_vr20_n[6:0]			
		Power On Sequence	5'h06	4'h05	7'h2b			
		SW Reset	5'h06	4'h05	7'h2b			
		HW Reset	5'h06	4'h05	7'h2b			

6.4.12. SET_GAMMA2 (F1h)

<table>
<tr><td>F1h</td><td colspan="13">SET_GAMMA2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>F1h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td colspan="7">dig2gam_vr43_n[6:0]</td><td>41</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="3">dig2gam_vr27_n[2:0]</td><td colspan="5">dig2gam_vr57_n[4:0]</td><td>97</td></tr>
<tr><td>3st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="3">dig2gam_vr36_n[2:0]</td><td colspan="5">dig2gam_vr59_n[4:0]</td><td>98</td></tr>
<tr><td>4nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td colspan="6">dig2gam_vr61_n[5:0]</td><td>13</td></tr>
<tr><td>5st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td colspan="6">dig2gam_vr62_n[5:0]</td><td>17</td></tr>
<tr><td>6nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="4">dig2gam_vr50_n[3:0]</td><td colspan="4">dig2gam_vr63_n[3:0]</td><td>CD</td></tr>
<tr><td>Description</td><td colspan="13">dig2gam_vr43_p[6:0]: γ gradient adjustment register for negative polarity
dig2gam_vr27_p[2:0]: γ gradient adjustment register for negative polarity
dig2gam_vr57_p[4:0]: γ gradient adjustment register for negative polarity
dig2gam_vr59_p[4:0]: γ gradient adjustment register for negative polarity
dig2gam_vr36_p[2:0]: γ gradient adjustment register for negative polarity
dig2gam_vr61_p[5:0]: γ gradient adjustment register for negative polarity
dig2gam_vr62_p[5:0]: γ gradient adjustment register for negative polarity
dig2gam_vr50_p[3:0]: γ gradient adjustment register for negative polarity
dig2gam_vr63_p[3:0]: γ gradient adjustment register for negative polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mo e On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

Default

Status	Default Value					
	dig2gam_vr43_p[6:0]	dig2gam_vr27_p[2:0]	dig2gam_vr57_p[4:0]	dig2gam_vr59_p[4:0]	dig2gam_vr36_p[2:0]	dig2gam_vr61_p[5:0]
Power On Sequence	7'h41	3'h04	5'h17	5'h18	3'h04	6'h13
SW Reset	7'h41	3'h04	5'h17	5'h18	3'h04	6'h13
HW Reset	7'h41	3'h04	5'h17	5'h18	3'h04	6'h13

Default

Status	Default Value					
	dig2gam_vr62_p[5:0]	dig2gam_vr50_p[3:0]	dig2gam_vr63_p[3:0]			
Power On Sequence	6'h17	4'h0C	4'h0D			
SW Reset	6'h17	4'h0C	4'h0D			
HW Reset	6'h17	4'h0C	4'h0D			

6.4.13. SET_GAMMA3 (F2h)

<table>
<tr><td>F2h</td><td colspan="13">SET_GAMMA3</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>F2h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>dig2gam_dig2j0_p[1:0]</td><td colspan="7">dig2gam_vr1_p[5:0]</td><td>40</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>dig2gam_dig2j1_p[1:0]</td><td colspan="7">dig2gam_vr2_p[5:0]</td><td>03</td></tr>
<tr><td>3st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td></td><td colspan="5">dig2gam_vr4_p[4:0]</td><td>08</td></tr>
<tr><td>4nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td></td><td colspan="5">dig2gam_vr6_p[4:0]</td><td>0B</td></tr>
<tr><td>5st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="4">dig2gam_vr0_p[3:0]</td><td colspan="4">dig2gam_vr13_p[3:0]</td><td>08</td></tr>
<tr><td>6nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td colspan="8">dig2gam_vr20_p[6:0]</td><td>2E</td></tr>
<tr><td>Description</td><td colspan="13">dig2gam_dig2j0_p[1:0]: γ gradient adjustment register for positive polarity
dig2gam_dig2j1_p[1:0]: γ gradient adjustment register for positive polarity
dig2gam_vr1_p[5:0]: γ gradient adjustment register for positive polarity
dig2gam_vr2_p[5:0]: γ gradient adjustment register for positive polarity
dig2gam_vr4_p[4:0]: γ gradient adjustment register for positive polarity
dig2gam_vr6_p[4:0]: γ gradient adjustment register for positive polarity
dig2gam_vr0_p[3:0]: γ gradient adjustment register for positive polarity
dig2gam_vr13_p[3:0]: γ gradient adjustment register for positive polarity
dig2gam_vr20_p[6:0]: γ gradient adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle M de Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

Default

Status	Default Value					
	dig2gam_dig2j0_p[1:0]	dig2gam_dig2j1_p[1:0]	dig2gam_vr1_p[5:0]	dig2gam_vr2_p[5:0]	dig2gam_vr4_p[4:0]	dig2gam_vr6_p[4:0]
Power On Sequence	2'h01	2'h00	6'h00	6'h03	5'h08	5'h0B
SW Reset	2'h01	2'h00	6'h00	6'h03	5'h08	5'h0B
HW Reset	2'h01	2'h00	6'h00	6'h03	5'h08	5'h0B

Default

Status	Default Value					
	dig2gam_vr0_p[3:0]	dig2gam_vr13_p[3:0]	dig2gam_vr20_p[6:0]			
Power On Sequence	4'h00	4'h08	7'h2E			
SW Reset	4'h00	4'h08	7'h2E			
HW Reset	4'h00	4'h08	7'h2E			

6.4.14. SET_GAMMA4 (F3h)

<table>
<tr><td>F3h</td><td colspan="13">SET_GAMMA4</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>F3h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td colspan="7">dig2gam_vr43_p[6:0]</td><td>3F</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="3">dig2gam_vr27_p[2:0]</td><td colspan="5">dig2gam_vr57_p[4:0]</td><td>98</td></tr>
<tr><td>3st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="3">dig2gam_vr36_p[2:0]</td><td colspan="5">dig2gam_vr59_p[4:0]</td><td>B4</td></tr>
<tr><td>4nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td colspan="6">dig2gam_vr61_p[5:0]</td><td>14</td></tr>
<tr><td>5st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td colspan="6">dig2gam_vr62_p[5:0]</td><td>18</td></tr>
<tr><td>6nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="4">dig2gam_vr50_p[3:0]</td><td colspan="4">dig2gam_vr63_p[3:0]</td><td>CD</td></tr>
<tr><td>Description</td><td colspan="13">dig2gam_vr43_p[6:0]: γ gradient adjustment register for positive polarity
dig2gam_vr27_p[2:0]: γ gradient adjustment register for positive polarity
dig2gam_vr57_p[4:0]: γ gradient adjustment register for positive polarity
dig2gam_vr36_p[2:0]: γ gradient adjustment register for positive polarity
dig2gam_vr59_p[4:0]: γ gradient adjustment register for positive polarity
dig2gam_vr61_p[5:0]: γ gradient adjustment register for positive polarity
dig2gam_vr62_p[5:0]: γ gradient adjustment register for positive polarity
dig2gam_vr50_p[3:0]: γ gradient adjustment register for positive polarity
dig2gam_vr63_p[3:0]: γ gradient adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

Default

Status	Default Value					
	dig2gam_vr43_p[6:0]	dig2gam_vr27_p[2:0]	dig2gam_vr57_p[4:0]	dig2gam_vr36_p[2:0]	dig2gam_vr59_p[4:0]	dig2gam_vr61_p[5:0]
Power On Sequence	7'h3F	3'h04	5'h18	3'h05	5'h14	6'h14
SW Reset	7'h3F	3'h04	5'h18	3'h05	5'h14	6'h14
HW Reset	7'h3F	3'h04	5'h18	3'h05	5'h14	6'h14

Default

Status	Default Value					
	dig2gam_vr62_p[5:0]	dig2gam_vr50_p[3:0]	dig2gam_vr63_p[3:0]			
Power On Sequence	6'h18	4'h0C	4'h0D			
SW Reset	6'h18	4'h0C	4'h0D			
HW Reset	6'h18	4'h0C	4'h0D			

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When GC9308 is used out of the absolute maximum ratings, GC9308 may be permanently damaged. To use GC9308 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, GC9308 will malfunction and cause poor reliability.

Table43.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3~+4.6
Supply voltage(Logic)	IOVCC	V	-0.3~+4.6
Supply voltage(Digital)	VCORE	V	-0.3~+2.0
Driver supply voltage	VGH-VGL	V	-0.3~+32.0
Logic input voltage range	VIN	V	-0.3~IOVCC+0.3
Logic output voltage range	VO	V	-0.3~IOVCC+0.3
Operation temperature	Topr	℃	-40~+80
Storage temperature	Tstg	℃	-55~+110
Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.			

7.2. DC Characteristics

General DC Characteristics

Table44.

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VCI	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	IOVCC	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.34	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	12.0	Note3
Gate Driver Low Voltage	VGL	V	-	-11.0	-	-9.0	Note3
Driver Supply Voltage	-	V	|VGH-VGL|	19	-	23	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	VSSC	-	0.3*IOVCC	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	VSSC	-	0.2*IOVCC	Note1,2,3
Logic High Level Input Current	IIH	uA	-	-	-	1	Note1,2,3
Logic Low Level Input Current	IIL	uA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=IOVCC or VSSC	-0.1	-	+0.1	Note1,2,3
Source Driver							
Source Output Range	Vsout	V	-	VREG2	-	VREG1	Note4

Note 1: IOVCC=1.65 to 3.3V, VCI=2.5 to 3.3V, AGND=VSS=0V, Ta=-30 to 70 (to +85 no damage)℃

Note2: Please supply digital IOVCC voltage equal or less than analog VCI voltage.

Note3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL, IM3, IM2, IM1,IM0, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

Note5: VCI=2.6V

Note6: VCI=3.3V

Note7: The Max. Value is between with Note 4 measure point and Gamma setting value

7.3. AC Characteristics

7.3.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-Ⅰ)

Figure90.

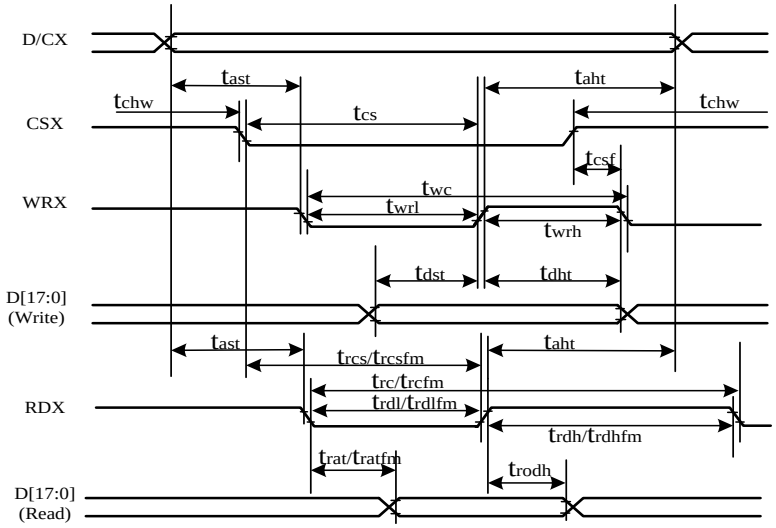


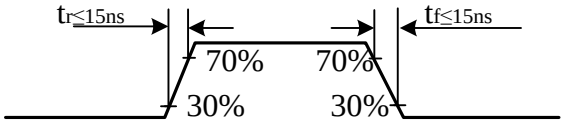
Table45.

Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	380	-	ns	
	trdhfm	Read Control H duration(FM)	180	-	ns	
	trdlfm	Read Control L duration(FM)	200	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control H pulse duration	90	-	ns	
	trdl	Read Control L pulse duration	70	-	ns	
D[17:0], D[15:0],	tdst	Write data setup time	10	-	ns	For maximum CL=30pF
	tdht	Write data hold time	10	-	ns	

D[8:0], D[7:0]	trat	Read access time	-	40	ns	For minimum CL=8pF
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

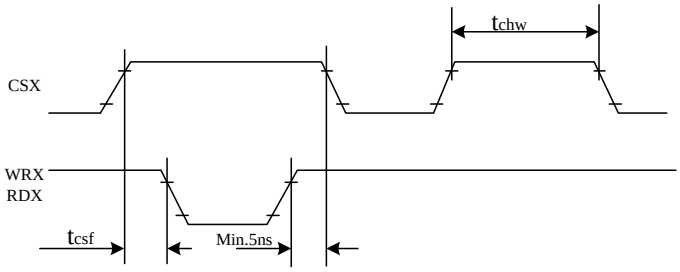
Note: Ta = -30 to 70 ℃, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

Figure91.



CSX timings :

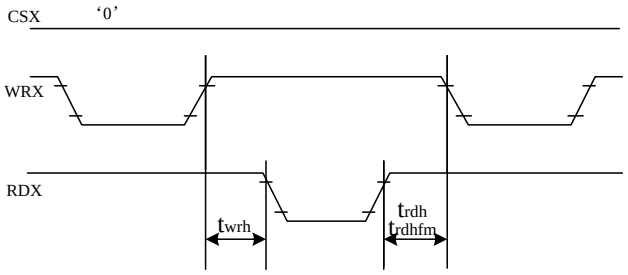
Figure92.



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:

Figure92.



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

7.3.2. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-Ⅱ)

Figure93.

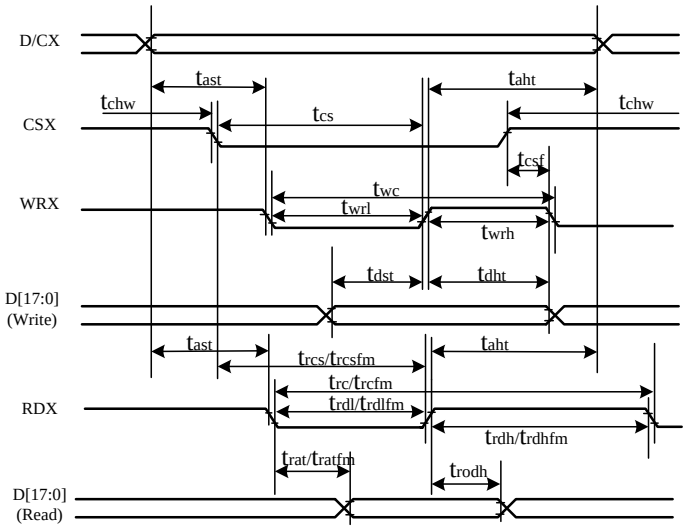
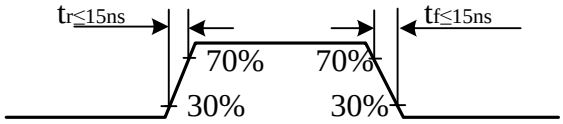


Table46.

Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	380	-	ns	
	trdhfm	Read Control H duration(FM)	180	-	ns	
	trdlfm	Read Control L duration(FM)	200	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	70	-	ns	
D[17:0], D[17:10] &D[8:1], D[17:10] ,D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

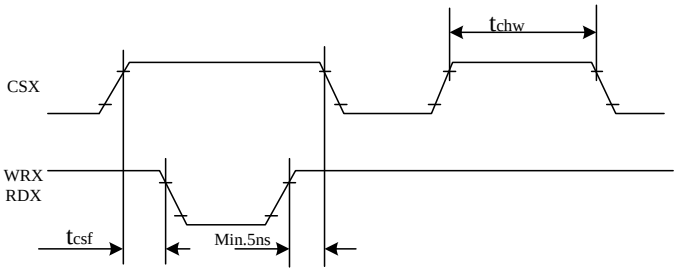
Note: Ta = -30 to 70 ℃, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.

Figure94.



CSX timings :

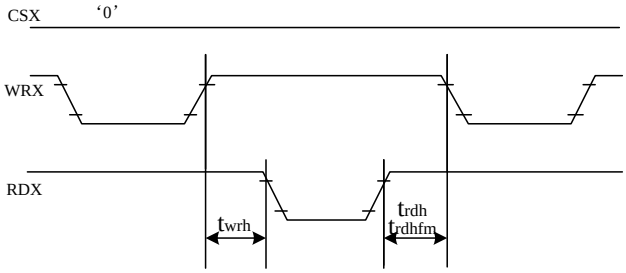
Figure95.



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:

Figure96.



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

7.3.3. Display Serial Interface Timing Characteristics (3-line SPI system)

Figure97.

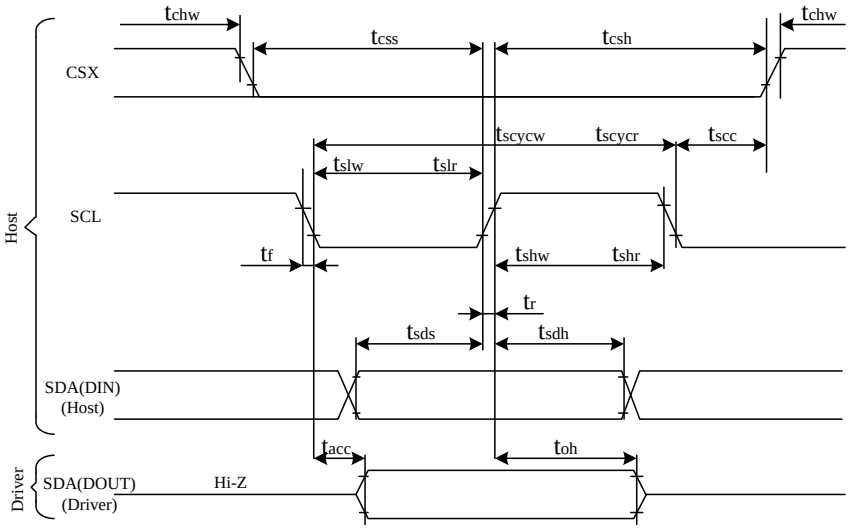
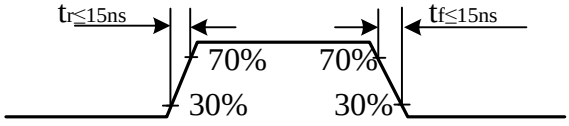


Table47.

Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	10	-	ns	
	tshw	SCL "H" Pulse Width (Write)	5	-	ns	
	tslw	SCL "L" Pulse Width (Write)	5	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA/SDI (Input)	tsds	Data setup time (Write)	5	-	ns	
	tsdh	Data hold time (Write)	5	-	ns	
SDA/SD0(Outp)	tacc	Access time (Read)	10	-	ns	
CSX	tscc	SCL-CSX	10	-	ns	
	tchw	CSX "H" Pulse Width	10	-	ns	
	tcss	CSX-SCL Time	20	-	ns	
	tcsh		40	-	ns	

Note: Ta = 25 ℃, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, VSSA=VSSC=0V

Figure98.



7.3.4. Display Serial Interface Timing Characteristics (4-line SPI system)

Figure98.

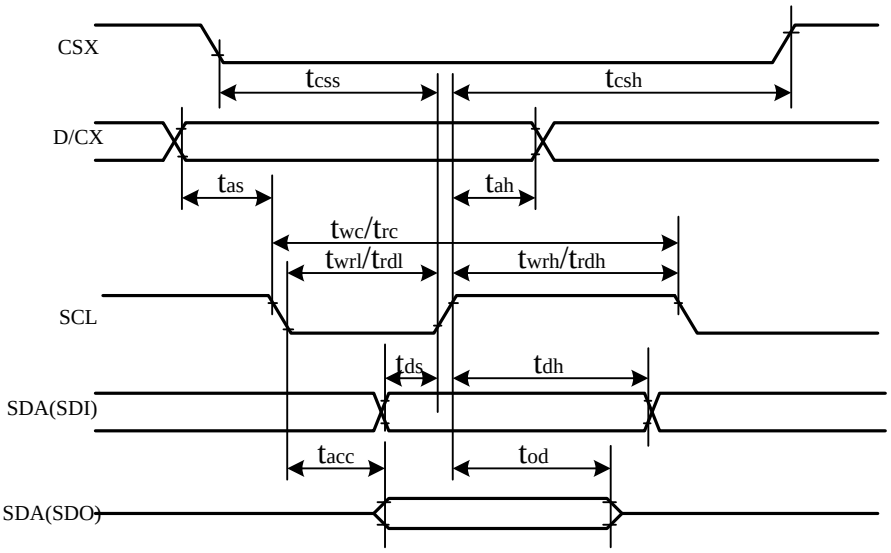
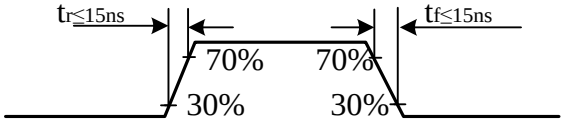


Table48.

Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	20	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial Clock Cycle (Write)	10	-	ns	
	twrh	SCL "H" Pulse Width (Write)	5	-	ns	
	twrl	SCL "L" Pulse Width (Write)	5	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL "H" Pulse Width (Read)	60	-	ns	
	trdl	SCL "L" Pulse Width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA/SDI (Input)	tds	Data setup time (Write)	5	-	ns	
	tdh	Data hold time (Write)	5	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	

Note: Ta = 25 ℃, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

Figure99.



7.3.5. Parallel 18/16/6-bit RGB Interface Timing Characteristics

Figure100.

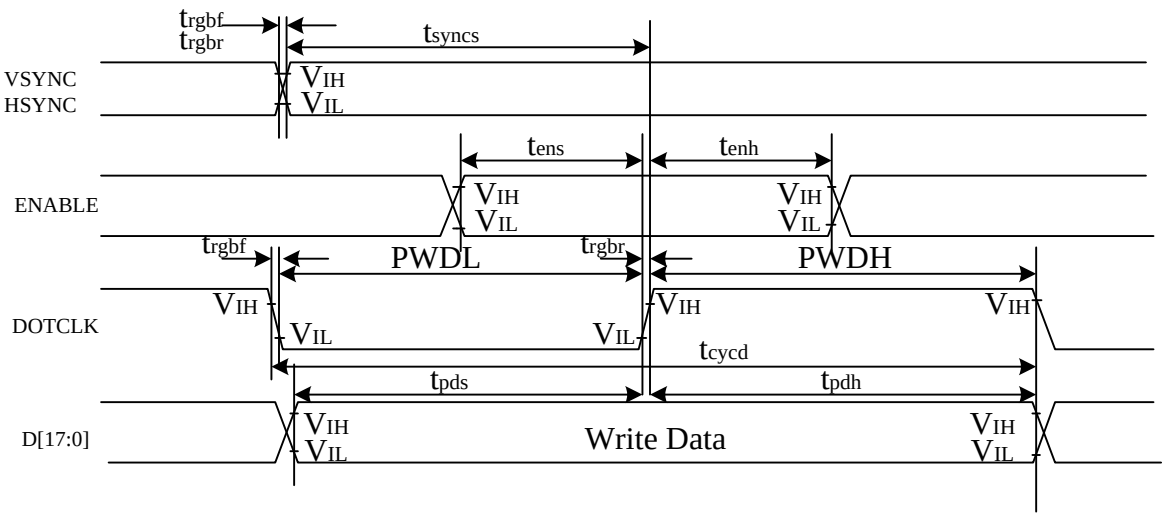


Table49.

Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	15	-	ns	
D[17:0]	tpos	Data setup time	15	-	ns	
	tpdh	Date hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	tcycd	DOTCLK cycle time	100	-	ns	
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	15	-	ns	
D[17:0]	tpos	Data setup time	15	-	ns	
	tpdh	Date hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	tcycd	DOTCLK cycle time	100	-	ns	
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 ℃, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

Figure101.