

# DataSheet

## S6D04M0

**-X21**

**MOBILE DISPLAY DRIVER IC**



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Samsung Electronics Co., Ltd.

San #24 Nongseo-Dong, Giheung-Gu,

Yongin-City, Gyeonggi-Do, Korea

446-711

<http://www.samsung.com/Products/Semiconductor/DisplayDriverIC>

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# Preface

## ***About This Reference Specification***

This document is to provide a complete reference specification of S6D04M0 IC design. It also provides useful information to those who works on a panel module or a set.

## **IMPORTANT NOTICE**

### **Precautions against Light**

The conductivity of a semiconductor is strongly influenced by electro-magnetic radiation such as visible light, infrared light, ultraviolet light, or gamma radiation. When light is absorbed, electron-hole pairs are generated raising the conductivity of the material, eventually altering the electrical characteristics of the IC. Therefore, if the packages that expose IC's to external light sources, such as COB, COG, TCP, and COF, are used, effective means to shield the IC from the light coming in all directions – top, bottom, and the sides – must be devised. Full observation of the following precautions is strongly recommended.

1. Make sure that the IC and substrate (board or glass) are protected from a stray light.
2. Always test and inspect products under the environment with no light penetration.

## CHAPTER 1

# OVERVIEW

- 1.1 Introduction
- 1.2 Product Options
- 1.3 Features
- 1.4 Block Diagram
- 1.5 Pad Information
- 1.6 Description

# 1 OVERVIEW

## 1.1. INTRODUCTION

S6D04M0 is a single-chip display driver IC for a TFT-LCD panel. Integrated on this chip are source drivers with built-in memory, gate drivers and power sources. S6D04M0 can support a TFT-LCD panel up to a resolution of 240-RGB x 320-dot graphics with 16M-color. S6D04M0 also supports various types of peripheral interface such as 80-series MCU interface (8-/9-/16-/18-/24-bits data), and 3-wire 9bit / 4-wire 8bit serial interface S6D04M0 supports various types of RGB interface (24-/18-/16-/8-/6-bits data)

The Integrated on-chip functions that are described in this document include:

- Power saving: It reduces the overall power consumed in a TFT-LCD panel module.
- Internal GRAM:
- Internal DC/DC voltage converter
- MIE (Mobile Image Enhancement) functions

S6D04M0 features several power saving functions to reduce the overall power consumed in a TFT-LCD panel module: S6D04M0 operates at low voltage and has internal GRAMs that can store 240-RGB x 320-dot 16M-color image data. In addition, it has an internal DC/DC voltage converter that generates various voltages needed for driving the TFT-LCD panel by using breeder resistors and the voltage followers.

## 1.2. FEATURES

S6D04M0 offers the following key features:

- A single-chip TFT-LCD Controller/gate driver/source driver with built-in Graphic RAM
- Supported Display panel resolution: 240\*R/G/B (H) \* 320 (V)
- Integrated 1,843,200bit of graphic RAM (GRAM)
  - GRAM configuration:  $240 \times 320 \times 24\text{-bits} = 1,843,200\text{bits}$
- Supported Interfaces
  - 3-wire 9-bit data, 4-wire 8-bit data serial interface (for RGB parallel Interface)
  - 8-/9-/16-/18-/24- bit interface with 80-Series MCU (so called 80-Series)
  - VSYNC I/F
- Outputs
  - Common electrode output
  - Gate outputs
  - Source outputs
- Color Display mode
  - Full color mode (Idle mode off): 16M / 260k / 65k colors
  - Reduced color mode (Idle mode on): 8-colors (3-bit binary mode)
- Color modes on the display host interface
  - 16-bits/Pixel: RGB= (565) using the 1,843k bit frame memory
  - 18-bits/Pixel: RGB= (666) using the 1,843k bit frame memory
  - 24-bits/Pixel: RGB= (888) using the 1,843k bit frame memory
- Display features
  - Partial display mode
- Driving scheme: line inversion & frame inversion
- MIE (Mobile Image Enhancement) functions
  - Adaptive luminance/contrast enhancement function.
  - Reduce the power consumption of backlight.
- On-chip functions
  - Voltage Boosters
  - Adjustable VCOM voltage source generator
  - An oscillator for display clock generation & Timing generation
  - 4 preset gamma curves to be selectable
  - **Gamma circuit for R,G, and B respectively**
  - Factory default value (Contrast, Module ID, Module version, etc) can be stored inside IC
  - MTP (Multiple-time Programmable) Memory
  - MTP initialization & program voltages are generated automatically from the built-in power circuit.
  - Each 8-bits product ID1, ID2, ID3

- Each 5-bits for VCM, VML, GVD offset adjustment
- 1 bit for MTP writing protection
- Voltage Supplies
  - 2.3V – 3.3V for VCI, supply voltage for Analog blocks
  - 1.65V – 3.3V for VDD3, Supply voltage for I/O
- Output voltage levels
  - 2.5V to 5.0V for GVDD, Source output voltage
  - AVDD, Power supply for driver circuit (Note 1)
  - Maximum 6.0V for VCOM, Common electrode output voltage
  - 11.25V to 16.50V for VGH, Positive Gate output voltage (Note 2, Note 3)
  - -13.75V to -6.75V for VGL, Negative Gate output voltage (Note 2)
- CMOS compatible inputs
- COG package
- Operating temperature range: -40 to +85

Note1. Available AVDD Min: 4.5V at VCI1 = 2.25V, Max=6V at VCI1 = 3V

Note2. |VGH| & |VGL| Min: VCI1 = 2.25V, |VGL| Max: VCI1=2.75V, |VGH – VGL| Max = 30V

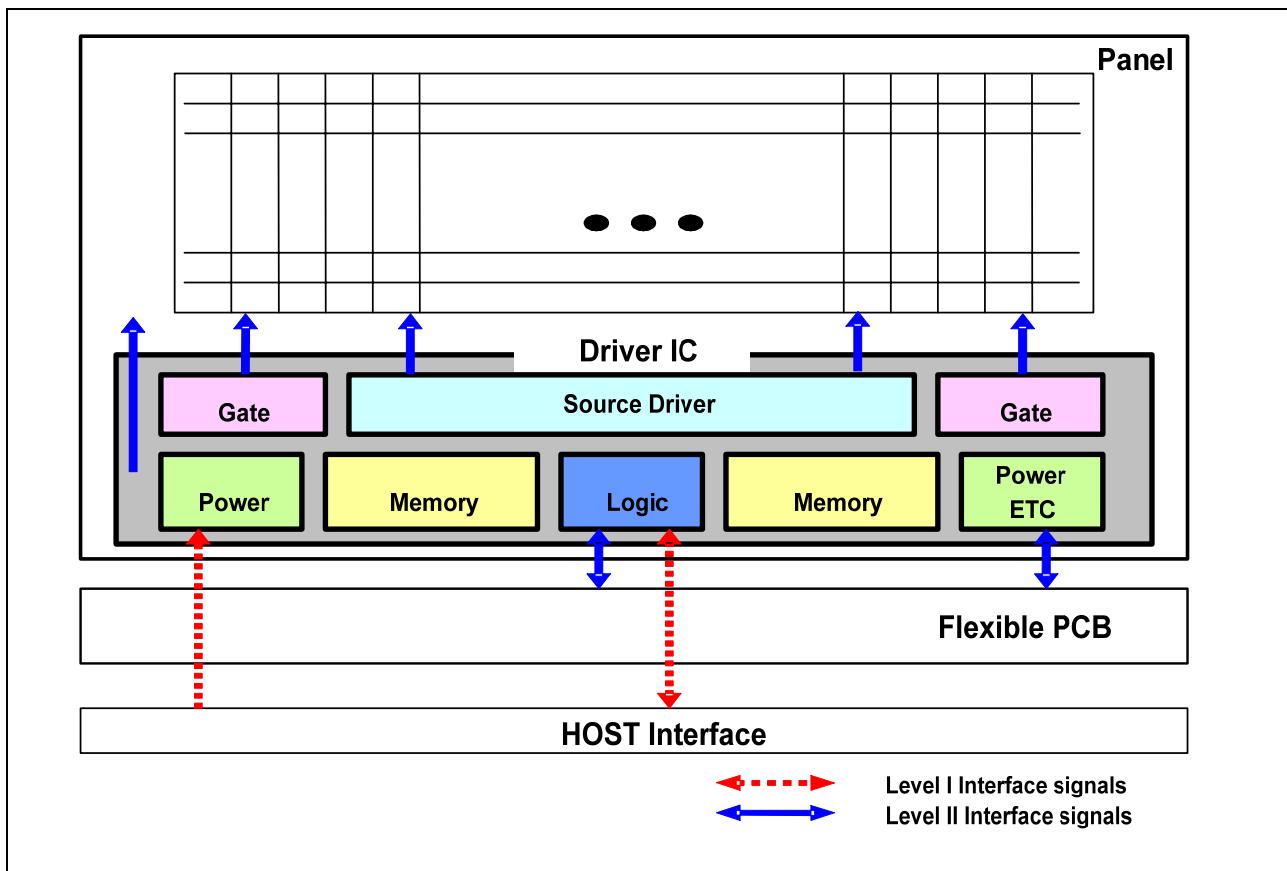
Note3. Maximum |VGH| should be lower than or equal to 16.5V in normal operating condition, regardless of VCI1 & BT settings.

Note4. Blank display means: For normally white panel, the blank display indicates white display. For normally black panel, the blank display indicates black display

## 1.3. BLOCK DIAGRAM

### 1.3.1. Module Level

Figure 1 shows the block diagram of a mobile display panel module and related interface signals required by set makers and module makers. Level I interface signals represent the requirements by a set manufacturer that must be complied to by a module manufacturer. Level II interface signals, on the other hand, represent the requirements from the module manufacturer to that, typically, a driver IC manufacturer must comply.



**Figure 1. Interface signal flow of a mobile display panel module.**

There are also Level III signals which are for internal use only for the driver IC itself. These signals may not necessarily be released to the customer since they are designed for a specific manufacturing purpose and are supposed to be hidden features.

The reference specifications shown in this document serve only as guidelines to Level I and II interface signals only; the reason being that a specification related to Level I and II considers the parasitic and design requirements within the flexible PCB used by a display module maker. IC specification will offer related information among Level I/II on how each interface signals relates to each other.

## 1.3.2. Functional Block Diagram of the IC

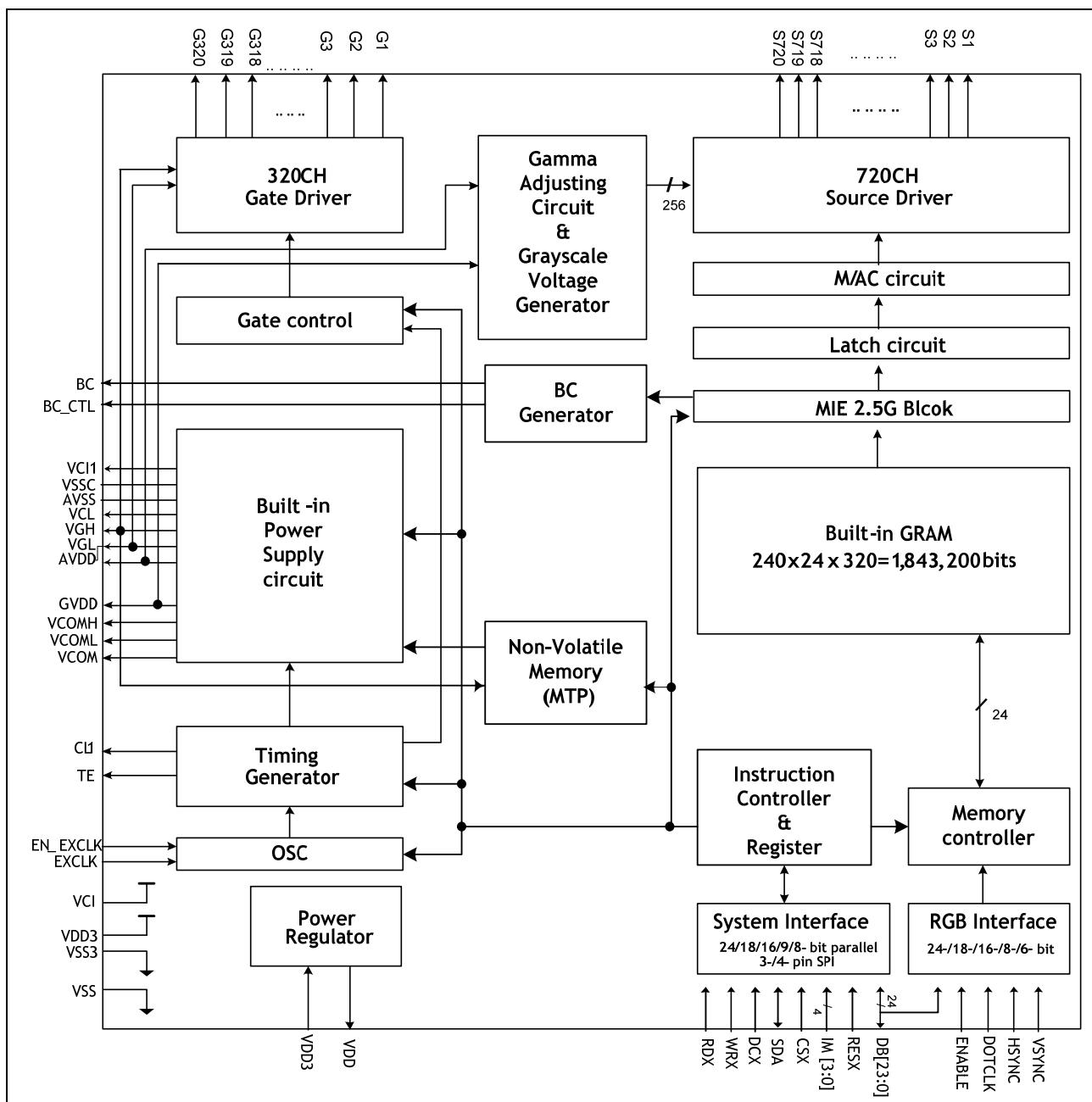


Figure 2. S6D04M0 block diagram

## 1.4. PAD INFORMATION

### 1.4.1. Configuration of Signal Pads

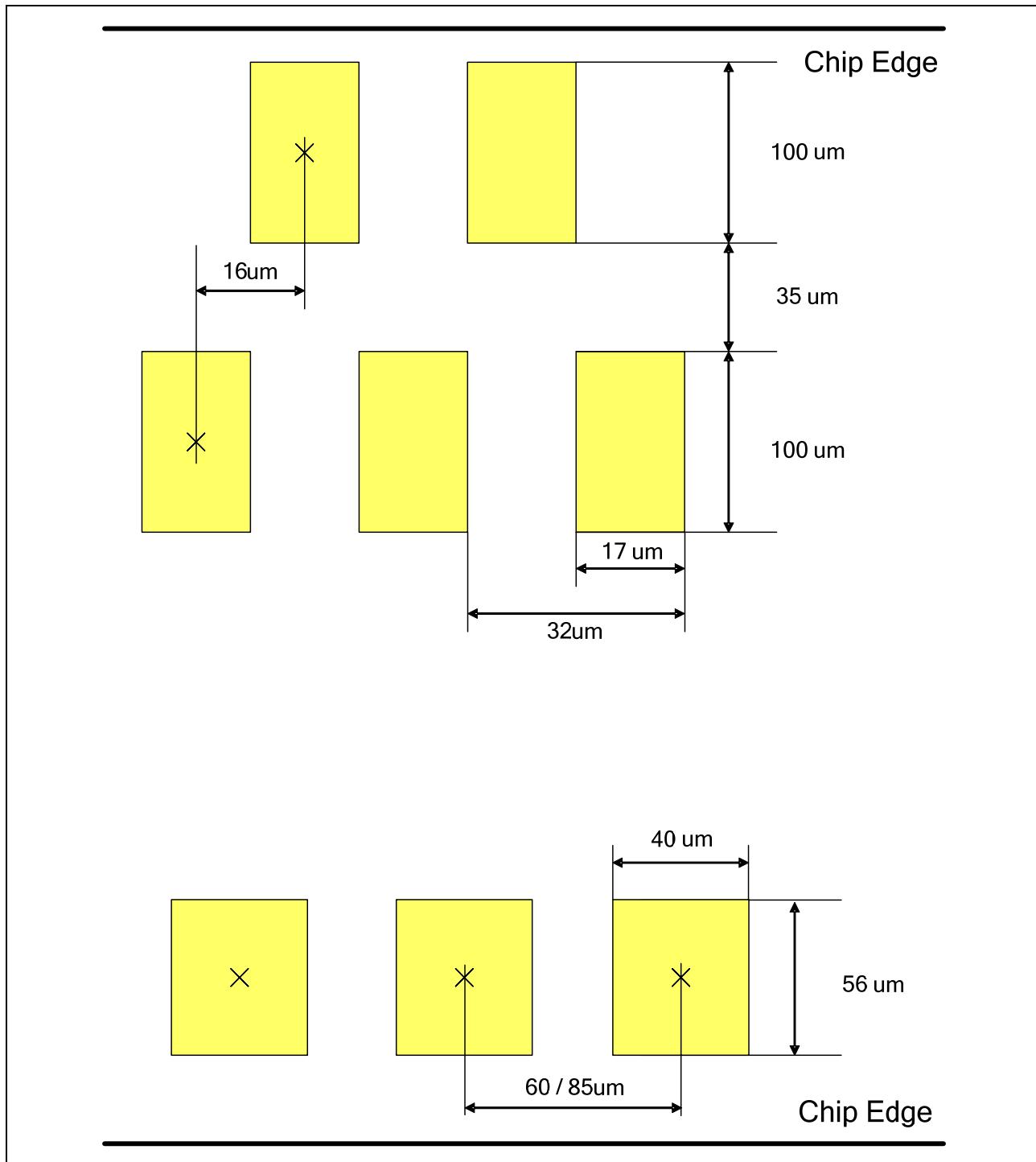


Figure 3. S6D04M0 pad configuration

Note: Pattern Surface

### 1.4.2. Bump

**Table 1. S6D04M0 pad dimensions**

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	17,300	1,140	
Pad pitch	Input Side	Data	60 / 85	μm
		Different signal	60 / 85	
		Same signal	60 / 85	
	Output Side	Gate	16	
		Source	16	
Bumped Pad top size	Input Side	Data	40±2	56±2
		Different signal	40±2	56±2
		Same signal	40±2	56±2
	Output Side	Gate	17±2	100±2
		Source	17±2	100±2
Bumped pad height	Height In Wafer		15±3	
	Tolerance In Chip		Under 2	
	Dimple Height		Under 2	
Chip Thickness	-		Note2	
PI Thickness			4.5 ~ 6.5	

Note1: Scribe lane 80um included in this die size

Note2: Wafer Thickness can be varies based on the Customer's need.

Ex) S6D04M0 - Y : 470um

S6D04M0 - G : 375um

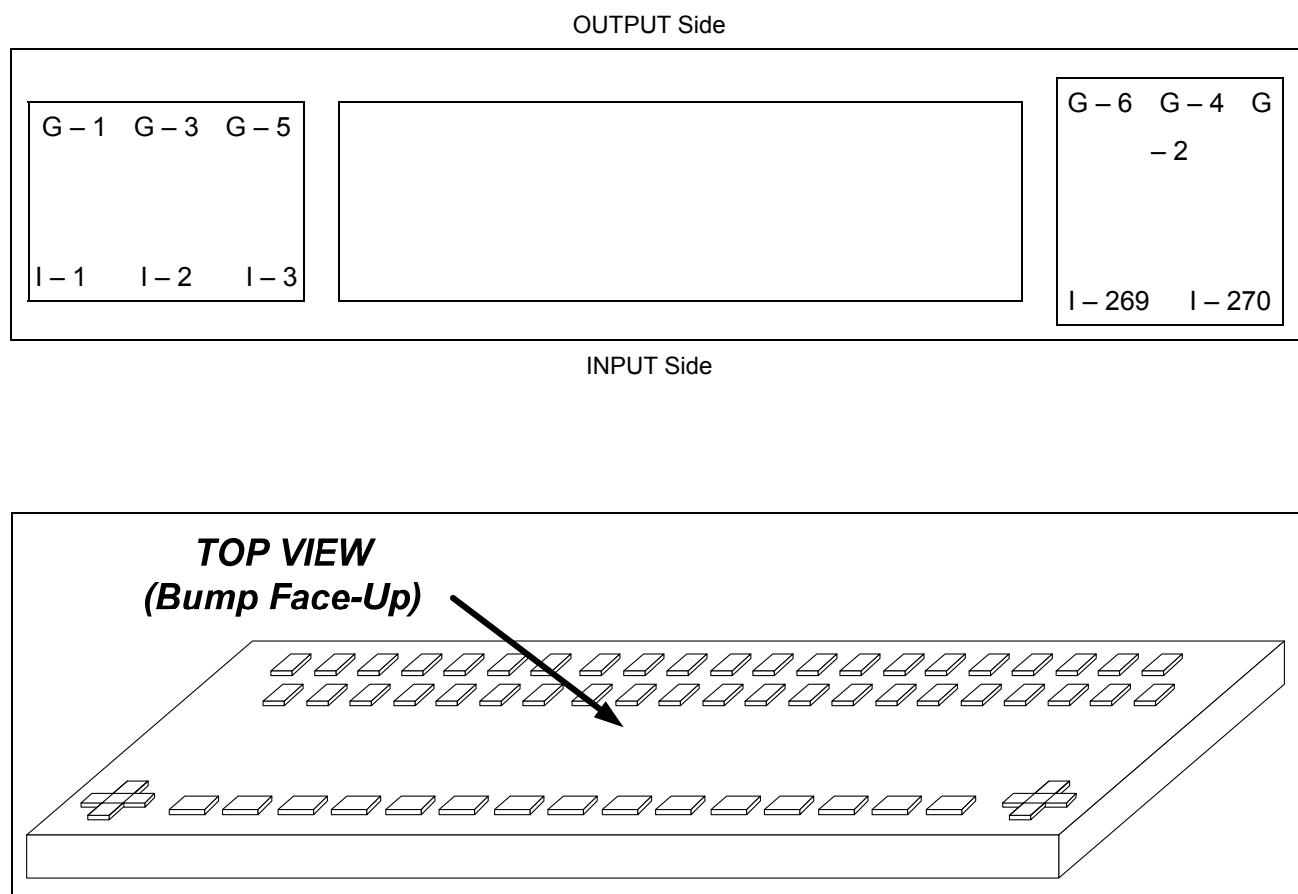


Figure 4. Pad arrangement layout

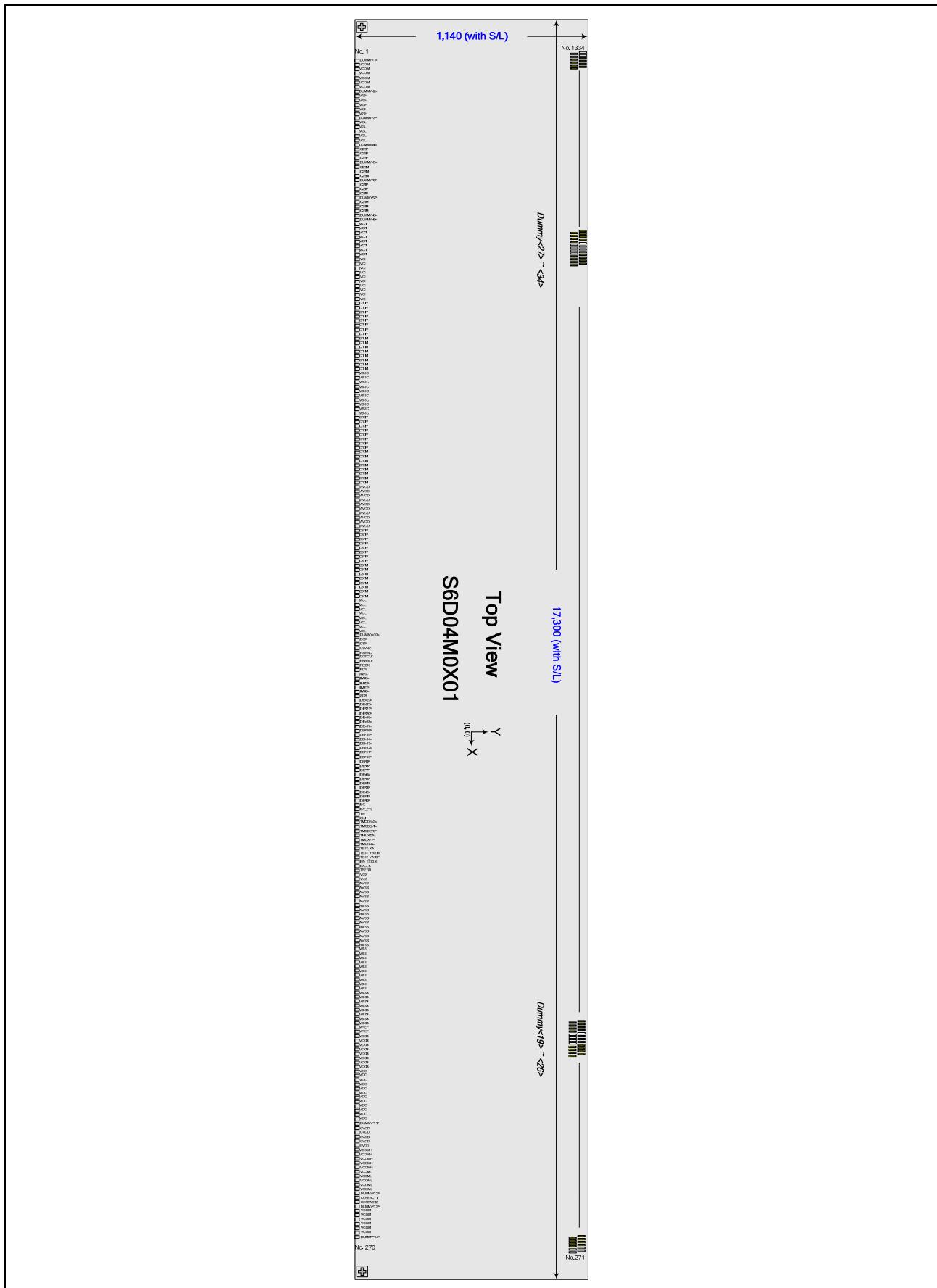


Figure 5. Chip outline

### 1.4.3. Align Key

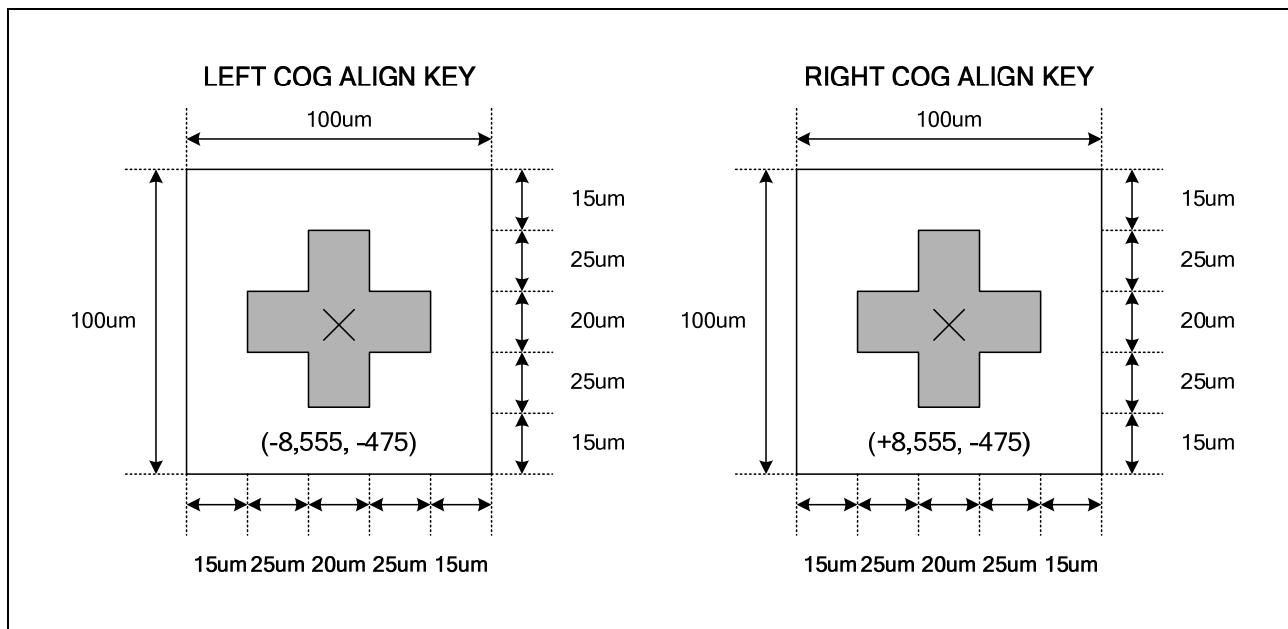


Figure 6. COG align key configuration and coordinate

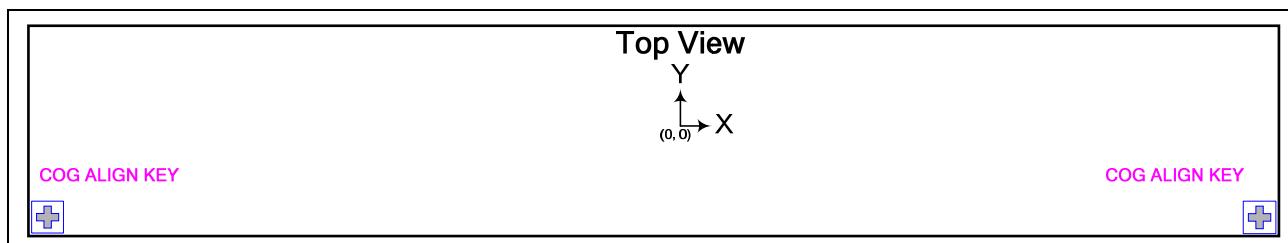


Figure 7. COG align key arrangement layout

## 1.5. DESCRIPTION OF SIGNAL PADS

### 1.5.1. Pads for Power Supplies

Table 2. Pads for power supplies

Name	I/O	Description
VDD	O	Voltage regulator output for internal memory and logic circuit. Do not apply any external power to this pad. Connect a capacitor for stabilization.
VDD3	P	Power supply for I/O block provided from outside
VCI	P	Power supply for analog and voltage booster block.

Name	I/O	Description
AVSS	P	GND for analog circuits.
VSSC	P	GND for voltage booster circuits.
VSS	P	GND for logic circuits.
VSS3	P	GND for I/O block.
AVDD	O	Internally generated voltage output pad for source driver block. Output voltage of 1 <sup>st</sup> booster circuit (=2 x VCI1) Input voltage to 2nd booster circuit. Connect a capacitor for storage function.
VCI1	O	Reference input voltage for 1st booster circuit. Connect a capacitor for stabilization. Note. VCI1 cannot exceed 3V.
VGH	O	Positive power output of the 2nd booster circuit. Gate "ON" level voltage. Connect a capacitor for storage function.
VGL	O	Negative power output of the 2nd booster circuit. Gate "OFF" level voltage. Connect a capacitor for storage function.
VCL	O	3rd booster output voltage. Power supply for generating VCOML block. Connect a capacitor for storage function.
VGS	I	Reference voltage input for grayscale voltage generator. Connect an external resistor or to the system ground.
VREF	O	Reference voltage for generating VCI1, GVDD, VCOMH and VCOML voltages. Connect a capacitor for better RF immunity (optional).
GVDD	O	Reference voltage input for grayscale voltage generator. An internal register can be used to adjust the GVDD voltage. Connect a capacitor for stabilization.
VCOMH	O	High level output voltage of VCOM. An internal register can be used to adjust the VCOMH voltage. Connect a capacitor for stabilization.
VCOML	O	Low level output voltage of VCOM. An internal register can be used to adjust the difference voltage between VCOMH and VCOML. Connect a capacitor for stabilization.

**Table 3. Pads for power supplies (continued)**

Symbol	I/O	Description
VCOM	O	Power supply pad for the TFT- display common electrode. Charge recycling method is used with VCI voltage. Connect this pad to the TFT-display common electrode
C11P C11M C12P C12M	-	Connect the charge-pumping capacitor for generating AVDD level.
C21P C21M C22P C22M	-	Connect the charge-pumping capacitor for generating VGH, VGL level.
C31P C31M	-	Connect the charge-pumping capacitor for generating VCL level.

### 1.5.2. Signal Pads for Logic Interface

**Table 4. Signal pads for logic interface**

Name	I/O	Description					
		Selects the interface mode.					
		IM3	IM2	IM1	IM0	Interface mode	DB pad
IM[3:0]	I	1	0	0	0	80 MCU 24-bit Parallel I/F Type I	DB[23:0]
		0	0	0	0	80 MCU 16-bit Parallel I/F Type I	DB[15:0]
		0	0	0	1	80 MCU 8-bit Parallel I/F Type I	DB[7:0]
		0	1	0	0	80 MCU 18-bit Parallel I/F Type I	DB[17:0]
		1	0	0	1	80 MCU 24-bit Parallel I/F Type II	DB[23:0]
		0	0	1	0	80 MCU 16-bit Parallel I/F Type II	DB[17:10], DB[8:1]
		0	0	1	1	80 MCU 8-bit Parallel I/F Type II	DB[17:10]
		1	0	1	0	80 MCU 18-bit Parallel I/F Type II	DB[17:0]
		1	0	1	1	80 MCU 9-bit Parallel I/F	DB[17:9]
		0	1	1	0	3-wire 9-bit data Serial interface	Refer to table6
		0	1	1	1	4-wire 8-bit data Serial interface	Refer to table6
RESX	I	Active low. This signal is used to reset the device and must be applied to initialize the chip properly.					
CSX	I	Chip select signal. Activate MCU interface mode by setting this to 'low'. This pad can be permanently connected to "Low" in MCU interface mode only.  If not used, connect this pad to either VSS or VDD3.					
DCX	I	Display Data/Command selection signal in parallel interface  DCX='1': Display Data or Command parameter.  DCX='0': Command Index.  Serial interface clock (SCL) in 3-wire/9-bit serial data interface.					
RDX	I	Read Enable in 80-parallel interface.  If not used, connect this pad to VDD3.					
WRX	I	Write Enable in 80-parallel interface.  <b>If not used, connect this pad to VDD3.</b>  Serial interface clock (SCL) in 4-wire/8-bit serial data interface.					

Table 5. Signal pads for logic interface(continued)

Name	I/O	Description																																																																										
		Data Bus.																																																																										
		<table border="1"> <thead> <tr> <th colspan="2">Interface Mode</th> <th colspan="2">Description</th> </tr> <tr> <th>IM</th> <th>Interface Mode</th> <th>Index</th> <th>Data</th> </tr> </thead> <tbody> <tr> <td>1000</td> <td>80 MCU 24-bit Parallel I/F Type I</td> <td>DB[7:0]</td> <td>DB[23:0]</td> </tr> <tr> <td>0000</td> <td>80 MCU 16-bit Parallel I/F Type I</td> <td>DB[7:0]</td> <td>DB[15:0]</td> </tr> <tr> <td>0001</td> <td>80 MCU 8-bit Parallel I/F Type I</td> <td>DB[7:0]</td> <td>DB[7:0]</td> </tr> <tr> <td>0100</td> <td>80 MCU 18-bit Parallel I/F Type I</td> <td>DB[7:0]</td> <td>DB[17:0]</td> </tr> <tr> <td>1001</td> <td>80 MCU 24-bit Parallel I/F Type II</td> <td>DB[8:1]</td> <td>DB[23:0]</td> </tr> <tr> <td>0010</td> <td>80 MCU 16-bit Parallel I/F Type II</td> <td>DB[8:1]</td> <td>DB[17:10], DB[8:1]</td> </tr> <tr> <td>0011</td> <td>80 MCU 8-bit Parallel I/F Type II</td> <td>DB[17:10]</td> <td>DB[17:10]</td> </tr> <tr> <td>1010</td> <td>80 MCU 18-bit Parallel I/F Type II</td> <td>DB[8:1]</td> <td>DB[17:0]</td> </tr> <tr> <td>1011</td> <td>80 MCU 9-bit Parallel I/F</td> <td>DB[17:10]</td> <td>DB[17:9]</td> </tr> </tbody> </table>				Interface Mode		Description		IM	Interface Mode	Index	Data	1000	80 MCU 24-bit Parallel I/F Type I	DB[7:0]	DB[23:0]	0000	80 MCU 16-bit Parallel I/F Type I	DB[7:0]	DB[15:0]	0001	80 MCU 8-bit Parallel I/F Type I	DB[7:0]	DB[7:0]	0100	80 MCU 18-bit Parallel I/F Type I	DB[7:0]	DB[17:0]	1001	80 MCU 24-bit Parallel I/F Type II	DB[8:1]	DB[23:0]	0010	80 MCU 16-bit Parallel I/F Type II	DB[8:1]	DB[17:10], DB[8:1]	0011	80 MCU 8-bit Parallel I/F Type II	DB[17:10]	DB[17:10]	1010	80 MCU 18-bit Parallel I/F Type II	DB[8:1]	DB[17:0]	1011	80 MCU 9-bit Parallel I/F	DB[17:10]	DB[17:9]																											
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1011	80 MCU 9-bit Parallel I/F	DB[17:10]	DB[17:9]																																																																									
		<table border="1"> <thead> <tr> <th colspan="3">Interface Mode</th> <th colspan="2">Description</th> </tr> <tr> <th>IM</th> <th>RIM</th> <th>VFPF (Note*)</th> <th>Interface Mode</th> <th>Index</th> <th>Data</th> </tr> </thead> <tbody> <tr> <td></td> <td>0</td> <td>111</td> <td>3-wire 9-bit data Serial Interface &amp; RGB 24-bit I/F</td> <td>SDA</td> <td>DB[23:0]</td> </tr> <tr> <td></td> <td>0</td> <td>110</td> <td>3-wire 9-bit data Serial Interface &amp; RGB 18-bit I/F</td> <td>SDA</td> <td>DB[17:0]</td> </tr> <tr> <td>DB[23:0]</td> <td>0110</td> <td>0</td> <td>3-wire 9-bit data Serial Interface &amp; RGB 16-bit I/F</td> <td>SDA</td> <td>DB[17:10], DB[8:1]</td> </tr> <tr> <td></td> <td></td> <td>1</td> <td>3-wire 9-bit data Serial Interface &amp; RGB 8-bit I/F</td> <td>SDA</td> <td>DB[17:10]</td> </tr> <tr> <td></td> <td></td> <td>1</td> <td>3-wire 9-bit data Serial Interface &amp; RGB 6-bit I/F</td> <td>SDA</td> <td>DB[17:12]</td> </tr> <tr> <td></td> <td></td> <td>0111</td> <td>4-wire 8-bit data Serial Interface &amp; RGB 24-bit I/F</td> <td>SDA</td> <td>DB[23:0]</td> </tr> <tr> <td></td> <td></td> <td>0</td> <td>4-wire 8-bit data Serial Interface &amp; RGB 18-bit I/F</td> <td>SDA</td> <td>DB[17:0]</td> </tr> <tr> <td></td> <td></td> <td>0</td> <td>4-wire 8-bit data Serial Interface &amp; RGB 16-bit I/F</td> <td>SDA</td> <td>DB[17:10], DB[8:1]</td> </tr> <tr> <td></td> <td></td> <td>1</td> <td>4-wire 8-bit data Serial Interface &amp; RGB 8-bit I/F</td> <td>SDA</td> <td>DB[17:10]</td> </tr> <tr> <td></td> <td></td> <td>1</td> <td>4-wire 8-bit data Serial Interface &amp; RGB 6-bit I/F</td> <td>SDA</td> <td>DB[17:12]</td> </tr> </tbody> </table>				Interface Mode			Description		IM	RIM	VFPF (Note*)	Interface Mode	Index	Data		0	111	3-wire 9-bit data Serial Interface & RGB 24-bit I/F	SDA	DB[23:0]		0	110	3-wire 9-bit data Serial Interface & RGB 18-bit I/F	SDA	DB[17:0]	DB[23:0]	0110	0	3-wire 9-bit data Serial Interface & RGB 16-bit I/F	SDA	DB[17:10], DB[8:1]			1	3-wire 9-bit data Serial Interface & RGB 8-bit I/F	SDA	DB[17:10]			1	3-wire 9-bit data Serial Interface & RGB 6-bit I/F	SDA	DB[17:12]			0111	4-wire 8-bit data Serial Interface & RGB 24-bit I/F	SDA	DB[23:0]			0	4-wire 8-bit data Serial Interface & RGB 18-bit I/F	SDA	DB[17:0]			0	4-wire 8-bit data Serial Interface & RGB 16-bit I/F	SDA	DB[17:10], DB[8:1]			1	4-wire 8-bit data Serial Interface & RGB 8-bit I/F	SDA	DB[17:10]			1	4-wire 8-bit data Serial Interface & RGB 6-bit I/F	SDA	DB[17:12]
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		1	4-wire 8-bit data Serial Interface & RGB 6-bit I/F	SDA	DB[17:12]																																																																							
		Note1. "X" denotes "Don't care"																																																																										
		Note2. VFPF = COLMOD[6:4] (Refer to 3Ah Command)																																																																										
		Must be connected to VDD3 or VSS level when not used.																																																																										
SDA	I/O	Serial data bus. If not used, leave this pad unconnected.																																																																										



**Table 6. Signal pads for logic interface(continued)**

Name	I/O	Description
TE	O	Tearing effect output pad to synchronize MCU to frame writing, activated by S/W command. When this pad is not activated, this signal stays low. If not used, leave this pad unconnected.
DOTCLK	I	Pixel clock signal in RGB I/F mode. If not used, connect this pad to either VDD3 or VSS.
VSYNC	I	Vertical Sync signal in RGB I/F mode. If not used, connect this pad to either VDD3 or VSS.
H SYNC	I	Horizontal Sync signal in RGB I/F mode. If not used, connect this pad to either VDD3 or VSS.
ENABLE	I	Data Enable signal in RGB I/F mode. If not used, connect this pad to either VDD3 or VSS.

Note.

If CSX is connected to VSS in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there should be no influence to the Power Consumption of the display module.

When CSX='1', there is no influence to the parallel interface.

**Table 7. Pads for source/gate driver output signal**

Name	I/O	Description
S1 to S720	O	Signal pads for Source driver output.
G1 to G320	O	Signal pads for Gate driver output.

**Table 8. MIE pins**

Symbol	I/O	Description
BC	O	This pin is used to PWM output for back light control of LED driver. If not used, this pin should be opened.
BC_CTL	O	This pin is used to enable the back light LED driver (active high). If not used, this pin should be opened.

**Table 9. Miscellaneous signal pads**

Name	I/O	Description
CL1	O	Output pads used only for test purpose at IC-side. In normal operation, leave this pad unconnected.
CONTACT1 CONTACT2	-	Contact resistance measurement pad. In normal operation, leave this unconnected. These pads are at VSS level. When measuring an ohmic resistance of the contact, do not apply any power.



## 1.6. INTERFACE PAD CONFIGURATION

**Table 10. Interface pad configuration1 (parallel mode)**

PIN NAME	80 MCU Type I				80 MCU Type II				
	24bit	16bit	8bit	18bit	24bit	16bit	8bit	18bit	9bit
IM[3]	VDD3	VSS	VSS	VSS	VDD3	VSS	VSS	VDD3	VDD3
IM[2]	VSS	VSS	VSS	VDD3	VSS	VSS	VSS	VSS	VSS
IM[1]	VSS	VSS	VSS	VSS	VSS	VDD3	VDD3	VDD3	VDD3
IM[0]	VSS	VSS	VDD3	VSS	VDD3	VSS	VDD3	VSS	VDD3
DB[23:18]	DB[23:18]	VDD3/VSS			DB[23:18]	VDD3/VSS			
DB[17:16]	DB[17:16]	VDD3/VSS		DB[17:16]	DB[17:16]	DB[17:16]	DB[17:16]	DB[17:16]	DB[17:16]
DB[15:13]	DB[15:13]	DB[15:13]	VDD3/VSS	DB[15:13]	DB[15:13]	DB[15:13]	DB[15:13]	DB[15:13]	DB[15:13]
DB[12]	DB[12]	DB[12]	VDD3/VSS	DB[12]	DB[12]	DB[12]	DB[12]	DB[12]	DB[12]
DB[11:10]	DB[11:10]	DB[11:10]	VDD3/VSS	DB[11:10]	DB[11:10]	DB[11:10]	DB[11:10]	DB[11:10]	DB[11:10]
DB[9]	DB[9]	DB[9]	VDD3/VSS	DB[9]	DB[9]	VDD3/VSS	VDD3/VSS	DB[9]	DB[9]
DB[8]	DB[8]	DB[8]	VDD3/VSS	DB[8]	DB[8]	DB[8]	VDD3/VSS	DB[8]	VDD3/VSS
DB[7:1]	DB[7:1]	DB[7:1]	DB[7:1]	DB[7:1]	DB[7:1]	DB[7:1]	VDD3/VSS	DB[7:1]	VDD3/VSS
DB[0]	DB[0]	DB[0]	DB[0]	DB[0]	DB[0]	VDD3/VSS	VDD3/VSS	DB[0]	VDD3/VSS
SDA	Floating								
CSX	CSX								
WRX	WRX								
RDX	RDX								
DCX	DCX								
RESX	RESX								
VSYNC	(VSYNC) Note1*								
HSYNC	VDD3/VSS								
ENABLE	VDD3/VSS								
DOTCLK	VDD3/VSS								
TMODE[2:0]	VSS								

Note1. In VSYNC Interface, VSYNC signal is valid. Other cases VSYNC has to tied to VDD3 or VSS.

Table 11. Interface pad configuration2 (serial mode)

PIN NAME	RGB(3wire)					RGB(4wire)																			
	24bit	18bit	16bit	8bit	6bit	24bit	18bit	16bit	8bit	6bit															
IM[3]	VSS					VSS																			
IM[2]	VDD3					VDD3																			
IM[1]	VDD3					VDD3																			
IM[0]	VSS					VDD3																			
DB[23:18]	DB [23:18]	VDD3/VSS				DB [23:18]	VDD3/VSS																		
DB[17:16]	DB [17:16]																								
DB[15:13]	DB [15:13]																								
DB[12]	DB[12]	DB[12]	DB[12]	DB[12]	DB[12]	DB[12]	DB[12]	DB[12]	DB[12]	DB[12]															
DB[11:10]	DB [11:10]	DB [11:10]	DB [11:10]	DB [11:10]	VDD3 /VSS	DB [11:10]	DB [11:10]	DB [11:10]	DB [11:10]	VDD3 /VSS															
DB[9]	DB[9]	DB[9]	VDD3/VSS			DB[9]	DB[9]	VDD3/VSS																	
DB[8]	DB[8]	DB[8]	DB[8]	VDD3/VSS		DB[8]	DB[8]	DB[8]	VDD3/VSS																
DB[7:1]	DB[7:1]	DB[7:1]	DB[7:1]	VDD3/VSS		DB[7:1]	DB[7:1]	DB[7:1]																	
DB[0]	DB[0]	DB[0]	VDD3/VSS			DB[0]	DB[0]	VDD3/VSS																	
SDA	SDA																								
CSX	CSX																								
WRX	VDD3					SCL																			
RDX	VDD3																								
DCX	SCL					DCX																			
RESX	RESX																								
VSYNC	VSYNC																								
HSYNC	HSYNC																								
ENABLE	ENABLE																								
DOTCLK	DOTCLK																								
TMODE[2:0]	VSS																								



**Table 12. Test signal pads and dummy pads.**

Name	I/O	Description
TMODE[2:0]	I	Input pads used only for test purpose at IC-side. During normal operation, connect this pad to VSS.
EN_EXCLK	I	Input pads used only for test purpose at IC-side. During normal operation, connect this pad to VSS.
EXCLK	I	Input pads used only for test purpose at IC-side. During normal operation, connect this pad to VSS.
TREGB	I	Input pads used only for test purpose at IC-side. During normal operation, connect this pad to VSS.
TMUX[2:0]	I	Input pads used only for test purpose at IC-side. During normal operation, connect this pad to VSS.
TEST_XA	I	Input pads used only for test purpose at IC-side. During normal operation, connect this pad to VSS.
TEST_YA[1:0]	I	Input pads used only for test purpose at IC-side. During normal operation, connect this pad to VSS.
Dummy[1]	-	Input-side dummy pad. This pad shows VSS potential during power-on status.
Dummy[2:13]	-	Input-side dummy pads. These pads have no potential.
Dummy[14]	-	Input-side dummy pad. This pad shows VSS potential during power-on status.
Dummy[15:18]	-	Output-side dummy pads. These pads have no potential.
Dummy[19:20]	-	Output-side dummy pads. These pads show VGL potential during normal operating condition.
Dummy[21:32]	-	Output-side dummy pads. These pads have no potential.
Dummy[33:34]	-	Output-side dummy pads. These pads show VGL potential during normal operating condition.
Dummy[35:38]	-	Output-side dummy pads. These pads have no potential.

## CHAPTER 2

# ELECTRICAL SPECIFICATION

- 2.1 Absolute Maximum Ratings
- 2.2 DC Electrical Characteristics
- 2.3 AC Characteristics

# 2 ELECTRICAL SPECIFICATIONS

## 2.1. ABSOLUTE MAXIMUM RATINGS

**Table 13. Absolute maximum ratings**

Item	Symbol	Rating	Unit
Supply voltage for logic block	VDD - VSS	-0.3 to +3.3	V
Supply voltage for I/O block	VDD3 - VSS	-0.3 to +5.0	V
Supply voltage for step-up circuit	VCI - VSS	-0.3 to +5.0	V
LCD Supply Voltage range	AVDD – VSS	-0.3 to +6.5	V
	VGH - VSS	-0.3 to +22.0	V
	VSS – VGL	-0.3 to +22.0	V
	VSS - VCL	-0.3 to +5.0	V
	VGH – VGL	-0.3 to +33	V
Input Voltage range	Vin	- 0.3 to VDD3 + 0.5	V
Operating temperature	Topr	-40 to +85	°C
Storage temperature	Tstg	-55 to +110	°C

Note1. The absolute maximum rating is the limit value. When the IC is exposed to the operating environment beyond this range, the IC does not assure normal operations and may be damaged permanently, not be able to be recovered.

Note2. The operating temperature is the range of device-operating temperature. It means that the performance of the driver IC would be guaranteed only within this temperature range.

### Caution

**Stresses above these absolute maximum ratings may cause permanent damage. These are stress ratings only and functional operation at these conditions is not implied. Exposure to maximum rating conditions for extended periods may reduce device reliability.**

## 2.2. DC ELECTRICAL CHARACTERISTICS

### 2.2.1. Basic Characteristics

**Table 14. DC electrical characteristics (Ta = - 40 ~ 85 °C ).**

Characteristic	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Power supply for I/O	VDD3		1.65	-	3.3	V	*1
Power supply	VCI		2.3	-	3.3	V	
LCD driving voltage	VGH		11.25	-	16.50	V	*8
	VGL		-13.75	-	-6.75	V	
	VCL		-3.0	-	-2.25	V	
	AVDD		4.5	-	6.0	V	
	GVDD		2.5	-	5.0	V	
Logic power supply	VDD	Ta= 25°C	1.4	1.5	1.6	V	*7
Reference Voltage	VREF	Ta= 25°C	1.9	2.0	2.1	V	*7
Logic Input voltage, high	V <sub>IH</sub>		0.7*VDD3	-	VDD3	V	*2
Logic Input voltage, low	V <sub>IL</sub>		0	-	0.3*VDD3	V	*2
Logic output voltage, high	V <sub>OH</sub>	I <sub>OH</sub> = -0.5mA	0.8*VDD3	-	VDD3	V	*3
Logic output voltage, low	V <sub>OL</sub>	I <sub>OL</sub> = 0.5mA	0.0	-	0.2*VDD3	V	*3
Leakage current, input	I <sub>IL</sub>	VIN = VSS3 or VDD3	-1.0		1.0	uA	*2
Leakage current, output	I <sub>OL</sub>	VIN = VSS3 or VDD3	-3.0		3.0	uA	*3
Operating frequency	Fosc	Frame freq. = 60 Hz Display line= 320 Ta= 25°C	9.5	10.0	10.5	MHz	*4
Input voltage to the 1 <sup>st</sup> Booster	VCI1		1.35	-	3.0	V	*5
Power efficiency of the 1 <sup>st</sup> Booster	η <sub>AVDD</sub>	Load current= 4mA	90	95	-	%	
Power efficiency of the 2 <sup>nd</sup> Booster	η <sub>VGH</sub>	Load current= 100uA	90	95	-	%	
Power efficiency of the 3 <sup>rd</sup> Booster	η <sub>VGL</sub>	Load current= 100uA	90	95	-	%	
Power efficiency of the 4 <sup>th</sup> Booster	η <sub>VCL</sub>	Load current= 300uA	90	95	-	%	
Current consumption during normal operation	IVDD3	No load, Ta= 25 °C	-	-	850	uA	*6
	IVCI	VCI=3V, Frame(f)=60Hz	-	-	8	mA	-
Current consumption during Sleep-In mode	IVDD3 <sub>SI</sub>	Supplied : VDD3, VCI,	-	-	25	uA	-
	IVCI <sub>SI</sub>	VSS3, Ta = 25 °C	-	-	5	uA	-



Current consumption during Deep-Standby mode	IVDD3 <sub>DS</sub>	Supplied : VDD3, VCI, VSS3, Ta = 25 °C	-	-	5	uA	-
	IVCI <sub>DS</sub>		-	-	5	uA	-

Note1. VSS3 = 0V.

Note2. Signals under consideration; CSX, RDX, WRX, DB0 to DB23, and RESX

Note3. Signals under consideration; DB0 to DB23

Note4. Target frame frequency = 60 Hz, Display line = 320, Back porch = 8, Front porch = 8, RTN4-0 = "10110", CRTN4-0 = "10110"

(Fosc can be observed indirectly by measuring CL1 pad (Fosc / (22x22))

Note5. Practical VCI1 range is over 2.25V. VCI1 under 2.25V is used only for power-up period.

Note6. CPU access is inactive. MIE function is inactive.

Note7. VDD and VREF are internally generated voltage outputs. Do not apply external power supply at these pins in normal operation.

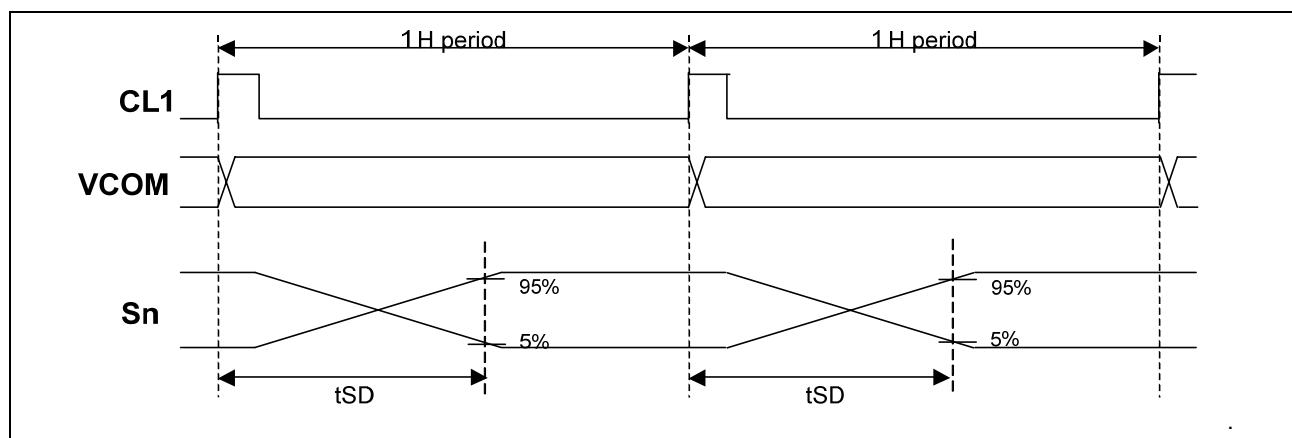
Note8. VGH should be lower than 16.5V except MTP programming session. In case of MTP programming, VGH can be set over 16.5V for a short period such as 100 ~ 200msec.

**Table 15. DC characteristics for LCD driver outputs (TYP: VCI=VDD3=3.0V, Ta=25°C)**

Characteristic	Symbol	Condition	MIN	TYP	MAX	Unit	Note
On resistance of Gate driver output	R <sub>onvgh</sub>	VGH = 6.3V VGL = -6.3V	-	-	3.0	kΩ	-
	R <sub>onvgl</sub>		-	-	3.0	kΩ	-
On resistance of source driver output	R <sub>onp</sub>	AVDD = 4.5V AVSS = 0V	-	-	20	kΩ	-
	R <sub>onn</sub>		-	-	20	kΩ	-
On resistance of binary driver Output	R <sub>onpb</sub>	GVDD = 4.5V AVSS = 0V	-	-	300	kΩ	-
	R <sub>onnb</sub>		-	-	300	kΩ	-
Output voltage deviation (Mean value) AVDD=5.0V, GDD=4.5V	ΔV <sub>O</sub>	AVDD-0.8V≤V <sub>SO</sub>	-	-	±55	mV	*1
		0.8V<V <sub>SO</sub> < AVDD-0.8V	-	-	±25	mV	*1
		V <sub>SO</sub> ≤0.8V	-	-	±55	mV	*1
Delay, source driver	t <sub>SD</sub>	AVDD = 5.5V GVDD = 5V SAP = '0011'	-	-	25.8	us	*2

Note1. VSO is the output voltage of analog output pads; S1 through S720

Note2. t<sub>SD</sub> : LCD Source driver delay.



**Figure 8. LCD source driver delay**

## 2.3. AC CHARACTERISTICS

### 2.3.1. Parallel Interface Characteristics (80-series MCU)

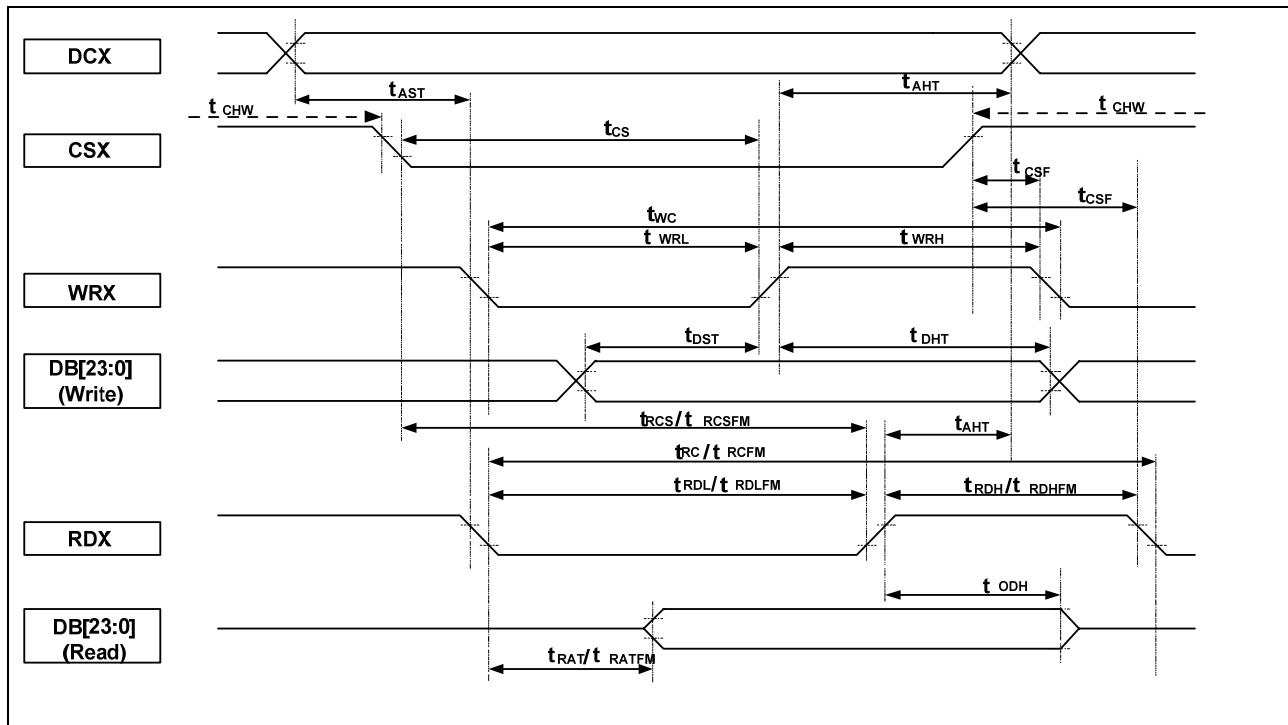


Figure 9. MCU 80 interface AC characteristics

Table 16. MCU 80 interface AC characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DCX	tAST	Address setup time	0	-	ns	
	tAHT	Address hold time (Write/Read)	10	-	ns	
CSX	tCHW	Chip select "H" pulse width	0	-	ns	
	tCS	Chip select setup time (Write)	15	-	ns	
	tRCS	Chip select setup time (Read ID)	45	-	ns	
	tRCSFM	Chip select setup time (Read FM)	355	-	ns	
	tCSF	Chip select wait time (Write/Read)	10	-	ns	
WRX	tWC	Write cycle	66	-	ns	
	tWRH	Control pulse "H" duration	15	-	ns	
	tWRL	Control pulse "L" duration	15	-	ns	
RDX(ID)	tRC	Read cycle (ID)	160	-	ns	
	tRDH	Control pulse "H" duration (ID)	90	-	ns	When read ID data
	tRDL	Control pulse "L" duration (ID)	45	-	ns	
RDX(FM)	tRCFM	Read cycle (FM)	450	-	ns	When read from the



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
	tRDHFM	Control pulse "H" duration (FM)	90	-	ns	frame memory
	tRDLFM	Control pulse "L" duration (FM)	355	-	ns	
DB[23:0]	tDST	Data setup time	10	-	ns	For the maximum CL=30pF,
	tDHT	Data hold time	10	-	ns	
	tRAT	Read access time (ID)	-	40	ns	For the minimum CL=8pF
	tRATFM	Read access time (FM)	-	340	ns	
	tODH	Output disable time	20	80	ns	

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Note1. The rise and fall times of input signals (tr &amp; tf) are less than 15 ns.

Note2. tRAT and tODH timings are based on 20% to 80 % of VDD3-GND.

Note3. Other timings are based on 30% to 70% of VDD3-GND.

Note4. tWRL and tRDL are related with an interval in which CSX="L" and WRX, RDX="L" overlap.

Note5. DCX timing is related with an interval in which CSX="L" and WRX, RDX="L" overlap.

### 2.3.2. Serial Interface Characteristics (3-wire/ 9-bit Serial Interface)

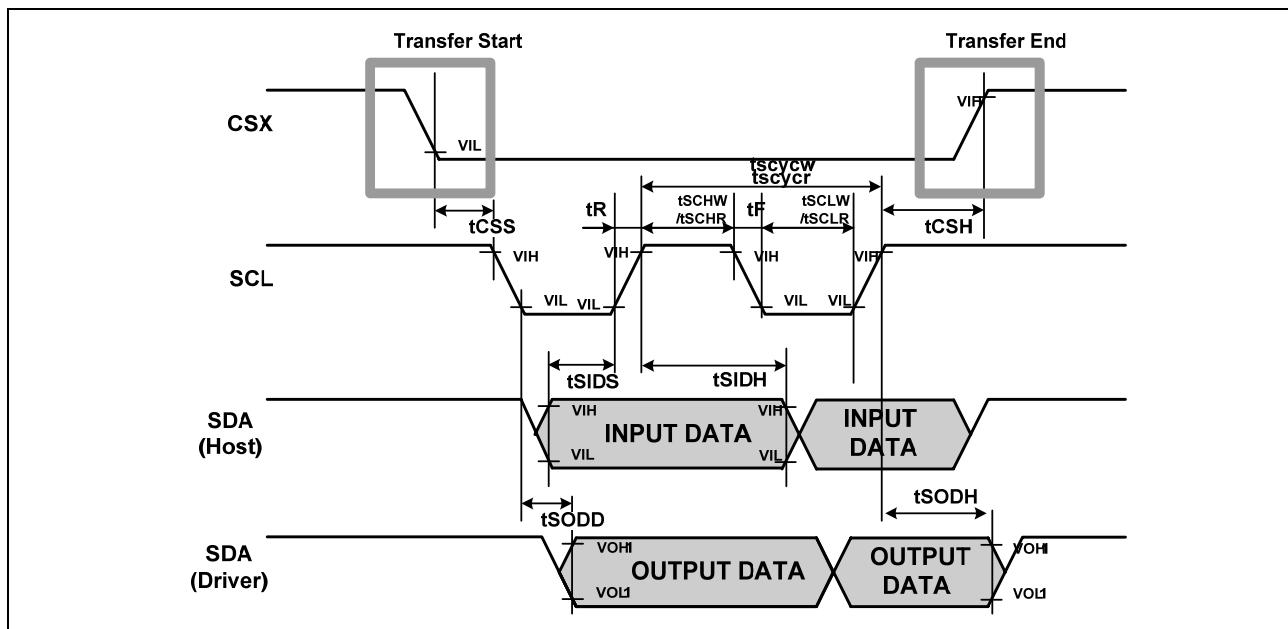


Figure 10. 3- wire 9bit Serial interface characteristics

Table 17. Serial interface AC characteristics(3-wire 9bit)

Characteristic	Symbol	specification		Unit
		Min.	Max.	
Serial clock write cycle time	tscycw	66		ns
Serial clock read cycle time	tscycr	150		ns
Serial clock rise / fall time	tR, tF		15	ns
Pulse width high for write	tSCHW	15		ns
Pulse width high for read	tSCHR	60		ns
Pulse width low for write	tSCLW	15		ns
Pulse width low for read	tSCLR	60		ns
Chip Select setup time	tCSS	15		ns
Chip Select hold time	tCSH	15		ns
Serial input data setup time	tSIDS	10		ns
Serial input data hold time	tSIDH	10		ns
Serial output data delay time	tSODD	10	50	ns
Serial output data hold time	tSODH	15	50	ns

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

### 2.3.3. Serial Interface Characteristics (4-wire/ 8-bit Serial Interface)

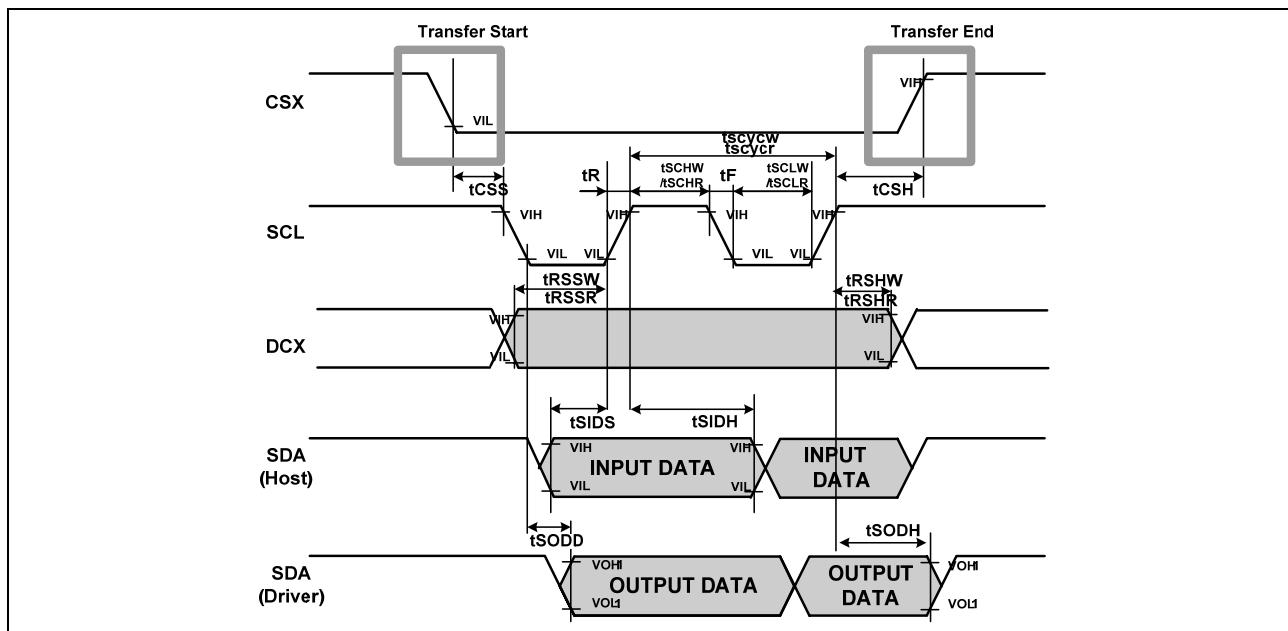


Figure 11. 4 wire 8bit Serial interface characteristics

Table 18. Serial interface AC characteristics(4-wire 8bit)

Characteristic	Symbol	specification		Unit
		Min.	Max.	
Serial clock write cycle time	tscycw	66		ns
Serial clock read cycle time	tscycr	150		ns
Serial clock rise / fall time	tR, tF		15	ns
Pulse width high for write	tSCHW	15		ns
Pulse width high for read	tSCHR	60		ns
Pulse width low for write	tSCLW	15		ns
Pulse width low for read	tSCLR	60		ns
Chip Select setup time	tCSS	15		ns
Chip Select hold time	tCSH	15		ns
RS Setup time for write	tRSSW	15		ns
RS Setup time for read	tRSSR	60		ns
RS hold time for write	tRSHW	15		ns
RS hold time for read	tRSHR	60		ns
Serial input data setup time	tSIDS	10		ns
Serial input data hold time	tSIDH	10		ns
Serial output data delay time	tSODD	10	50	ns
Serial output data hold time	tSODH	15	50	ns

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

### 2.3.4. RGB Interface Characteristics

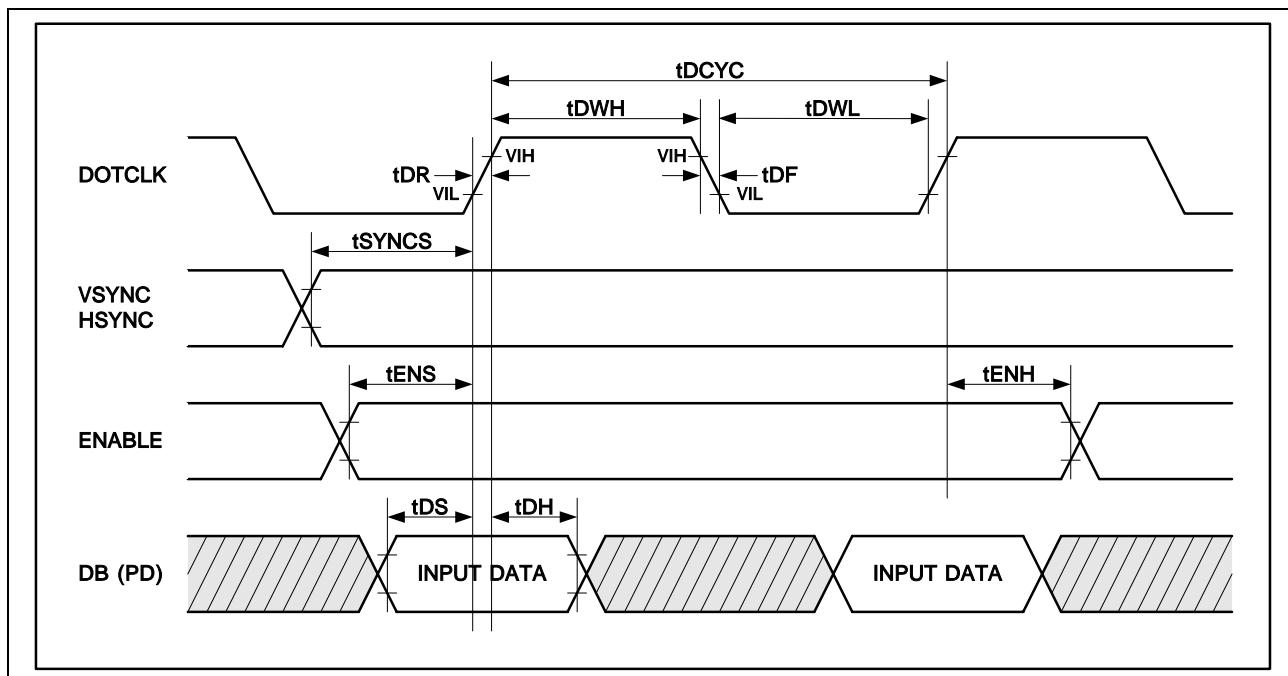


Figure 12. RGB interface characteristics

Table 19. RGB interface AC characteristics

Parameter	Description	24/18/16 bit		8/6 bit		Unit
		Min	Max	Min	Max	
tDCYC	DOTCLK period	100	-	60	-	ns
tDWL	DOTCLK pulse width low	45	-	25	-	ns
tDWH	DOTCLK pulse width high	45	-	25	-	ns
tDR / tDF	DOTCLK rising / falling time	-	10	-	10	ns
tSYNCS	VSYNC, HSYNC setup	30	-	25	-	ns
tENS	ENABLE setup	50	-	20	-	ns
tENH	ENABLE hold	50	-	20	-	ns
tDS	Input Data setup	50	-	20	-	ns
tDH	Input Data hold	50	-	20	-	ns

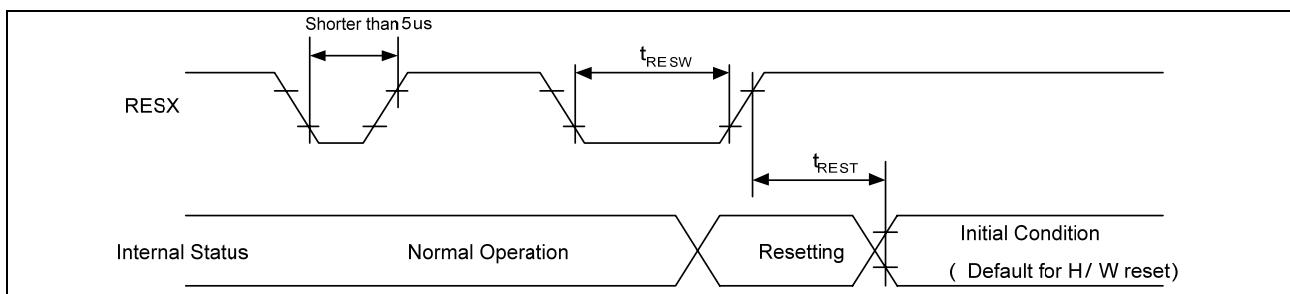
(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Note1. VSYNC Low Pulse Width ≥ 1H

Note2. HSYNC Low Pulse Width ≥ 1 DOTCLK (24/18/16 bit I/F)

Note3. HSYNC Low Pulse Width ≥ 3 DOTCLK (8/6 bit I/F)

### 2.3.5. RESX Signal



**Figure 13.** Reset input timing

**Table 20. Reset Input Timing**

Symbol	Parameter	Pad	Min	Typ	Max	Unit	Note
tRESW	1) Reset low pulse width	RESX	10	-	-	μs	-
tREST	2) Reset completion time	RESX	-	-	5	ms	Reset during Sleep In mode
		RESX		-	120	ms	Reset during Sleep Out mode

(Ta = -40 ~ 85 °C, VCI = 2.3 ~ 3.3V, VDD3 = 1.65 ~ 3.3V)

Note1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

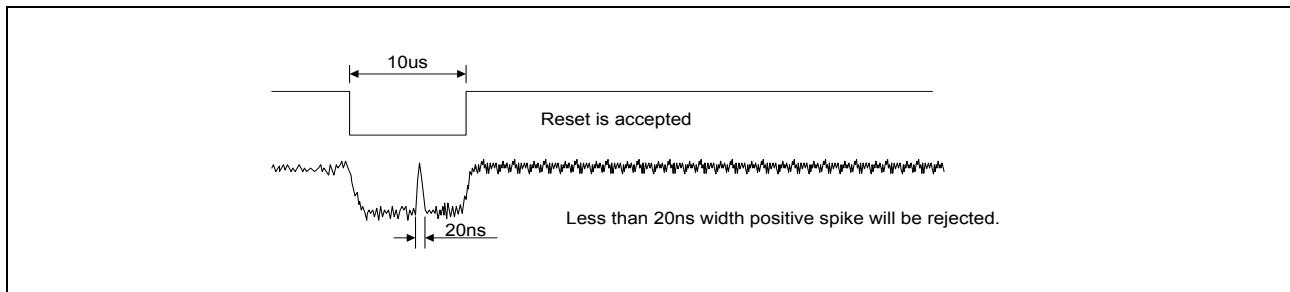
**Table 21. RESX pulse**

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset Start

Note2. During the reset period, the display will be blanked (The display is entering blanking sequence, for which the maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains in the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

Note3. During Reset Completion Time, ID1, ID2, ID3 and VCM, VML, GVD Offset value in MTP will be latched to the internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note4. Spike Rejection also applies during a valid reset pulse as shown below:



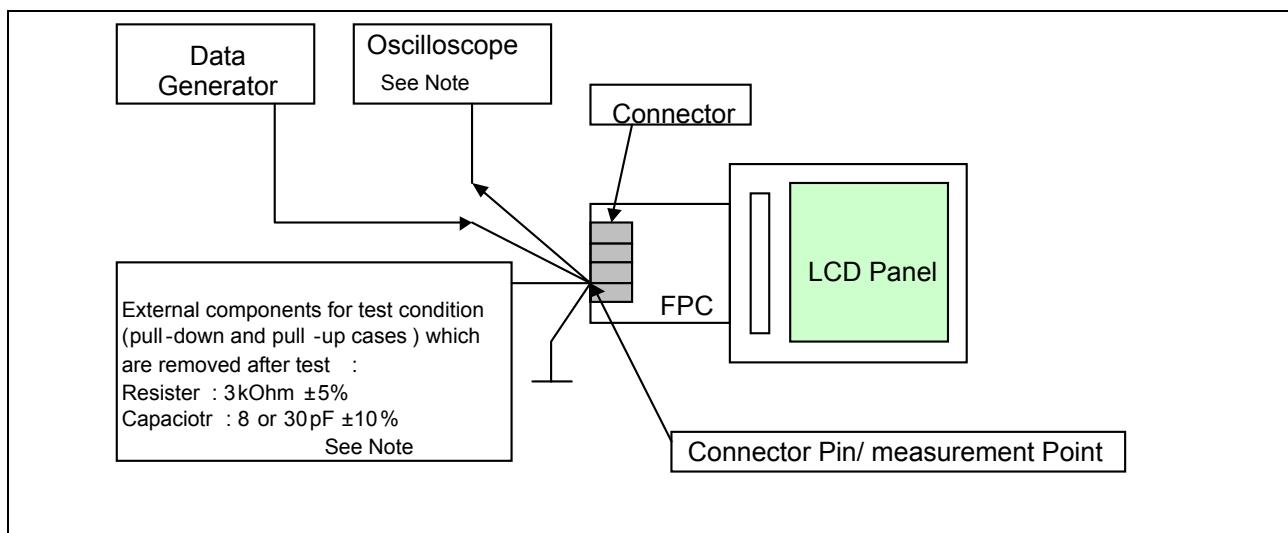
**Figure 14.** RESX pulse

Note5. It is necessary to wait for 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

### 2.3.6. Measurement Conditions

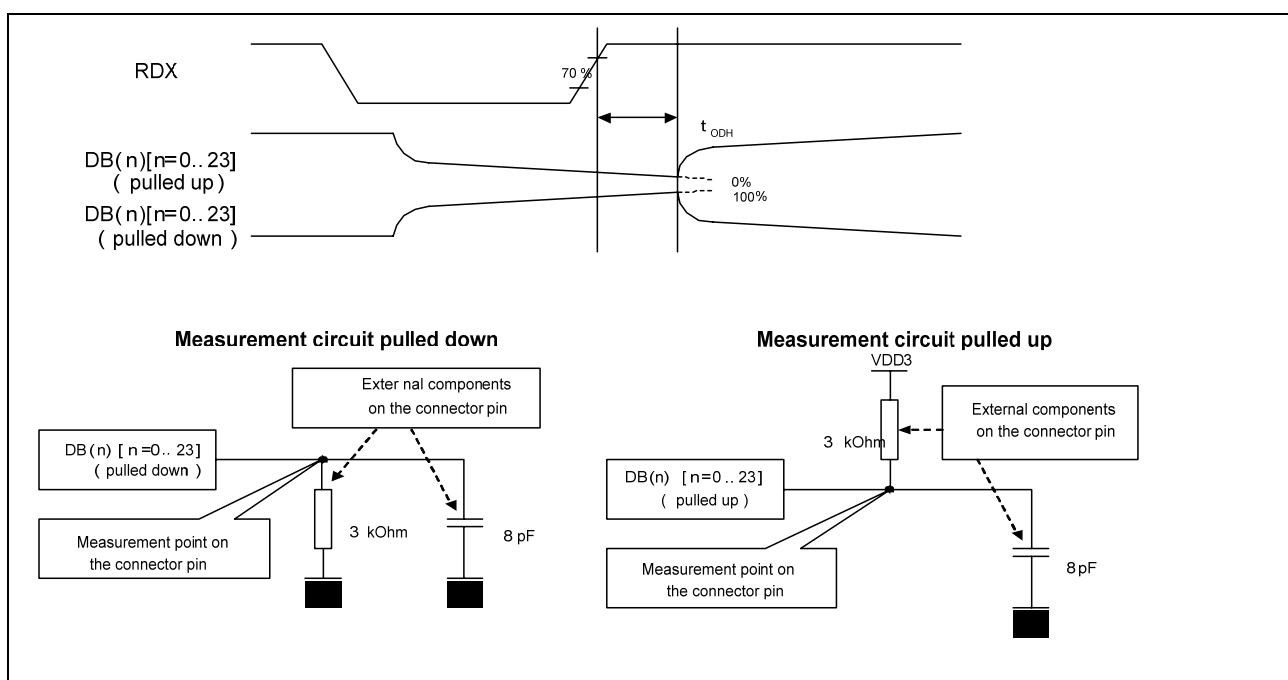
The measurement conditions shown in this section is provided for a reference purpose to the module makers. The condition for the actual IC measurement will be determined after the consideration of a practical manufacturing environment of mass production.

#### 2.3.6.1. tRATFM, tODH Measurement Condition



**Figure 15. Measurement condition set-up of MCU interface at a module level**

Note. Capacitances and resistances of the oscilloscope probe must be included an external components in these measurements



**Figure 16. Minimum value measurement of MCU interface**

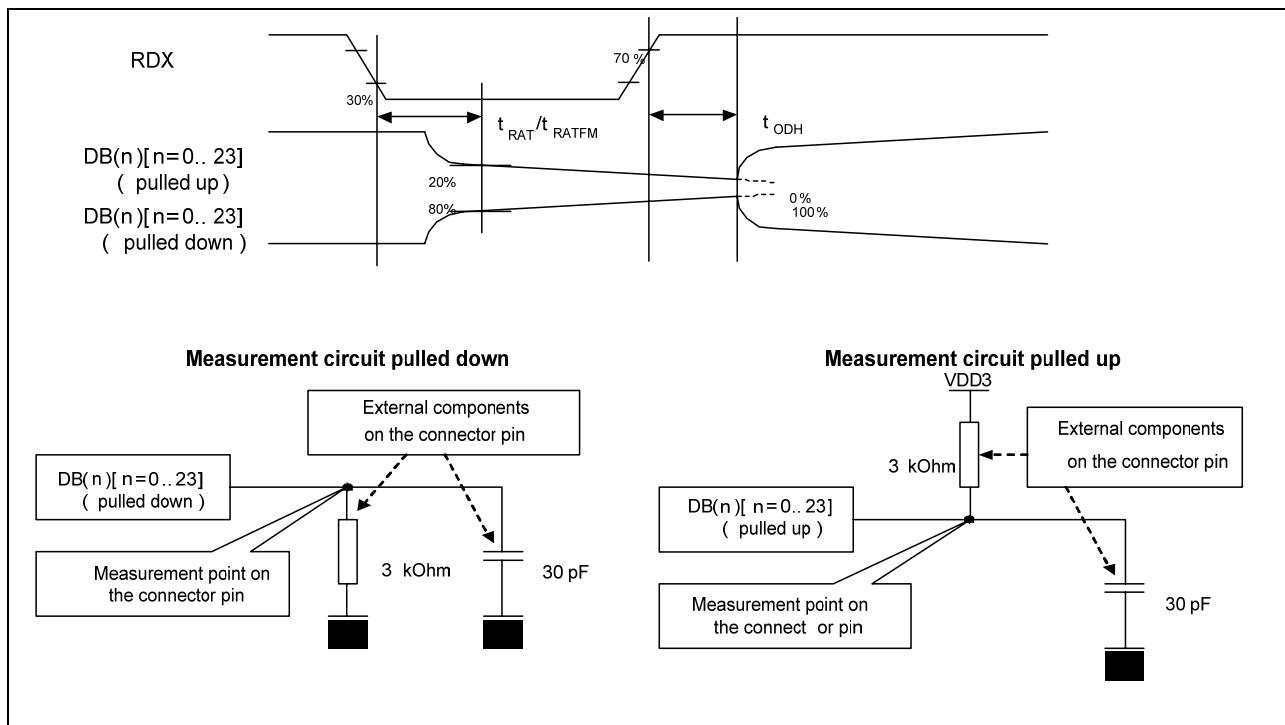


Figure 17. Maximum value measurement of MCU interface

## 2.3.6.2. tSODD, tSODH Measurement Condition

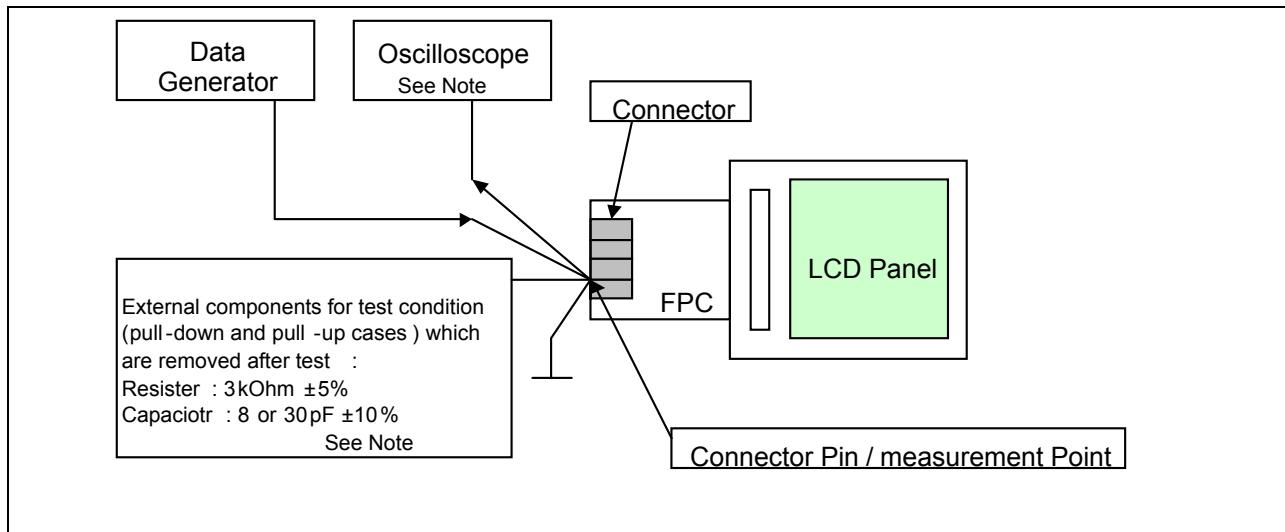


Figure 18. Measurement condition set-up of SPI at a module level

Note. Capacitances and resistances of the oscilloscope probe must be included an external components in these measurements

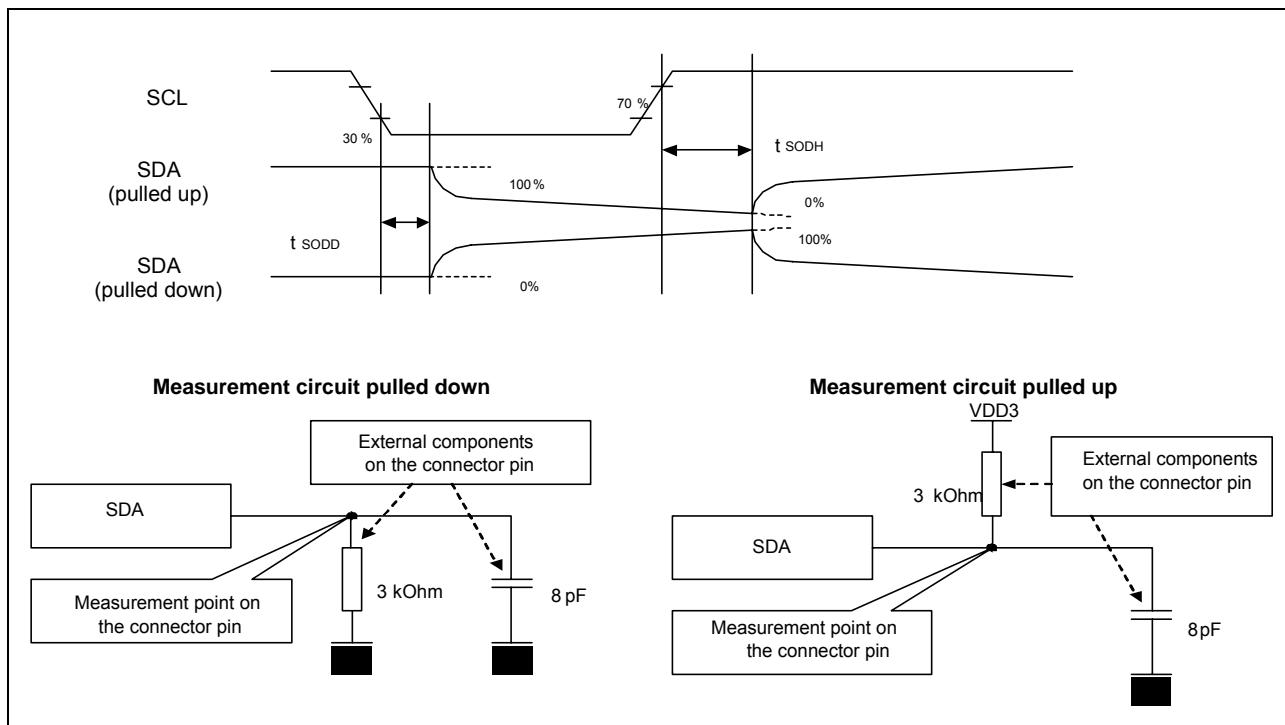


Figure 19. Minimum value measurement of SPI

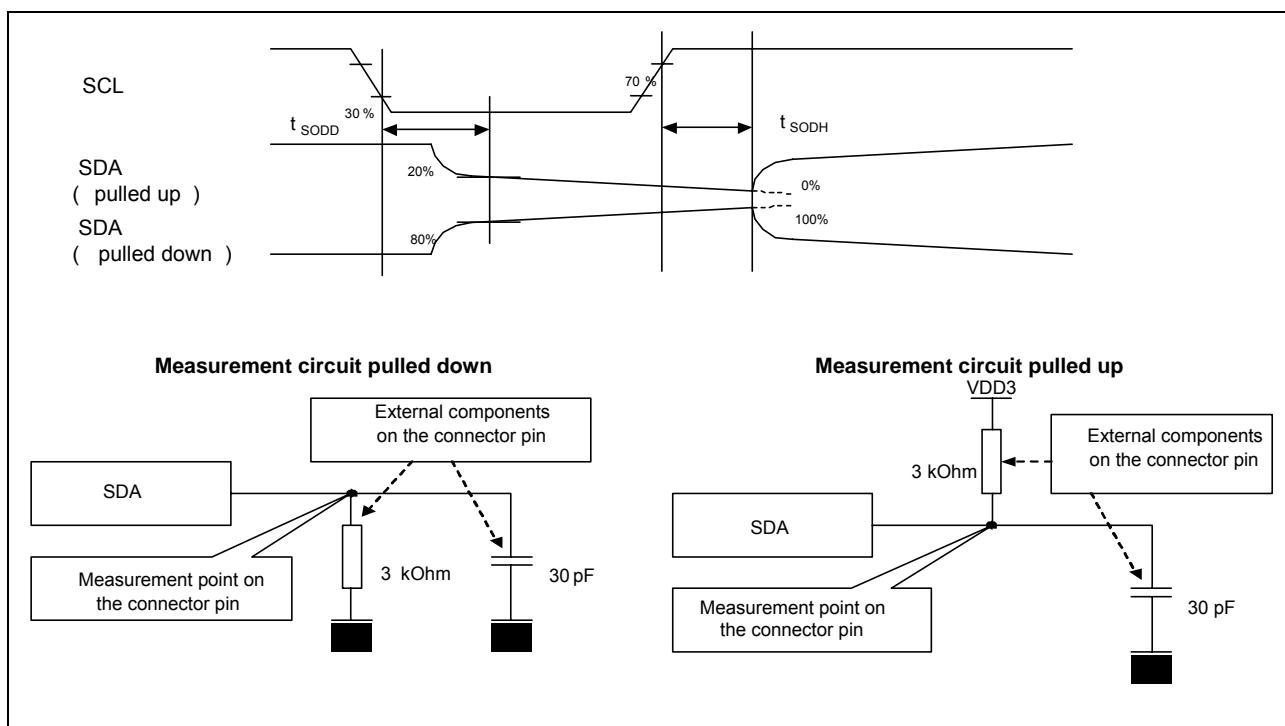


Figure 20. Maximum value measurement of SPI

## CHAPTER 3

# INTERFACE

- 3.1 MPU Interface
- 3.2 Display Module Data Color Coding
- 3.3 RGB Interface
- 3.4 VSYNC Interface

# 3 INTERFACE

## 3.1. MPU INTERFACE

### 3.1.1. Interface Type Selection

While the driver IC is used to parallel interface, it transfers commands, parameters and display data between the driver IC and MPU using a bi-directional data line up to 24 bits of bus width. The interface which communicates with MPU is selected by using a combination of IM [3:0] pins.

**Table 22. Interface type selection**

Mode	IM3	IM2	IM1	IM0
80 MCU 24-bit Parallel I/F Type I	1	0	0	0
80 MCU 16-bit Parallel I/F Type I	0	0	0	0
80 MCU 8-bit Parallel I/F Type I	0	0	0	1
80 MCU 18-bit Parallel I/F Type I	0	1	0	0
80 MCU 24-bit Parallel I/F Type II	1	0	0	1
80 MCU 16-bit Parallel I/F Type II	0	0	1	0
80 MCU 8-bit Parallel I/F Type II	0	0	1	1
80 MCU 18-bit Parallel I/F Type II	1	0	1	0
80 MCU 9-bit Parallel I/F	1	0	1	1
3-wire 9bit Data Serial I/F	0	1	1	0
4-wire 8bit Data Serial I/F	0	1	1	1

### 3.1.2. Pad Description of MPU Interface

MPU interface of the S6D04M0 is changed according to the bus width used. The pin assignments are listed in the table below. The unused input pads have to connect to VSS or VDD3.

When CSX is inactive as high, DB23 to DB0 are placed in the high-impedance state internally.

#### 3.1.2.1. 80-Series MCU Parallel Interface

**Table 23. Interface signal description in case of MCU I/F**

Pad signal	Description																			
CSX	Chip select control signal																			
DCX	Data bus transfers a command when DCX is low. Data bus transfers parameters or display data when DCX is high.																			
RDX	Read control signal When RDX is low, the data bus is held on output state.																			
WRX	Write control signal Data is latched on the rising edge of WRX.																			
DB23 to DB0	Data bus																			
	<table border="1"> <thead> <tr> <th>Mode</th><th>DB pads</th></tr> </thead> <tbody> <tr> <td>80 MCU 24-bit Parallel I/F Type I</td><td>DB23-DB0 : 24-bit data</td></tr> <tr> <td>80 MCU 16-bit Parallel I/F Type I</td><td>DB23-DB16 : unused DB15-DB0 : 16-bit data</td></tr> <tr> <td>80 MCU 8-bit Parallel I/F Type I</td><td>DB23-DB8 : unused DB7-DB0 : 8-bit data</td></tr> <tr> <td>80 MCU 18-bit Parallel I/F Type I</td><td>DB23-DB18 : unused DB17-DB0 : 18-bit data</td></tr> <tr> <td>80 MCU 24-bit Parallel I/F Type II</td><td>DB23-DB0 : 24-bit data</td></tr> <tr> <td>80 MCU 16-bit Parallel I/F Type II</td><td>DB23-DB18 : unused DB17-DB10 : upper 8-bit data DB9 : unused DB8-DB1 : lower 8-bit data DB0 : unused</td></tr> <tr> <td>80 MCU 8-bit Parallel I/F Type II</td><td>DB23-DB18 : unused DB17-DB10 : 8-bit data DB9-DB0 : unused</td></tr> <tr> <td>80 MCU 18-bit Parallel I/F Type II</td><td>DB23-DB18 : unused DB17-DB0 : 18-bit data</td></tr> <tr> <td>80 MCU 9-bit Parallel I/F</td><td>DB23-DB18: unused DB17-DB9 : 9-bit data</td></tr> </tbody> </table>	Mode	DB pads	80 MCU 24-bit Parallel I/F Type I	DB23-DB0 : 24-bit data	80 MCU 16-bit Parallel I/F Type I	DB23-DB16 : unused DB15-DB0 : 16-bit data	80 MCU 8-bit Parallel I/F Type I	DB23-DB8 : unused DB7-DB0 : 8-bit data	80 MCU 18-bit Parallel I/F Type I	DB23-DB18 : unused DB17-DB0 : 18-bit data	80 MCU 24-bit Parallel I/F Type II	DB23-DB0 : 24-bit data	80 MCU 16-bit Parallel I/F Type II	DB23-DB18 : unused DB17-DB10 : upper 8-bit data DB9 : unused DB8-DB1 : lower 8-bit data DB0 : unused	80 MCU 8-bit Parallel I/F Type II	DB23-DB18 : unused DB17-DB10 : 8-bit data DB9-DB0 : unused	80 MCU 18-bit Parallel I/F Type II	DB23-DB18 : unused DB17-DB0 : 18-bit data	80 MCU 9-bit Parallel I/F
Mode	DB pads																			
80 MCU 24-bit Parallel I/F Type I	DB23-DB0 : 24-bit data																			
80 MCU 16-bit Parallel I/F Type I	DB23-DB16 : unused DB15-DB0 : 16-bit data																			
80 MCU 8-bit Parallel I/F Type I	DB23-DB8 : unused DB7-DB0 : 8-bit data																			
80 MCU 18-bit Parallel I/F Type I	DB23-DB18 : unused DB17-DB0 : 18-bit data																			
80 MCU 24-bit Parallel I/F Type II	DB23-DB0 : 24-bit data																			
80 MCU 16-bit Parallel I/F Type II	DB23-DB18 : unused DB17-DB10 : upper 8-bit data DB9 : unused DB8-DB1 : lower 8-bit data DB0 : unused																			
80 MCU 8-bit Parallel I/F Type II	DB23-DB18 : unused DB17-DB10 : 8-bit data DB9-DB0 : unused																			
80 MCU 18-bit Parallel I/F Type II	DB23-DB18 : unused DB17-DB0 : 18-bit data																			
80 MCU 9-bit Parallel I/F	DB23-DB18: unused DB17-DB9 : 9-bit data																			



		DB8-DB0 : unused
If not used, connect these pads to VDD3 or VSS.		

## 3.1.2.2. 4-wire/8-bit Serial Interface

**Table 24. Interface signals in case of 4-wire/8-bit serial interface.**

Pad signal	Description
CSX	Chip select signal
DCX	Data bus is regarded as a command when DCX is low. Data bus is regarded as a parameter when DCX is high.
SCL (WRX)	Clock signal During write mode, the data is latched on the rising edge of SCL signal.
SDA	Serial Data signal.

## 3.1.2.3. 3-wire/9-bit Serial Interface

**Table 25. Interface signals in case of 3-wire/9-bit serial interface.**

Pad signal	Description
CSX	Chip select signal
SCL (DCX)	Clock signal During write mode, the data is latched on the rising edge of SCL signal.
SDA	Serial Data signal.

### 3.1.3. Sequence of MPU Interface

In 80 MCU 24-bit parallel interfaces, the chip-select CSX (active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write signal, RDX is the parallel data read signal and DB[23:0] is parallel data. The MCU reads the data at the rising edge of RDX signal. The DCX is the data/command flag. When DCX='1', DB[23:0] bits are display RAM data or command parameters. When DCX='0', DB[8:1] bits are commands. The 80-Series bi-directional interface can be used for communication between the micro controller and LCD driver chip. Interface bus width can be selected with IM[3:0].

**Table 26. The function of 80-series parallel interface**

DCX	RDX	WRX	Function
L	1	↑	Write 8-bit command
H	1	↑	Write 8-bit parameter or [80 MCU 24-bit Parallel I/F Type I] Write 24-bit display data (DB23 to DB0) [80 MCU 16-bit Parallel I/F Type I] Write 16-bit display data (DB15 to DB0) [80 MCU 8-bit Parallel I/F Type I] Write 8-bit display data (DB7 to DB0) [80 MCU 18-bit Parallel I/F Type I] Write 18-bit display data (DB17 to DB0) [80 MCU 24-bit Parallel I/F Type II] Write 24-bit display data (DB23 to DB0) [80 MCU 16-bit Parallel I/F Type II] Write 16-bit display data (DB17 to DB10, DB8 to DB1) [80 MCU 8-bit Parallel I/F Type II] Write 8-bit display data (DB17 to DB10) [80 MCU 18-bit Parallel I/F Type II] Write 18-bit display data (DB17 to DB0) [80 MCU 9-bit Parallel I/F] Write 9-bit display data (DB17 to DB9)
H	↑	1	Read 8-bit parameter or Read dummy data (1st output data after read command) or [80 MCU 24-bit Parallel I/F Type I] Read 24-bit display data (DB23 to DB0) [80 MCU 16-bit Parallel I/F Type I] Read 16-bit display data (DB15 to DB0) [80 MCU 8-bit Parallel I/F Type I] Read 8-bit display data (DB7 to DB0)



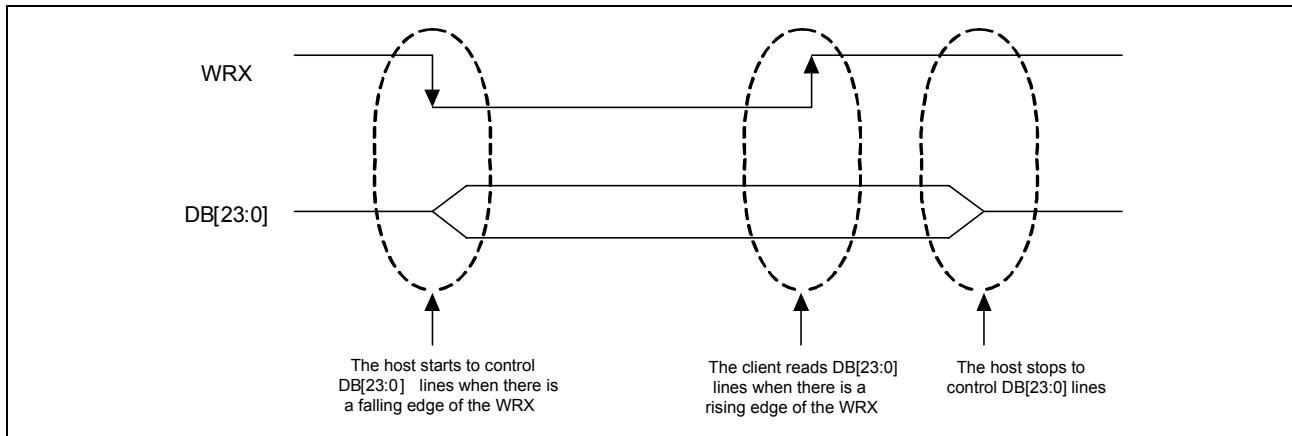
DCX	RDX	WRX	Function
			<p>[80 MCU 18-bit Parallel I/F Type I]            Read 18-bit display data (DB17 to DB0)</p> <p>[80 MCU 24-bit Parallel I/F Type II]            Read 24-bit display data (DB23 to DB0)</p> <p>[80 MCU 16-bit Parallel I/F Type II]            Read 16-bit display data (DB17 to DB10, DB8 to DB1)</p> <p>[80 MCU 8-bit Parallel I/F Type II]            Read 8-bit display data (DB17 to DB10)</p> <p>[80 MCU 18-bit Parallel I/F Type II]            Read 18-bit display data (DB17 to DB0)</p> <p>[80 MCU 9-bit Parallel I/F]            Read 9-bit display data (DB17 to DB9)</p>

Note. ↑ = rising edge

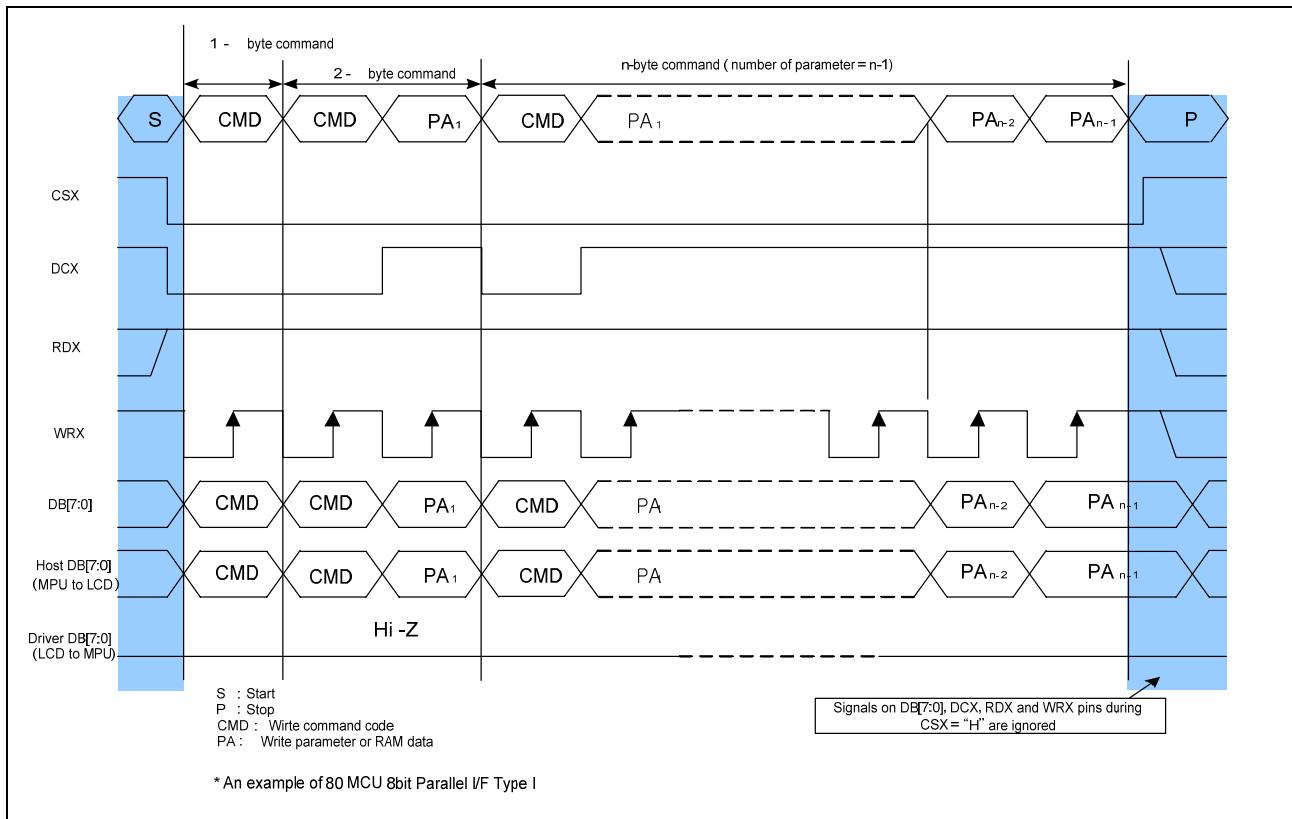


### 3.1.3.1. Write Sequence of MPU Interface

The write cycle means that the host writes information (command or/and data) to the driver IC via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (DCX, RDX, and WRX) and data signals (DB[23:0]). DCX bit is a control signal, which represents the data is a command or a data. The data signals represent command if the control signal is low ('=0') and represent data if the control signal is high ('=1').



**Figure 21. 80-series WRX protocol**

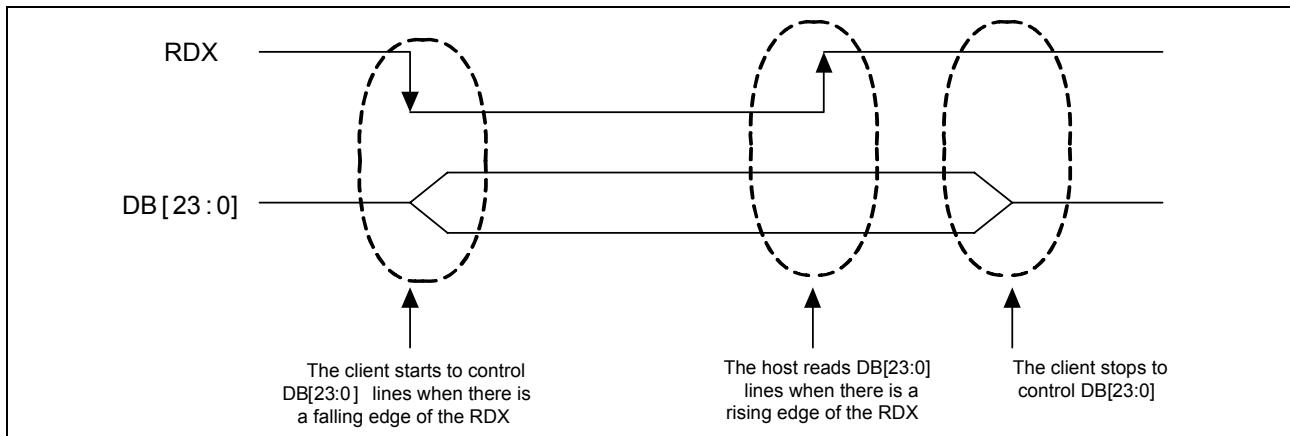


**Figure 22. 80-series Parallel bus protocol, write to register or display RAM**

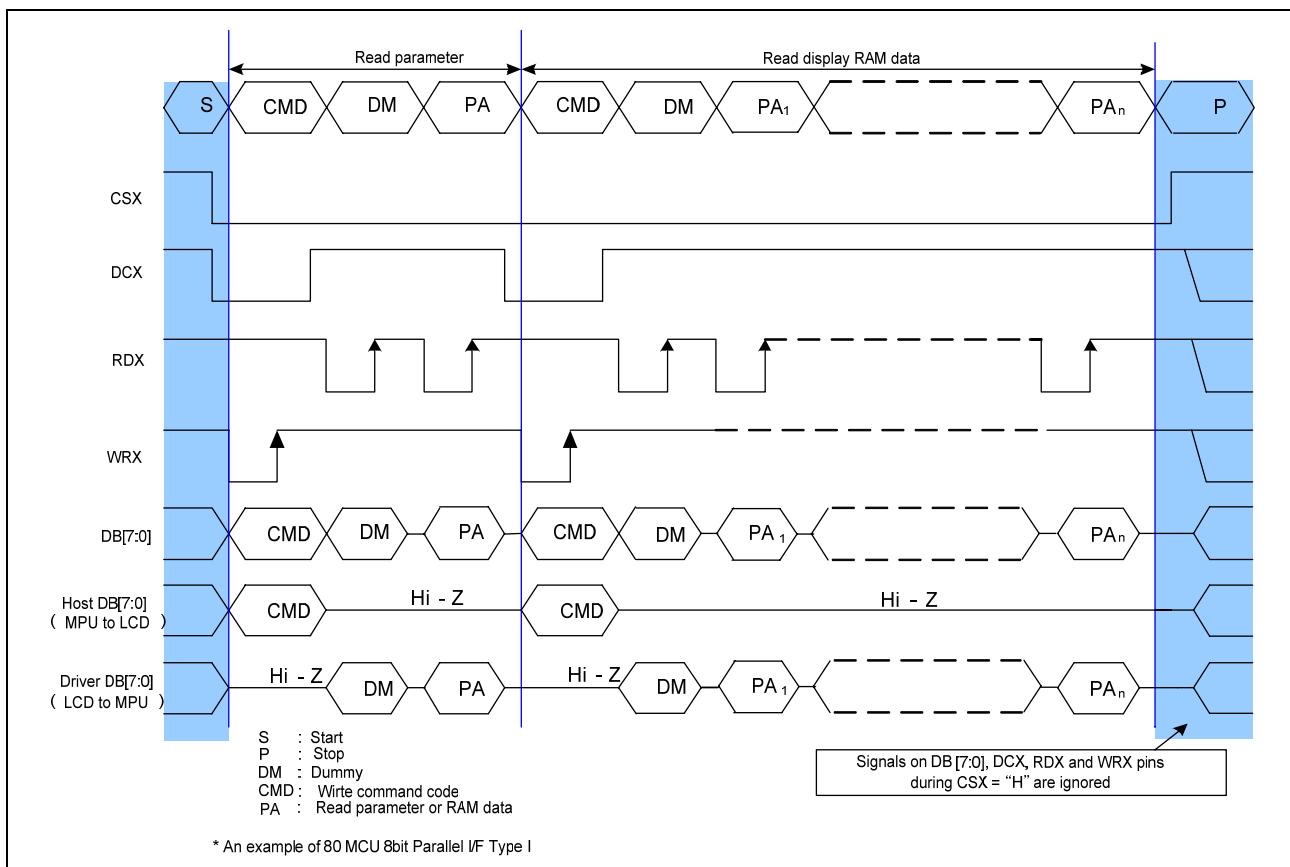
### 3.1.3.2. Read Sequence of MPU Interface

The read cycle (RDX high-low-high sequence) means that the host reads information from driver IC via the interface.

The IC sends data (DB[23:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.



**Figure 23. 80-series RDX protocol**



**Figure 24. 80-series Parallel bus protocol, read from register or display RAM**

### 3.1.4. Sequence of 4-wire/8-bit Serial Interface

The serial interface is 4-wire/8-bit interface for communication between the micro controller and the LCD driver chip. The 4-wire serial use: CSX (chip enable), DCX (Data / Command selection pad), SCL (WRX) and SDA are used for interface with MCU only, so it can be stopped when no communication is necessary.

#### 3.1.4.1. Write Sequence of 4-wire/8-bit Serial Interface

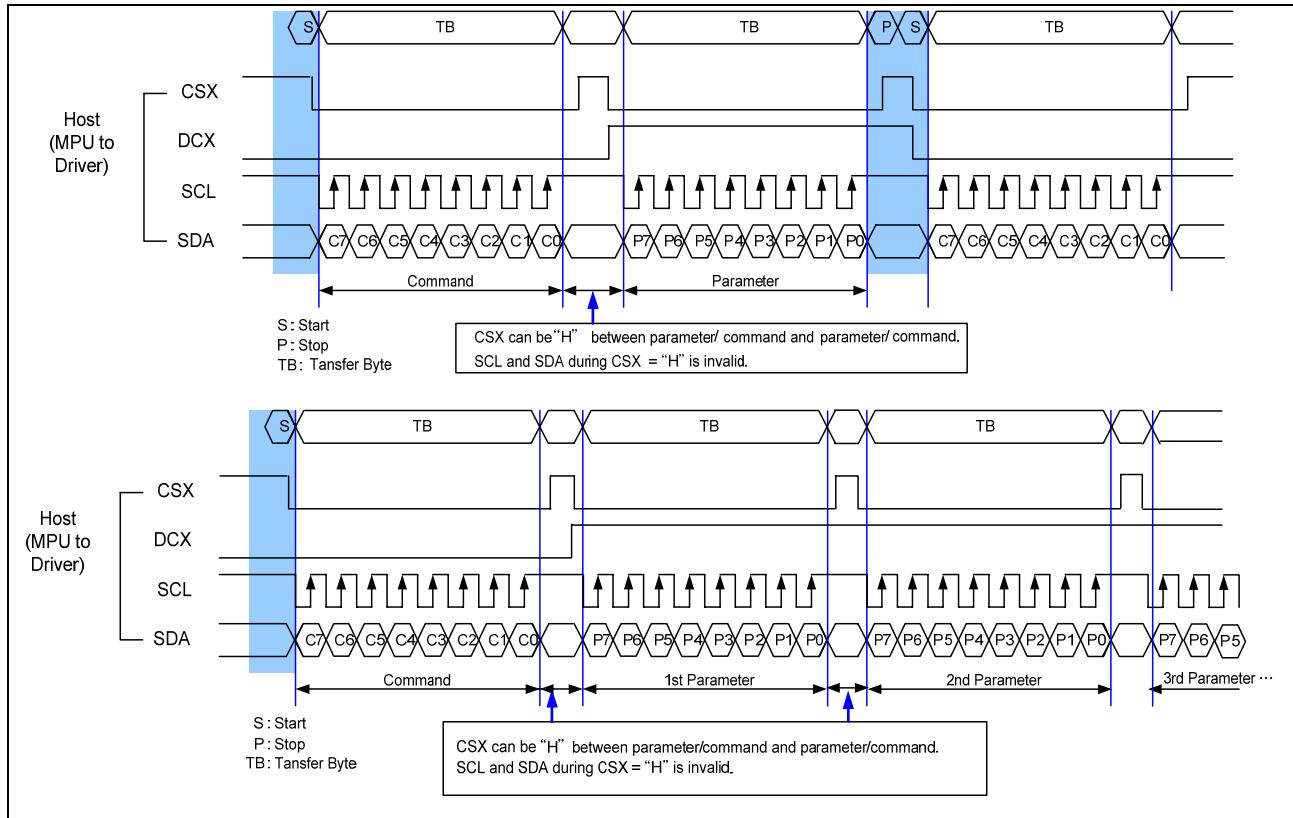


Figure 25. 4-wire/8-bit Data serial interface write mode

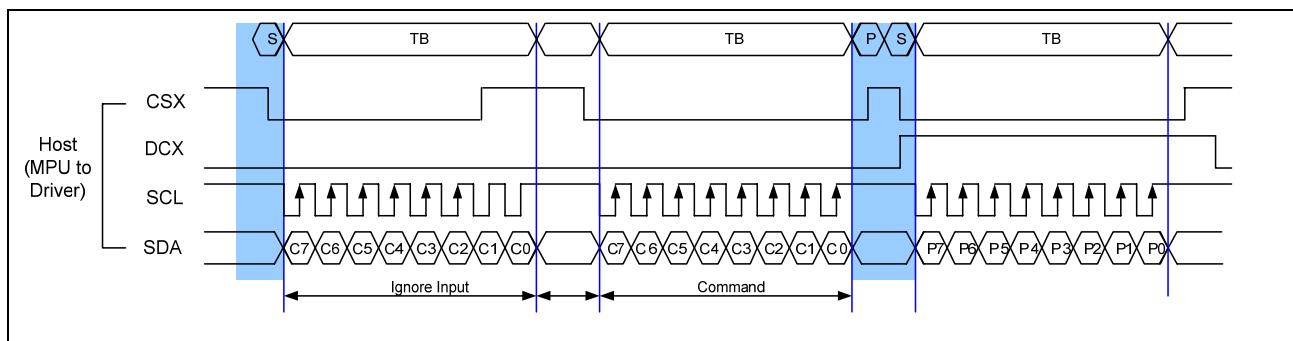


Figure 26. 4-wire/8-bit Data serial interface write mode (CSX='H' during transmission)

## 3.1.4.2. Read Sequence of 4-wire/8-bit Serial Interface

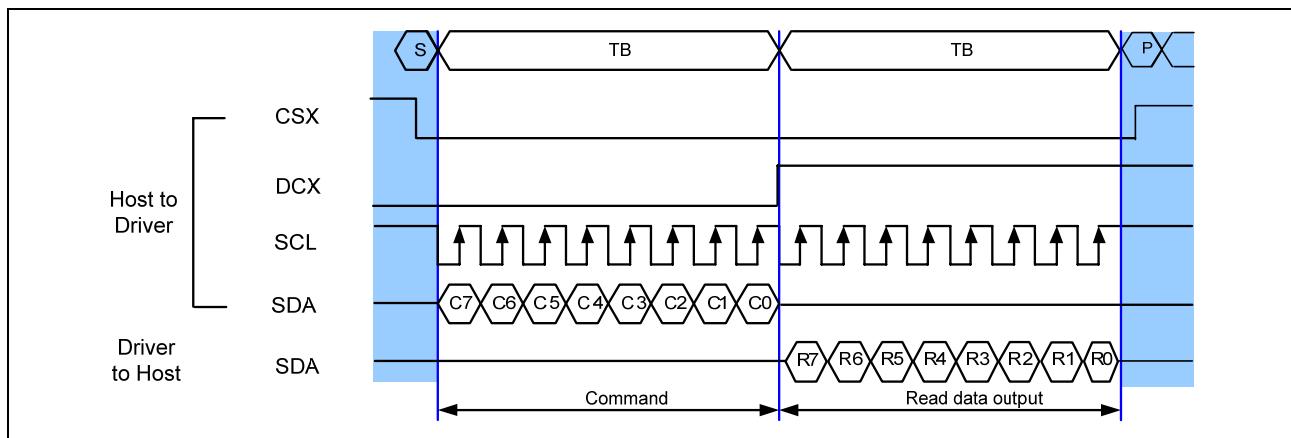


Figure 27. 4-wire/8-bit Data serial interface read 1-byte mode

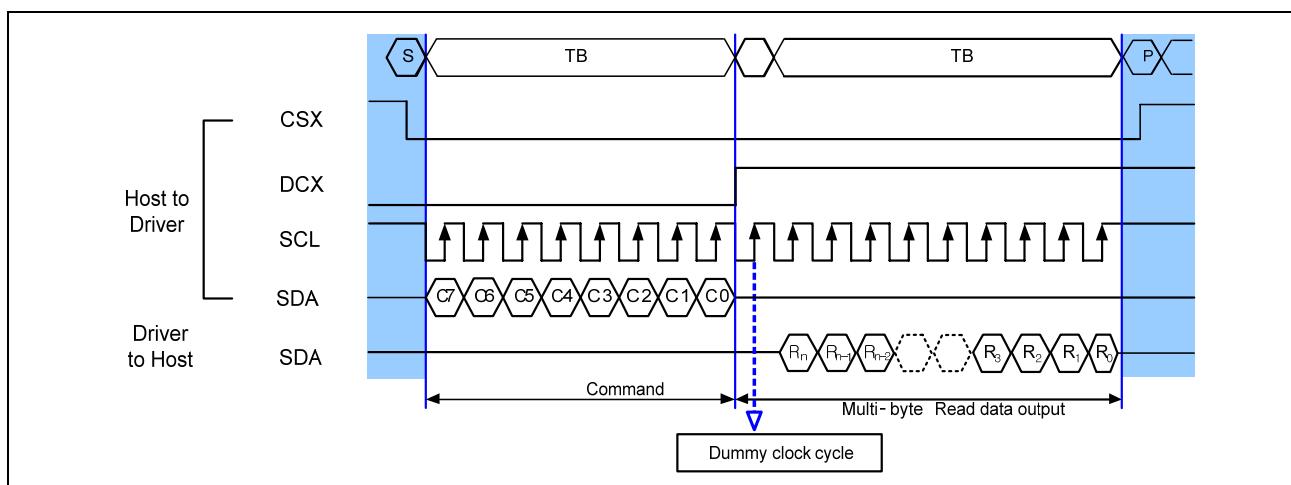
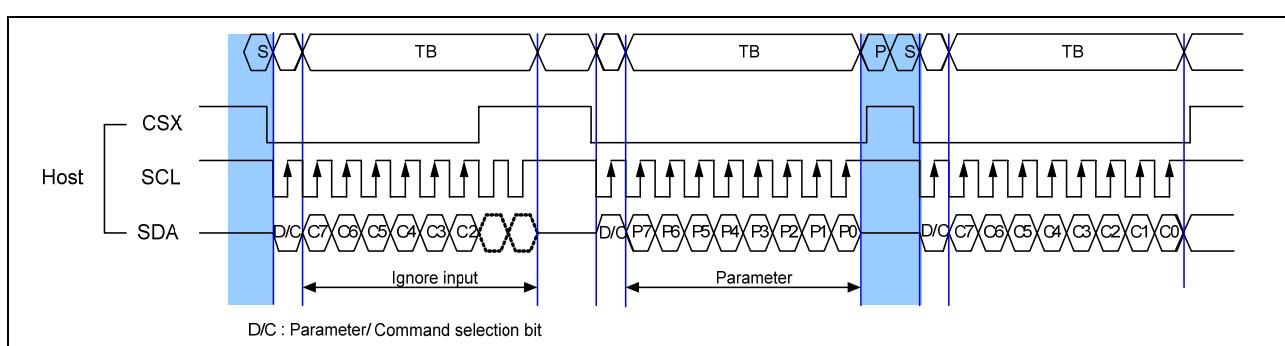
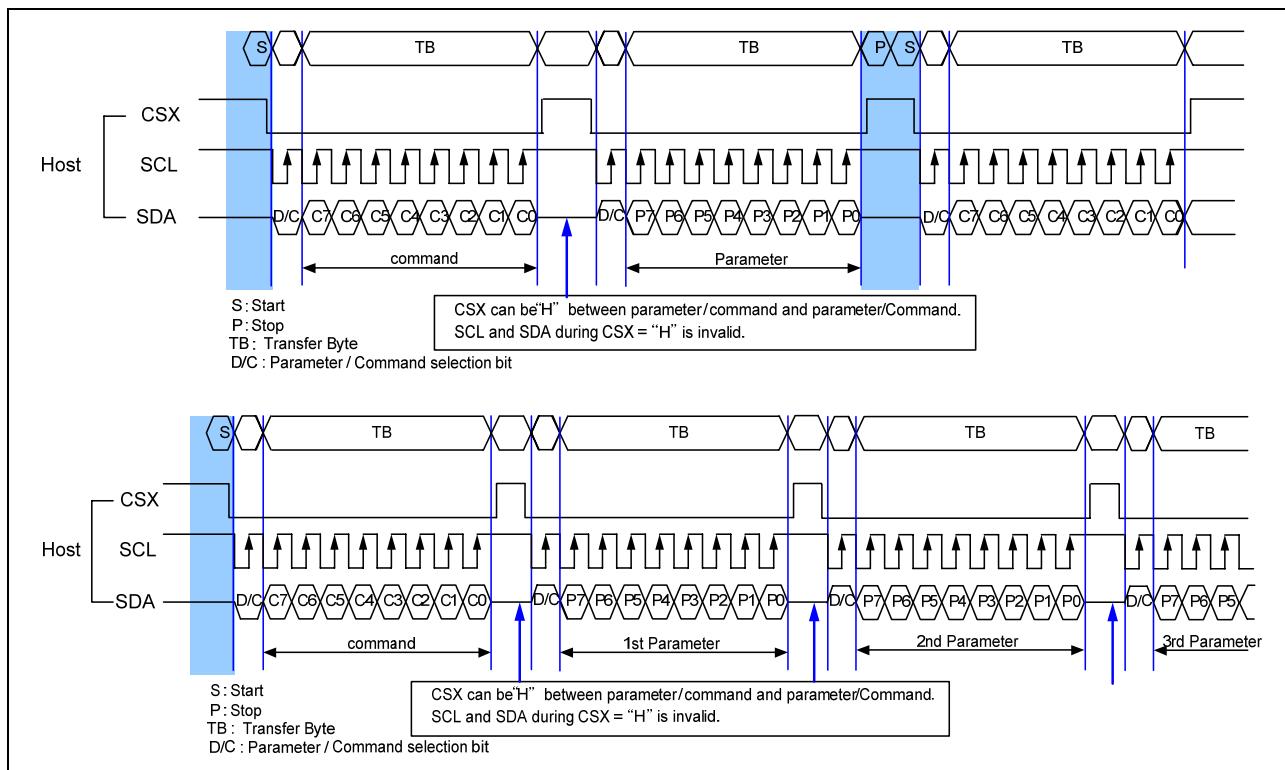


Figure 28. 4-wire/8-bit Data serial interface read multi-byte mode

### 3.1.5. Sequence of 3-wire/9-bit Serial Interface

The serial interface is 3-wire/9-bit interface for communication between the micro controller and the LCD driver chip. The 3-wire serial use: CSX, SCL (DCX) and SDA are used for interface with MCU only, so it can be stopped when no communication is necessary.

#### 3.1.5.1. Write Sequence of 3-wire/9-bit Serial Interface



## 3.1.5.2. Read Sequence of 3-wire/9-bit Serial Interface

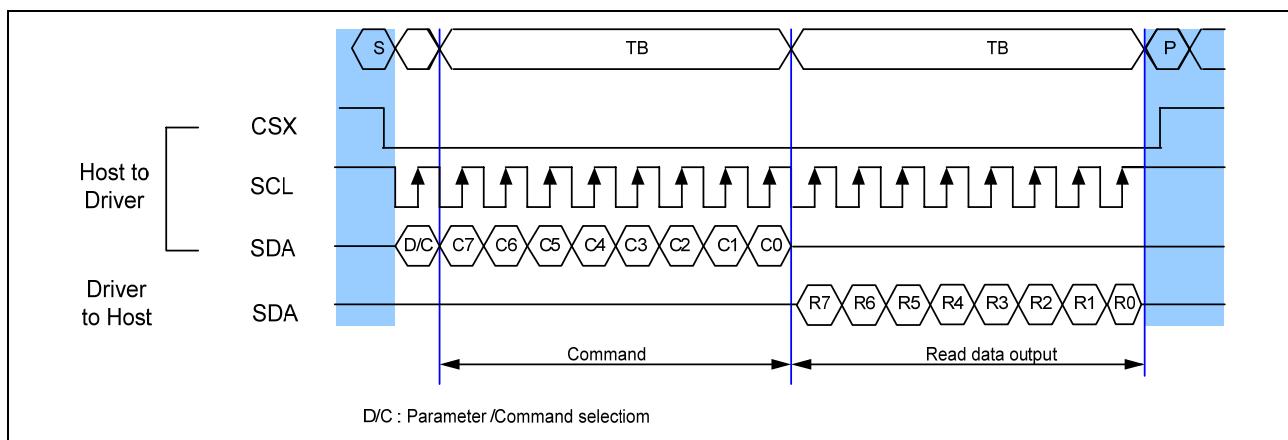


Figure 31. 3-wire/9-bit Data serial interface read 1-byte mode

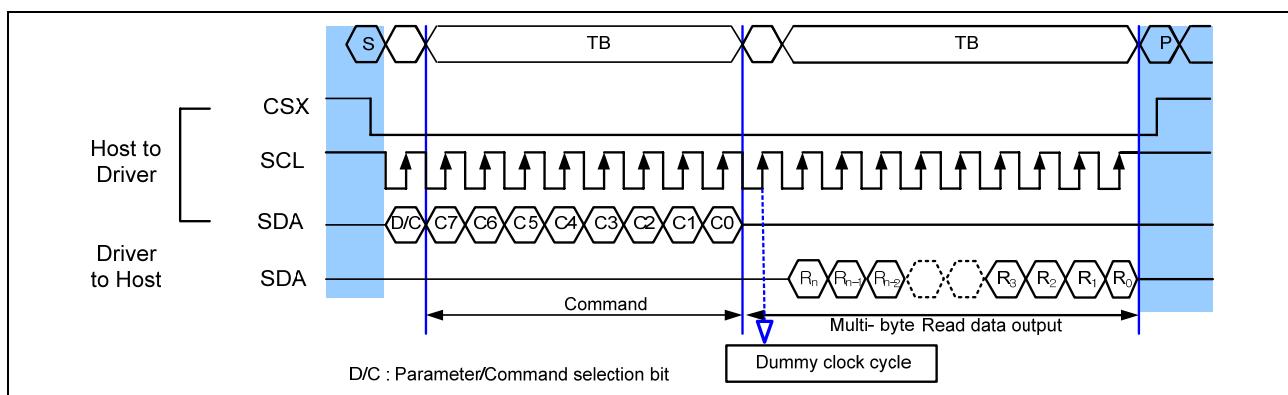


Figure 32. 3-wire/9-bit Data serial interface read multi-byte mode

### 3.1.6. Description of MPU Interface

The parallel interface of the S6D04M0 can communicate with the MCU using 24 bit bidirectional data bus (DB23 to DB0) to transfer command, parameter and display data.

#### 3.1.6.1. Bidirectional Data Bus

The purpose of MCU interface in the S6D04M0 is to communicate with the MCU in a direct connection. If the driver IC is not selected (CSX = L), the data bus (data line) is placed in the high-impedance state to prevent the other driver IC's from adverse effects. When the driver IC is not selected, inputs through the MCU interface (DCX, RDX, and WRX) have no effect. The example below represents the 80 MCU 24bit Parallel interfaces.

**Table 27. Bidirectional data bus description of MCU 24bit type**

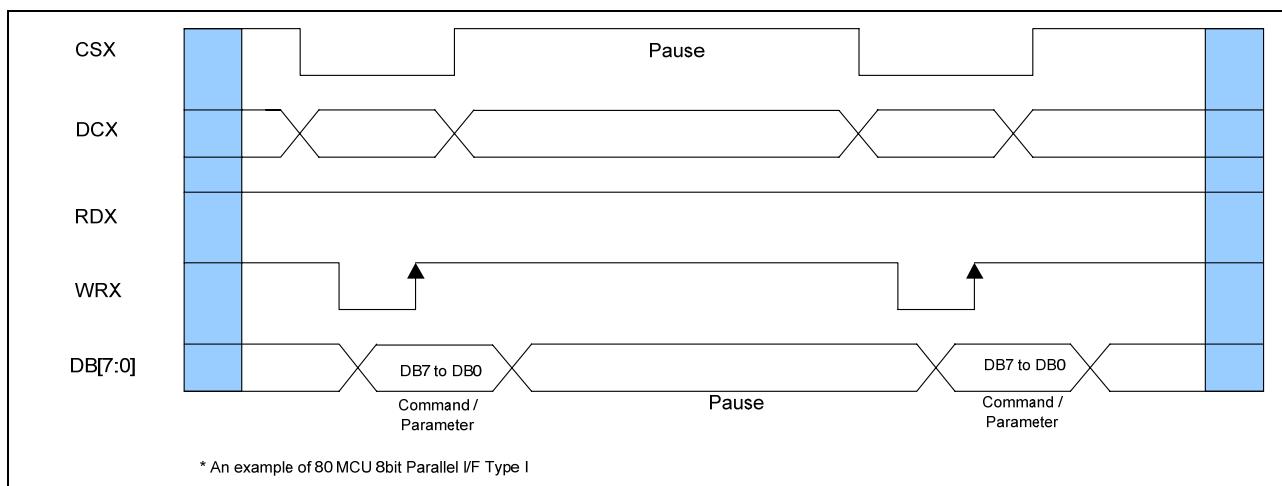
DCX	WRX	RDX	Description
L	↑	1	Command write Commands are input to DB8 to DB1. (In case of Type , Commands are input to DB7 to 0)
H	↑	1	Parameter or display data write Parameters and display data are respectively input to DB8 to DB1 and DB23 to DB0. (In case of Type , Commands are input to DB7 to 0)
H	1	↑	Parameter or display data read Parameters and display data are respectively output to DB8 to DB1 and DB23 to DB0. (In case of Type , Commands are output to DB7 to 0) or dummy data read (1st output data after read command).

### 3.1.6.2. Data Transfer Pause

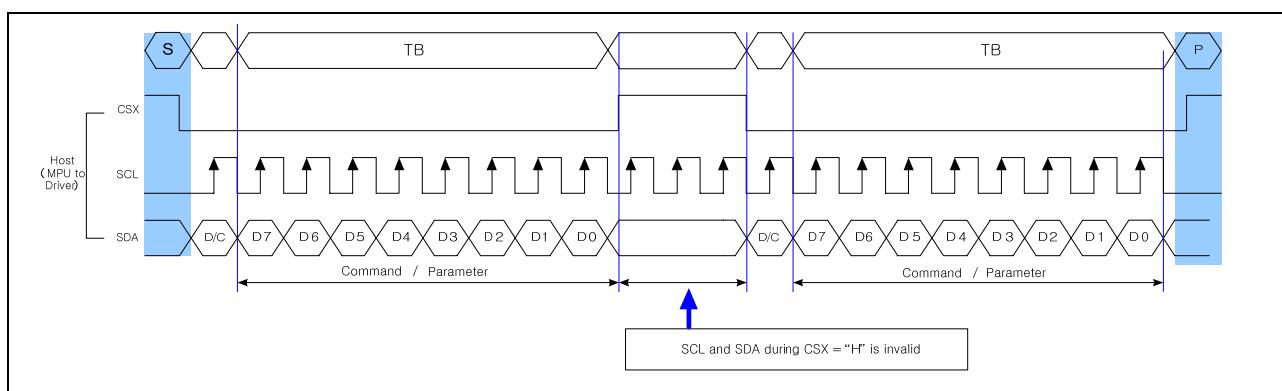
It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then S6D04M0 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command as been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter



**Figure 33. Parallel interface pause**

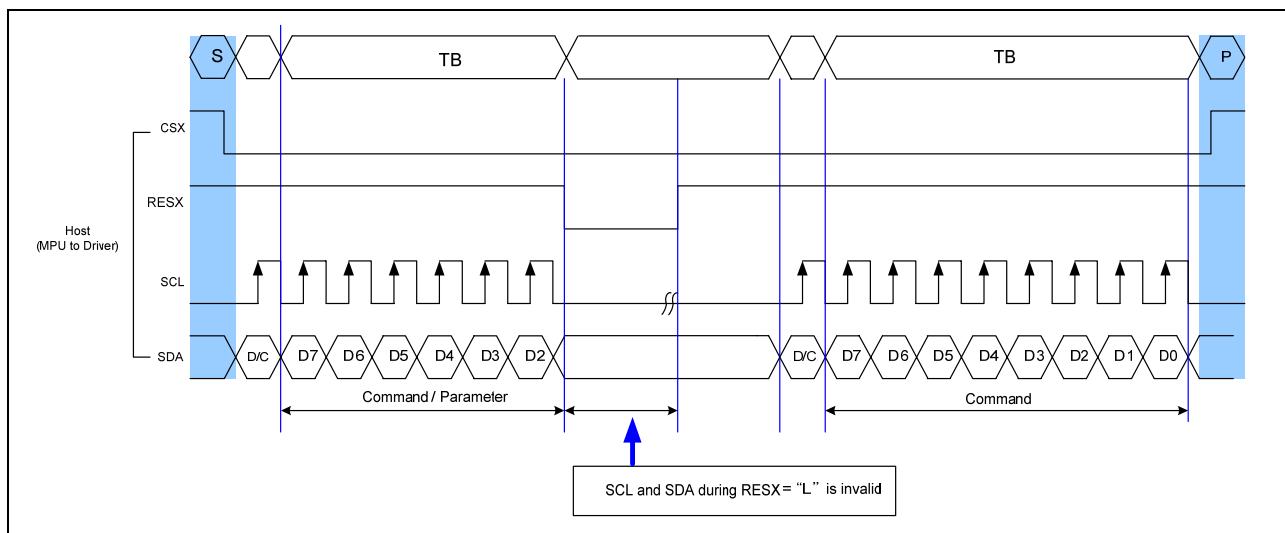


**Figure 34. Serial interface pause**

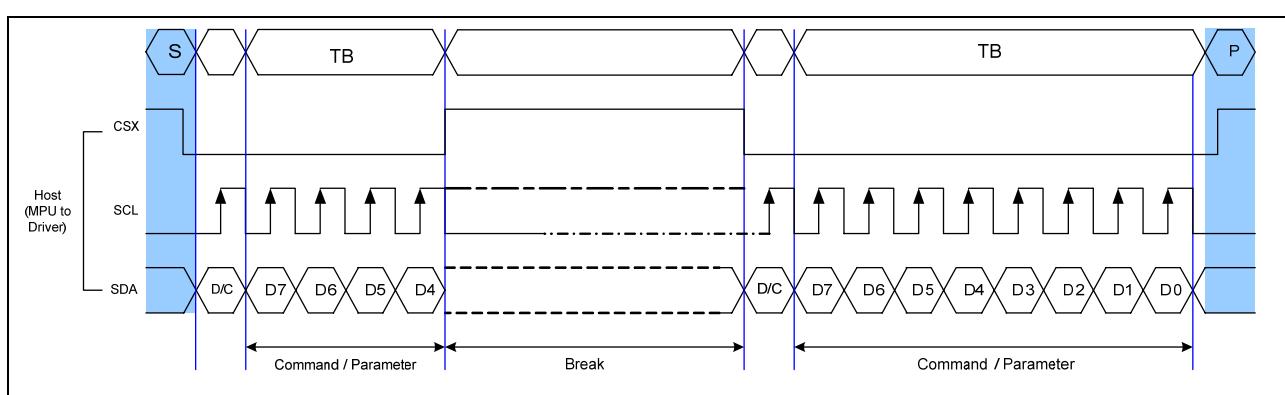
### 3.1.6.3. Data Transfer Recovery

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before SDA of the byte has been completed, then S6D04M0 will reject the previous bits have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX has reached the High state.

If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before SDA of the byte has been completed, then S6D04M0 will reject the previous bits and reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated.

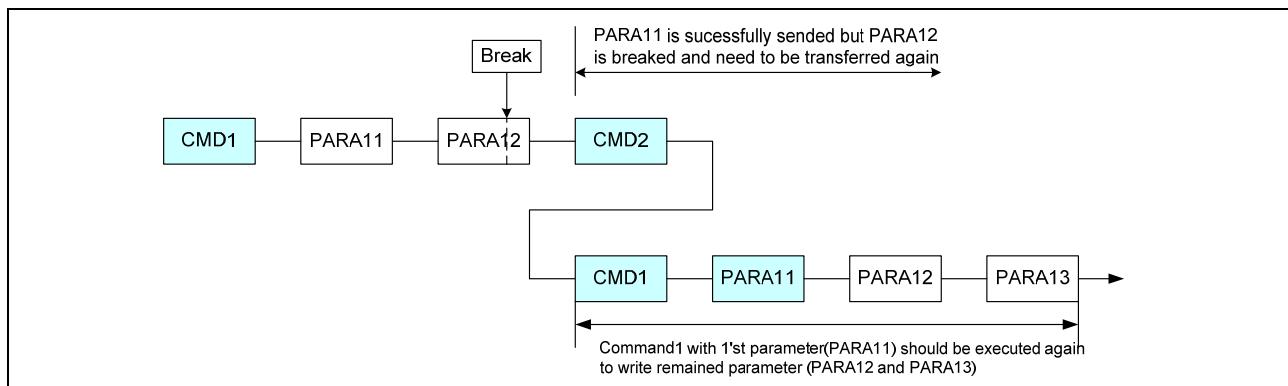


**Figure 35. Serial bus protocol, write mode – interrupted by RESX (3-wire 9bit data serial I/F)**



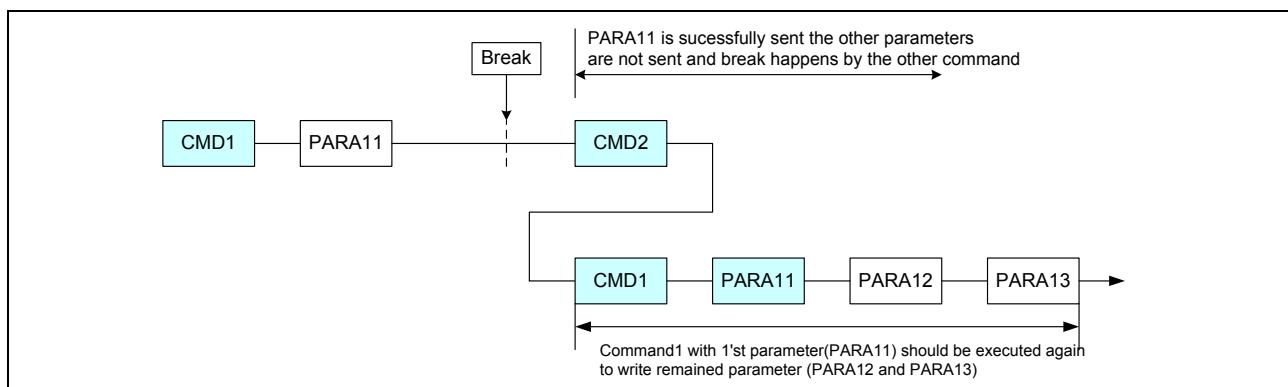
**Figure 36. Serial bus protocol, write mode – interrupted by CSX (3-wire 9bit data serial I/F)**

If 1, 2 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown in following Figure.



**Figure 37. Write interrupt recovery (serial interface)**

If 2 or more parameter command are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains in the previous value.



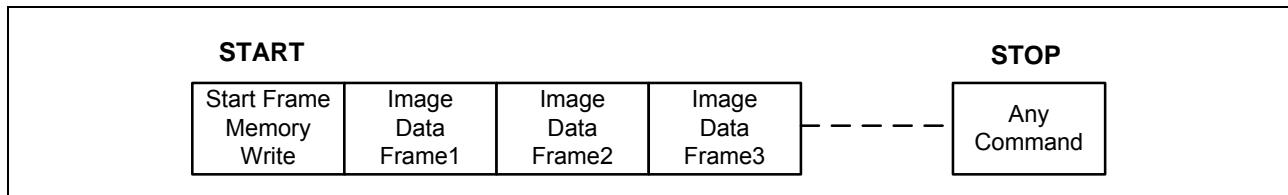
**Figure 38. Write interrupt recovery (both serial and parallel interface)**

### 3.1.6.4. Display Module Data Transfer Modes

The Module has 2 color modes for transferring data to the display RAM. Data can be downloaded to the Frame Memory by 2 methods.

#### Method 1

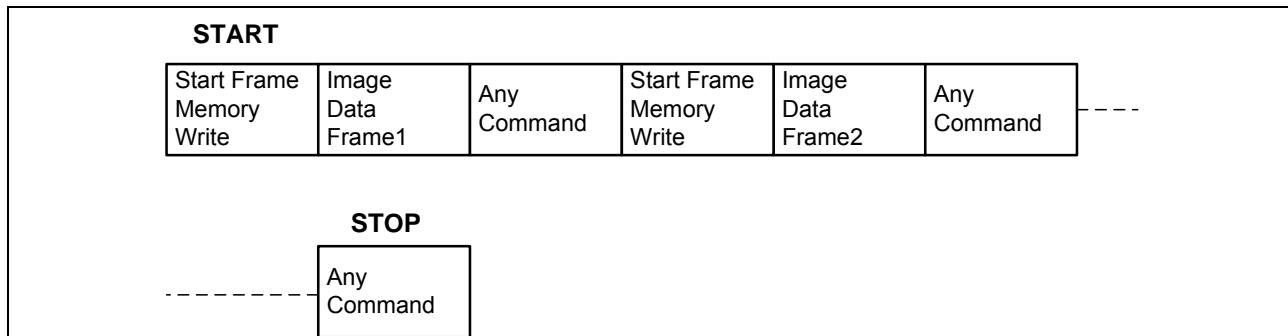
The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.



**Figure 39. Image data writing method 1**

#### Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Frame Memory Write command is sent, and a new Frame is downloaded.



**Figure 40. Image data writing method 2**

#### Note

These methods apply to all Data Transfer Color modes on any interfaces.

The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.

### 3.2. DISPLAY MODULE DATA COLOR CODING

Various data formats are available in which display data can be written to the display data RAM. It is possible to choose a format suitable for the purpose of use. The data format is determined by a combination of COLMOD and MDT commands.

#### 3.2.1. Display Data Format for Write

**Table 28. Display data format for wirte**

Color mode	Interface (IM[3:0])					CM		
	24bit ,	18bit ,	9bit	16bit ,	8bit ,	0	1	
	1000 or 1001	0100 or 1010	1011	0000 or 0010	0001 or 0011			
16M Color (COLMOD[2:0] = 111)	24bit 888 1/1 (MDT=00)	16bit 888 2/3 (MDT=00)	8bit 888 1/3 (MDT=00)	16bit 888 2/3 (MDT=00)	8bit 888 1/3 (MDT=00)	-		
		16bit 888 1/2 (MDT=01)		16bit 888 1/2 (MDT=01)				
262k Color (COLMOD[2:0] = 110)	18bit 666 1/1 (MDT=00)	18bit 666 1/1 (MDT=00)	9bit 666 1/2 (MDT=00)	16bit 666 2/3 (MDT=00)	6bit 666 1/3 (MDT=00)	Expand by IPM Note1	Use Look Up Table Note2	
			6bit 666 1/3 (MDT=01)	12bit 666 1/2 (MDT=01) 16bit 666 1/2 (MDT=10) 16bit 666 1/2 (MDT=11)				
65k Color (COLMOD[2:0] = 101)	16bit 565 1/1 (MDT=00)	16bit 565 1/1 (MDT=00)	8bit 565 1/2 (MDT=00)	16bit 565 1/1 (MDT=00)	8bit 565 1/2 (MDT=00)	Expand by IPM Note1	Use Look Up Table	

Note1. When CM = L, display data expand (666 → 888 or 565 → 888) method is decided by IPM command. In default condition (IPM = "100"), MSB data are copied to LSB data for expanding. See Figure. 41 and Figure. 42.

Note2. If CM is high, display data are expanded by using "Colour depth conversion Look Up Table" (Refer to the section 4.11). In default condition (CM= Low), S6D04M0 does not support Look Up Table.

Note3. Registers set related to data format (CM, IPM, MDT,...) are on the F6H command (Level 2)

In 65k color mode (16-bit data) data bit should be expanded to 24-bit like below. It will be used “CM=0” and “IPM=100”

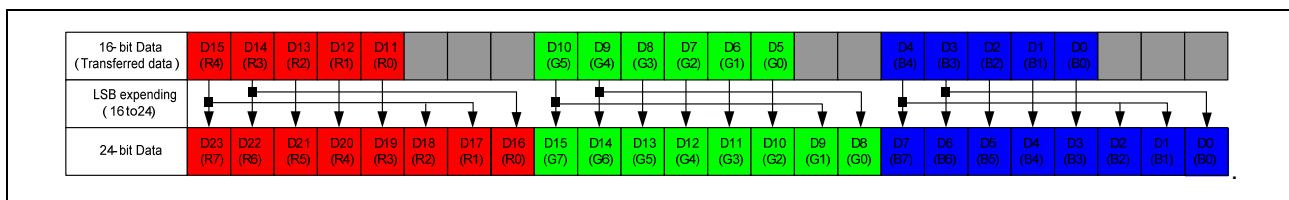


Figure 41. Data expand method (65K color mode)

In 262k color mode (18-bit data) data bit should be expanded to 24-bit like below. It will be used “CM=0” and “IPM=100”

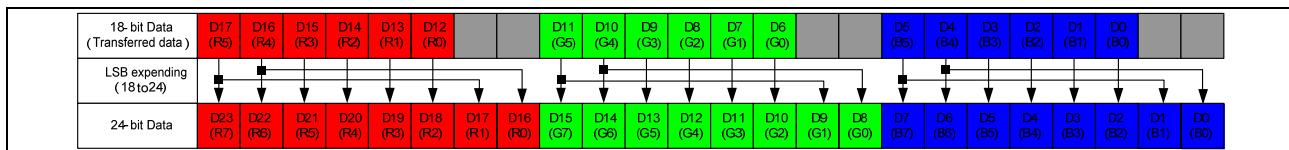


Figure 42. Data expand method (262K color mode)

### 3.2.2. Display Data Format for Read

#### 3.2.2.1. Read Data Format when CM = "L"

In every color mode, output display data is 24bit.

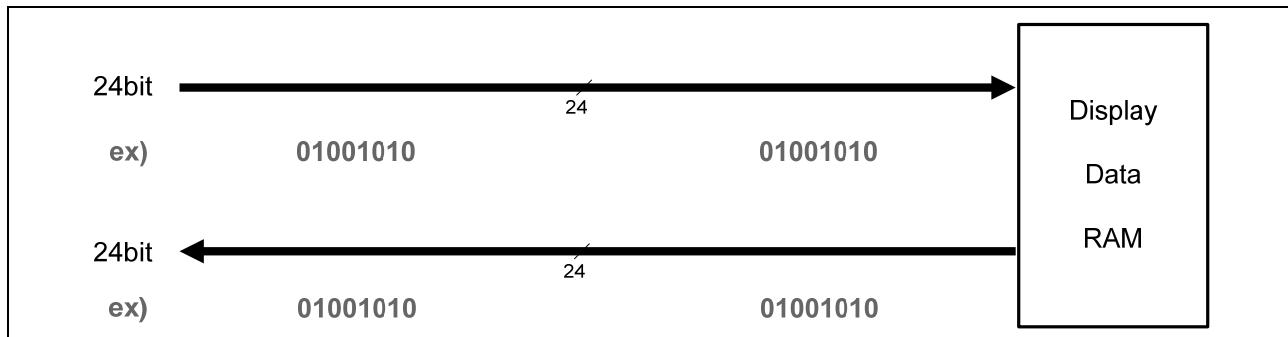


Figure 43. Case of 16M color mode (CM="L", IPM="100")

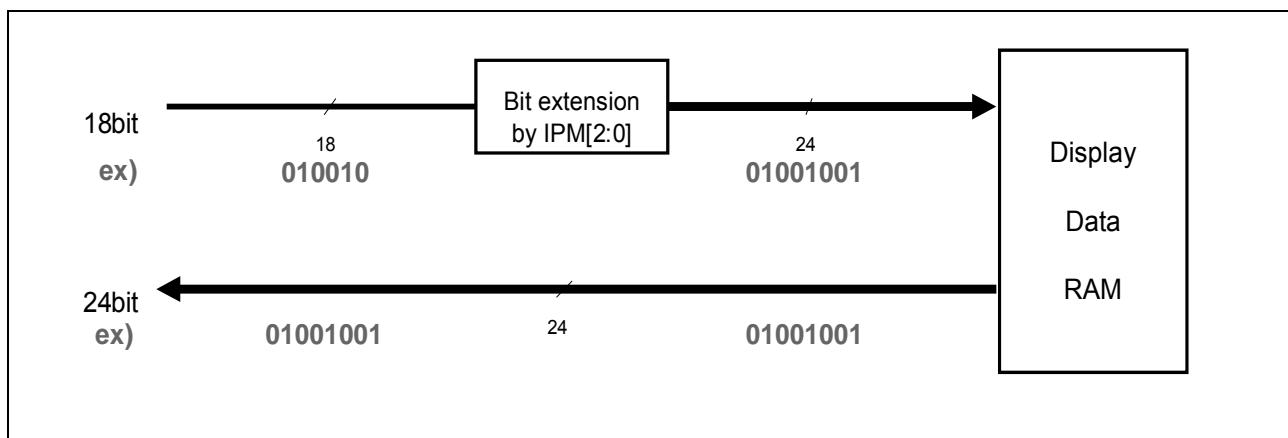


Figure 44. Case of 262K color mode (CM="L", IPM="100")

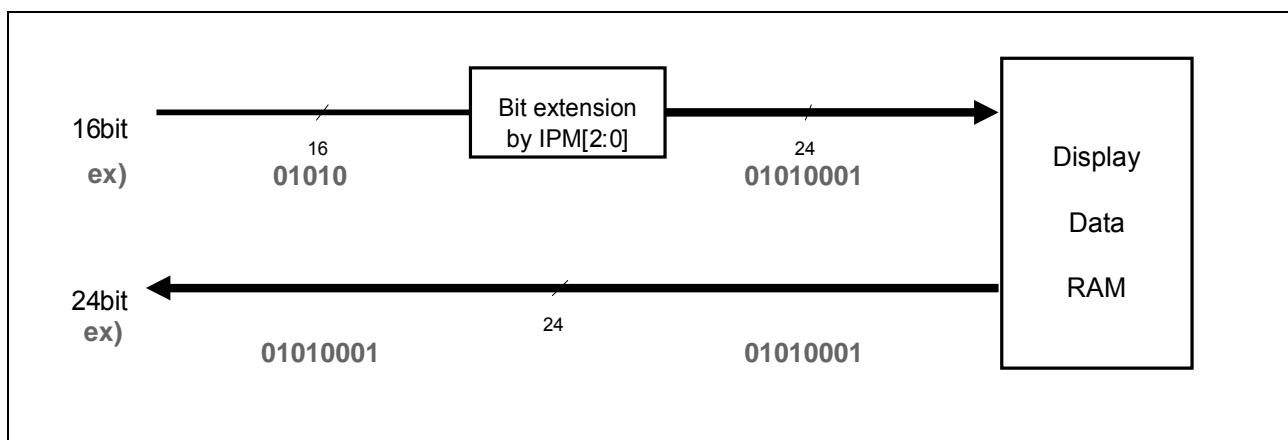
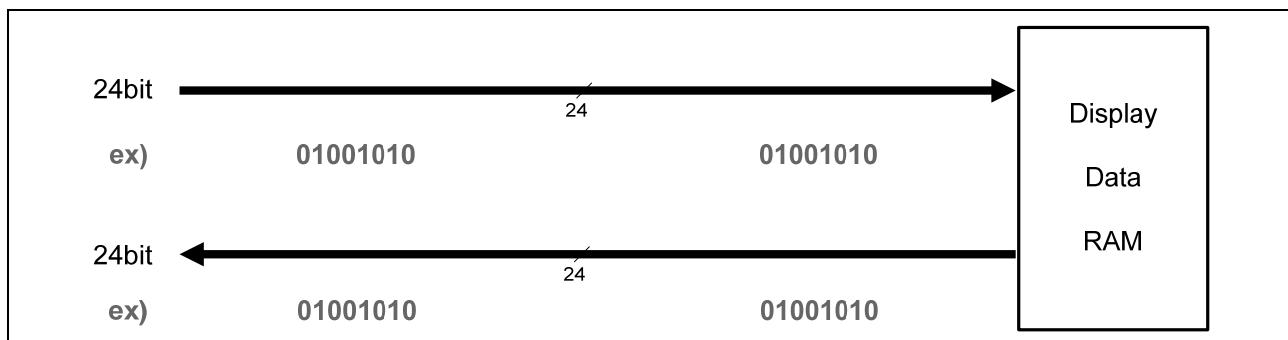


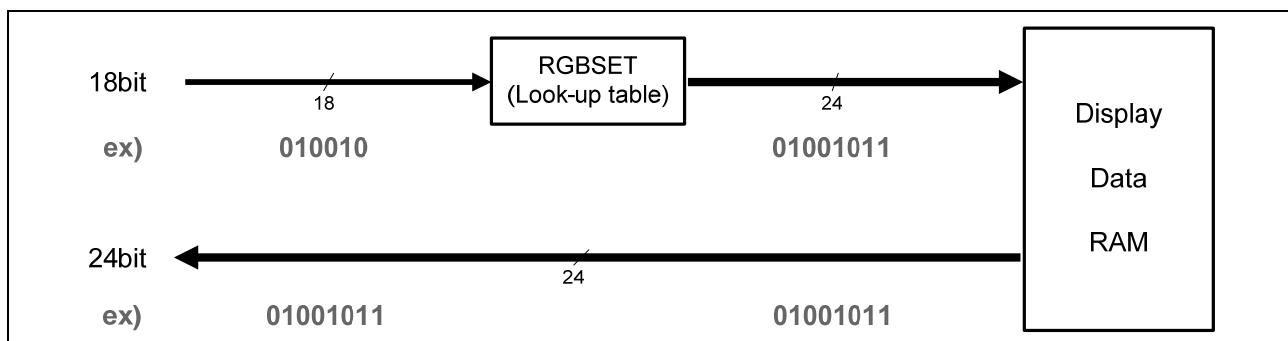
Figure 45. Case of 65K color mode (CM = "L", IPM="100")

### 3.2.2.2. Read Data Format when CM = "H"

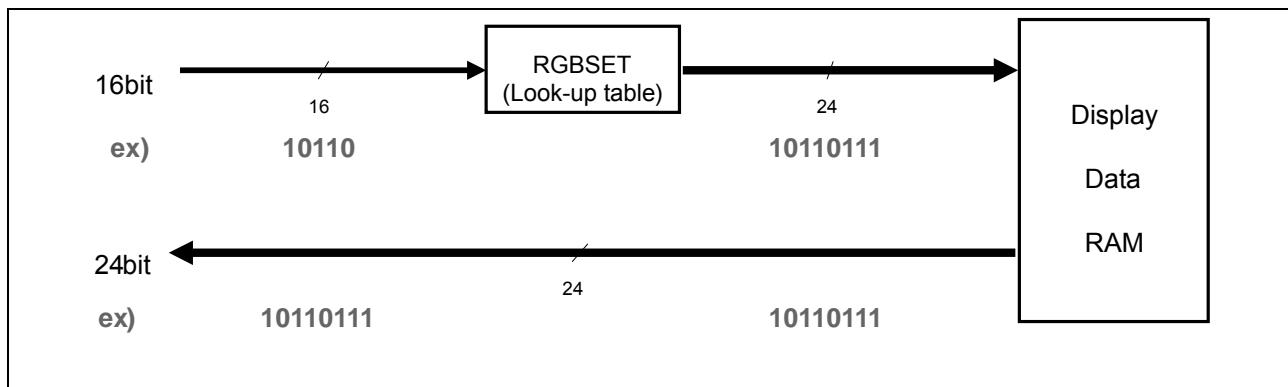
In every color mode, output display data is 24bit.



**Figure 46. Case of 16M color mode (CM="H")**



**Figure 47. Case of 262K color mode (CM="H")**



**Figure 48. Case of 65K color mode (CM="H")**

### 3.2.2.3. Display data read sequence.

Regardless of color mode, output display data is 24bit in read operation. So there are some limits on setting MDT[1:0] register in read mode.

#### 1) 24bit Interface

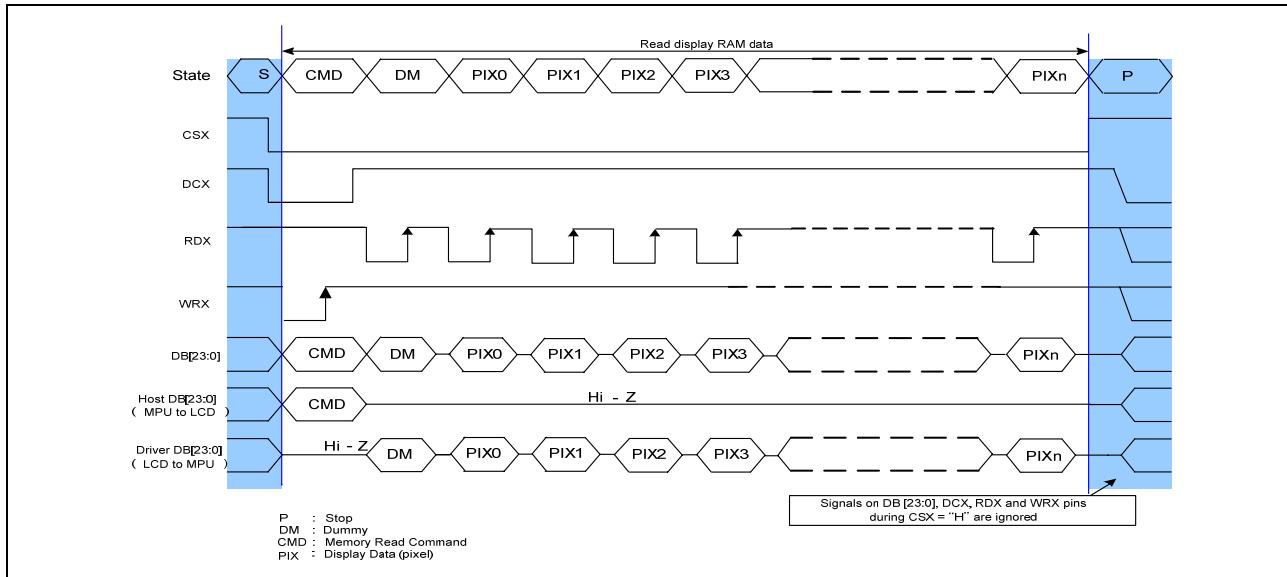


Figure 49. Display data read (24bit Interface type , )

#### 2) 8bit Interface

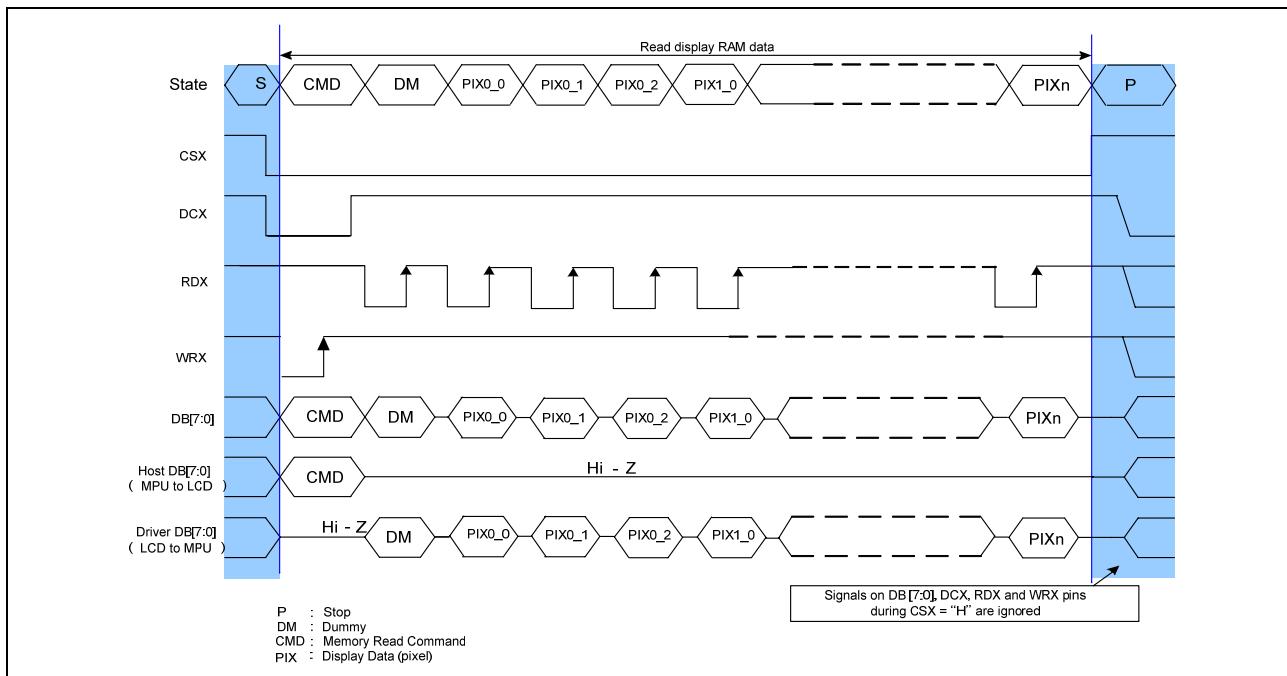
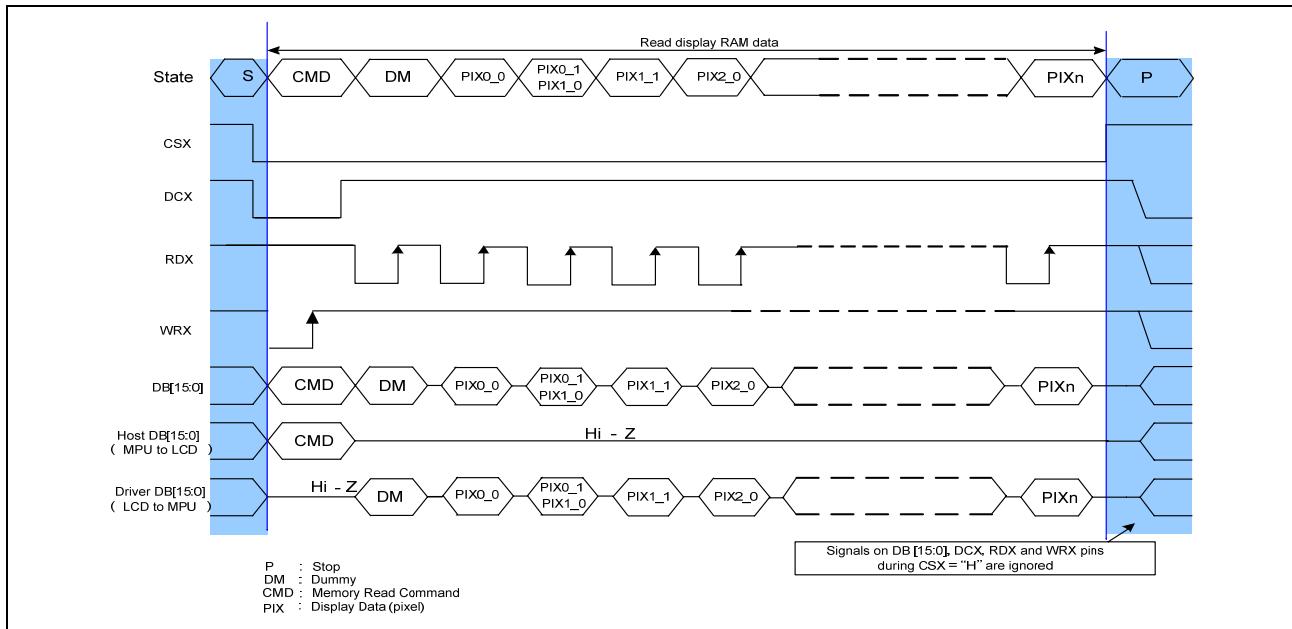


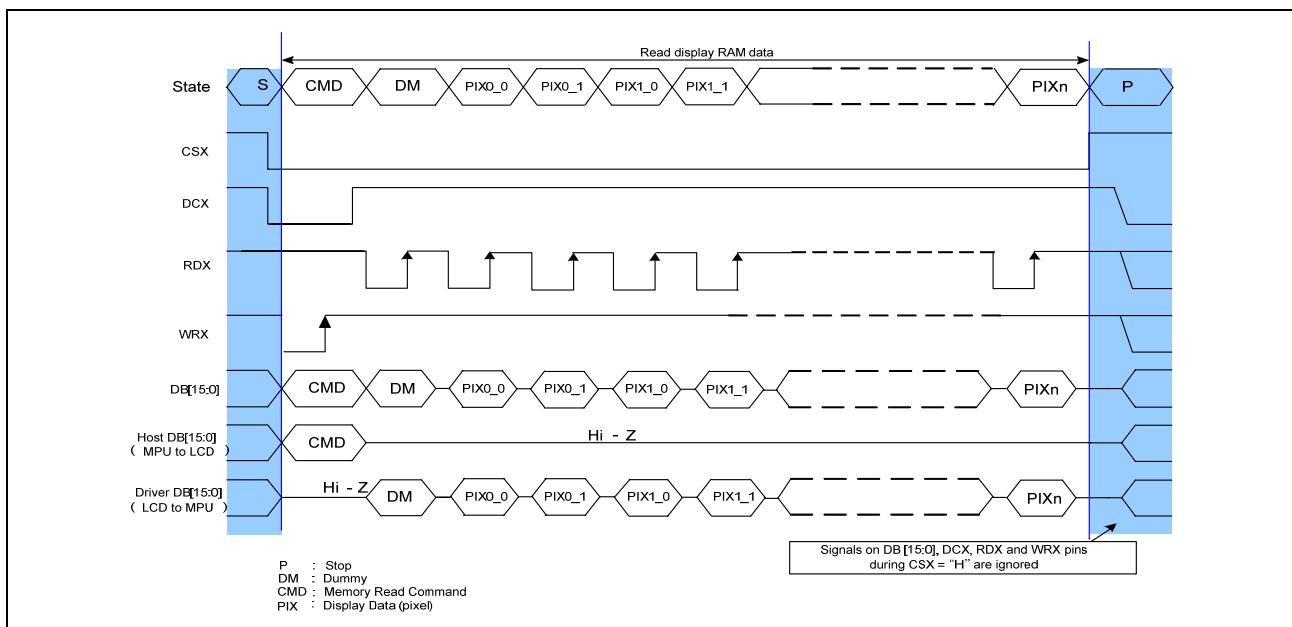
Figure 50. Display data read (8bit Interface type )

Note. In 8-bit Interface Type mode, D[7:0] must be assigned to DB[17:10]. See Table 6. Signal pads for logic Interface for more information.

## 3) 16bit Interface

**Figure 51. Display data read (16bit Interface type : MDT=00)**

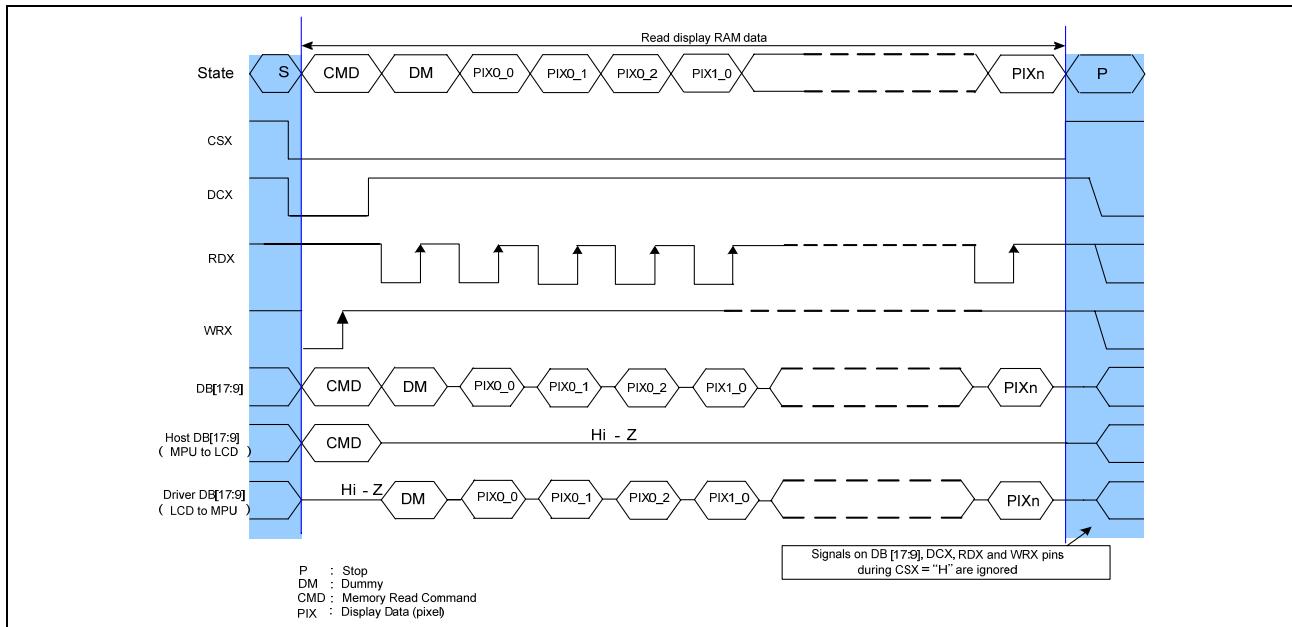
Note. In 16-bit Interface Type mode, D[17:0] must be assigned to DB[17:10], DB[8:1] pads. See Table 6. Signal pads for logic Interface for more information.

**Figure 52. Display data read (16bit Interface type : MDT=01)**

Note1. In 16-bit Interface Type mode, D[17:0] must be assigned to DB[17:10], DB[8:1] pads. See Table 6. Signal pads for logic Interface for more information.

Note2. If MDT[1:0] register set to "10" or "11", data read sequence operate as MDT[1:0] = "00".

## 3) 9bit Interface

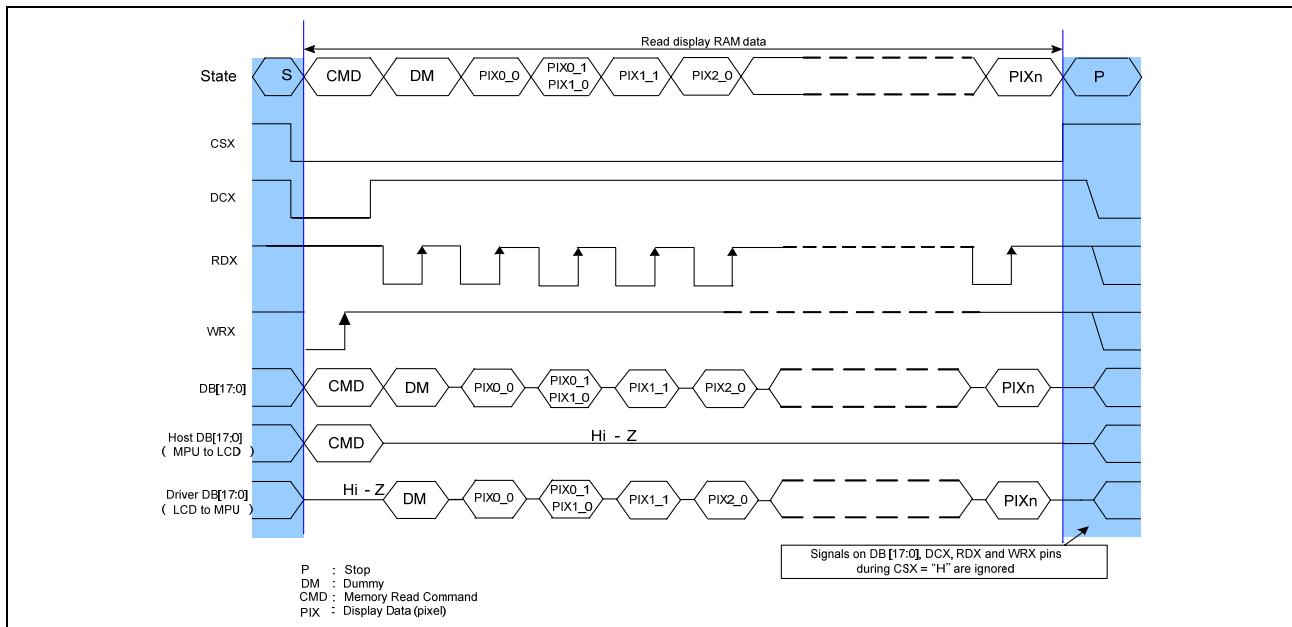
**Figure 53. Display data read (9bit Interface: MDT=00)**

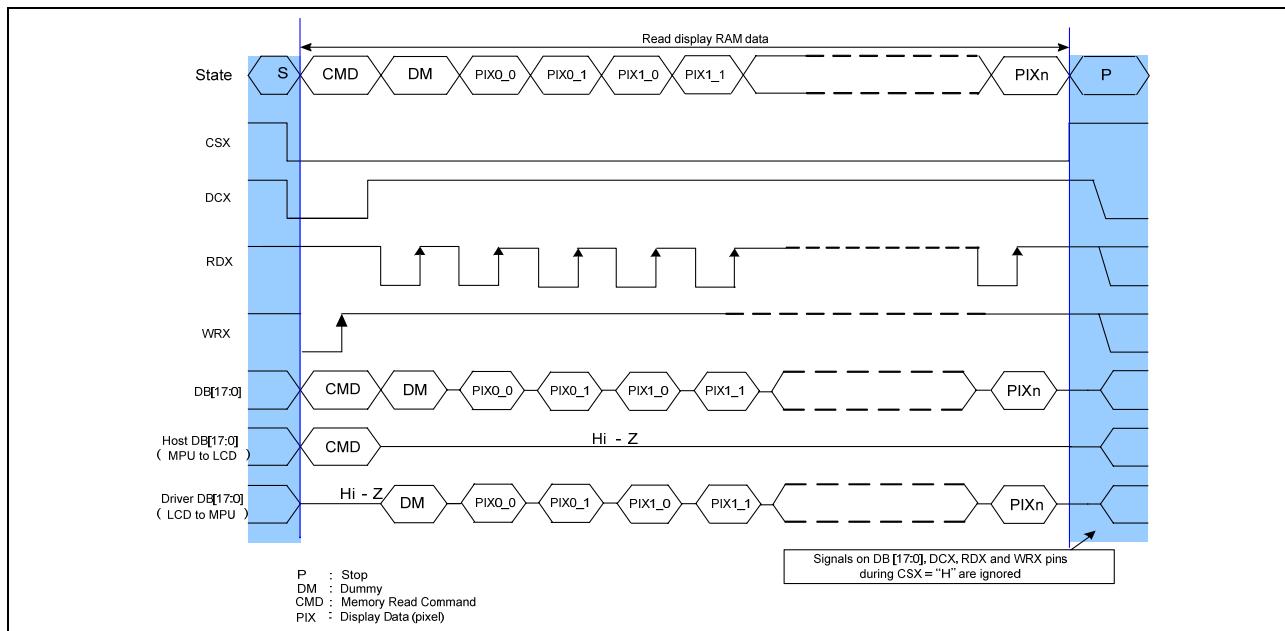
Note1. In 9-bit Interface mode, setting MDT[1:0] register to “10” or “11” is disable.

Note2. In 9-bit Interface mode for read operation, MDT[1:0] can not be “01”.

Note3. If MDT[1:0] register set to “01”, “10” or “11”, data read sequence operate as MDT = 00.

## 3) 18bit Interface

**Figure 54. Display data read (18bit Interface Type : MDT=00)**



**Figure 55. Display data read (18bit Interface : MDT=01)**

Note. In 18-bit Interface mode, setting MDT[1:0] register to "10" or "11" is disable. If MDT[1:0] register set to "10" or "11", data read sequence operate as MDT = 00.

### 3.2.3. 16M Color Mode

For the display data to be accessed in 16M color mode, it is necessary that 16M color mode be selected (B2 to B0: 111) using COLMOD command before writing/reading to or from the display data RAM. In this mode, the display data per pixel comprised of 8 bits for R, 8 bits for G and 8 bits for B is written to the display data RAM. When all of the data for one pixel (RGB) is prepared in the internal register, the MCU writes the data to the display data RAM. When the display data is read from the display data RAM after RAMRD command is issued, 1 byte of dummy read cycle is needed. For detail information of data read format, refer to section 3.2.2.

**Table 29. 24-bit Parallel interface type for 888 1/1 formats (MDT = 00)**

count	0	1	2	...	239	240
D/CX	0	1	1	...	1	1
D23		0R7	1R7	...	238R7	239R7
D22		0R6	1R6	...	238R6	239R6
D21		0R5	1R5	...	238R5	239R5
D20		0R4	1R4	...	238R4	239R4
D19		0R3	1R3	...	238R3	239R3
D18		0R2	1R2	...	238R2	239R2
D17		0R1	1R1	...	238R1	239R1
D16		0R0	1R0	...	238R0	239R0
D15		0G7	1G7	...	238G7	239G7
D14		0G6	1G6	...	238G6	239G6
D13		0G5	1G5	...	238G5	239G5
D12		0G4	1G4	...	238G4	239G4
D11		0G3	1G3	...	238G3	239G3
D10		0G2	1G2	...	238G2	239G2
D9		0G1	1G1	...	238G1	239G1
D8		0G0	1G0	...	238G0	239G0
D7	C7	0B7	1B7	...	238B7	239B7
D6	C6	0B6	1B6	...	238B6	239B6
D5	C5	0B5	1B5	...	238B5	239B5
D4	C4	0B4	1B4	...	238B4	239B4
D3	C3	0B3	1B3	...	238B3	239B3
D2	C2	0B2	1B2	...	238B2	239B2
D1	C1	0B1	1B1	...	238B1	239B1
D0	C0	0B0	1B0	...	238B0	239B0

Note. In 24-bit Interface Type mode, Command bits (C[7:0]) must be assigned to DB[8:1]. See Table 6. Signal pads for logic Interface

for more information



**Table 30. 8-bit Parallel interface type for 888 1/3 formats (MDT = 00)**

<b>count</b>	<b>0</b>	<b>1</b>	<b>2</b>	<b>3</b>	<b>...</b>	<b>718</b>	<b>719</b>	<b>720</b>
D/CX	0	1	1	1	...	1	1	1
D7	C7	0R7	0G7	0B7	...	239R7	239G7	239B7
D6	C6	0R6	0G6	0B6	...	239R6	239G6	239B6
D5	C5	0R5	0G2	0B5	...	239R5	239G5	239B5
D4	C4	0R4	0G1	0B4	...	239R4	239G4	239B4
D3	C3	0R3	0G0	0B3	...	239R3	239G3	239B3
D2	C2	0R2	0G2	0B2	...	239R2	239G2	239B2
D1	C1	0R1	0G1	0B1	...	239R1	239G1	239B1
D0	C0	0R0	0G0	0B0	...	239R0	239G0	239B0

Note. In 8-bit Interface Type mode, D[7:0] must be assigned to DB[17:10]. See Table 6. Signal pads for logic Interface for more information.

**Table 31. 16-bit Parallel interface type for 888 2/3 formats (MDT = 00)**

<b>count</b>	<b>0</b>	<b>1</b>	<b>2</b>	<b>3</b>	<b>...</b>	<b>358</b>	<b>359</b>	<b>360</b>
D/CX	0	1	1	1	...	1	1	1
D15		0R7	0B7	1G7	...	238R7	238B6	239G7
D14		0R6	0B6	1G6	...	238R6	238B5	239G6
D13		0R5	0B5	1G5	...	238R5	238B5	239G5
D12		0R4	0B4	1G4	...	238R4	238B4	239G4
D11		0R3	0B3	1G3	...	238R3	238B3	239G3
D10		0R2	0B2	1G2	...	238R2	238B2	239G2
D9		0R1	0B1	1G1	...	238R1	238B1	239G1
D8		0R0	0B0	1G0	...	238R0	238B0	239G0
D7	C7	0G7	1R7	1B7	...	238G7	239R7	239B7
D6	C6	0G6	1R6	1B6	...	238G6	239R6	239B6
D5	C5	0G5	1R5	1B5	...	238G5	239R5	239B5
D4	C4	0G4	1R4	1B4	...	238G4	239R4	239B4
D3	C3	0G3	1R3	1B3	...	238G3	239R3	239B3
D2	C2	0G2	1R2	1B2	...	238G2	239R2	239B2
D1	C1	0G1	1R1	1B1	...	238G1	239R1	239B1
D0	C0	0G0	1R0	1B0	...	238G0	239R0	239B0

Note. In 16-bit Interface Type mode, D[7:0] must be assigned to DB[8:1] pads and D[15:8] must be assigned to DB[17:10] pads.

See Table 6. Signal pads for logic Interface for more information.



**Table 32. 16-bit Parallel interface type for 888 1/2 formats (MDT = 01)**

<b>count</b>	<b>0</b>	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>	<b>...</b>	<b>479</b>	<b>480</b>
D/CX	0	1	1	1	1	...	1	1
D15		0R7	0B7	1R7	1B7	...	239R7	239B7
D14		0R6	0B6	1R6	1B6	...	239R6	239B6
D13		0R5	0B5	1R5	1B5	...	239R5	239B5
D12		0R4	0B4	1R4	1B4	...	239R4	239B4
D11		0R3	0B3	1R3	1B3	...	239R3	239B3
D10		0R2	0B2	1R2	1B2	...	239R2	239B2
D9		0R1	0B1	1R1	1B1	...	239R1	239B1
D8		0R0	0B0	1R0	1B0	...	239R0	239B0
D7	C7	0G7		1G7		...	239G7	
D6	C6	0G6		1G6		...	239G6	
D5	C5	0G5		1G5		...	239G5	
D4	C4	0G4		1G4		...	239G4	
D3	C3	0G3		1G3		...	239G3	
D2	C2	0G2		1G2		...	239G2	
D1	C1	0G1		1G1		...	239G1	
D0	C0	0G0		1G0		...	239G0	

Note. In 16-bit Interface Type mode, D[7:0] must be assigned to DB[8:1] pads and D[15:8] must be assigned to DB[17:10] pads.

See Table 6. Signal pads for logic Interface for more information.

**Table 33. 9-bit Parallel interface for 888 1/3 formats (MDT = 00)**

<b>count</b>	<b>0</b>	<b>1</b>	<b>2</b>	<b>3</b>	<b>...</b>	<b>718</b>	<b>719</b>	<b>720</b>
D/CX	0	1	1	1	...	1	1	1
D17	C7	0R7	0G7	0B7	...	239R7	239G7	239B7
D16	C6	0R6	0G6	0B6	...	239R6	239G6	239B6
D15	C5	0R5	0G5	0B5	...	239R5	239G5	239B5
D14	C4	0R4	0G4	0B4	...	239R4	239G4	239B4
D13	C3	0R3	0G3	0B3	...	239R3	239G3	239B3
D12	C2	0R2	0G2	0B2	...	239R2	239G2	239B2
D11	C1	0R1	0G1	0B1	...	239R1	239G1	239B1
D10	C0	0R0	0G0	0B0	...	239R0	239G0	239B0
D9					...			

Table 34. 18-bit Parallel interface type for 888 2/3 formats (MDT = 00)

count	0	1	2	3	...	358	359	360
D/CX	0	1	1	1	...	1	1	1
D17		0R7	0B7	1G7	...	238R7	238B6	239G7
D16		0R6	0B6	1G6	...	238R6	238B5	239G6
D15		0R5	0B5	1G5	...	238R5	238B5	239G5
D14		0R4	0B4	1G4	...	238R4	238B4	239G4
D13		0R3	0B3	1G3	...	238R3	238B3	239G3
D12		0R2	0B2	1G2	...	238R2	238B2	239G2
D11		0R1	0B1	1G1	...	238R1	238B1	239G1
D10		0R0	0B0	1G0	...	238R0	238B0	239G0
D9								
D8		0G7	1R7	1B7	...	238G7	239R7	239B7
D7	C7	0G6	1R6	1B6	...	238G6	239R6	239B6
D6	C6	0G5	1R5	1B5	...	238G5	239R5	239B5
D5	C5	0G4	1R4	1B4	...	238G4	239R4	239B4
D4	C4	0G3	1R3	1B3	...	238G3	239R3	239B3
D3	C3	0G2	1R2	1B2	...	238G2	239R2	239B2
D2	C2	0G1	1R1	1B1	...	238G1	239R1	239B1
D1	C1	0G0	1R0	1B0	...	238G0	239R0	239B0
D0	C0							

Note. In 18-bit Interface Type mode, Command bits (C[7:0]) must be assigned to DB[8:1]. See Table 6. Signal pads for logic Interface for more information

**Table 35. 18-bit Parallel interface type for 888 1/2 formats (MDT = 01)**

<b>count</b>	<b>0</b>	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>	<b>...</b>	<b>479</b>	<b>480</b>
D/CX	0	1	1	1	1	...	1	1
D17		0R7	0B7	1R7	1B7	...	239R7	239B7
D16		0R6	0B6	1R6	1B6	...	239R6	239B6
D15		0R5	0B5	1R5	1B5	...	239R5	239B5
D14		0R4	0B4	1R4	1B4	...	239R4	239B4
D13		0R3	0B3	1R3	1B3	...	239R3	239B3
D12		0R2	0B2	1R2	1B2	...	239R2	239B2
D11		0R1	0B1	1R1	1B1	...	239R1	239B1
D10		0R0	0B0	1R0	1B0	...	239R0	239B0
D9								
D8		0G7		1G7		...	239G7	
D7	C7	0G6		1G6		...	239G6	
D6	C6	0G5		1G5		...	239G5	
D5	C5	0G4		1G4		...	239G4	
D4	C4	0G3		1G3		...	239G3	
D3	C3	0G2		1G2		...	239G2	
D2	C2	0G1		1G1		...	239G1	
D1	C1	0G0		1G0		...	239G0	
D0	C0							

Note. In 18-bit Interface Type mode, Command bits (C[7:0]) must be assigned to DB[8:1]. See Table 6. Signal pads for logic Interface for more information

### 3.2.4. 262k Color Mode

For the display data to be accessed in 262k color mode, it is necessary that 262k color mode be selected (B2 to B0: 110) using COLMOD command before writing/reading to or from the display data RAM. In this mode, the display data per pixel comprised of 6 bits for R, 6 bits for G and 6 bits for B is written to the display data RAM. When all of the data for one pixel (RGB) is prepared in the internal register, the MCU writes the data to the display data RAM. When the display data is read from the display data RAM after RAMRD command is issued, 1 byte of dummy read cycle is needed. For detail information of data read format, refer to section 3.2.2.

**Table 36. 24-bit Parallel interface type for 666 1/1 formats (MDT = 00)**

count	0	1	2	...	239	240
D/CX	0	1	1	...	1	1
D23				...		
D22				...		
D21				...		
D20				...		
D19				...		
D18				...		
D17		0R5	1R5	...	238R5	239R5
D16		0R4	1R4	...	238R4	239R4
D15		0R3	1R3	...	238R3	239R3
D14		0R2	1R2	...	238R2	239R2
D13		0R1	1R1	...	238R1	239R1
D12		0R0	1R0	...	238R0	239R0
D11		0G5	1G5	...	238G5	239G5
D10		0G4	1G4	...	238G4	239G4
D9		0G3	1G3	...	238G3	239G3
D8		0G2	1G2	...	238G2	239G2
D7	C7	0G1	1G1	...	238G1	239G1
D6	C6	0G0	1G0	...	238G0	239G0
D5	C5	0B5	1B5	...	238B5	239B5
D4	C4	0B4	1B4		238B4	239B4
D3	C3	0B3	1B3		238B3	239B3
D2	C2	0B2	1B2	...	238B2	239B2
D1	C1	0B1	1B1	...	238B1	239B1
D0	C0	0B0	1B0	...	238B0	239B0

Note. In 24-bit Interface Type mode, Command bits (C[7:0]) must be assigned to DB[8:1]. See Table 6. Signal pads for logic Interface for more information.



**Table 37. 8-bit Parallel interface type for 666 1/3 formats (MDT = 00)**

count	0	1	2	3	...	718	719	720
D/CX	0	1	1	1	...	1	1	1
D7	C7	0R5	0G5	0B5	...	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	...	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	...	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	...	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	...	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	...	239R0	239G0	239B0
D1	C1				...			
D0	C0				...			

Note. In 8-bit Interface Type mode, D[7:0] must be assigned to DB[17:10]. See Table 6. Signal pads for logic Interface for more information.

**Table 38. 16-bit Parallel interface type for 666 2/3 formats (MDT = 00)**

count	0	1	2	...	...	358	359	360
D/CX	0	1	1	...	...	1	1	1
D15		0R5	0B5	1G5	...	238R5	238B5	239G5
D14		0R4	0B4	1G4	...	238R4	238B4	239G4
D13		0R3	0B3	1G3	...	238R3	238B3	239G3
D12		0R2	0B2	1G2	...	238R2	238B2	239G2
D11		0R1	0B1	1G1	...	238R1	238B1	239G1
D10		0R0	0B0	1G0	...	238R0	238B0	239G0
D9					...			
D8					...			
D7	C7	0G5	1R5	1B5	...	238G5	239R5	239B5
D6	C6	0G4	1R4	1B4	...	238G4	239R4	239B4
D5	C5	0G3	1R3	1B3	...	238G3	239R3	239B3
D4	C4	0G2	1R2	1B2	...	238G2	239R2	239B2
D3	C3	0G1	1R1	1B1	...	238G1	239R1	239B1
D2	C2	0G0	1R0	1B0	...	238G0	239R0	239B0
D1	C1				...			
D0	C0				...			

Note. In 16-bit Interface Type mode, D[7:0] must be assigned to DB[8:1] pads and D[15:8] must be assigned to DB[17:10] pads.

See Table 6. Signal pads for logic Interface for more information.

Table 39. 16-bit Parallel interface type for 666 1/2 formats ( MDT = 01 )

count	0	1	2	3	4	...	479	480
D/CX	0	1	1	1	1	...	1	1
D15		0R5	0B5	1R5	1B5	...	239R5	239B5
D14		0R4	0B4	1R4	1B4	...	239R4	239B4
D13		0R3	0B3	1R3	1B3	...	239R3	239B3
D12		0R2	0B2	1R2	1B2	...	239R2	239B2
D11		0R1	0B1	1R1	1B1	...	239R1	239B1
D10		0R0	0B0	1R0	1B0	...	239R0	239B0
D9						...		
D8						...		
D7	C7	0G5		1G5		...	239G5	
D6	C6	0G4		1G4		...	239G4	
D5	C5	0G3		1G3		...	239G3	
D4	C4	0G2		1G2		...	239G2	
D3	C3	0G1		1G1		...	239G1	
D2	C2	0G0		1G0		...	239G0	
D1	C1					...		
D0	C0					...		

Note. In 16-bit Interface Type mode, D[7:0] must be assigned to DB[8:1] pads and D[15:8] must be assigned to DB[17:10] pads.

See Table 6. Signal pads for logic Interface for more information.

Table 40. 16-bit Parallel interface type for 666 1/2 formats ( MDT = 10 )

count	0	1	2	3	4	...	479	480
D/CX	0	1	1	1	1	...	1	1
D15		0R5	0B1	1R5	1B1	...	239R5	239B1
D14		0R4	0B0	1R4	1B0	...	239R4	239B0
D13		0R3		1R3		...	239R3	
D12		0R2		1R2		...	239R2	
D11		0R1		1R1		...	239R1	
D10		0R0		1R0		...	239R0	
D9		0G5		1G5		...	239G5	
D8		0G4		1G4		...	239G4	
D7	C7	0G3		1G3		...	239G3	
D6	C6	0G2		1G2		...	239G2	
D5	C5	0G1		1G1		...	239G1	
D4	C4	0G0		1G0		...	239G0	
D3	C3	0B5		1B5		...	239B5	
D2	C2	0B4		1B4		...	239B4	
D1	C1	0B3		1B3		...	239B3	
D0	C0	0B2		1B2		...	239B2	

Note. In 16-bit Interface Type mode, D[7:0] must be assigned to DB[8:1] pads and D[15:8] must be assigned to DB[17:10] pads.

See Table 6. Signal pads for logic Interface for more information.

**Table 41. 16-bit Parallel interface type for 666 1/2 formats (MDT = 11)**

count	0	1	2	3	4	...	479	480
D/CX	0	1	1	1	1	...	1	1
D15			0R3		1R3	...		239R3
D14			0R2		1R2	...		239R2
D13			0R1		1R1	...		239R1
D12			0R0		1R0	...		239R0
D11			0G5		1G5	...		239G5
D10			0G4		1G4	...		239G4
D9			0G3		1G3	...		239G3
D8			0G2		1G2	...		239G2
D7	C7		0G1		1G1	...		239G1
D6	C6		0G0		1G0	...		239G0
D5	C5		0B5		1B5	...		239B5
D4	C4		0B4		1B4	...		239B4
D3	C3		0B3		1B3	...		239B3
D2	C2		0B2		1B2	...		239B2
D1	C1	0R5	0B1	1R5	1B1	...	239R5	239B1
D0	C0	0R4	0B0	1R4	1B0	...	239R4	239B0

Note. In 16-bit Interface Type mode, D[7:0] must be assigned to DB[8:1] pads and D[15:8] must be assigned to DB[17:10] pads.

See Table 6. Signal pads for logic Interface for more information.

**Table 42. 9-bit Parallel interface for 666 1/2 formats (MDT = 00)**

count	0	1	2	3	4	...	479	480
D/CX	0	1	1	1	1	...	1	1
D17	C7	0R5	0G2	1R5	1G2	...	239R5	239G2
D16	C6	0R4	0G1	1R4	1G1	...	239R4	239G1
D15	C5	0R3	0G0	1R3	1G0	...	239R3	239G0
D14	C4	0R2	0B5	1R2	1B5	...	239R2	239B5
D13	C3	0R1	0B4	1R1	1B4	...	239R1	239B4
D12	C2	0R0	0B3	1R0	1B3	...	239R0	239B3
D11	C1	0G5	0B2	1G5	1B2	...	239G5	239B2
D10	C0	0G4	0B1	1G4	1B1	...	239G5	239B1
D9		0G3	0B0	1G3	1B0	...	239G4	239B0

Table 43. 9-bit Parallel interface for 666 1/3 formats (MDT = 01)

count	0	1	2	3	...	718	719	720
D/CX	0	1	1	1	...	1	1	1
D17	C7	0R5	0G5	0B5	...	239R5	239G5	239B5
D16	C6	0R4	0G4	0B4	...	239R4	239G5	239B4
D15	C5	0R3	0G3	0B3	...	239R3	239G4	239B3
D14	C4	0R2	0G2	0B2	...	239R2	239G2	239B2
D13	C3	0R1	0G1	0B1	...	239R1	239G1	239B1
D12	C2	0R0	0G0	0B0	...	239R0	239G0	239B0
D11	C1				...			
D10	C0				...			
D9					...			

Table 44. 18-bit Parallel interface type for 666 1/1 formats (MDT = 00)

count	0	1	2	...	239	240
D/CX	0	1	1	...	1	1
D17		0R5	1R5	...	238R5	239R5
D16		0R4	1R4	...	238R4	239R4
D15		0R3	1R3	...	238R3	239R3
D14		0R2	1R2	...	238R2	239R2
D13		0R1	1R1	...	238R1	239R1
D12		0R0	1R0	...	238R0	239R0
D11		0G5	1G5	...	238G5	239G5
D10		0G4	1G4	...	238G4	239G4
D9		0G3	1G3	...	238G3	239G3
D8		0G2	1G2	...	238G2	239G2
D7	C7	0G1	1G1	...	238G1	239G1
D6	C6	0G0	1G0	...	238G0	239G0
D5	C5	0B5	1B5	...	238B5	239B5
D4	C4	0B4	1B4	...	238B4	239B4
D3	C3	0B3	1B3	...	238B3	239B3
D2	C2	0B2	1B2	...	238B2	239B2
D1	C1	0B1	1B1	...	238B1	239B1
D0	C0	0B0	1B0	...	238B0	239B0

Note. In 18-bit Interface Type mode, Command bits (C[7:0]) must be assigned to DB[8:1]. See Table 6. Signal pads for logic Interface for more information

### 3.2.5. 65k Color Mode

For the display data to be accessed in 65k color mode, it is necessary that 65k color mode be selected (B2 to B0: 101) using COLMOD command before writing or reading to or from the display data RAM. In this mode, the display data per pixel comprised of 5 bits for R, 6 bits for G and 5 bits for B is written to the display data RAM. When all of the data for one pixel (RGB) is prepared in the internal register, the MCU writes the data to the display data RAM. When the display data is read from the display data RAM after RAMRD command is issued, 1 byte of dummy read cycle is needed. For detail information of data read format, refer to section 3.2.2.

**Table 45. 24-bit Parallel interface type for 565 1/1 formats (MDT = 00)**

count	0	1	2	...	239	240
D/CX	0	1	1	...	1	1
D23						
D22						
D21						
D20						
D19						
D18						
D17						
D16						
D15		0R4	1R4	...	238R4	239R4
D14		0R3	1R3	...	238R3	239R3
D13		0R2	1R2	...	238R2	239R2
D12		0R1	1R1	...	238R1	239R1
D11		0R0	1R0	...	238R0	239R0
D10		0G5	1G5	...	238G5	239G5
D9		0G4	1G4	...	238G4	239G4
D8		0G3	1G3	...	238G3	239G3
D7	C7	0G2	1G2	...	238G2	239G2
D6	C6	0G1	1G1	...	238G1	239G1
D5	C5	0G0	1G0	...	238G0	239G0
D4	C4	0B4	1B4	...	238B4	239B4
D3	C3	0B3	1B3	...	238B3	239B3
D2	C2	0B2	1B2	...	238B2	239B2
D1	C1	0B1	1B1	...	238B1	239B1
D0	C0	0B0	1B0	...	238B0	239B0

Note. In 24-bit Interface Type mode, Command bits (C[7:0]) must be assigned to DB[8:1]. See Table 6. Signal pads for logic Interface for more information.



**Table 46. 8-bit Parallel interface type for 565 1/2 formats (MDT = 00)**

<b>count</b>	<b>0</b>	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>	<b>...</b>	<b>359</b>	<b>480</b>
D/CX	0	1	1	1	1	...	1	1
D7	C7	0R4	0G2	1R4	1G2	...	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	...	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	...	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	...	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	...	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	...	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	...	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	...	239G3	239B0

Note. In 8-bit Interface Type mode, D[7:0] must be assigned to DB[17:10]. See Table 6. Signal pads for logic Interface for more information.

**Table 47. 16-bit Parallel interface type for 565 1/1 formats (MDT = 00)**

<b>count</b>	<b>0</b>	<b>1</b>	<b>2</b>	<b>...</b>	<b>239</b>	<b>240</b>
D/CX	0	1	1	...	1	1
D15		0R4	1R4	...	238R4	239R4
D14		0R3	1R3	...	238R3	239R3
D13		0R2	1R2	...	238R2	239R2
D12		0R1	1R1	...	238R1	239R1
D11		0R0	1R0	...	238R0	239R0
D10		0G5	1G5	...	238G5	239G5
D9		0G4	1G4	...	238G4	239G4
D8		0G3	1G3	...	238G3	239G3
D7	C7	0G2	1G2	...	238G2	239G2
D6	C6	0G1	1G1	...	238G1	239G1
D5	C5	0G0	1G0	...	238G0	239G0
D4	C4	0B4	1B4	...	238B4	239B4
D3	C3	0B3	1B3	...	238B3	239B3
D2	C2	0B2	1B2	...	238B2	239B2
D1	C1	0B1	1B1	...	238B1	239B1
D0	C0	0B0	1B0	...	238B0	239B0

Note. In 16-bit Interface Type mode, D[7:0] must be assigned to DB[8:1] pads and D[15:8] must be assigned to DB[17:10] pads.

See Table 6. Signal pads for logic Interface for more information.

**Table 48. 9-bit Parallel interface for 565 1/2 formats (MDT = 00)**

count	0	1	2	3	4	...	359	480
D/CX	0	1	1	1	1	...	1	1
D17	C7	0R4	0G2	1R4	1G2	...	239R4	239G2
D16	C6	0R3	0G1	1R3	1G1	...	239R3	239G1
D15	C5	0R2	0G0	1R2	1G0	...	239R2	239G0
D14	C4	0R1	0B4	1R1	1B4	...	239R1	239B4
D13	C3	0R0	0B3	1R0	1B3	...	239R0	239B3
D12	C2	0G5	0B2	1G5	1B2	...	239G5	239B2
D11	C1	0G4	0B1	1G4	1B1	...	239G4	239B1
D10	C0	0G3	0B0	1G3	1B0	...	239G3	239B0
D9								

**Table 49. 18-bit Parallel interface type for 565 1/1 formats (MDT = 00)**

count	0	1	2	...	239	240
D/CX	0	1	1	...	1	1
D17		0R4	1R4		238R4	239R4
D16		0R3	1R3		238R3	239R3
D15		0R2	1R2	...	238R2	239R2
D14		0R1	1R1	...	238R1	239R1
D13		0R0	1R0	...	238R0	239R0
D12		0G5	1G5	...	238G5	239G5
D11		0G4	1G4	...	238G4	239G4
D10		0G3	1G3	...	238G3	239G3
D9		0G2	1G2	...	238G2	239G2
D8		0G1	1G1	...	238G1	239G1
D7	C7	0G0	1G0	...	238G0	239G0
D6	C6	0B4	1B4	...	238B4	239B4
D5	C5	0B3	1B3	...	238B3	239B3
D4	C4	0B2	1B2	...	238B2	239B2
D3	C3	0B1	1B1	...	238B1	239B1
D2	C2	0B0	1B0	...	238B0	239B0
D1	C1			...		
D0	C0			...		

Note. In 18-bit Interface Type mode, Command bits (C[7:0]) must be assigned to DB[8:1]. See Table 6. Signal pads for logic Interface for more information.

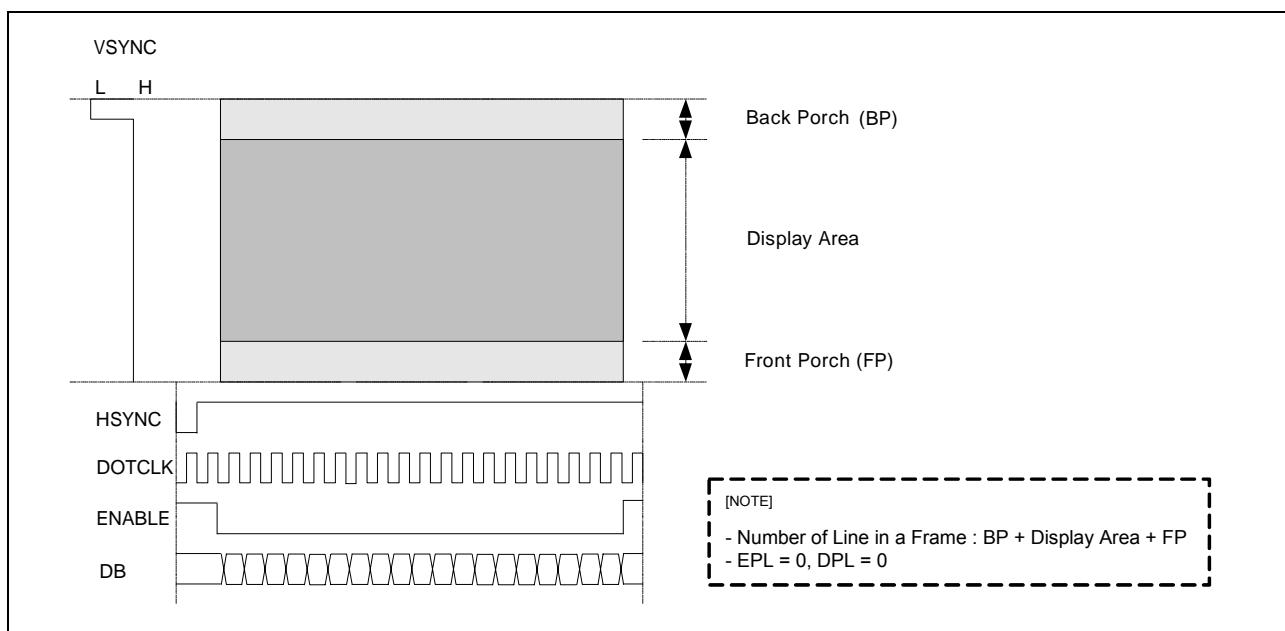
### 3.3. RGB INTERFACE

#### 3.3.1. Motion Picture Display

S6D04M0 incorporates RGB interface to display motion pictures and GRAM to store data for display.

The RGB interface is performed in synchronization with VSYNC, HSYNC, and DOTCLK.

In the period between the completion of displaying one frame data and the next VSYNC signal, the display status will remain in front porch period.



**Figure 56. RGB interface**

Note1 . For RGB interface, VSYNC, HSYNC, DOTCLK should be supplied at much higher resolution than that of panel.

Note2 . The number of DOTCLK for 1H period must be bigger than 260.

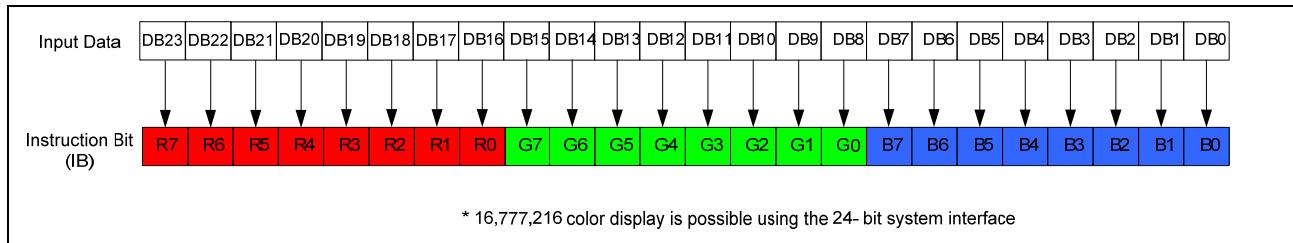
There are five timing conditions for RGB Interface that is determined according to RIM, COLMOD and each condition is described below.

**Table 50. RGB interface mode selection**

RIM	COLMOD[6:4]	RGB Interface Mode
0	111 (16M color)	24- bit RGB interface (1 transfer/pixel)
	110 (262k color)	18- bit RGB interface (1 transfer/pixel)
	101 (65k color)	16- bit RGB interface (1 transfer/pixel)
1	111 (16M color)	8- bit RGB interface (3 transfer/pixel)
	110 (262k color)	6- bit RGB interface (3 transfer/pixel)

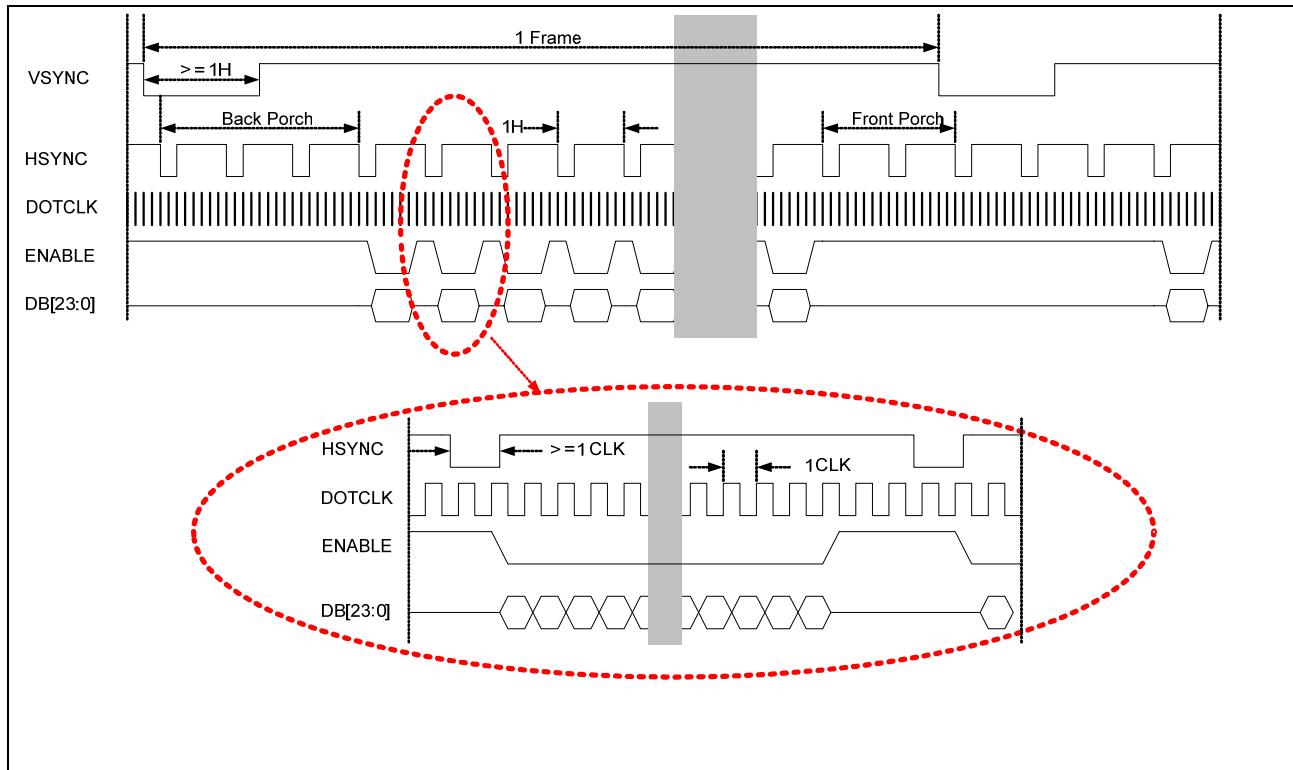
### 3.3.2. 24-bit RGB Interface (VFPP=111, RIM=0)

#### 3.3.2.1. Bit Assignment



**Figure 57.** Bit assignment of GRAM data on 24bit RGB interface

#### 3.3.2.2. Timing Diagram



**Figure 58.** Timing diagram of 24bit RGB interface

Note. The number of DOTCLK for 1H period must be bigger than 260.

### 3.3.3. 18-bit RGB Interface (VFPP=110, RIM=0)

#### 3.3.3.1. Bit Assignment

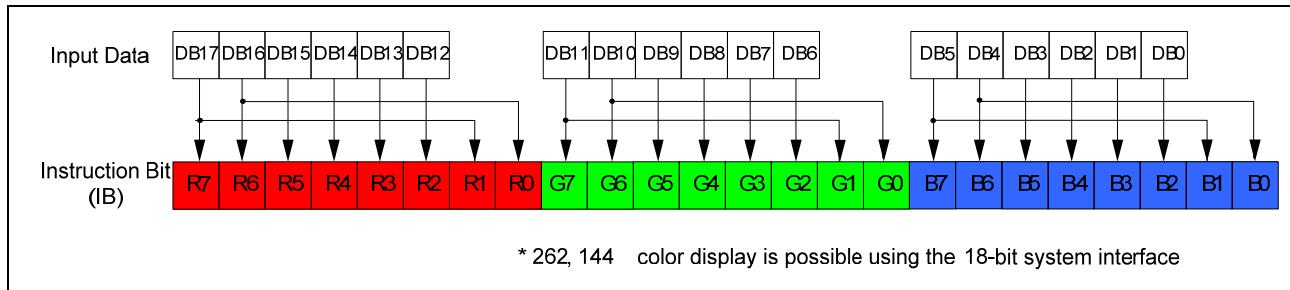


Figure 59. Bit assignment of GRAM data on 18bit RGB interface

#### 3.3.3.2. Timing Diagram

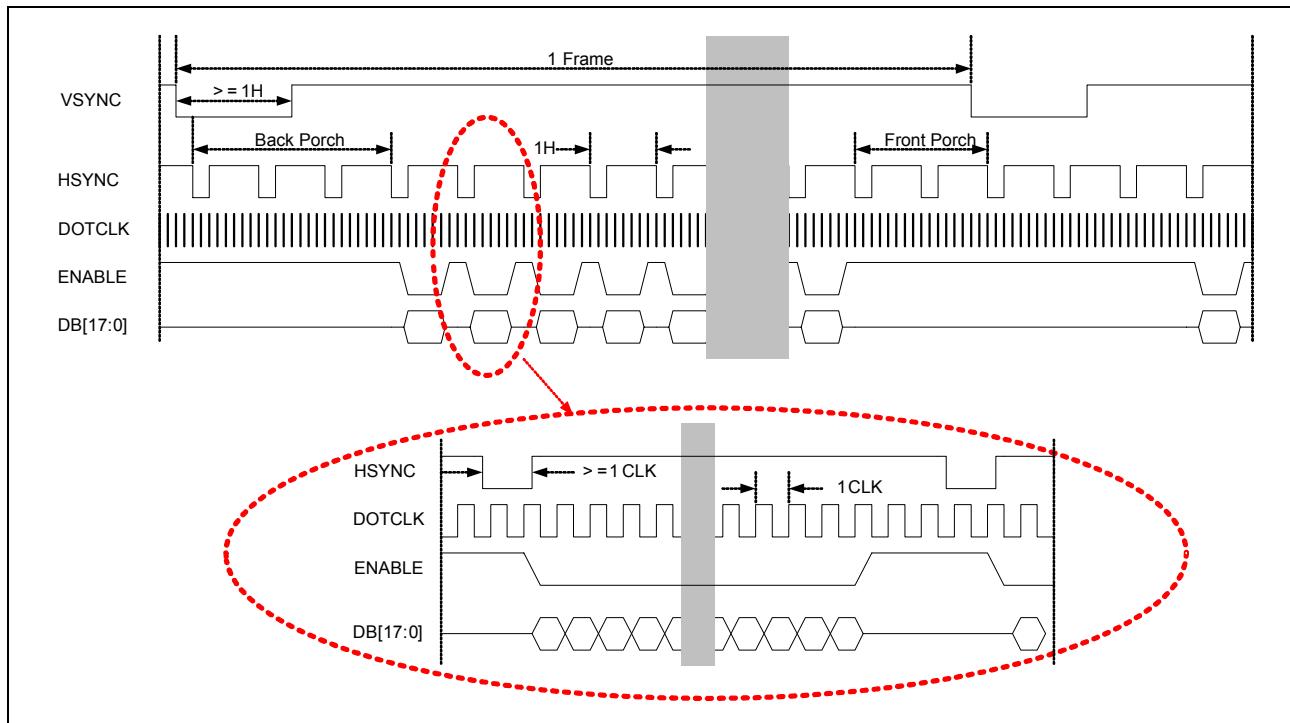
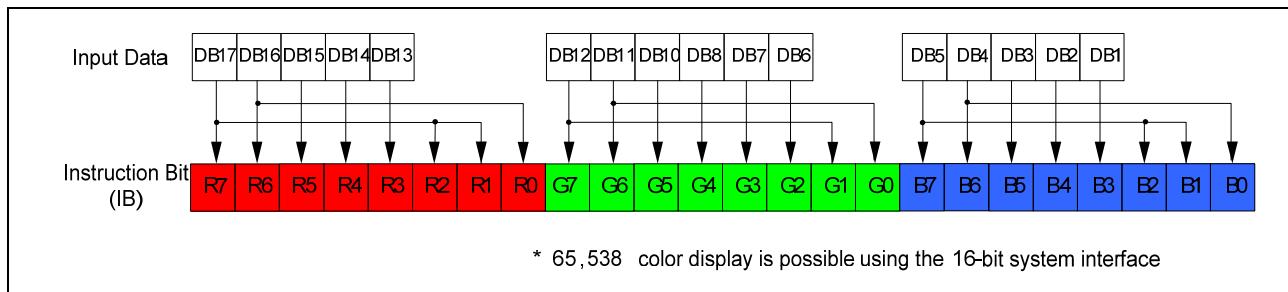


Figure 60. Timing diagram of 18bit RGB interface

Note. The number of DOTCLK for 1H period must be bigger than 260.

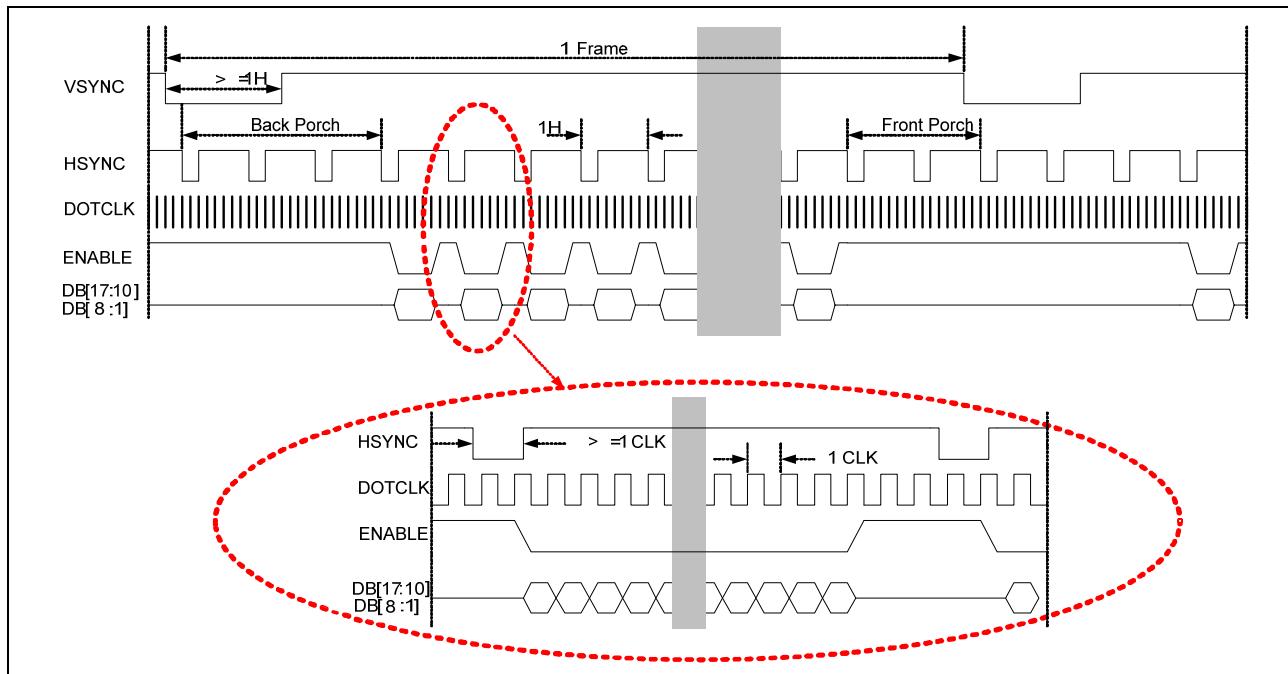
### 3.3.4. 16-bit RGB Interface (VFPP=101, RIM=0)

#### 3.3.4.1. Bit Assignment



**Figure 61.** Bit assignment of GRAM data on 16bit RGB interface

#### 3.3.4.2. Timing Diagram

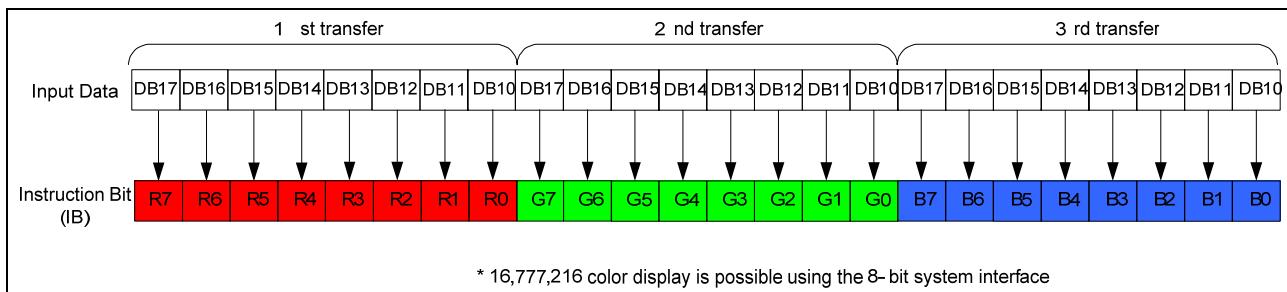


**Figure 62.** Timing diagram of 16bit RGB interface

### 3.3.5. 8-bit RGB Interface (VFPP=111, RIM=1)

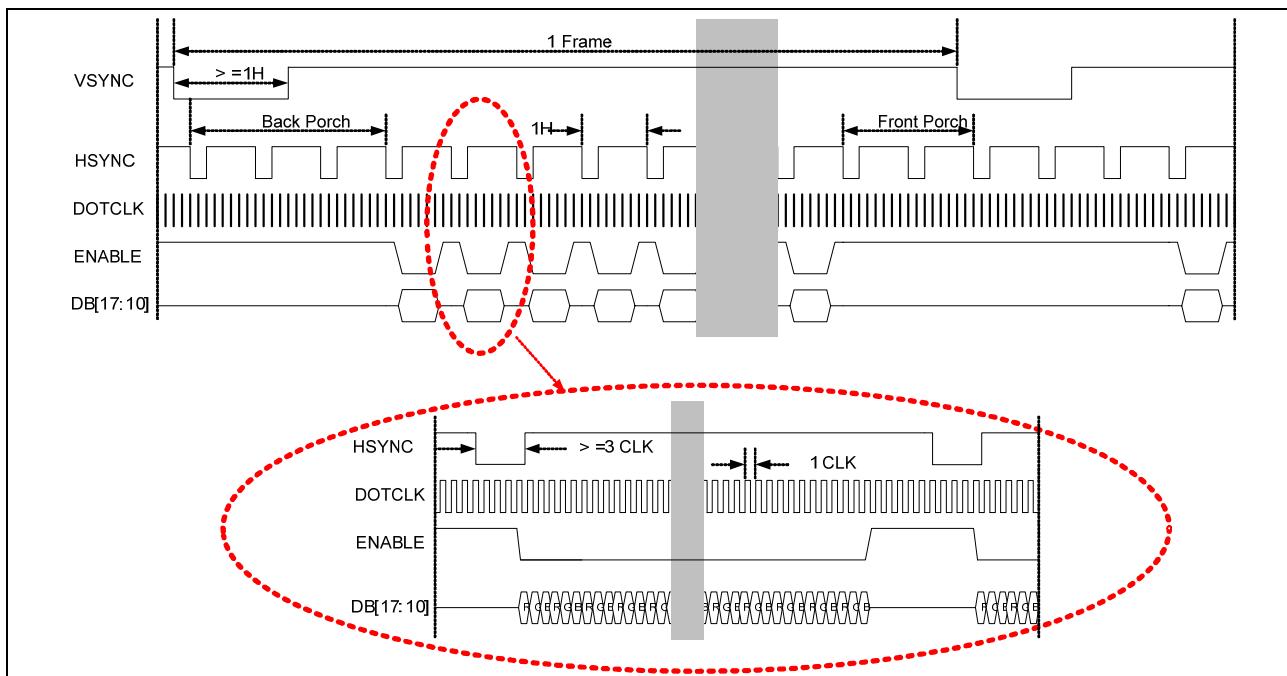
In order to transfer data on 8bit RGB Interface there should be three transfers.

#### 3.3.5.1. Bit Assignment



**Figure 63.** Bit assignment of GRAM data on 8bit RGB interface

#### 3.3.5.2. Timing Diagram



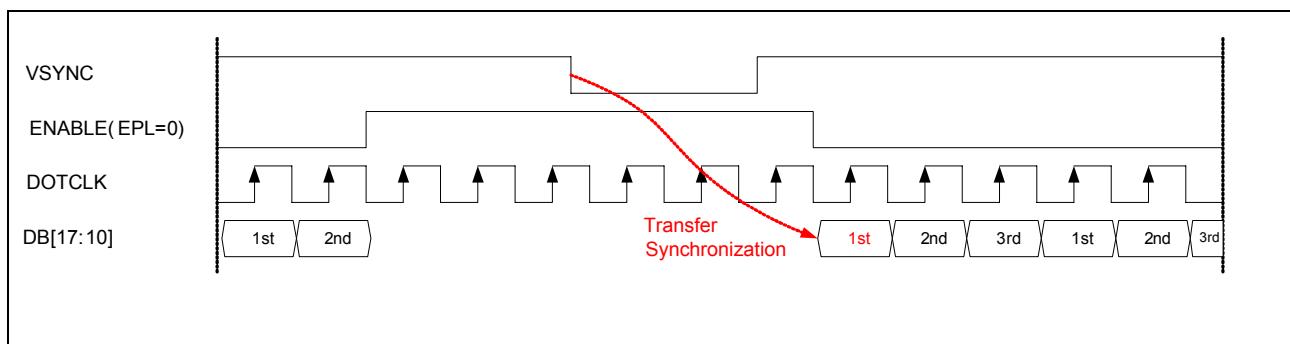
**Figure 64.** Timing diagram of 8-bit RGB interface

Note1. Three clocks are regarded as one clock for transfer when data is transferred in 8-bit interface.

VSYNC, HSYNC, ENABLE, DOTCLK, and DB[17:10] should be transferred in units of three clocks.

Note2. The number of DOTCLK for 1H period must be bigger than (260x3).

### 3.3.5.3. Transfer Synchronization



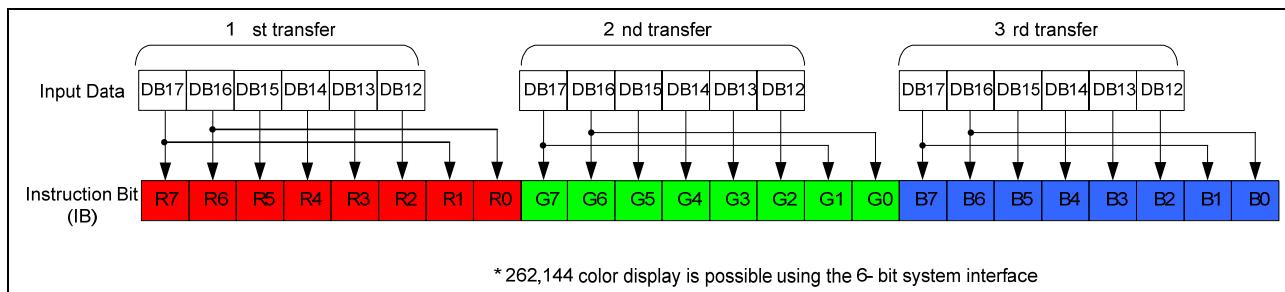
**Figure 65. Transfer synchronization function in 8-bit RGB interface mode**

Note. The figure above shows Transfer Synchronization functions for 8bit RGB Interface. S6D04M0 has a transfer counter internally to count 1st, 2nd and 3rd data transfer of 8bit RGB Interface. The transfer counter is reset on the falling edge of VSYNC and enters the 1st data transmission state. Transfer mismatch can be corrected at every VSYNC signal assertion. In this method, when data is consecutively transferred in for displaying motion pictures, the effect of transfer mismatch will be reduced and recovered by normal operation. The display is operated in units of three DOTCLKs. When DOTCLK is not input in units of pixels, clock mismatch occurs and the frame, which is operated, and the next frame are not displayed correctly.

### 3.3.6. 6-bit RGB Interface (VFPP=110, RIM=1)

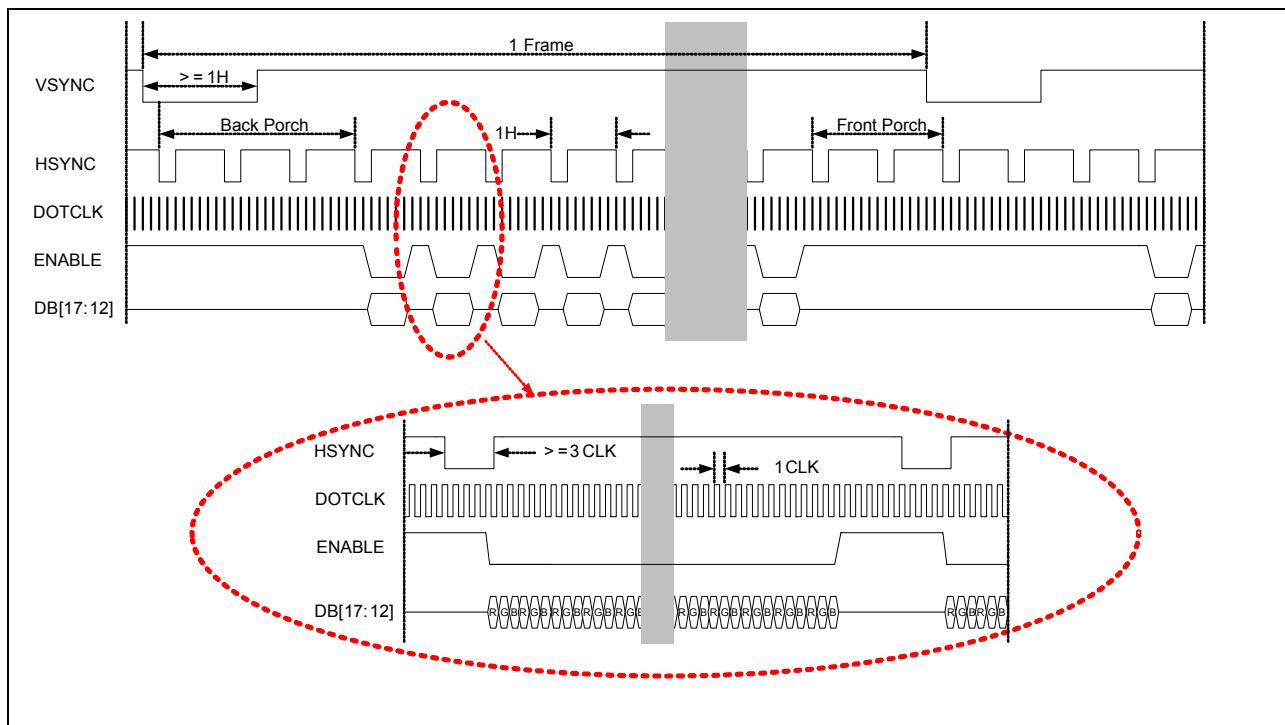
In order to transfer data on 6bit RGB Interface there should be three transfers.

#### 3.3.6.1. Bit Assignment



**Figure 66. Bit assignment of GRAM data on 6bit RGB interface**

#### 3.3.6.2. Timing Diagram



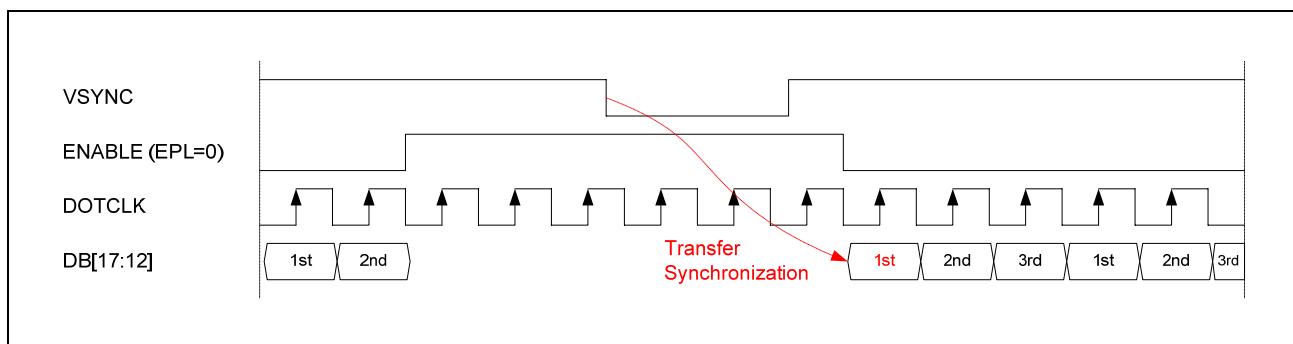
**Figure 67. Timing diagram of 6bit RGB interface**

Note1. Three clocks are regarded as one clock for transfer when data is transferred in 6-bit interface.

VSYNC, HSYNC, ENABLE, DOTCLK, and DB[17:12] should be transferred in units of three clocks.

Note2. The number of DOTCLK for 1H period must be bigger than (260x3).

### 3.3.6.3. Transfer Synchronization



**Figure 68. Transfer synchronization function in 6-bit RGB interface mode**

Note. The figure above shows Transfer Synchronization functions for 6bit RGB Interface. S6D04M0 has a transfer counter internally to count 1st, 2nd and 3rd data transfer of 6bit RGB Interface. The transfer counter is reset on the falling edge of VSYNC and enters the 1st data transmission state. Transfer mismatch can be corrected at every VSYNC signal assertion. In this method, when data is consecutively transferred in for displaying motion pictures, the effect of transfer mismatch will be reduced and recovered by normal operation. The display is operated in units of three DOTCLKs. When DOTCLK is not input in units of pixels, clock mismatch occurs and the frame, which is operated, and the next frame are not displayed correctly.

### 3.3.7. Transition Sequences between Display Modes

Transitions between Internal Clock Operation mode and External Clock Operation mode should follow the mode transition sequence shown below.

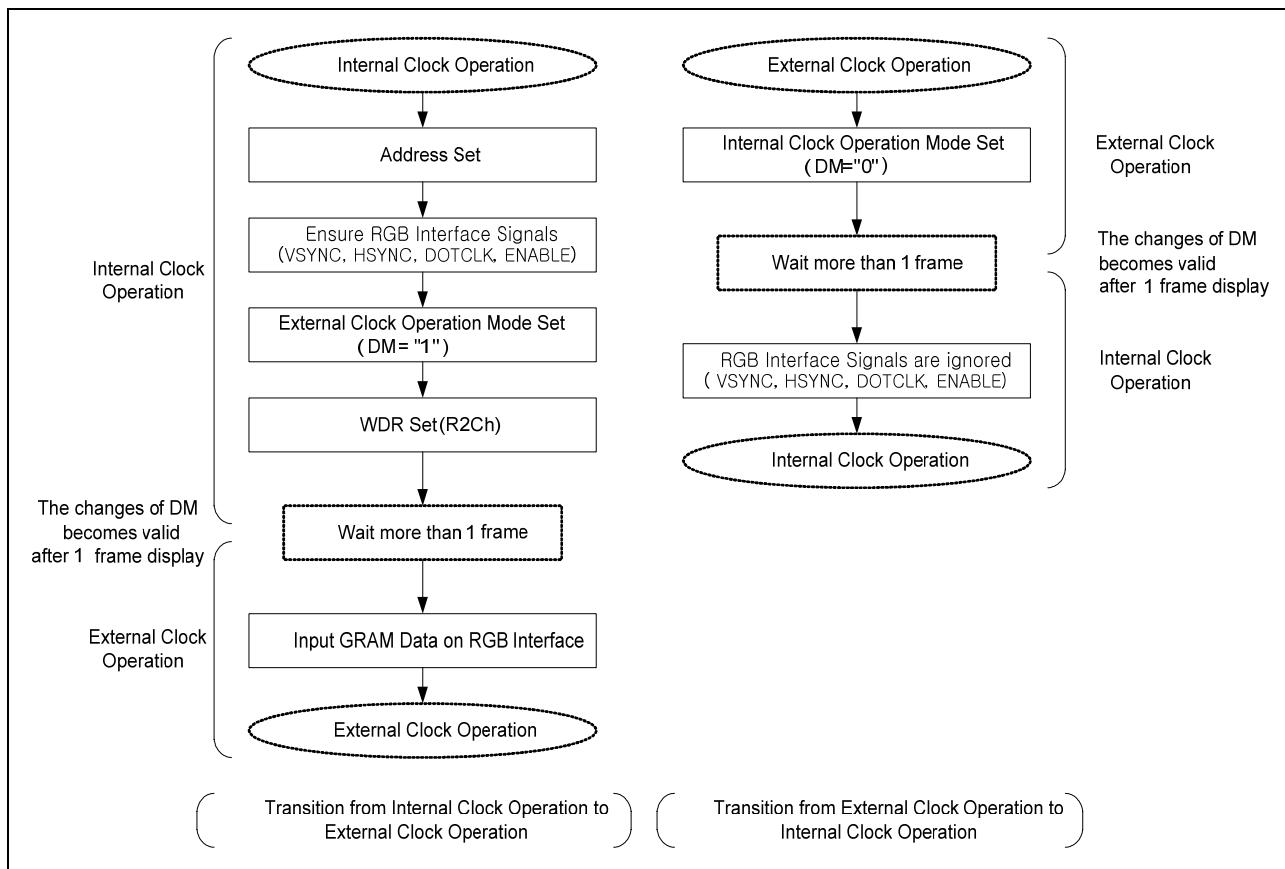


Figure 69. Transition between Internal clock operation mode and external clock operation mode

### 3.4. VSYNC INTERFACE

The S6D04M0 incorporates VSYNC interface as external interface for motion picture display.

When the VSYNC interface is selected, internal operation is normally synchronized with internal clock except operation related to frame synchronization: It is synchronized with the VSYNC signal. The data for display are written to GRAM via conventional system interface. There are some limitations on the timing and methods for writing to GRAM in VSYNC interface.

The S6D04M0 incorporates VSYNC interface, which enables motion pictures to be displayed with only the conventional system interface and the frame synchronization signal (VSYNC). This interface requires minimal changes from the conventional system to display motion pictures.

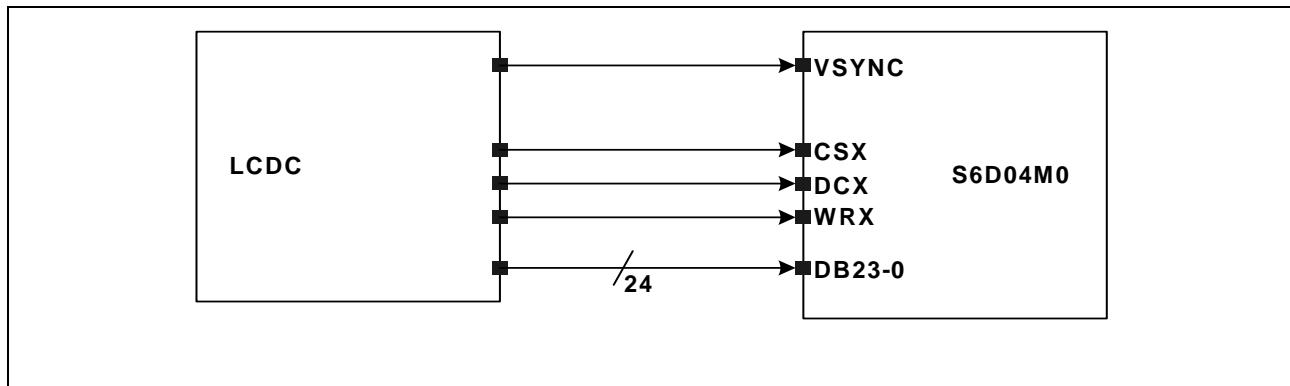


Figure 70. VSYNC interface (example: 24bit interface)

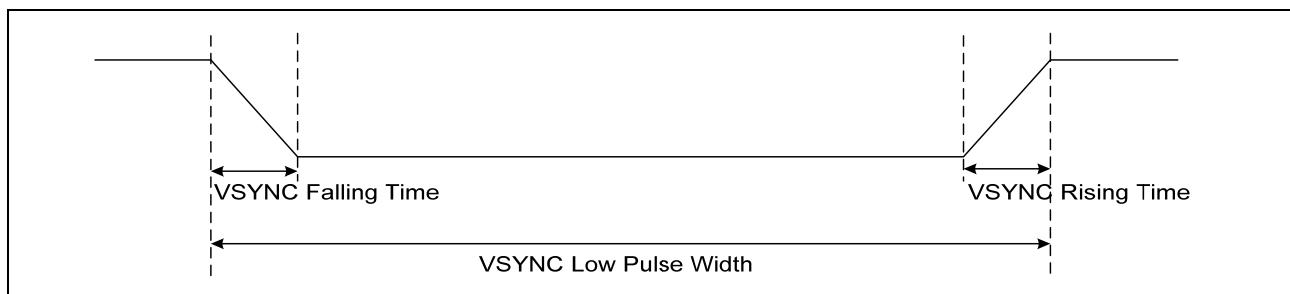


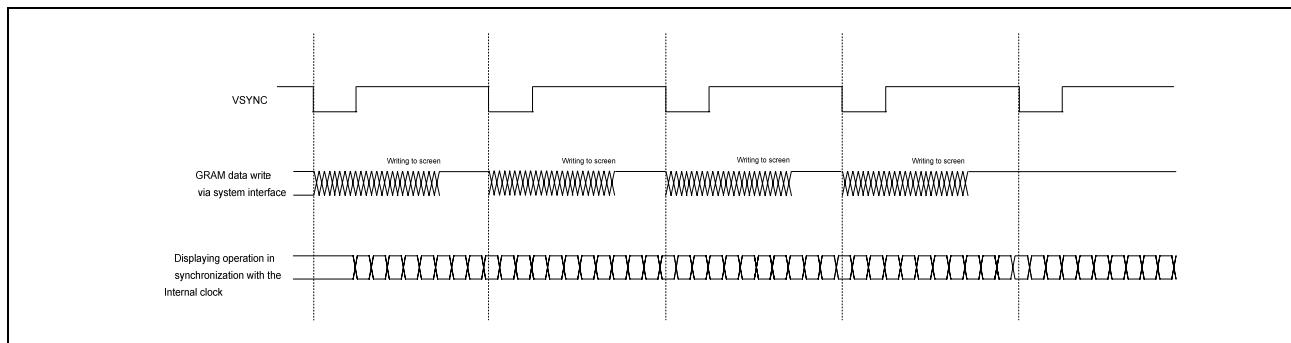
Figure 71. VSYNC signal timing

Table 51. AC characteristics of VSYNC signal

Parameter	min	max	unit
VSYNC Falling Time	-	15	ns
VSYNC Rising Time	-	15	ns
VSYNC Low Pulse Width	2-Horizontal Display Time	-	-

When VSM="1", VSYNC interface is available. In this interface the internal display operation is synchronized with VSYNC. Data for display is written to RAM via the system interface with higher speed than for internal display operation. This method enables flicker-free display of motion pictures with the conventional interface.

Display operation can be achieved by using the internal clock generated by the internal oscillator and the VSYNC input. Because all the data for display is written to RAM, only the data to be rewritten is transferred. This method reduces the amount of data transferred during motion picture display operation.



**Figure 72. Motion picture data transfer via VSYNC interface**

VSYNC interface requires taking the minimum speed for RAM writing via the system interface and the frequency of the internal clock into consideration. RAM writing should be performed with higher speed than the result obtained from the calculation shown below.

$$\text{Internal clock frequency (fosc) [Hz]} = 10\text{MHz}$$

$$= \text{Frame freq.} (\text{Display raster-row (320)} + \text{Front porch (VFP)} + \text{Back porch (VBP)}) \times \text{RTN} \times \text{CRTN} \times \text{Fluctuation}$$

$$\text{Minimum speed for RAM writing [Hz]}$$

$$> 240 \times \text{Display raster-row (320)} / \{((\text{Back porch (VBP)} + \text{Display raster-row (320)} - \text{Margin}) \times \text{RTN} \times \text{CRTN}) / 10\text{MHz}\}$$

Note: hen RAM writing does not start immediately after the falling edge of VSYNC, the time between the falling edge of VSYNC and the RAM writing start timing must also be considered.

An example is shown below.

#### Example

Display size	240RGB X 320 raster-rows
Back/Front porch	14 lines/2 lines (VBP=0001101/VFP=0000010)
OSC Frequency	10MHz fix
RTN , CTRN	22

Internal clock frequency is 10MHz. It is a fixed value.

Minimum speed for RAM writing [Hz] >  $240 \times 320 / \{((14 + 320 - 2) \text{ lines} \times 22 \times 22 \text{ clock}) / 10 \text{ MHz}\} = 4.78 \text{ MHz}$

Note1: In this case RAM writing starts immediately after the falling edge of VSYNC.

Note2: The margin for display raster-row should be two raster-rows or more at the completion of RAM writing for one frame.

Therefore, when RAM writing starting immediately after the falling edge of VSYNC is performed at 4.78 MHz or more, the data for display can be rewritten before display operation starts. This means that flicker-free display operation is achieved.

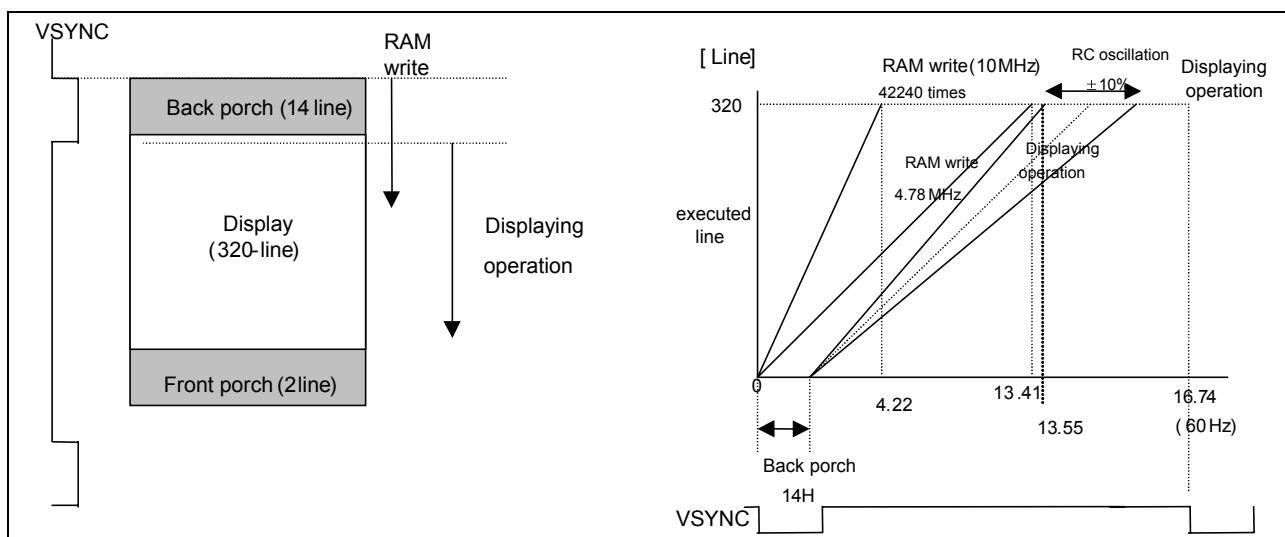
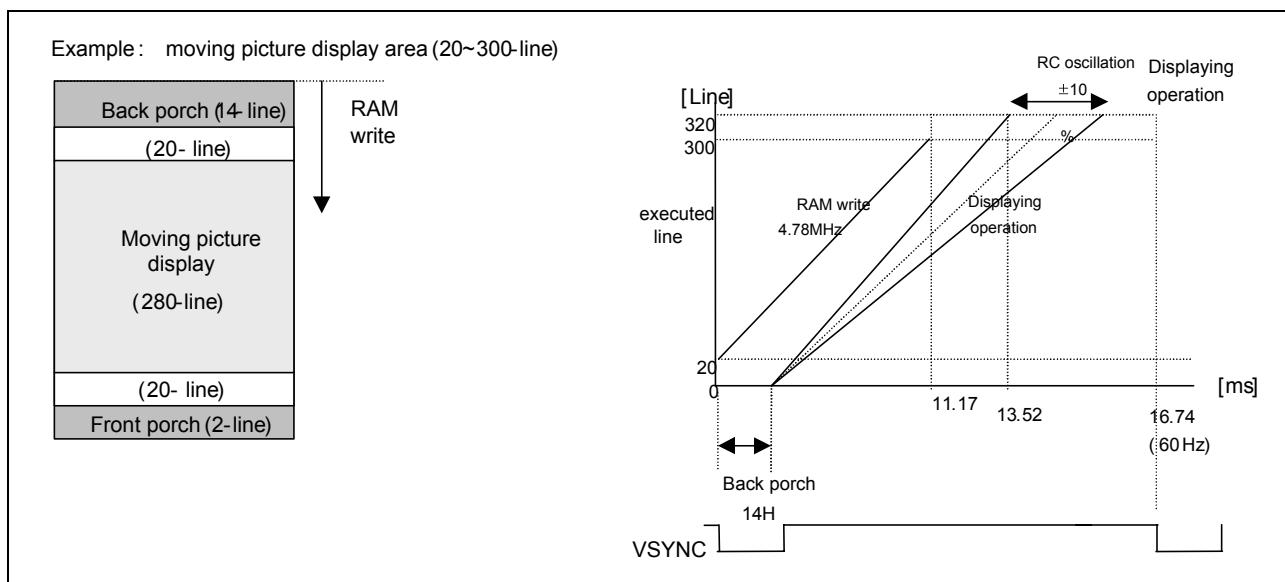


Figure 73. Operation for VSYNC interface

### 3.4.1. Usage on VSYNC interface

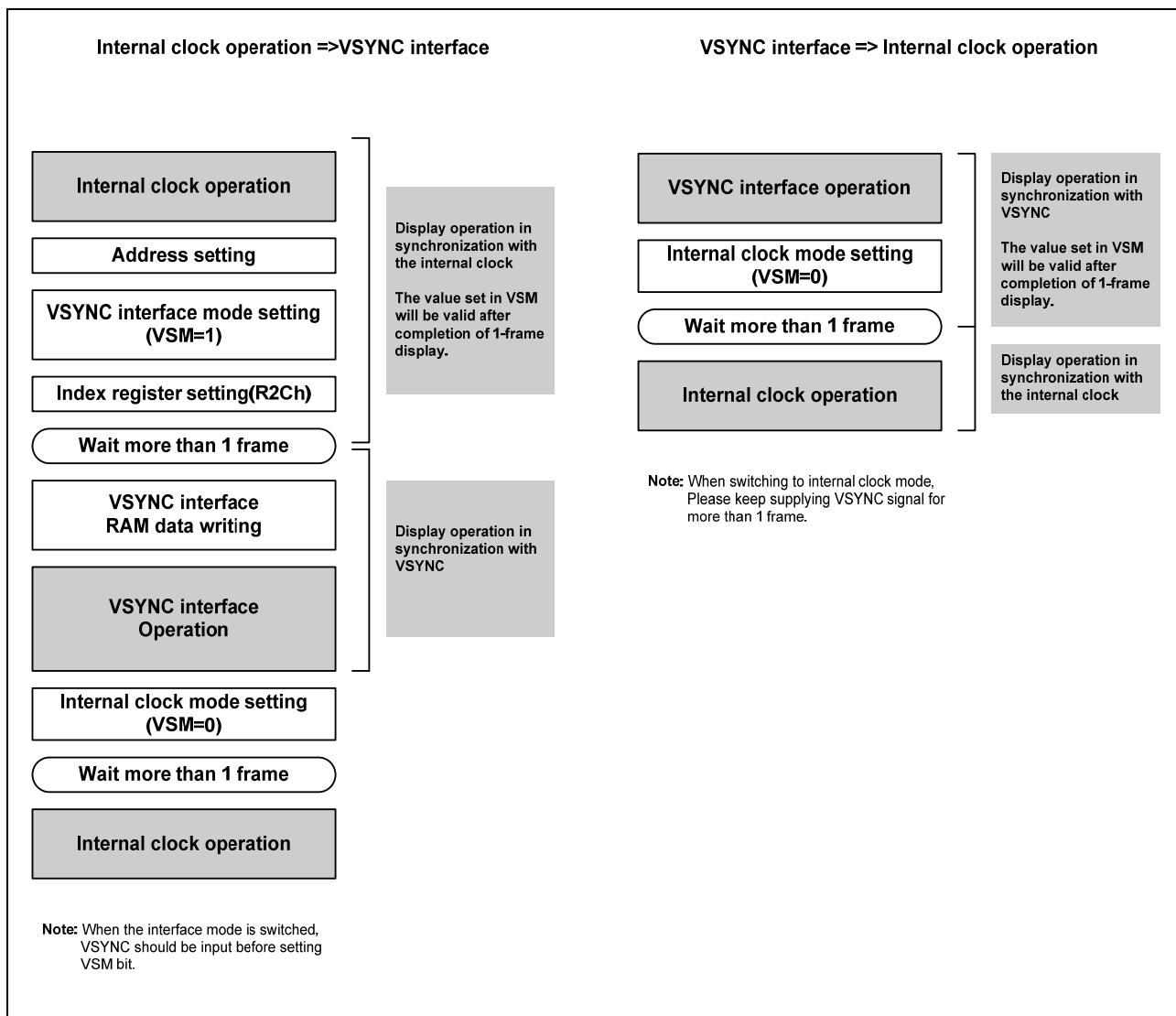
- The Example above is a calculated value. Please keep in mind that a margin for these factors is also needed. Because the variation of the internal oscillator requires a consideration.
- The Example above is a calculated value of rewriting the whole screen. A limitation of the motion picture area generates a margin for the RAM write speed.



**Figure 74. Limitation of motion picture area**

- During the period between the completion of displaying one frame data and the next VSYNC signal, the display will remain front porch period.

4. Transition between the internal operating clock mode (VSM="1") and VSYNC interface mode will be valid after the completion of the screen, which is displayed when the instruction is set.



**Figure 75. Transition between the internal operating clock mode and VSYNC interface mode**

5. Partial display and vertical scroll functions are not available on VSYNC interface mode.  
6. The VSYNC interface is performed by the method above.

## CHAPTER 4

# FUNCTIONAL DESCRIPTION

- 4.1 Power
- 4.2 Source
- 4.3 Pannel Control
- 4.4 Oscillator –System Clock Generator
- 4.5 Display Data RAM
- 4.6 Reset
- 4.7 Sleep Out
- 4.8 MTP Control
- 4.9 8-color Display Mode
- 4.10 Instruction Setup Flow
- 4.11 Colour Depth Conversion Look Up Table
- 4.12 Tearing Effect Output Line
- 4.13 MIE Function

# 4 FUNCTIONAL DESCRIPTION

## 4.1. POWER

### 4.1.1. Power ON / OFF sequence

VDD3 and VCI can be applied in any order.

VDD3 and VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and VDD3 must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDD3 or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note:

There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

There will be no abnormal visible effects on the display between the end of Power On Sequence and before the reception of Sleep Out command. Same is the case between receiving Sleep In command and Power Off Sequence.

If RESX line is not held stable by host during Power On Sequence, it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise, function is not guaranteed.

The power on/off sequence is illustrated in the next pages.

#### 4.1.1.1. Case-1 RESX line is held High or Unstable by Host at Power On

If RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and VDD3 have been applied – otherwise, correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

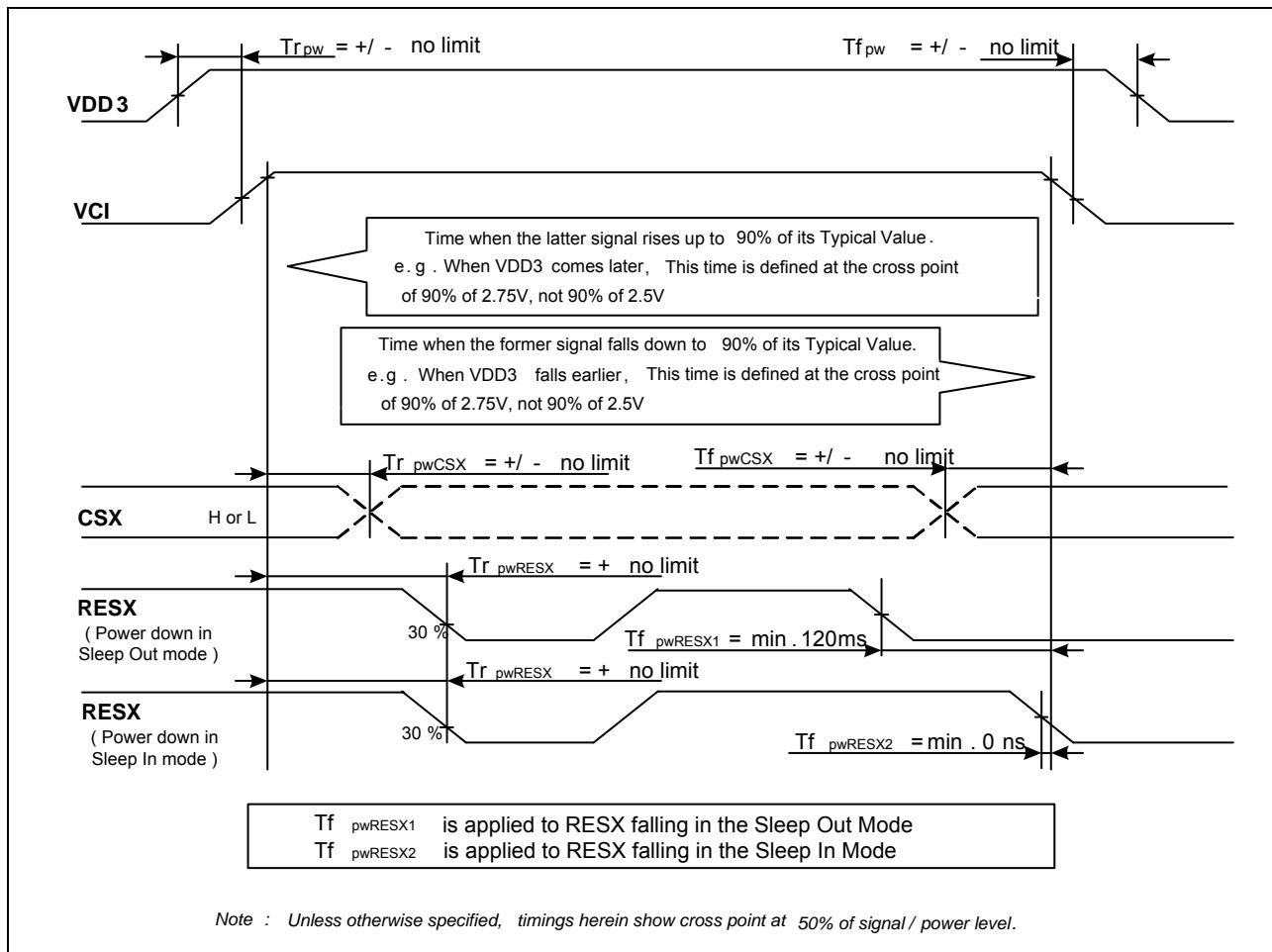


Figure 76. RESX line is held high or unstable by host at power on

#### 4.1.1.2. Case-2 RESX line is held Low by Host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10 $\mu$ sec after both VCI and VDD3 have been applied

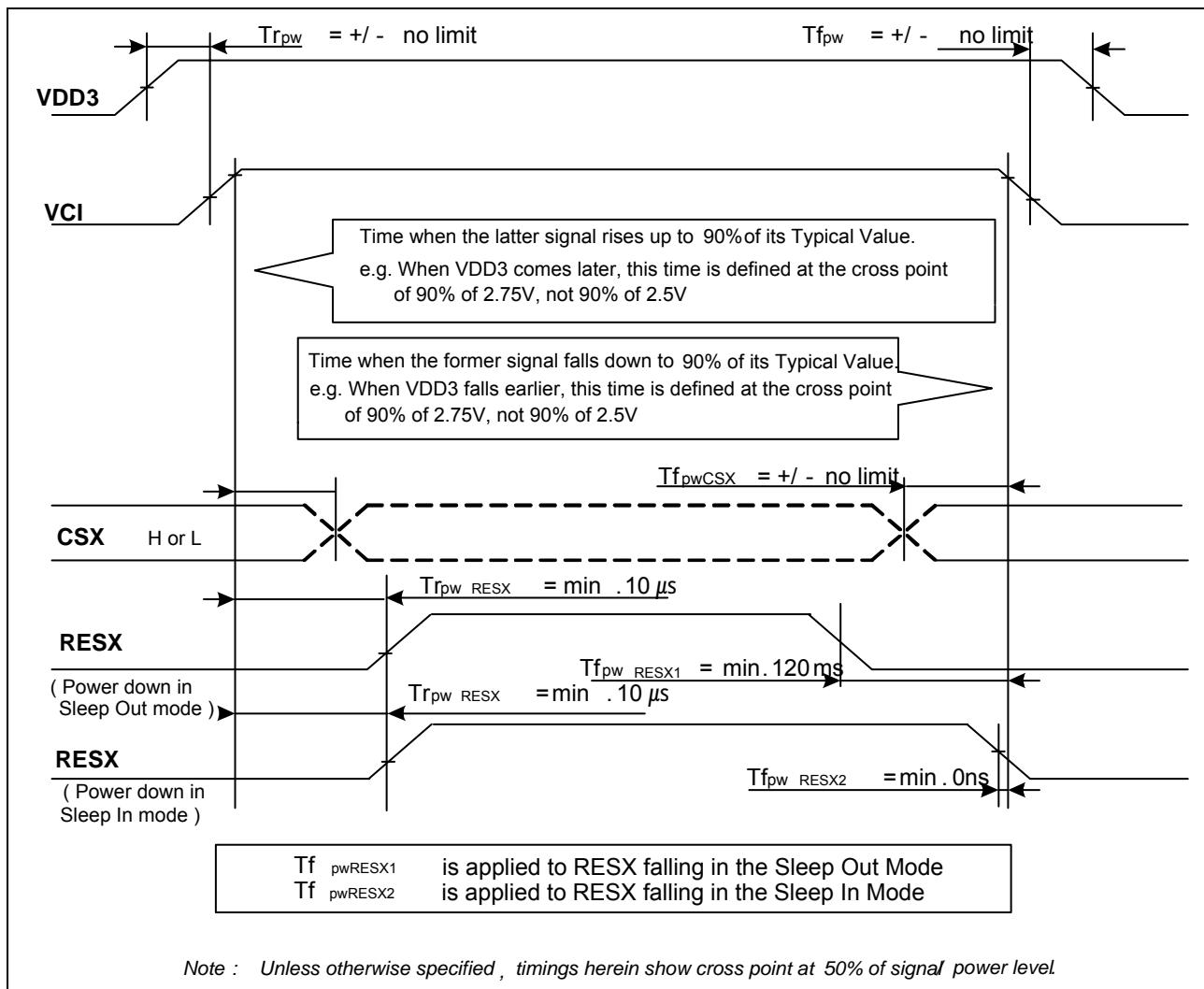


Figure 77. RESX line is held low by host at power on

#### 4.1.2. Abrupt Power Off

The abrupt power-off represents a situation where, for e.g., a battery is removed without the expected power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abrupt power-off, the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until "Power-On Sequence" powers it up.

#### 4.1.3. Power Levels

S6D04M0 supports 7 types of power-consumption modes. Each mode is described as follows:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out

In this mode, the display is able to show maximum 16,777,216 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out

In this mode, part of the display is used with maximum 16,777,216 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out

In this mode, the full display area is used but with 8 colors,

4. Partial Mode On, Idle Mode On, Sleep Out

In this mode, part of the display is used but with 8 colors

5. Sleep In Mode

In this mode, the booster, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDD3 power supply. Contents of the memory are safe.

6. Deep Standby Mode

In this mode, the booster, internal oscillator, panel driver circuit and power regulator circuit for memory / logic block are stopped. No circuit block in the driver IC works even though VCI and VDD3 are still on. Contents of the memory and register values are lost.

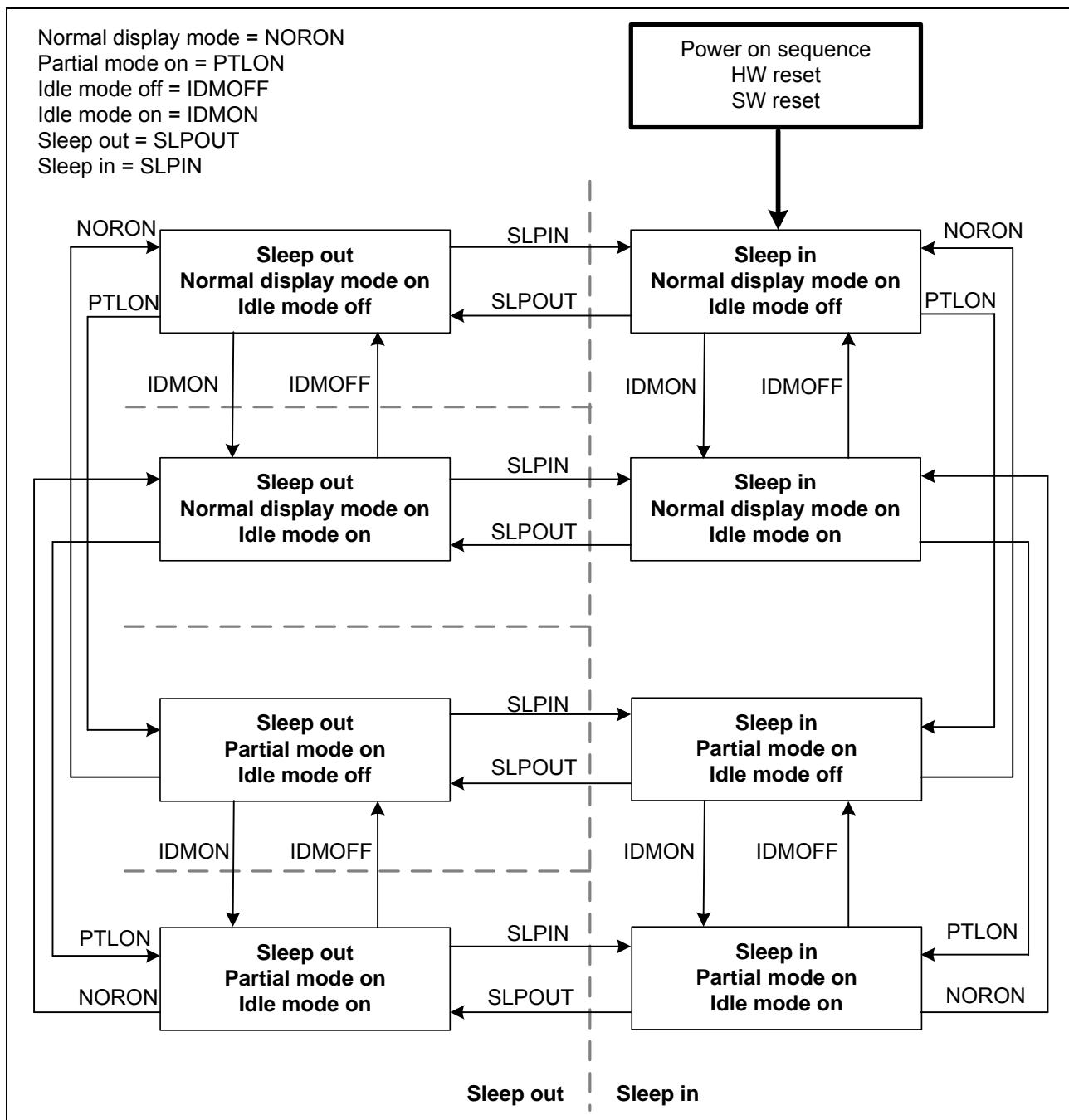
7. Power Off Mode.

In this mode, both VCI and VDD3 are removed

Note. Transition between modes 1-5 is controllable by MCU commands. Mode 6 can be escaped only by CSX toggle or hardware reset.

Mode 7 is entered only when both Power supplies are removed.

#### 4.1.4. Power Flow Chart for Different Power Modes



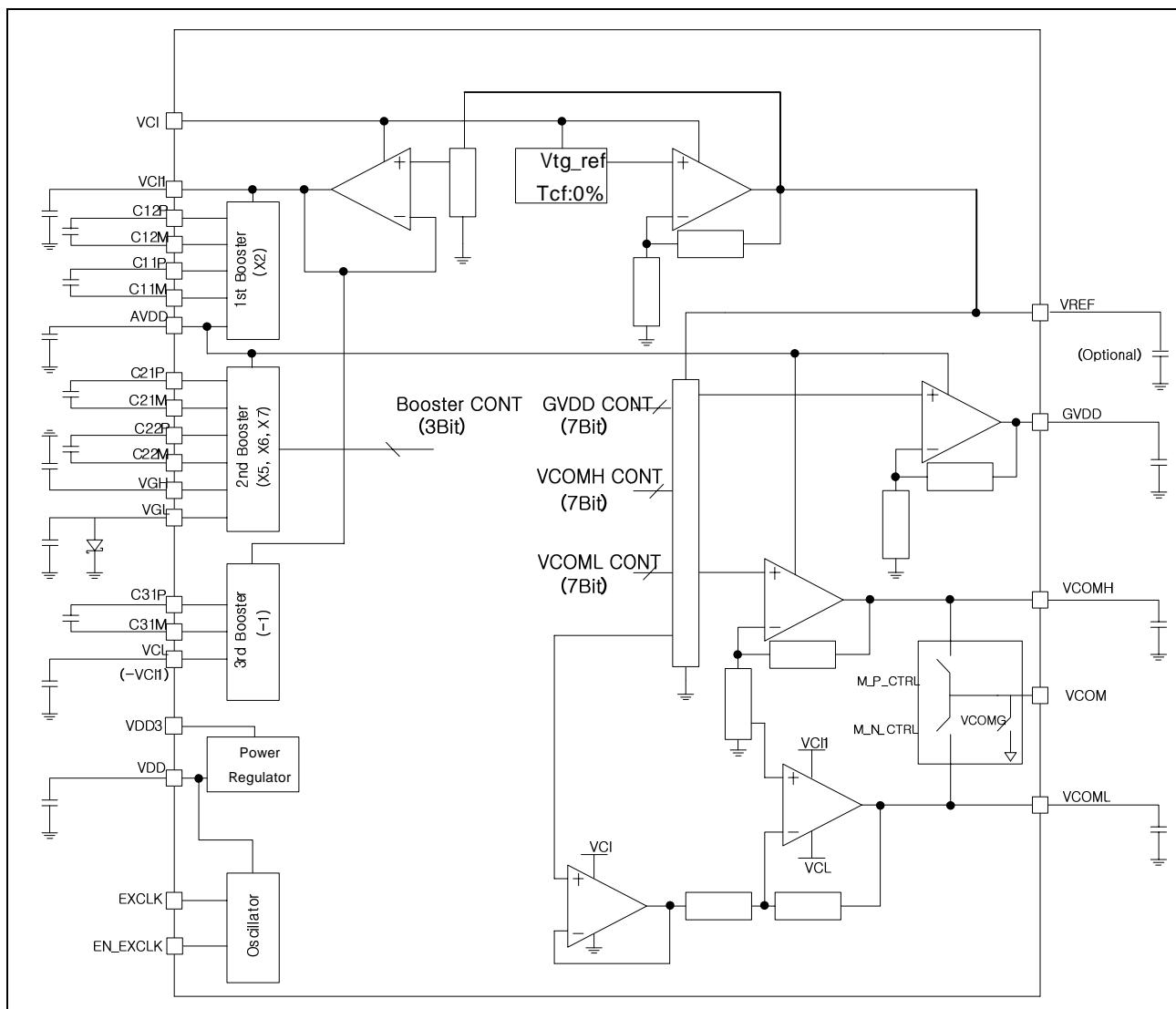
**Figure 78.** Power-on flowchart for various power modes

Note1. There is no abnormal visual effect when changing from one power mode to another power mode.

Note2. There is no limitation, which is not specified by this spec, when changing from one power mode to another power mode.

#### 4.1.5. Power Supply

The following figure shows a configuration of the voltage generation circuit of S6D04M0. The booster circuit consists of booster circuits 1 to 3. Booster circuit1 doubles input voltage supplied from VCI1 for AVDD level. Booster circuit2 makes 2.5, 3 or 3.5 times AVDD level for VGH level, and makes -1.5, -2 or -2.5 times AVDD level for VGL level. Booster circuit3 reverses the VCI1 level with respect to VSS to generate VCL level. These Booster circuits generate power supplies AVDD, VGH, VGL, and VCL. Reference voltages such as GVDD, VCOMH and VCOML are generated with VREF from the voltage adjustment circuit. Connect VCOM to the TFT panel.



**Figure 79. Configuration of the internal power-supply circuit**

Note. Use the 1uF capacitor. Schottky diode between VGL and VSS is positively necessary for making the circuitry latch-up free.

The Capacitor between VREF and VSS may be used in the case of occurring fluctuation in VCOM swing level.

#### 4.1.6. Pattern Diagrams for Voltage Setting

The following figure shows a pattern diagram for the voltage setting and an example of waveforms.

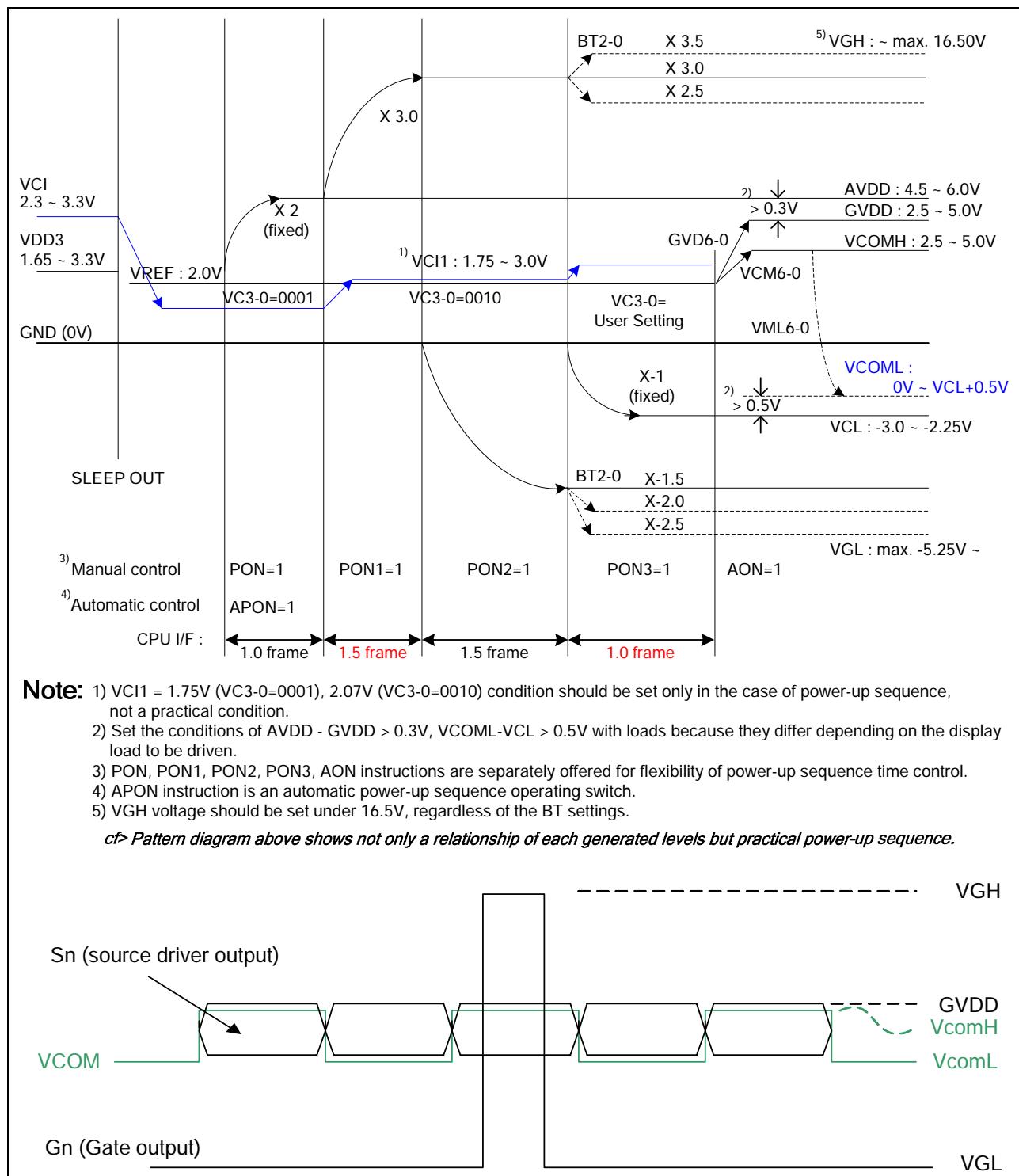


Figure 80. Power-up pattern diagram & an example of source/VCOM waveforms

#### 4.1.7. Set up Flow of Power

Apply the power in a sequential way as shown in the following figure. The settling time of the oscillation circuit, booster1/2/3 circuits, and operational amplifier depends on the external resistance or capacitance value.

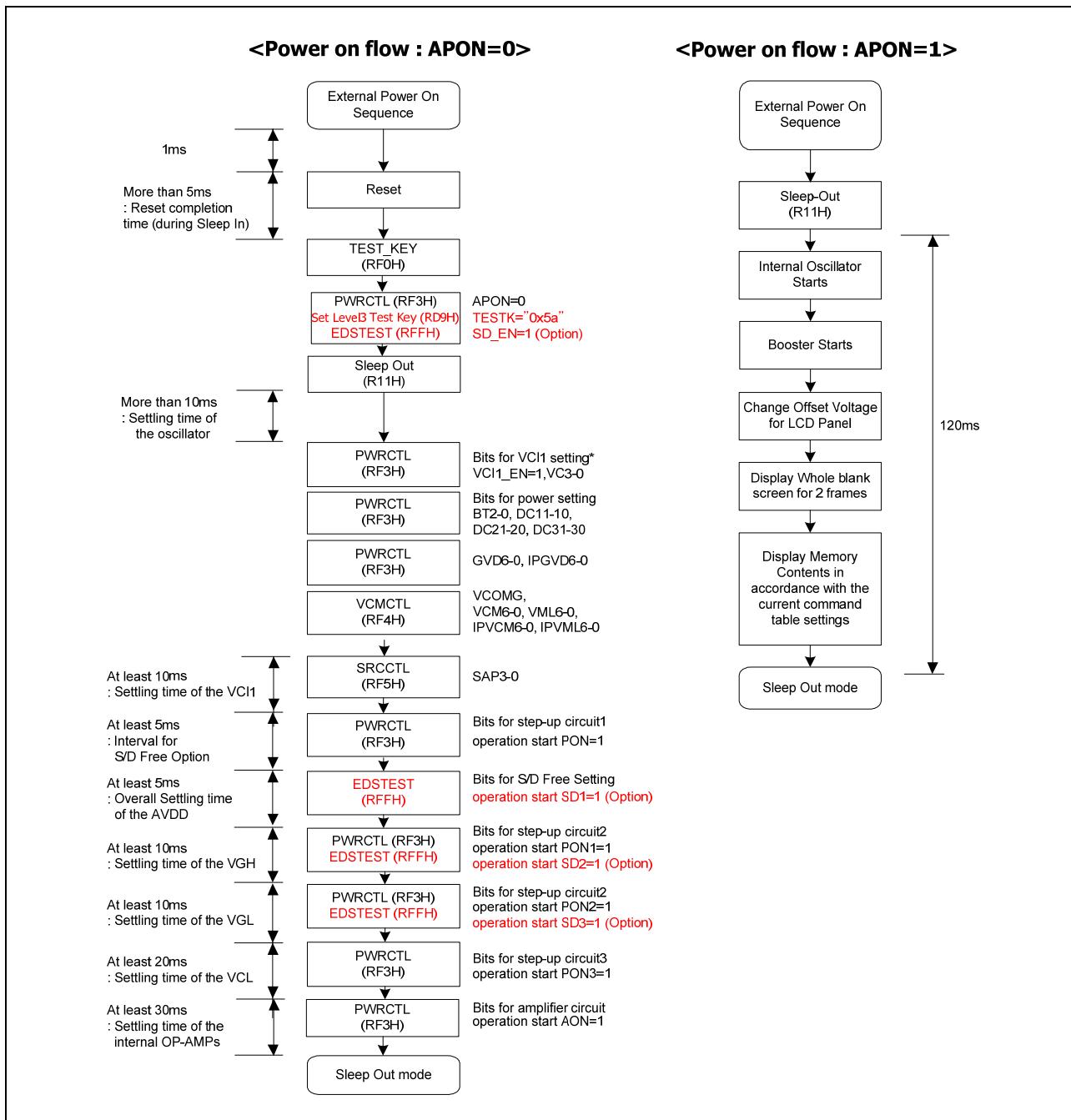


Figure 81. Setup flow of power

Note. When APON=1, the VCI1 voltage level is set to the user setting value after PON3 value is high for latch-up free sequence.

When PON3=0 : VCI1 = 1.35V after SLPOUT, 2.07V after PON1=1.

When PON3=1 : VCI1 = User setting value (VC3-0)

Power on flow (APON=0): manual power-up sequence by register setting.

Power on flow (APON=1): automatic power-up sequence.



#### 4.1.8. Deep-Standby Sequence

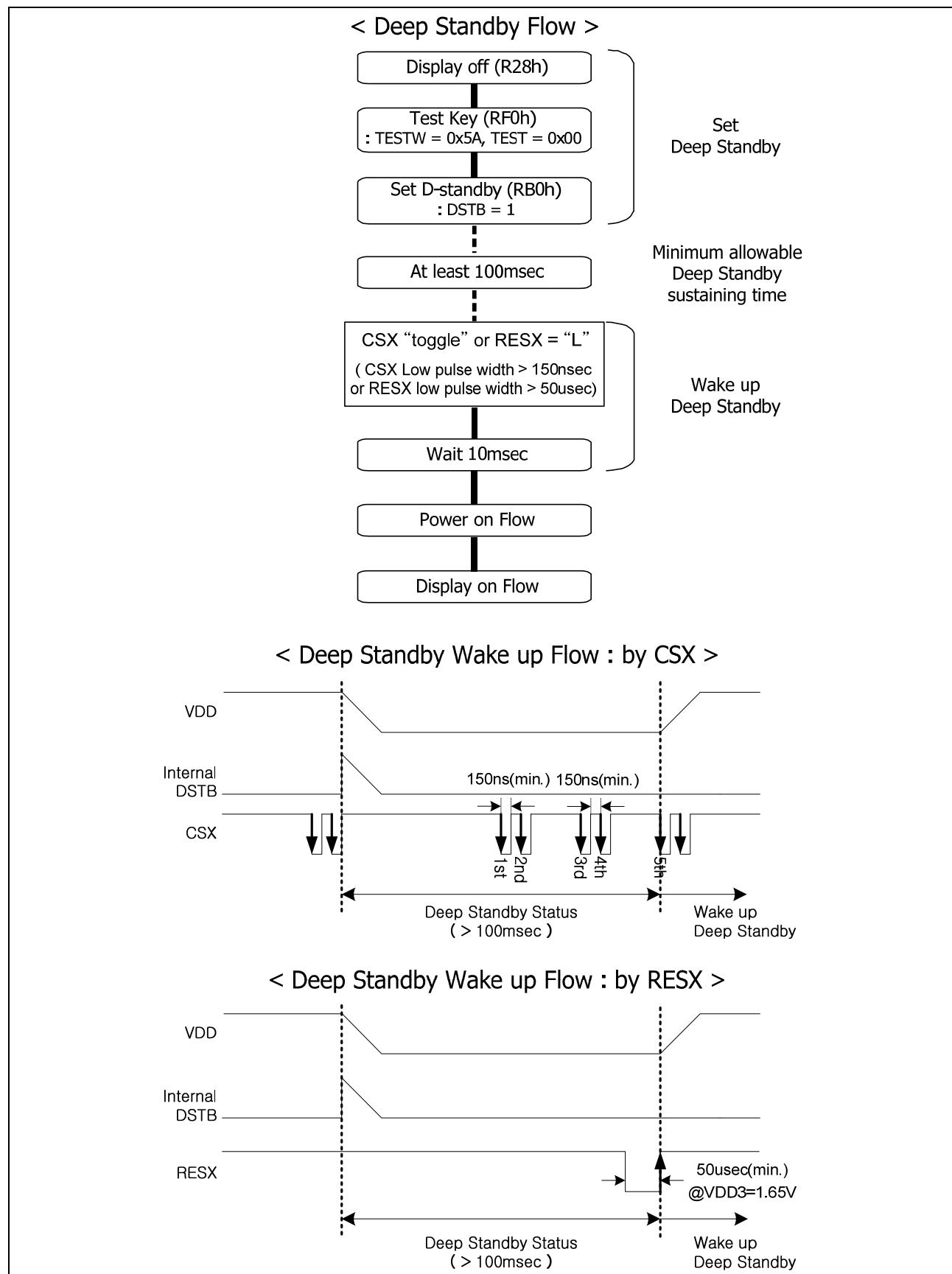


Figure 82. Deep-Standby Sequence

#### 4.1.9. Voltage Regulation Function

The S6D04M0 has an internal voltage regulator. By the use of this function, unexpected damages on internal logic circuit can be avoided. Furthermore, low power consumption can also be obtained. Detailed function description and applicable configuration are described in the following diagram.

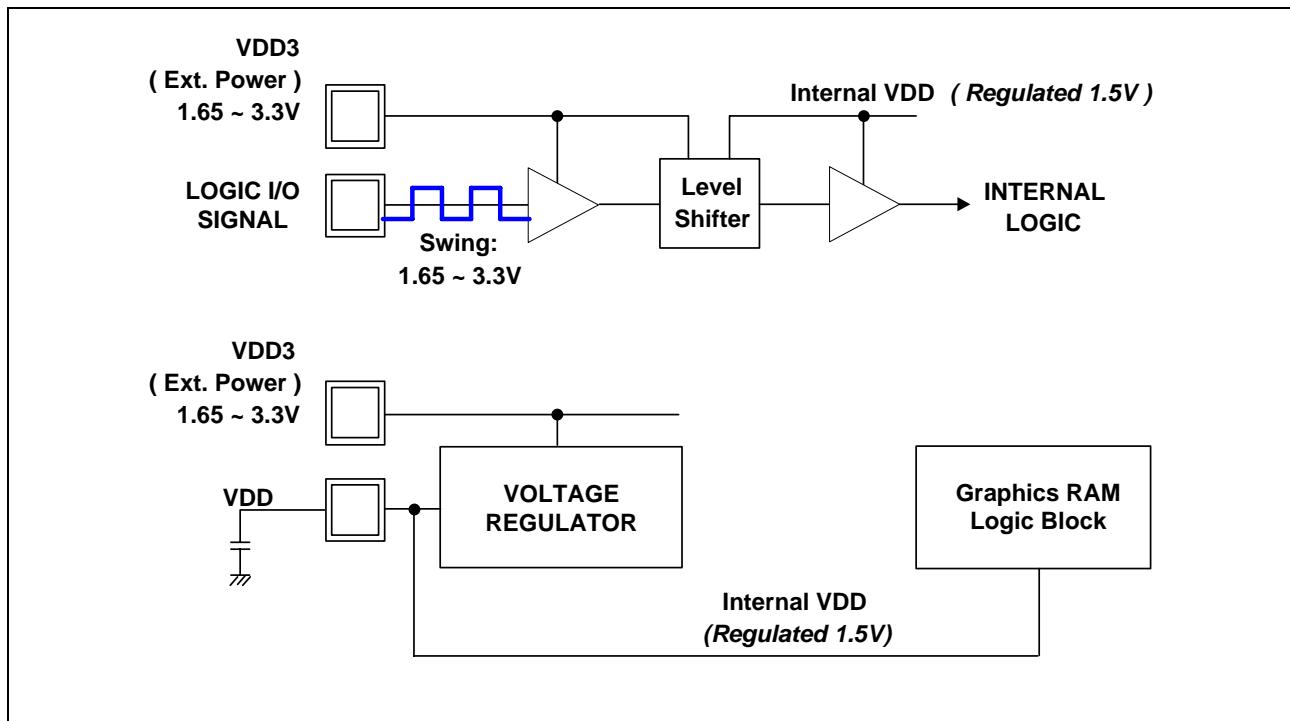


Figure 83. Voltage regulation function

## 4.2. SOURCE

### 4.2.1. Source Driver

The liquid crystal display source driver circuit consists of 720 drivers (S1 to S720).

Display pattern data is latched when 720-bit data has arrived. Then the latched data enables the source drivers to output to expected voltage level. The SS bit can change the shift direction of 720-bit data by selecting an appropriate direction for the device-mounted configuration. When less than 720 sources are required, the unused source outputs should be left open.

### 4.2.2. Gamma Adjustment Function

S6D04M0 provides the gamma adjustment function to display 16,777,216 colors simultaneously for each R/G/B color. The gamma adjustment executed by the high/ mid/ low level adjustment registers determines 13 grayscale reference levels. Furthermore, since the high-level adjustment register, mid-level adjustment register and the low-level adjustment register have the positive polarities and negative polarities, you can adjust them to match LCD panel and a gamma for each R/G/B color, respectively..

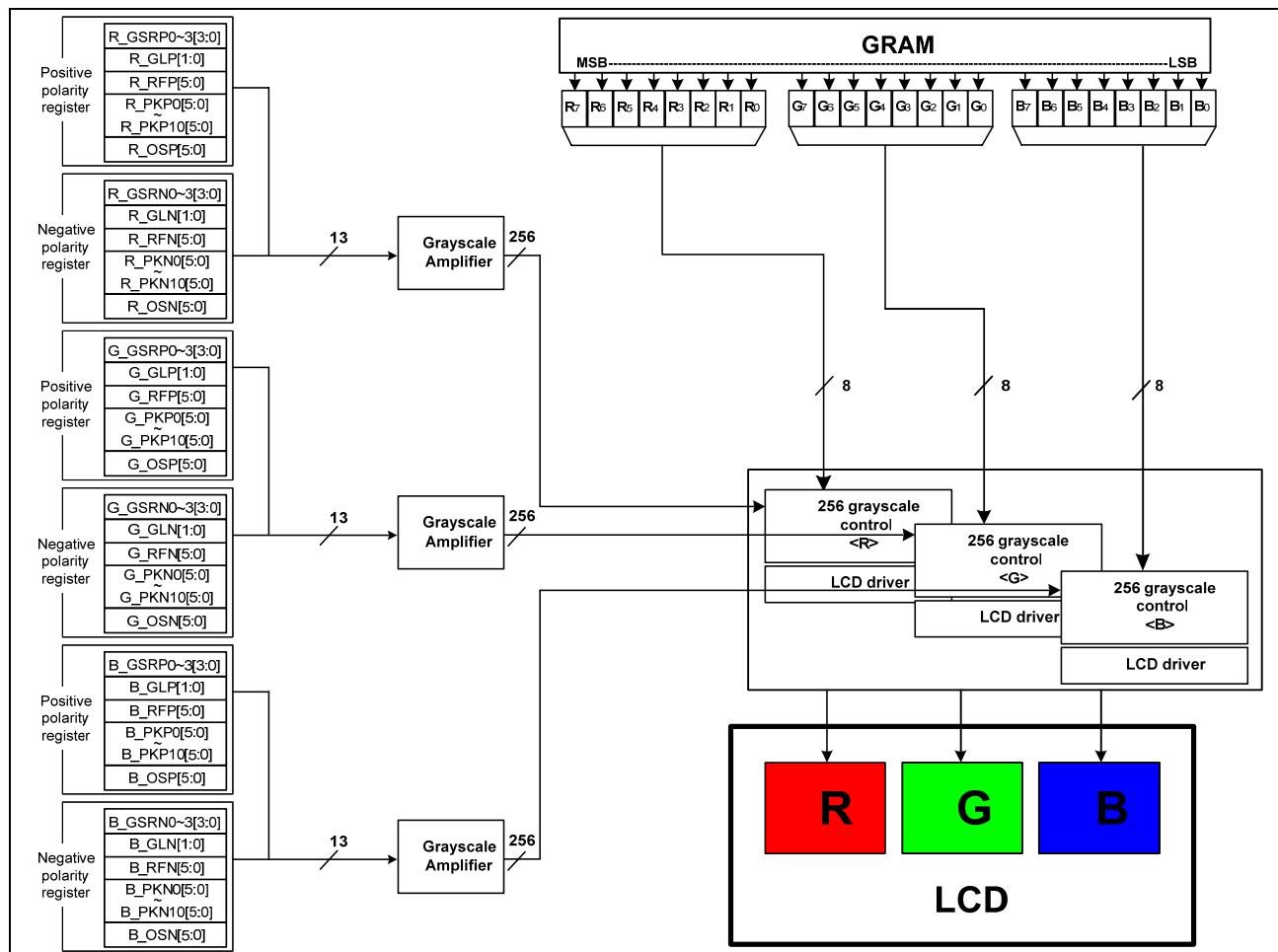


Figure 84. Block diagram of gamma adjustment function

#### 4.2.3. Gamma Curve

##### 4.2.3.1. Gamma Curve 1 (GC0)

Gamma Curve 1 (GC0), applies the function.  $y = x^{2.2}$

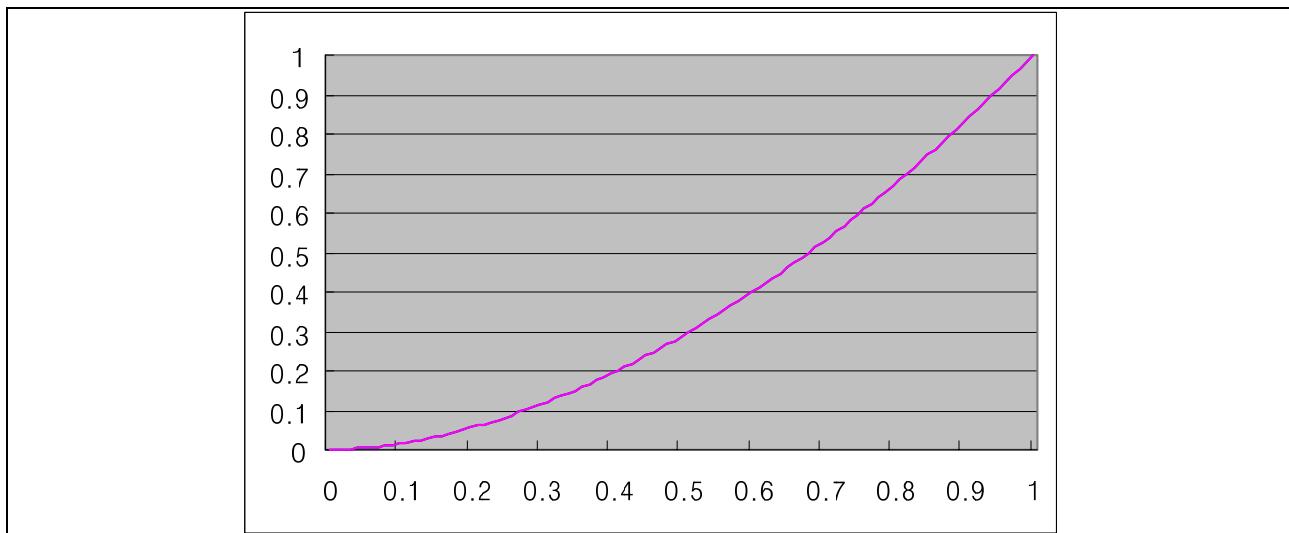


Figure 85. Gamma  $y = x^{2.2}$

##### 4.2.3.2. Gamma Curve 2 (GC1)

Gamma Curve 2 (GC1), applies the function.  $y = x^{1.8}$

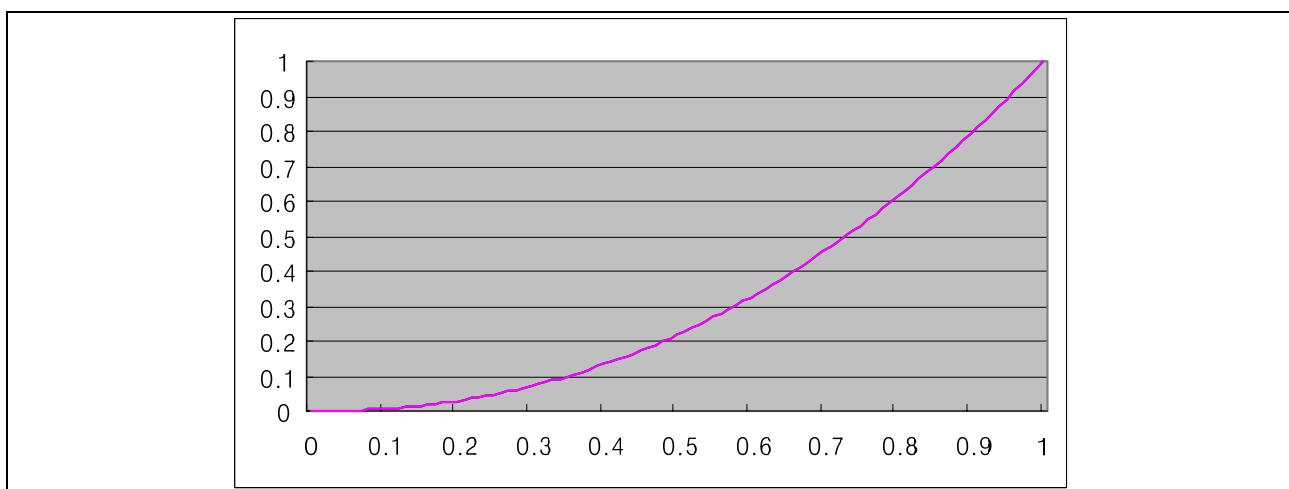


Figure 86. Gamma  $y = x^{1.8}$

#### 4.2.3.3. Gamma Curve 3(GC2)

Gamma Curve 3(GC2), applies the function.  $y = x^{2.5}$

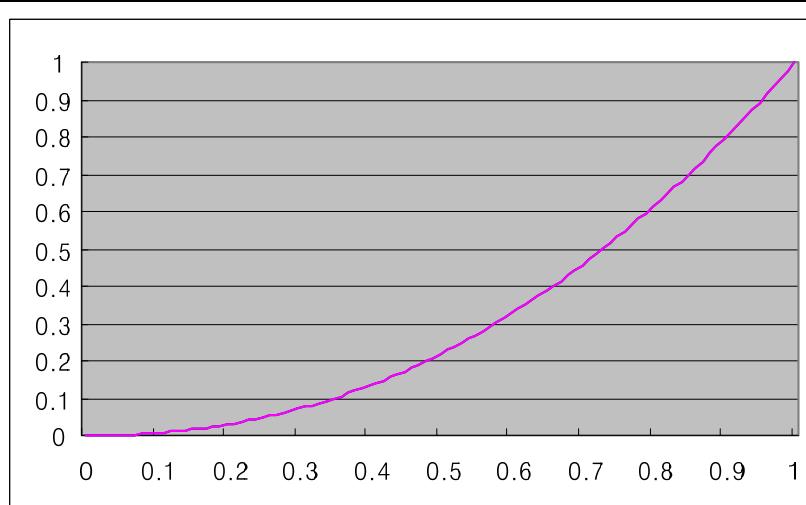


Figure 87. Gamma  $y = x^{2.5}$

#### 4.2.3.4. Gamma Curve 4 (GC3)

Gamma Curve 4 (GC3) is linear, i. e.  $y = x^1$

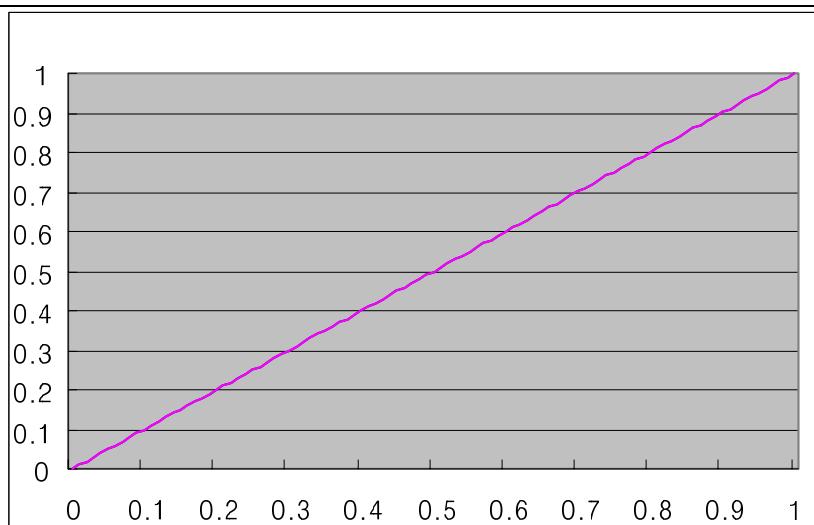


Figure 88. Gamma  $y = x^1$

#### 4.2.4. Structure of Grayscale Amplifier

The structure of grayscale amplifier is shown as below. The 13 voltage levels (VIN0-VIN12) between GVDD and VGS are determined by the reference adjustment register, the amplitude adjustment register, the x-axis symmetric adjustment register, the micro-adjustment register and the gray-shift register. Each level is split into 256 levels again by the internal ladder resistor network. As a result, grayscale amplifier generates 256 voltage levels ranging from V0 to V255.

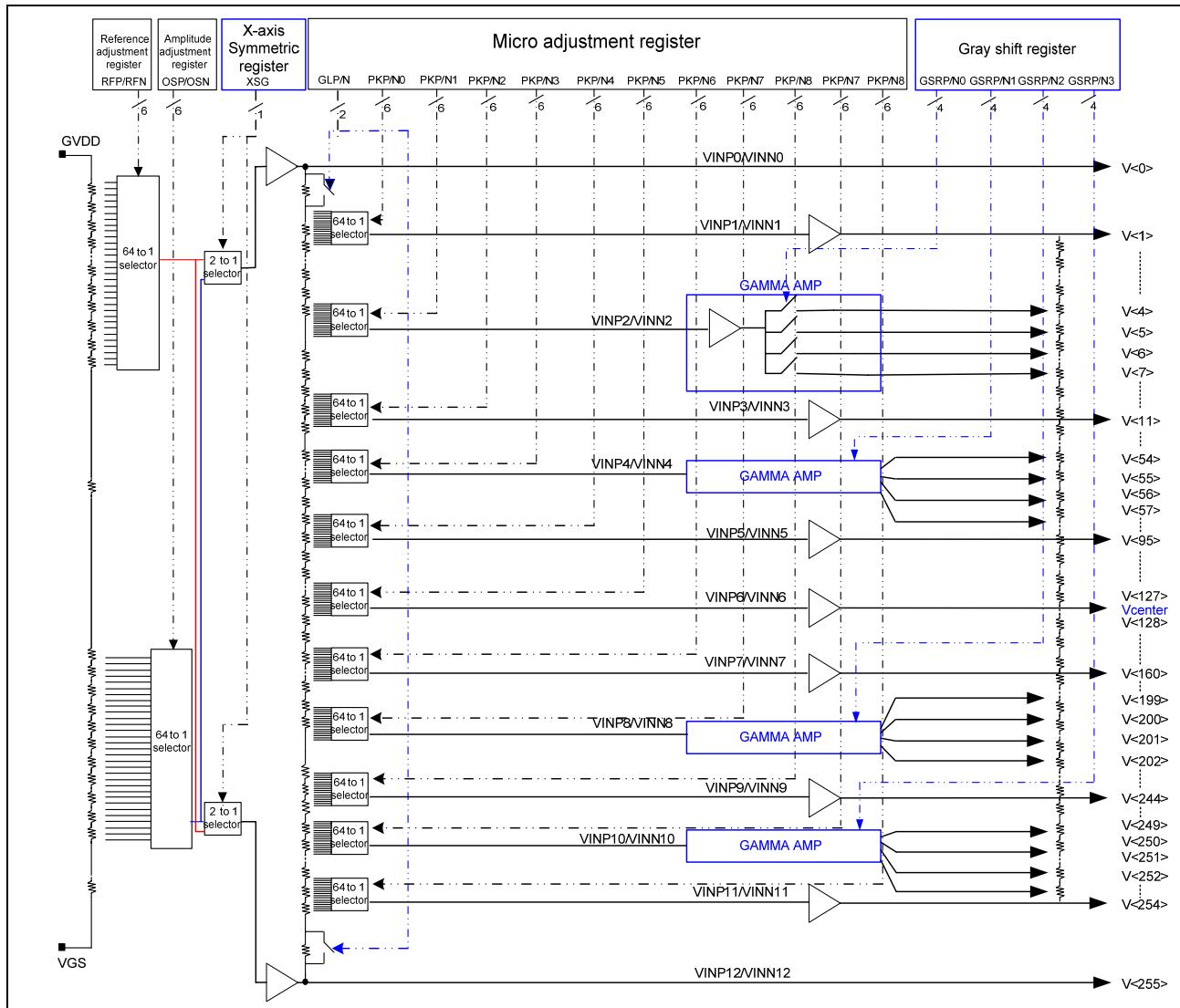


Figure 89. Structure of gray scale amplifier

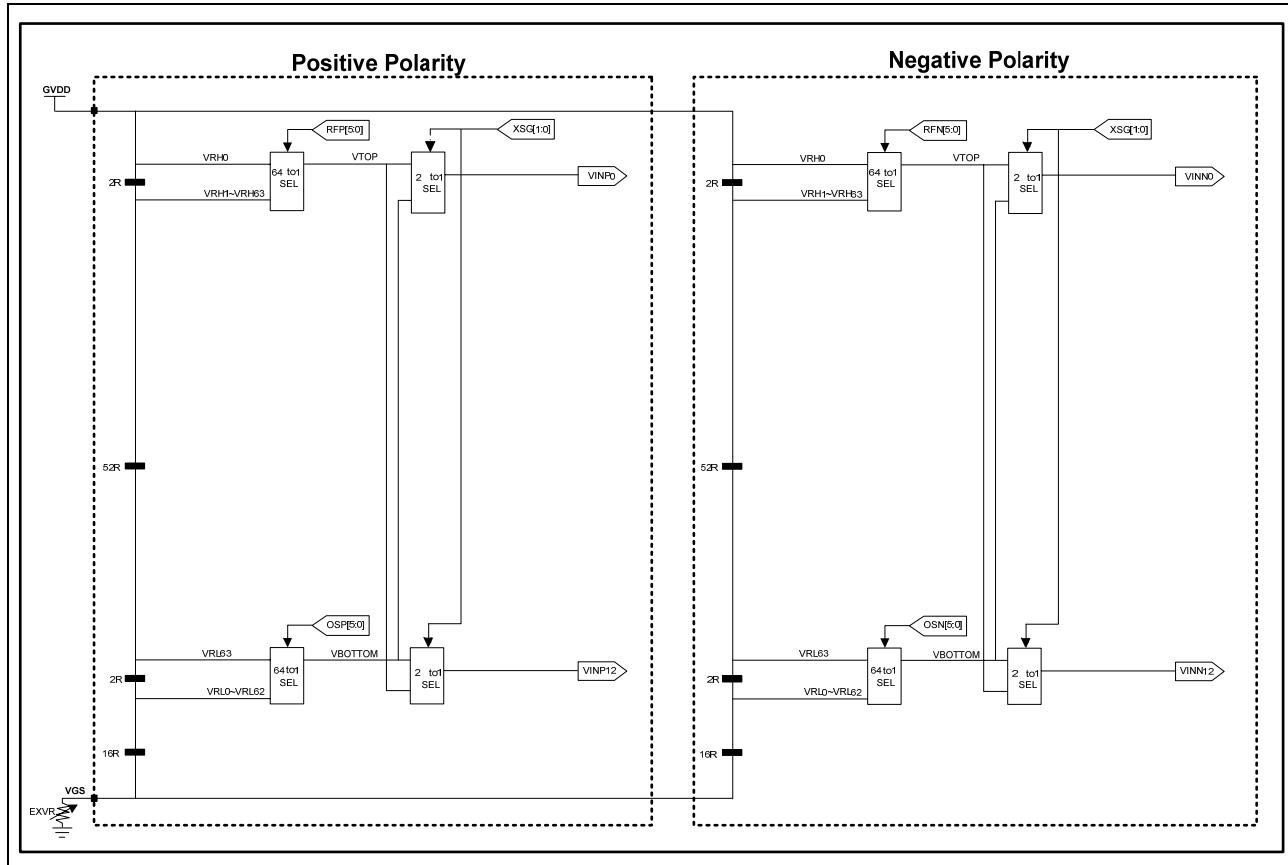


Figure 90. Structure of resistor ladder network 1.

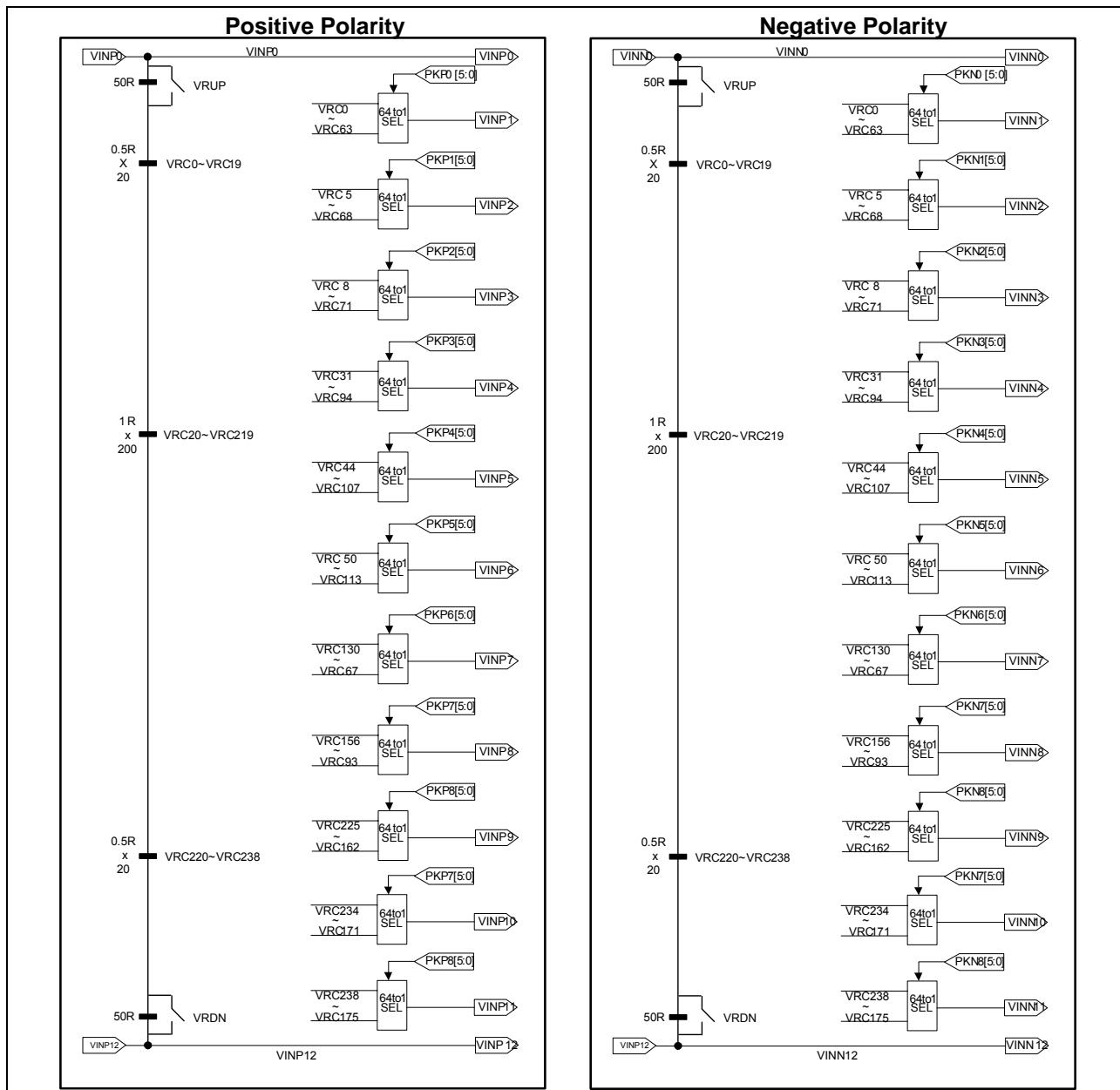
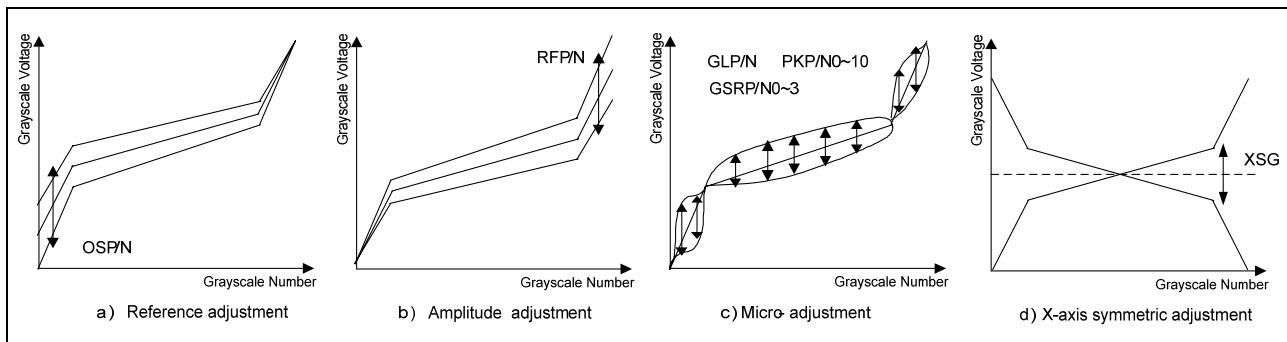


Figure 91. Structure of resistor ladder network 2.

#### 4.2.5. Gamma Adjustment Register

This block has registers to set up the grayscale voltage according to the gamma specification of the LCD panel. These registers can independently set up the positive/negative polarities. There are 4 types of register groups to adjust the amplitude on the grayscale characteristics of the grayscale voltage, and R/G/B gamma adjustment registers are separated. The following figures indicate the operation of each adjustment registers.



**Figure 92. The operation of adjusting register**

##### 4.2.5.1. Reference adjustment register

The Reference adjustment register is used to adjust the reference of the grayscale voltage. To accomplish the adjustment, it controls the VINP12/VINN12 voltage level by 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder between GVDD and VGS.

##### 4.2.5.2. Amplitude adjustment register

The Amplitude adjustment register is to adjust the amplitude of the grayscale voltage. To accomplish the adjustment, it controls the VINP0/VINN0 voltage level by 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder between GVDD and VGS.

##### 4.2.5.3. Micro-adjustment register

The Micro adjustment register is employed to make subtle adjustment to the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 64 to 1 selector towards the 64-leveled reference voltage generated from the resistor ladder. Also, there is an independent register on the positive/negative polarities as well as other adjustment registers.

##### 4.2.5.4. Gray shift register

The Gray shift register is employed to make subtle adjustment to the grayscale voltage level. To accomplish the adjustment, it controls 4 point reference voltage level by the switch. Also, there is an independent register on the positive/negative polarities as well as other adjustment registers

#### 4.2.5.5. X-axis symmetric adjustment register

The X-axis symmetric adjustment register is to adjust X-axis symmetric of the grayscale voltage. This register can be detailedly explained with NGF register selection. 1st case; when XSG=0 and NGF=0,  $Vp<N>+Vn<N>=Vp<0>+Vn<0>$  and gamma symmetric axis is  $(Vp<0>+Vn<0>)/2$ . 2nd case; when XSG=0 and NGF=1, negative gamma voltage can be changed using negative gamma register value and symmetric axis will be changed according to negative gamma voltage. 3rd case; when XSG=1 and NGF=0,  $Vp<N>=Vn<|255-N|>$ . 4th case; when XSG=1 and NGF=1,  $Vp<N>+Vn<N>=Vp<0>+Vn<0>$  but can have similar value in some degree using both positive and negative gamma registers.

**Table 52. Description of gamma adjustment register**

Register	Positive polarity	Negative polarity	Set-up contents
Reference adjustment	OSP[5:0]	OSN[5:0]	The voltage of VBOTTOM is selected by the 64 to 1 selector
Amplitude adjustment	RFP[5:0]	RFN[5:0]	The voltage of VTOP is selected by the 64 to 1 selector
X-axis symmetric adjustment	XSG		The voltage of VINP12/VINN12 is selected by the 2 to 1 selector
			The voltage of VINP0/VINN0 is selected by the 2 to 1 selector
Micro adjustment	GLP[1:0]	GLN[1:0]	The voltage of grayscale number from 1 to 254 is adjusted by the variable resistor
	PKP0[5:0]	PKN0[5:0]	The voltage of grayscale number 1 is selected by the 64 to 1 selector
	PKP1[5:0]	PKN1[5:0]	The voltage of grayscale number 5 is selected by the 64 to 1 selector
	PKP2[5:0]	PKN2[5:0]	The voltage of grayscale number 11 is selected by the 64 to 1 selector
	PKP3[5:0]	PKN3[5:0]	The voltage of grayscale number 55 is selected by the 64 to 1 selector
	PKP4[5:0]	PKN4[5:0]	The voltage of grayscale number 95 is selected by the 64 to 1 selector
	PKP5[5:0]	PKN5[5:0]	The voltage of grayscale number VC (middle voltage between $v<127>$ and $V<128>$ ) is selected by the 64 to 1 selector
	PKP6[5:0]	PKN6[5:0]	The voltage of grayscale number 160 is selected by the 64 to 1 selector
	PKP7[5:0]	PKN7[5:0]	The voltage of grayscale number 200 is selected by the 64 to 1 selector
	PKP8[5:0]	PKN8[5:0]	The voltage of grayscale number 244 is selected by the 64 to 1 selector
	PKP9[5:0]	PKN9[5:0]	The voltage of grayscale number 250 is selected by the 64 to 1 selector

Register	Positive polarity	Negative polarity	Set-up contents
	PKP10[5:0]	PKN10[5:0]	The voltage of grayscale number 254 is selected by the 64 to 1 selector
	GSRP0[3:0]	GSRN0[3:0]	The register is used to select one among the grayscale numbers 4 to 7
	GSRP1[3:0]	GSRN1[3:0]	The register is used to select one among the grayscale numbers 54 to 57
	GSRP2[3:0]	GSRN2[3:0]	The register is used to select one among the grayscale numbers 199 to 202
	GSRP3[3:0]	GSRN3[3:0]	The register is used to select one among the grayscale numbers 249 to 252

#### 4.2.6. Resistor Ladder Network / Selector

This block outputs the reference voltage of the grayscale voltage. There are three ladder resistors including the 64 to 1 selector selecting voltage generated by the ladder resistance voltage. Also, there are pins that connect to the external volume resistor. In addition, it allows compensating the dispersion of length between one panel and another.

##### 4.2.6.1. Resistor ladder network 1 / selector

There are 2 adjustments that are for the reference / amplitude adjustment (RFP(N)/ OSP(N)) and micro adjustment (PKP(N)). The voltage level is set by the reference / amplitude adjustment registers and micro adjustments as below.

**Table 53. Amplitude adjustment**

Register value RFP(N) [5:0]	Selected voltage VTOP	Formula of VTOP
000000	VRH0	(320R/320R) * (GVDD-VGS) + VGS
000001	VRH1	(318R/320R) * (GVDD-VGS) + VGS
000010	VRH2	(316R/320R) * (GVDD-VGS) + VGS
000011	VRH3	(314R/320R) * (GVDD-VGS) + VGS
000100	VRH4	(312R/320R) * (GVDD-VGS) + VGS
000101	VRH5	(310R/320R) * (GVDD-VGS) + VGS
000110	VRH6	(308R/320R) * (GVDD-VGS) + VGS
000111	VRH7	(306R/320R) * (GVDD-VGS) + VGS
001000	VRH8	(304R/320R) * (GVDD-VGS) + VGS
001001	VRH9	(302R/320R) * (GVDD-VGS) + VGS
001010	VRH10	(300R/320R) * (GVDD-VGS) + VGS
001011	VRH11	(298R/320R) * (GVDD-VGS) + VGS
001100	VRH12	(296R/320R) * (GVDD-VGS) + VGS
001101	VRH13	(294R/320R) * (GVDD-VGS) + VGS
001110	VRH14	(292R/320R) * (GVDD-VGS) + VGS
001111	VRH15	(290R/320R) * (GVDD-VGS) + VGS
010000	VRH16	(288R/320R) * (GVDD-VGS) + VGS
010001	VRH17	(286R/320R) * (GVDD-VGS) + VGS
010010	VRH18	(284R/320R) * (GVDD-VGS) + VGS
010011	VRH19	(282R/320R) * (GVDD-VGS) + VGS
010100	VRH20	(280R/320R) * (GVDD-VGS) + VGS
010101	VRH21	(278R/320R) * (GVDD-VGS) + VGS
010110	VRH22	(276R/320R) * (GVDD-VGS) + VGS
010111	VRH23	(274R/320R) * (GVDD-VGS) + VGS
011000	VRH24	(272R/320R) * (GVDD-VGS) + VGS
011001	VRH25	(270R/320R) * (GVDD-VGS) + VGS
011010	VRH26	(268R/320R) * (GVDD-VGS) + VGS
011011	VRH27	(266R/320R) * (GVDD-VGS) + VGS
011100	VRH28	(264R/320R) * (GVDD-VGS) + VGS
011101	VRH29	(262R/320R) * (GVDD-VGS) + VGS
011110	VRH30	(260R/320R) * (GVDD-VGS) + VGS
011111	VRH31	(258R/320R) * (GVDD-VGS) + VGS
100000	VRH32	(256R/320R) * (GVDD-VGS) + VGS
100001	VRH33	(254R/320R) * (GVDD-VGS) + VGS
100010	VRH34	(252R/320R) * (GVDD-VGS) + VGS
100011	VRH35	(250R/320R) * (GVDD-VGS) + VGS



**Table 54. Amplitude adjustment(continued)**

Register value RFP(N) [5:0]	Selected voltage VTOP	Formula of VTOP
100100	VRH36	(248R/320R) * (GVDD-VGS) + VGS
100101	VRH37	(246R/320R) * (GVDD-VGS) + VGS
100110	VRH38	(244R/320R) * (GVDD-VGS) + VGS
100111	VRH39	(242R/320R) * (GVDD-VGS) + VGS
101000	VRH40	(240R/320R) * (GVDD-VGS) + VGS
101001	VRH41	(238R/320R) * (GVDD-VGS) + VGS
101010	VRH42	(236R/320R) * (GVDD-VGS) + VGS
101011	VRH43	(234R/320R) * (GVDD-VGS) + VGS
101100	VRH44	(232R/320R) * (GVDD-VGS) + VGS
101101	VRH45	(230R/320R) * (GVDD-VGS) + VGS
101110	VRH46	(228R/320R) * (GVDD-VGS) + VGS
101111	VRH47	(226R/320R) * (GVDD-VGS) + VGS
110000	VRH48	(224R/320R) * (GVDD-VGS) + VGS
110001	VRH49	(222R/320R) * (GVDD-VGS) + VGS
110010	VRH50	(220R/320R) * (GVDD-VGS) + VGS
110011	VRH51	(218R/320R) * (GVDD-VGS) + VGS
110100	VRH52	(216R/320R) * (GVDD-VGS) + VGS
110101	VRH53	(214R/320R) * (GVDD-VGS) + VGS
110110	VRH54	(212R/320R) * (GVDD-VGS) + VGS
110111	VRH55	(210R/320R) * (GVDD-VGS) + VGS
111000	VRH56	(208R/320R) * (GVDD-VGS) + VGS
111001	VRH57	(206R/320R) * (GVDD-VGS) + VGS
111010	VRH58	(204R/320R) * (GVDD-VGS) + VGS
111011	VRH59	(202R/320R) * (GVDD-VGS) + VGS
111100	VRH60	(200R/320R) * (GVDD-VGS) + VGS
111101	VRH61	(198R/320R) * (GVDD-VGS) + VGS
111110	VRH62	(196R/320R) * (GVDD-VGS) + VGS
111111	VRH63	(194R/320R) * (GVDD-VGS) + VGS

**Table 55. Reference adjustment**

<b>Register value OSP(N) [5:0]</b>	<b>Selected voltage VBOTTOM</b>	<b>Formula of VBOTTOM</b>
000000	VRL0	(16R/320R) * (GVDD-VGS) + VGS
000001	VRL1	(18R/320R) * (GVDD-VGS) + VGS
000010	VRL2	(20R/320R) * (GVDD-VGS) + VGS
000011	VRL3	(22R/320R) * (GVDD-VGS) + VGS
000100	VRL4	(24R/320R) * (GVDD-VGS) + VGS
000101	VRL5	(26R/320R) * (GVDD-VGS) + VGS
000110	VRL6	(28R/320R) * (GVDD-VGS) + VGS
000111	VRL7	(30R/320R) * (GVDD-VGS) + VGS
001000	VRL8	(32R/320R) * (GVDD-VGS) + VGS
001001	VRL9	(34R/320R) * (GVDD-VGS) + VGS
001010	VRL10	(36R/320R) * (GVDD-VGS) + VGS
001011	VRL11	(38R/320R) * (GVDD-VGS) + VGS
001100	VRL12	(40R/320R) * (GVDD-VGS) + VGS
001101	VRL13	(42R/320R) * (GVDD-VGS) + VGS
001110	VRL14	(44R/320R) * (GVDD-VGS) + VGS
001111	VRL15	(46R/320R) * (GVDD-VGS) + VGS
010000	VRL16	(48R/320R) * (GVDD-VGS) + VGS
010001	VRL17	(50R/320R) * (GVDD-VGS) + VGS
010010	VRL18	(52R/320R) * (GVDD-VGS) + VGS
010011	VRL19	(54R/320R) * (GVDD-VGS) + VGS
010100	VRL20	(56R/320R) * (GVDD-VGS) + VGS
010101	VRL21	(58R/320R) * (GVDD-VGS) + VGS
010110	VRL22	(60R/320R) * (GVDD-VGS) + VGS
010111	VRL23	(62R/320R) * (GVDD-VGS) + VGS
011000	VRL24	(64R/320R) * (GVDD-VGS) + VGS
011001	VRL25	(66R/320R) * (GVDD-VGS) + VGS
011010	VRL26	(68R/320R) * (GVDD-VGS) + VGS
011011	VRL27	(70R/320R) * (GVDD-VGS) + VGS
011100	VRL28	(72R/320R) * (GVDD-VGS) + VGS
011101	VRL29	(74R/320R) * (GVDD-VGS) + VGS
011110	VRL30	(76R/320R) * (GVDD-VGS) + VGS
011111	VRL31	(78R/320R) * (GVDD-VGS) + VGS
100000	VRL32	(80R/320R) * (GVDD-VGS) + VGS
100001	VRL33	(82R/320R) * (GVDD-VGS) + VGS
100010	VRL34	(84R/320R) * (GVDD-VGS) + VGS
100011	VRL35	(86R/320R) * (GVDD-VGS) + VGS



**Table 56. Reference adjustment (continued)**

Register value OSP(N) [5:0]	Selected voltage VBOTTOM	Formula of VBOTTOM
100100	VRL36	(88R/320R) * (GVDD-VGS) + VGS
100101	VRL37	(90R/320R) * (GVDD-VGS) + VGS
100110	VRL38	(92R/320R) * (GVDD-VGS) + VGS
100111	VRL39	(94R/320R) * (GVDD-VGS) + VGS
101000	VRL40	(96R/320R) * (GVDD-VGS) + VGS
101001	VRL41	(98R/320R) * (GVDD-VGS) + VGS
101010	VRL42	(100R/320R) * (GVDD-VGS) + VGS
101011	VRL43	(102R/320R) * (GVDD-VGS) + VGS
101100	VRL44	(104R/320R) * (GVDD-VGS) + VGS
101101	VRL45	(106R/320R) * (GVDD-VGS) + VGS
101110	VRL46	(108R/320R) * (GVDD-VGS) + VGS
101111	VRL47	(110R/320R) * (GVDD-VGS) + VGS
110000	VRL48	(112R/320R) * (GVDD-VGS) + VGS
110001	VRL49	(114R/320R) * (GVDD-VGS) + VGS
110010	VRL50	(116R/320R) * (GVDD-VGS) + VGS
110011	VRL51	(118R/320R) * (GVDD-VGS) + VGS
110100	VRL52	(120R/320R) * (GVDD-VGS) + VGS
110101	VRL53	(122R/320R) * (GVDD-VGS) + VGS
110110	VRL54	(124R/320R) * (GVDD-VGS) + VGS
110111	VRL55	(126R/320R) * (GVDD-VGS) + VGS
111000	VRL56	(128R/320R) * (GVDD-VGS) + VGS
111001	VRL57	(130R/320R) * (GVDD-VGS) + VGS
111010	VRL58	(132R/320R) * (GVDD-VGS) + VGS
111011	VRL59	(134R/320R) * (GVDD-VGS) + VGS
111100	VRL60	(136R/320R) * (GVDD-VGS) + VGS
111101	VRL61	(138R/320R) * (GVDD-VGS) + VGS
111110	VRL62	(140R/320R) * (GVDD-VGS) + VGS
111111	VRL63	(142R/320R) * (GVDD-VGS) + VGS

#### 4.2.6.2. Resistor ladder network 2 / selector

In the 64-to-1 selector, the voltage level must be selected by the given ladder resistance and the micro-adjustment register and output the nine types of the reference voltage, VIN1 to VIN11.

Following figure explains the relationship between the micro-adjustment register and the selected voltage

**Table 57. Relationship between micro-adjustment register and selected voltage**

Register value	Selected voltage										
	PKP(N) [5:0]	VINP (N)1	VINP (N)2	VINP (N)3	VINP (N)4	VINP (N)5	VINP (N)6	VINP (N)7	VINP (N)8	VINP (N)9	VINP (N)10
000000	VRC0	VRC5	VRC8	VRC31	VRC44	VRC50	VRC130	VRC156	VRC225	VRC234	VRC238
000001	VRC1	VRC6	VRC9	VRC32	VRC45	VRC51	VRC129	VRC155	VRC224	VRC233	VRC237
000010	VRC2	VRC7	VRC10	VRC33	VRC46	VRC52	VRC128	VRC154	VRC223	VRC232	VRC236
000011	VRC3	VRC8	VRC11	VRC34	VRC47	VRC53	VRC127	VRC153	VRC222	VRC231	VRC235
000100	VRC4	VRC9	VRC12	VRC35	VRC48	VRC54	VRC126	VRC152	VRC221	VRC230	VRC234
000101	VRC5	VRC10	VRC13	VRC36	VRC49	VRC55	VRC125	VRC151	VRC220	VRC229	VRC233
000110	VRC6	VRC11	VRC14	VRC37	VRC50	VRC56	VRC124	VRC150	VRC219	VRC228	VRC232
000111	VRC7	VRC12	VRC15	VRC38	VRC51	VRC57	VRC123	VRC149	VRC218	VRC227	VRC231
001000	VRC8	VRC13	VRC16	VRC39	VRC52	VRC58	VRC122	VRC148	VRC217	VRC226	VRC230
001001	VRC9	VRC14	VRC17	VRC40	VRC53	VRC59	VRC121	VRC147	VRC216	VRC225	VRC229
001010	VRC10	VRC15	VRC18	VRC41	VRC54	VRC60	VRC120	VRC146	VRC215	VRC224	VRC228
001011	VRC11	VRC16	VRC19	VRC42	VRC55	VRC61	VRC119	VRC145	VRC214	VRC223	VRC227
001100	VRC12	VRC17	VRC20	VRC43	VRC56	VRC62	VRC118	VRC144	VRC213	VRC222	VRC226
001101	VRC13	VRC18	VRC21	VRC44	VRC57	VRC63	VRC117	VRC143	VRC212	VRC221	VRC225
001110	VRC14	VRC19	VRC22	VRC45	VRC58	VRC64	VRC116	VRC142	VRC211	VRC220	VRC224
001111	VRC15	VRC20	VRC23	VRC46	VRC59	VRC65	VRC115	VRC141	VRC210	VRC219	VRC223
010000	VRC16	VRC21	VRC24	VRC47	VRC60	VRC66	VRC114	VRC140	VRC209	VRC218	VRC222
010001	VRC17	VRC22	VRC25	VRC48	VRC61	VRC67	VRC113	VRC139	VRC208	VRC217	VRC221
010010	VRC18	VRC23	VRC26	VRC49	VRC62	VRC68	VRC112	VRC138	VRC207	VRC216	VRC220
010011	VRC19	VRC24	VRC27	VRC50	VRC63	VRC69	VRC111	VRC137	VRC206	VRC215	VRC219
010100	VRC20	VRC25	VRC28	VRC51	VRC64	VRC70	VRC110	VRC136	VRC205	VRC214	VRC218
010101	VRC21	VRC26	VRC29	VRC52	VRC65	VRC71	VRC109	VRC135	VRC204	VRC213	VRC217
010110	VRC22	VRC27	VRC30	VRC53	VRC66	VRC72	VRC108	VRC134	VRC203	VRC212	VRC216
010111	VRC23	VRC28	VRC31	VRC54	VRC67	VRC73	VRC107	VRC133	VRC202	VRC211	VRC215
011000	VRC24	VRC29	VRC32	VRC55	VRC68	VRC74	VRC106	VRC132	VRC201	VRC210	VRC214
011001	VRC25	VRC30	VRC33	VRC56	VRC69	VRC75	VRC105	VRC131	VRC200	VRC209	VRC213
011010	VRC26	VRC31	VRC34	VRC57	VRC70	VRC76	VRC104	VRC130	VRC199	VRC208	VRC212



Table 58. Relationship between micro-adjustment register and selected voltage(continued)

Register value	Selected voltage										
PKP(N) [5:0]	VINP (N)1	VINP (N)2	VINP (N)3	VINP (N)4	VINP (N)5	VINP (N)6	VINP (N)7	VINP (N)8	VINP (N)9	VINP (N)10	VINP (N)11
011011	VRC27	VRC32	VRC35	VRC58	VRC71	VRC77	VRC103	VRC129	VRC198	VRC207	VRC211
011100	VRC28	VRC33	VRC36	VRC59	VRC72	VRC78	VRC102	VRC128	VRC197	VRC206	VRC210
011101	VRC29	VRC34	VRC37	VRC60	VRC73	VRC79	VRC101	VRC127	VRC196	VRC205	VRC209
011110	VRC30	VRC35	VRC38	VRC61	VRC74	VRC80	VRC100	VRC126	VRC195	VRC204	VRC208
011111	VRC31	VRC36	VRC39	VRC62	VRC75	VRC81	VRC99	VRC125	VRC194	VRC203	VRC207
100000	VRC32	VRC37	VRC40	VRC63	VRC76	VRC82	VRC98	VRC124	VRC193	VRC202	VRC206
100001	VRC33	VRC38	VRC41	VRC64	VRC77	VRC83	VRC97	VRC123	VRC192	VRC201	VRC205
100010	VRC34	VRC39	VRC42	VRC65	VRC78	VRC84	VRC96	VRC122	VRC191	VRC200	VRC204
100011	VRC35	VRC40	VRC43	VRC66	VRC79	VRC85	VRC95	VRC121	VRC190	VRC199	VRC203
100100	VRC36	VRC41	VRC44	VRC67	VRC80	VRC86	VRC94	VRC120	VRC189	VRC198	VRC202
100101	VRC37	VRC42	VRC45	VRC68	VRC81	VRC87	VRC93	VRC119	VRC188	VRC197	VRC201
100110	VRC38	VRC43	VRC46	VRC69	VRC82	VRC88	VRC92	VRC118	VRC187	VRC196	VRC200
100111	VRC39	VRC44	VRC47	VRC70	VRC83	VRC89	VRC91	VRC117	VRC186	VRC195	VRC199
101000	VRC40	VRC45	VRC48	VRC71	VRC84	VRC90	VRC90	VRC116	VRC185	VRC194	VRC198
101001	VRC41	VRC46	VRC49	VRC72	VRC85	VRC91	VRC89	VRC115	VRC184	VRC193	VRC197
101010	VRC42	VRC47	VRC50	VRC73	VRC86	VRC92	VRC88	VRC114	VRC183	VRC192	VRC196
101011	VRC43	VRC48	VRC51	VRC74	VRC87	VRC93	VRC87	VRC113	VRC182	VRC191	VRC195
101100	VRC44	VRC49	VRC52	VRC75	VRC88	VRC94	VRC86	VRC112	VRC181	VRC190	VRC194
101101	VRC45	VRC50	VRC53	VRC76	VRC89	VRC95	VRC85	VRC111	VRC180	VRC189	VRC193
101110	VRC46	VRC51	VRC54	VRC77	VRC90	VRC96	VRC84	VRC110	VRC179	VRC188	VRC192
101111	VRC47	VRC52	VRC55	VRC78	VRC91	VRC97	VRC83	VRC109	VRC178	VRC187	VRC191
110000	VRC48	VRC53	VRC56	VRC79	VRC92	VRC98	VRC82	VRC108	VRC177	VRC186	VRC190
110001	VRC49	VRC54	VRC57	VRC80	VRC93	VRC99	VRC81	VRC107	VRC176	VRC185	VRC189
110010	VRC50	VRC55	VRC58	VRC81	VRC94	VRC100	VRC80	VRC106	VRC175	VRC184	VRC188
110011	VRC51	VRC56	VRC59	VRC82	VRC95	VRC101	VRC79	VRC105	VRC174	VRC183	VRC187
110100	VRC52	VRC57	VRC60	VRC83	VRC96	VRC102	VRC78	VRC104	VRC173	VRC182	VRC186
110101	VRC53	VRC58	VRC61	VRC84	VRC97	VRC103	VRC77	VRC103	VRC172	VRC181	VRC185
110110	VRC54	VRC59	VRC62	VRC85	VRC98	VRC104	VRC76	VRC102	VRC171	VRC180	VRC184
110111	VRC55	VRC60	VRC63	VRC86	VRC99	VRC105	VRC75	VRC101	VRC170	VRC179	VRC183
111000	VRC56	VRC61	VRC64	VRC87	VRC100	VRC106	VRC74	VRC100	VRC169	VRC178	VRC182
111001	VRC57	VRC62	VRC65	VRC88	VRC101	VRC107	VRC73	VRC99	VRC168	VRC177	VRC181
111010	VRC58	VRC63	VRC66	VRC89	VRC102	VRC108	VRC72	VRC98	VRC167	VRC176	VRC180



**Table 59. Relationship between micro-adjustment register and selected voltage(continued)**

Register value	Selected voltage										
	PKP(N) [5:0]	VINP (N)1	VINP (N)2	VINP (N)3	VINP (N)4	VINP (N)5	VINP (N)6	VINP (N)7	VINP (N)8	VINP (N)9	VINP (N)10
111011	VRC59	VRC64	VRC67	VRC90	VRC103	VRC109	VRC71	VRC97	VRC166	VRC175	VRC179
111100	VRC60	VRC65	VRC68	VRC91	VRC104	VRC110	VRC70	VRC96	VRC165	VRC174	VRC178
111101	VRC61	VRC66	VRC69	VRC92	VRC105	VRC111	VRC69	VRC95	VRC164	VRC173	VRC177
111110	VRC62	VRC67	VRC70	VRC93	VRC106	VRC112	VRC68	VRC94	VRC163	VRC172	VRC176
111111	VRC63	VRC68	VRC71	VRC94	VRC107	VRC113	VRC67	VRC93	VRC162	VRC171	VRC175

The grayscale levels are determined by the following formulas listed in the following equations.

Negative gamma voltages are calculated with the same equation of positive gamma voltages, but the gray scale is symmetric, which means negative V<0> is equal to positive V<255>. Rt and Ra in the below equations are determined by GL[1:0] Registers as follows.

GLP/N[1:0]=00, Rt = 220R, Ra=0

GLP/N [1:0]=01, Rt = 270R, Ra=50R

GLP/N [1:0]=10, Rt = 270R, Ra=0

GLP/N [1:0]=11, Rt = 320R, Ra=50R

#### 4.2.7. Grayscale Levels

**Table 60. Formulas for calculating gamma adjusting voltage (positive polarity) 1**

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC0	$((219.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "000000"	VNP1
VRC1	$((219R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "000001"	
VRC2	$((218.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "000010"	
VRC3	$((218R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "000011"	
VRC4	$((217.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "000100"	
VRC5	$((217R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "000101"	
VRC6	$((216.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "000110"	
VRC7	$((216R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "000111"	
VRC8	$((215.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "001000"	
VRC9	$((215R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "001001"	
VRC10	$((214.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "001010"	
VRC11	$((214R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "001011"	
VRC12	$((213.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "001100"	
VRC13	$((213R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "001101"	
VRC14	$((212.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "001110"	
VRC15	$((212R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "001111"	
VRC16	$((211.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "010000"	
VRC17	$((211R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "010001"	
VRC18	$((210.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "010010"	
VRC19	$((210R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "010011"	
VRC20	$((209R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "010100"	
VRC21	$((208R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "010101"	
VRC22	$((207R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "010110"	
VRC23	$((206R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "010111"	
VRC24	$((205R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "011000"	
VRC25	$((204R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "011001"	
VRC26	$((203R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "011010"	
VRC27	$((202R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "011011"	
VRC28	$((201R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "011100"	
VRC29	$((200R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "011101"	
VRC30	$((199R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "011110"	
VRC31	$((198R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "011111"	
VRC32	$((197R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "100000"	
VRC33	$((196R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "100001"	
VRC34	$((195R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "100010"	
VRC35	$((194R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "100011"	

Table 61. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC36	$((193R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "100100"	VINP1
VRC37	$((192R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "100101"	
VRC38	$((191R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "100110"	
VRC39	$((190R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "100111"	
VRC40	$((189R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "101000"	
VRC41	$((188R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "101001"	
VRC42	$((187R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "101010"	
VRC43	$((186R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "101011"	
VRC44	$((185R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "101100"	
VRC45	$((184R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "101101"	
VRC46	$((183R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "101110"	
VRC47	$((182R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "101111"	
VRC48	$((181R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "110000"	
VRC49	$((180R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "110001"	
VRC50	$((179R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "110010"	
VRC51	$((178R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "110011"	
VRC52	$((177R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "110100"	
VRC53	$((176R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "110101"	
VRC54	$((175R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "110110"	
VRC55	$((174R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "110111"	
VRC56	$((173R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "111000"	
VRC57	$((172R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "111001"	
VRC58	$((171R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "111010"	
VRC59	$((170R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "111011"	
VRC60	$((169R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "111100"	VINP2
VRC61	$((168R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "111101"	
VRC62	$((167R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "111110"	
VRC63	$((166R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP0[5:0] = "111111"	
VRC5	$((217R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "000000"	
VRC6	$((216.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "000001"	
VRC7	$((216R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "000010"	
VRC8	$((215.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "000011"	
VRC9	$((215R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "000100"	
VRC10	$((214.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "000101"	
VRC11	$((214R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "000110"	
VRC12	$((213.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "000111"	



Table 62. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC13	$((213R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "001000"	VINP2
VRC14	$((212.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "001001"	
VRC15	$((212R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "001010"	
VRC16	$((211.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "001011"	
VRC17	$((211R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "001100"	
VRC18	$((210.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "001101"	
VRC19	$((210R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "001110"	
VRC20	$((209R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "001111"	
VRC21	$((208R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "010000"	
VRC22	$((207R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "010001"	
VRC23	$((206R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "010010"	
VRC24	$((205R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "010011"	
VRC25	$((204R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "010100"	
VRC26	$((203R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "010101"	
VRC27	$((202R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "010110"	
VRC28	$((201R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "010111"	
VRC29	$((200R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "011000"	
VRC30	$((199R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "011001"	
VRC31	$((198R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "011010"	
VRC32	$((197R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "011011"	
VRC33	$((196R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "011100"	
VRC34	$((195R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "011101"	
VRC35	$((194R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "011110"	
VRC36	$((193R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "011111"	
VRC37	$((192R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "100000"	
VRC38	$((191R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "100001"	
VRC39	$((190R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "100010"	
VRC40	$((189R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "100011"	
VRC41	$((188R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "100100"	
VRC42	$((187R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "100101"	
VRC43	$((186R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "100110"	
VRC44	$((185R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "100111"	
VRC45	$((184R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "101000"	
VRC46	$((183R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "101001"	
VRC47	$((182R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "101010"	
VRC48	$((181R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "101011"	



Table 63. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC49	$((180R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "101100"	VINP2
VRC50	$((179R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "101101"	
VRC51	$((178R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "101110"	
VRC52	$((177R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "101111"	
VRC53	$((176R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "110000"	
VRC54	$((175R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "110001"	
VRC55	$((174R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "110010"	
VRC56	$((173R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "110011"	
VRC57	$((172R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "110100"	
VRC58	$((171R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "110101"	
VRC59	$((170R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "110110"	
VRC60	$((169R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "110111"	
VRC61	$((168R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "111000"	
VRC62	$((167R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "111001"	
VRC63	$((166R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "111010"	
VRC64	$((165R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "111011"	
VRC65	$((164R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "111100"	
VRC66	$((163R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "111101"	
VRC67	$((162R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "111110"	
VRC68	$((161R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP1[5:0] = "111111"	
VRC8	$((215.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "000000"	VINP3
VRC9	$((215R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "000001"	
VRC10	$((214.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "000010"	
VRC11	$((214R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "000011"	
VRC12	$((213.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "000100"	
VRC13	$((213R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "000101"	
VRC14	$((212.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "000110"	
VRC15	$((212R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "000111"	
VRC16	$((211.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "001000"	
VRC17	$((211R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "001001"	
VRC18	$((210.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "001010"	
VRC19	$((210R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "001011"	
VRC20	$((209R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "001100"	
VRC21	$((208R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "001101"	
VRC22	$((207R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "001110"	
VRC23	$((206R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "001111"	



Table 64. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC24	$((205R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "010000"	VINP3
VRC25	$((204R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "010001"	
VRC26	$((203R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "010010"	
VRC27	$((202R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "010011"	
VRC28	$((201R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "010100"	
VRC29	$((200R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "010101"	
VRC30	$((199R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "010110"	
VRC31	$((198R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "010111"	
VRC32	$((197R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "011000"	
VRC33	$((196R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "011001"	
VRC34	$((195R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "011010"	
VRC35	$((194R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "011011"	
VRC36	$((193R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "011100"	
VRC37	$((192R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "011101"	
VRC38	$((191R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "011110"	
VRC39	$((190R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "011111"	
VRC40	$((189R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "100000"	
VRC41	$((188R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "100001"	
VRC42	$((187R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "100010"	
VRC43	$((186R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "100011"	
VRC44	$((185R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "100100"	
VRC45	$((184R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "100101"	
VRC46	$((183R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "100110"	
VRC47	$((182R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "100111"	
VRC48	$((181R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "101000"	
VRC49	$((180R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "101001"	
VRC50	$((179R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "101010"	
VRC51	$((178R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "101011"	
VRC52	$((177R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "101100"	
VRC53	$((176R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "101101"	
VRC54	$((175R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "101110"	
VRC55	$((174R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "101111"	
VRC56	$((173R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "110000"	
VRC57	$((172R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "110001"	
VRC58	$((171R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "110010"	
VRC59	$((170R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "110011"	



Table 65. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC60	$((169R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "110100"	VINP3
VRC61	$((168R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "110101"	
VRC62	$((167R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "110110"	
VRC63	$((166R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "110111"	
VRC64	$((165R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "111000"	
VRC65	$((164R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "111001"	
VRC66	$((163R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "111010"	
VRC67	$((162R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "111011"	
VRC68	$((161R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "111100"	
VRC69	$((160R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "111101"	
VRC70	$((159R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "111110"	
VRC71	$((158R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP2[5:0] = "111111"	
VRC31	$((198R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "000000"	VINP4
VRC32	$((197R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "000001"	
VRC33	$((196R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "000010"	
VRC34	$((195R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "000011"	
VRC35	$((194R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "000100"	
VRC36	$((193R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "000101"	
VRC37	$((192R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "000110"	
VRC38	$((191R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "000111"	
VRC39	$((190R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "001000"	
VRC40	$((189R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "001001"	
VRC41	$((188R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "001010"	
VRC42	$((187R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "001011"	
VRC43	$((186R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "001100"	
VRC44	$((185R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "001101"	
VRC45	$((184R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "001110"	
VRC46	$((183R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "001111"	
VRC47	$((182R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "010000"	
VRC48	$((181R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "010001"	
VRC49	$((180R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "010010"	
VRC50	$((179R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "010011"	
VRC51	$((178R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "010100"	
VRC52	$((177R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "010101"	
VRC53	$((176R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "010110"	
VRC54	$((175R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "010111"	



Table 66. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC55	$((174R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "011000"	
VRC56	$((173R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "011001"	
VRC57	$((172R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "011010"	
VRC58	$((171R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "011011"	
VRC59	$((170R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "011100"	
VRC60	$((169R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "011101"	
VRC61	$((168R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "011110"	
VRC62	$((167R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "011111"	
VRC63	$((166R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "100000"	
VRC64	$((165R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "100001"	
VRC65	$((164R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "100010"	
VRC66	$((163R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "100011"	
VRC67	$((162R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "100100"	
VRC68	$((161R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "100101"	
VRC69	$((160R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "100110"	
VRC70	$((159R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "100111"	
VRC71	$((158R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "101000"	
VRC72	$((157R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "101001"	
VRC73	$((156R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "101010"	
VRC74	$((155R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "101011"	
VRC75	$((154R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "101100"	
VRC76	$((153R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "101101"	
VRC77	$((152R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "101110"	
VRC78	$((151R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "101111"	
VRC79	$((150R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "110000"	
VRC80	$((149R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "110001"	
VRC81	$((148R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "110010"	
VRC82	$((147R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "110011"	
VRC83	$((146R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "110100"	
VRC84	$((145R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "110101"	
VRC85	$((144R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "110110"	
VRC86	$((143R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "110111"	
VRC87	$((142R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "111000"	
VRC88	$((141R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "111001"	
VRC89	$((140R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "111010"	
VRC90	$((139R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "111011"	

VINP4



Table 67. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC91	$((138R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "111100"	VINP4
VRC92	$((137R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "111101"	
VRC93	$((136R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "111110"	
VRC94	$((135R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP3[5:0] = "111111"	
VRC44	$((185R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "000000"	
VRC45	$((184R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "000001"	
VRC46	$((183R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "000010"	
VRC47	$((182R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "000011"	
VRC48	$((181R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "000100"	
VRC49	$((180R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "000101"	
VRC50	$((179R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "000110"	
VRC51	$((178R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "000111"	
VRC52	$((177R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "001000"	
VRC53	$((176R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "001001"	
VRC54	$((175R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "001010"	VINP5
VRC55	$((174R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "001011"	
VRC56	$((173R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "001100"	
VRC57	$((172R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "001101"	
VRC58	$((171R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "001110"	
VRC59	$((170R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "001111"	
VRC60	$((169R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "010000"	
VRC61	$((168R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "010001"	
VRC62	$((167R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "010010"	
VRC63	$((166R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "010011"	
VRC64	$((165R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "010100"	
VRC65	$((164R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "010101"	
VRC66	$((163R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "010110"	
VRC67	$((162R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "010111"	
VRC68	$((161R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "011000"	
VRC69	$((160R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "011001"	
VRC70	$((159R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "011010"	
VRC71	$((158R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "011011"	
VRC72	$((157R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "011100"	
VRC73	$((156R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "011101"	
VRC74	$((155R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "011110"	
VRC75	$((154R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "011111"	



Table 68. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC76	$((153R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "100000"	VINP5
VRC77	$((152R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "100001"	
VRC78	$((151R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "100010"	
VRC79	$((150R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "100011"	
VRC80	$((149R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "100100"	
VRC81	$((148R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "100101"	
VRC82	$((147R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "100110"	
VRC83	$((146R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "100111"	
VRC84	$((145R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "101000"	
VRC85	$((144R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "101001"	
VRC86	$((143R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "101010"	
VRC87	$((142R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "101011"	
VRC88	$((141R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "101100"	
VRC89	$((140R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "101101"	
VRC90	$((139R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "101110"	
VRC91	$((138R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "101111"	
VRC92	$((137R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "110000"	
VRC93	$((136R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "110001"	
VRC94	$((135R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "110010"	
VRC95	$((134R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "110011"	
VRC96	$((133R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "110100"	
VRC97	$((132R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "110101"	
VRC98	$((131R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "110110"	
VRC99	$((130R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "110111"	
VRC100	$((129R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "111000"	VINP6
VRC101	$((128R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "111001"	
VRC102	$((127R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "111010"	
VRC103	$((126R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "111011"	
VRC104	$((125R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "111100"	
VRC105	$((124R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "111101"	
VRC106	$((123R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "111110"	
VRC107	$((122R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP4[5:0] = "111111"	
VRC50	$((179R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "000000"	VINP6
VRC51	$((178R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "000001"	
VRC52	$((177R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "000010"	
VRC53	$((176R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "000011"	



Table 69. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC54	$((175R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "000100"	VINP6
VRC55	$((174R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "000101"	
VRC56	$((173R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "000110"	
VRC57	$((172R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "000111"	
VRC58	$((171R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "001000"	
VRC59	$((170R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "001001"	
VRC60	$((169R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "001010"	
VRC61	$((168R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "001011"	
VRC62	$((167R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "001100"	
VRC63	$((166R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "001101"	
VRC64	$((165R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "001110"	
VRC65	$((164R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "001111"	
VRC66	$((163R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "010000"	
VRC67	$((162R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "010001"	
VRC68	$((161R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "010010"	
VRC69	$((160R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "010011"	
VRC70	$((159R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "010100"	
VRC71	$((158R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "010101"	
VRC72	$((157R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "010110"	
VRC73	$((156R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "010111"	
VRC74	$((155R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "011000"	
VRC75	$((154R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "011001"	
VRC76	$((153R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "011010"	
VRC77	$((152R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "011011"	
VRC78	$((151R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "011100"	
VRC79	$((150R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "011101"	
VRC80	$((149R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "011110"	
VRC81	$((148R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "011111"	
VRC82	$((147R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "100000"	
VRC83	$((146R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "100001"	
VRC84	$((145R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "100010"	
VRC85	$((144R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "100011"	
VRC86	$((143R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "100100"	
VRC87	$((142R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "100101"	
VRC88	$((141R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "100110"	
VRC89	$((140R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "100111"	



Table 70. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC90	$((139R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "101000"	VINP6
VRC91	$((138R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "101001"	
VRC92	$((137R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "101010"	
VRC93	$((136R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "101011"	
VRC94	$((135R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "101100"	
VRC95	$((134R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "101101"	
VRC96	$((133R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "101110"	
VRC97	$((132R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "101111"	
VRC98	$((131R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "110000"	
VRC99	$((130R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "110001"	
VRC100	$((129R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "110010"	
VRC101	$((128R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "110011"	
VRC102	$((127R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "110100"	
VRC103	$((126R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "110101"	
VRC104	$((125R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "110110"	
VRC105	$((124R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "110111"	
VRC106	$((123R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "111000"	
VRC107	$((122R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "111001"	
VRC108	$((121R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "111010"	
VRC109	$((120R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "111011"	
VRC110	$((119R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "111100"	
VRC111	$((118R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "111101"	
VRC112	$((117R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "111110"	
VRC113	$((116R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP5[5:0] = "111111"	
VRC130	$((99R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "000000"	VINP7
VRC129	$((100R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "000001"	
VRC128	$((101R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "000010"	
VRC127	$((102R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "000011"	
VRC126	$((103R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "000100"	
VRC125	$((104R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "000101"	
VRC124	$((105R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "000110"	
VRC123	$((106R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "000111"	
VRC122	$((107R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "001000"	
VRC121	$((108R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "001001"	
VRC120	$((109R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "001010"	
VRC119	$((110R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "001011"	



Table 71. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC118	$((111R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "001100"	VINP7
VRC117	$((112R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "001101"	
VRC116	$((113R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "001110"	
VRC115	$((114R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "001111"	
VRC114	$((115R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "010000"	
VRC113	$((116R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "010001"	
VRC112	$((117R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "010010"	
VRC111	$((118R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "010011"	
VRC110	$((119R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "010100"	
VRC109	$((120R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "010101"	
VRC108	$((121R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "010110"	
VRC107	$((122R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "010111"	
VRC106	$((123R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "011000"	
VRC105	$((124R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "011001"	
VRC104	$((125R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "011010"	
VRC103	$((126R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "011011"	
VRC102	$((127R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "011100"	
VRC101	$((128R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "011101"	
VRC100	$((129R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "011110"	
VRC99	$((130R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "011111"	
VRC98	$((131R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "100000"	
VRC97	$((132R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "100001"	
VRC96	$((133R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "100010"	
VRC95	$((134R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "100011"	
VRC94	$((135R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "100100"	
VRC93	$((136R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "100101"	
VRC92	$((137R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "100110"	
VRC91	$((138R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "100111"	
VRC90	$((139R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "101000"	
VRC89	$((140R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "101001"	
VRC88	$((141R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "101010"	
VRC87	$((142R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "101011"	
VRC86	$((143R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "101100"	
VRC85	$((144R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "101101"	
VRC84	$((145R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "101110"	
VRC83	$((146R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "101111"	



Table 72. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC82	$((147R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "110000"	VINP7
VRC81	$((148R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "110001"	
VRC80	$((149R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "110010"	
VRC79	$((150R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "110011"	
VRC78	$((151R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "110100"	
VRC77	$((152R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "110101"	
VRC76	$((153R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "110110"	
VRC75	$((154R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "110111"	
VRC74	$((155R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "111000"	
VRC73	$((156R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "111001"	
VRC72	$((157R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "111010"	
VRC71	$((158R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "111011"	
VRC70	$((159R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "111100"	
VRC69	$((160R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "111101"	
VRC68	$((161R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "111110"	
VRC67	$((162R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP6[5:0] = "111111"	
VRC156	$((73R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "000000"	VINP8
VRC155	$((74R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "000001"	
VRC154	$((75R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "000010"	
VRC153	$((76R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "000011"	
VRC152	$((77R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "000100"	
VRC151	$((78R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "000101"	
VRC150	$((79R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "000110"	
VRC149	$((80R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "000111"	
VRC148	$((81R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "001000"	
VRC147	$((82R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "001001"	
VRC146	$((83R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "001010"	
VRC145	$((84R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "001011"	
VRC144	$((85R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "001100"	
VRC143	$((86R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "001101"	
VRC142	$((87R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "001110"	
VRC141	$((88R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "001111"	
VRC140	$((89R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "010000"	
VRC139	$((90R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "010001"	
VRC138	$((91R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "010010"	
VRC137	$((92R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "010011"	



Table 73. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC136	$((93R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "010100"	VINP8
VRC135	$((94R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "010101"	
VRC134	$((95R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "010110"	
VRC133	$((96R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "010111"	
VRC132	$((97R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "011000"	
VRC131	$((98R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "011001"	
VRC130	$((99R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "011010"	
VRC129	$((100R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "011011"	
VRC128	$((101R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "011100"	
VRC127	$((102R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "011101"	
VRC126	$((103R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "011110"	
VRC125	$((104R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "011111"	
VRC124	$((105R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "100000"	
VRC123	$((106R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "100001"	
VRC122	$((107R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "100010"	
VRC121	$((108R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "100011"	
VRC120	$((109R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "100100"	
VRC119	$((110R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "100101"	
VRC118	$((111R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "100110"	
VRC117	$((112R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "100111"	
VRC116	$((113R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "101000"	
VRC115	$((114R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "101001"	
VRC114	$((115R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "101010"	
VRC113	$((116R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "101011"	
VRC112	$((117R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "101100"	
VRC111	$((118R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "101101"	
VRC110	$((119R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "101110"	
VRC109	$((120R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "101111"	
VRC108	$((121R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "110000"	
VRC107	$((122R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "110001"	
VRC106	$((123R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "110010"	
VRC105	$((124R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "110011"	
VRC104	$((125R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "110100"	
VRC103	$((126R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "110101"	
VRC102	$((127R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "110110"	
VRC101	$((128R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "110111"	



Table 74. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC100	$((129R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "111000"	VINP8
VRC99	$((130R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "111001"	
VRC98	$((131R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "111010"	
VRC97	$((132R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "111011"	
VRC96	$((133R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "111100"	
VRC95	$((134R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "111101"	
VRC94	$((135R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "111110"	
VRC93	$((136R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP7[5:0] = "111111"	
VRC225	$((7R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "000000"	VINP9
VRC224	$((7.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "000001"	
VRC223	$((8R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "000010"	
VRC222	$((8.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "000011"	
VRC221	$((9R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "000100"	
VRC220	$((9.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "000101"	
VRC219	$((10R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "000110"	
VRC218	$((11R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "000111"	
VRC217	$((12R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "001000"	
VRC216	$((13R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "001001"	
VRC215	$((14R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "001010"	
VRC214	$((15R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "001011"	
VRC213	$((16R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "001100"	
VRC212	$((17R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "001101"	
VRC211	$((18R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "001110"	
VRC210	$((19R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "001111"	
VRC209	$((20R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "010000"	
VRC208	$((21R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "010001"	
VRC207	$((22R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "010010"	
VRC206	$((23R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "010011"	
VRC205	$((24R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "010100"	
VRC204	$((25R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "010101"	
VRC203	$((26R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "010110"	
VRC202	$((27R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "010111"	
VRC201	$((28R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "011000"	
VRC200	$((29R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "011001"	
VRC199	$((30R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "011010"	
VRC198	$((31R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "011011"	



Table 75. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC197	$((32R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "011100"	VINP9
VRC196	$((33R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "011101"	
VRC195	$((34R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "011110"	
VRC194	$((35R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "011111"	
VRC193	$((36R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "100000"	
VRC192	$((37R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "100001"	
VRC191	$((38R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "100010"	
VRC190	$((39R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "100011"	
VRC189	$((40R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "100100"	
VRC188	$((41R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "100101"	
VRC187	$((42R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "100110"	
VRC186	$((43R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "100111"	
VRC185	$((44R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "101000"	
VRC184	$((45R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "101001"	
VRC183	$((46R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "101010"	
VRC182	$((47R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "101011"	
VRC181	$((48R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "101100"	
VRC180	$((49R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "101101"	
VRC179	$((50R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "101110"	
VRC178	$((51R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "101111"	
VRC177	$((52R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "110000"	
VRC176	$((53R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "110001"	
VRC175	$((54R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "110010"	
VRC174	$((55R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "110011"	
VRC173	$((56R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "110100"	
VRC172	$((57R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "110101"	
VRC171	$((58R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "110110"	
VRC170	$((59R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "110111"	
VRC169	$((60R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "111000"	
VRC168	$((61R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "111001"	
VRC167	$((62R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "111010"	
VRC166	$((63R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "111011"	
VRC165	$((64R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "111100"	
VRC164	$((65R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "111101"	
VRC163	$((66R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "111110"	
VRC162	$((67R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP8[5:0] = "111111"	



Table 76. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC234	$((2.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "000000"	VNP10
VRC233	$((3R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "000001"	
VRC232	$((3.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "000010"	
VRC231	$((4R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "000011"	
VRC230	$((4.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "000100"	
VRC229	$((5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "000101"	
VRC228	$((5.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "000110"	
VRC227	$((6R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "000111"	
VRC226	$((6.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "001000"	
VRC225	$((7R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "001001"	
VRC224	$((7.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "001010"	
VRC223	$((8R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "001011"	
VRC222	$((8.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "001100"	
VRC221	$((9R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "001101"	
VRC220	$((9.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "001110"	
VRC219	$((10R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "001111"	
VRC218	$((11R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "010000"	
VRC217	$((12R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "010001"	
VRC216	$((13R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "010010"	
VRC215	$((14R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "010011"	
VRC214	$((15R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "010100"	
VRC213	$((16R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "010101"	
VRC212	$((17R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "010110"	
VRC211	$((18R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "010111"	
VRC210	$((19R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "011000"	
VRC209	$((20R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "011001"	
VRC208	$((21R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "011010"	
VRC207	$((22R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "011011"	
VRC206	$((23R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "011100"	
VRC205	$((24R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "011101"	
VRC204	$((25R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "011110"	
VRC203	$((26R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "011111"	
VRC202	$((27R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "100000"	
VRC201	$((28R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "100001"	
VRC200	$((29R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "100010"	
VRC199	$((30R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "100011"	



Table 77. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC198	$((31R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "100100"	VINP10
VRC197	$((32R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "100101"	
VRC196	$((33R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "100110"	
VRC195	$((34R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "100111"	
VRC194	$((35R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "101000"	
VRC193	$((36R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "101001"	
VRC192	$((37R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "101010"	
VRC191	$((38R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "101011"	
VRC190	$((39R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "101100"	
VRC189	$((40R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "101101"	
VRC188	$((41R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "101110"	
VRC187	$((42R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "101111"	
VRC186	$((43R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "110000"	
VRC185	$((44R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "110001"	
VRC184	$((45R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "110010"	
VRC183	$((46R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "110011"	
VRC182	$((47R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "110100"	
VRC181	$((48R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "110101"	
VRC180	$((49R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "110110"	
VRC179	$((50R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "110111"	
VRC178	$((51R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "111000"	
VRC177	$((52R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "111001"	
VRC176	$((53R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "111010"	
VRC175	$((54R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "111011"	
VRC174	$((55R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "111100"	
VRC173	$((56R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "111101"	
VRC172	$((57R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "111110"	
VRC171	$((58R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP9[5:0] = "111111"	
VRC238	$((0.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "000000"	VINP11
VRC237	$((1R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "000001"	
VRC236	$((1.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "000010"	
VRC235	$((2R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "000011"	
VRC234	$((2.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "000100"	
VRC233	$((3R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "000101"	
VRC232	$((3.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "000110"	
VRC231	$((4R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "000111"	



Table 78. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC230	$((4.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "001000"	
VRC229	$((5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "001001"	
VRC228	$((5.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "001010"	
VRC227	$((6R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "001011"	
VRC226	$((6.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "001100"	
VRC225	$((7R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "001101"	
VRC224	$((7.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "001110"	
VRC223	$((8R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "001111"	
VRC222	$((8.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "010000"	
VRC221	$((9R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "010001"	
VRC220	$((9.5R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "010010"	
VRC219	$((10R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "010011"	
VRC218	$((11R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "010100"	
VRC217	$((12R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "010101"	
VRC216	$((13R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "010110"	
VRC215	$((14R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "010111"	
VRC214	$((15R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "011000"	
VRC213	$((16R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "011001"	
VRC212	$((17R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "011010"	
VRC211	$((18R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "011011"	
VRC210	$((19R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "011100"	
VRC209	$((20R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "011101"	
VRC208	$((21R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "011110"	
VRC207	$((22R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "011111"	
VRC206	$((23R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "100000"	
VRC205	$((24R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "100001"	
VRC204	$((25R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "100010"	
VRC203	$((26R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "100011"	
VRC202	$((27R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "100100"	
VRC201	$((28R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "100101"	
VRC200	$((29R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "100110"	
VRC199	$((30R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "100111"	
VRC198	$((31R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "101000"	
VRC197	$((32R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "101001"	
VRC196	$((33R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "101010"	
VRC195	$((34R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "101011"	

VINP11



Table 79. Formulas for calculating gamma adjusting voltage (positive polarity) 1 (continued)

Pads	Formula	Micro-adjusting register value	Reference voltage
VRC194	$((35R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "101100"	VINP11
VRC193	$((36R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "101101"	
VRC192	$((37R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "101110"	
VRC191	$((38R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "101111"	
VRC190	$((39R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "110000"	
VRC189	$((40R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "110001"	
VRC188	$((41R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "110010"	
VRC187	$((42R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "110011"	
VRC186	$((43R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "110100"	
VRC185	$((44R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "110101"	
VRC184	$((45R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "110110"	
VRC183	$((46R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "110111"	
VRC182	$((47R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "111000"	
VRC181	$((48R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "111001"	
VRC180	$((49R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "111010"	
VRC179	$((50R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "111011"	
VRC178	$((51R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "111100"	
VRC177	$((52R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "111101"	
VRC176	$((53R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "111110"	
VRC175	$((54R+Ra)/Rt) * (VINP0 - VINP12) + VINP12$	PKP10[5:0] = "111111"	

Table 80. Formulas for calculating gamma adjusting voltage (positive polarity) 2

Grayscale Voltage	Formula			
	GSRP[3:0]			
	0001	0010	0100	1000
V0	VINP0			
V1	VINP1			
V2	$V1 - (V1 - V4) * (2/6)$	$V1 - (V1 - V5) * (2/8.5)$	$V1 - (V1 - V6) * (2/9.5)$	$V1 - (V1 - V7) * (2/11)$
V3	$V1 - (V1 - V4) * (4/6)$	$V1 - (V1 - V5) * (4/8.5)$	$V1 - (V1 - V6) * (4/9.5)$	$V1 - (V1 - V7) * (4/11)$
V4	VINP2	$V1 - (V1 - V5) * (6/8.5)$	$V1 - (V1 - V6) * (6/9.5)$	$V1 - (V1 - V7) * (6/11)$
V5	$V4 - (V4 - V11) * (2.5/10.5)$	VINP2	$V1 - (V1 - V6) * (8.5/9.5)$	$V1 - (V1 - V7) * (8.5/11)$
V6	$V4 - (V4 - V11) * (3.5/10.5)$	$V5 - (V5 - V11) * (1/8)$	VINP2	$V1 - (V1 - V7) * (9.5/11)$
V7	$V4 - (V4 - V11) * (5/10.5)$	$V5 - (V5 - V11) * (2.5/8)$	$V6 - (V6 - V11) * (1.5/7)$	VINP2
V8	$V4 - (V4 - V11) * (6.5/10.5)$	$V5 - (V5 - V11) * (4/8)$	$V6 - (V6 - V11) * (3/7)$	$V7 - (V7 - V11) * (1.5/5.5)$
V9	$V4 - (V4 - V11) * (7.5/10.5)$	$V5 - (V5 - V11) * (5/8)$	$V6 - (V6 - V11) * (4/7)$	$V7 - (V7 - V11) * (2.5/5.5)$
V10	$V4 - (V4 - V11) * (9.5/10.5)$	$V5 - (V5 - V11) * (7/8)$	$V6 - (V6 - V11) * (6/7)$	$V7 - (V7 - V11) * (4.5/5.5)$
V11	VINP3			
V12	$V11 - (V11 - V54) * (1/52.5)$	$V11 - (V11 - V55) * (1/53.5)$	$V11 - (V11 - V56) * (1/54.5)$	$V11 - (V11 - V57) * (1/56)$
V13	$V11 - (V11 - V54) * (3/52.5)$	$V11 - (V11 - V55) * (3/53.5)$	$V11 - (V11 - V56) * (3/54.5)$	$V11 - (V11 - V57) * (3/56)$
V14	$V11 - (V11 - V54) * (5/52.5)$	$V11 - (V11 - V55) * (5/53.5)$	$V11 - (V11 - V56) * (5/54.5)$	$V11 - (V11 - V57) * (5/56)$
V15	$V11 - (V11 - V54) * (6/52.5)$	$V11 - (V11 - V55) * (6/53.5)$	$V11 - (V11 - V56) * (6/54.5)$	$V11 - (V11 - V57) * (6/56)$
V16	$V11 - (V11 - V54) * (8/52.5)$	$V11 - (V11 - V55) * (8/53.5)$	$V11 - (V11 - V56) * (8/54.5)$	$V11 - (V11 - V57) * (8/56)$
V17	$V11 - (V11 - V54) * (9.5/52.5)$	$V11 - (V11 - V55) * (9.5/53.5)$	$V11 - (V11 - V56) * (9.5/54.5)$	$V11 - (V11 - V57) * (9.5/56)$
V18	$V11 - (V11 - V54) * (11.5/52.5)$	$V11 - (V11 - V55) * (11.5/53.5)$	$V11 - (V11 - V56) * (11.5/54.5)$	$V11 - (V11 - V57) * (11.5/56)$
V19	$V11 - (V11 - V54) * (12.5/52.5)$	$V11 - (V11 - V55) * (12.5/53.5)$	$V11 - (V11 - V56) * (12.5/54.5)$	$V11 - (V11 - V57) * (12.5/56)$
V20	$V11 - (V11 - V54) * (14/52.5)$	$V11 - (V11 - V55) * (14/53.5)$	$V11 - (V11 - V56) * (14/54.5)$	$V11 - (V11 - V57) * (14/56)$
V21	$V11 - (V11 - V54) * (15/52.5)$	$V11 - (V11 - V55) * (15/53.5)$	$V11 - (V11 - V56) * (15/54.5)$	$V11 - (V11 - V57) * (15/56)$
V22	$V11 - (V11 - V54) * (16/52.5)$	$V11 - (V11 - V55) * (16/53.5)$	$V11 - (V11 - V56) * (16/54.5)$	$V11 - (V11 - V57) * (16/56)$
V23	$V11 - (V11 - V54) * (17.5/52.5)$	$V11 - (V11 - V55) * (17.5/53.5)$	$V11 - (V11 - V56) * (17.5/54.5)$	$V11 - (V11 - V57) * (17.5/56)$
V24	$V11 - (V11 - V54) * (19.5/52.5)$	$V11 - (V11 - V55) * (19.5/53.5)$	$V11 - (V11 - V56) * (19.5/54.5)$	$V11 - (V11 - V57) * (19.5/56)$
V25	$V11 - (V11 - V54) * (21/52.5)$	$V11 - (V11 - V55) * (21/53.5)$	$V11 - (V11 - V56) * (21/54.5)$	$V11 - (V11 - V57) * (21/56)$
V26	$V11 - (V11 - V54) * (22/52.5)$	$V11 - (V11 - V55) * (22/53.5)$	$V11 - (V11 - V56) * (22/54.5)$	$V11 - (V11 - V57) * (22/56)$
V27	$V11 - (V11 - V54) * (23.5/52.5)$	$V11 - (V11 - V55) * (23.5/53.5)$	$V11 - (V11 - V56) * (23.5/54.5)$	$V11 - (V11 - V57) * (23.5/56)$
V28	$V11 - (V11 - V54) * (25/52.5)$	$V11 - (V11 - V55) * (25/53.5)$	$V11 - (V11 - V56) * (25/54.5)$	$V11 - (V11 - V57) * (25/56)$
V29	$V11 - (V11 - V54) * (26/52.5)$	$V11 - (V11 - V55) * (26/53.5)$	$V11 - (V11 - V56) * (26/54.5)$	$V11 - (V11 - V57) * (26/56)$
V30	$V11 - (V11 - V54) * (27/52.5)$	$V11 - (V11 - V55) * (27/53.5)$	$V11 - (V11 - V56) * (27/54.5)$	$V11 - (V11 - V57) * (27/56)$
V31	$V11 - (V11 - V54) * (29/52.5)$	$V11 - (V11 - V55) * (29/53.5)$	$V11 - (V11 - V56) * (29/54.5)$	$V11 - (V11 - V57) * (29/56)$
V32	$V11 - (V11 - V54) * (30/52.5)$	$V11 - (V11 - V55) * (30/53.5)$	$V11 - (V11 - V56) * (30/54.5)$	$V11 - (V11 - V57) * (30/56)$
V33	$V11 - (V11 - V54) * (31/52.5)$	$V11 - (V11 - V55) * (31/53.5)$	$V11 - (V11 - V56) * (31/54.5)$	$V11 - (V11 - V57) * (31/56)$



Table 81. Formulas for calculating gamma adjusting voltage (positive polarity) 2 (continued)

Grayscale Voltage	Formula			
	GSRP[3:0]			
	0001	0010	0100	1000
V34	$V11-(V11-V54)*(32/52.5)$	$V11-(V11-V55)*(32/53.5)$	$V11-(V11-V56)*(32/54.5)$	$V11-(V11-V57)*(32/56)$
V35	$V11-(V11-V54)*(33/52.5)$	$V11-(V11-V55)*(33/53.5)$	$V11-(V11-V56)*(33/54.5)$	$V11-(V11-V57)*(33/56)$
V36	$V11-(V11-V54)*(34/52.5)$	$V11-(V11-V55)*(34/53.5)$	$V11-(V11-V56)*(34/54.5)$	$V11-(V11-V57)*(34/56)$
V37	$V11-(V11-V54)*(35/52.5)$	$V11-(V11-V55)*(35/53.5)$	$V11-(V11-V56)*(35/54.5)$	$V11-(V11-V57)*(35/56)$
V38	$V11-(V11-V54)*(36.5/52.5)$	$V11-(V11-V55)*(36.5/53.5)$	$V11-(V11-V56)*(36.5/54.5)$	$V11-(V11-V57)*(36.5/56)$
V39	$V11-(V11-V54)*(37.5/52.5)$	$V11-(V11-V55)*(37.5/53.5)$	$V11-(V11-V56)*(37.5/54.5)$	$V11-(V11-V57)*(37.5/56)$
V40	$V11-(V11-V54)*(38.5/52.5)$	$V11-(V11-V55)*(38.5/53.5)$	$V11-(V11-V56)*(38.5/54.5)$	$V11-(V11-V57)*(38.5/56)$
V41	$V11-(V11-V54)*(39.5/52.5)$	$V11-(V11-V55)*(39.5/53.5)$	$V11-(V11-V56)*(39.5/54.5)$	$V11-(V11-V57)*(39.5/56)$
V42	$V11-(V11-V54)*(40.5/52.5)$	$V11-(V11-V55)*(40.5/53.5)$	$V11-(V11-V56)*(40.5/54.5)$	$V11-(V11-V57)*(40.5/56)$
V43	$V11-(V11-V54)*(41.5/52.5)$	$V11-(V11-V55)*(41.5/53.5)$	$V11-(V11-V56)*(41.5/54.5)$	$V11-(V11-V57)*(41.5/56)$
V44	$V11-(V11-V54)*(42.5/52.5)$	$V11-(V11-V55)*(42.5/53.5)$	$V11-(V11-V56)*(42.5/54.5)$	$V11-(V11-V57)*(42.5/56)$
V45	$V11-(V11-V54)*(43.5/52.5)$	$V11-(V11-V55)*(43.5/53.5)$	$V11-(V11-V56)*(43.5/54.5)$	$V11-(V11-V57)*(43.5/56)$
V46	$V11-(V11-V54)*(44.5/52.5)$	$V11-(V11-V55)*(44.5/53.5)$	$V11-(V11-V56)*(44.5/54.5)$	$V11-(V11-V57)*(44.5/56)$
V47	$V11-(V11-V54)*(45.5/52.5)$	$V11-(V11-V55)*(45.5/53.5)$	$V11-(V11-V56)*(45.5/54.5)$	$V11-(V11-V57)*(45.5/56)$
V48	$V11-(V11-V54)*(46.5/52.5)$	$V11-(V11-V55)*(46.5/53.5)$	$V11-(V11-V56)*(46.5/54.5)$	$V11-(V11-V57)*(46.5/56)$
V49	$V11-(V11-V54)*(47.5/52.5)$	$V11-(V11-V55)*(47.5/53.5)$	$V11-(V11-V56)*(47.5/54.5)$	$V11-(V11-V57)*(47.5/56)$
V50	$V11-(V11-V54)*(48.5/52.5)$	$V11-(V11-V55)*(48.5/53.5)$	$V11-(V11-V56)*(48.5/54.5)$	$V11-(V11-V57)*(48.5/56)$
V51	$V11-(V11-V54)*(49.5/52.5)$	$V11-(V11-V55)*(49.5/53.5)$	$V11-(V11-V56)*(49.5/54.5)$	$V11-(V11-V57)*(49.5/56)$
V52	$V11-(V11-V54)*(50.5/52.5)$	$V11-(V11-V55)*(50.5/53.5)$	$V11-(V11-V56)*(50.5/54.5)$	$V11-(V11-V57)*(50.5/56)$
V53	$V11-(V11-V54)*(51.5/52.5)$	$V11-(V11-V55)*(51.5/53.5)$	$V11-(V11-V56)*(51.5/54.5)$	$V11-(V11-V57)*(51.5/56)$
V54	VINP4	$V11-(V11-V55)*(52.5/53.5)$	$V11-(V11-V56)*(52.5/54.5)$	$V11-(V11-V57)*(52.5/56)$
V55	$V54-(V54-V95)*(1/42)$	VINP4	$V11-(V11-V56)*(53.5/54.5)$	$V11-(V11-V57)*(53.5/56)$
V56	$V54-(V54-V95)*(2/42)$	$V55-(V55-V95)*(1/41)$	VINP4	$V11-(V11-V57)*(54.5/56)$
V57	$V54-(V54-V95)*(3.5/42)$	$V55-(V55-V95)*(2.5/41)$	$V56-(V56-V95)*(1.5/40)$	VINP4
V58	$V54-(V54-V95)*(4.5/42)$	$V55-(V55-V95)*(3.5/41)$	$V56-(V56-V95)*(2.5/40)$	$V57-(V57-V95)*(1/38.5)$
V59	$V54-(V54-V95)*(5.5/42)$	$V55-(V55-V95)*(4.5/41)$	$V56-(V56-V95)*(3.5/40)$	$V57-(V57-V95)*(2/38.5)$
V60	$V54-(V54-V95)*(7/42)$	$V55-(V55-V95)*(6/41)$	$V56-(V56-V95)*(5/40)$	$V57-(V57-V95)*(3.5/38.5)$
V61	$V54-(V54-V95)*(8/42)$	$V55-(V55-V95)*(7/41)$	$V56-(V56-V95)*(6/40)$	$V57-(V57-V95)*(4.5/38.5)$
V62	$V54-(V54-V95)*(9/42)$	$V55-(V55-V95)*(8/41)$	$V56-(V56-V95)*(7/40)$	$V57-(V57-V95)*(5.5/38.5)$
V63	$V54-(V54-V95)*(10/42)$	$V55-(V55-V95)*(9/41)$	$V56-(V56-V95)*(8/40)$	$V57-(V57-V95)*(6.5/38.5)$
V64	$V54-(V54-V95)*(11/42)$	$V55-(V55-V95)*(10/41)$	$V56-(V56-V95)*(9/40)$	$V57-(V57-V95)*(7.5/38.5)$
V65	$V54-(V54-V95)*(12/42)$	$V55-(V55-V95)*(11/41)$	$V56-(V56-V95)*(10/40)$	$V57-(V57-V95)*(8.5/38.5)$
V66	$V54-(V54-V95)*(13/42)$	$V55-(V55-V95)*(12/41)$	$V56-(V56-V95)*(11/40)$	$V57-(V57-V95)*(9.5/38.5)$
V67	$V54-(V54-V95)*(14/42)$	$V55-(V55-V95)*(13/41)$	$V56-(V56-V95)*(12/40)$	$V57-(V57-V95)*(10.5/38.5)$



Table 82. Formulas for calculating gamma adjusting voltage (positive polarity) 2 (continued)

Grayscale Voltage	Formula			
	GSRP[3:0]			
	0001	0010	0100	1000
V68	$V54-(V54-V95)*(15/42)$	$V55-(V55-V95)*(14/41)$	$V56-(V56-V95)*(13/40)$	$V57-(V57-V95)*(11.5/38.5)$
V69	$V54-(V54-V95)*(16/42)$	$V55-(V55-V95)*(15/41)$	$V56-(V56-V95)*(14/40)$	$V57-(V57-V95)*(12.5/38.5)$
V70	$V54-(V54-V95)*(17/42)$	$V55-(V55-V95)*(16/41)$	$V56-(V56-V95)*(15/40)$	$V57-(V57-V95)*(13.5/38.5)$
V71	$V54-(V54-V95)*(18/42)$	$V55-(V55-V95)*(17/41)$	$V56-(V56-V95)*(16/40)$	$V57-(V57-V95)*(14.5/38.5)$
V72	$V54-(V54-V95)*(19/42)$	$V55-(V55-V95)*(18/41)$	$V56-(V56-V95)*(17/40)$	$V57-(V57-V95)*(15.5/38.5)$
V73	$V54-(V54-V95)*(20/42)$	$V55-(V55-V95)*(19/41)$	$V56-(V56-V95)*(18/40)$	$V57-(V57-V95)*(16.5/38.5)$
V74	$V54-(V54-V95)*(21/42)$	$V55-(V55-V95)*(20/41)$	$V56-(V56-V95)*(19/40)$	$V57-(V57-V95)*(17.5/38.5)$
V75	$V54-(V54-V95)*(22/42)$	$V55-(V55-V95)*(21/41)$	$V56-(V56-V95)*(20/40)$	$V57-(V57-V95)*(18.5/38.5)$
V76	$V54-(V54-V95)*(23/42)$	$V55-(V55-V95)*(22/41)$	$V56-(V56-V95)*(21/40)$	$V57-(V57-V95)*(19.5/38.5)$
V77	$V54-(V54-V95)*(24/42)$	$V55-(V55-V95)*(23/41)$	$V56-(V56-V95)*(22/40)$	$V57-(V57-V95)*(20.5/38.5)$
V78	$V54-(V54-V95)*(25/42)$	$V55-(V55-V95)*(24/41)$	$V56-(V56-V95)*(23/40)$	$V57-(V57-V95)*(21.5/38.5)$
V79	$V54-(V54-V95)*(26/42)$	$V55-(V55-V95)*(25/41)$	$V56-(V56-V95)*(24/40)$	$V57-(V57-V95)*(22.5/38.5)$
V80	$V54-(V54-V95)*(27/42)$	$V55-(V55-V95)*(26/41)$	$V56-(V56-V95)*(25/40)$	$V57-(V57-V95)*(23.5/38.5)$
V81	$V54-(V54-V95)*(28/42)$	$V55-(V55-V95)*(27/41)$	$V56-(V56-V95)*(26/40)$	$V57-(V57-V95)*(24.5/38.5)$
V82	$V54-(V54-V95)*(29/42)$	$V55-(V55-V95)*(28/41)$	$V56-(V56-V95)*(27/40)$	$V57-(V57-V95)*(25.5/38.5)$
V83	$V54-(V54-V95)*(30/42)$	$V55-(V55-V95)*(29/41)$	$V56-(V56-V95)*(28/40)$	$V57-(V57-V95)*(26.5/38.5)$
V84	$V54-(V54-V95)*(31/42)$	$V55-(V55-V95)*(30/41)$	$V56-(V56-V95)*(29/40)$	$V57-(V57-V95)*(27.5/38.5)$
V85	$V54-(V54-V95)*(32/42)$	$V55-(V55-V95)*(31/41)$	$V56-(V56-V95)*(30/40)$	$V57-(V57-V95)*(28.5/38.5)$
V86	$V54-(V54-V95)*(33/42)$	$V55-(V55-V95)*(32/41)$	$V56-(V56-V95)*(31/40)$	$V57-(V57-V95)*(29.5/38.5)$
V87	$V54-(V54-V95)*(34/42)$	$V55-(V55-V95)*(33/41)$	$V56-(V56-V95)*(32/40)$	$V57-(V57-V95)*(30.5/38.5)$
V88	$V54-(V54-V95)*(35/42)$	$V55-(V55-V95)*(34/41)$	$V56-(V56-V95)*(33/40)$	$V57-(V57-V95)*(31.5/38.5)$
V89	$V54-(V54-V95)*(36/42)$	$V55-(V55-V95)*(35/41)$	$V56-(V56-V95)*(34/40)$	$V57-(V57-V95)*(32.5/38.5)$
V90	$V54-(V54-V95)*(37/42)$	$V55-(V55-V95)*(36/41)$	$V56-(V56-V95)*(35/40)$	$V57-(V57-V95)*(33.5/38.5)$
V91	$V54-(V54-V95)*(38/42)$	$V55-(V55-V95)*(37/41)$	$V56-(V56-V95)*(36/40)$	$V57-(V57-V95)*(34.5/38.5)$
V92	$V54-(V54-V95)*(39/42)$	$V55-(V55-V95)*(38/41)$	$V56-(V56-V95)*(37/40)$	$V57-(V57-V95)*(35.5/38.5)$
V93	$V54-(V54-V95)*(40/42)$	$V55-(V55-V95)*(39/41)$	$V56-(V56-V95)*(38/40)$	$V57-(V57-V95)*(36.5/38.5)$
V94	$V54-(V54-V95)*(41/42)$	$V55-(V55-V95)*(40/41)$	$V56-(V56-V95)*(39/40)$	$V57-(V57-V95)*(37.5/38.5)$
V95	VINP5			
V96	$V95-(V95-VC)*(1/33)$			
V97	$V95-(V95-VC)*(2/33)$			
V98	$V95-(V95-VC)*(3/33)$			
V99	$V95-(V95-VC)*(4/33)$			
V100	$V95-(V95-VC)*(5/33)$			
V101	$V95-(V95-VC)*(6/33)$			



Table 83. Formulas for calculating gamma adjusting voltage (positive polarity) 2 (continued)

Grayscale Voltage	Formula			
	GSRP[3:0]			
	0001	0010	0100	1000
V102		$V95-(V95-VC)*(7/33)$		
V103		$V95-(V95-VC)*(8/33)$		
V104		$V95-(V95-VC)*(9/33)$		
V105		$V95-(V95-VC)*(10/33)$		
V106		$V95-(V95-VC)*(11/33)$		
V107		$V95-(V95-VC)*(12/33)$		
V108		$V95-(V95-VC)*(13/33)$		
V109		$V95-(V95-VC)*(14/33)$		
V110		$V95-(V95-VC)*(15/33)$		
V111		$V95-(V95-VC)*(16/33)$		
V112		$V95-(V95-VC)*(17/33)$		
V113		$V95-(V95-VC)*(18/33)$		
V114		$V95-(V95-VC)*(19/33)$		
V115		$V95-(V95-VC)*(20/33)$		
V116		$V95-(V95-VC)*(21/33)$		
V117		$V95-(V95-VC)*(22/33)$		
V118		$V95-(V95-VC)*(23/33)$		
V119		$V95-(V95-VC)*(24.5/33)$		
V120		$V95-(V95-VC)*(25.5/33)$		
V121		$V95-(V95-VC)*(26.5/33)$		
V122		$V95-(V95-VC)*(27.5/33)$		
V123		$V95-(V95-VC)*(28.5/33)$		
V124		$V95-(V95-VC)*(29.5/33)$		
V125		$V95-(V95-VC)*(30.5/33)$		
V126		$V95-(V95-VC)*(31/33)$		
V127		$V95-(V95-VC)*(32/33)$		
VC	VINP6			
V128		$VC-(VC-V160)*(0.5/32)$		
V129		$VC-(VC-V160)*(1.5/32)$		
V130		$VC-(VC-V160)*(2.5/32)$		
V131		$VC-(VC-V160)*(3.5/32)$		
V132		$VC-(VC-V160)*(4.5/32)$		
V133		$VC-(VC-V160)*(5.5/32)$		
V134		$VC-(VC-V160)*(6.5/32)$		



Table 84. Formulas for calculating gamma adjusting voltage (positive polarity) 2 (continued)

Grayscale Voltage	Formula			
	GSRP[3:0]			
	0001	0010	0100	1000
V135		VC-(VC-V160)*(7.5/32)		
V136		VC-(VC-V160)*(8.5/32)		
V137		VC-(VC-V160)*(9/32)		
V138		VC-(VC-V160)*(10/32)		
V139		VC-(VC-V160)*(11/32)		
V140		VC-(VC-V160)*(12/32)		
V141		VC-(VC-V160)*(13/32)		
V142		VC-(VC-V160)*(14/32)		
V143		VC-(VC-V160)*(15/32)		
V144		VC-(VC-V160)*(16/32)		
V145		VC-(VC-V160)*(17/32)		
V146		VC-(VC-V160)*(18/32)		
V147		VC-(VC-V160)*(19/32)		
V148		VC-(VC-V160)*(20/32)		
V149		VC-(VC-V160)*(21/32)		
V150		VC-(VC-V160)*(22/32)		
V151		VC-(VC-V160)*(23/32)		
V152		VC-(VC-V160)*(24.5/32)		
V153		VC-(VC-V160)*(25.5/32)		
V154		VC-(VC-V160)*(26.5/32)		
V155		VC-(VC-V160)*(27.5/32)		
V156		VC-(VC-V160)*(28.5/32)		
V157		VC-(VC-V160)*(29.5/32)		
V158		VC-(VC-V160)*(30/32)		
V159		VC-(VC-V160)*(31/32)		
V160	VINP7			
V161	V160-(V160-V199)*(1/40.5)	V160-(V160-V200)*(1/41.5)	V160-(V160-V201)*(1/42.5)	V160-(V160-V202)*(1/43)
V162	V160-(V160-V199)*(2/40.5)	V160-(V160-V200)*(2/41.5)	V160-(V160-V201)*(2/42.5)	V160-(V160-V202)*(2/43)
V163	V160-(V160-V199)*(3/40.5)	V160-(V160-V200)*(3/41.5)	V160-(V160-V201)*(3/42.5)	V160-(V160-V202)*(3/43)
V164	V160-(V160-V199)*(3.5/40.5)	V160-(V160-V200)*(3.5/41.5)	V160-(V160-V201)*(3.5/42.5)	V160-(V160-V202)*(3.5/43)
V165	V160-(V160-V199)*(4.5/40.5)	V160-(V160-V200)*(4.5/41.5)	V160-(V160-V201)*(4.5/42.5)	V160-(V160-V202)*(4.5/43)
V166	V160-(V160-V199)*(5.5/40.5)	V160-(V160-V200)*(5.5/41.5)	V160-(V160-V201)*(5.5/42.5)	V160-(V160-V202)*(5.5/43)
V167	V160-(V160-V199)*(6.5/40.5)	V160-(V160-V200)*(6.5/41.5)	V160-(V160-V201)*(6.5/42.5)	V160-(V160-V202)*(6.5/43)
V168	V160-(V160-V199)*(7.5/40.5)	V160-(V160-V200)*(7.5/41.5)	V160-(V160-V201)*(7.5/42.5)	V160-(V160-V202)*(7.5/43)



Table 85. Formulas for calculating gamma adjusting voltage (positive polarity) 2 (continued)

Grayscale Voltage	Formula			
	GSRP[3:0]			
	0001	0010	0100	1000
V169	$V160 - (V160 - V199) * (8.5 / 40.5)$	$V160 - (V160 - V200) * (8.5 / 41.5)$	$V160 - (V160 - V201) * (8.5 / 42.5)$	$V160 - (V160 - V202) * (8.5 / 43)$
V170	$V160 - (V160 - V199) * (9.5 / 40.5)$	$V160 - (V160 - V200) * (9.5 / 41.5)$	$V160 - (V160 - V201) * (9.5 / 42.5)$	$V160 - (V160 - V202) * (9.5 / 43)$
V171	$V160 - (V160 - V199) * (10.5 / 40.5)$	$V160 - (V160 - V200) * (10.5 / 41.5)$	$V160 - (V160 - V201) * (10.5 / 42.5)$	$V160 - (V160 - V202) * (10.5 / 43)$
V172	$V160 - (V160 - V199) * (11.5 / 40.5)$	$V160 - (V160 - V200) * (11.5 / 41.5)$	$V160 - (V160 - V201) * (11.5 / 42.5)$	$V160 - (V160 - V202) * (11.5 / 43)$
V173	$V160 - (V160 - V199) * (12.5 / 40.5)$	$V160 - (V160 - V200) * (12.5 / 41.5)$	$V160 - (V160 - V201) * (12.5 / 42.5)$	$V160 - (V160 - V202) * (12.5 / 43)$
V174	$V160 - (V160 - V199) * (13.5 / 40.5)$	$V160 - (V160 - V200) * (13.5 / 41.5)$	$V160 - (V160 - V201) * (13.5 / 42.5)$	$V160 - (V160 - V202) * (13.5 / 43)$
V175	$V160 - (V160 - V199) * (14.5 / 40.5)$	$V160 - (V160 - V200) * (14.5 / 41.5)$	$V160 - (V160 - V201) * (14.5 / 42.5)$	$V160 - (V160 - V202) * (14.5 / 43)$
V176	$V160 - (V160 - V199) * (15.5 / 40.5)$	$V160 - (V160 - V200) * (15.5 / 41.5)$	$V160 - (V160 - V201) * (15.5 / 42.5)$	$V160 - (V160 - V202) * (15.5 / 43)$
V177	$V160 - (V160 - V199) * (16.5 / 40.5)$	$V160 - (V160 - V200) * (16.5 / 41.5)$	$V160 - (V160 - V201) * (16.5 / 42.5)$	$V160 - (V160 - V202) * (16.5 / 43)$
V178	$V160 - (V160 - V199) * (17.5 / 40.5)$	$V160 - (V160 - V200) * (17.5 / 41.5)$	$V160 - (V160 - V201) * (17.5 / 42.5)$	$V160 - (V160 - V202) * (17.5 / 43)$
V179	$V160 - (V160 - V199) * (18.5 / 40.5)$	$V160 - (V160 - V200) * (18.5 / 41.5)$	$V160 - (V160 - V201) * (18.5 / 42.5)$	$V160 - (V160 - V202) * (18.5 / 43)$
V180	$V160 - (V160 - V199) * (19.5 / 40.5)$	$V160 - (V160 - V200) * (19.5 / 41.5)$	$V160 - (V160 - V201) * (19.5 / 42.5)$	$V160 - (V160 - V202) * (19.5 / 43)$
V181	$V160 - (V160 - V199) * (20.5 / 40.5)$	$V160 - (V160 - V200) * (20.5 / 41.5)$	$V160 - (V160 - V201) * (20.5 / 42.5)$	$V160 - (V160 - V202) * (20.5 / 43)$
V182	$V160 - (V160 - V199) * (21.5 / 40.5)$	$V160 - (V160 - V200) * (21.5 / 41.5)$	$V160 - (V160 - V201) * (21.5 / 42.5)$	$V160 - (V160 - V202) * (21.5 / 43)$
V183	$V160 - (V160 - V199) * (22.5 / 40.5)$	$V160 - (V160 - V200) * (22.5 / 41.5)$	$V160 - (V160 - V201) * (22.5 / 42.5)$	$V160 - (V160 - V202) * (22.5 / 43)$
V184	$V160 - (V160 - V199) * (23.5 / 40.5)$	$V160 - (V160 - V200) * (23.5 / 41.5)$	$V160 - (V160 - V201) * (23.5 / 42.5)$	$V160 - (V160 - V202) * (23.5 / 43)$
V185	$V160 - (V160 - V199) * (24.5 / 40.5)$	$V160 - (V160 - V200) * (24.5 / 41.5)$	$V160 - (V160 - V201) * (24.5 / 42.5)$	$V160 - (V160 - V202) * (24.5 / 43)$
V186	$V160 - (V160 - V199) * (25.5 / 40.5)$	$V160 - (V160 - V200) * (25.5 / 41.5)$	$V160 - (V160 - V201) * (25.5 / 42.5)$	$V160 - (V160 - V202) * (25.5 / 43)$
V187	$V160 - (V160 - V199) * (26.5 / 40.5)$	$V160 - (V160 - V200) * (26.5 / 41.5)$	$V160 - (V160 - V201) * (26.5 / 42.5)$	$V160 - (V160 - V202) * (26.5 / 43)$
V188	$V160 - (V160 - V199) * (27.5 / 40.5)$	$V160 - (V160 - V200) * (27.5 / 41.5)$	$V160 - (V160 - V201) * (27.5 / 42.5)$	$V160 - (V160 - V202) * (27.5 / 43)$
V189	$V160 - (V160 - V199) * (29.5 / 40.5)$	$V160 - (V160 - V200) * (29.5 / 41.5)$	$V160 - (V160 - V201) * (29.5 / 42.5)$	$V160 - (V160 - V202) * (29.5 / 43)$
V190	$V160 - (V160 - V199) * (30.5 / 40.5)$	$V160 - (V160 - V200) * (30.5 / 41.5)$	$V160 - (V160 - V201) * (30.5 / 42.5)$	$V160 - (V160 - V202) * (30.5 / 43)$
V191	$V160 - (V160 - V199) * (31.5 / 40.5)$	$V160 - (V160 - V200) * (31.5 / 41.5)$	$V160 - (V160 - V201) * (31.5 / 42.5)$	$V160 - (V160 - V202) * (31.5 / 43)$
V192	$V160 - (V160 - V199) * (32.5 / 40.5)$	$V160 - (V160 - V200) * (32.5 / 41.5)$	$V160 - (V160 - V201) * (32.5 / 42.5)$	$V160 - (V160 - V202) * (32.5 / 43)$
V193	$V160 - (V160 - V199) * (33.5 / 40.5)$	$V160 - (V160 - V200) * (33.5 / 41.5)$	$V160 - (V160 - V201) * (33.5 / 42.5)$	$V160 - (V160 - V202) * (33.5 / 43)$
V194	$V160 - (V160 - V199) * (35 / 40.5)$	$V160 - (V160 - V200) * (35 / 41.5)$	$V160 - (V160 - V201) * (35 / 42.5)$	$V160 - (V160 - V202) * (35 / 43)$
V195	$V160 - (V160 - V199) * (36 / 40.5)$	$V160 - (V160 - V200) * (36 / 41.5)$	$V160 - (V160 - V201) * (36 / 42.5)$	$V160 - (V160 - V202) * (36 / 43)$
V196	$V160 - (V160 - V199) * (37 / 40.5)$	$V160 - (V160 - V200) * (37 / 41.5)$	$V160 - (V160 - V201) * (37 / 42.5)$	$V160 - (V160 - V202) * (37 / 43)$
V197	$V160 - (V160 - V199) * (38 / 40.5)$	$V160 - (V160 - V200) * (38 / 41.5)$	$V160 - (V160 - V201) * (38 / 42.5)$	$V160 - (V160 - V202) * (38 / 43)$
V198	$V160 - (V160 - V199) * (39.5 / 40.5)$	$V160 - (V160 - V200) * (39.5 / 41.5)$	$V160 - (V160 - V201) * (39.5 / 42.5)$	$V160 - (V160 - V202) * (39.5 / 43)$
V199	VINP8	$V160 - (V160 - V200) * (40.5 / 41.5)$	$V160 - (V160 - V201) * (40.5 / 42.5)$	$V160 - (V160 - V202) * (40.5 / 43)$
V200	$V199 - (V199 - V244) * (1 / 50.5)$	VINP8	$V160 - (V160 - V201) * (41.5 / 42.5)$	$V160 - (V160 - V202) * (41.5 / 43)$
V201	$V199 - (V199 - V244) * (2 / 50.5)$	$V200 - (V200 - V244) * (1 / 49.5)$	VINP8	$V160 - (V160 - V202) * (42.5 / 43)$
V202	$V199 - (V199 - V244) * (2.5 / 50.5)$	$V200 - (V200 - V244) * (1.5 / 49.5)$	$V201 - (V201 - V244) * (0.5 / 48.5)$	VINP8



**Table 86. Formulas for calculating gamma adjusting voltage (positive polarity) 2 (continued)**

Grayscale Voltage	Formula			
	GSRP[3:0]			
	0001	0010	0100	1000
V203	$V199 - (V199-V244)*(3/50.5)$	$V200 - (V200-V244)*(2/49.5)$	$V201 - (V201-V244)*(1/48.5)$	$V202 - (V202-V244)*(0.5/48)$
V204	$V199 - (V199-V244)*(3.5/50.5)$	$V200 - (V200-V244)*(2.5/49.5)$	$V201 - (V201-V244)*(1.5/48.5)$	$V202 - (V202-V244)*(1/48)$
V205	$V199 - (V199-V244)*(5/50.5)$	$V200 - (V200-V244)*(4/49.5)$	$V201 - (V201-V244)*(3/48.5)$	$V202 - (V202-V244)*(2.5/48)$
V206	$V199 - (V199-V244)*(5.5/50.5)$	$V200 - (V200-V244)*(4.5/49.5)$	$V201 - (V201-V244)*(3.5/48.5)$	$V202 - (V202-V244)*(3/48)$
V207	$V199 - (V199-V244)*(6/50.5)$	$V200 - (V200-V244)*(5/49.5)$	$V201 - (V201-V244)*(4/48.5)$	$V202 - (V202-V244)*(3.5/48)$
V208	$V199 - (V199-V244)*(6.5/50.5)$	$V200 - (V200-V244)*(5.5/49.5)$	$V201 - (V201-V244)*(4.5/48.5)$	$V202 - (V202-V244)*(4/48)$
V209	$V199 - (V199-V244)*(7.5/50.5)$	$V200 - (V200-V244)*(6.5/49.5)$	$V201 - (V201-V244)*(5.5/48.5)$	$V202 - (V202-V244)*(5/48)$
V210	$V199 - (V199-V244)*(8/50.5)$	$V200 - (V200-V244)*(7/49.5)$	$V201 - (V201-V244)*(6/48.5)$	$V202 - (V202-V244)*(5.5/48)$
V211	$V199 - (V199-V244)*(9/50.5)$	$V200 - (V200-V244)*(8/49.5)$	$V201 - (V201-V244)*(7/48.5)$	$V202 - (V202-V244)*(6.5/48)$
V212	$V199 - (V199-V244)*(10/50.5)$	$V200 - (V200-V244)*(9/49.5)$	$V201 - (V201-V244)*(8/48.5)$	$V202 - (V202-V244)*(7.5/48)$
V213	$V199 - (V199-V244)*(11/50.5)$	$V200 - (V200-V244)*(10/49.5)$	$V201 - (V201-V244)*(9/48.5)$	$V202 - (V202-V244)*(8.5/48)$
V214	$V199 - (V199-V244)*(11.5/50.5)$	$V200 - (V200-V244)*(10.5/49.5)$	$V201 - (V201-V244)*(9.5/48.5)$	$V202 - (V202-V244)*(9/48)$
V215	$V199 - (V199-V244)*(12/50.5)$	$V200 - (V200-V244)*(11/49.5)$	$V201 - (V201-V244)*(10/48.5)$	$V202 - (V202-V244)*(9.5/48)$
V216	$V199 - (V199-V244)*(13/50.5)$	$V200 - (V200-V244)*(12/49.5)$	$V201 - (V201-V244)*(11/48.5)$	$V202 - (V202-V244)*(10.5/48)$
V217	$V199 - (V199-V244)*(14/50.5)$	$V200 - (V200-V244)*(13/49.5)$	$V201 - (V201-V244)*(12/48.5)$	$V202 - (V202-V244)*(11.5/48)$
V218	$V199 - (V199-V244)*(15/50.5)$	$V200 - (V200-V244)*(14/49.5)$	$V201 - (V201-V244)*(13/48.5)$	$V202 - (V202-V244)*(12.5/48)$
V219	$V199 - (V199-V244)*(16/50.5)$	$V200 - (V200-V244)*(15/49.5)$	$V201 - (V201-V244)*(14/48.5)$	$V202 - (V202-V244)*(13.5/48)$
V220	$V199 - (V199-V244)*(17/50.5)$	$V200 - (V200-V244)*(16/49.5)$	$V201 - (V201-V244)*(15/48.5)$	$V202 - (V202-V244)*(14.5/48)$
V221	$V199 - (V199-V244)*(18/50.5)$	$V200 - (V200-V244)*(17/49.5)$	$V201 - (V201-V244)*(16/48.5)$	$V202 - (V202-V244)*(15.5/48)$
V222	$V199 - (V199-V244)*(19/50.5)$	$V200 - (V200-V244)*(18/49.5)$	$V201 - (V201-V244)*(17/48.5)$	$V202 - (V202-V244)*(16.5/48)$
V223	$V199 - (V199-V244)*(20/50.5)$	$V200 - (V200-V244)*(19/49.5)$	$V201 - (V201-V244)*(18/48.5)$	$V202 - (V202-V244)*(17.5/48)$
V224	$V199 - (V199-V244)*(21/50.5)$	$V200 - (V200-V244)*(20/49.5)$	$V201 - (V201-V244)*(19/48.5)$	$V202 - (V202-V244)*(18.5/48)$
V225	$V199 - (V199-V244)*(22/50.5)$	$V200 - (V200-V244)*(21/49.5)$	$V201 - (V201-V244)*(20/48.5)$	$V202 - (V202-V244)*(19.5/48)$
V226	$V199 - (V199-V244)*(23/50.5)$	$V200 - (V200-V244)*(22/49.5)$	$V201 - (V201-V244)*(21/48.5)$	$V202 - (V202-V244)*(20.5/48)$
V227	$V199 - (V199-V244)*(24/50.5)$	$V200 - (V200-V244)*(23/49.5)$	$V201 - (V201-V244)*(22/48.5)$	$V202 - (V202-V244)*(21.5/48)$
V228	$V199 - (V199-V244)*(25.5/50.5)$	$V200 - (V200-V244)*(24.5/49.5)$	$V201 - (V201-V244)*(23.5/48.5)$	$V202 - (V202-V244)*(23/48)$
V229	$V199 - (V199-V244)*(26.5/50.5)$	$V200 - (V200-V244)*(25.5/49.5)$	$V201 - (V201-V244)*(24.5/48.5)$	$V202 - (V202-V244)*(24/48)$
V230	$V199 - (V199-V244)*(27.5/50.5)$	$V200 - (V200-V244)*(26.5/49.5)$	$V201 - (V201-V244)*(25.5/48.5)$	$V202 - (V202-V244)*(25/48)$
V231	$V199 - (V199-V244)*(29/50.5)$	$V200 - (V200-V244)*(28/49.5)$	$V201 - (V201-V244)*(27/48.5)$	$V202 - (V202-V244)*(26.5/48)$
V232	$V199 - (V199-V244)*(30.5/50.5)$	$V200 - (V200-V244)*(29.5/49.5)$	$V201 - (V201-V244)*(28.5/48.5)$	$V202 - (V202-V244)*(28/48)$
V233	$V199 - (V199-V244)*(32/50.5)$	$V200 - (V200-V244)*(31/49.5)$	$V201 - (V201-V244)*(30/48.5)$	$V202 - (V202-V244)*(29.5/48)$
V234	$V199 - (V199-V244)*(33.5/50.5)$	$V200 - (V200-V244)*(32.5/49.5)$	$V201 - (V201-V244)*(31.5/48.5)$	$V202 - (V202-V244)*(31/48)$
V235	$V199 - (V199-V244)*(34.5/50.5)$	$V200 - (V200-V244)*(33.5/49.5)$	$V201 - (V201-V244)*(32.5/48.5)$	$V202 - (V202-V244)*(32/48)$
V236	$V199 - (V199-V244)*(36/50.5)$	$V200 - (V200-V244)*(35/49.5)$	$V201 - (V201-V244)*(34/48.5)$	$V202 - (V202-V244)*(33.5/48)$



**Table 87. Formulas for calculating gamma adjusting voltage (positive polarity) 2 (continued)**

Grayscale Voltage	Formula			
	GSRP[3:0]			
	0001	0010	0100	1000
V237	$V199-(V199-V244)*(37.5/50.5)$	$V200-(V200-V244)*(36.5/49.5)$	$V201-(V201-V244)*(35.5/48.5)$	$V202-(V202-V244)*(35/48)$
V238	$V199-(V199-V244)*(39.5/50.5)$	$V200-(V200-V244)*(38.5/49.5)$	$V201-(V201-V244)*(37.5/48.5)$	$V202-(V202-V244)*(37/48)$
V239	$V199-(V199-V244)*(40.5/50.5)$	$V200-(V200-V244)*(39.5/49.5)$	$V201-(V201-V244)*(38.5/48.5)$	$V202-(V202-V244)*(38/48)$
V240	$V199-(V199-V244)*(42.5/50.5)$	$V200-(V200-V244)*(41.5/49.5)$	$V201-(V201-V244)*(40.5/48.5)$	$V202-(V202-V244)*(40/48)$
V241	$V199-(V199-V244)*(44.5/50.5)$	$V200-(V200-V244)*(43.5/49.5)$	$V201-(V201-V244)*(42.5/48.5)$	$V202-(V202-V244)*(42/48)$
V242	$V199-(V199-V244)*(46.5/50.5)$	$V200-(V200-V244)*(45.5/49.5)$	$V201-(V201-V244)*(44.5/48.5)$	$V202-(V202-V244)*(44/48)$
V243	$V199-(V199-V244)*(48.5/50.5)$	$V200-(V200-V244)*(47.5/49.5)$	$V201-(V201-V244)*(46.5/48.5)$	$V202-(V202-V244)*(46/48)$
V244	VINP9			
V245	$V244-(V244-V249)*(1.5/9.5)$	$V244-(V244-V250)*(1.5/13)$	$V244-(V244-V251)*(1.5/15)$	$V244-(V244-V252)*(1.5/17)$
V246	$V244-(V244-V249)*(3.5/9.5)$	$V244-(V244-V250)*(3.5/13)$	$V244-(V244-V251)*(3.5/15)$	$V244-(V244-V252)*(3.5/17)$
V247	$V244-(V244-V249)*(5.5/9.5)$	$V244-(V244-V250)*(5.5/13)$	$V244-(V244-V251)*(5.5/15)$	$V244-(V244-V252)*(5.5/17)$
V248	$V244-(V244-V249)*(7.5/9.5)$	$V244-(V244-V250)*(7.5/13)$	$V244-(V244-V251)*(7.5/15)$	$V244-(V244-V252)*(7.5/17)$
V249	VINP10		$V244-(V244-V250)*(9.5/13)$	$V244-(V244-V251)*(9.5/15)$
V250	$V249-(V249-V254)*(3.5/12)$	VINP10	$V244-(V244-V251)*(13/15)$	$V244-(V244-V252)*(13/17)$
V251	$V249-(V249-V254)*(5.5/12)$	$V250-(V250-V254)*(2/8.5)$	VINP10	$V244-(V244-V252)*(15/17)$
V252	$V249-(V249-V254)*(7.5/12)$	$V250-(V250-V254)*(4/8.5)$	$V251-(V251-V254)*(2/6.5)$	VINP10
V253	$V249-(V249-V254)*(10/12)$	$V250-(V250-V254)*(6.5/8.5)$	$V251-(V251-V254)*(4.5/4.5)$	$V252-(V252-V254)*(2.5/4.5)$
V254	VINP11			
V255	VINP12			

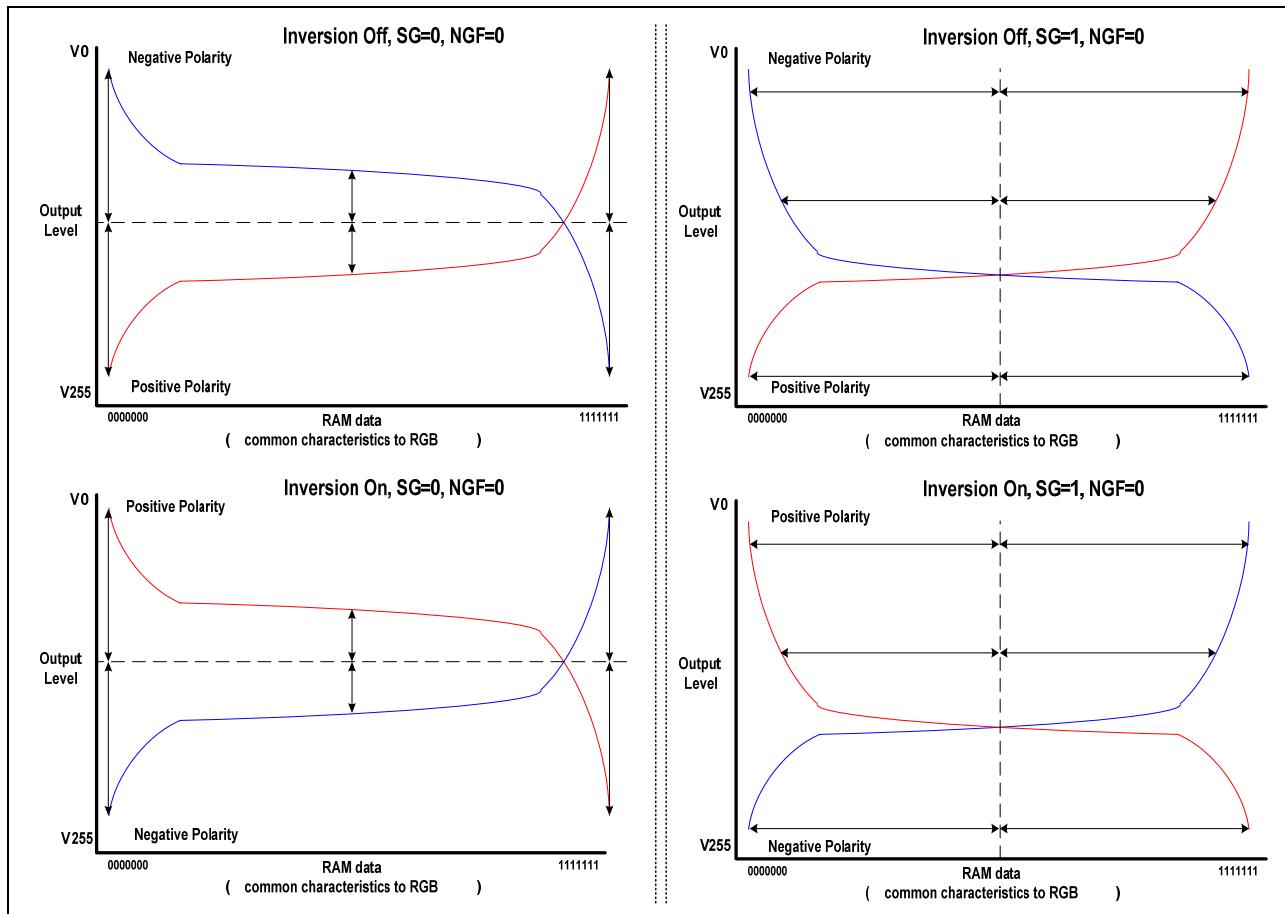


Figure 93. Relationship between RAM data and output voltage

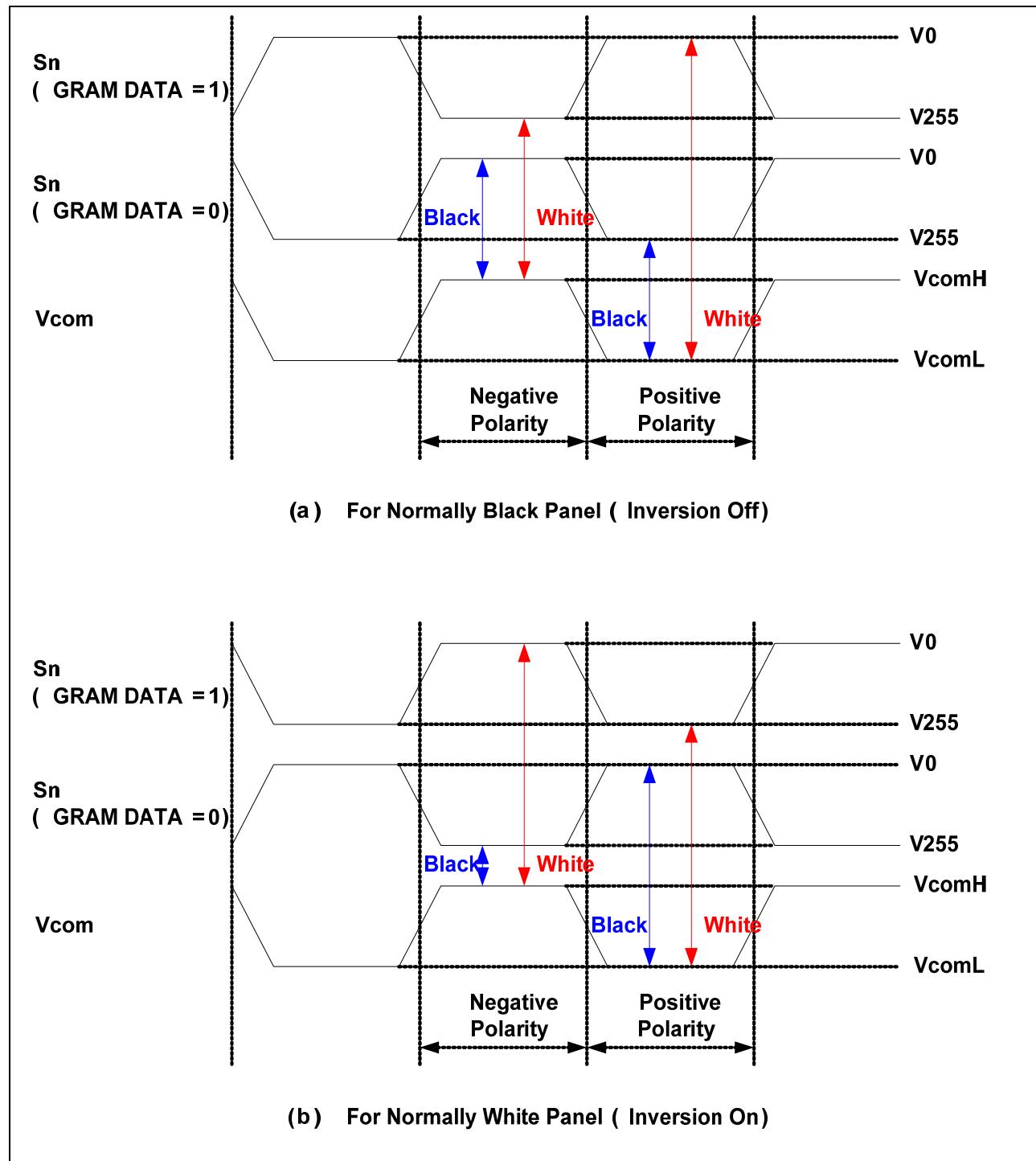


Figure 94. Relationship between source output and VCOM

## 4.3. PANEL CONTROL

### 4.3.1. Gate Driver

The gate driver block includes gate control outputs (G1 to G320) which should be connected directly to the TFT-LCD.

## 4.4. OSCILLATOR- SYSTEM CLOCK GENERATOR

S6D04M0 has an on-chip oscillator which does not require any external components. This oscillator output signal is used for the system clock generation for internal display operation.

### 4.4.1. Oscillator Circuit

The S6D04M0 can provide R-C oscillation. S6D04M0 internal oscillator does not need to attach the external resistor. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the oscillator frequency control register setting. Since R-C oscillation stops during the standby mode, power consumption can be reduced.

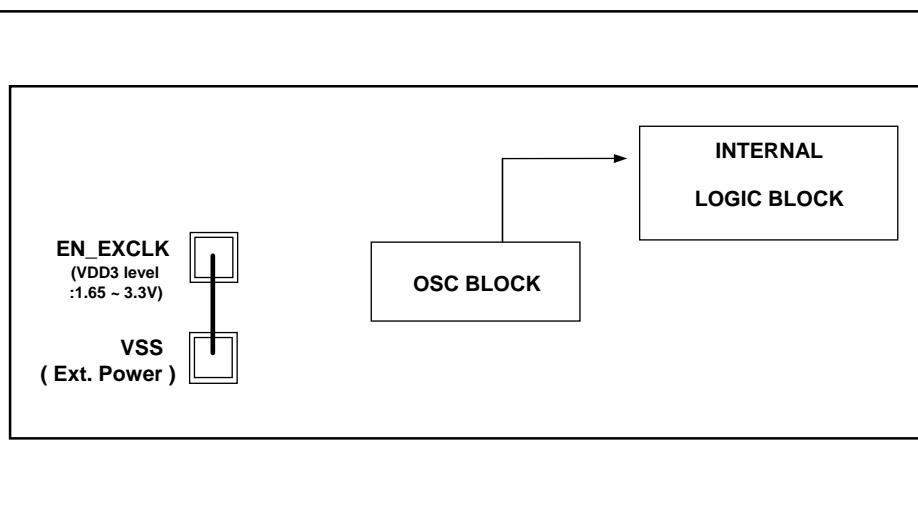


Figure 95. Application diagram for oscillator circuitry

#### 4.4.2. Frame Frequency Adjusting Function

The S6D04M0 has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting (RTN & CRTN) during the LCD driver operation as the oscillation frequency is always same. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching for an animated display is required, the frame frequency can be set high.

The relationship between the LCD driving duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the RTN (1H period adjusting bit) and CRTN (1 RTN period adjusting bit) .

$$\text{Frame Frequency} = \frac{f_{\text{osc}}}{\text{CRTN} \times \text{RTN} \times (\text{Line} + \text{B})} \quad [\text{Hz}]$$

$f_{\text{osc}}$  : R-C oscillation frequency (Fixed to 10MHz)  
 Line : Number of raster rows  
 RTN : Clock cycles per raster rows  
 CRTN : Clock cycles per 1 RTN Clock  
 B : Blank period ( Back porch + Front porch)

\* Note :  $(\text{RTN} \times \text{CRTN}) > 260$

**Figure 96. Formula for the frame frequency**

Calculation Example:

\* Display Condition

- Line: 320

- Frame frequency = 60 Hz

- B: Blank period (BP + FP): 16

If RTN[4:0] set to 10110(1H period: 22 clock), CRTN[4:0] set to 10110(1RTN period: 22 clock),

$10 \text{ MHz} / \{(22 \times 22) \times (320+16)\} = 61.5 \text{ [Hz]}$

The calculation result says that the required RTN, CRTN setting in the display condition listed above is 22. So the RTN and CRTN value should be selected to make 60Hz frame frequency is 22.

## 4.5. DISPLAY DATA RAM

### 4.5.1. Address Counter

The address counter sets the addresses of the display data RAM for writing and reading. Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 8-8-8-bit), according to the data formats. As soon as this pixel-data information is complete the “Write access” is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=239 (EFh) and Y=0 to Y=319 (13Fh). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined onto which it will be written. The window is programmable via the command registers SC, SP designating the start address and EC, EP designating the end address. For example, the whole display contents will be written, and the window will be defined by the following values: SC=0 (0h), SP=0 (0h) and EC=239 (EFh), EP=319 (13Fh).

In vertical addressing mode (D5=1), the Y-address increments after each byte. After the last Y-address (Y=EP), Y wraps around to SP and X increments to address the next column. In horizontal addressing mode (D5=0), the X-address increments after each byte. After the last X-address (X=EC), X wraps around to SC and Y increments to address the next page. After every last address (X=EC and Y=EP) the address pointers wrap around to address (X=SC and Y=SP). For flexibility in handling a wide variety of display architectures, the commands “CASET, PASET” and “MADCTL” (see section 5 command lists) define flags D6 and D7, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Following Figure shows the available combinations of writing to the display RAM. When D6, D7 and D5 will be changed the data must be rewritten to the display RAM.

For each image condition, the controls for the column and page counters apply as below:

**Table 88. Control for column and page counter**

Condition	Column counter	Page counter
When RAMWR/RAMRD command is accepted	Return to “start column(SC)”	Return to “start page(SP)”
Complete pixel read/write action	Increment by 1	No change
The column counter value is large than “End column (EC)”	Return to “start column(SC)”	Increment by 1
The page counter value is large than “End page (EP)”	Return to “start column(SC)”	Return to “start page(SP)”

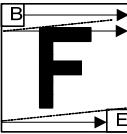
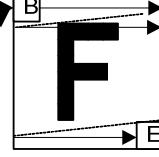
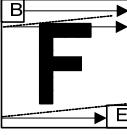
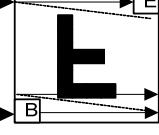
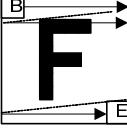
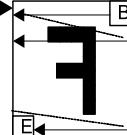
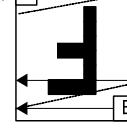
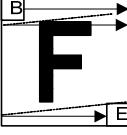
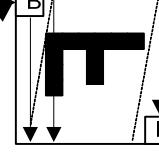
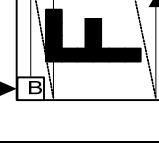
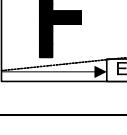
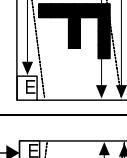
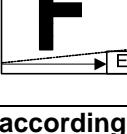
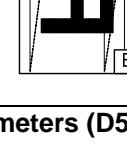
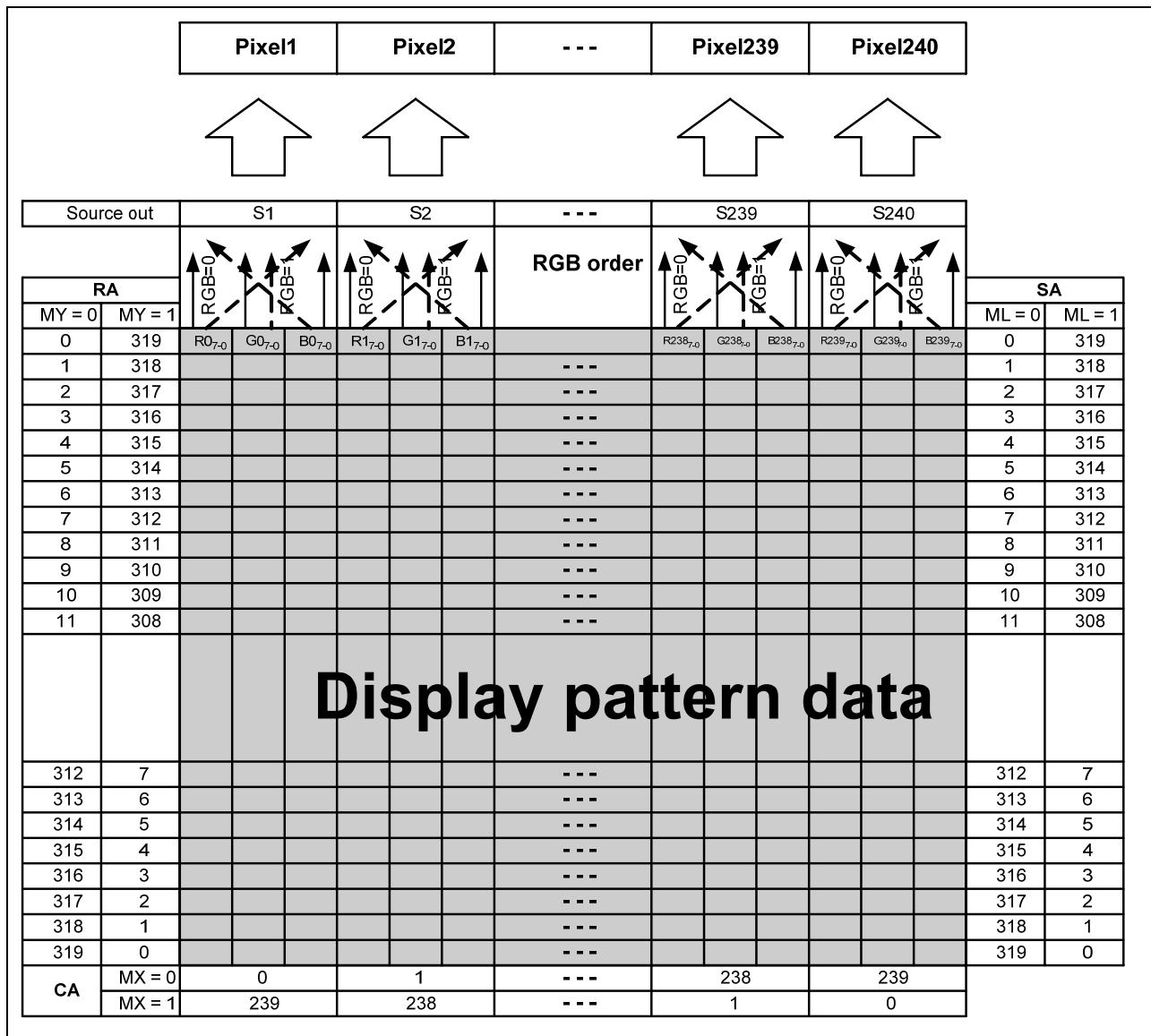
Display Data direction	MADCTL parameter			Image in the host(MCU)	Image in the driver (DDRAM)	
	D5	D6	D7			
Normal	0	0	0		H/W position(0,0) X-Y address(0,0) X : CASET, Y : RASET	
Y-mirror	0	0	1		H/W position(0,0) X-Y address(0,0) X : CASET, Y : RASET	
X-mirror	0	1	0		H/W position(0,0)	 X-Y address(0,0) X : CASET, Y : RASET
X-mirror Y-mirror	0	1	1		H/W position(0,0)	 X-Y address(0,0) X : CASET, Y : RASET
X-Y exchange	1	0	0		H/W position(0,0) X-Y address(0,0) X : CASET, Y : RASET	
X-Y exchange Y-mirror	1	0	1		H/W position(0,0) X-Y address(0,0) X : CASET, Y : RASET	
X-Y exchange X-mirror	1	1	0		H/W position(0,0)	 X-Y address(0,0) X : CASET, Y : RASET
X-Y exchange X-mirror Y-mirror	1	1	1		H/W position(0,0)	 X-Y address(0,0) X : CASET, Y : RASET

Figure 97. Frame data write direction according to the MADCTL parameters (D5, D6 and D7)

Note.D5, D6 and D7 are parameters of MADCTL command. D5(MV), D6(MX), D7(MY)

#### 4.5.2. Memory to Display Address Mapping

#### 4.5.2.1. When Using 240RGB x 320 Resolution (MX = MY = RGB = '0')



**Figure 98.** Memory to display address mapping

### Note.

RA = Row Address, (Page Address)

CA = Column Address,

SA = Scan Address,

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Page address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter. D4 parameter of MADCTL command

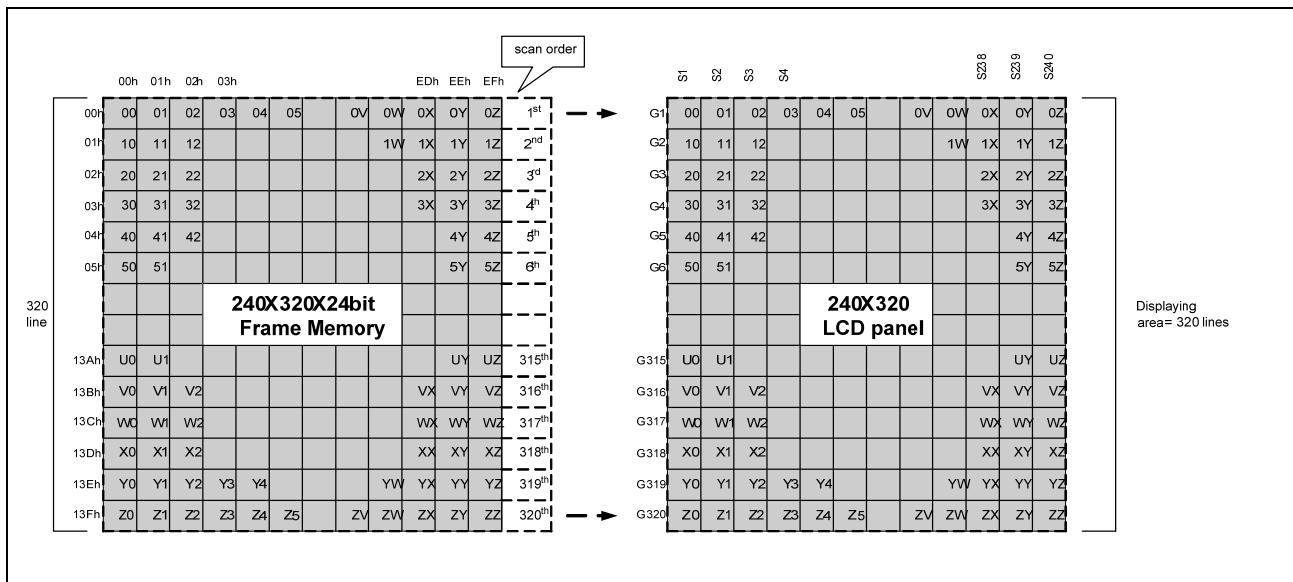
RGB= Red, Green and Blue pixel position change, D3 parameter of MADCTL command

#### 4.5.3. Normal Display On or Partial Mode On

##### 4.5.3.1. When Using 240RGB x 320 Resolution

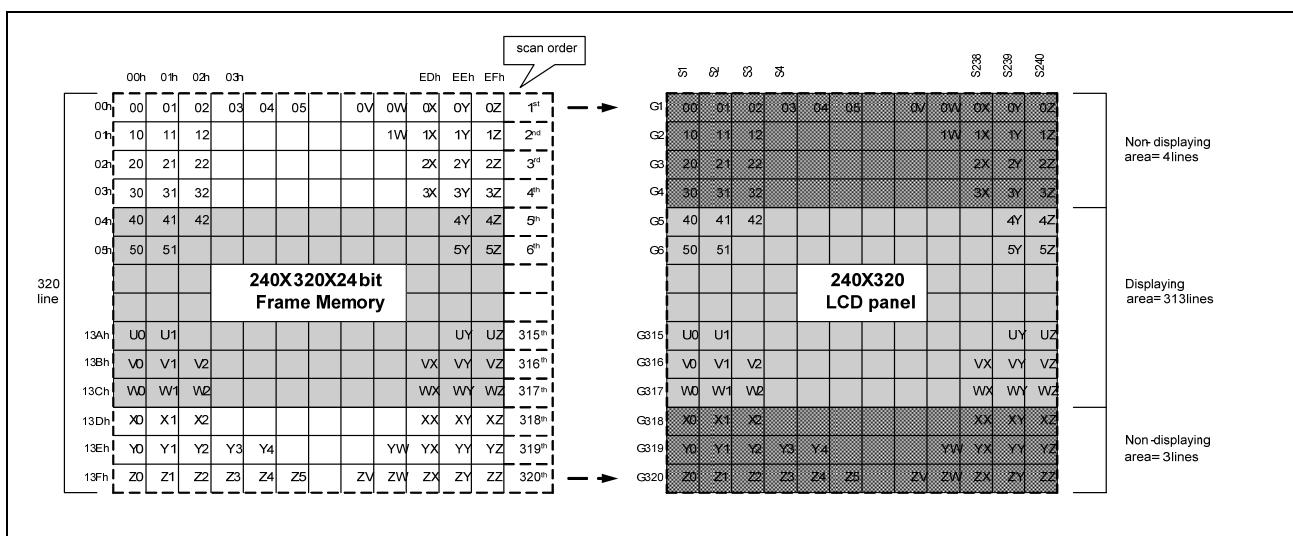
In this mode, the content of the frame memory within an area where column pointer is 00h to EFh and page pointer is 000h to 13Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0).

##### 1). Example for Normal Display On (D6 = D7 = D4 = '0', MX = MY = '0')



**Figure 99. Example for normal display on (D6 = D7 = D4 = '0', MX = MY = '0')**

##### 2). Partial Display On: SR [15:0] = 04h, ER [15:0] = 13Ch, MADCTL



**Figure 100. Partial display on: SR [15:0] = 04h, ER [15:0] = 13Ch, MADCTL**

#### 4.5.4. Command Definition is Independent of the IC Mount Position

Depending on how the MADCTL command is set, the top-bottom / left-right definitions are changed in the driver IC to adapt to the mounted form.

##### 4.5.4.1. Model of LCD Module for the S6D04M0

The LCD module for the S6D04M0 is shown below. The top-bottom / left-right positions, RGB filter and white/ black background defined in this development specification are in accordance with the diagram shown below.

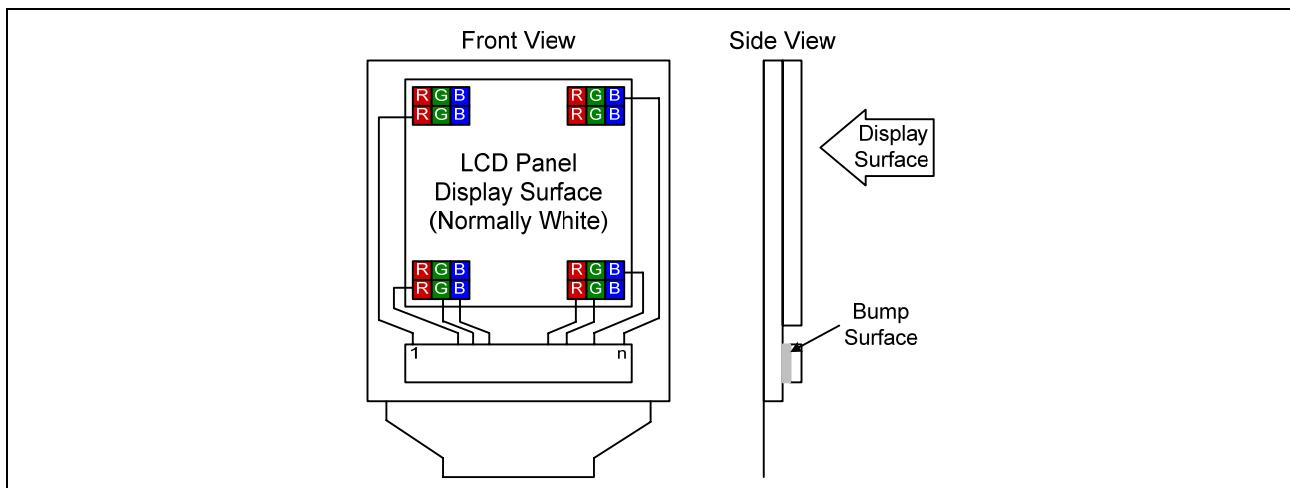


Figure 101. Model of LCD module for the S6D04M0

#### 4.5.4.2. Position Definition by IC Mount

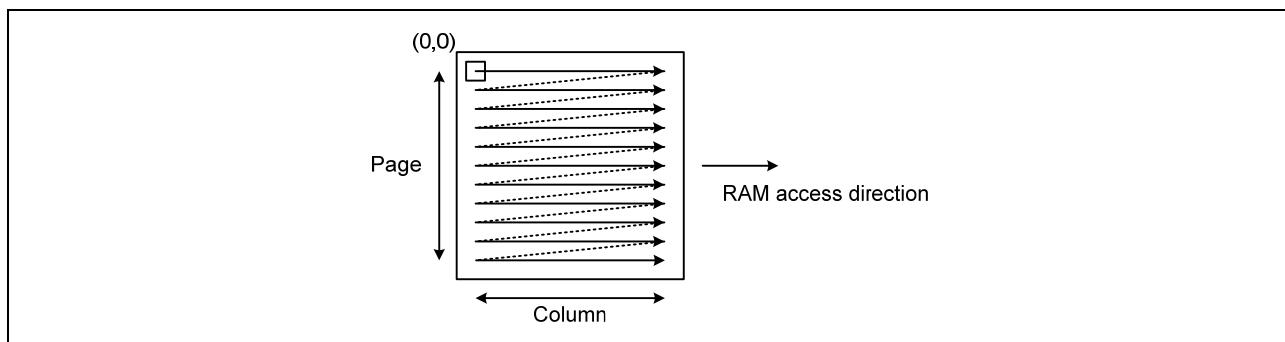
The set value of MADCTL actually used internally in the IC changes depending on how MADDEF is set. The arithmetic operation in the table below is performed on each bit. (The 'n' in the table means the nth bit.)

**Table 89. Arithmetic operation between MADCTL & MADDEF**

MADCTL(0Bh)	MADDEF(F6h)	IC Internal setting value
0	0	0
0	1	1
1	0	1
1	1	0

Note. MADDEF is F6h's 1<sup>st</sup> Parameter.

In the case of MADDEF set to "00h," the result of memory access is controlled as show below.



**Figure 102. An example of MADDEF(00h)**

Refer to the top-bottom / left-right relationship. (The non-bump plane is the surface.)

If the driver IC is left-mounted or right-mounted due to the device structure, the display data RAM to LCD display data readout and gate scan direction should be set left-right rather than top-bottom.

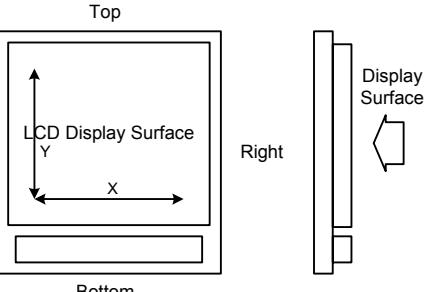
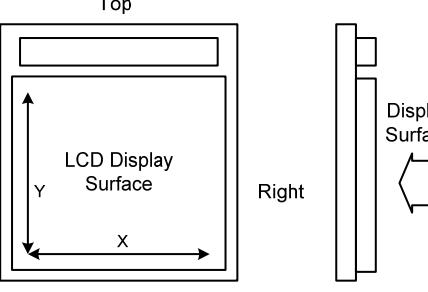
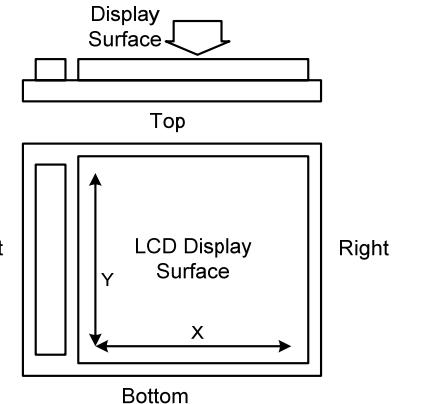
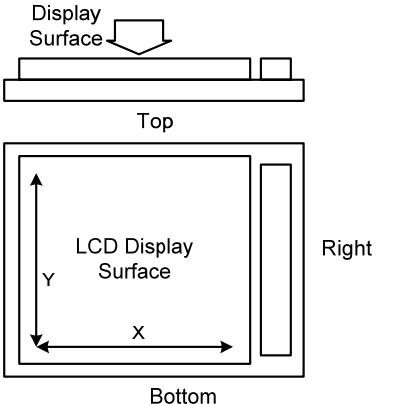
Case of bottom-mounted IC		Case of top-mounted IC	
Top		Top	
(Example) MADDEF(00h)		(Example) MADDEF(D0h)	
RAM address (0,0) Position	Left-top	RAM address (0,0) Position	Left-top
RAM Access Direction	Column Direction	RAM Access Direction	Column Direction
Column	X direction	Column	X direction
Page	Y direction	Page	Y direction
RAM→LCD readout direction	Top to Bottom	RAM→LCD readout direction	Top to Bottom
Gate line scan Direction	Top to Bottom	Gate line scan Direction	Top to Bottom
Case of left-mounted IC		Case of right-mounted IC	
Top		Top	
(Example) MADDEF(A0h)		(Example) MADDEF(60h)	
RAM address (0,0) Position	Left-top	RAM address (0,0) Position	Left-top
RAM Access Direction	Column Direction	RAM Access Direction	Column Direction
Column	X direction	Column	X direction
Page	Y direction	Page	Y direction
RAM→LCD readout direction	Right to Left	RAM→LCD readout direction	Left to Right
Gate line scan Direction	Right to Left	Gate line scan Direction	Left to Right

Figure 103. Cases of panel position mounted IC

## 4.5.4.3. 0-Address Position and RAM Access Scan Direction

Refer to MADCTL (MADDEF=00h)

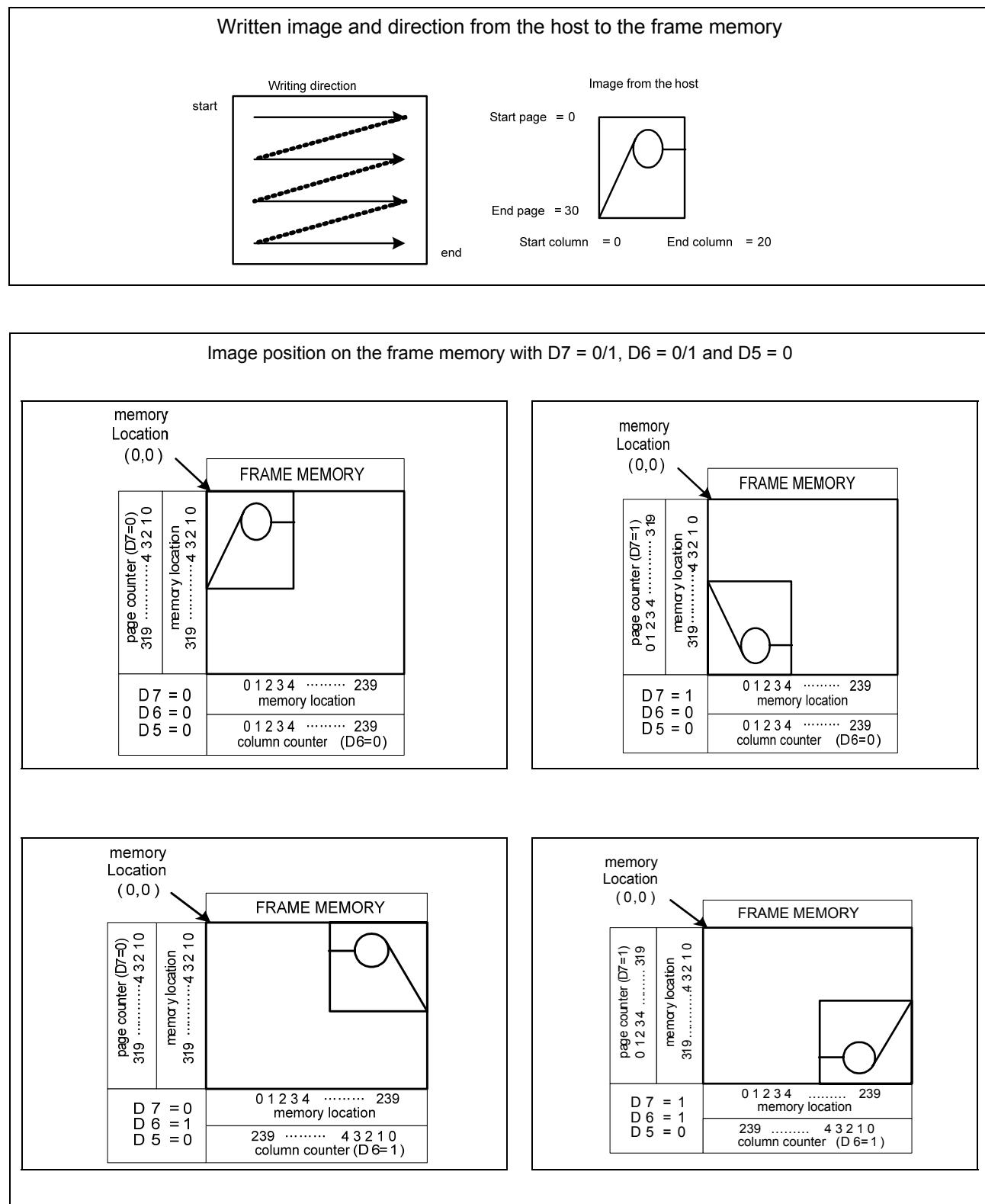


Figure 104. 0-Address position and RAM access scan direction(D5=0)

Written image and direction from the host to the frame memory

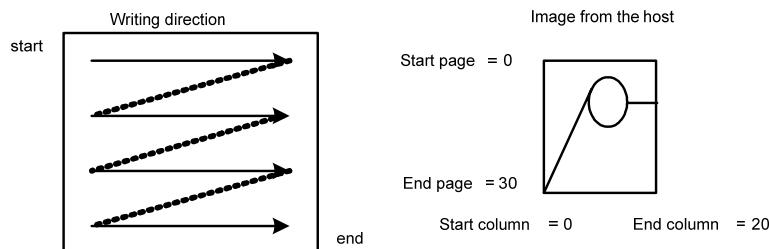


Image position on the frame memory with D7 = 0/1, D6 = 0/1 and D5 = 1

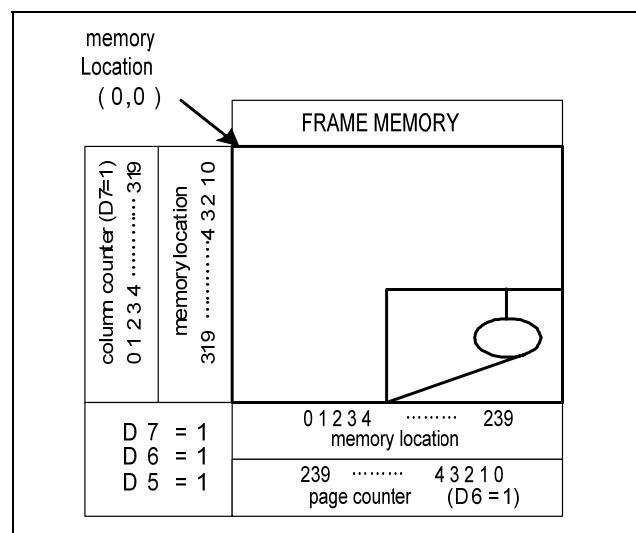
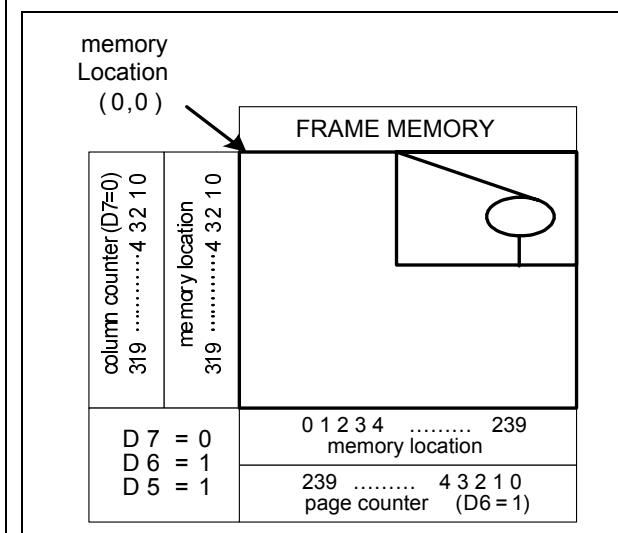
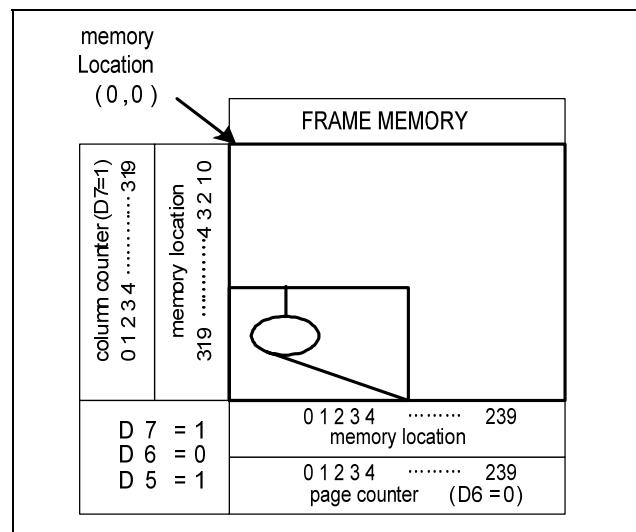
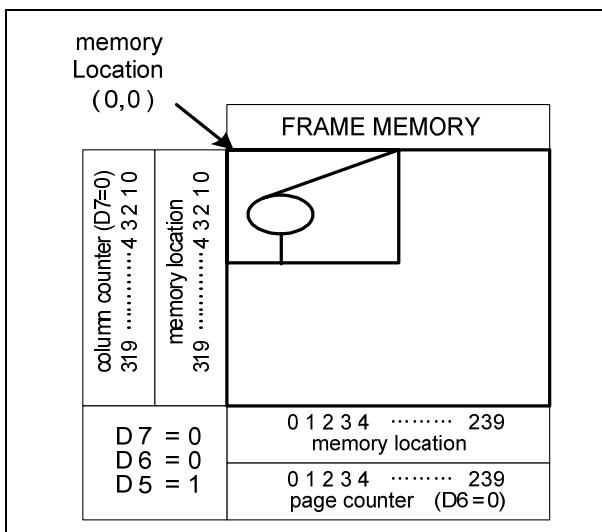


Figure 105. 0-Address position and RAM access scan direction(D5=1)

#### 4.5.4.4. LCD Read Scan Direction and Common Scan Direction

Refer to MADCTL ( MADDEF = 00h )

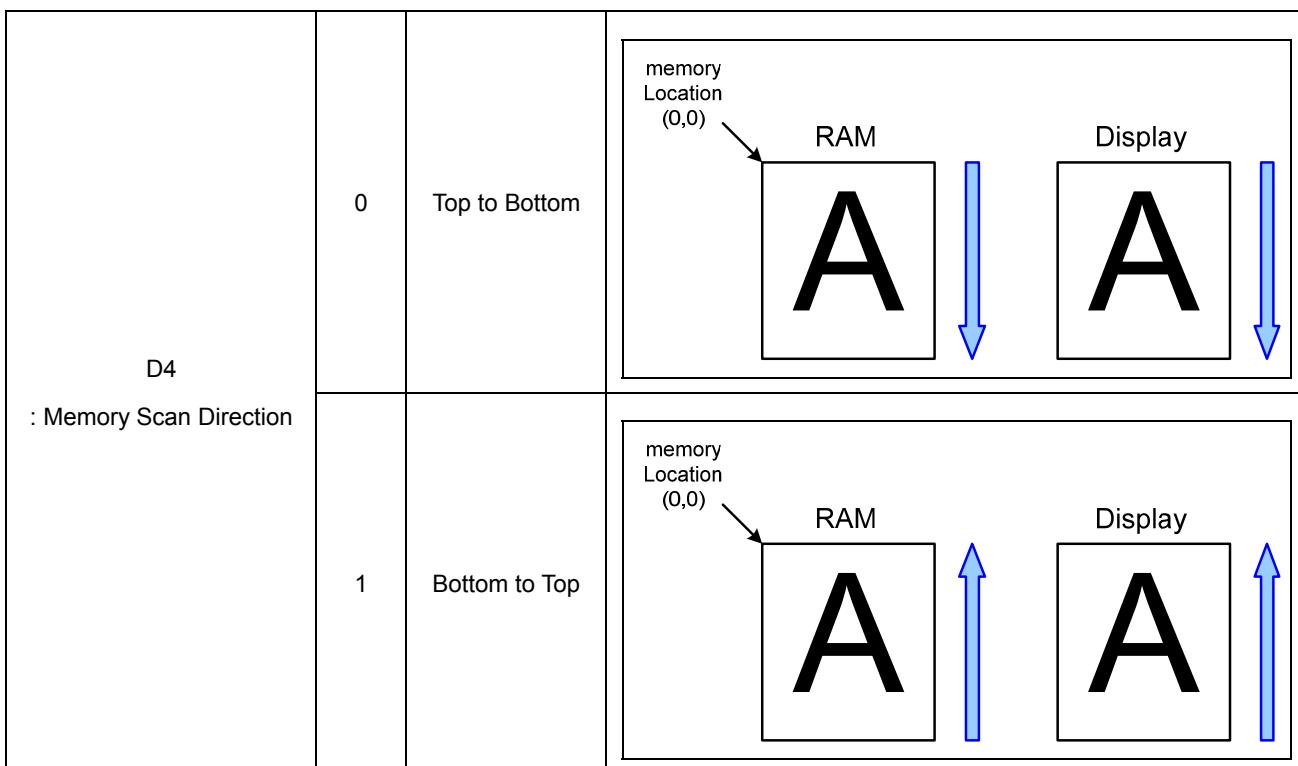


Figure 106. LCD read scan direction and common scan direction

#### 4.5.4.5. Partial Area and Scan Direction

Refer to MADCTL, PTLAR

##### A. Partial Mode

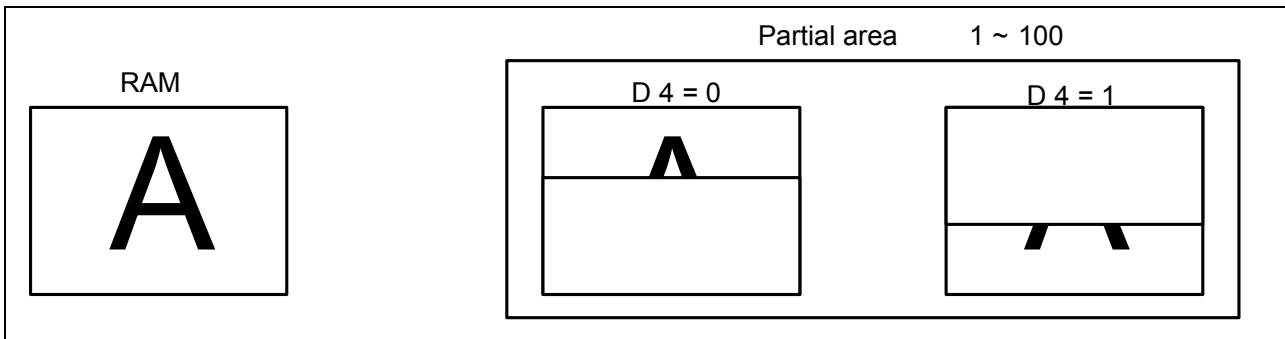


Figure 107. Partial area and scan direction

## 4.6. RESET

### 4.6.1. Registers

**Table 90. The default value of the register set**

Item	After Power On	After Hardware Reset	After Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Gamma setting	GC0	GC0	GC0
Column: Start Address (SC)	00_00h	00_00h	00_00h
Column: End Address (EC)	00_EFh	00_EFh	00EFh (239d) (when MADCTL's D5=0) 013Fh (319d) (when MADCTL's D5=1)
Page: Start Address (SP)	0000h	0000h	0000h
Page: End Address (EP)	01_3Fh (319d)	01_3Fh (319d)	013Fh (319d) (when MADCTL's D5=0) 00EFh (239d) (when MADCTL's D5=1)
RGB Color set (Look up Table)	Random	Random	No Change
Partial: Start Address (SR)	00_00h	00_00h	00_00h
Partial: End Address (ER)	01_3Fh	01_3Fh	01_3Fh
Color Pixel Fomat	24bit/pixel	24bit/pixel	No change
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode	00h (Mode1)	00h (Mode1)	00h (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB/MH)	0/0/0/0/0/0	0/0/0/0/0/0	No Change
RDDPM (0Ah)	08h	08h	08h
RDDMADCTL (0Bh)	00h	00h	No Change
RDDCOLMOD(0Ch)	24bit/pixel	24bit/pixel	No change
RDDIM (0Dh)	00h	00h	00h
RDDSM (0Eh)	00h	00h	00h
RDDSDR (0Fh)	00h	00h	00h
ID1 (DAh)	(MTP values)	(MTP values)	(MTP values)
ID2 (DBh)	(MTP values)	(MTP values)	(MTP values)
ID3 (DCh)	(MTP values)	(MTP values)	(MTP values)
WRDISBV(51h)	00h	00h	00h
RDDISBV(52h)	00h	00h	00h
WRCTRLD(53h)	00h	00h	00h
RDCTRLD(54h)	00h	00h	00h
WRCABC(55h)	00h	00h	00h
RDCABC(56h)	00h	00h	00h
WRCABCM(5Eh)	00h	00h	00h
RDCABCM(5Fh)	00h	00h	00h
MIECTL(CAh)	80_80_10h	80_80_10h	80_80_10h
BCMODE(CBh)	01h	01h	01h

Note1. There will be no abnormal visible effects on the display when S/W or H/W Reset is applied.

Note2. Powered-On Reset finishes within 10μs after both VDD3 & VCI are applied.

Note3. For detail information of TE Mode 1 , refer to the section 4.12



Table 91. The default value of the register set 1(level II)

Item	Default value ( After Hardware/Software Reset )			
	GC0	GC1	GC2	GC3
MIECTL2(CCh)	20_01_3F_00_EFh			
MIECTL3(CDh)		01_14h		
MTPCTL (D0h)		0C_05h		
WRVCMOC (D1h)		00h		
WRVMLOC (D2h)		00h		
WRGVDOC (D3h)		00h		
WRID (D4h)		00_00_00h		
RDOFFSETC (D5h)		MTP[30:16]		
D_CON(D9h)		00_00_00h		
WRPWD (F0h)		04_30h		
RDRWD (F1h)		04h		
DISCTL (F2h)		13_16_03_08_08_08_08_10_00_16_16h		
PWRCTL (F3h)		80_00_00_01_22_00_00_2Ch		
VCMCTL (F4h)		00_00_00_00_44h		
SRCCTL (F5h)		10_00_03_F0_40_1Fh		
IFCTL (F6h)		00_80_00_10h		
RPGAMCTL(F7h)	06h	06h	06h	46h
	03h	03h	03h	03h
	04h	03h	04h	03h
	0Ah	07h	0Bh	04h
	10h	0Eh	12h	0Ah
	1Ah	15h	1Eh	0Eh
	22h	1Bh	27h	13h
	2Ch	23h	32h	1Bh
	13h	1Dh	0Ch	26h
	12h	1Fh	09h	2Ah
	1Dh	2Fh	11h	3Fh
	11h	24h	09h	35h
	02h	0Ch	01h	17h
	22h	22h	22h	22h
	22h	22h	22h	22h
RNPGAMCTL(F8h)	06h	06h	06h	46h
	03h	03h	03h	03h
	04h	03h	04h	03h
	0Ah	07h	0Bh	04h
	10h	0Eh	12h	0Ah
	1Ah	15h	1Eh	0Eh
	22h	1Bh	27h	13h
	2Ch	23h	32h	1Bh
	13h	1Dh	0Ch	26h
	12h	1Fh	09h	2Ah
	1Dh	2Fh	11h	3Fh
	11h	24h	09h	35h
	02h	0Ch	01h	17h
	22h	22h	22h	22h
	22h	22h	22h	22h

Table 92. The default value of the register set 2 (level II)

Item	Default value ( After Hardware/Software Reset )			
	GC0	GC1	GC2	GC3
GPGAMCTL(F9h)	06h	06h	06h	46h
	03h	03h	03h	03h
	04h	03h	04h	03h
	0Ah	07h	0Bh	04h
	10h	0Eh	12h	0Ah
	1Ah	15h	1Eh	0Eh
	22h	1Bh	27h	13h
	2Ch	23h	32h	1Bh
	13h	1Dh	0Ch	26h
	12h	1Fh	09h	2Ah
	1Dh	2Fh	11h	3Fh
	11h	24h	09h	35h
	02h	0Ch	01h	17h
	22h	22h	22h	22h
	22h	22h	22h	22h
GNPGAMCTL(FAh)	06h	06h	06h	46h
	03h	03h	03h	03h
	04h	03h	04h	03h
	0Ah	07h	0Bh	04h
	10h	0Eh	12h	0Ah
	1Ah	15h	1Eh	0Eh
	22h	1Bh	27h	13h
	2Ch	23h	32h	1Bh
	13h	1Dh	0Ch	26h
	12h	1Fh	09h	2Ah
	1Dh	2Fh	11h	3Fh
	11h	24h	09h	35h
	02h	0Ch	01h	17h
	22h	22h	22h	22h
	22h	22h	22h	22h
BPGAMCTL(FBh)	06h	06h	06h	46h
	03h	03h	03h	03h
	04h	03h	04h	03h
	0Ah	07h	0Bh	04h
	10h	0Eh	12h	0Ah
	1Ah	15h	1Eh	0Eh
	22h	1Bh	27h	13h
	2Ch	23h	32h	1Bh
	13h	1Dh	0Ch	26h
	12h	1Fh	09h	2Ah
	1Dh	2Fh	11h	3Fh
	11h	24h	09h	35h
	02h	0Ch	01h	17h
	22h	22h	22h	22h
	22h	22h	22h	22h

Table 93. The default value of the register set 2 (level II)

Item	Default value ( After Hardware/Software Reset )			
	GC0	GC1	GC2	GC3
BNPGAMCTL(FCh)	06h	06h	06h	46h
	03h	03h	03h	03h
	04h	03h	04h	03h
	0Ah	07h	0Bh	04h
	10h	0Eh	12h	0Ah
	1Ah	15h	1Eh	0Eh
	22h	1Bh	27h	13h
	2Ch	23h	32h	1Bh
	13h	1Dh	0Ch	26h
	12h	1Fh	09h	2Ah
	1Dh	2Fh	11h	3Fh
	11h	24h	09h	35h
	02h	0Ch	01h	17h
	22h	22h	22h	22h
	22h	22h	22h	22h
GATECTL(FDh)	11h			
EDSTEST(FFh)	00_00_00_00_00h			

#### 4.6.2. Module input/output/Bi-direction (I/O) Pads

##### 4.6.2.1. Output or Bi-directional (I/O) Pads

**Table 94. Reset states of output pads**

Output or Bi-directional pads	When RESX is Low	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low	Low
BC	Low	Low	Low	Low
BC_CTL	High	High	High	High
DB23 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
SDA (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Note. There will be no output from DB23-DB0 during Power On/Off sequence, Hardware Reset and Software Reset

##### 4.6.2.2. Input Pads

**Table 95. Reset states of input pads**

Input pads	During Power On Process	After Power On	When RESX is Low	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See Section 4.1.1	Input valid	-	Input valid	Input valid	See Section 4.1.1
CSX	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input invalid
DCX	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input invalid
DB23 to DB0 (Input driver)	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input invalid
SDA (Input driver)	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input valid (RGB IF & DM=1) Input invalid (The other cases)
VSYNC	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input valid



						(RGB IF & DM=1or VSM = 1) Input invalid (The other cases)
DOTCLK	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input valid (RGB IF & DM=1) Input invalid (The other cases)
ENABLE	Input invalid	Input valid	Input invalid	Input valid	Input valid	Input invalid

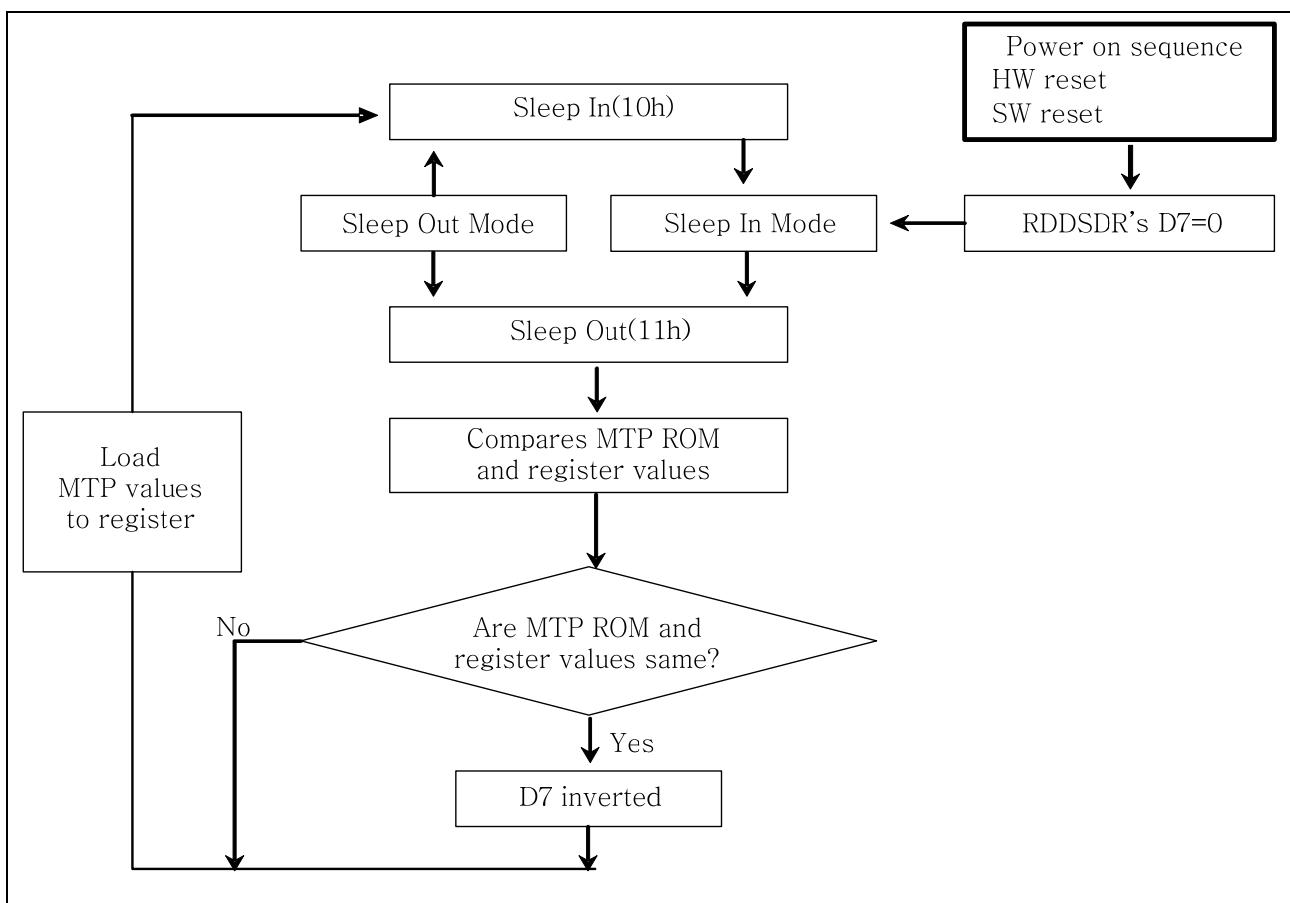
## 4.7. SLEEP OUT –COMMAND AND SELF-DIAGNOSTIC FUNCTIONS OF THE DISPLAY MODULE

### 4.7.1. Register Loading Detection

Sleep-out command is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from MTP (or similar device) to registers of the display controller is working properly.

Data of the MTP and register values of driver IC are compared as shown in the figure below. If those both values (MTP and register values) are the same, there is an inverted (=increased by 1) bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If both those values are not same, this bit (D7) is not inverted (= not increased by 1).

The flowchart of the function described above is as follows.



**Figure 108. Flowchart of register loading detection**

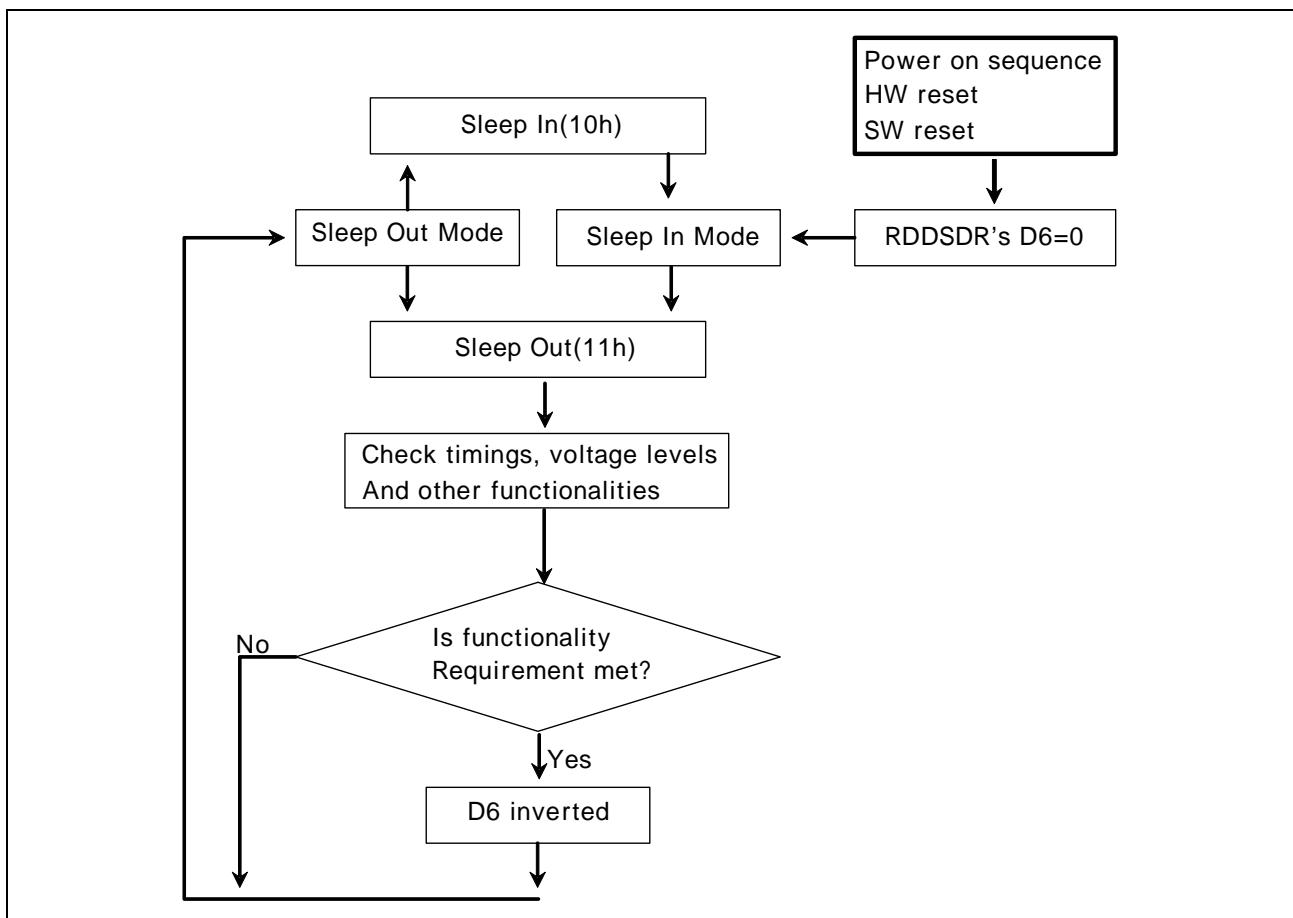
Note. There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DDh), by the display module.

#### 4.7.2. Functionality Detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= not increased by 1).

The flow chart for this internal function is following:



**Figure 109. Flowchart of functionality detection**

Note: There is needed 120msec after Sleep Out –command, when there is changing from Sleep In –mode to Sleep Out –mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out –mode.

## 4.8. MTP CONTROL

### 4.8.1. Multiple-Time Programmable (MTP) ROM Control

#### 4.8.1.1. MTP Control Flow

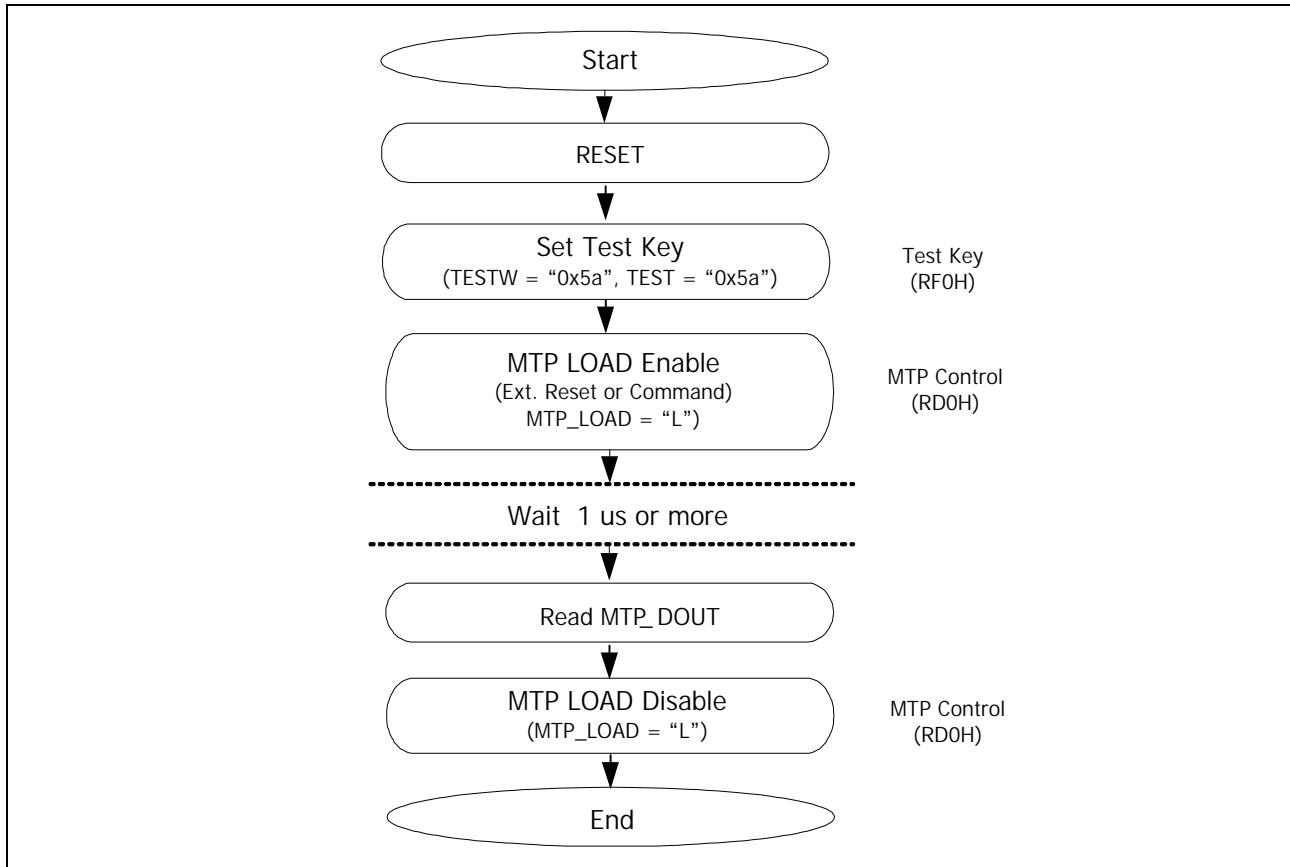


Figure 110. Flow of MTP load / read

## 4.8.1.2. Internal Control

## a. Using VCI for MTP

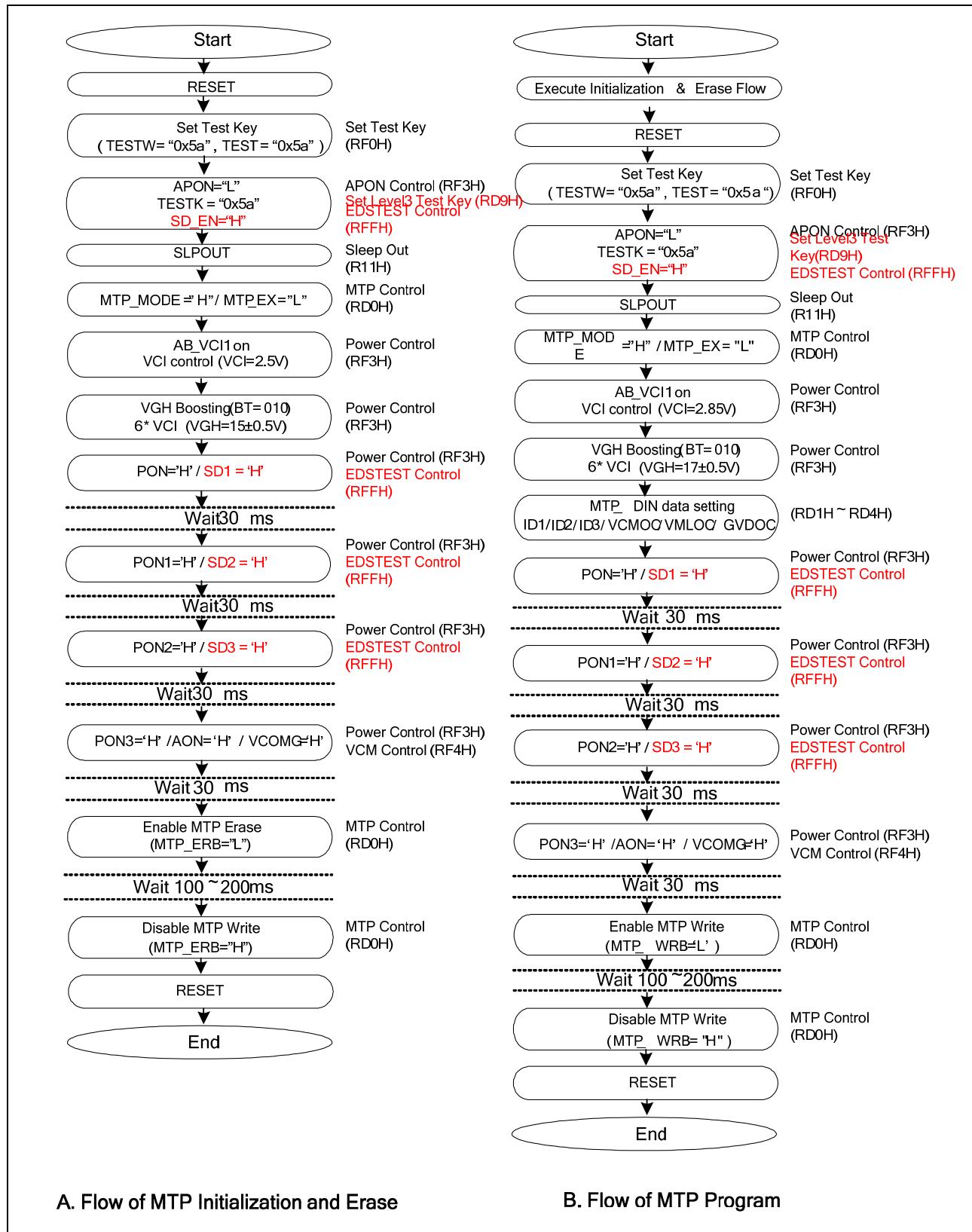


Figure 111. MTP initialization, erase and program (internal mode using VCI)

b. Using VCI1 for MTP

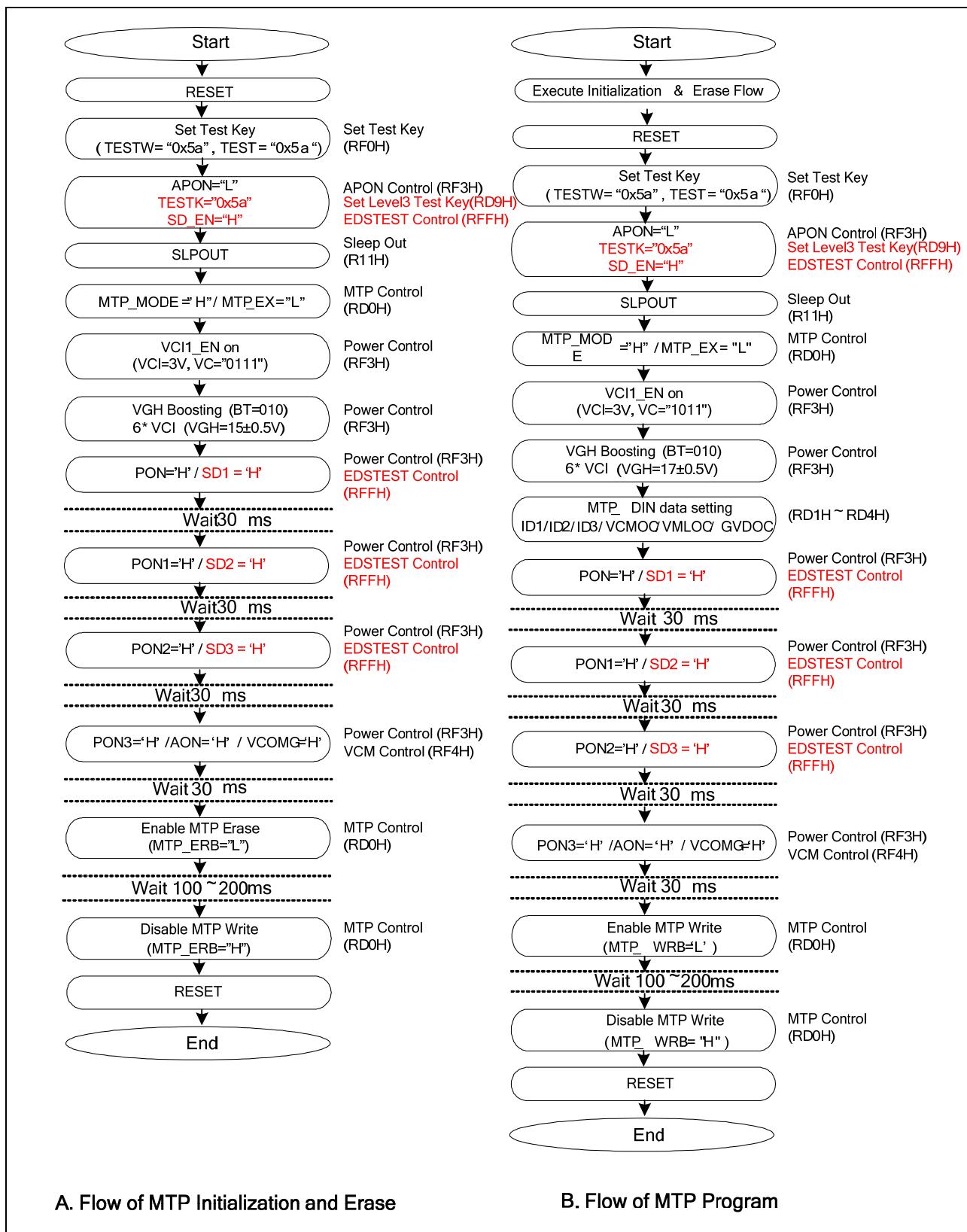


Figure 112. MTP initialization, erase and program (internal mode using VCI1)

## 4.8.1.3. External Control

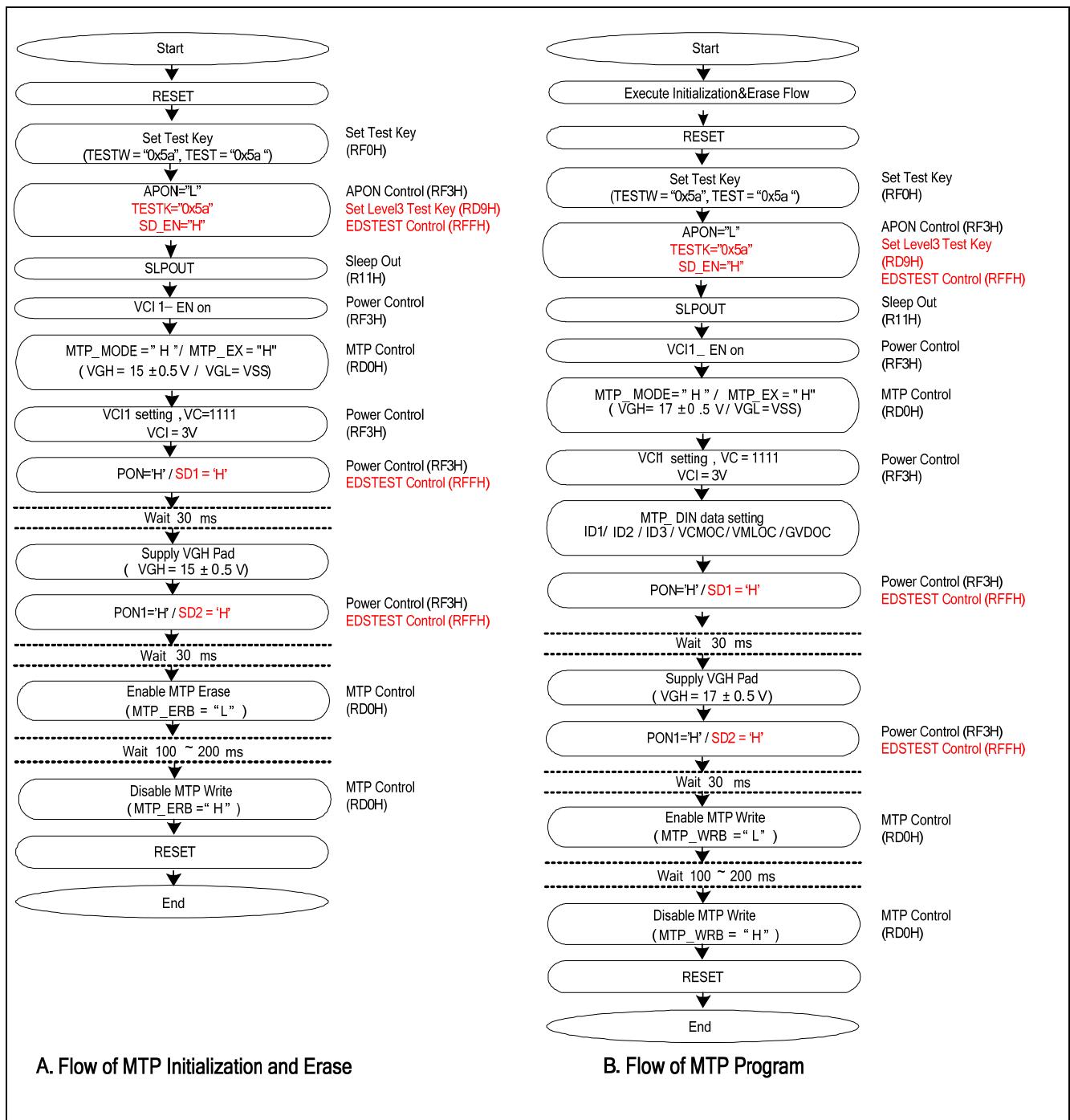


Figure 113. MTP initialization, erase and program (external mode)

#### 4.8.1.4. Timing of MTP Control

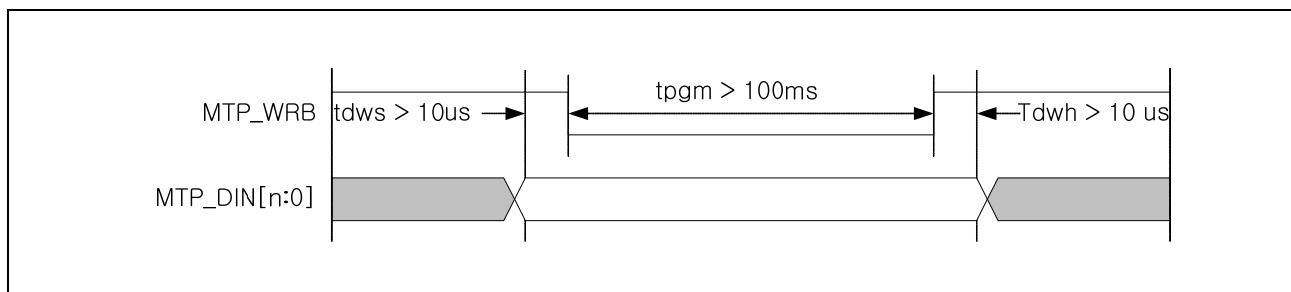


Figure 114. Timing of MTP program

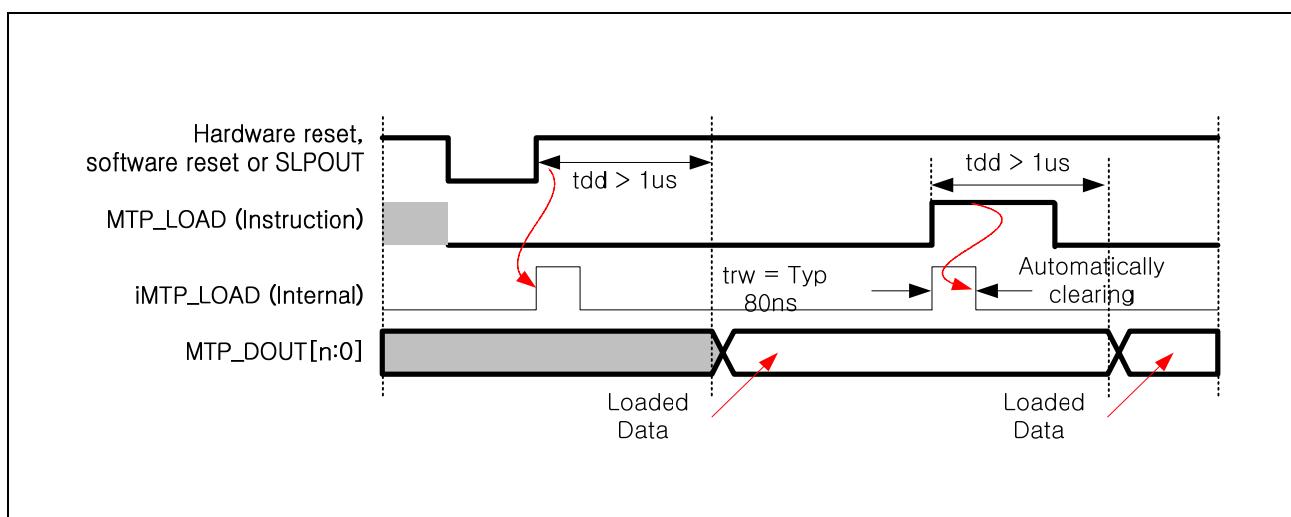


Figure 115. Timing of MTP load

Note :

1. The shipping value (=initialized value) of MTP ROM : All "0".
2. The maximum number of re-writable times of MTP ROM : 20 times.

#### 4.9. 8-COLOR DISPLAY MODE

An 8-color display mode is also provided by the S6D04M0. In an 8-color mode of operation, gray scale voltage generation (V0-V255) is halted to conserve power and the values of gamma micro-adjustment registers (PKP and PKN) become invalid. Also, the only MSB of each R, G, and B in the Frame Memory are displayed. (Refer to 39h Command)

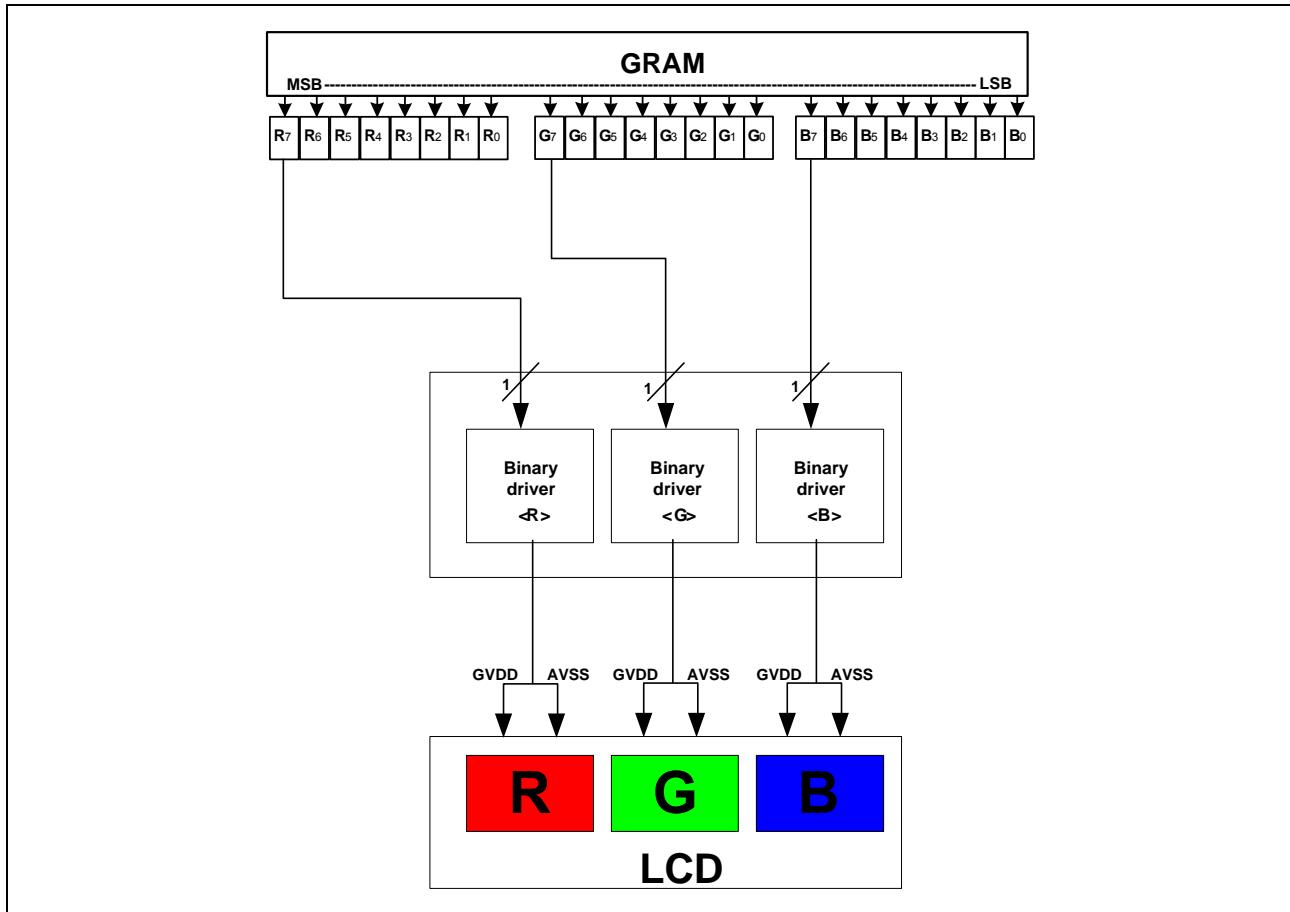


Figure 116. 8-color display control.

## 4.10. INSTRUCTION SETUP FLOW

### 4.10.1. Initializing the Built-In Power Supply Circuits

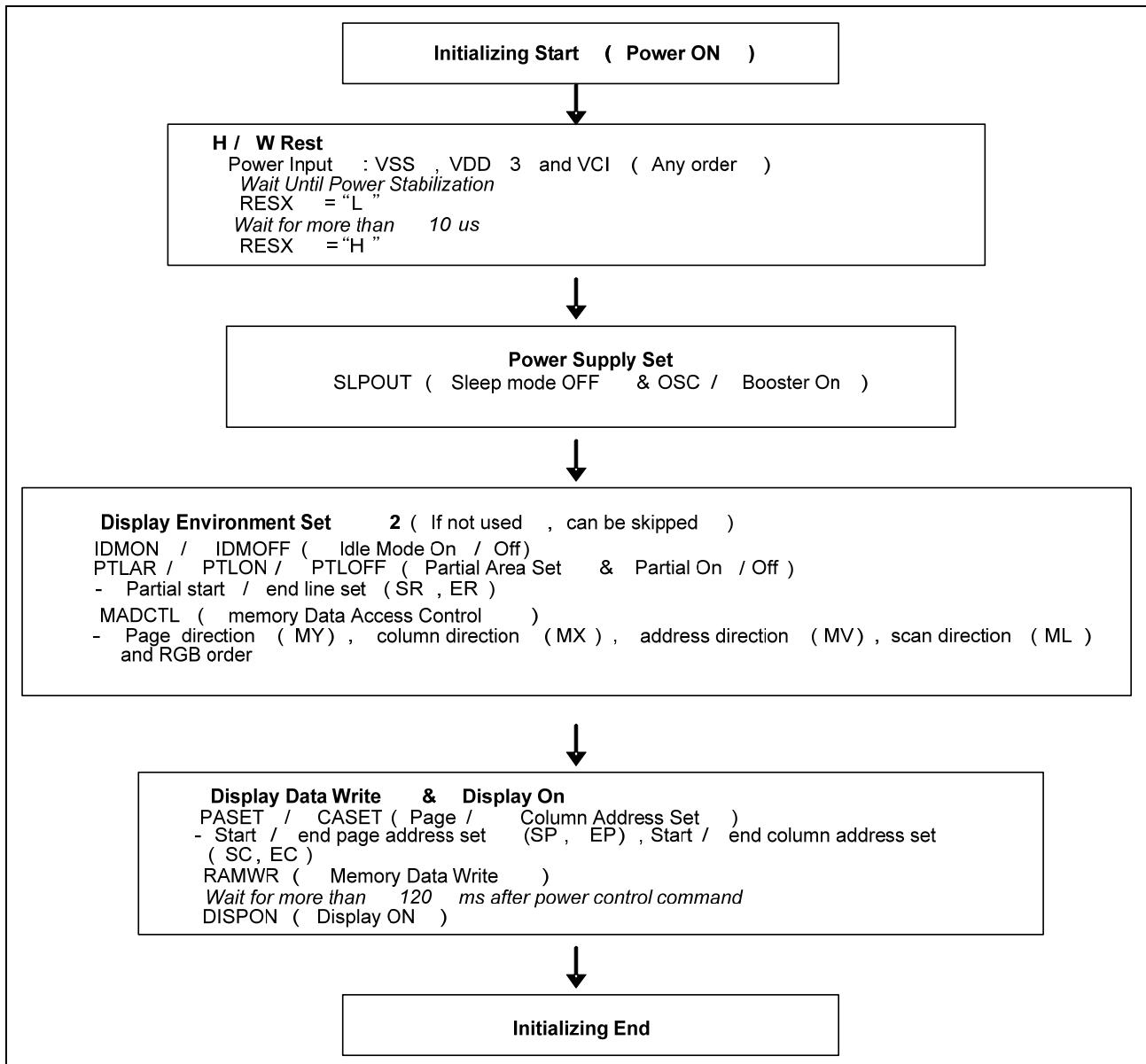


Figure 117. Initializing the built-in power supply circuits

The initializing sequence does not have any effect on the display. The display is in its normal background color during the initialization.

#### 4.10.2. Power OFF Sequence

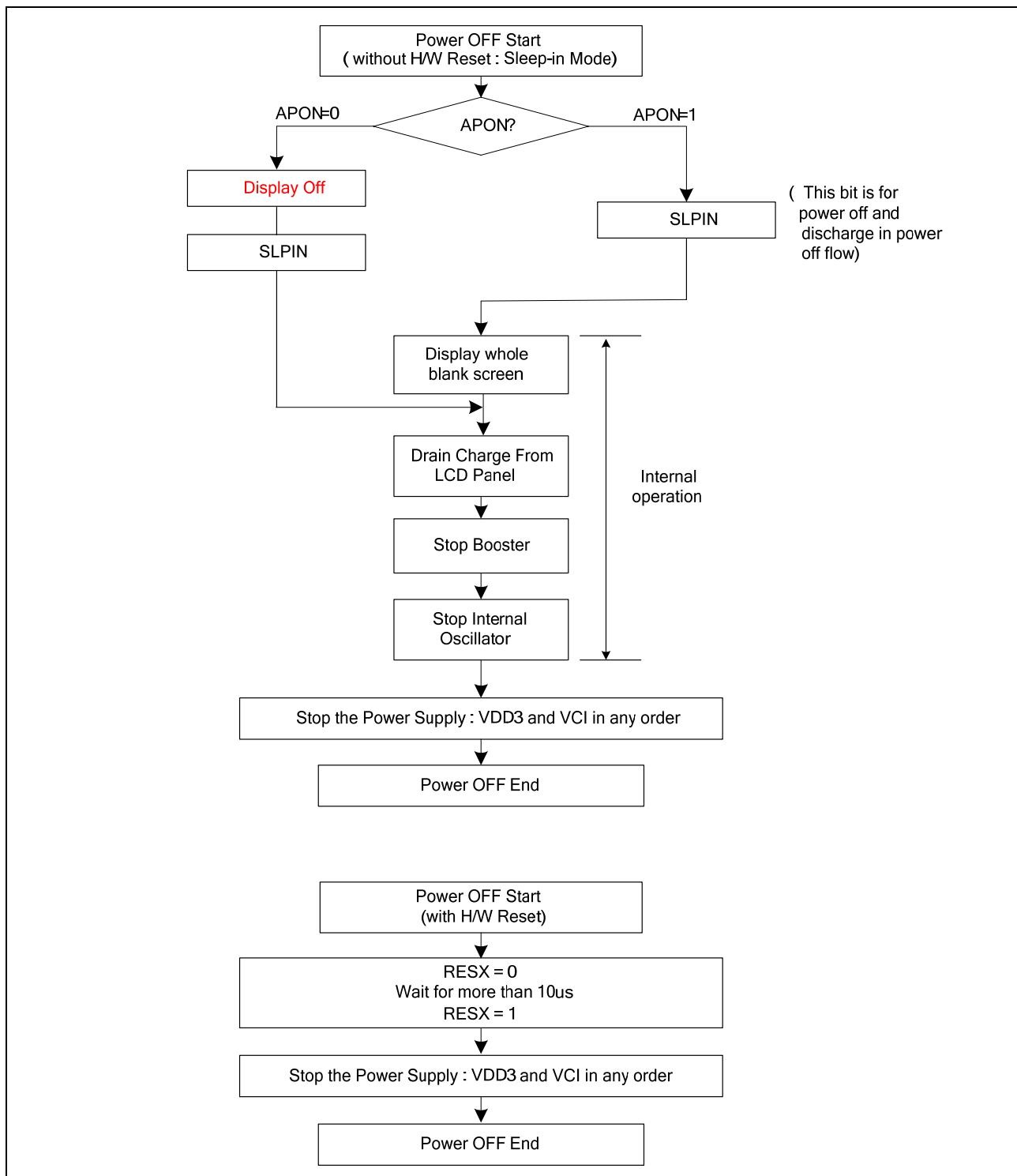


Figure 118. Power off sequence

#### 4.11. COLOUR DEPTH CONVERSION LOOK UP TABLE.

In normal mode, display data don't use Look up table blow. For using Look up table to expand data bit, CM register must be high. (Defalt value of CM register is low. Refer to section 3.2.1)

The number of parameter is decided by Interface Pixel Format (3Ah).Refer to section 5.2.21 RGBSET.

**Table 96. Look up table (Red) 1**

16 bit/pixel - mode 65,536 colours		18 bit/pixel -mode 262,144 colours		R output (8bit) 24 bit/pixel -mode 16,777,216 colours
R input (5 bit)	RGBSET parameter	R input (6 bit)	RGBSET parameter	
00000	1	000000	1	R <sub>007</sub> R <sub>006</sub> R <sub>005</sub> R <sub>004</sub> R <sub>003</sub> R <sub>002</sub> R <sub>001</sub> R <sub>000</sub>
00001	2	000001	2	R <sub>017</sub> R <sub>016</sub> R <sub>015</sub> R <sub>014</sub> R <sub>013</sub> R <sub>012</sub> R <sub>011</sub> R <sub>010</sub>
00010	3	000010	3	R <sub>027</sub> R <sub>026</sub> R <sub>025</sub> R <sub>024</sub> R <sub>023</sub> R <sub>022</sub> R <sub>021</sub> R <sub>020</sub>
00011	4	000011	4	R <sub>037</sub> R <sub>036</sub> R <sub>035</sub> R <sub>034</sub> R <sub>033</sub> R <sub>032</sub> R <sub>031</sub> R <sub>030</sub>
00100	5	000100	5	R <sub>047</sub> R <sub>046</sub> R <sub>045</sub> R <sub>044</sub> R <sub>043</sub> R <sub>042</sub> R <sub>041</sub> R <sub>040</sub>
00101	6	000101	6	R <sub>057</sub> R <sub>056</sub> R <sub>055</sub> R <sub>054</sub> R <sub>053</sub> R <sub>052</sub> R <sub>051</sub> R <sub>050</sub>
00110	7	000110	7	R <sub>067</sub> R <sub>066</sub> R <sub>065</sub> R <sub>064</sub> R <sub>063</sub> R <sub>062</sub> R <sub>061</sub> R <sub>060</sub>
00111	8	000111	8	R <sub>077</sub> R <sub>076</sub> R <sub>075</sub> R <sub>074</sub> R <sub>073</sub> R <sub>072</sub> R <sub>071</sub> R <sub>070</sub>
01000	9	001000	9	R <sub>087</sub> R <sub>086</sub> R <sub>085</sub> R <sub>084</sub> R <sub>083</sub> R <sub>082</sub> R <sub>081</sub> R <sub>080</sub>
01001	10	001001	10	R <sub>097</sub> R <sub>096</sub> R <sub>095</sub> R <sub>094</sub> R <sub>093</sub> R <sub>092</sub> R <sub>091</sub> R <sub>090</sub>
01010	11	001010	11	R <sub>107</sub> R <sub>106</sub> R <sub>105</sub> R <sub>104</sub> R <sub>103</sub> R <sub>102</sub> R <sub>101</sub> R <sub>100</sub>
01011	12	001011	12	R <sub>117</sub> R <sub>116</sub> R <sub>115</sub> R <sub>114</sub> R <sub>113</sub> R <sub>112</sub> R <sub>011</sub> R <sub>110</sub>
01100	13	001100	13	R <sub>127</sub> R <sub>126</sub> R <sub>125</sub> R <sub>124</sub> R <sub>123</sub> R <sub>122</sub> R <sub>121</sub> R <sub>120</sub>
01101	14	001101	14	R <sub>137</sub> R <sub>136</sub> R <sub>135</sub> R <sub>134</sub> R <sub>133</sub> R <sub>132</sub> R <sub>131</sub> R <sub>130</sub>
01110	15	001110	15	R <sub>147</sub> R <sub>146</sub> R <sub>145</sub> R <sub>144</sub> R <sub>143</sub> R <sub>142</sub> R <sub>141</sub> R <sub>140</sub>
01111	16	001111	16	R <sub>157</sub> R <sub>156</sub> R <sub>155</sub> R <sub>154</sub> R <sub>153</sub> R <sub>152</sub> R <sub>151</sub> R <sub>150</sub>
10000	17	010000	17	R <sub>167</sub> R <sub>166</sub> R <sub>165</sub> R <sub>164</sub> R <sub>163</sub> R <sub>162</sub> R <sub>161</sub> R <sub>160</sub>
10001	18	010001	18	R <sub>177</sub> R <sub>176</sub> R <sub>175</sub> R <sub>174</sub> R <sub>173</sub> R <sub>172</sub> R <sub>171</sub> R <sub>170</sub>
10010	19	010010	19	R <sub>187</sub> R <sub>186</sub> R <sub>185</sub> R <sub>184</sub> R <sub>183</sub> R <sub>182</sub> R <sub>181</sub> R <sub>180</sub>
10011	20	010011	20	R <sub>197</sub> R <sub>196</sub> R <sub>195</sub> R <sub>194</sub> R <sub>193</sub> R <sub>192</sub> R <sub>191</sub> R <sub>190</sub>
10100	21	010100	21	R <sub>207</sub> R <sub>206</sub> R <sub>205</sub> R <sub>204</sub> R <sub>203</sub> R <sub>202</sub> R <sub>201</sub> R <sub>200</sub>
10101	22	010101	22	R <sub>217</sub> R <sub>216</sub> R <sub>215</sub> R <sub>214</sub> R <sub>213</sub> R <sub>212</sub> R <sub>211</sub> R <sub>210</sub>
10110	23	010110	23	R <sub>227</sub> R <sub>226</sub> R <sub>225</sub> R <sub>224</sub> R <sub>223</sub> R <sub>222</sub> R <sub>221</sub> R <sub>220</sub>
10111	24	010111	24	R <sub>237</sub> R <sub>236</sub> R <sub>235</sub> R <sub>234</sub> R <sub>233</sub> R <sub>232</sub> R <sub>231</sub> R <sub>230</sub>
11000	25	011000	25	R <sub>247</sub> R <sub>246</sub> R <sub>245</sub> R <sub>244</sub> R <sub>243</sub> R <sub>242</sub> R <sub>241</sub> R <sub>240</sub>
11001	26	011001	26	R <sub>257</sub> R <sub>256</sub> R <sub>255</sub> R <sub>254</sub> R <sub>253</sub> R <sub>252</sub> R <sub>251</sub> R <sub>250</sub>
11010	27	011010	27	R <sub>267</sub> R <sub>266</sub> R <sub>265</sub> R <sub>264</sub> R <sub>263</sub> R <sub>262</sub> R <sub>261</sub> R <sub>260</sub>
11011	28	011011	28	R <sub>277</sub> R <sub>276</sub> R <sub>275</sub> R <sub>274</sub> R <sub>273</sub> R <sub>272</sub> R <sub>271</sub> R <sub>270</sub>
11100	29	011100	29	R <sub>287</sub> R <sub>286</sub> R <sub>285</sub> R <sub>284</sub> R <sub>283</sub> R <sub>282</sub> R <sub>281</sub> R <sub>280</sub>
11101	30	011101	30	R <sub>297</sub> R <sub>296</sub> R <sub>295</sub> R <sub>294</sub> R <sub>293</sub> R <sub>292</sub> R <sub>291</sub> R <sub>290</sub>
11110	31	011110	31	R <sub>307</sub> R <sub>306</sub> R <sub>305</sub> R <sub>304</sub> R <sub>303</sub> R <sub>302</sub> R <sub>301</sub> R <sub>300</sub>
11111	32	011111	32	R <sub>317</sub> R <sub>316</sub> R <sub>315</sub> R <sub>314</sub> R <sub>313</sub> R <sub>312</sub> R <sub>311</sub> R <sub>310</sub>

Table 97. Look up table (Red) 2

16 bit/pixel - mode 65,536 colours		18 bit/pixel -mode 262,144 colours		R output (8bit) 24 bit/pixel -mode 16,777,216 colours
R input (5 bit)	RGBSET parameter	R input (6 bit)	RGBSET parameter	
No Input	-	100000	33	R <sub>327</sub> R <sub>326</sub> R <sub>325</sub> R <sub>324</sub> R <sub>323</sub> R <sub>322</sub> R <sub>321</sub> R <sub>320</sub>
No Input	-	100001	34	R <sub>337</sub> R <sub>336</sub> R <sub>335</sub> R <sub>334</sub> R <sub>333</sub> R <sub>332</sub> R <sub>331</sub> R <sub>330</sub>
No Input	-	100010	35	R <sub>347</sub> R <sub>346</sub> R <sub>345</sub> R <sub>344</sub> R <sub>343</sub> R <sub>342</sub> R <sub>341</sub> R <sub>340</sub>
No Input	-	100011	36	R <sub>357</sub> R <sub>356</sub> R <sub>355</sub> R <sub>354</sub> R <sub>353</sub> R <sub>352</sub> R <sub>351</sub> R <sub>350</sub>
No Input	-	100100	37	R <sub>367</sub> R <sub>366</sub> R <sub>365</sub> R <sub>364</sub> R <sub>363</sub> R <sub>362</sub> R <sub>361</sub> R <sub>360</sub>
No Input	-	100101	38	R <sub>377</sub> R <sub>376</sub> R <sub>375</sub> R <sub>374</sub> R <sub>373</sub> R <sub>372</sub> R <sub>371</sub> R <sub>370</sub>
No Input	-	100110	39	R <sub>387</sub> R <sub>386</sub> R <sub>385</sub> R <sub>384</sub> R <sub>383</sub> R <sub>382</sub> R <sub>381</sub> R <sub>380</sub>
No Input	-	100111	40	R <sub>397</sub> R <sub>396</sub> R <sub>395</sub> R <sub>394</sub> R <sub>393</sub> R <sub>392</sub> R <sub>391</sub> R <sub>390</sub>
No Input	-	101000	41	R <sub>407</sub> R <sub>406</sub> R <sub>405</sub> R <sub>404</sub> R <sub>403</sub> R <sub>402</sub> R <sub>401</sub> R <sub>400</sub>
No Input	-	101001	42	R <sub>417</sub> R <sub>416</sub> R <sub>415</sub> R <sub>414</sub> R <sub>413</sub> R <sub>412</sub> R <sub>411</sub> R <sub>410</sub>
No Input	-	101010	43	R <sub>427</sub> R <sub>426</sub> R <sub>425</sub> R <sub>424</sub> R <sub>423</sub> R <sub>422</sub> R <sub>421</sub> R <sub>420</sub>
No Input	-	101011	44	R <sub>437</sub> R <sub>436</sub> R <sub>435</sub> R <sub>434</sub> R <sub>433</sub> R <sub>432</sub> R <sub>431</sub> R <sub>430</sub>
No Input	-	101100	45	R <sub>447</sub> R <sub>446</sub> R <sub>445</sub> R <sub>444</sub> R <sub>443</sub> R <sub>442</sub> R <sub>441</sub> R <sub>440</sub>
No Input	-	101101	46	R <sub>457</sub> R <sub>456</sub> R <sub>455</sub> R <sub>454</sub> R <sub>453</sub> R <sub>452</sub> R <sub>451</sub> R <sub>450</sub>
No Input	-	101110	47	R <sub>467</sub> R <sub>466</sub> R <sub>465</sub> R <sub>464</sub> R <sub>463</sub> R <sub>462</sub> R <sub>461</sub> R <sub>460</sub>
No Input	-	101111	48	R <sub>477</sub> R <sub>476</sub> R <sub>475</sub> R <sub>474</sub> R <sub>473</sub> R <sub>472</sub> R <sub>471</sub> R <sub>470</sub>
No Input	-	110000	49	R <sub>487</sub> R <sub>486</sub> R <sub>485</sub> R <sub>484</sub> R <sub>483</sub> R <sub>482</sub> R <sub>481</sub> R <sub>480</sub>
No Input	-	110001	50	R <sub>497</sub> R <sub>496</sub> R <sub>495</sub> R <sub>494</sub> R <sub>493</sub> R <sub>492</sub> R <sub>491</sub> R <sub>490</sub>
No Input	-	110010	51	R <sub>507</sub> R <sub>506</sub> R <sub>505</sub> R <sub>504</sub> R <sub>503</sub> R <sub>502</sub> R <sub>501</sub> R <sub>500</sub>
No Input	-	110011	52	R <sub>517</sub> R <sub>516</sub> R <sub>515</sub> R <sub>514</sub> R <sub>513</sub> R <sub>512</sub> R <sub>511</sub> R <sub>510</sub>
No Input	-	110100	53	R <sub>527</sub> R <sub>526</sub> R <sub>525</sub> R <sub>524</sub> R <sub>523</sub> R <sub>522</sub> R <sub>521</sub> R <sub>520</sub>
No Input	-	110101	54	R <sub>537</sub> R <sub>536</sub> R <sub>535</sub> R <sub>534</sub> R <sub>533</sub> R <sub>532</sub> R <sub>531</sub> R <sub>530</sub>
No Input	-	110110	55	R <sub>547</sub> R <sub>546</sub> R <sub>545</sub> R <sub>544</sub> R <sub>543</sub> R <sub>542</sub> R <sub>541</sub> R <sub>540</sub>
No Input	-	110111	56	R <sub>557</sub> R <sub>556</sub> R <sub>555</sub> R <sub>554</sub> R <sub>553</sub> R <sub>552</sub> R <sub>551</sub> R <sub>550</sub>
No Input	-	111000	57	R <sub>567</sub> R <sub>566</sub> R <sub>565</sub> R <sub>564</sub> R <sub>563</sub> R <sub>562</sub> R <sub>561</sub> R <sub>560</sub>
No Input	-	111001	58	R <sub>577</sub> R <sub>576</sub> R <sub>575</sub> R <sub>574</sub> R <sub>573</sub> R <sub>572</sub> R <sub>571</sub> R <sub>570</sub>
No Input	-	111010	59	R <sub>587</sub> R <sub>586</sub> R <sub>585</sub> R <sub>584</sub> R <sub>583</sub> R <sub>582</sub> R <sub>581</sub> R <sub>580</sub>
No Input	-	111011	60	R <sub>597</sub> R <sub>596</sub> R <sub>595</sub> R <sub>594</sub> R <sub>593</sub> R <sub>592</sub> R <sub>591</sub> R <sub>590</sub>
No Input	-	111100	61	R <sub>607</sub> R <sub>606</sub> R <sub>605</sub> R <sub>604</sub> R <sub>603</sub> R <sub>602</sub> R <sub>601</sub> R <sub>600</sub>
No Input	-	111101	62	R <sub>617</sub> R <sub>616</sub> R <sub>615</sub> R <sub>614</sub> R <sub>613</sub> R <sub>612</sub> R <sub>611</sub> R <sub>610</sub>
No Input	-	111110	63	R <sub>627</sub> R <sub>626</sub> R <sub>625</sub> R <sub>624</sub> R <sub>623</sub> R <sub>622</sub> R <sub>621</sub> R <sub>620</sub>
No Input	-	111111	64	R <sub>637</sub> R <sub>636</sub> R <sub>635</sub> R <sub>634</sub> R <sub>633</sub> R <sub>632</sub> R <sub>631</sub> R <sub>630</sub>

Table 98. Look up table (Green) 1

16 bit/pixel - mode 65,536 colours		18 bit/pixel -mode 262,144 colours		G output (8bit) 24 bit/pixel -mode 16,777,216 colours
G input (6 bit)	RGBSET parameter	G input (6 bit)	RGBSET parameter	
000000	33	000000	65	G <sub>007</sub> G <sub>006</sub> G <sub>005</sub> G <sub>004</sub> G <sub>003</sub> G <sub>002</sub> G <sub>001</sub> G <sub>000</sub>
000001	34	000001	66	G <sub>017</sub> G <sub>016</sub> G <sub>015</sub> G <sub>014</sub> G <sub>013</sub> G <sub>012</sub> G <sub>011</sub> G <sub>010</sub>
000010	35	000010	67	G <sub>027</sub> G <sub>026</sub> G <sub>025</sub> G <sub>024</sub> G <sub>023</sub> G <sub>022</sub> G <sub>021</sub> G <sub>020</sub>
000011	36	000011	68	G <sub>037</sub> G <sub>036</sub> G <sub>035</sub> G <sub>034</sub> G <sub>033</sub> G <sub>032</sub> G <sub>031</sub> G <sub>030</sub>
000100	37	000100	69	G <sub>047</sub> G <sub>046</sub> G <sub>045</sub> G <sub>044</sub> G <sub>043</sub> G <sub>042</sub> G <sub>041</sub> G <sub>040</sub>
000101	38	000101	70	G <sub>057</sub> G <sub>056</sub> G <sub>055</sub> G <sub>054</sub> G <sub>053</sub> G <sub>052</sub> G <sub>051</sub> G <sub>050</sub>
000110	39	000110	71	G <sub>067</sub> G <sub>066</sub> G <sub>065</sub> G <sub>064</sub> G <sub>063</sub> G <sub>062</sub> G <sub>061</sub> G <sub>060</sub>
000111	40	000111	72	G <sub>077</sub> G <sub>076</sub> G <sub>075</sub> G <sub>074</sub> G <sub>073</sub> G <sub>072</sub> G <sub>071</sub> G <sub>070</sub>
001000	41	001000	73	G <sub>087</sub> G <sub>086</sub> G <sub>085</sub> G <sub>084</sub> G <sub>083</sub> G <sub>082</sub> G <sub>081</sub> G <sub>080</sub>
001001	42	001001	74	G <sub>097</sub> G <sub>096</sub> G <sub>095</sub> G <sub>094</sub> G <sub>093</sub> G <sub>092</sub> G <sub>091</sub> G <sub>090</sub>
001010	43	001010	75	G <sub>107</sub> G <sub>106</sub> G <sub>105</sub> G <sub>104</sub> G <sub>103</sub> G <sub>102</sub> G <sub>101</sub> G <sub>100</sub>
001011	44	001011	76	G <sub>117</sub> G <sub>116</sub> G <sub>115</sub> G <sub>114</sub> G <sub>113</sub> G <sub>112</sub> G <sub>011</sub> G <sub>110</sub>
001100	45	001100	77	G <sub>127</sub> G <sub>126</sub> G <sub>125</sub> G <sub>124</sub> G <sub>123</sub> G <sub>122</sub> G <sub>121</sub> G <sub>120</sub>
001101	46	001101	78	G <sub>137</sub> G <sub>136</sub> G <sub>135</sub> G <sub>134</sub> G <sub>133</sub> G <sub>132</sub> G <sub>131</sub> G <sub>130</sub>
001110	47	001110	79	G <sub>147</sub> G <sub>146</sub> G <sub>145</sub> G <sub>144</sub> G <sub>143</sub> G <sub>142</sub> G <sub>141</sub> G <sub>140</sub>
001111	48	001111	80	G <sub>157</sub> G <sub>156</sub> G <sub>155</sub> G <sub>154</sub> G <sub>153</sub> G <sub>152</sub> G <sub>151</sub> G <sub>150</sub>
010000	49	010000	81	G <sub>167</sub> G <sub>166</sub> G <sub>165</sub> G <sub>164</sub> G <sub>163</sub> G <sub>162</sub> G <sub>161</sub> G <sub>160</sub>
010001	50	010001	82	G <sub>177</sub> G <sub>176</sub> G <sub>175</sub> G <sub>174</sub> G <sub>173</sub> G <sub>172</sub> G <sub>171</sub> G <sub>170</sub>
010010	51	010010	83	G <sub>187</sub> G <sub>186</sub> G <sub>185</sub> G <sub>184</sub> G <sub>183</sub> G <sub>182</sub> G <sub>181</sub> G <sub>180</sub>
010011	52	010011	84	G <sub>197</sub> G <sub>196</sub> G <sub>195</sub> G <sub>194</sub> G <sub>193</sub> G <sub>192</sub> G <sub>191</sub> G <sub>190</sub>
010100	53	010100	85	G <sub>207</sub> G <sub>206</sub> G <sub>205</sub> G <sub>204</sub> G <sub>203</sub> G <sub>202</sub> G <sub>201</sub> G <sub>200</sub>
010101	54	010101	86	G <sub>217</sub> G <sub>216</sub> G <sub>215</sub> G <sub>214</sub> G <sub>213</sub> G <sub>212</sub> G <sub>211</sub> G <sub>210</sub>
010110	55	010110	87	G <sub>227</sub> G <sub>226</sub> G <sub>225</sub> G <sub>224</sub> G <sub>223</sub> G <sub>222</sub> G <sub>221</sub> G <sub>220</sub>
010111	56	010111	88	G <sub>237</sub> G <sub>236</sub> G <sub>235</sub> G <sub>234</sub> G <sub>233</sub> G <sub>232</sub> G <sub>231</sub> G <sub>230</sub>
011000	57	011000	89	G <sub>247</sub> G <sub>246</sub> G <sub>245</sub> G <sub>244</sub> G <sub>243</sub> G <sub>242</sub> G <sub>241</sub> G <sub>240</sub>
011001	58	011001	90	G <sub>257</sub> G <sub>256</sub> G <sub>255</sub> G <sub>254</sub> G <sub>253</sub> G <sub>252</sub> G <sub>251</sub> G <sub>250</sub>
011010	59	011010	91	G <sub>267</sub> G <sub>266</sub> G <sub>265</sub> G <sub>264</sub> G <sub>263</sub> G <sub>262</sub> G <sub>261</sub> G <sub>260</sub>
011011	60	011011	92	G <sub>277</sub> G <sub>276</sub> G <sub>275</sub> G <sub>274</sub> G <sub>273</sub> G <sub>272</sub> G <sub>271</sub> G <sub>270</sub>
011100	61	011100	93	G <sub>287</sub> G <sub>286</sub> G <sub>285</sub> G <sub>284</sub> G <sub>283</sub> G <sub>282</sub> G <sub>281</sub> G <sub>280</sub>
011101	62	011101	94	G <sub>297</sub> G <sub>296</sub> G <sub>295</sub> G <sub>294</sub> G <sub>293</sub> G <sub>292</sub> G <sub>291</sub> G <sub>290</sub>
011110	63	011110	95	G <sub>307</sub> G <sub>306</sub> G <sub>305</sub> G <sub>304</sub> G <sub>303</sub> G <sub>302</sub> G <sub>301</sub> G <sub>300</sub>
011111	64	011111	96	G <sub>317</sub> G <sub>316</sub> G <sub>315</sub> G <sub>314</sub> G <sub>313</sub> G <sub>312</sub> G <sub>311</sub> G <sub>310</sub>



Table 99. Look up Table (Green) 2

16 bit/pixel - mode 65,536 colours		18 bit/pixel -mode 262,144 colours		G output (8bit) 24 bit/pixel -mode 16,777,216 colours
G input (6 bit)	RGBSET parameter	G input (6 bit)	RGBSET parameter	
100000	65	100000	97	G <sub>327</sub> G <sub>326</sub> G <sub>325</sub> G <sub>324</sub> G <sub>323</sub> G <sub>322</sub> G <sub>321</sub> G <sub>320</sub>
100001	66	100001	98	G <sub>337</sub> G <sub>336</sub> G <sub>335</sub> G <sub>334</sub> G <sub>333</sub> G <sub>332</sub> G <sub>331</sub> G <sub>330</sub>
100010	67	100010	99	G <sub>347</sub> G <sub>346</sub> G <sub>345</sub> G <sub>344</sub> G <sub>343</sub> G <sub>342</sub> G <sub>341</sub> G <sub>340</sub>
100011	68	100011	100	G <sub>357</sub> G <sub>356</sub> G <sub>355</sub> G <sub>354</sub> G <sub>353</sub> G <sub>352</sub> G <sub>351</sub> G <sub>350</sub>
100100	69	100100	101	G <sub>367</sub> G <sub>366</sub> G <sub>365</sub> G <sub>364</sub> G <sub>363</sub> G <sub>362</sub> G <sub>361</sub> G <sub>360</sub>
100101	70	100101	102	G <sub>377</sub> G <sub>376</sub> G <sub>375</sub> G <sub>374</sub> G <sub>373</sub> G <sub>372</sub> G <sub>371</sub> G <sub>370</sub>
100110	71	100110	103	G <sub>387</sub> G <sub>386</sub> G <sub>385</sub> G <sub>384</sub> G <sub>383</sub> G <sub>382</sub> G <sub>381</sub> G <sub>380</sub>
100111	72	100111	104	G <sub>397</sub> G <sub>396</sub> G <sub>395</sub> G <sub>394</sub> G <sub>393</sub> G <sub>392</sub> G <sub>391</sub> G <sub>390</sub>
101000	73	101000	105	G <sub>407</sub> G <sub>406</sub> G <sub>405</sub> G <sub>404</sub> G <sub>403</sub> G <sub>402</sub> G <sub>401</sub> G <sub>400</sub>
101001	74	101001	106	G <sub>417</sub> G <sub>416</sub> G <sub>415</sub> G <sub>414</sub> G <sub>413</sub> G <sub>412</sub> G <sub>411</sub> G <sub>410</sub>
101010	75	101010	107	G <sub>427</sub> G <sub>426</sub> G <sub>425</sub> G <sub>424</sub> G <sub>423</sub> G <sub>422</sub> G <sub>421</sub> G <sub>420</sub>
101011	76	101011	108	G <sub>437</sub> G <sub>436</sub> G <sub>435</sub> G <sub>434</sub> G <sub>433</sub> G <sub>432</sub> G <sub>431</sub> G <sub>430</sub>
101100	77	101100	109	G <sub>447</sub> G <sub>446</sub> G <sub>445</sub> G <sub>444</sub> G <sub>443</sub> G <sub>442</sub> G <sub>441</sub> G <sub>440</sub>
101101	78	101101	110	G <sub>457</sub> G <sub>456</sub> G <sub>455</sub> G <sub>454</sub> G <sub>453</sub> G <sub>452</sub> G <sub>451</sub> G <sub>450</sub>
101110	79	101110	111	G <sub>467</sub> G <sub>466</sub> G <sub>465</sub> G <sub>464</sub> G <sub>463</sub> G <sub>462</sub> G <sub>461</sub> G <sub>460</sub>
101111	80	101111	112	G <sub>477</sub> G <sub>476</sub> G <sub>475</sub> G <sub>474</sub> G <sub>473</sub> G <sub>472</sub> G <sub>471</sub> G <sub>470</sub>
110000	81	110000	113	G <sub>487</sub> G <sub>486</sub> G <sub>485</sub> G <sub>484</sub> G <sub>483</sub> G <sub>482</sub> G <sub>481</sub> G <sub>480</sub>
110001	82	110001	114	G <sub>497</sub> G <sub>496</sub> G <sub>495</sub> G <sub>494</sub> G <sub>493</sub> G <sub>492</sub> G <sub>491</sub> G <sub>490</sub>
110010	83	110010	115	G <sub>507</sub> G <sub>506</sub> G <sub>505</sub> G <sub>504</sub> G <sub>503</sub> G <sub>502</sub> G <sub>501</sub> G <sub>500</sub>
110011	84	110011	116	G <sub>517</sub> G <sub>516</sub> G <sub>515</sub> G <sub>514</sub> G <sub>513</sub> G <sub>512</sub> G <sub>511</sub> G <sub>510</sub>
110100	85	110100	117	G <sub>527</sub> G <sub>526</sub> G <sub>525</sub> G <sub>524</sub> G <sub>523</sub> G <sub>522</sub> G <sub>521</sub> G <sub>520</sub>
110101	86	110101	118	G <sub>537</sub> G <sub>536</sub> G <sub>535</sub> G <sub>534</sub> G <sub>533</sub> G <sub>532</sub> G <sub>531</sub> G <sub>530</sub>
110110	87	110110	119	G <sub>547</sub> G <sub>546</sub> G <sub>545</sub> G <sub>544</sub> G <sub>543</sub> G <sub>542</sub> G <sub>541</sub> G <sub>540</sub>
110111	88	110111	120	G <sub>557</sub> G <sub>556</sub> G <sub>555</sub> G <sub>554</sub> G <sub>553</sub> G <sub>552</sub> G <sub>551</sub> G <sub>550</sub>
111000	89	111000	121	G <sub>567</sub> G <sub>566</sub> G <sub>565</sub> G <sub>564</sub> G <sub>563</sub> G <sub>562</sub> G <sub>561</sub> G <sub>560</sub>
111001	90	111001	122	G <sub>577</sub> G <sub>576</sub> G <sub>575</sub> G <sub>574</sub> G <sub>573</sub> G <sub>572</sub> G <sub>571</sub> G <sub>570</sub>
111010	91	111010	123	G <sub>587</sub> G <sub>586</sub> G <sub>585</sub> G <sub>584</sub> G <sub>583</sub> G <sub>582</sub> G <sub>581</sub> G <sub>580</sub>
111011	92	111011	124	G <sub>597</sub> G <sub>596</sub> G <sub>595</sub> G <sub>594</sub> G <sub>593</sub> G <sub>592</sub> G <sub>591</sub> G <sub>590</sub>
111100	93	111100	125	G <sub>607</sub> G <sub>606</sub> G <sub>605</sub> G <sub>604</sub> G <sub>603</sub> G <sub>602</sub> G <sub>601</sub> G <sub>600</sub>
111101	94	111101	126	G <sub>617</sub> G <sub>616</sub> G <sub>615</sub> G <sub>614</sub> G <sub>613</sub> G <sub>612</sub> G <sub>611</sub> G <sub>610</sub>
111110	95	111110	127	G <sub>627</sub> G <sub>626</sub> G <sub>625</sub> G <sub>624</sub> G <sub>623</sub> G <sub>622</sub> G <sub>621</sub> G <sub>620</sub>
111111	96	111111	128	G <sub>637</sub> G <sub>636</sub> G <sub>635</sub> G <sub>634</sub> G <sub>633</sub> G <sub>632</sub> G <sub>631</sub> G <sub>630</sub>

Table 100. Look up table (Blue) 1

16 bit/pixel - mode 65,536 colours		18 bit/pixel -mode 262,144 colours		B output (8bit) 24 bit/pixel -mode 16,777,216 colours
B input (5 bit)	RGBSET parameter	B input (6 bit)	RGBSET parameter	
00000	97	000000	129	B <sub>007</sub> B <sub>006</sub> B <sub>005</sub> B <sub>004</sub> B <sub>003</sub> B <sub>002</sub> B <sub>001</sub> B <sub>000</sub>
00001	98	000001	130	B <sub>017</sub> B <sub>016</sub> B <sub>015</sub> B <sub>014</sub> B <sub>013</sub> B <sub>012</sub> B <sub>011</sub> B <sub>010</sub>
00010	99	000010	131	B <sub>027</sub> B <sub>026</sub> B <sub>025</sub> B <sub>024</sub> B <sub>023</sub> B <sub>022</sub> B <sub>021</sub> B <sub>020</sub>
00011	100	000011	132	B <sub>037</sub> B <sub>036</sub> B <sub>035</sub> B <sub>034</sub> B <sub>033</sub> B <sub>032</sub> B <sub>031</sub> B <sub>030</sub>
00100	101	000100	133	B <sub>047</sub> B <sub>046</sub> B <sub>045</sub> B <sub>044</sub> B <sub>043</sub> B <sub>042</sub> B <sub>041</sub> B <sub>040</sub>
00101	102	000101	134	B <sub>057</sub> B <sub>056</sub> B <sub>055</sub> B <sub>054</sub> B <sub>053</sub> B <sub>052</sub> B <sub>051</sub> B <sub>050</sub>
00110	103	000110	135	B <sub>067</sub> B <sub>066</sub> B <sub>065</sub> B <sub>064</sub> B <sub>063</sub> B <sub>062</sub> B <sub>061</sub> B <sub>060</sub>
00111	104	000111	136	B <sub>077</sub> B <sub>076</sub> B <sub>075</sub> B <sub>074</sub> B <sub>073</sub> B <sub>072</sub> B <sub>071</sub> B <sub>070</sub>
01000	105	001000	137	B <sub>087</sub> B <sub>086</sub> B <sub>085</sub> B <sub>084</sub> B <sub>083</sub> B <sub>082</sub> B <sub>081</sub> B <sub>080</sub>
01001	106	001001	138	B <sub>097</sub> B <sub>096</sub> B <sub>095</sub> B <sub>094</sub> B <sub>093</sub> B <sub>092</sub> B <sub>091</sub> B <sub>090</sub>
01010	107	001010	139	B <sub>107</sub> B <sub>106</sub> B <sub>105</sub> B <sub>104</sub> B <sub>103</sub> B <sub>102</sub> B <sub>101</sub> B <sub>100</sub>
01011	108	001011	140	B <sub>117</sub> B <sub>116</sub> B <sub>115</sub> B <sub>114</sub> B <sub>113</sub> B <sub>112</sub> B <sub>011</sub> B <sub>110</sub>
01100	109	001100	141	B <sub>127</sub> B <sub>126</sub> B <sub>125</sub> B <sub>124</sub> B <sub>123</sub> B <sub>122</sub> B <sub>121</sub> B <sub>120</sub>
01101	110	001101	142	B <sub>137</sub> B <sub>136</sub> B <sub>135</sub> B <sub>134</sub> B <sub>133</sub> B <sub>132</sub> B <sub>131</sub> B <sub>130</sub>
01110	111	001110	143	B <sub>147</sub> B <sub>146</sub> B <sub>145</sub> B <sub>144</sub> B <sub>143</sub> B <sub>142</sub> B <sub>141</sub> B <sub>140</sub>
01111	112	001111	144	B <sub>157</sub> B <sub>156</sub> B <sub>155</sub> B <sub>154</sub> B <sub>153</sub> B <sub>152</sub> B <sub>151</sub> B <sub>150</sub>
10000	113	010000	145	B <sub>167</sub> B <sub>166</sub> B <sub>165</sub> B <sub>164</sub> B <sub>163</sub> B <sub>162</sub> B <sub>161</sub> B <sub>160</sub>
10001	114	010001	146	B <sub>177</sub> B <sub>176</sub> B <sub>175</sub> B <sub>174</sub> B <sub>173</sub> B <sub>172</sub> B <sub>171</sub> B <sub>170</sub>
10010	115	010010	147	B <sub>187</sub> B <sub>186</sub> B <sub>185</sub> B <sub>184</sub> B <sub>183</sub> B <sub>182</sub> B <sub>181</sub> B <sub>180</sub>
10011	116	010011	148	B <sub>197</sub> B <sub>196</sub> B <sub>195</sub> B <sub>194</sub> B <sub>193</sub> B <sub>192</sub> B <sub>191</sub> B <sub>190</sub>
10100	117	010100	149	B <sub>207</sub> B <sub>206</sub> B <sub>205</sub> B <sub>204</sub> B <sub>203</sub> B <sub>202</sub> B <sub>201</sub> B <sub>200</sub>
10101	118	010101	150	B <sub>217</sub> B <sub>216</sub> B <sub>215</sub> B <sub>214</sub> B <sub>213</sub> B <sub>212</sub> B <sub>211</sub> B <sub>210</sub>
10110	119	010110	151	B <sub>227</sub> B <sub>226</sub> B <sub>225</sub> B <sub>224</sub> B <sub>223</sub> B <sub>222</sub> B <sub>221</sub> B <sub>220</sub>
10111	120	010111	152	B <sub>237</sub> B <sub>236</sub> B <sub>235</sub> B <sub>234</sub> B <sub>233</sub> B <sub>232</sub> B <sub>231</sub> B <sub>230</sub>
11000	121	011000	153	B <sub>247</sub> B <sub>246</sub> B <sub>245</sub> B <sub>244</sub> B <sub>243</sub> B <sub>242</sub> B <sub>241</sub> B <sub>240</sub>
11001	122	011001	154	B <sub>257</sub> B <sub>256</sub> B <sub>255</sub> B <sub>254</sub> B <sub>253</sub> B <sub>252</sub> B <sub>251</sub> B <sub>250</sub>
11010	123	011010	155	B <sub>267</sub> B <sub>266</sub> B <sub>265</sub> B <sub>264</sub> B <sub>263</sub> B <sub>262</sub> B <sub>261</sub> B <sub>260</sub>
11011	124	011011	156	B <sub>277</sub> B <sub>276</sub> B <sub>275</sub> B <sub>274</sub> B <sub>273</sub> B <sub>272</sub> B <sub>271</sub> B <sub>270</sub>
11100	125	011100	157	B <sub>287</sub> B <sub>286</sub> B <sub>285</sub> B <sub>284</sub> B <sub>283</sub> B <sub>282</sub> B <sub>281</sub> B <sub>280</sub>
11101	126	011101	158	B <sub>297</sub> B <sub>296</sub> B <sub>295</sub> B <sub>294</sub> B <sub>293</sub> B <sub>292</sub> B <sub>291</sub> B <sub>290</sub>
11110	127	011110	159	B <sub>307</sub> B <sub>306</sub> B <sub>305</sub> B <sub>304</sub> B <sub>303</sub> B <sub>302</sub> B <sub>301</sub> B <sub>300</sub>
11111	128	011111	160	B <sub>317</sub> B <sub>316</sub> B <sub>315</sub> B <sub>314</sub> B <sub>313</sub> B <sub>312</sub> B <sub>311</sub> B <sub>310</sub>

Table 101. Look up table (Blue) 2

16 bit/pixel - mode 65,536 colours		18 bit/pixel -mode 262,144 colours		B output (8bit) 24 bit/pixel -mode 16,777,216 colours
B input (5 bit)	RGBSET parameter	B input (6 bit)	RGBSET parameter	
No Input	-	100000	161	B <sub>327</sub> B <sub>326</sub> B <sub>325</sub> B <sub>324</sub> B <sub>323</sub> B <sub>322</sub> B <sub>321</sub> B <sub>320</sub>
No Input	-	100001	162	B <sub>337</sub> B <sub>336</sub> B <sub>335</sub> B <sub>334</sub> B <sub>333</sub> B <sub>332</sub> B <sub>331</sub> B <sub>330</sub>
No Input	-	100010	163	B <sub>347</sub> B <sub>346</sub> B <sub>345</sub> B <sub>344</sub> B <sub>343</sub> B <sub>342</sub> B <sub>341</sub> B <sub>340</sub>
No Input	-	100011	164	B <sub>357</sub> B <sub>356</sub> B <sub>355</sub> B <sub>354</sub> B <sub>353</sub> B <sub>352</sub> B <sub>351</sub> B <sub>350</sub>
No Input	-	100100	165	B <sub>367</sub> B <sub>366</sub> B <sub>365</sub> B <sub>364</sub> B <sub>363</sub> B <sub>362</sub> B <sub>361</sub> B <sub>360</sub>
No Input	-	100101	166	B <sub>377</sub> B <sub>376</sub> B <sub>375</sub> B <sub>374</sub> B <sub>373</sub> B <sub>372</sub> B <sub>371</sub> B <sub>370</sub>
No Input	-	100110	167	B <sub>387</sub> B <sub>386</sub> B <sub>385</sub> B <sub>384</sub> B <sub>383</sub> B <sub>382</sub> B <sub>381</sub> B <sub>380</sub>
No Input	-	100111	168	B <sub>397</sub> B <sub>396</sub> B <sub>395</sub> B <sub>394</sub> B <sub>393</sub> B <sub>392</sub> B <sub>391</sub> B <sub>390</sub>
No Input	-	101000	169	B <sub>407</sub> B <sub>406</sub> B <sub>405</sub> B <sub>404</sub> B <sub>403</sub> B <sub>402</sub> B <sub>401</sub> B <sub>400</sub>
No Input	-	101001	170	B <sub>417</sub> B <sub>416</sub> B <sub>415</sub> B <sub>414</sub> B <sub>413</sub> B <sub>412</sub> B <sub>411</sub> B <sub>410</sub>
No Input	-	101010	171	B <sub>427</sub> B <sub>426</sub> B <sub>425</sub> B <sub>424</sub> B <sub>423</sub> B <sub>422</sub> B <sub>421</sub> B <sub>420</sub>
No Input	-	101011	172	B <sub>437</sub> B <sub>436</sub> B <sub>435</sub> B <sub>434</sub> B <sub>433</sub> B <sub>432</sub> B <sub>431</sub> B <sub>430</sub>
No Input	-	101100	173	B <sub>447</sub> B <sub>446</sub> B <sub>445</sub> B <sub>444</sub> B <sub>443</sub> B <sub>442</sub> B <sub>441</sub> B <sub>440</sub>
No Input	-	101101	174	B <sub>457</sub> B <sub>456</sub> B <sub>455</sub> B <sub>454</sub> B <sub>453</sub> B <sub>452</sub> B <sub>451</sub> B <sub>450</sub>
No Input	-	101110	175	B <sub>467</sub> B <sub>466</sub> B <sub>465</sub> B <sub>464</sub> B <sub>463</sub> B <sub>462</sub> B <sub>461</sub> B <sub>460</sub>
No Input	-	101111	176	B <sub>477</sub> B <sub>476</sub> B <sub>475</sub> B <sub>474</sub> B <sub>473</sub> B <sub>472</sub> B <sub>471</sub> B <sub>470</sub>
No Input	-	110000	177	B <sub>487</sub> B <sub>486</sub> B <sub>485</sub> B <sub>484</sub> B <sub>483</sub> B <sub>482</sub> B <sub>481</sub> B <sub>480</sub>
No Input	-	110001	178	B <sub>497</sub> B <sub>496</sub> B <sub>495</sub> B <sub>494</sub> B <sub>493</sub> B <sub>492</sub> B <sub>491</sub> B <sub>490</sub>
No Input	-	110010	179	B <sub>507</sub> B <sub>506</sub> B <sub>505</sub> B <sub>504</sub> B <sub>503</sub> B <sub>502</sub> B <sub>501</sub> B <sub>500</sub>
No Input	-	110011	180	B <sub>517</sub> B <sub>516</sub> B <sub>515</sub> B <sub>514</sub> B <sub>513</sub> B <sub>512</sub> B <sub>511</sub> B <sub>510</sub>
No Input	-	110100	181	B <sub>527</sub> B <sub>526</sub> B <sub>525</sub> B <sub>524</sub> B <sub>523</sub> B <sub>522</sub> B <sub>521</sub> B <sub>520</sub>
No Input	-	110101	182	B <sub>537</sub> B <sub>536</sub> B <sub>535</sub> B <sub>534</sub> B <sub>533</sub> B <sub>532</sub> B <sub>531</sub> B <sub>530</sub>
No Input	-	110110	183	B <sub>547</sub> B <sub>546</sub> B <sub>545</sub> B <sub>544</sub> B <sub>543</sub> B <sub>542</sub> B <sub>541</sub> B <sub>540</sub>
No Input	-	110111	184	B <sub>557</sub> B <sub>556</sub> B <sub>555</sub> B <sub>554</sub> B <sub>553</sub> B <sub>552</sub> B <sub>551</sub> B <sub>550</sub>
No Input	-	111000	185	B <sub>567</sub> B <sub>566</sub> B <sub>565</sub> B <sub>564</sub> B <sub>563</sub> B <sub>562</sub> B <sub>561</sub> B <sub>560</sub>
No Input	-	111001	186	B <sub>577</sub> B <sub>576</sub> B <sub>575</sub> B <sub>574</sub> B <sub>573</sub> B <sub>572</sub> B <sub>571</sub> B <sub>570</sub>
No Input	-	111010	187	B <sub>587</sub> B <sub>586</sub> B <sub>585</sub> B <sub>584</sub> B <sub>583</sub> B <sub>582</sub> B <sub>581</sub> B <sub>580</sub>
No Input	-	111011	188	B <sub>597</sub> B <sub>596</sub> B <sub>595</sub> B <sub>594</sub> B <sub>593</sub> B <sub>592</sub> B <sub>591</sub> B <sub>590</sub>
No Input	-	111100	189	B <sub>607</sub> B <sub>606</sub> B <sub>605</sub> B <sub>604</sub> B <sub>603</sub> B <sub>602</sub> B <sub>601</sub> B <sub>600</sub>
No Input	-	111101	190	B <sub>617</sub> B <sub>616</sub> B <sub>615</sub> B <sub>614</sub> B <sub>613</sub> B <sub>612</sub> B <sub>611</sub> B <sub>610</sub>
No Input	-	111110	191	B <sub>627</sub> B <sub>626</sub> B <sub>625</sub> B <sub>624</sub> B <sub>623</sub> B <sub>622</sub> B <sub>621</sub> B <sub>620</sub>
No Input	-	111111	192	B <sub>637</sub> B <sub>636</sub> B <sub>635</sub> B <sub>634</sub> B <sub>633</sub> B <sub>632</sub> B <sub>631</sub> B <sub>630</sub>

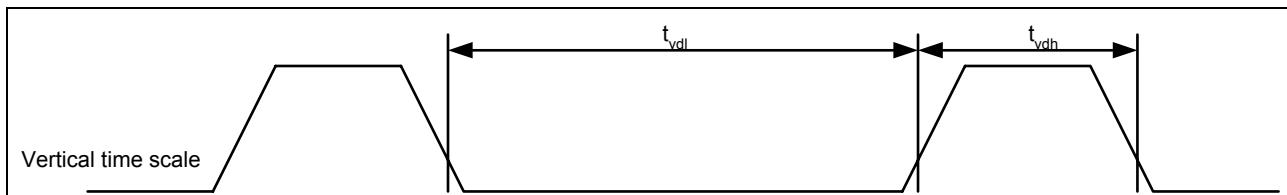
## 4.12. TEARING EFFECT OUTPUT LINE

The Tearing Effect output line supplies a Panel synchronization signal to the MCU. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command and interface type (IM[3:0] pads). The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

Note. In MPU I/F type II mode, TE pad is not used for tearing effect signal. Refer to section 4.12.3

### 4.12.1. Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

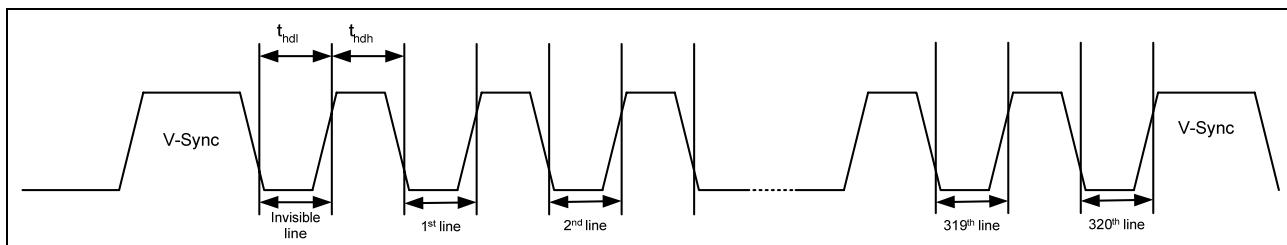


**Figure 119. Tearing effect output signal consists of v-blanking information only**

$t_{vdh}$  = The LCD display is not updated from the Frame Memory

$t_{vdl}$  = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 320H-sync pulses per field.



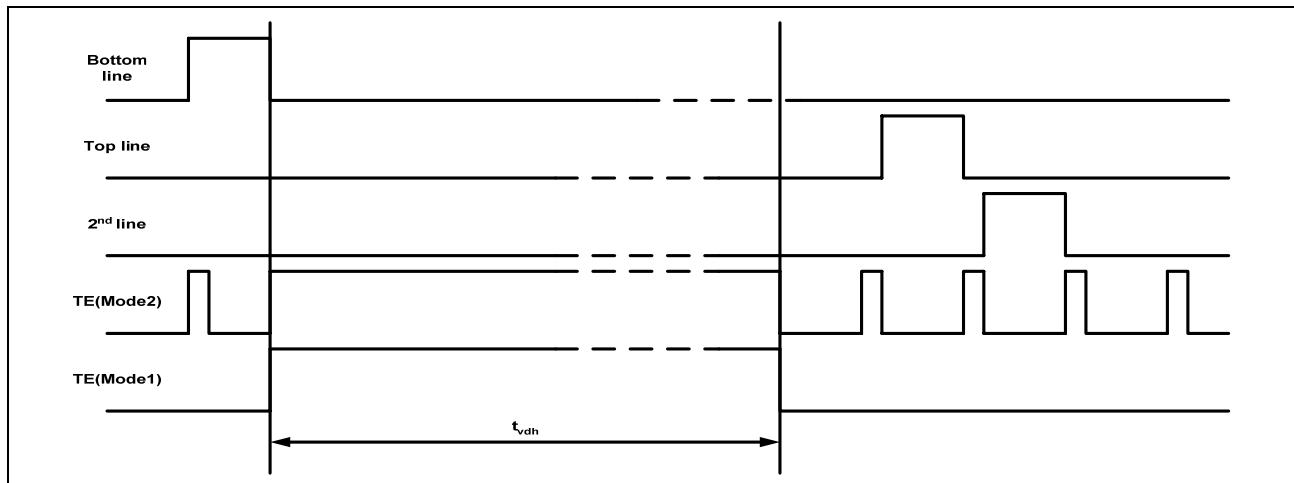
**Figure 120. Tearing effect output signal consists of v-blanking and g-blanking information**

$t_{vdh}$  = The LCD display is not updated from the Frame Memory

$t_{vdl}$  = The LCD display is updated from the Frame Memory (except Invisible Line- see above)

$t_{hdh}$  = The LCD display is not updated from the Frame Memory

$t_{hdl}$  = The LCD display is updated from the Frame Memory (except Invisible Line – see above)

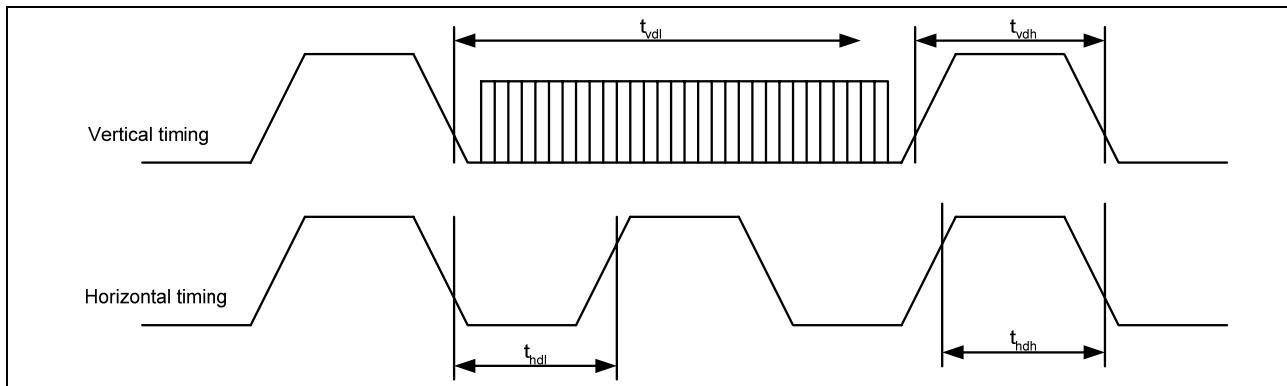


**Figure 121. Tearing effect output signal**

Note. During Sleep In Mode, The Tearing Output Pin is active Low

#### 4.12.2. Tearing Effect Line Timings

The Tearing effect signal is described below.



**Figure 122. Tearing effect output signal timing**

**Table 102. AC characteristics of tearing effect signal (IDLE mode off)**

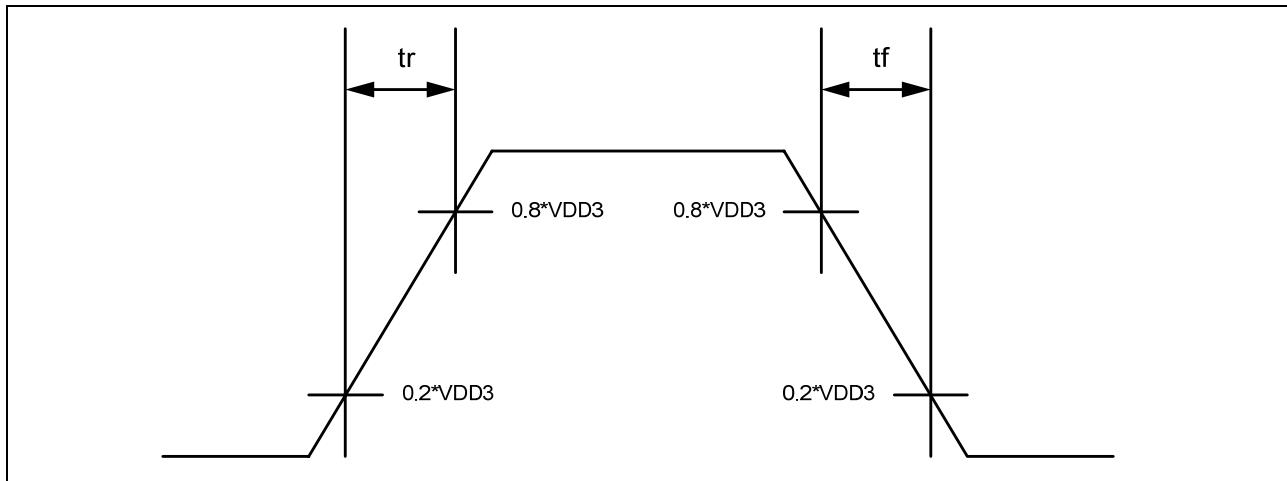
Symbol	Parameter	min	max	unit	Description
t <sub>vdl</sub>	Vertical timing low duration	-	-	ms	
t <sub>vdh</sub>	Vertical timing high duration	1000	-	us	
t <sub>hdl</sub>	Horizontal timing low duration	-	-	us	
t <sub>hdh</sub>	Horizontal timing high duration	-	500	us	

Note1. The timings in above Table apply when MADCTL D4=0 and D4=1

Note2. tvdh is controlled by VBP and VFP. To meet the timing in above table, BP + FP must be bigger than 21 (Frame Freq. 60Hz)

Note3. When TE mode 2 in MCU Interface, the high period of TE signal in horizontal timing can be controlled in HBP+2.

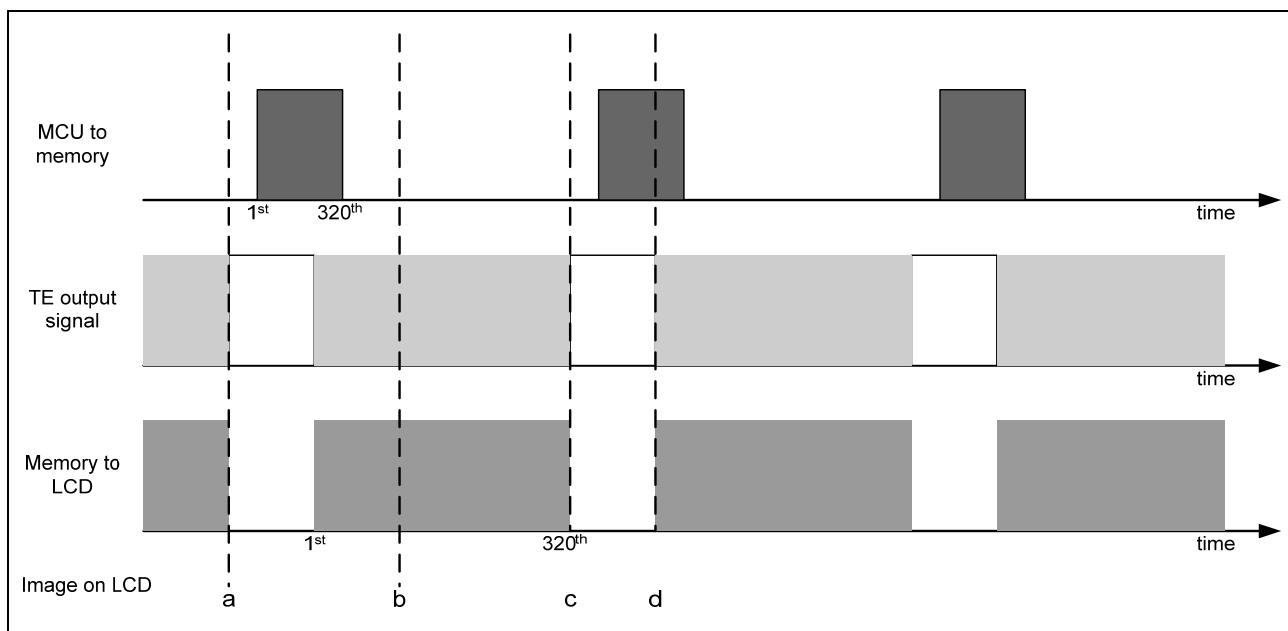
The rise and fall time of TE signal is stipulated to be equal to or less than 15ns.



**Figure 123. Rise and fall time of TE signal**

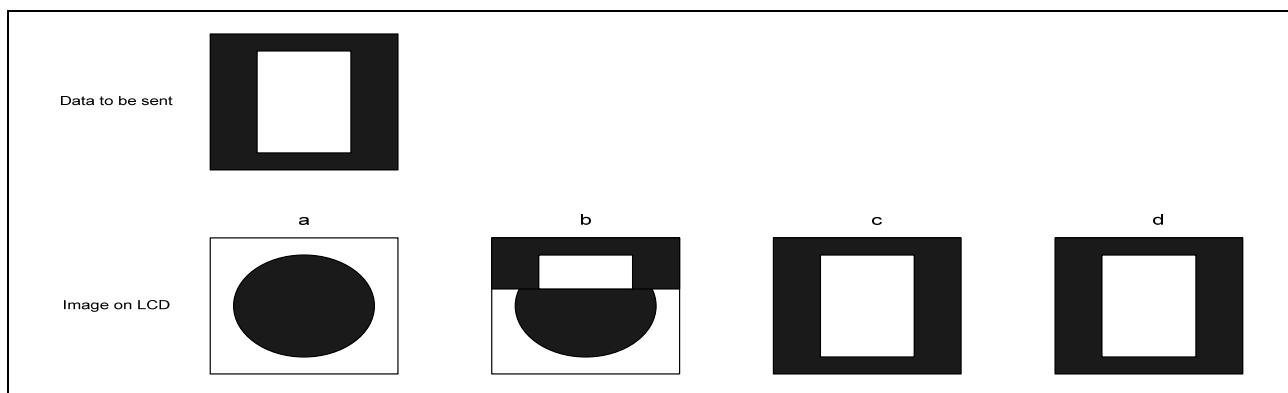
The Tearing Effect Output Line is fed back to the MCU and should be used as shown below to avoid Tearing Effect.

4.12.2.1. Example 1: MCU write is faster than panel read.



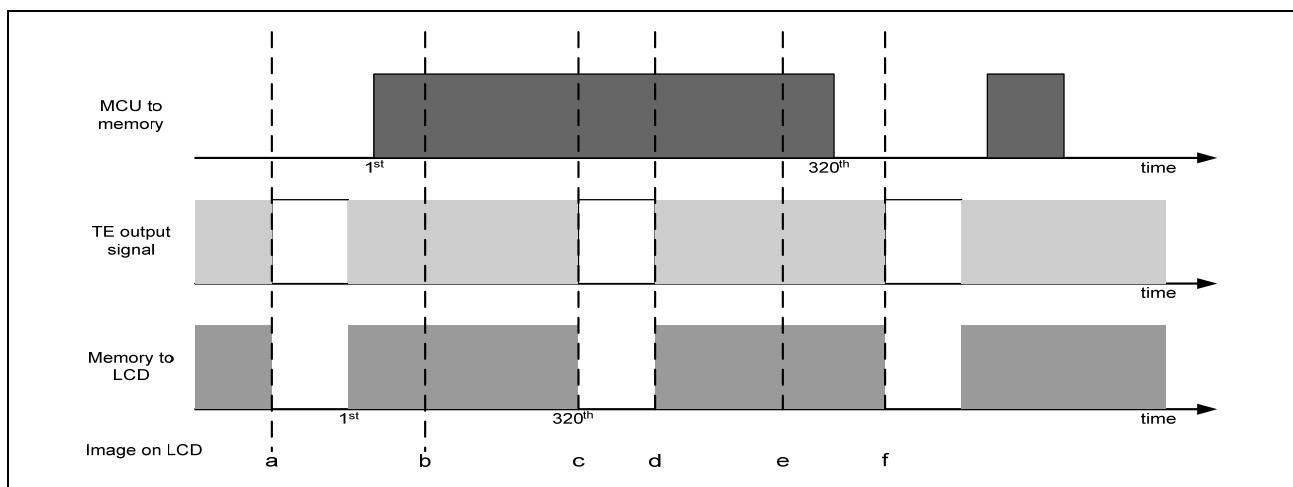
**Figure 124. Method 1 to avoid tearing effect**

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image.



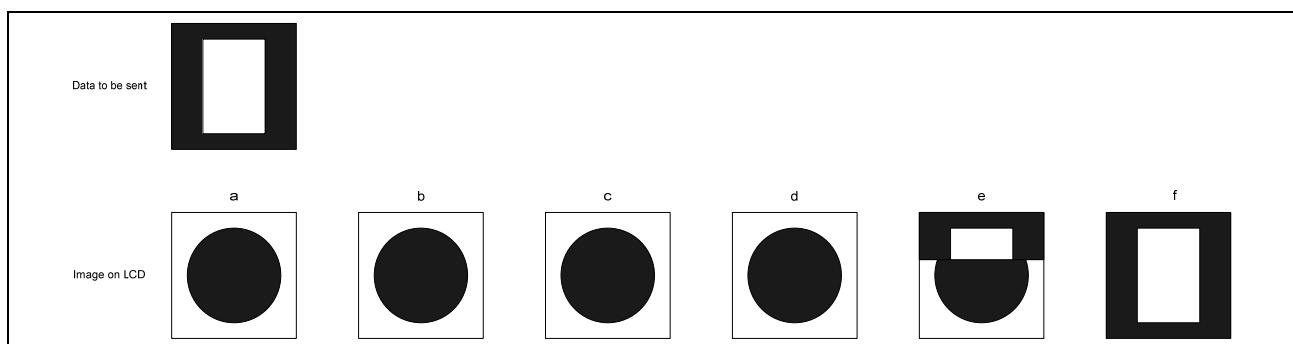
**Figure 125. Panel image refreshment of method 1**

4.12.2.2. Example 2 : MCU write is slower than panel read.



**Figure 126. Method 2 to avoid tearing effect**

The MCU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and to finish downloading during the subsequent Frame before the Read Pointer “catches” the MCU to Frame memory write position.



**Figure 127. Panel image refreshment of method 2**

#### 4.12.3. TE signal in MPU IF type II

In MPU I/F type II mode, S6D04M0 outputs the frame mark signal instead of tearing effect signal through TE pad. This signal also can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the signal is defined by the parameter of the Tearing Effect Line On command and interface type (IM[3:0] pads).

Mode1. TE is toggling every frame.

Mode2. TE is toggling every 2 frame.

Timing diagram of TE signal in MPU I/F type II is shown below.

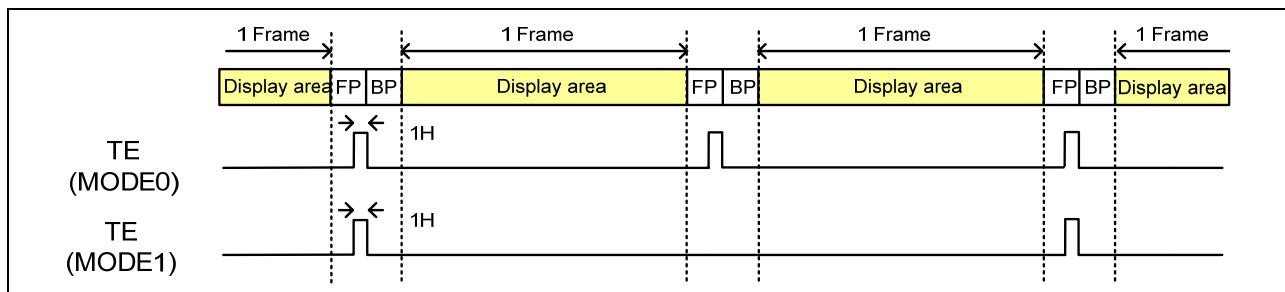
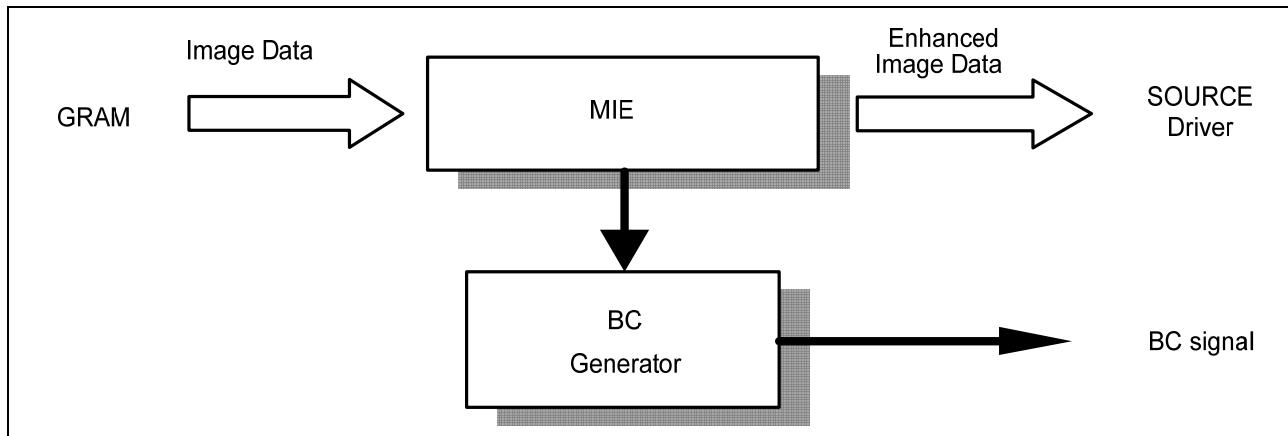


Figure 128. TE output signal (MPU I/F type II)

#### 4.13. MIE FUNCTION

S6D04M0 has a special image enhancement function. MIE (Mobile Image Enhancement) reduces power consumption of backlight unit by adaptive enhancement of luminance and contrast. According the brightness enhancement rate of input image, the power reduction of BLU is controlled automatically.



**Figure 129. Flowchart of MIE function**

When MIE is enabled, MIE dynamically changes the brightness of backlight unit by on-chip BC(Backlight Control) Generator. Host can control the rate of BLU power reduction by setting RRC value (Refer to CAh Command.)

When MIE is enabled, the enhanced data is outputted to Source block. Host processor should select movie or still-Image mode (Refer to 55h Command).

## CHAPTER 5

# COMMAND

- 5.1 Command List
- 5.2 Description of Level 1 Command
- 5.3 Description of Level 2 Command
- 5.4 Description of Level 3 Command

# 5 COMMAND

## 5.1. COMMAND LIST

### 5.1.1. Level 1: Function Command

**Table 103. Instruction code**

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Reference
NOP	W	0	0	0	0	0	0	0	0	0	00h	5.2.1
SWRESET	W	0	0	0	0	0	0	0	0	1	01h	5.2.2
RDDIDIF	R	0	0	0	0	0	0	1	0	0	04h	5.2.3
		1	-	-	-	-	-	-	-	-	-	
		1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		
		1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		
		1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		
RDDST	R	0	0	0	0	0	1	0	0	1	09h	5.2.4
		1	-	-	-	-	-	-	-	-	-	
		1	D31	D30	D29	D28	D27	D26	D25	0		
		1	0	1	1	0	D19	D18	D17	D16		
		1	0	0	0	0	0	D10	D9	D8		
		1	D7	D6	D5	0	0	0	0	0		
RDDPM	R	0	0	0	0	0	1	0	1	0	0Ah	5.2.5
		1	-	-	-	-	-	-	-	-	-	
		1	D7	D6	D5	D4	D3	D2	0	0		
RDD MADCTL	R	0	0	0	0	0	1	0	1	1	0Bh	5.2.6
		1	-	-	-	-	-	-	-	-	-	
		1	D7	D6	D4	D4	D3	D2	0	0		
RDD COLMOD	R	0	0	0	0	0	1	1	0	0	0Ch	5.2.7
		1	-	-	-	-	-	-	-	-	-	
		1	0	D6	D5	D4	0	D2	D1	D0		
RDDIM	R	0	0	0	0	0	1	1	0	1	0Dh	5.2.8
		1	-	-	-	-	-	-	-	-	-	
		1	0	0	0	0	0	D2	D1	D0		
RDDSM	R	0	0	0	0	0	1	1	1	0	0Eh	5.2.9
		1	-	-	-	-	-	-	-	-	-	



Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Reference
		1	D7	D6	0	0	0	0	0	0		
RDDSDR	R	0	0	0	0	0	1	1	1	1	0Fh	5.2.10
		1	-	-	-	-	-	-	-	-		
		1	D7	D6	0	0	0	0	0	0		
SLPIN	W	0	0	0	0	1	0	0	0	0	10h	5.2.11
SLPOUT	W	0	0	0	0	1	0	0	0	1	11h	5.2.12
PTLON	W	0	0	0	0	1	0	0	1	0	12h	5.2.13
NORON	W	0	0	0	0	1	0	0	1	1	13h	5.2.14
GAMSET	W	0	0	0	1	0	0	1	1	0	26h	5.2.15
		1	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0		
DISPOFF	W	0	0	0	1	0	1	0	0	0	28h	5.2.16
DISPON	W	0	0	0	1	0	1	0	0	1	29h	5.2.17
CASET	W	0	0	0	1	0	1	0	1	0	2Ah	5.2.18
		1	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8		
		1	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0		
		1	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8		
		1	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0		
PASET	W	0	0	0	1	0	1	0	1	1	2Bh	5.2.19
		1	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8		
		1	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0		
		1	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8		
		1	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0		
RAMWR	W	0	0	0	1	0	1	1	0	0	2Ch	5.2.20
		1	D7	D6	D5	D4	D3	D2	D1	D0		
RGBSET	W	0	0	0	1	0	1	1	0	1	2Dh	5.2.21
		1	R007	R006	R005	R004	R003	R002	R001	R000		
		1	...	...	...	...	...	...	...	...		
		1	B637	B636	B635	B634	B633	B632	B631	B630		
RAMRD	R	0	0	0	1	0	1	1	1	0	2Eh	5.2.22
		1	-	-	-	-	-	-	-	-		
		1	D7	D6	D5	D4	D3	D2	D1	D0		

Table 104. Instruction code (continued)

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Reference
PTLAR	W	0	0	0	1	1	0	0	0	0	30h	5.2.23
		1	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8		
		1	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0		
		1	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8		
		1	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0		
TEOFF	W	0	0	0	1	1	0	1	0	0	34h	5.2.24
TEON	W	0	0	0	1	1	0	1	0	1	35h	5.2.25
		1	0	0	0	0	0	0	0	M		
MADCTL	W	0	0	0	1	1	0	1	1	0	36h	5.2.26
		1	D7	D6	D5	D4	D3	D2	0	0		
IDMOFF	W	0	0	0	1	1	1	0	0	0	38h	5.2.27
IDMON	W	0	0	0	1	1	1	0	0	1	39h	5.2.28
COLMOD	W	0	0	0	1	1	1	0	1	0	3Ah	5.2.29
		1	-	D6	D5	D4	-	D2	D1	D0		
RDID1	R	0	1	1	0	1	1	0	1	0	DAh	5.2.30
		1	-	-	-	-	-	-	-	-		
		1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		
RDID2	R	0	1	1	0	1	1	0	1	1	DBh	5.2.31
		1	-	-	-	-	-	-	-	-		
		1	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20		
RDID3	R	0	1	1	0	1	1	1	0	0	DCh	5.2.32
		1	-	-	-	-	-	-	-	-		
		1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		
WRDISBV	W	0	0	1	0	1	0	0	0	1	51h	5.2.33
		1	MAN_B RIGHT7	MAN_B RIGHT6	MAN_B RIGHT5	MAN_B RIGHT4	MAN_B RIGHT3	MAN_B RIGHT2	MAN_B RIGHT1	MAN_B RIGHT0		
RDDISBV	R	0	0	1	0	1	0	0	1	0	52h	5.2.34
		1	-	-	-	-	-	-	-	-		
		1	DISP_B RIGHT7	DISP_B RIGHT6	DISP_B RIGHT5	DISP_B RIGHT4	DISP_B RIGHT3	DISP_B RIGHT2	DISP_B RIGHT1	DISP_B RIGHT0		
WRCTRLD	W	0	0	1	0	1	0	0	1	1	53h	5.2.35
		1	-	-	BCTRL	-	DD	BL	-	-		
RDCTRLD	R	0	0	1	0	1	0	1	0	0	54h	5.2.36
		1	-	-	-	-	-	-	-	-		
		1	-	-	BCTRL	-	DD	BL	-	-		



Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Reference
WRCABC	W	0	0	1	0	1	0	1	0	1	55h	5.2.37
		1	-	-	-	-	-	-	MIE_M ODE1	MIE_M ODE0		
RDCABC	R	0	0	1	0	1	0	1	1	0	56h	5.2.38
		1	-	-	-	-	-	-	-	-		
		1	-	-	-	-	-	-	MIE_M ODE1	MIE_M ODE0		
WRCABCM B	W	0	0	1	0	1	1	1	1	0	5Eh	5.2.39
		1	MIN_B RIGHT7	MIN_B RIGHT6	MIN_B RIGHT5	MIN_B RIGHT4	MIN_B RIGHT3	MIN_B RIGHT2	MIN_B RIGHT1	MIN_B RIGHT0		
RDCABCMB	R	0	0	1	0	1	1	1	1	1	5Fh	5.2.40
		1	-	-	-	-	-	-	-	-		
		1	MIN_B RIGHT7	MIN_B RIGHT6	MIN_B RIGHT5	MIN_B RIGHT4	MIN_B RIGHT3	MIN_B RIGHT2	MIN_B RIGHT1	MIN_B RIGHT0		
MIECTL1	W	0	1	1	0	0	1	0	1	0	CAh	5.2.41
		1	RRC7	RRC6	RRC5	RRC4	RRC3	RRC2	RRC1	RRC0		
		1	IERC7	IERC6	IERC5	IERC4	IERC3	IERC2	IERC1	IERC0		
		1	-	-	ONOFF _DIMM _EN	SERC 4	SERC 3	SERC 2	SERC 1	SERC 0		
BCMODE	W	0	1	1	0	0	1	0	1	1	CBh	5.2.42
		1	-	-	-	-	-	-	BC_M ODE1	BC_M ODE0		

Note. Undefined commands are treated as NOP(00h) command for MPU80 interface type .

B0 to D9 and DE to FF are for the factory use of the display supplier. User can decide if these commands are available or they are treated as NOP(00h) commands before shipping to user. Default value is NOP(00h).

Commands 10h, 12h, 13h, 26h, 28h, 29h, 30h, 36h (Bit 4 only), 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh) and Read Self Diagnostic Result (0Fh) commands are updated immediately both in Sleep In mode and Sleep Out mode.

### 5.1.2. Level 2 : Function Command

**Table 105.Instruction code – (B0)**

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
DSTB	W	0	1	1	0	0	1	1	0	1	B0h	5.3.1
		1	-	-	-	-	-	-	-	DSTB		

**Table 106.Instruction code – (CC ~ CD)**

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
MIECTL2	R/W	0	1	1	0	0	1	1	0	0	CCh	5.3.2
		-	-	CAT1	CAT0	CST1	CST0	WINVA DDR08	WINVA DDR07			
		WINVA DDR06	WINVA DDR05	WINVA DDR04	WINVA DDR03	WINVA DDR02	WINVA DDR01	WINVA DDR00	WINVA DDR18			
		WINVA DDR17	WINVA DDR16	WINVA DDR15	WINVA DDR14	WINVA DDR13	WINVA DDR12	WINVA DDR11	WINVA DDR10			
		0	0	0	0	0	0	0	0	0		
		1	1	1	0	1	1	1	1	1		
		0	1	1	0	0	1	1	0	1	CDh	
MIECTL3	R/W	1	-	BC_FR	BC_FR	BC_FR	BC_FR	BC_FR	BC_FR	BC_FR		5.3.3
			Q_ SEL6	Q_ SEL5	Q_ SEL4	Q_ SEL3	Q_ SEL2	Q_ SEL1	Q_ SEL0			
			BL_MO DE_IN SLP	-	DT2	DT1	DT0	BL_DR V_EN	BL_DI MM_S TEP1	BL_DI MM_S TEP0		

Table 107. Instruction code – (D0 ~ D5)

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
MTPCTL	R/W	0	1	1	0	1	0	0	0	0	D0h	5.3.4
		1	-	-	-	-	ID_SEL	MTP_SEL	MTP_MODE	MTP_EX		
		-	-	-	-	-	-	MTP_ERB	MTP_LOAD	MTP_WRB		
WRVCMOC	R/W	0	1	1	0	1	0	0	0	1	D1h	5.3.5
		1	-	-	-	C4	VCMO	VCMO	VCMO	VCMO		
WRVMLOC	R/W	0	1	1	0	1	0	0	1	0	D2h	5.3.6
		1	-	-	-	C3	VMLO	VMLO	VMLO	VMLO		
WRGVDOC	R/W	0	1	1	0	1	0	0	1	1	D3h	5.3.7
		1	-	-	-	C4	GVDO	GVDO	GVDO	GVDO		
WRID	R/W	0	1	1	0	1	0	1	0	0	D4h	5.3.8
		1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		
		1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		
		1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		
RDOFFSETC	R	0	1	1	0	1	0	1	0	1	D5h	5.3.9
		-	-	-	-	-	-	-	-	-		
		0	0	0	C_MTP	VCMO	VCMO	VCMO	VCMO	VCMO		
		1	0	0	C_MTP	C_MTP	C_MTP	C_MTP	C_MTP	C_MTP		
		0	0	0	C_MTP	VMLO	VMLO	VMLO	VMLO	VMPO		
DCON	R/W	0	1	1	0	1	1	0	0	1	D9h	5.3.25
		0	0	0	0	0	0	0	0	0		
		1	TESTK	TESTK	TESTK	TESTK	TESTK	TESTK	TESTK	TESTK		
		7	6	5	4	3	2	1	0			

Table 108. Instruction code – (F0 ~ F6)

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
WRPWD	R/W	0	1	1	1	1	0	0	0	0	F0h	5.3.10
		1	TESTW7	TESTW6	TESTW5	TESTW4	TESTW3	TESTW2	TESTW1	TESTW0		
			TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0		
RDPWD	R/W	0	1	1	1	1	0	0	0	1	F1h	5.3.11
		1	TESTR7	TESTR6	TESTR5	TESTR4	TESTR3	TESTR2	TESTR1	TESTR0		
DISCTL	R/W	0	1	1	1	1	0	0	1	0	F2h	5.3.12
		-	-	-	NRTN4	NRTN3	NRTN2	NRTN1	NRTN0			
		-	-	-	IPRTN 4	IPRTN 3	IPRTN 2	IPRTN 1	IPRTN 0			
		-	-	-	-	IPINV	IINV	PINV	NINV			
		NVBP7	NVBP6	NVBP5	NVBP4	NVBP3	NVBP2	NVBP1	NVBP0			
		NVFP7	NVFP6	NVFP5	NVFP4	NVFP3	NVFP2	NVFP1	NVFP0			
		IPVBP7	IPVBP6	IPVBP5	IPVBP4	IPVBP3	IPVBP2	IPVBP1	IPVBP0			
		IPVFP7	IPVFP6	IPVFP5	IPVFP4	IPVFP3	IPVFP2	IPVFP1	IPVFP0			
		-	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0			
		-	-	-	-	-	SM	GS	REV			
		-	-	-	NCRTN4	NCRTN3 2	NCRTN 1	NCRTN 0				
		-	-	-	IPCRTN 4	IPCRTN 3	IPCRTN 2	IPCRTN 1	IPCRTN 0			
PWRCTL	R/W	0	1	1	1	1	0	0	1	1	F3h	5.3.13
		APON	GON	AON	PON3	PON2	PON1	PON	VCI1_E N			
		-	-	NDC31	NDC30	NDC21	NDC20	NDC11	NDC10			
		-	-	IPDC31	IPDC30	IPDC21	IPDC20	IPDC11	IPDC10			
		-	-	-	-	VC3	VC2	VC1	VC0			
		-	IPBT2	IPBT1	IPBT0	-	NBT2	NBT1	NBT0			
		-	GVD6	GVD5	GVD4	GVD3	GVD2	GVD1	GVD0			
		-	IPGVD6	IPGVD5	IPGVD4	IPGVD3	IPGVD2	IPGVD1	IPGVD0			
		-	-	VGH_ FLAG_E N	AB_ VCI1	NAB2A_ G	IPAB2A_ G	NAB2A	IPAB2A			
VCMCTL	R/W	0	1	1	1	1	0	1	0	0	F4h	5.3.14
		1	-	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0		
		-	IPVCM6	IPVCM5	IPVCM4	IPVCM3	IPVCM2	IPVCM1	IPVCM0			



Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
			VCOMG	VML6	VML5	VML4	VML3	VML2	VML1	VML0		
			-	IPVML6	IPVML5	IPVML4	IPVML3	IPVML2	IPVML1	IPVML0		
			-	VCIRA2	VCIRA1	VCIRA0	0	VCIR2	VCIR1	VCIR0		
SRCCTL	R/W	0	1	1	1	1	0	1	0	1	F5h	5.3.15
			--	-	-	GS_EN	-	-	NGF	SG		
			-	IPSDT2	IPSDT1	IPSDT0	-	NSDT2	NSDT1	NSDT0		
			-	-	-	-	SAP3	SAP2	SAP1	SAP0		
			NBLK_ VCIR1	NBLK_ VCIR0	IPBLK_ VCIR1	IPBLK_ VCIR0	NDISP_ CON1	NDISP_ CON0	IPDISP_ CON1	IPDISP_ CON0		
			-	VCOM_ BLK_OF F	-	-	NBLK_ CON1	NBLK_ CON0	IPBLK_ CON1	IPBLK_ CON0		
			-	-	-	GOCM2	GOCM1	GOCM0	OCM1	OCM0		
IFCTL	R/W	0	1	1	1	1	0	1	1	0	F6h	5.3.16
			MY_ EOR	MX_ EOR	MV_ EOR	ML_ EOR	BGR_ EOR	-	-	-		
			IPM2	IPM1	IPM0	MDT1	MDT0	CM	VSM	DM		
			VPL	HPL	DPL	EPL	ENDIAN	-	-	RIM		
			-	-	SPR_SE L1	SPR_ SEL0	RGB_ DIV3	RGB_ DIV2	RGB_ DIV1	RGB_ DIV0		

Table 109. Instruction Code – (F7 ~ FD)

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
RPGAMCTL	R/W	0	1	1	1	1	0	1	1	1	F7h	5.3.17
			RGLP1	RGLP0	RRFP5	RRFP4	RRFP3	RRFP2	RRFP1	RRFP0		
			-	-	ROSP5	ROSP4	ROSP3	ROSP2	ROSP1	ROSP0		
			-	-	RPKP05	RPKP04	RPKP03	RPKP02	RPKP01	RPKP00		
			-	-	RPKP15	RPKP14	RPKP13	RPKP12	RPKP11	RPKP10		
			-	-	RPKP25	RPKP24	RPKP23	RPKP22	RPKP21	RPKP20		
			-	-	RPKP35	RPKP34	RPKP33	RPKP32	RPKP31	RPKP30		
			-	-	RPKP45	RPKP44	RPKP43	RPKP42	RPKP41	RPKP40		
			-	-	RPKP55	RPKP54	PPKP53	RPKP52	RPKP51	RPKP50		
		1	-	-	RPKP65	RPKP64	RPKP63	RPKP62	RPKP61	RPKP60		
			-	-	RPKP75	RPKP74	RPKP73	RPKP72	RPKP71	RPKP70		
			-	-	RPKP85	RPKP84	RPKP83	RPKP82	RPKP81	RPKP80		
			-		RPKP95	RPKP94	RPKP93	RPKP92	RPKP91	RPKP90		
			-		RPKP105	RPKP104	RPKP103	RPKP102	RPKP101	RPKP100		
			RGSR	RGSR	RGSR	RGSR	RGSR	RGSR	RGSR	RGSR		
			P03	P02	P01	P00	P13	P12	P11	P10		
			RGSR	RGSR	RGSR	RGSR	RGSR	RGSR	RGSR	RGSR		
			P23	P22	P21	P20	P33	P32	P31	P30		
RNGAMCTL	R/W	0	1	1	1	1	1	0	0	0	F8h	5.3.18
		1	RGLN1	RGLN0	RRFN5	RRFN4	RRFN3	RRFN2	RRFN1	RRFN0		
			-	-	ROSN5	ROSN4	ROSN3	ROSN2	ROSN1	ROSN0		
			-	-	RPKN05	RPKN04	RPKN03	RPKN02	RPKN01	RPKN00		
			-	-	RPKN15	RPKN14	RPKN13	RPKN12	RPKN11	RPKN10		
			-	-	RPKN25	RPKN24	RPKN23	RPKN22	RPKN21	RPKN20		
			-	-	RPKN35	RPKN34	RPKN33	RPKN32	RPKN31	RPKN30		
			-	-	RPKN45	RPKN44	RPKN43	RPKN42	RPKN41	RPKN40		
			-	-	RPKN55	RPKN54	RPKN53	RPKN52	RPKN51	RPKN50		
			-	-	RPKN65	RPKN64	RPKN63	RPKN62	RPKN61	RPKN60		
			-	-	RPKN75	RPKN74	RPKN73	RPKN72	RPKN71	RPKN70		
			-	-	RPKN85	RPKN84	RPKN83	RPKN82	RPKN81	RPKN80		
			-	-	RPKN95	RPKN94	RPKN93	RPKN92	RPKN91	RPKN90		
			-	-	RPKN105	RPKN104	RPKN103	RPKN102	RPKN101	RPKN100		
			RGSR	RGSR	RGSR	RGSR	RGSR	RGSR	RGSR	RGSR		
			N03	N02	N01	N00	N13	N12	N11	N11		



Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
			RGSR N23	RGSR N22	RGSR N21	RGSR N20	RGSR N33	RGSR N32	RGSR N31	RGSR N31		
GPGAMCTL	R/W	0	1	1	1	1	1	0	0	1	F9h	5.3.19
		GGLP1	GGLP0	GRFP5	GRFP4	GRFP3	GRFP2	GRFP1	GRFP0			
		-	-	GOSP5	GOSP4	GOSP3	GOSP2	GOSP1	GOSP0			
		-	-	GPKP05	GPKP04	GPKP03	GPKP02	GPKP01	GPKP00			
		-	-	GPKP15	GPKP14	GPKP13	GPKP12	GPKP11	GPKP10			
		-	-	GPKP25	GPKP24	GPKP23	GPKP22	GPKP21	GPKP20			
		-	-	GPKP35	GPKP34	GPKP33	GPKP32	GPKP31	GPKP30			
		-	-	GPKP45	GPKP44	GPKP43	GPKP42	GPKP41	GPKP40			
		-	-	GPKP55	GPKP54	GPKP53	GPKP52	GPKP51	GPKP50			
		-	-	GPKP65	GPKP64	GPKP63	GPKP62	GPKP61	GPKP60			
		-	-	GPKP75	GPKP74	GPKP73	GPKP72	GPKP71	GPKP70			
		-	-	GPKP85	GPKP84	GPKP83	GPKP82	GPKP81	GPKP80			
		-		GPKP95	GPKP94	GPKP93	GPKP92	GPKP91	GPKP90			
		-		GPKP105	GPKP104	GPKP103	GPKP102	GPKP101	GPKP100			
		GGSR P03	GGSR P02	GGSR P01	GGSR P00	GGSR P13	GGSR P12	GGSR P11	GGSR P10			
		GGSR P23	GGSR P22	GGSR P21	GGSR P20	GGSR P33	GGSR P32	GGSR P31	GGSR P30			

Table 110. Instruction code – (F7 ~ FD) (continued)

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
GNGAMCTL	R/W	0	1	1	1	1	1	0	0	0	FAh	5.3.20
		1	GGLN1	GGLN0	GRFN5	GRFN4	GRFN3	GRFN2	GRFN1	GRFN0		
		-	-	GOSN5	GOSN4	GOSN3	GOSN2	GOSN1	GOSN0			
		-	-	GPKN05	GPKN04	GPKN03	GPKN02	GPKN01	GPKN00			
		-	-	GPKN15	GPKN14	GPKN13	GPKN12	GPKN11	GPKN10			
		-	-	GPKN25	GPKN24	GPKN23	GPKN22	GPKN21	GPKN20			
		-	-	GPKN35	GPKN34	GPKN33	GPKN32	GPKN31	GPKN30			
		-	-	GPKN45	GPKN44	GPKN43	GPKN42	GPKN41	GPKN40			
		-	-	GPKN55	GPKN54	GPKN53	GPKN52	GPKN51	GPKN50			
		-	-	GPKN65	GPKN64	GPKN63	GPKN62	GPKN61	GPKN60			
		-	-	GPKN75	GPKN74	GPKN73	GPKN72	GPKN71	GPKN70			
		-	-	GPKN85	GPKN84	GPKN83	GPKN82	GPKN81	GPKN80			
		-	-	GPKN95	GPKN94	GPKN93	GPKN92	GPKN91	GPKN90			
		-	-	GPKN10	GPKN10	GPKN10	GPKN10	GPKN10	GPKN10			
		-	-	5	4	3	2	1	0			
		GGSR	GGSR	GGSR	GGSR	GGSR	GGSR	GGSR	GGSR	GGSR		
		N03	N02	N01	N00	N13	N12	N11	N11	N11		
		GGSR	GGSR	GGSR	GGSR	GGSR	GGSR	GGSR	GGSR	GGSR		
		N23	N22	N21	N20	N33	N32	N31	N31	N31		
BPGAMCTL	R/W	0	1	1	1	1	1	0	1	1	FBh	5.3.21
		1	BGLP1	BGLP0	BRFP5	BRFP4	BRFP3	BRFP2	BRFP1	BRFP0		
		-	-	BOSP5	BOSP4	BOSP3	BOSP2	BOSP1	BOSP0			
		-	-	BPKP05	BPKP04	BPKP03	BPKP02	BPKP01	BPKP00			
		-	-	BPKP15	BPKP14	BPKP13	BPKP12	BPKP11	BPKP10			
		-	-	BPKP25	BPKP24	BPKP23	BPKP22	BPKP21	BPKP20			
		-	-	BPKP35	BPKP34	BPKP33	BPKP32	BPKP31	BPKP30			
		-	-	BPKP45	BPKP44	BPKP43	BPKP42	BPKP41	BPKP40			
		-	-	BPKP55	BPKP54	BPKP53	BPKP52	BPKP51	BPKP50			
		-	-	BPKP65	BPKP64	BPKP63	BPKP62	BPKP61	BPKP60			
		-	-	BPKP75	BPKP74	BPKP73	BPKP72	BPKP71	BPKP70			
		-	-	BPKP85	BPKP84	BPKP83	BPKP82	BPKP81	BPKP80			
		-	-	BPKP95	BPKP94	BPKP93	BPKP92	BPKP91	BPKP90			
		-	-	BPKP10	BPKP10	BPKP10	BPKP10	BPKP10	BPKP10			
		-	-	5	4	3	2	1	0			

Instruction	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Reference
			BGSR P03	BGSR P02	BGSR P01	BGSR P00	BGRS P13	BGRS P12	BGRS P11	BGRS P10		
			BGSR P23	BGSR P22	BGSR P21	BGSR P20	BGRS P33	BGRS P32	BGRS P31	BGRS P30		
		0	1	1	1	1	1	1	0	0	FCh	
BNGAMCTL	R/W	1	BGLN1	BGLN0	BRFN5	BRFN4	BRFN3	BRFN2	BRFN1	BRFN0		5.3.22
			-	-	BOSN5	BOSN4	BOSN3	BOSN2	BOSN1	BOSN0		
			-	-	BPKN05	BPKN04	BPKN03	BPKN02	BPKN01	BPKN00		
			-	-	BPKN15	BPKN14	BPKN13	BPKN12	BPKN11	BPKN10		
			-	-	BPKN25	BPKN24	BPKN23	BPKN22	BPKN21	BPKN20		
			-	-	BPKN35	BPKN34	BPKN33	BPKN32	BPKN31	BPKN30		
			-	-	BPKN45	BPKN44	BPKN43	BPKN42	BPKN41	BPKN40		
			-	-	BPKN55	BPKN54	BPKN53	BPKN52	BPKN51	BPKN50		
			-	-	BPKN65	BPKN64	BPKN63	BPKN62	BPKN61	BPKN60		
			-	-	BPKN75	BPKN74	BPKN73	BPKN72	BPKN71	BPKN70		
			-	-	BPKN85	BPKN84	BPKN83	BPKN82	BPKN81	BPKN80		
			-	-	BPKN95	BPKN94	BPKN93	BPKN92	BPKN91	BPKN90		
			-	-	BPKN10	BPKN10	BPKN10	BPKN10	BPKN10	BPKN10		
					5	4	3	2	1	0		
			BGRS N03	BGRS N02	BGRS N01	BGRS N00	BGRS N13	BGRS N12	BGRS N11	BGRS N11		
			BGRS N23	BGRS N22	BGRS N21	BGRS N20	BGRS N33	BGRS N32	BGRS N31	BGRS N31		
GATECTL	R/W	0	1	1	1	1	1	1	0	1	FDh	5.3.23
		1	-	IPNO2	IPNO1	IPNO0	-	NNO2	NNO1	NNO0		
EDSTEST	R/W	0	1	1	1	1	1	1	0	1	FFh	5.3.24
		1	-	-	0	0	0	0	0	0		
			-	-	0	0	0	0	0	0		
			-	-	0	0	0	0	0	0		
			-	SD_EN	SD1	SD2	SD3	0	0	0		
			-	-	0	0	0	0	0	0		

Note1: For Level1 and Level 2 register read action, in case of 80 MCU Interface mode, 1-byte Dummy Read will be needed.

Note2: Level 2 registers are not readable in SPI mode.



## 5.2. DESCRIPTION OF LEVEL1 COMMAND

### 5.2.1. NOP (00h)

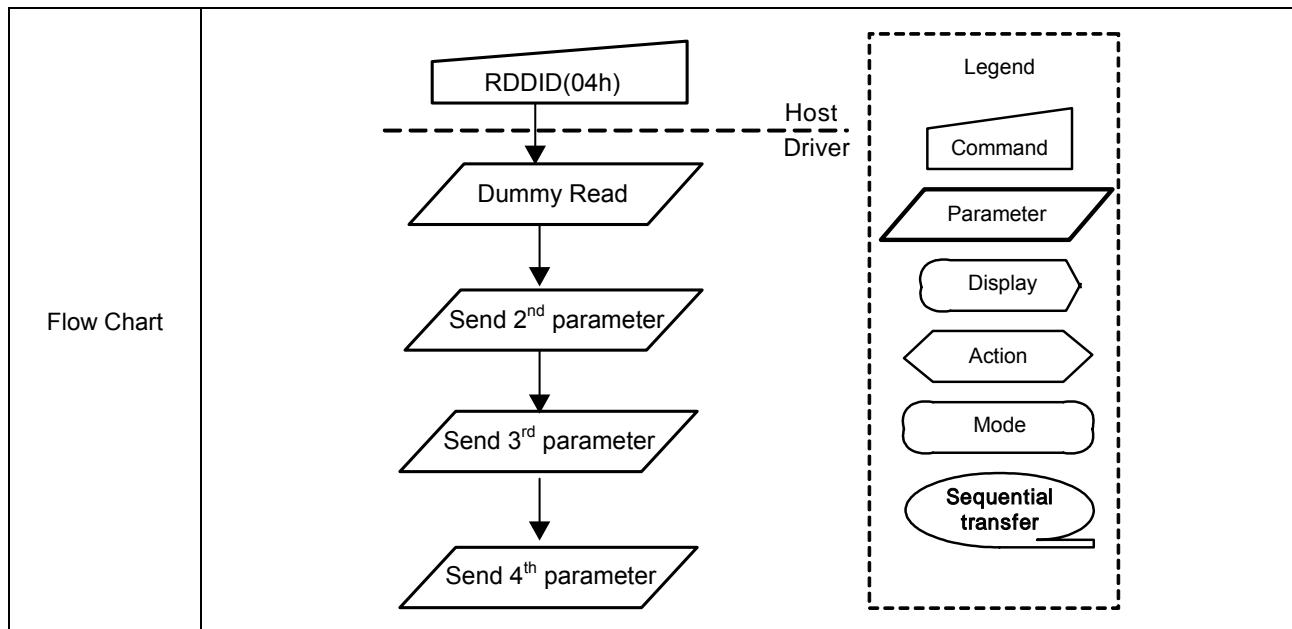
Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
NOP	W	0	0	0	0	0	0	0	0	0	00h	
Parameter	No Parameter											
Description	<p>This is a null command. It does not have any effect on the display module.</p> <p>However it can be used to terminate the write/read operation of RAM data as described in RAMWR (Memory Write), RAMRD (Memory Read) and parameter write commands.</p>											
Restriction	-											
Register Availability	<b>Status</b>		<b>Availability</b>									
	Normal Mode On, Idle Mode Off, Sleep Out		Yes									
	Normal Mode On, Idle Mode On, Sleep Out		Yes									
	Partial Mode On, Idle Mode Off, Sleep Out		Yes									
	Partial Mode On, Idle Mode On, Sleep Out		Yes									
	Sleep In		Yes									
Default	<b>Status</b>		<b>Default Value</b>									
	Power On Sequence		N/A									
	S/W Reset		N/A									
	H/W Reset		N/A									

## 5.2.2. SWRESET: Software Reset (01h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
SWRESET	W	0	0	0	0	0	0	0	0	1	01h												
Parameter	No Parameter																						
Description	<p>The Software Reset command resets the commands and parameters to their S/W Reset default values, and all the source &amp; gate outputs are set to VSS (display off). (See default tables in each command description)</p> <p>Note: The Frame Memory contents are not affected by this command</p>																						
Restriction	<p>It is necessary to wait for 5msec before sending new commands following the software reset.</p> <p>The display module loads all of display supplier's factory default values to the registers during 5msec.</p> <p>If Software Reset is applied during Sleep Out mode, it is necessary to wait 120msec before sending Sleep Out command.</p> <p>Software Reset command cannot be sent during Sleep Out sequence.</p>																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
Status	Default Value																						
Power On Sequence	N/A																						
S/W Reset	N/A																						
H/W Reset	N/A																						
Flow Chart	<pre> graph TD     SWRESET[SWRESET] --&gt; Blank[Display whole blank screen]     Blank --&gt; Set[Set Commands to S/W Default Value]     Set --&gt; SleepIn[Sleep In Mode]     </pre> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																						

## 5.2.3. RDDIDIF: Read Display ID (04h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
RDDIDIF	R	0	0	0	0	0	0	1	0	0	04h																			
Dummy Read		1	X	X	X	X	X	X	X	X	X																			
2 <sup>nd</sup> parameter		1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	xx																			
3 <sup>rd</sup> parameter		1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	xx																			
4 <sup>th</sup> parameter		1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	xx																			
Description	<p>This read command returns 24-bit display identification information.</p> <p>The 1<sup>st</sup> parameter is dummy data.</p> <p>The 2<sup>nd</sup> parameter identifies the LCD module's manufacturers. It is specified by a user.</p> <p>The 3<sup>rd</sup> parameter has 2 purposes. Bit7(MSB) defines the type of a panel. 0=Driver (STN B/W), 1=Module(Color). Bit 6..0 are used to track the LCD module/driver version. It is defined by a panel supplier and updated each time; a version of the display is updated.</p> <p>The 4<sup>th</sup> parameter identifies the LCD module/driver. It is specified by a user.</p> <p>Note.</p> <p>Commands RDID1/2/3(DAh, DBh, DCh) reads data corresponding to the parameters 2, 3, 4 of the command 04h, respectively.</p> <p>"X" denotes "Don't care"</p>																													
Restriction	-																													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																													
Normal Mode On, Idle Mode Off, Sleep Out	Yes																													
Normal Mode On, Idle Mode On, Sleep Out	Yes																													
Partial Mode On, Idle Mode Off, Sleep Out	Yes																													
Partial Mode On, Idle Mode On, Sleep Out	Yes																													
Sleep In	Yes																													
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th><th colspan="3">Default Value</th></tr> <tr> <th>ID1</th><th>ID2</th><th>ID3</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>(MTP value)</td><td>(MTP value)</td><td>(MTP value)</td></tr> <tr> <td>S/W Reset</td><td>(MTP value)</td><td>(MTP value)</td><td>(MTP value)</td></tr> <tr> <td>H/W Reset</td><td>(MTP value)</td><td>(MTP value)</td><td>(MTP value)</td></tr> </tbody> </table>											Status	Default Value			ID1	ID2	ID3	Power On Sequence	(MTP value)	(MTP value)	(MTP value)	S/W Reset	(MTP value)	(MTP value)	(MTP value)	H/W Reset	(MTP value)	(MTP value)	(MTP value)
Status	Default Value																													
	ID1	ID2	ID3																											
Power On Sequence	(MTP value)	(MTP value)	(MTP value)																											
S/W Reset	(MTP value)	(MTP value)	(MTP value)																											
H/W Reset	(MTP value)	(MTP value)	(MTP value)																											



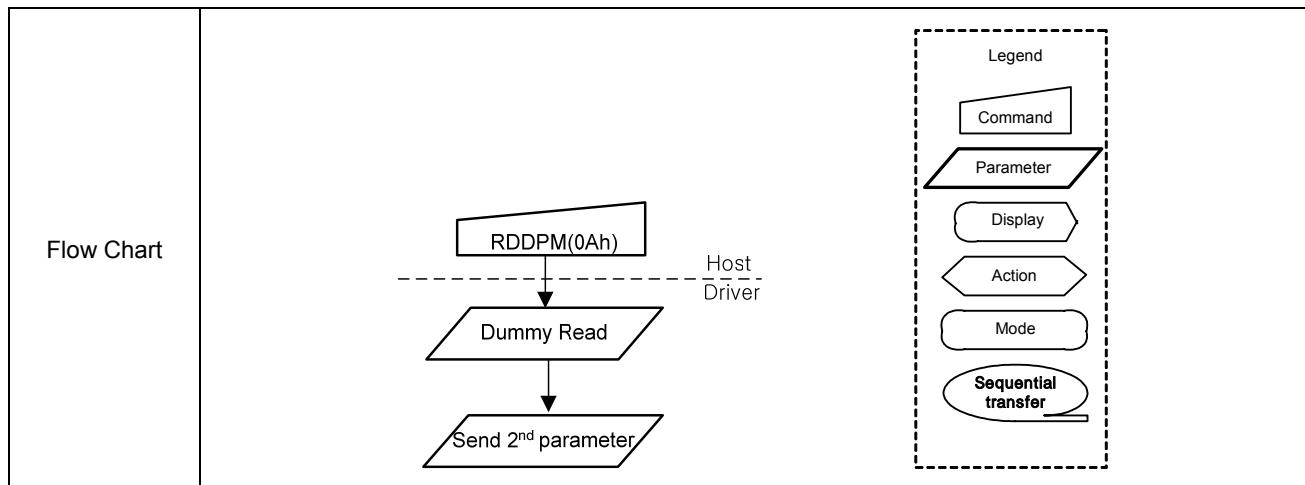
## 5.2.4. RDDST: Read Display Status (09h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDST	R	0	0	0	0	0	1	0	0	1	09h
Dummy Read		1	X	X	X	X	X	X	X	X	X
2 <sup>nd</sup> parameter		1	D31	D30	D29	D28	D27	D26	D25	0	xx
3 <sup>rd</sup> parameter		1	0	D22	D21	D20	D19	D18	D17	D16	xx
4 <sup>th</sup> parameter		1	0	0	0	0	0	D10	D9	D8	xx
5 <sup>th</sup> parameter		1	D7	D6	D5	0	0	0	0	0	xx
This command indicates the current status of the display as described in the table below:											
Description	Bit	Description				Value					
	D31	Booster Voltage Status				“1”=Booster on, “0”=off					
	D30	Page Address Order (MY)				“1”=Decrement, “0”=Increment					
	D29	Column Address Order (MX)				“1”=Decrement, “0”=Increment					
	D28	Page/Column Exchange (MV)				“1”= Page/column exchange (MV=1), “0”= Normal (MV=0)					
	D27	Vertical Refresh Order (ML)				“1”=Decrement, “0”=Increment					
	D26	RGB/BGR Order (RGB)				“1”=BGR, “0”=RGB					
	D25	Display Data Latch Order(MH)				Refer to MADCTL					
	D24	Not Used				“0”					
	D23	Not Used				“0”					
	D22	Interface Color Pixel Format Definition (IFPF)				“101”=16-bits/pixel					
	D21					“110”=18-bits/pixel					
	D20					“111”= 24-bits/pixel					
	D19	Idle Mode On/Off				“1” = On, “0” = Off					
	D18	Partial Mode On/Off				“1” = On, “0” = Off					
	D17	Sleep In/Out				“1” = Out, “0” = In					
	D16	Display Normal Mode On/Off				“1” = Normal Display, “0” = Partial Display					
	D15	Not Used				“0”					
	D14	Not Used				“0”					
	D13	Not Used				“0”					
	D12	Not Used				“0”					
	D11	Not Used				“0”					
	D10	Display On/Off				“1” = On, “0” = Off					
	D9	Tearing effect line on/off				“1” = On, “0” = Off					

	D8~D6	Gamma Curve Selection	"000" = GC0 "001" = GC1 "010" = GC2 "011" = GC3 "100" to "111" = Not defined
	D5	Tearing effect line mode	"0" = mode1, V_Blanking only "1" = mode2, Both H & V-Blanking.
	D4	Not Used	"0"
	D3	Not Used	"0"
	D2	Not Used	"0"
	D1	Not Used	"0"
	D0	Not Used	"0"
Note: "X" denotes "Don't care"			
Restriction	-		
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value (D31 to D0)	
	Power On Sequence	0000_0000_0111_0001_0000_0000_0000_0000	
	S/W Reset	0xxx_xxx0_0xxx_0001_0000_0000_0000_0000	
	H/W Reset	0000_0000_0111_0001_0000_0000_0000_0000	
Flow Chart	<pre> graph TD     RDDST[RDDST(09h)] --&gt; DR[Dummy Read]     DR --&gt; S2[Send 2nd parameter]     S2 --&gt; S3[Send 3rd parameter]     S3 --&gt; S4[Send 4th parameter]     S4 --&gt; S5[Send 5th parameter]   </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>		

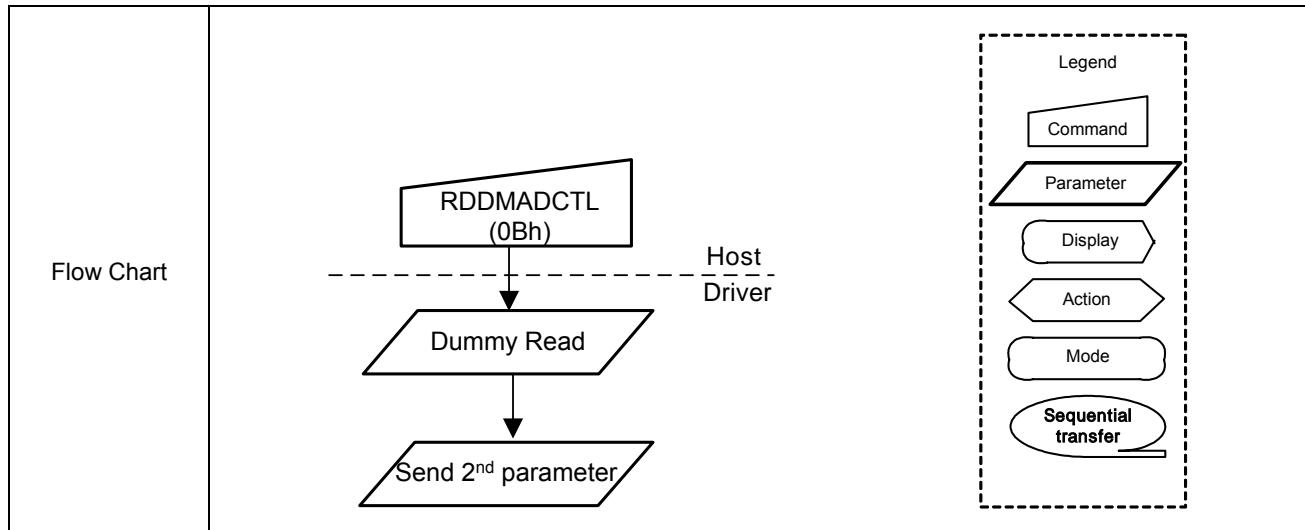
## 5.2.5. RDDPM: Read Display Power Mode (0Ah)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX										
RDDPM	R	0	0	0	0	0	1	0	1	0	0Ah										
Dummy Read		1	X	X	X	X	X	X	X	X	X										
2 <sup>nd</sup> parameter		1	D7	D6	D5	D4	D3	D2	0	0	xx										
This command indicates the current status of the display as described in the table below:																					
Description	Bit	Description				Value															
	D7	Booster Voltage Status				“1”=Booster on, “0”=off															
	D6	Idle Mode On/Off				“1” = Idle Mode On, “0”= idle Mode Off															
	D5	Partial Mode On/Off				“1” = Partial Mode On, “0” = Partial Mode Off															
	D4	Sleep In/Out				“1” = Sleep Out, “0” = Sleep In															
	D3	Display Normal Mode On/Off				“1” = Normal Display, “0” = Partial Display															
	D2	Display On/Off				“1” = Display On, “0” = Display Off															
	D1	Not Used				“0”															
	D0	Not Used				“0”															
Note: “X” denotes “Don’t care”																					
Restriction	-																				
Register Availability	Status	Availability																			
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																			
	Normal Mode On, Idle Mode On, Sleep Out	Yes																			
	Partial Mode On, Idle Mode Off, Sleep Out	Yes																			
	Partial Mode On, Idle Mode On, Sleep Out	Yes																			
Default	Sleep In	Yes																			
	Status	Default Value (D7 to D0)																			
	Power On Sequence	0000_1000 (08h)																			
	S/W Reset	0000_1000 (08h)																			
	H/W Reset	0000_1000 (08h)																			



## 5.2.6. RDDMADCTL: Read Display MADCTL (0Bh)

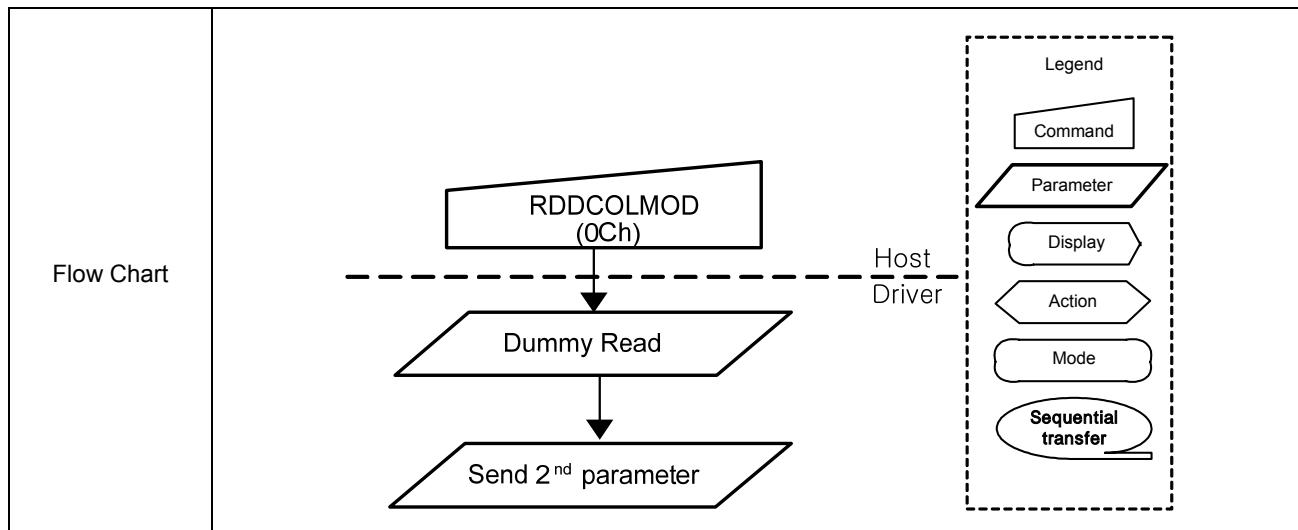
Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX										
RDDMADCTL	R	0	0	0	0	0	1	0	1	1	0Bh										
Dummy Read		1	X	X	X	X	X	X	X	X	X										
2 <sup>nd</sup> parameter		1	D7	D6	D5	D4	D3	D2	0	0	xx										
		This command indicates the current status of the display MADCTL(memory address control) as described in the table below:																			
Description	Bit	Description				Value															
	D7	Page Address Order				“1”=Decrement, “0”=Increment															
	D6	Column Address Order				“1”=Decrement, “0”=Increment															
	D5	Page/Column Order (MV)				“1”= Page/column exchange (MV=1) “0”= Normal (MV=0)															
	D4	Vertical fresh Order (ML)				“1”=Decrement, “0”=Increment															
	D3	RGB/BGR Order(RGB)				“1”=BGR, “0”=RGB															
	D2	Display Data Latch Order(MH)				Refer to MADCTL															
	D1	Not Used				“0”															
	D0	Not Used				“0”															
Note: “X” denotes “Don’t care”																					
Restriction	D2 is Read/Write Register Only, It is not active Function.																				
Register Availability	Status						Availability														
	Normal Mode On, Idle Mode Off, Sleep Out						Yes														
	Normal Mode On, Idle Mode On, Sleep Out						Yes														
	Partial Mode On, Idle Mode Off, Sleep Out						Yes														
	Partial Mode On, Idle Mode On, Sleep Out						Yes														
	Sleep In						Yes														
Default	Status						Default Value (D7 to D0)														
	Power On Sequence						0000_0000 (00h)														
	S/W Reset						No change														
	H/W Reset						0000_0000 (00h)														



## 5.2.7. RDDCOLMOD: Read Display Pixel Format (0Ch)

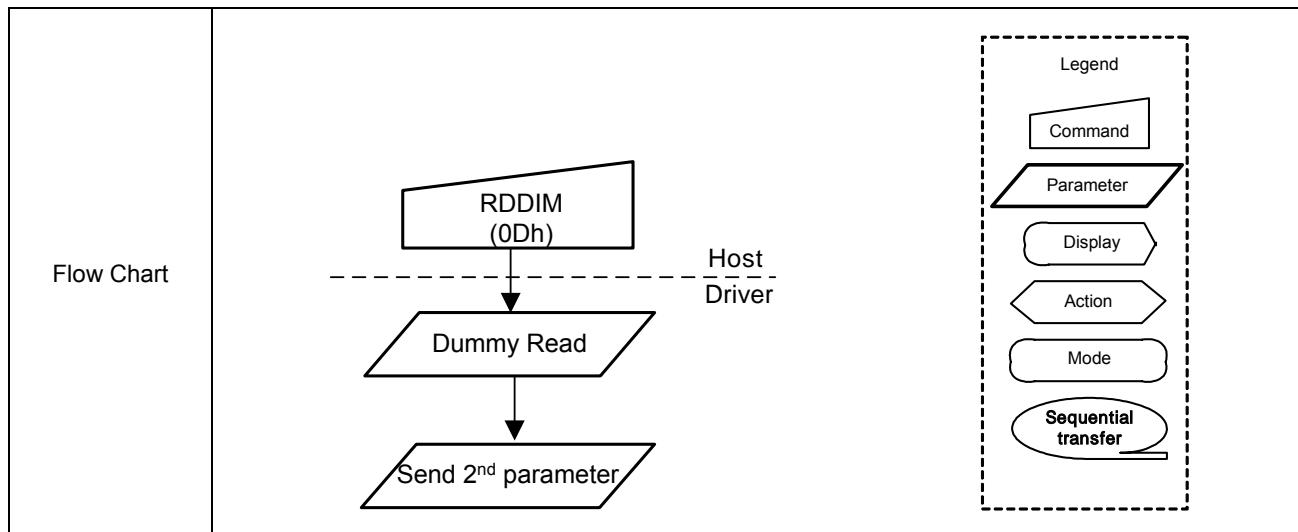
Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																
RDDCOLMOD	R	0	0	0	0	0	1	1	0	0	0Ch																
Dummy Read		1	X	X	X	X	X	X	X	X	X																
2 <sup>nd</sup> parameter		1	0	D6	D5	D4	0	D2	D1	D0	xx																
		This command indicates the current status of the display as described in the table below:																									
Description	Bit	Description				Value																					
	D7	-				"0" (Not Used)																					
	D6	Control RGB Interface Color Format (VFPF)				"101"=16-bits/pixel																					
	D5					"110"=18-bits/pixel																					
	D4					"111"= 24-bits/pixel																					
	D3	-				Others = not defined																					
	D2	Control MPU Interface Color Format (IFPF)				"101"=16-bits/pixel																					
	D1					"110"=18-bits/pixel																					
	D0					"111"= 24-bits/pixel																					
		Others = not defined																									
<p>Bit D7: Set to '0'.</p> <p>Bit D6~4 : Control RGB Interface Color Pixel Format Definition.</p> <p>Bit D3 : Set to '0'.</p> <p>Bit D2~0 : Control MPU Interface Color Pixel Format Definition.</p> <p>Note: "X" denotes "Don't care"</p>																											
Restriction	-																										
Register Availability			Status			Availability																					
			Normal Mode On, Idle Mode Off, Sleep Out			Yes																					
			Normal Mode On, Idle Mode On, Sleep Out			Yes																					
			Partial Mode On, Idle Mode Off, Sleep Out			Yes																					
			Partial Mode On, Idle Mode On, Sleep Out			Yes																					
			Sleep In			Yes																					
Default			Status			Default Value (D7 to D0)																					
			Power On Sequence			0111_0111 (77h)																					
			S/W Reset			No change																					
			H/W Reset			0111_0111 (77h)																					





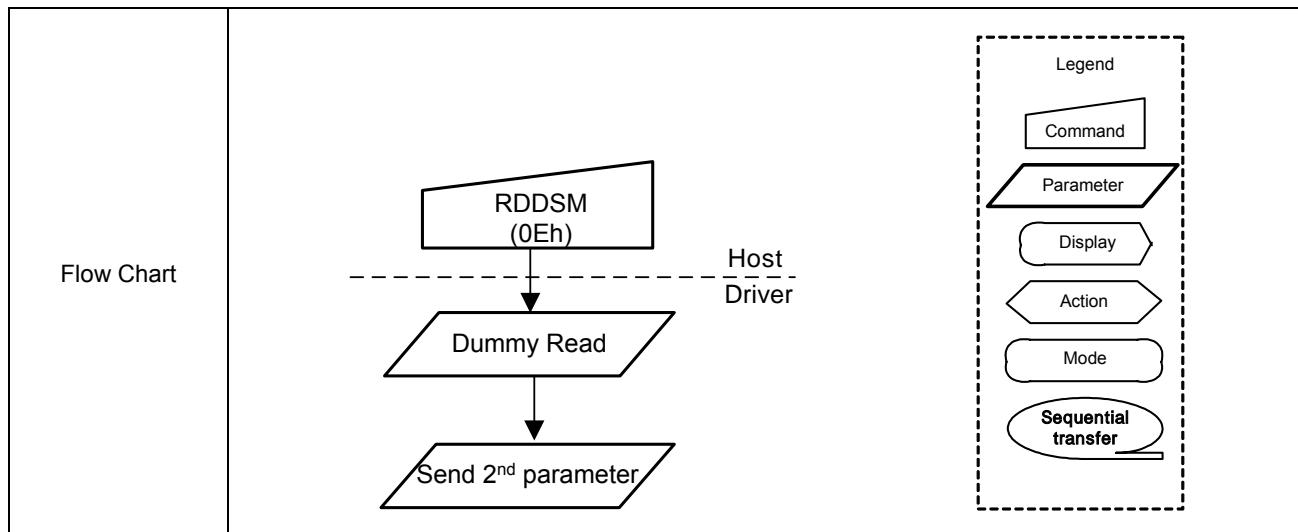
## 5.2.8. RDDIM: Read Display Image Mode (0Dh)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
RDDIM	R	0	0	0	0	0	1	1	0	1	0Dh																			
Dummy Read		1	X	X	X	X	X	X	X	X	X																			
2 <sup>nd</sup> parameter		1	0	0	0	0	0	D2	D1	D0	xx																			
Description		This command indicates the current status of the display image mode as described in the table below:																												
		Bit	Description			Value																								
		D7	Not Used			“0”																								
		D6	Not Used			“0”																								
		D5	Not Used			“0”																								
		D4	Not Used			“0”																								
		D3	Not Used			“0”																								
		D2	Gamma Curve Selection			“000” = GC0																								
		D1				“001” = GC1																								
		D0				“010” = GC2																								
		“011” = GC3 ”100” to “111” = Not defined																												
Note: “X” denotes “Don’t care”																														
Restriction	-																													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																													
Normal Mode On, Idle Mode Off, Sleep Out	Yes																													
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Partial Mode On, Idle Mode On, Sleep Out	Yes																													
Sleep In	Yes																													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value (D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0000_0000 (00h)</td> </tr> <tr> <td>S/W Reset</td> <td>0000_0000 (00h)</td> </tr> <tr> <td>H/W Reset</td> <td>0000_0000 (00h)</td> </tr> </tbody> </table>											Status	Default Value (D7 to D0)	Power On Sequence	0000_0000 (00h)	S/W Reset	0000_0000 (00h)	H/W Reset	0000_0000 (00h)											
Status	Default Value (D7 to D0)																													
Power On Sequence	0000_0000 (00h)																													
S/W Reset	0000_0000 (00h)																													
H/W Reset	0000_0000 (00h)																													



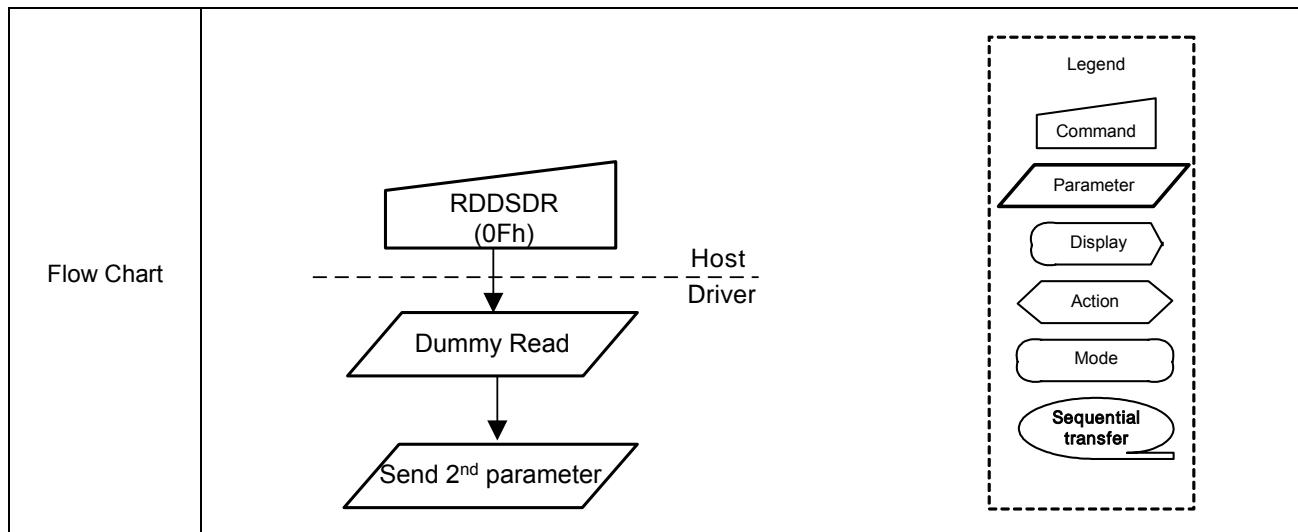
## 5.2.9. RDDSM: Read Display Signal Mode (0Eh)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
RDDSM	R	0	0	0	0	0	1	1	1	0	0Eh								
Dummy Read		1	X	X	X	X	X	X	X	X	X								
2 <sup>nd</sup> parameter		1	D7	D6	0	0	0	0	0	0	xx								
Description		This command indicates the current status of the display signal mode as described in the table below:																	
		<b>Bit</b>	<b>Description</b>			<b>Value</b>													
		D7	Tearing Effect Line On/Off			“1” = On, “0” = Off													
		D6	Tearing effect line mode			“0” = Mode1 “1” = Mode2													
		D5	Not Used			“0”													
		D4	Not Used			“0”													
		D3	Not Used			“0”													
		D2	Not Used			“0”													
		D1	Not Used			“0”													
		D0	Not Used			“0”													
		Note: “X” denotes “Don’t care”																	
Restriction	-																		
Register Availability			<b>Status</b>				<b>Availability</b>												
			Normal Mode On, Idle Mode Off, Sleep Out				Yes												
			Normal Mode On, Idle Mode On, Sleep Out				Yes												
			Partial Mode On, Idle Mode Off, Sleep Out				Yes												
			Partial Mode On, Idle Mode On, Sleep Out				Yes												
			Sleep In				Yes												
Default			<b>Status</b>				<b>Default Value (D7 to D0)</b>												
			Power On Sequence				0000_0000 (00h)												
			S/W Reset				0000_0000 (00h)												
			H/W Reset				0000_0000 (00h)												

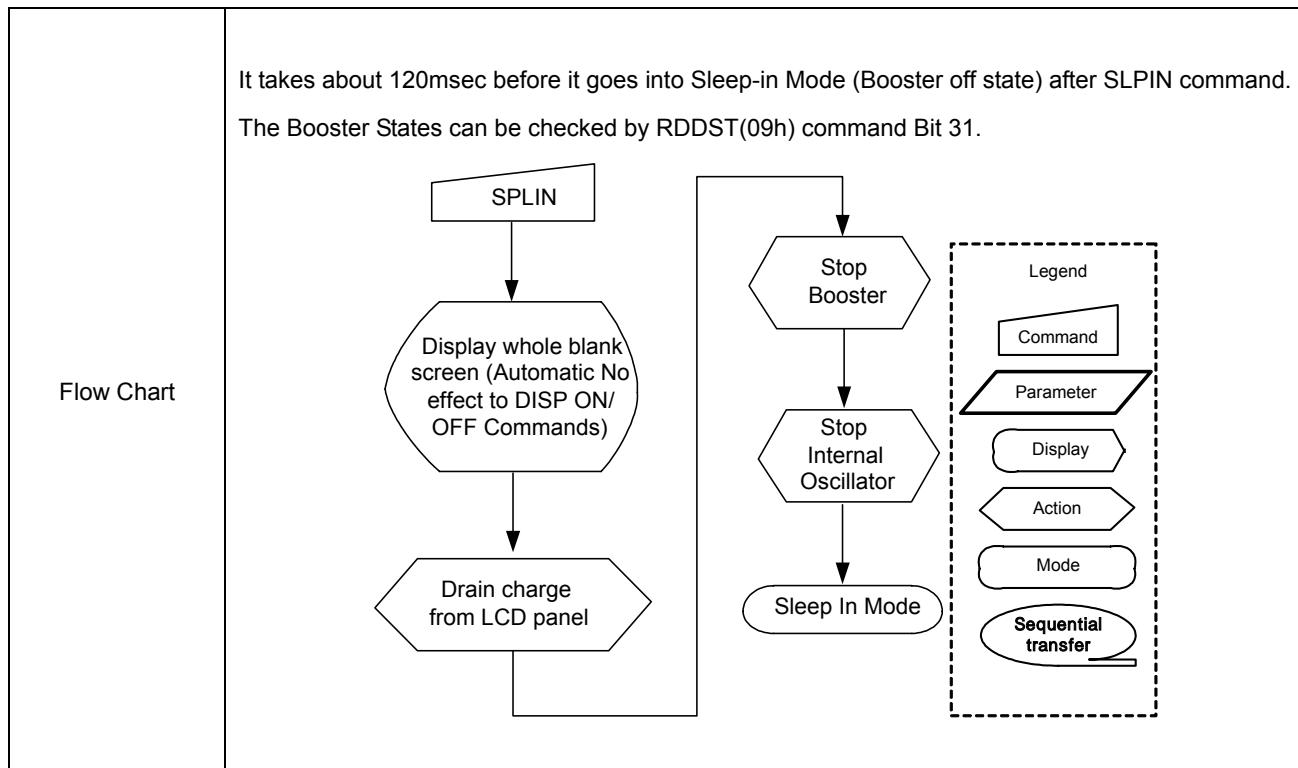


## 5.2.10. RDDSDR: Read Display Self-Diagnostic Result (0Fh)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																									
RDDSDR	R	0	0	0	0	0	1	1	1	1	0Fh																									
Dummy Read		1	X	X	X	X	X	X	X	X	X																									
2 <sup>nd</sup> parameter		1	D7	D6	0	0	0	0	0	0	xx																									
This command indicates the current status of the display self-diagnostics as described in the table below:																																				
Description	<table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Value</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Register Loading Detection</td><td rowspan="2">See section 4.7</td></tr> <tr> <td>D6</td><td>Functionality Detection</td></tr> <tr> <td>D5</td><td>Not Used</td><td>"0"</td></tr> <tr> <td>D4</td><td>Not Used</td><td>"0"</td></tr> <tr> <td>D3</td><td>Not Used</td><td>"0"</td></tr> <tr> <td>D2</td><td>Not Used</td><td>"0"</td></tr> <tr> <td>D1</td><td>Not Used</td><td>"0"</td></tr> <tr> <td>D0</td><td>Not Used</td><td>"0"</td></tr> </tbody> </table>										Bit	Description	Value	D7	Register Loading Detection	See section 4.7	D6	Functionality Detection	D5	Not Used	"0"	D4	Not Used	"0"	D3	Not Used	"0"	D2	Not Used	"0"	D1	Not Used	"0"	D0	Not Used	"0"
Bit	Description	Value																																		
D7	Register Loading Detection	See section 4.7																																		
D6	Functionality Detection																																			
D5	Not Used	"0"																																		
D4	Not Used	"0"																																		
D3	Not Used	"0"																																		
D2	Not Used	"0"																																		
D1	Not Used	"0"																																		
D0	Not Used	"0"																																		
Note: "X" denotes "Don't care"																																				
Restriction	-																																			
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes													
Status	Availability																																			
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																			
Normal Mode On, Idle Mode On, Sleep Out	Yes																																			
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																			
Partial Mode On, Idle Mode On, Sleep Out	Yes																																			
Sleep In	Yes																																			
<table border="1"> <thead> <tr> <th>Status</th><th>Default Value (D7 to D0)</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>0000_0000 (00h)</td></tr> <tr> <td>S/W Reset</td><td>0000_0000 (00h)</td></tr> <tr> <td>H/W Reset</td><td>0000_0000 (00h)</td></tr> </tbody> </table>											Status	Default Value (D7 to D0)	Power On Sequence	0000_0000 (00h)	S/W Reset	0000_0000 (00h)	H/W Reset	0000_0000 (00h)																		
Status	Default Value (D7 to D0)																																			
Power On Sequence	0000_0000 (00h)																																			
S/W Reset	0000_0000 (00h)																																			
H/W Reset	0000_0000 (00h)																																			



### **5.2.11. SLPIN: Sleep In (10h)**



### 5.2.12. SLPOUT: Sleep Out (11h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
SLPOUT	W	0	0	0	0	1	0	0	0	1	11h												
Parameter	No Parameter																						
Description	<p>This command turns off the sleep mode.</p> <p>During this mode, the Booster, the Internal display oscillator, and panel scanning are in normal operation.</p>																						
Restriction	<p>This command has no effect when the module is already in sleep out mode. Sleep Out Mode can only exit by the Sleep In Command (10h).</p> <p>It is necessary to wait for 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.</p> <p>S6D04M0 loads the default values of extended and test commands to the registers during this 5msec duration. There cannot be any abnormal visual effect on the display image if those default and register values are the same when this loading is done and when the S6D04M0 is already in Sleep Out –mode.</p> <p>S6D04M0 performs self-diagnostic during this 5msec. See also section 4.7. It is necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</p>																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						

	Status	Default Value
Default	Power On Sequence	Sleep in mode
	S/W Reset	Sleep in mode
	H/W Reset	Sleep in mode

Flow Chart	<p>It takes 120msec to be in Sleep Out mode (booster on mode) after SLOUT command is issued.</p> <p>The booster on status can be checked by RDDST (09h) command Bit31.</p> <pre> graph TD     S[SLOUT] --&gt; O1{Start Internal Oscillator}     O1 --&gt; O2{Strat Booster}     O2 --&gt; O3{Charge Offset voltage for LCD Panel}     O3 --&gt; D1{Display whole blank screen for 2 frames Automatic No effect to DISP ON/OFF Commands}     D1 --&gt; D2{Display Memory contents in accordance with the current command table settings}     D2 --&gt; S2{Sleep Out Mode}     </pre> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>
------------	--

## 5.2.13. PTLON: Partial Display Mode On (12h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
PTLON	W	0	0	0	0	1	0	0	1	0	12h												
Parameter	No Parameter																						
Description	<p>This command turns on Partial mode. The partial mode window is described by the Partial Area command (30H).</p> <p>To leave Partial mode, the Normal Display Mode On command (13H) should be written.</p> <p>There is no abnormal visual effect during mode change between Normal mode On and Partial mode On.</p>																						
Restriction	This command has no effect when Partial mode is active.																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Mode On</td> </tr> <tr> <td>S/W Reset</td> <td>Normal Mode On</td> </tr> <tr> <td>H/W Reset</td> <td>Normal Mode On</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	Normal Mode On	S/W Reset	Normal Mode On	H/W Reset	Normal Mode On				
Status	Default Value																						
Power On Sequence	Normal Mode On																						
S/W Reset	Normal Mode On																						
H/W Reset	Normal Mode On																						
Flow Chart	See Partial Area (30h)																						

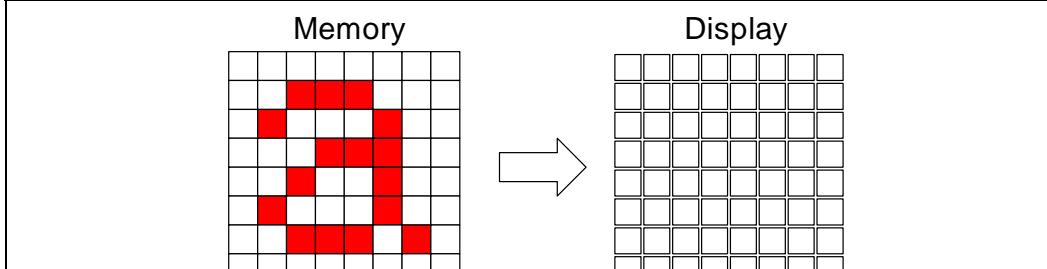
## 5.2.14. NORON: Normal Display Mode On (13h)

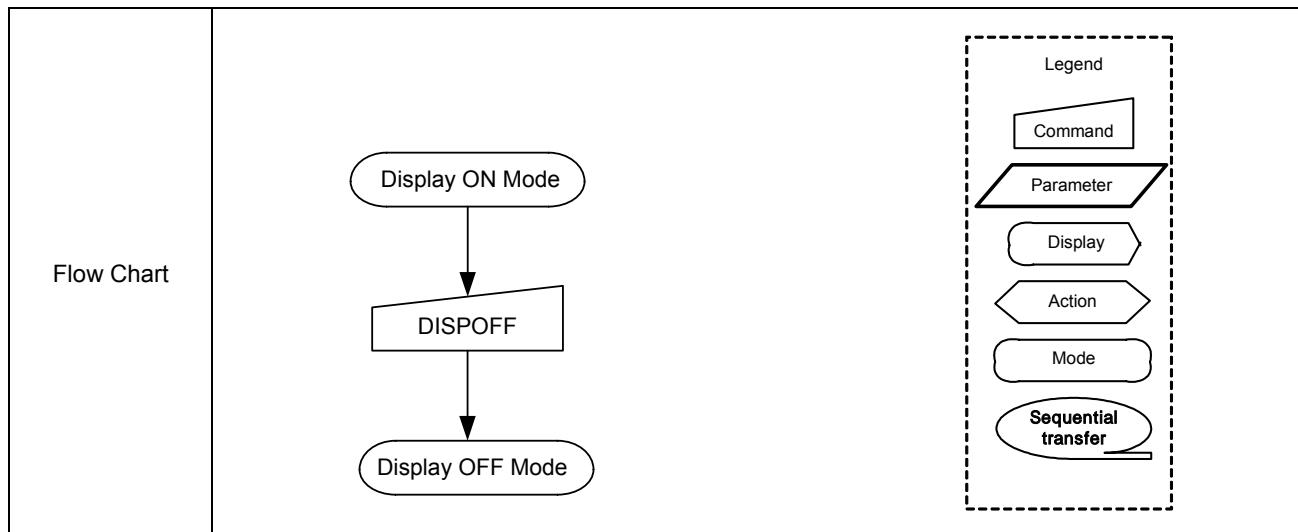
Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
NORON	W	0	0	0	0	1	0	0	1	1	13h												
Parameter	No Parameter																						
Description	<p>This command returns the display to normal mode.</p> <p>Turning normal display mode on means Partial mode off.</p> <p>Exiting from NORON can be done by the Partial mode On command (12h).</p> <p>There is no abnormal visual effect during the mode change from Normal mode On to Partial mode On.</p>																						
Restriction	This command has no effect when Normal Display mode is active.																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Mode On</td> </tr> <tr> <td>S/W Reset</td> <td>Normal Mode On</td> </tr> <tr> <td>H/W Reset</td> <td>Normal Mode On</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	Normal Mode On	S/W Reset	Normal Mode On	H/W Reset	Normal Mode On				
Status	Default Value																						
Power On Sequence	Normal Mode On																						
S/W Reset	Normal Mode On																						
H/W Reset	Normal Mode On																						
Flow Chart	See Partial Area for details of when to use this command.																						

## 5.2.15. GAMSET: Gamma Set (26h)

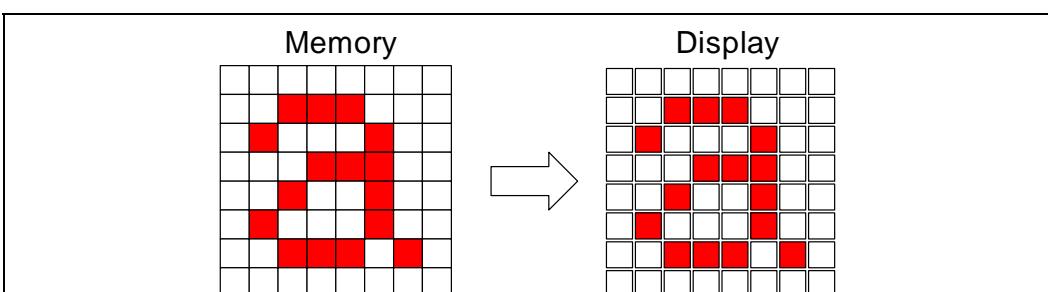
Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
GAMSET	W	0	0	0	1	0	0	1	1	0	26h															
Parameter		1	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	1~8h															
Description	This command is used to select the desired Gamma curve for the current display. One of 4 available curves can be selected. The curves are defined in section 4.2.3 The curve is selected by setting the appropriate bit in the parameter as described in the Table.																									
	<table border="1"> <thead> <tr> <th>GC[7:0]</th><th>Parameter</th><th>Curve Selected</th></tr> </thead> <tbody> <tr> <td>01h</td><td>GC0</td><td>Gamma Curve 1</td></tr> <tr> <td>02h</td><td>GC1</td><td>Gamma Curve 2</td></tr> <tr> <td>04h</td><td>GC2</td><td>Gamma Curve 3</td></tr> <tr> <td>08h</td><td>GC3</td><td>Gamma Curve 4</td></tr> </tbody> </table>				GC[7:0]	Parameter	Curve Selected	01h	GC0	Gamma Curve 1	02h	GC1	Gamma Curve 2	04h	GC2	Gamma Curve 3	08h	GC3	Gamma Curve 4	Note: All other values are not defined						
GC[7:0]	Parameter	Curve Selected																								
01h	GC0	Gamma Curve 1																								
02h	GC1	Gamma Curve 2																								
04h	GC2	Gamma Curve 3																								
08h	GC3	Gamma Curve 4																								
Restriction	Any value of GC [7:0] not specified in the table above are invalid and will not change the current selected Gamma curve until valid value is received.																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes			
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>01h</td></tr> <tr> <td>S/W Reset</td><td>01h</td></tr> <tr> <td>H/W Reset</td><td>01h</td></tr> </tbody> </table>											Status	Default Value	Power On Sequence	01h	S/W Reset	01h	H/W Reset	01h							
Status	Default Value																									
Power On Sequence	01h																									
S/W Reset	01h																									
H/W Reset	01h																									
Flow Chart	<pre> graph TD     GAMSET[GAMSET] --&gt; GC7[GC[7:0]]     GC7 --&gt; NewGamma[New Gamma Curve Loaded]     </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																									

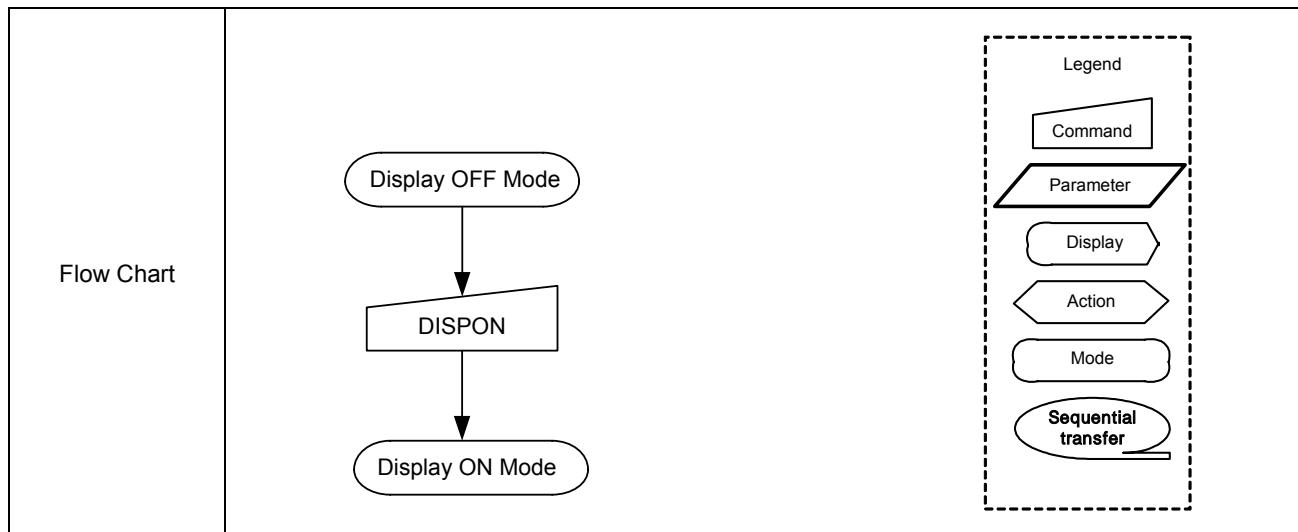
## 5.2.16. DISPOFF: Display Off (28h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
DISPOFF	W	0	0	0	1	0	1	0	0	0	28h												
Parameter	No Parameter																						
Description	<p>This command turns on DISPLAY OFF mode. During this mode, the output from the Frame Memory is disabled and blank page is inserted.</p> <p>This command makes no change to the contents of frame memory.</p> <p>This command does not alter any other status.</p> <p>There will be no abnormal visible effect on the display.</p> <p>Exiting from this command can be done by Display On (29h)</p> <p>(Example)</p> 																						
Restriction	This command has no effect when module is already in Display Off mode.																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
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Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display off</td> </tr> <tr> <td>S/W Reset</td> <td>Display off</td> </tr> <tr> <td>H/W Reset</td> <td>Display off</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off				
Status	Default Value																						
Power On Sequence	Display off																						
S/W Reset	Display off																						
H/W Reset	Display off																						

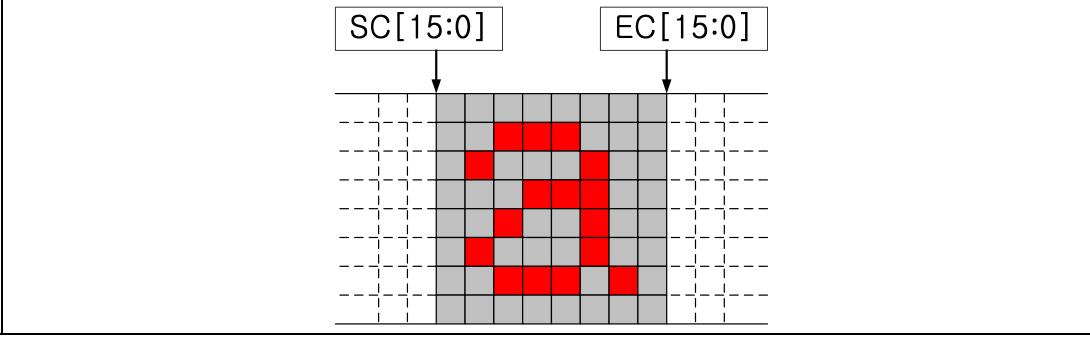


## 5.2.17. DISPON: Display On (29h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
DISPON	W	0	0	0	1	0	1	0	0	1	29h												
Parameter	No Parameter																						
Description	<p>This command enables DISPLAY ON mode. Output from the Frame Memory is enabled.</p> <p>This command makes no change to the contents of frame memory.</p> <p>This command does not alter any other status.</p> <p>(Example)</p> 																						
Restriction	This command has no effect when the module is already in Display On mode.																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display off</td> </tr> <tr> <td>S/W Reset</td> <td>Display off</td> </tr> <tr> <td>H/W Reset</td> <td>Display off</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off				
Status	Default Value																						
Power On Sequence	Display off																						
S/W Reset	Display off																						
H/W Reset	Display off																						



## 5.2.18. CASET: Column Address Set (2Ah)

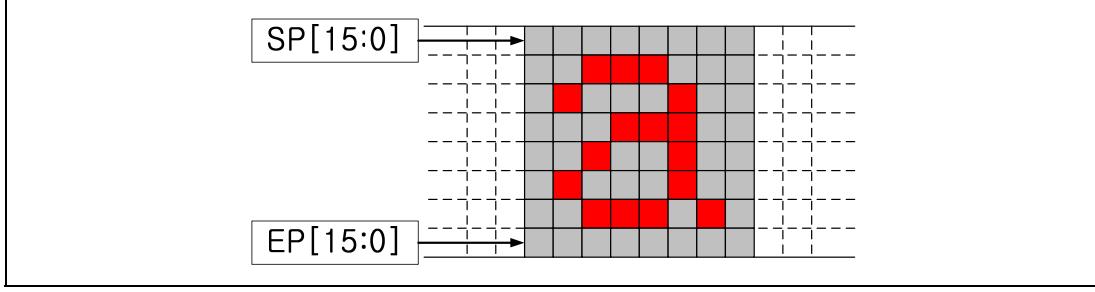
Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
CASET	W	0	0	0	1	0	1	0	1	0	2Ah												
1 <sup>st</sup> para		1	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	*Note 1												
2 <sup>nd</sup> para		1	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0													
3 <sup>rd</sup> para		1	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	*Note 1												
4 <sup>th</sup> para		1	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0													
Description	<p>This command is used to define the area of the frame memory where MCU can access.</p> <p>This command does not alter any other status.</p> <p>The value of SC [15:0] and EC [15:0] are referred when RAMWR command is issued.</p> <p>Each value represents one column line of the Frame Memory.</p> <p>(Example)</p> 																						
Restriction	<p>SC [15:0] always must be equal to or less than EC [15:0].</p> <p>Note.</p> <p>1. When SC [15:0] or EC [15:0] is greater than maximum address like below, data of out of range will be ignored.</p> <p>(Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 239 (00EFh)): MV="0"</p> <p>(Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 319 (013Fh)): MV="1"</p>																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						

	Status	Default Value		
		SC[15:0]	EC[15:0] (MV=0)	EC[15:0] (MV=1)
Default	Power On Sequence	0000h		00EFh (239d)
	S/W Reset	0000h	00EFh(239d)	013Fh(319d)
	H/W Reset	0000h		00EFh (239d)

Flow Chart	<pre> graph TD     CASET[CASET (2Ah)] --&gt; PASET[PASET (2Bh)]     PASET --&gt; RAMWR[RAMWR (2Ch)]     RAMWR --&gt; ImageData([Image Data&lt;br/&gt;D1 [23:0], D2 [23:0],&lt;br/&gt;... , Dn [23:0]])     ImageData --&gt; AnyCommand[Any Command]     </pre>
	<p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>

## 5.2.19. PASET: Page Address Set (2Bh)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
PASET	W	0	0	0	1	0	1	0	1	1	2Bh												
1 <sup>st</sup> para		1	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	*Note 1												
2 <sup>nd</sup> para		1	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	1												
3 <sup>rd</sup> para		1	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	*Note 1												
4 <sup>th</sup> para		1	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	1												
Description	<p>This command is used to define the area of the frame memory where MCU can access.</p> <p>This command makes no change on the other driver status.</p> <p>The value of SP [15:0] and EP [15:0] is referred when RAMWR command is issued.</p> <p>Each value represents one column line of the Frame Memory.</p> <p>(Example)</p> 																						
Restriction	<p>SP [15:0] should be equal to or less than EP [15:0]</p> <p>Note. When SP [15:0] or EP [15:0] are greater than maximum Page address like below, any data out of range will be ignored.</p> <p>(Parameter range: 0 ≤ SP [15:0] ≤ EP [15:0] ≤ 319 (013Fh)): MV="0"</p> <p>(Parameter range: 0 ≤ SP [15:0] ≤ EP [15:0] ≤ 239 (00EFh)): MV="1"</p>																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						

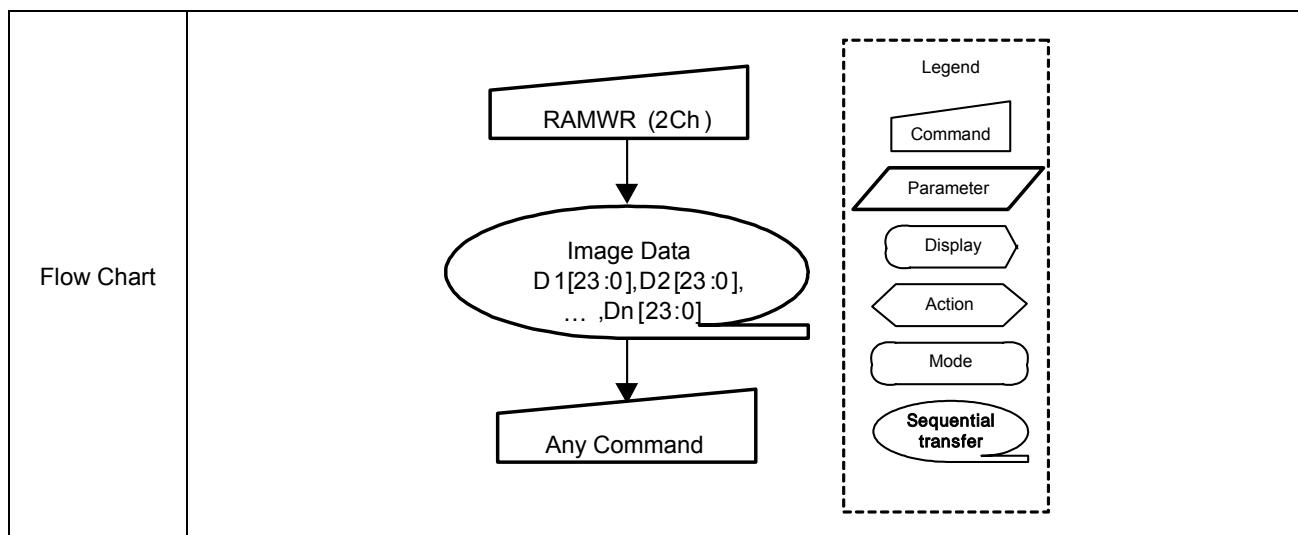
	Status	Default Value		
		SP[15:0]	EP[15:0] (MV=0)	EP[15:0] (MV=1)
Default	Power On Sequence	0000h	013Fh (319d)	
	S/W Reset	0000h	013Fh (319d)	00EFh (239d)
	H/W Reset	0000h		013Fh (319d)

Flow Chart	<pre> graph TD     CASET[CASET (2Ah)] --&gt; PASET[PASET (2Bh)]     PASET --&gt; RAMWR[RAMWR (2Ch)]     RAMWR --&gt; ImageData((Image Data D1 [23:0], D2 [23:0], ..., Dn [23:0]))     ImageData --&gt; AnyCommand[Any Command]     </pre> <p>If needed:</p> <ul style="list-style-type: none"> <li>Legend:             <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul> </li> </ul>
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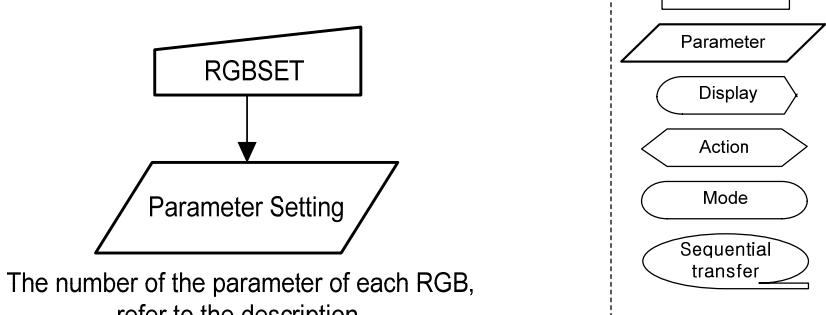
## 5.2.20. RAMWR: Memory Write (2Ch)

Inst/Para	R/W	DCX	D23~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
RAMWR	W	0	X	0	0	1	0	1	1	0	0	2Ch												
1 <sup>st</sup> para		1	D23~8	D17	D16	D15	D14	D13	D12	D11	D10	000000h ~ FFFFFFFh												
:		1	Dx~Dx	Dx	000000h ~ FFFFFFFh																			
N <sup>th</sup> para		1	Dn23~8	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	000000h ~ FFFFFFFh												
Description	<p>This command is used to transfer data from MCU to the frame memory.</p> <p>This command makes no change to the other status of the driver.</p> <p>When this command is issued, the Column register and the Page register are programmed to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting. (See section 4.5.2)</p> <p>Then D [23:0] is stored in the frame memory, the Column register and the Page register increments as in section 4.5.2</p> <p>Sending any other command can stop the Frame Write.</p>																							
Restriction	In all color modes, there is no restriction on the length of the parameters.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared				
Status	Default Value																							
Power On Sequence	Contents of memory is set randomly																							
S/W Reset	Contents of memory is not cleared																							
H/W Reset	Contents of memory is not cleared																							



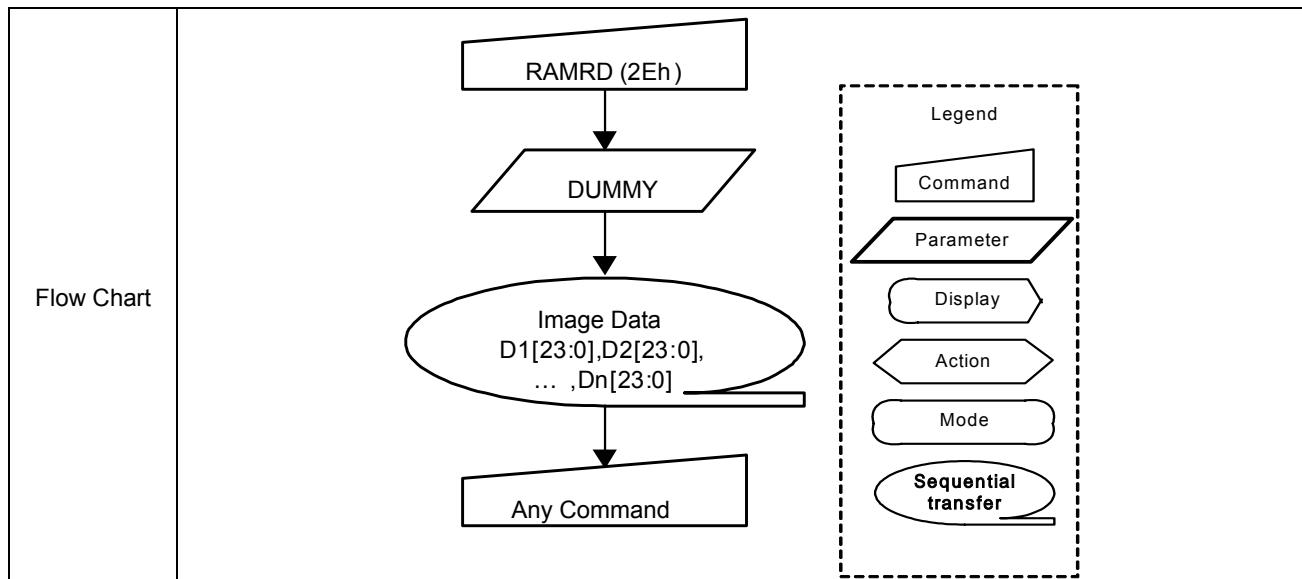
## 5.2.21. RGBSET : Color Set for 65k or 262K-Color Display (2Dh)

Inst / Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RGBSET	W	0	0	0	1	0	1	1	0	1	2Dh
1 <sup>st</sup> para		1	R007	R006	R005	R004	R003	R002	R001	R000	00h~FFh
:		1	Rn7	Rn6	Rn5	Rn4	Rn3	Rn2	Rn1	Rn0	00h~FFh
32 <sup>th</sup> para or 64 <sup>st</sup> para		1	Rn <sub>1</sub> 7	Rn <sub>1</sub> 6	R6n <sub>1</sub> 5	Rn <sub>1</sub> 4	Rn <sub>1</sub> 3	Rn <sub>1</sub> 2	Rn <sub>1</sub> 1	Rn <sub>1</sub> 0	00h~FFh
:		1	G007	G006	G005	G004	G003	G002	G001	G000	00h~FFh
:		1	Gn7	Gn6	Gn5	Gn4	Gn3	Gn2	Gn1	Gn0	00h~FFh
96 <sup>th</sup> para or 128 <sup>st</sup> para		1	Gn <sub>2</sub> 7	Gn <sub>2</sub> 6	Gn <sub>2</sub> 5	Gn <sub>2</sub> 4	Gn <sub>2</sub> 3	Gn <sub>2</sub> 2	Gn <sub>2</sub> 1	Gn <sub>2</sub> 0	00h~FFh
:		1	B007	B006	B005	B004	B003	B002	B001	B000	00h~FFh
:		1	Bn7	Bn6	Bn5	Bn4	Bn3	Bn2	Bn1	Bn0	00h~FFh
128 <sup>th</sup> para or 192 <sup>st</sup> para		1	Bn <sub>1</sub> 7	Bn <sub>1</sub> 6	Bn <sub>1</sub> 5	B6n <sub>1</sub> 4	Bn <sub>1</sub> 3	Bn <sub>1</sub> 2	Bn <sub>1</sub> 1	Bn <sub>1</sub> 0	00h~FFh
Description	<p>This command is used to define the LUT which is used for the color depth conversion such as 16-bit-to-24bit / 18bit-to-24bit. Section 4.11 shows this LUT.</p> <p>The number of parameter is decided by Interface Pixel Format (3Ah). In 262k color mode (use 18bit-to-24bit extension), this command needs 192 parameter. In 65k color mode (use 18bit-to-24bit extension), this command needs only 128 parameter.</p> <ul style="list-style-type: none"> <li>- 262k color mode: n1 = n2 = 63</li> <li>- 65k color mode: n1 = 31, n2 = 63</li> </ul> <p>This command has no effect on other commands/parameters or the contents of the frame memory. Visible change takes effect only after the Frame Memory is written. .</p>										
Restriction	<p>1. In normal mode, display data don't use Look up table. For using Look up table to expand data bit, CM register must be high. (Defalt value of CM register is low. Refer to section 3.2.1)</p> <p>2. Do not send any command before the last data is sent or LUT is not defined correctly.</p>										

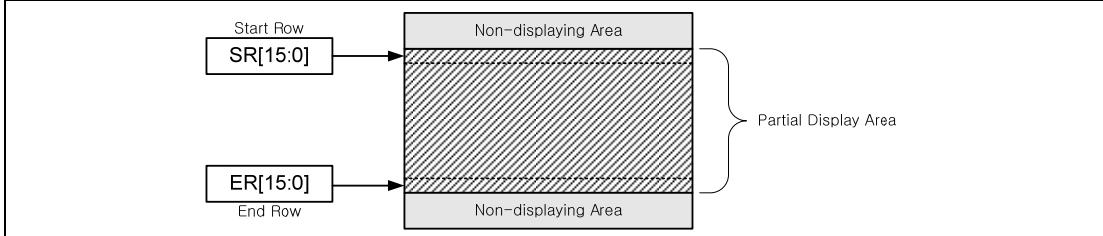
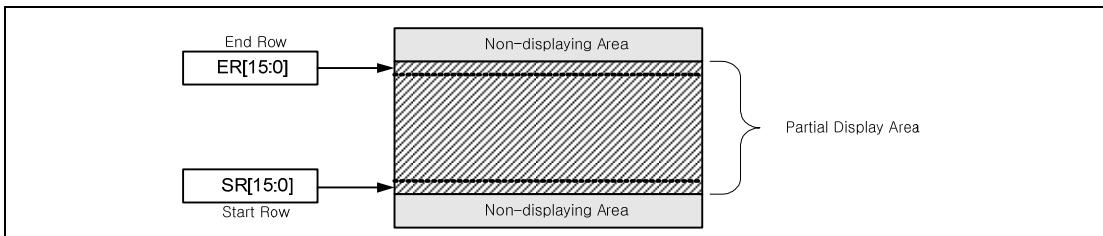
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Random values</td></tr> <tr> <td>S/W Reset</td><td>Contents of the look-up table protected</td></tr> <tr> <td>H/W Reset</td><td>Random values</td></tr> </tbody> </table>		Status	Default Value	Power On Sequence	Random values	S/W Reset	Contents of the look-up table protected	H/W Reset	Random values					
Status	Default Value													
Power On Sequence	Random values													
S/W Reset	Contents of the look-up table protected													
H/W Reset	Random values													
 <p>The number of the parameter of each RGB, refer to the description.</p>														

## 5.2.22. RAMRD: Memory Read (2Eh)

Inst/Para	R/W	DCX	D23~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
RAMRD	R	0	X	0	0	1	0	1	1	1	0	2Eh												
Dummy read		1	X	X	X	X	X	X	X	X	X	XX												
2 <sup>nd</sup> para		1	D123~8	D17	D16	D15	D14	D13	D12	D11	D10	000000h~FFFFFh												
:		1	Dx~Dx	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	000000h~FFFFFh												
(N+1) <sup>th</sup> para		1	Dn23~8	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	000000h~FFFFFh												
Description		<p>This command is used to transfer data from the frame memory to MCU.</p> <p>This command makes no change to the other driver status.</p> <p>With this command, the column register and the Page register are programmed to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting. (See section 4.5.2)</p> <p>Then D[23:0] is read back from the frame memory, and the column register and the Page register increments as in section 4.5.2</p> <p>Frame Read can be cancelled by sending any other command.</p> <p>See section 3.2 "Display Data Format" for color coding.</p> <p>Note: "X" denotes "Don't care"</p>																						
Restriction	-																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
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Sleep In	Yes																							
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Status	Default Value																							
Power On Sequence	Contents of memory is set randomly																							
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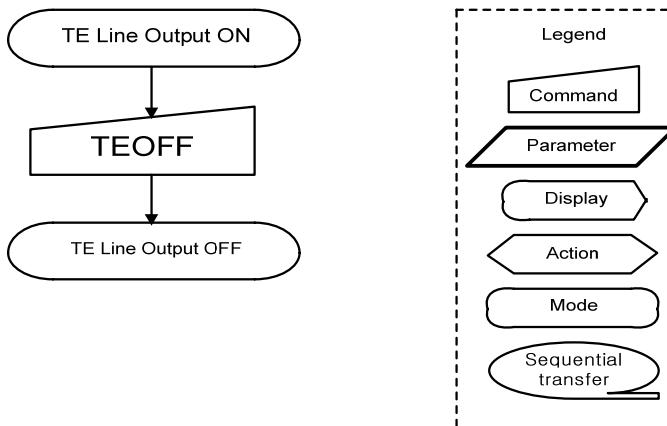


### 5.2.23. PTLAR: Partial Area (30h)

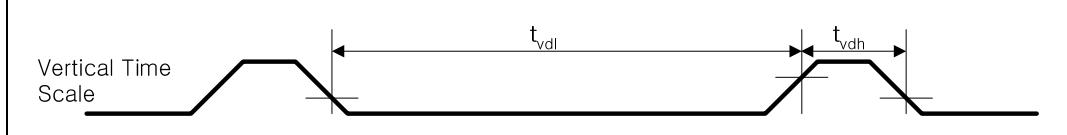
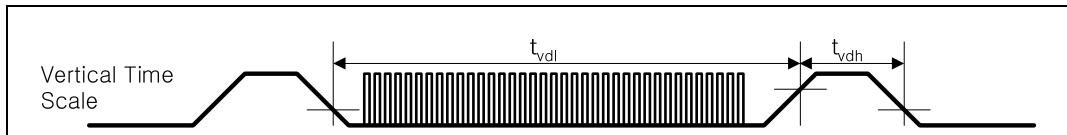
Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PLTAR	W	0	0	0	1	1	0	0	0	0	30h
1 <sup>st</sup> para		1	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	0000h~
2 <sup>nd</sup> para		1	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	013Fh
3 <sup>rd</sup> para		1	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	0000h~
4 <sup>th</sup> para		1	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	013Fh
Description	<p>This command defines the display area of the partial display mode. There are 4 parameters associated with this command. The 1<sup>st</sup> &amp; 2<sup>nd</sup> parameters define the Start Row (SR) and the 3<sup>rd</sup> and 4<sup>th</sup> parameters define the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Row address counter.</p> <p>If End Row &gt; Start Row when MADCTL D4=0</p>  <p>If End Row &gt; Start Row when MADCTL D4=1:</p>  <p>If End Row &lt; Start Row when MADCTL D4=0:</p>  <p>If End Row &lt; Start Row when MADCTL D4=1:</p>										

	<p>If End Row = Start Row, then the Partial Area will be one Row.</p>														
Restriction	SR[15:0] and ER[15:0] should have the range below (Parameter range: $0 \leq SR[15:0], ER[15:0] \leq 319(013Fh)$ )														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes		
Status	Availability														
Normal Mode On, Idle Mode Off, Sleep Out	Yes														
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Sleep In	Yes														
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th><th colspan="2">Default Value</th></tr> <tr> <th>SR[15:0]</th><th>ER[15:0]</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>0000h</td><td>013Fh</td></tr> <tr> <td>S/W Reset</td><td>0000h</td><td>013Fh</td></tr> <tr> <td>H/W Reset</td><td>0000h</td><td>013Fh</td></tr> </tbody> </table>	Status	Default Value		SR[15:0]	ER[15:0]	Power On Sequence	0000h	013Fh	S/W Reset	0000h	013Fh	H/W Reset	0000h	013Fh
Status	Default Value														
	SR[15:0]	ER[15:0]													
Power On Sequence	0000h	013Fh													
S/W Reset	0000h	013Fh													
H/W Reset	0000h	013Fh													
Flow Chart	<p>(optional) To prevent Tearing Effect Image displayed</p> <p>[ to enter partial mode ]      [ to leave partial mode ]</p> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>														

### 5.2.24. TEOFF: Tearing Effect Line OFF (34h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
TEOFF	W	0	0	0	1	1	0	1	0	0	34h	
parameter	No Parameter											
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.											
Restriction	This command has no effect when Tearing Effect output is already OFF.											
Register Availability	<b>Status</b>		<b>Availability</b>									
	Normal Mode On, Idle Mode Off, Sleep Out		Yes									
	Normal Mode On, Idle Mode On, Sleep Out		Yes									
	Partial Mode On, Idle Mode Off, Sleep Out		Yes									
	Partial Mode On, Idle Mode On, Sleep Out		Yes									
Default	<b>Status</b>		<b>Default Value</b>									
	Power On Sequence		Off									
	S/W Reset		Off									
	H/W Reset		Off									
Flow Chart	 <pre> graph TD     A([TE Line Output ON]) --&gt; B[TEOFF]     B --&gt; C([TE Line Output OFF])     </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>											

### 5.2.25. TEON: Tearing Effect Line ON (35h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
TEON	W	0	0	0	1	1	0	1	0	1	35h	
		1	0	0	0	0	0	0	0	M	xx	
		<p>This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit D4.</p> <p>The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. The TE has a different signal by interface mode.</p> <p>1) MPU Type I interface</p> <p>When M=0: The Tearing Effect Output line consists of V-Blanking information only.</p>  <p>When M=1: The Tearing Effect Output line consists of both V-Blanking and H-Blanking Information.</p> 										
		<p>2) MPU Type II interface</p> <p>When M=0: The TE signal is toggling every frame.</p>  <p>When M=1: The TE signal is toggling every 2 frame.</p> 										
		<p>See Section 4.12 for more information.</p> <p>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.</p>										
Restriction	This command has no effect when Tearing Effect output is already ON.											

	Status	Availability
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
	Status	Default Value
Default	Power On Sequence	Tearing effect off & M=0
	S/W Reset	Tearing effect off & M=0
	H/W Reset	Tearing effect off & M=0
Flow Chart	<pre> graph TD     A([TE Line Output OFF]) --&gt; B[TEON]     B --&gt; C{TE Mode Parameter(M)}     C --&gt; D([TE Line Output ON])     </pre> <p>The flowchart illustrates the sequence of operations. It starts with 'TE Line Output OFF' in an oval, followed by a rectangular box labeled 'TEON'. This leads to a parallelogram labeled 'TE Mode Parameter(M)'. Finally, it ends with 'TE Line Output ON' in an oval.</p>	<p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>

## 5.2.26. MADCTL: Memory Data Access Control (36h)

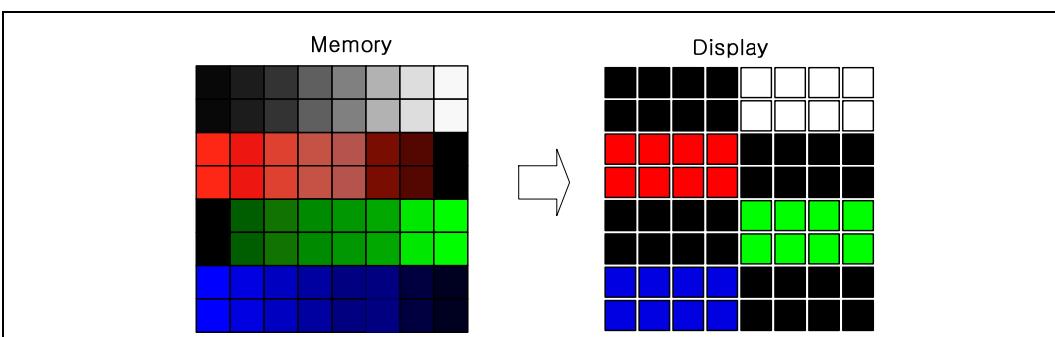
Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																	
MADCTL	W	0	0	0	1	1	0	1	1	0	36h																	
parameter		1	D7	D6	D5	D4	D3	D2	0	0	xx																	
	<p>This command defines the read/write scanning direction of the frame memory.</p> <p>This command makes no change on the other driver status.</p> <table border="1"> <thead> <tr> <th>Bit</th><th>Name</th><th>Description</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Page Address order(MY)</td><td rowspan="3">These 3-bits control MCU for the memory write/read direction.</td></tr> <tr> <td>D6</td><td>Column Address order(MX)</td></tr> <tr> <td>D5</td><td>Page/Column exchange(MV)</td></tr> <tr> <td>D4</td><td>Vertical refresh order(ML)</td><td>LCD Vertical refresh direction control</td></tr> <tr> <td>D3</td><td>RGB-BGR order(RGB)</td><td>Color selector refresh direction control (0=RGB color filter panel, 1=BGR color filter panel)</td></tr> <tr> <td>D2</td><td>Display Data Latch order(MH)</td><td>LCD horizontal refresh direction control</td></tr> </tbody> </table>									Bit	Name	Description	D7	Page Address order(MY)	These 3-bits control MCU for the memory write/read direction.	D6	Column Address order(MX)	D5	Page/Column exchange(MV)	D4	Vertical refresh order(ML)	LCD Vertical refresh direction control	D3	RGB-BGR order(RGB)	Color selector refresh direction control (0=RGB color filter panel, 1=BGR color filter panel)	D2	Display Data Latch order(MH)	LCD horizontal refresh direction control
Bit	Name	Description																										
D7	Page Address order(MY)	These 3-bits control MCU for the memory write/read direction.																										
D6	Column Address order(MX)																											
D5	Page/Column exchange(MV)																											
D4	Vertical refresh order(ML)	LCD Vertical refresh direction control																										
D3	RGB-BGR order(RGB)	Color selector refresh direction control (0=RGB color filter panel, 1=BGR color filter panel)																										
D2	Display Data Latch order(MH)	LCD horizontal refresh direction control																										
Description	<p><b>D4(ML): Vertical refresh Order</b></p> <p><b>D3(RGB) : RGB-BGR order</b></p> <p>Note1. D3 setting is effective only to display the panel. D3 setting doesn't swap memory data itself.</p>																											

	<p style="text-align: center;"><b>D2(MH): Horizontal refresh Order</b></p>												
Restriction	<p>D1 and D0 of the 1st parameter are set to '00' internally.</p> <p>D2 is effective only to Read/Write registers. It is not effective to the display function.</p>												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Availability</th> </tr> </thead> <tbody> <tr> <td style="padding: 2px;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="padding: 2px; text-align: center;">Yes</td> </tr> <tr> <td style="padding: 2px;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="padding: 2px; text-align: center;">Yes</td> </tr> <tr> <td style="padding: 2px;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="padding: 2px; text-align: center;">Yes</td> </tr> <tr> <td style="padding: 2px;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="padding: 2px; text-align: center;">Yes</td> </tr> <tr> <td style="padding: 2px;">Sleep In</td> <td style="padding: 2px; text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="padding: 2px;">Power On Sequence</td> <td style="padding: 2px; text-align: center;">D7=0, D6=0, D5=0, D4=0, D3=0, D2=0</td> </tr> <tr> <td style="padding: 2px;">S/W Reset</td> <td style="padding: 2px; text-align: center;">No Change</td> </tr> <tr> <td style="padding: 2px;">H/W Reset</td> <td style="padding: 2px; text-align: center;">D7=0, D6=0, D5=0, D4=0, D3=0, D2=0</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	D7=0, D6=0, D5=0, D4=0, D3=0, D2=0	S/W Reset	No Change	H/W Reset	D7=0, D6=0, D5=0, D4=0, D3=0, D2=0				
Status	Default Value												
Power On Sequence	D7=0, D6=0, D5=0, D4=0, D3=0, D2=0												
S/W Reset	No Change												
H/W Reset	D7=0, D6=0, D5=0, D4=0, D3=0, D2=0												
Flowchart	<pre>     graph TD         MADCTL[MADCTL] --&gt; P1[1st parameter]         subgraph Legend [Legend]             Command[Command]             Parameter[Parameter]             Display[Display]             Action[Action]             Mode[Mode]             Sequential[Sequential transfer]         end     </pre>												

## 5.2.27. IDMOFF: Idle Mode Off (38h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
IDMOFF	W	0	0	0	1	1	1	0	0	0	38h												
Parameter	No Parameter																						
Description	<p>This command turns Idle mode off.</p> <p>There will be no abnormal visible effect during the mode transition of the display.</p> <p>During the idle off mode,</p> <ol style="list-style-type: none"> <li>1. LCD can display maximum 16M-colors.</li> <li>2. Normal frame frequency is applied.</li> </ol>																						
Restriction	This command has no effect when module is already in idle off mode.																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Idle Mode Off</td></tr> <tr> <td>S/W Reset</td><td>Idle Mode Off</td></tr> <tr> <td>H/W Reset</td><td>Idle Mode Off</td></tr> </tbody> </table>											Status	Default Value	Power On Sequence	Idle Mode Off	S/W Reset	Idle Mode Off	H/W Reset	Idle Mode Off				
Status	Default Value																						
Power On Sequence	Idle Mode Off																						
S/W Reset	Idle Mode Off																						
H/W Reset	Idle Mode Off																						
Flowchart	<pre> graph TD     A([Idle mode on]) --&gt; B[/IDMOFF/]     B --&gt; C([Idle mode off])     </pre> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																						

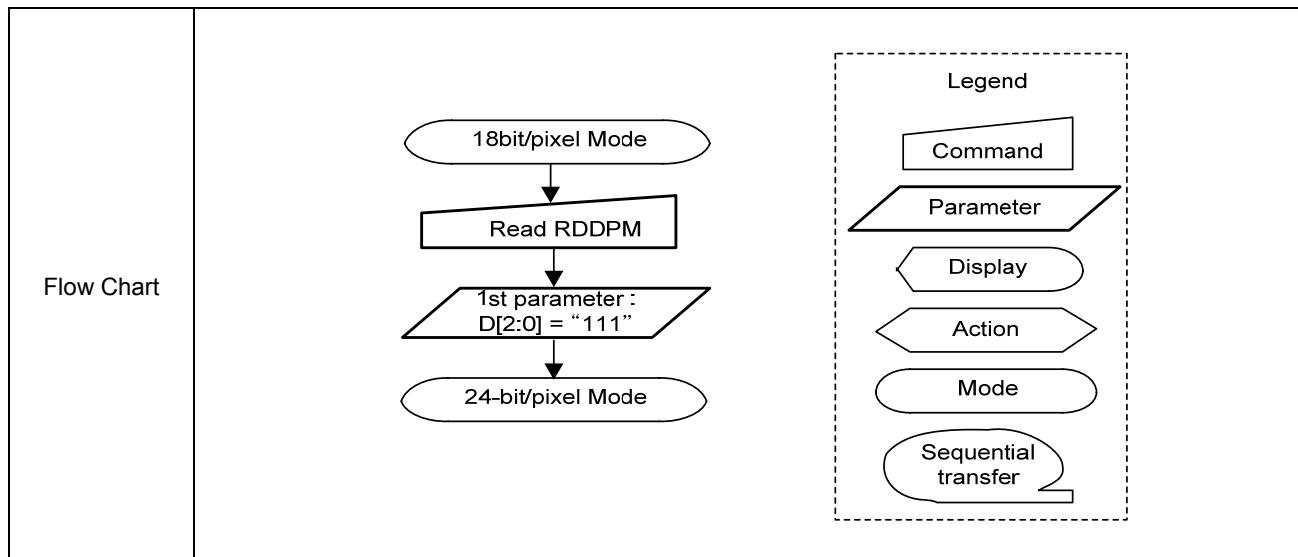
## 5.2.28. IDMON: Idle Mode On (39h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																					
IDMON	W	0	0	0	1	1	1	0	0	1	39h																																					
Parameter	No Parameter																																															
Description	<p>This command turns Idle mode on. (Refer to section 4.9 8-Color mode)  There will be no abnormal visible effect during mode transition.  During the idle on mode,</p> <ol style="list-style-type: none"> <li>1. Color expression is reduced to 8-color. 8-color is displayed by MSB of each R, G, and B in the Frame Memory.</li> <li>2. 8-Color mode frame frequency is applied.</li> <li>3. Exit from IDMON by Idle Mode Off (38h) command</li> </ol> <p>(Example)</p>  <table border="1"> <thead> <tr> <th>Color</th><th>R<sub>7</sub>R<sub>6</sub>R<sub>5</sub>R<sub>4</sub>R<sub>3</sub>R<sub>2</sub>R<sub>1</sub>R<sub>0</sub></th><th>G<sub>7</sub>G<sub>6</sub>G<sub>5</sub>G<sub>4</sub>G<sub>3</sub>G<sub>2</sub>G<sub>1</sub>G<sub>0</sub></th><th>B<sub>7</sub>B<sub>6</sub>B<sub>5</sub>B<sub>4</sub>B<sub>3</sub>B<sub>2</sub>B<sub>1</sub>B<sub>0</sub></th></tr> </thead> <tbody> <tr> <td>Black</td><td>0XXXXXXX</td><td>0XXXXXXX</td><td>0XXXXXXX</td></tr> <tr> <td>Blue</td><td>0XXXXXXX</td><td>0XXXXXXX</td><td>1XXXXXXX</td></tr> <tr> <td>Red</td><td>1XXXXXXX</td><td>0XXXXXXX</td><td>0XXXXXXX</td></tr> <tr> <td>Magenta</td><td>1XXXXXXX</td><td>0XXXXXXX</td><td>1XXXXXXX</td></tr> <tr> <td>Green</td><td>0XXXXXXX</td><td>1XXXXXXX</td><td>0XXXXXXX</td></tr> <tr> <td>Cyan</td><td>0XXXXXXX</td><td>1XXXXXXX</td><td>1XXXXXXX</td></tr> <tr> <td>Yellow</td><td>1XXXXXXX</td><td>1XXXXXXX</td><td>0XXXXXXX</td></tr> <tr> <td>White</td><td>1XXXXXXX</td><td>1XXXXXXX</td><td>1XXXXXXX</td></tr> </tbody> </table> <p>Note: "X" denotes "Don't care"</p>												Color	R <sub>7</sub> R <sub>6</sub> R <sub>5</sub> R <sub>4</sub> R <sub>3</sub> R <sub>2</sub> R <sub>1</sub> R <sub>0</sub>	G <sub>7</sub> G <sub>6</sub> G <sub>5</sub> G <sub>4</sub> G <sub>3</sub> G <sub>2</sub> G <sub>1</sub> G <sub>0</sub>	B <sub>7</sub> B <sub>6</sub> B <sub>5</sub> B <sub>4</sub> B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	Black	0XXXXXXX	0XXXXXXX	0XXXXXXX	Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX	Red	1XXXXXXX	0XXXXXXX	0XXXXXXX	Magenta	1XXXXXXX	0XXXXXXX	1XXXXXXX	Green	0XXXXXXX	1XXXXXXX	0XXXXXXX	Cyan	0XXXXXXX	1XXXXXXX	1XXXXXXX	Yellow	1XXXXXXX	1XXXXXXX	0XXXXXXX	White	1XXXXXXX	1XXXXXXX	1XXXXXXX
Color	R <sub>7</sub> R <sub>6</sub> R <sub>5</sub> R <sub>4</sub> R <sub>3</sub> R <sub>2</sub> R <sub>1</sub> R <sub>0</sub>	G <sub>7</sub> G <sub>6</sub> G <sub>5</sub> G <sub>4</sub> G <sub>3</sub> G <sub>2</sub> G <sub>1</sub> G <sub>0</sub>	B <sub>7</sub> B <sub>6</sub> B <sub>5</sub> B <sub>4</sub> B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>																																													
Black	0XXXXXXX	0XXXXXXX	0XXXXXXX																																													
Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX																																													
Red	1XXXXXXX	0XXXXXXX	0XXXXXXX																																													
Magenta	1XXXXXXX	0XXXXXXX	1XXXXXXX																																													
Green	0XXXXXXX	1XXXXXXX	0XXXXXXX																																													
Cyan	0XXXXXXX	1XXXXXXX	1XXXXXXX																																													
Yellow	1XXXXXXX	1XXXXXXX	0XXXXXXX																																													
White	1XXXXXXX	1XXXXXXX	1XXXXXXX																																													
Restriction	This command has no effect when module is already in idle off mode.																																															

	Status	Availability
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
	Status	Default Value
Default	Power On Sequence	Idle Mode Off
	S/W Reset	Idle Mode Off
	H/W Reset	Idle Mode Off
Flow Chart	<pre> graph TD     A([Idle mode off]) --&gt; B[IDMON]     B --&gt; C([Idle mode on])     </pre>	<p>Legend</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>

## 5.2.29. COLMOD : Interface Pixel Format (3Ah)

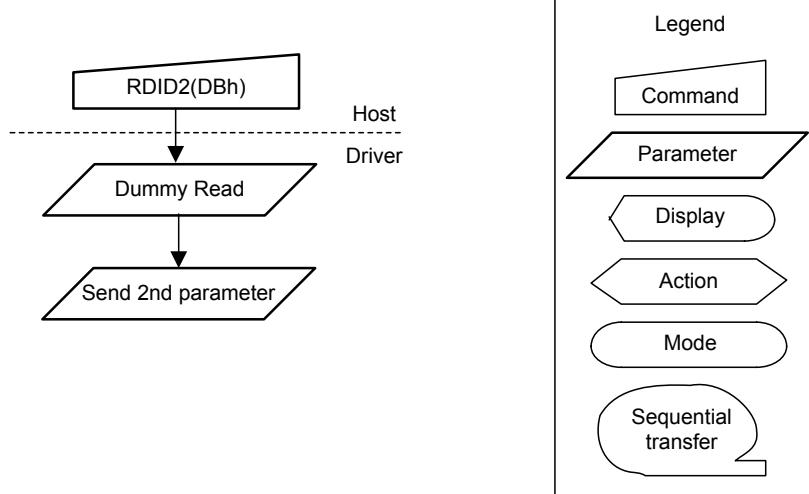
Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
COLMOD	W	0	0	0	1	1	1	0	1	0	3Ah												
Parameter		1	D7	D6	D5	D4	D3	D2	D1	D0	XX												
Description		This command is used to define the format of RGB picture data, which is to be transferred via the MPU interface. The formats are as shown in the table below.																					
		<b>Bit</b>	<b>Description</b>				<b>Value</b>																
		D7	-				"0" (Not Used)																
		D6	Control RGB Interface Color Format (VFPPF)				"101"=16-bits/pixel																
		D5					"110"=18-bits/pixel																
		D4					"111"= 24-bits/pixel																
		D3	-				Others = not defined																
		D2	Control MPU Interface Color Format (IFPF)				"101"=16-bits/pixel																
		D1					"110"=18-bits/pixel																
		D0					"111"= 24-bits/pixel																
Note																							
In 16-bit/pixel or 18-bit/pixel mode, display data is expended to 24bit data. Refer to Section 3.2.1 12-bits/pixel (4096 color mode) is not supported.																							
Restrictions	There is no visible effect until the frame memory is written.																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal mode on, Idle mode off, Sleep out</td> <td>Yes</td> </tr> <tr> <td>Normal mode on, Idle mode on, Sleep out</td> <td>Yes</td> </tr> <tr> <td>Partial mode on, Idle mode off, Sleep out</td> <td>Yes</td> </tr> <tr> <td>Partial mode on, Idle mode on, Sleep out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal mode on, Idle mode off, Sleep out	Yes	Normal mode on, Idle mode on, Sleep out	Yes	Partial mode on, Idle mode off, Sleep out	Yes	Partial mode on, Idle mode on, Sleep out	Yes	Sleep In	Yes
Status	Availability																						
Normal mode on, Idle mode off, Sleep out	Yes																						
Normal mode on, Idle mode on, Sleep out	Yes																						
Partial mode on, Idle mode off, Sleep out	Yes																						
Partial mode on, Idle mode on, Sleep out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>24-bits/pixel</td> </tr> <tr> <td>S/W Reset</td> <td>No change</td> </tr> <tr> <td>H/W Reset</td> <td>24-bits/pixel</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	24-bits/pixel	S/W Reset	No change	H/W Reset	24-bits/pixel				
Status	Default Value																						
Power On Sequence	24-bits/pixel																						
S/W Reset	No change																						
H/W Reset	24-bits/pixel																						



## 5.2.30. RDID1 : Read ID1 Value (DAh)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
RDID1	R	0	1	1	0	1	1	0	1	0	DAh												
Dummy read		1	X	X	X	X	X	X	X	X	X												
2 <sup>nd</sup> Parameter		1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	xx												
Description	This read byte identifies the LCD module's manufacturer.  Note: "X" denotes "Don't care"																						
Restrictions	-																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal mode on, Idle mode off, Sleep out</td><td>Yes</td></tr> <tr> <td>Normal mode on, Idle mode on, Sleep out</td><td>Yes</td></tr> <tr> <td>Partial mode on, Idle mode off, Sleep out</td><td>Yes</td></tr> <tr> <td>Partial mode on, Idle mode on, Sleep out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>											Status	Availability	Normal mode on, Idle mode off, Sleep out	Yes	Normal mode on, Idle mode on, Sleep out	Yes	Partial mode on, Idle mode off, Sleep out	Yes	Partial mode on, Idle mode on, Sleep out	Yes	Sleep In	Yes
Status	Availability																						
Normal mode on, Idle mode off, Sleep out	Yes																						
Normal mode on, Idle mode on, Sleep out	Yes																						
Partial mode on, Idle mode off, Sleep out	Yes																						
Partial mode on, Idle mode on, Sleep out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>(MTP value)</td></tr> <tr> <td>S/W Reset</td><td>(MTP value)</td></tr> <tr> <td>H/W Reset</td><td>(MTP value)</td></tr> </tbody> </table>											Status	Default Value	Power On Sequence	(MTP value)	S/W Reset	(MTP value)	H/W Reset	(MTP value)				
Status	Default Value																						
Power On Sequence	(MTP value)																						
S/W Reset	(MTP value)																						
H/W Reset	(MTP value)																						
Flow Chart	<p>The flowchart illustrates the communication sequence between the Host and the Driver. It starts with the Host sending the RDID1(DAh) command to the Driver. This is followed by a Dummy Read action, and finally, the Driver sends the 2nd parameter back to the Host.</p> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul> <pre> graph TD     RDID1[RDID1(DAh)] --&gt; DummyRead[/Dummy Read/]     DummyRead --&gt; SendParam[/Send 2nd parameter/]   </pre>																						

## 5.2.31. RDID2 : Read ID2 Value (DBh)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
RDID2	R	0	1	1	0	1	1	0	1	1	DBh												
Dummy read		1	X	X	X	X	X	X	X	X	X												
2 <sup>nd</sup> Parameter		1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	xx												
Description	This read byte is used to track the LCD module/driver version. It is provided by a display supplier and updated each time a revision is made to the display, material or construction specifications.  Note: "X" denotes "Don't care"																						
Restrictions	-																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal mode on, Idle mode off, Sleep out</td><td>Yes</td></tr> <tr> <td>Normal mode on, Idle mode on, Sleep out</td><td>Yes</td></tr> <tr> <td>Partial mode on, Idle mode off, Sleep out</td><td>Yes</td></tr> <tr> <td>Partial mode on, Idle mode on, Sleep out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>											Status	Availability	Normal mode on, Idle mode off, Sleep out	Yes	Normal mode on, Idle mode on, Sleep out	Yes	Partial mode on, Idle mode off, Sleep out	Yes	Partial mode on, Idle mode on, Sleep out	Yes	Sleep In	Yes
Status	Availability																						
Normal mode on, Idle mode off, Sleep out	Yes																						
Normal mode on, Idle mode on, Sleep out	Yes																						
Partial mode on, Idle mode off, Sleep out	Yes																						
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Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>(MTP value)</td></tr> <tr> <td>S/W Reset</td><td>(MTP value)</td></tr> <tr> <td>H/W Reset</td><td>(MTP value)</td></tr> </tbody> </table>											Status	Default Value	Power On Sequence	(MTP value)	S/W Reset	(MTP value)	H/W Reset	(MTP value)				
Status	Default Value																						
Power On Sequence	(MTP value)																						
S/W Reset	(MTP value)																						
H/W Reset	(MTP value)																						
Flow Chart	 <pre> graph TD     RDID2[RDID2(DBh)] --&gt; DR{Dummy Read}     DR --&gt; S2P[Send 2nd parameter]   </pre> <p>Legend:</p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																						

## 5.2.32. RDID3 : Read ID3 Value (DCh)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
RDID3	R	0	1	1	0	1	1	1	0	0	DC												
Dummy read		1	X	X	X	X	X	X	X	X	X												
2 <sup>nd</sup> Parameter		1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	xx												
Description	This read byte identifies the LCD module/driver. It is specified by a user.  Note: "X" denotes "Don't care"																						
Restrictions	-																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal mode on, Idle mode off, Sleep out</td><td>Yes</td></tr> <tr> <td>Normal mode on, Idle mode on, Sleep out</td><td>Yes</td></tr> <tr> <td>Partial mode on, Idle mode off, Sleep out</td><td>Yes</td></tr> <tr> <td>Partial mode on, Idle mode on, Sleep out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>											Status	Availability	Normal mode on, Idle mode off, Sleep out	Yes	Normal mode on, Idle mode on, Sleep out	Yes	Partial mode on, Idle mode off, Sleep out	Yes	Partial mode on, Idle mode on, Sleep out	Yes	Sleep In	Yes
Status	Availability																						
Normal mode on, Idle mode off, Sleep out	Yes																						
Normal mode on, Idle mode on, Sleep out	Yes																						
Partial mode on, Idle mode off, Sleep out	Yes																						
Partial mode on, Idle mode on, Sleep out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>(MTP value)</td></tr> <tr> <td>S/W Reset</td><td>(MTP value)</td></tr> <tr> <td>H/W Reset</td><td>(MTP value)</td></tr> </tbody> </table>											Status	Default Value	Power On Sequence	(MTP value)	S/W Reset	(MTP value)	H/W Reset	(MTP value)				
Status	Default Value																						
Power On Sequence	(MTP value)																						
S/W Reset	(MTP value)																						
H/W Reset	(MTP value)																						
Flow Chart	<pre> graph TD     RDID3[RDID3(DCh)] --&gt; DummyRead[/Dummy Read/]     DummyRead --&gt; SendParam[/Send 2nd parameter/]     </pre> <p><b>Legend:</b></p> <ul style="list-style-type: none"> <li>Command</li> <li>Parameter</li> <li>Display</li> <li>Action</li> <li>Mode</li> <li>Sequential transfer</li> </ul>																						

### 5.2.33. WRDISBV : Write Manual Brightness (51h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRDISBV	W	0	0	1	0	1	0	0	0	1	51
1 <sup>st</sup> para		1	MAN_BRIGHT [7]	MAN_BRIGHT [6]	MAN_BRIGHT [5]	MAN_BRIGHT [4]	MAN_BRIGHT [3]	MAN_BRIGHT [2]	MAN_BRIGHT [1]	MAN_BRIGHT [0]	-

This command is used to set the manual brightness value. If the manual brightness is used (BC\_MODE = "01" or "11"), the value of register "MAN\_BRIGHT[7:0] is selected or merged with the MIE brightness to generate BC.

Table 111. MAN\_BRIGHT[7:0]

MAN_BRIGHT[7:0]	Brightness Level
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
...	...
1111_1100	252
1111_1101	253
1111_1110	254
1111_1111	255

Status	Default Value
Initial	MAN_BRIGHT[7:0] = 0000_0000

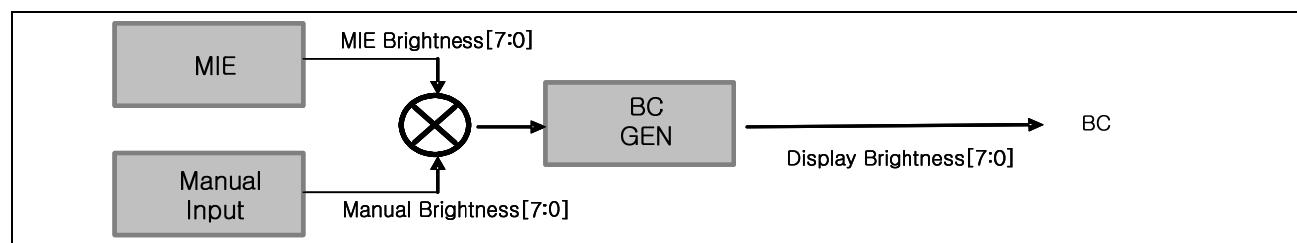


Figure 130. Manual brightness

The display brightness level is calculated with the following formula.

$$\text{Display_Brightness} = \text{MIE_Brightness} \times \text{Manual_Brightness} / 255$$

Figure 131. Calculation formula

The MIE brightness has transition time A and the manual brightness has transition time B.

The maximum transition time is transition time C ( $C = A + B$ ).

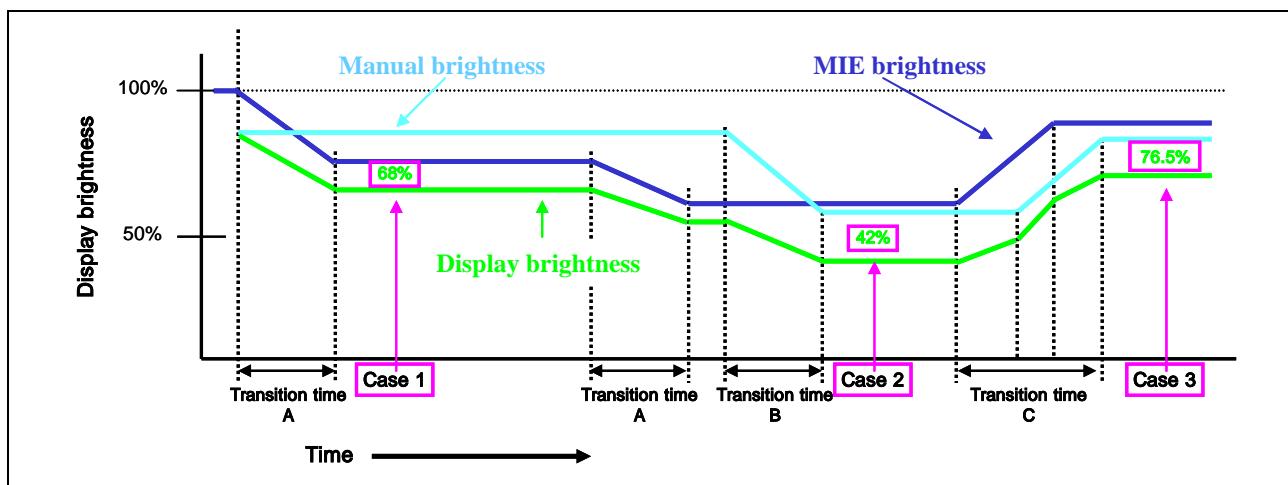


Figure 132. Example of manual brightness

Table 112. Example of manual brightness

Operation Mode	Manual Brightness	MIE Brightness	Display Brightness
Case 1	85 %	80 %	68 %
Case 2	60 %	70 %	42 %
Case 3	85 %	90 %	76.5 %

### 5.2.34. RDDISBV : Read Display Brightness (52h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDISBV	R	0	0	1	0	1	0	0	1	0	52
1 <sup>st</sup> para		1	DISP_BRIGHT [7]	DISP_BRIGHT [6]	DISP_BRIGHT [5]	DISP_BRIGHT [4]	DISP_BRIGHT [3]	DISP_BRIGHT [2]	DISP_BRIGHT [1]	DISP_BRIGHT [0]	-

This command is used to read the display brightness value. It is a real brightness value of BC output which is calculated with MIE brightness and manual brightness. The value of this register is updated after display V-sync and host can read exact value after display V-sync.

**Table 113. DISP\_BRIGHT[7:0]**

DISP_BRIGHT[7:0]	Brightness Level
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
...	...
1111_1100	252
1111_1101	253
1111_1110	254
1111_1111	255

Status	Default Value
Initial	DISP_BRIGHT[7:0] = 0000_0000

### 5.2.35. WRCTRLD : Write BL Control (53h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCTRLD	W	0	0	1	0	1	0	0	1	1	53
1st para		1	0	0	BCTRL	0	DD	BL	0	0	-

#### 5.2.35.1. BCTRL

This register is used to enable the backlight control block. If BCTRL is turned off, the BL control block is not working and BC output is fixed to low.

**Table 114. BCTRL**

BCTRL	BL Control
0	Off
1	On

Note 1. When BCTRL does ON, establish VBP and VFP by same value.

Status	Default Value
Initial	BCTRL = 0

#### 5.2.35.2. DD

This register is used to enable the manual brightness dimming function. The manual brightness should be changed smoothly for preventing a visible artifact, e.g. flicker. So the dimming function is needed when the transition of input manual brightness is fast to make a visible artifact. When the manual dimming is enabled, the new manual brightness value has to be changed after former dimming transition is finished. The transition time is controlled by DT[2:0].

**Table 115. DD**

DD	Manual Dimming Function
0	Off
1	On

Status	Default Value
Initial	DD = 0

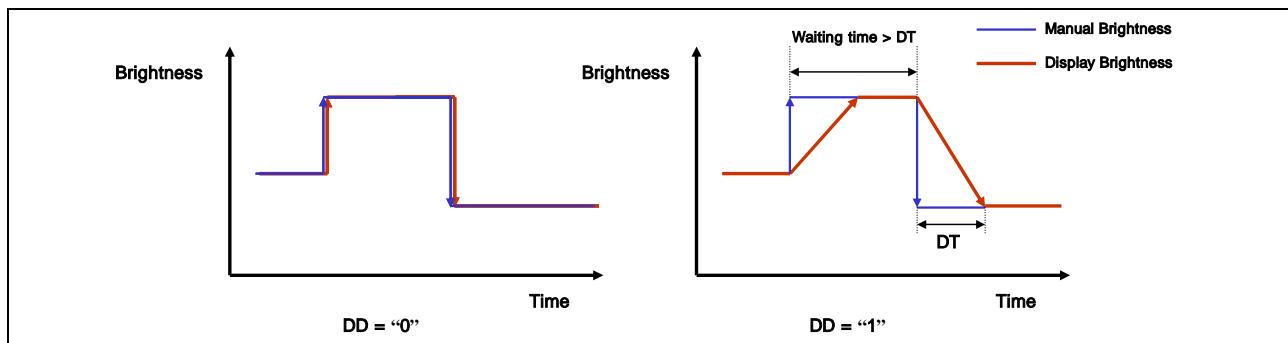


Figure 133. Manual dimming function

## 5.2.35.3. BL

This register is used to enable the BC output. Even if the value of BL is "0", the backlight control block is working when BCTRL is "1". And the host can read the display brightness value (DISP\_BRIGHT[7:0]) and control the BLU directly.

Table 116. BL

BL	BC state
0	Low
1	Active

Status	Default Value
Initial	BL = 0

### 5.2.36. Read BL Control (54h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCTRLD	R	0	0	1	0	1	0	1	0	0	54
1 <sup>st</sup> para		1	0	0	BCTRL	0	DD	BL	0	0	-

This command is used to read BL control register. For details, refer to Write BL Control (53h).

### 5.2.37. WRCABC : Write MIE Mode (55h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCABC	W	0	0	1	0	1	0	1	0	1	55
1 <sup>st</sup> para		1	0	0	0	0	0	0	MIE_MODE [1]	MIE_MODE [0]	-

This command is used to select the operation mode of MIE. If the MIE is off mode, the BLU brightness value of MIE is set to 255.

**Table 117. MIE\_MODE[1:0]**

MIE_MODE[1:0]	Operation Mode
00	Off
01	UI (User Interface)
10	Still Image
11	Moving Image

Status	Default Value
Initial	MIE_MODE[1:0] = 00

### 5.2.38. Read MIE Mode (56h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCABC	R	0	0	1	0	1	0	1	1	0	56
1 <sup>st</sup> para		1	0	0	0	0	0	0	MIE_MODE [1]	MIE_MODE [0]	-

This command is used to read MIE mode register. For details, refer to Write MIE Mode (55h).

### 5.2.39. WRCABCMB : Write Minimum Brightness (5Eh)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCABCMB	W	0	0	1	0	1	1	1	1	0	5E
1 <sup>st</sup> para		1	MIN_BRIGHT [7]	MIN_BRIGHT [6]	MIN_BRIGHT [5]	MIN_BRIGHT [4]	MIN_BRIGHT [3]	MIN_BRIGHT [2]	MIN_BRIGHT [1]	MIN_BRIGHT [0]	-

This command is used to set the minimum brightness value.

The MIE function is automatically reduced the backlight brightness based on the content of image. In the case of the combination with the manual brightness setting, the display brightness can be too dark. It must affect to image quality degradation. So the minimum brightness setting is used to avoid too much brightness reduction.

When the MIE is activated, the display brightness can not be reduced less than the value of minimum brightness setting. The image processing function is worked as normal, even if the display brightness can not be decreased by the minimum brightness setting.

This function of the manual brightness setting does not affect to the other functions. The smooth transition and dimming function can be worked as normal. The manual brightness shouldn't be set less than the minimum brightness. When the BL control block is turned off (BCTRL=0), the MIE minimum brightness setting is ignored.

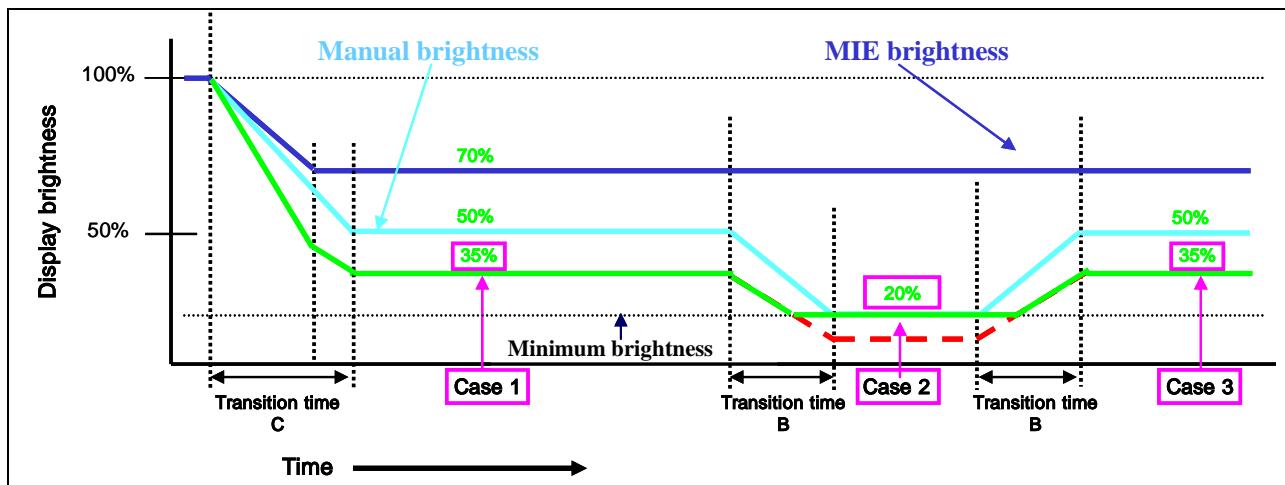


Figure 134. Example of minimum brightness

Table 118. Example of minimum brightness (Minimum brightness = 20%)

Operation Mode	Manual Brightness	MIE Brightness	Calculated Display Brightness	Display Brightness
Case 1	50 %	70 %	35%	35 %
Case 2	20 %	70 %	14%	20 %
Case 3	50 %	70 %	35%	35 %

Table 119. MIN\_BRIGHT[7:0]

MIN_BRIGHT[7:0]	Brightness Level
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
...	...
1111_1100	252
1111_1101	253
1111_1110	254
1111_1111	255

Status	Default Value
Initial	MIN_BRIGHT[7:0] = 0000_0000

### 5.2.40. Read Minimum Brightness (5Fh)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	R	0	0	1	0	1	1	1	1	1	5F
1 <sup>st</sup> para		1	MIN_ BRIGHT [7]	MIN_ BRIGHT [6]	MIN_ BRIGHT [5]	MIN_ BRIGHT [4]	MIN_ BRIGHT [3]	MIN_ BRIGHT [2]	MIN_ BRIGHT [1]	MIN_ BRIGHT [0]	-

This command is used to read Minimum Brightness register. For details, refer to Write Minimum Brightness (5Eh).

### 5.2.41. MIECTRL1 : Write MIE Control 1 (CAh)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MIECTL1	W	0	1	1	0	0	1	0	1	0	CA
1 <sup>st</sup> para		1	RRC[7]	RRC[6]	RRC[5]	RRC[4]	RRC[3]	RRC[2]	RRC[1]	RRC[0]	-
2 <sup>nd</sup> para		1	IERC[7]	IERC[6]	IERC[5]	IERC[4]	IERC[3]	IERC[2]	IERC[1]	IERC[0]	-
3 <sup>rd</sup> para		1	0	0	ONOFF _DIMM_ EN	SERC[4]	SERC[3]	SERC[2]	SERC[1]	SERC[0]	-

#### 5.2.41.1. RRC[7:0]

This register is used to adjust the reduction rate of the backlight power.

$$\text{Adjusted\_Power\_Reduction\_Rate} = \text{Power\_Reduction\_Rate} \times \frac{\text{RRC}}{128}$$

Figure 135. Power reduction rate

The Power Reduction Rate is the power reduction rate by the MIE algorithm. The Reduction range is from '0' (no reduction) to two times of the contents adaptive backlight power. To increase the value of RRC, more backlight power can be reduced but the displayed image become darker. The other way, brighter image is obtained by decreasing the value of RRC.

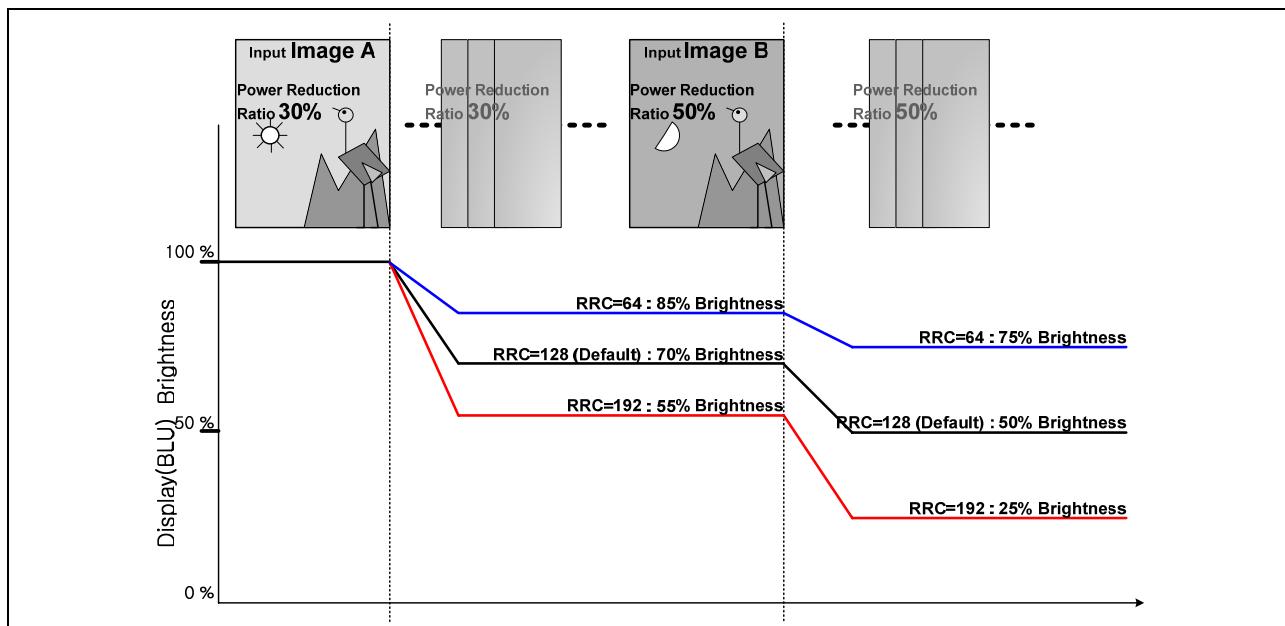


Figure 136. Example of RRC

Table 120. RRC[7:0]

RRC[7:0]	Adjusted Power Reduction Rate
0000_0000	Power Reduction Rate x 0/128
0000_0001	Power Reduction Rate x 1/128
0000_0010	Power Reduction Rate x 2/128
...	...
1000_0000	Power Reduction Rate x 128/128
...	...
1111_1101	Power Reduction Rate x 253/128
1111_1110	Power Reduction Rate x 254/128
1111_1111	Power Reduction Rate x 255/128

Status	Default Value
Initial	RRC[7:0] = 1000_0000

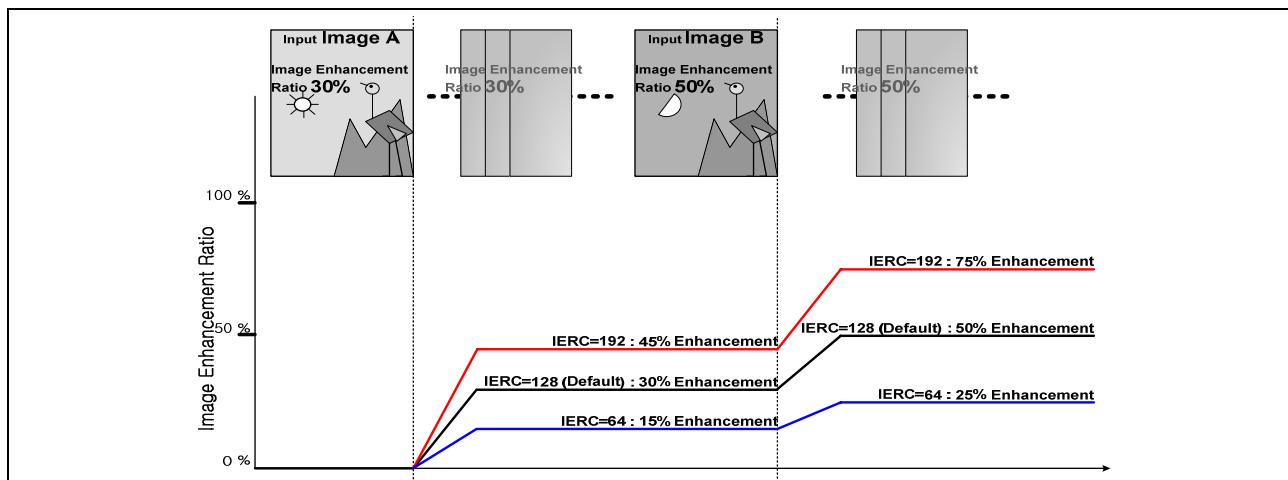
## 5.2.41.2. IERC[7:0]

This register is used to adjust the image enhancement rate.

$$\text{Adjusted\_Image\_Enhancement\_Rate} = \text{Image\_Enhancement\_Rate} \times \frac{\text{IERC}}{128}$$

**Figure 137. Image enhancement rate**

If the value of IERC is '0', there is no enhancement in output image. If its value is '255', the enhancement rate is two times of Image Enhancement Rate. If the value of IERC is increased, brighter image is obtained but the quality of displayed image may be decreased. The other way, if the value of IERC register is decreased, the quality of image will be increased.



**Figure 138. Example of IERC**

**Table 121. IERC[7:0]**

IERC[7:0]	Adjust Image Enhancement Rate
0000_0000	Image Enhancement Rate x 0/128
0000_0001	Image Enhancement Rate x 1/128
0000_0010	Image Enhancement Rate x 2/128
...	...
1000_0000	Image Enhancement Rate x 128/128
...	...
1111_1101	Image Enhancement Rate x 253/128
1111_1110	Image Enhancement Rate x 254/128
1111_1111	Image Enhancement Rate x 255/128

Status	Default Value
Initial	IERC[7:0] = 1000_0000

### 5.2.41.3. ONOFF\_DIMM\_EN

This register is used to enable the on/off dimming function of MIE.

The MIE has a dimming function for preventing abnormal visible artifacts when the MIE is turning on or off.

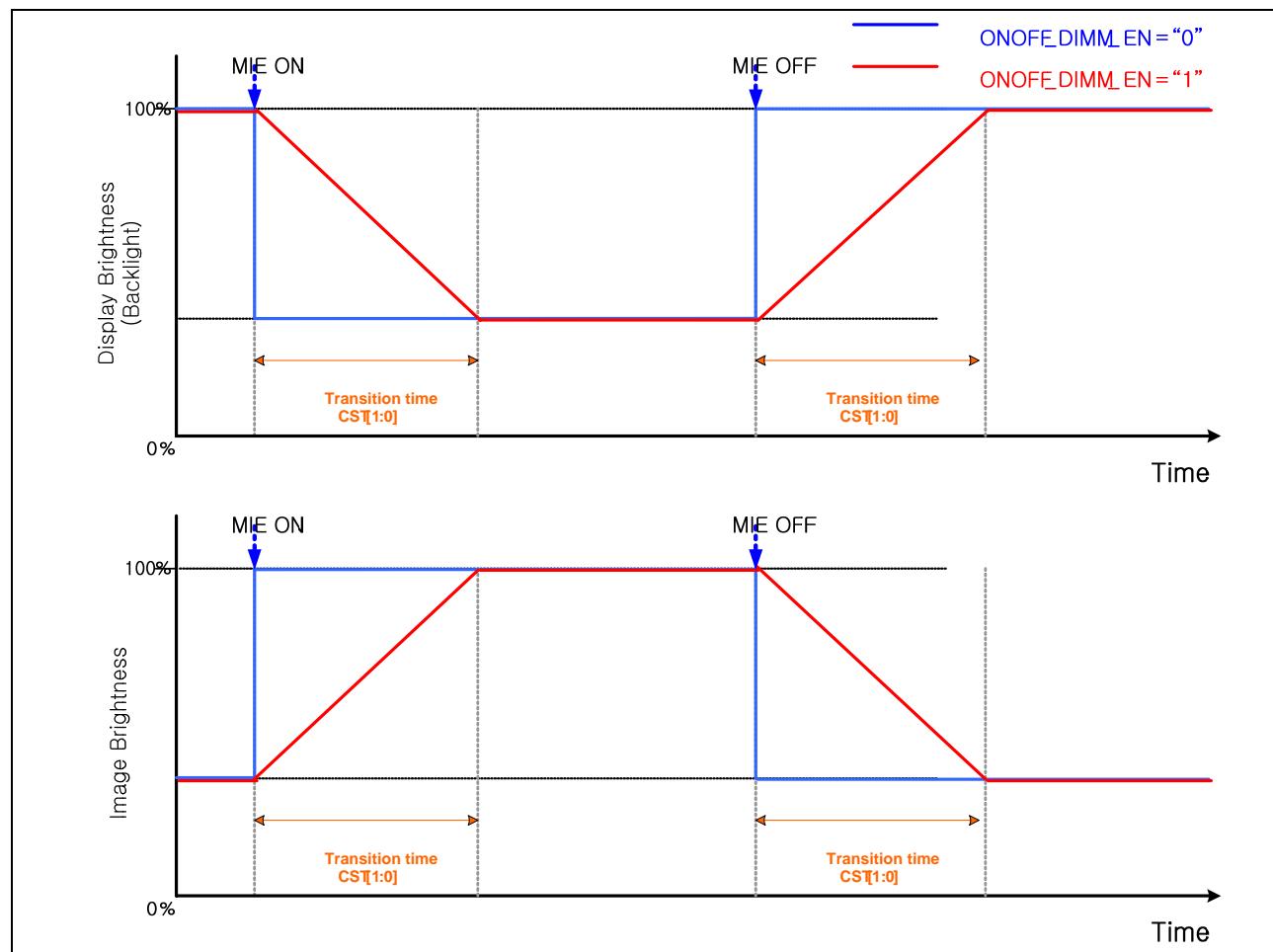
If the ONOFF\_DIMM\_EN is “1”, the MIE is smoothly turning on or off. When the ONOFF\_DIMM\_EN is “0”, the MIE is turning on or off immediately. The transition time is controlled by CST[1:0].

If the MIE mode is changed during on/off dimming transition, it will be updated after finishing the dimming transition.

**Table 122. ONOFF\_DIMM\_EN**

ONOFF_DIMM_EN	On / Off Dimming Function
0	Disable
1	Enable

Status	Default Value
Initial	ONOFF_DIMM_EN = 0



**Figure 139. Example of MIE on / off dimming transition control**

## 5.2.41.4. SERC[4:0]

This register is used to adjust the Image Saturation Enhancement Rate.

$$\text{Adjusted_Saturation_Enhancement_Rate} = \text{Saturation_Enhancement_Rate} \times \frac{\text{SERC}}{16}$$

Figure 140. Saturation enhancement rate

If the value of SERC is '0', there is no saturation enhancement in output image. If the value of SERC is increased, the saturation enhancement rate will be increased and more vivid image is obtained. The other way, if the value of SERC is decreased, the saturation enhancement rate will be decreased.

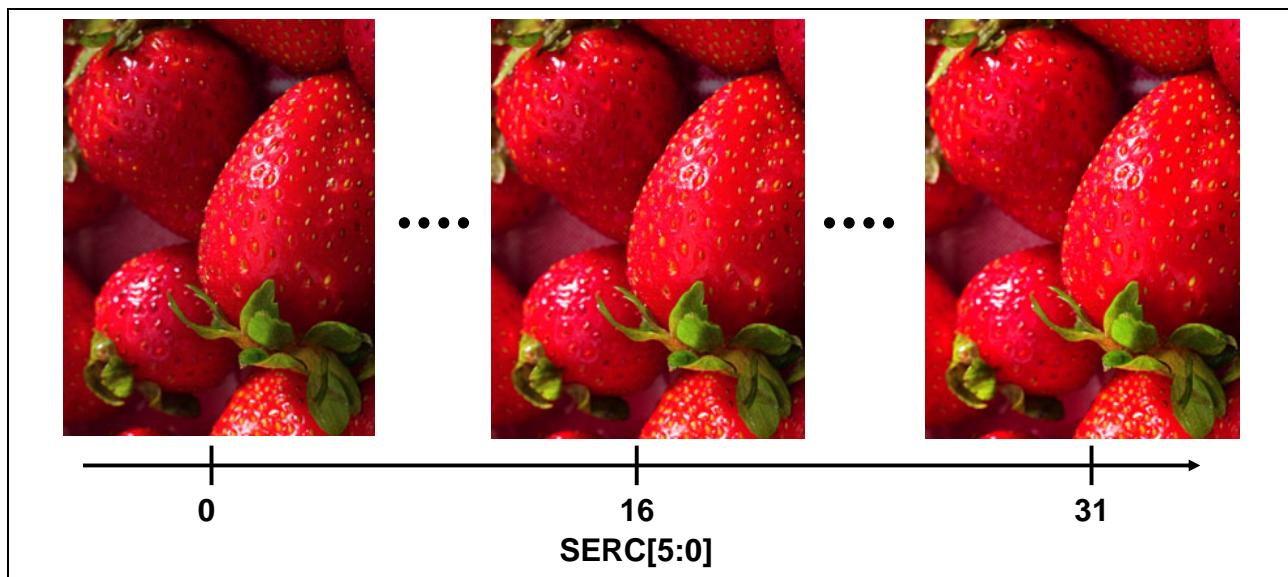


Figure 141. Example of SERC

**Table 123. SERC[4:0]**

<b>SERC[4:0]</b>	<b>Adjust Saturation Enhancement Rate</b>
00000	Saturation Enhancement Rate x 0/16
00001	Saturation Enhancement Rate x 1/16
00010	Saturation Enhancement Rate x 2/16
...	...
10000	Saturation Enhancement Rate x 16/16
...	...
11101	Saturation Enhancement Rate x 29/16
11110	Saturation Enhancement Rate x 30/16
11111	Saturation Enhancement Rate x 31/16

<b>Status</b>	<b>Default Value</b>
Initial	SERC[4:0] = 10000

### 5.2.42. BCMODE : Write BL Control Mode (CBh)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BCMODE	W	0	1	1	0	0	1	0	1	1	CB
1 <sup>st</sup> para		1	0	0	0	0	0	0	BC_MODE [1]	BC_MODE [0]	-

This command is used to select the source of brightness value for the display brightness calculation.

**Table 124. BC\_MODE[1:0]**

BC_MODE[1:0]	Brightness Source
00	Setting disabled
01	Manual Brightness
10	MIE Brightness
11	Merged Brightness (MIE + Manual)

Status	Default Value
Initial	BC_MODE[1:0] = 01

### 5.3. DESCRIPTION OF LEVEL2 COMMAND

Command Description Tables are explained by 80mode Interface standard.

Level2 Commands are not readable in SPI.

#### 5.3.1. DSTB : Deep Stand By mode (B0h)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DSTB	W	0	1	0	1	1	0	0	0	0	B0
1 <sup>st</sup> para		1	0	0	0	0	0	0	0	DSTB	-

**DSTB:** When DSTB = 1, the S6D04M0 enters the deep standby mode, where the power supply for the internal logic is off to save more power than the standby mode. The GRAM data and the instruction sets are prohibited during the deep standby mode and they must be reset after releasing from the deep standby mode.

Status	Default Value
Intial	DSTB = 0

### 5.3.2. MIECTL2 : Write MIE Control 2 (CCh)

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MIECTL2	W	0	1	1	0	0	1	1	0	0	CC
1 <sup>st</sup> para		1	0	0	CAT [1]	CAT [0]	CST [1]	CST [0]	WIN [8]	VADDR0 [7]	-
2 <sup>nd</sup> para		1	WIN [6]	WIN [5]	WIN [4]	WIN [3]	WIN [2]	WIN [1]	WIN [0]	VADDR0 [8]	-
3 <sup>rd</sup> para		1	WIN [7]	WIN [6]	WIN [5]	WIN [4]	WIN [3]	WIN [2]	WIN [1]	VADDR1 [0]	-
4 <sup>th</sup> para		1	0	0	0	0	0	0	0	0	-
5 <sup>th</sup> para		1	1	1	1	0	1	1	1	1	-

#### 5.3.2.1. CAT[1:0]

This register is used to select the abrupt transition time. The MIE has two transition times based on image contents for preventing abnormal visible artifacts (e.g. flicker). The MIE controls transition time between CAT and CST automatically in moving mode (MIE\_MODE = "11").

- Abrupt transition time: If input image is changed abruptly, short transition time is needed.
- Smooth transition time: If input image is changed smoothly, long transition time is needed.

**Table 125. CAT[1:0]**

CAT[1:0]	Abrupt Transition Time
00	1 frame
01	2 frames
10	4 frames
11	8 frames

Status	Default Value
Initial	CAT[1:0] = 10

## 5.3.2.2. CST [1 : 0]

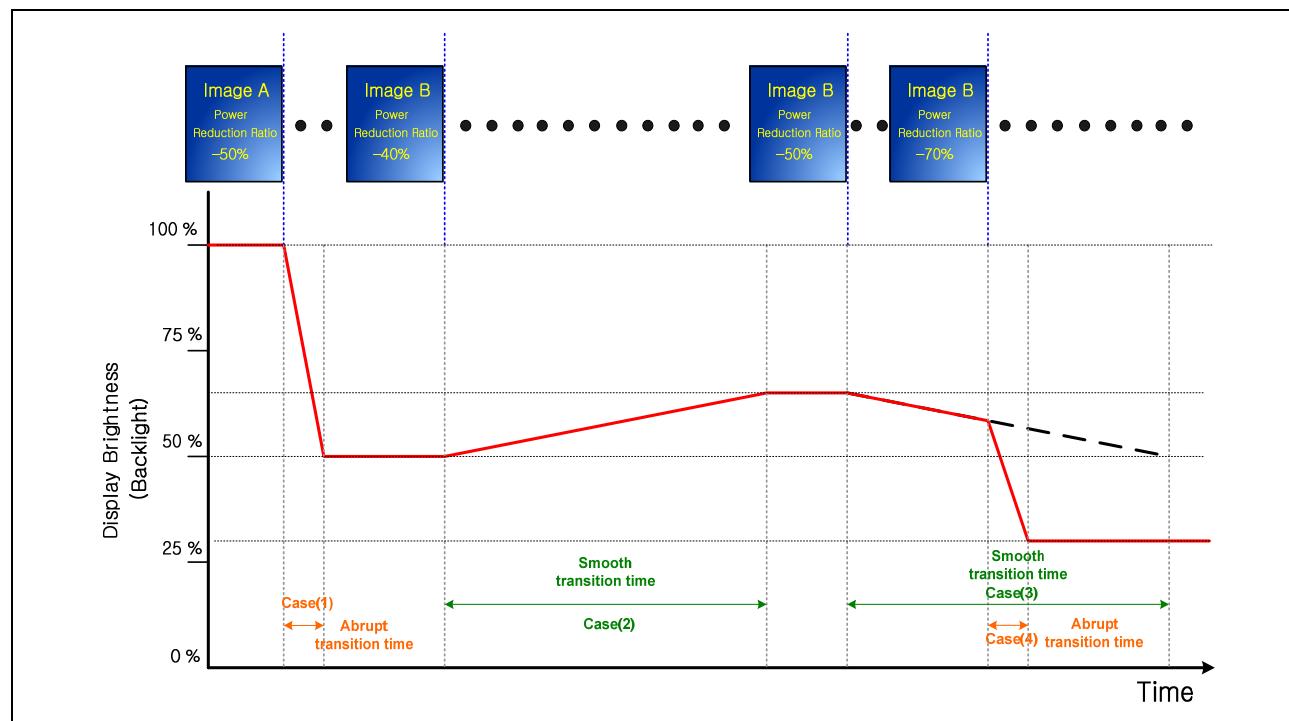
This register is used to select the smooth transition time

**Table 126. CST[1:0]**

CST[1:0]	Smooth Transition Time
00	32 frames
01	64 frames
10	96 frames
11	128 frames

Status	Default Value
Initial	CST[1:0] = 00

An example of MIE transition time is illustrated as below. If the input image is changed abruptly, the MIE has an abrupt transition time “case (1)” and if the input image is changed smoothly, the MIE has a smooth transition time “case (2)”. The display brightness changes to target brightness abruptly “case (4)” when the abrupt change of image is happened during the smooth transition “case (3)”.

**Figure 142. Example of MIE transition control**

## 5.3.2.3. WINVADDR0[8:0]

This register is used to set the vertical start address of MIE window.

**Table 127. WINVADDR0[8:0]**

WINVADDR0[8:0]	Vertical Start Address of MIE Window
0_0000_0000	0
0_0000_0001	1
0_0000_0010	2
0_0000_0011	3
...	...
1_0011_0101	309
1_0011_0110	310
1_0011_1110	Setting disabled
...	...
1_1111_1111	Setting disabled

Status	Default Value
Initial	WINVADDR0[8:0] = 0_0000_0000

Note: WINVADDR1 – WINVADDR0 ≥ 100

## 5.3.2.4. WINVADDR1[8:0]

This register is used to set the vertical end address of MIE window.

**Table 128. WINVADDR1[8:0]**

WINVADDR1[8:0]	Vertical End Address of MIE Window
0_0000_0000	Setting disabled
0_0000_0001	Setting disabled
0_0000_0010	Setting disabled
0_0000_0011	Setting disabled
0_0000_0100	Setting disabled
0_0000_0101	Setting disabled
0_0000_0110	Setting disabled
0_0000_0111	Setting disabled
0_0000_1000	8
0_0000_1001	9
...	...
1_0011_1110	318
1_0011_1111	319
1_0100_0000	Setting disabled
...	...
1_1111_1111	Setting disabled

Status	Default Value
Initial	WINVADDR1[8:0] = 1_0011_1111

Note: WINVADDR1 – WINVADDR0 ≥ 100

The MIE can select the window area which is used to analysis and enhance input image. The outside area of the MIE window is not used to MIE analysis and there is no image enhancement.

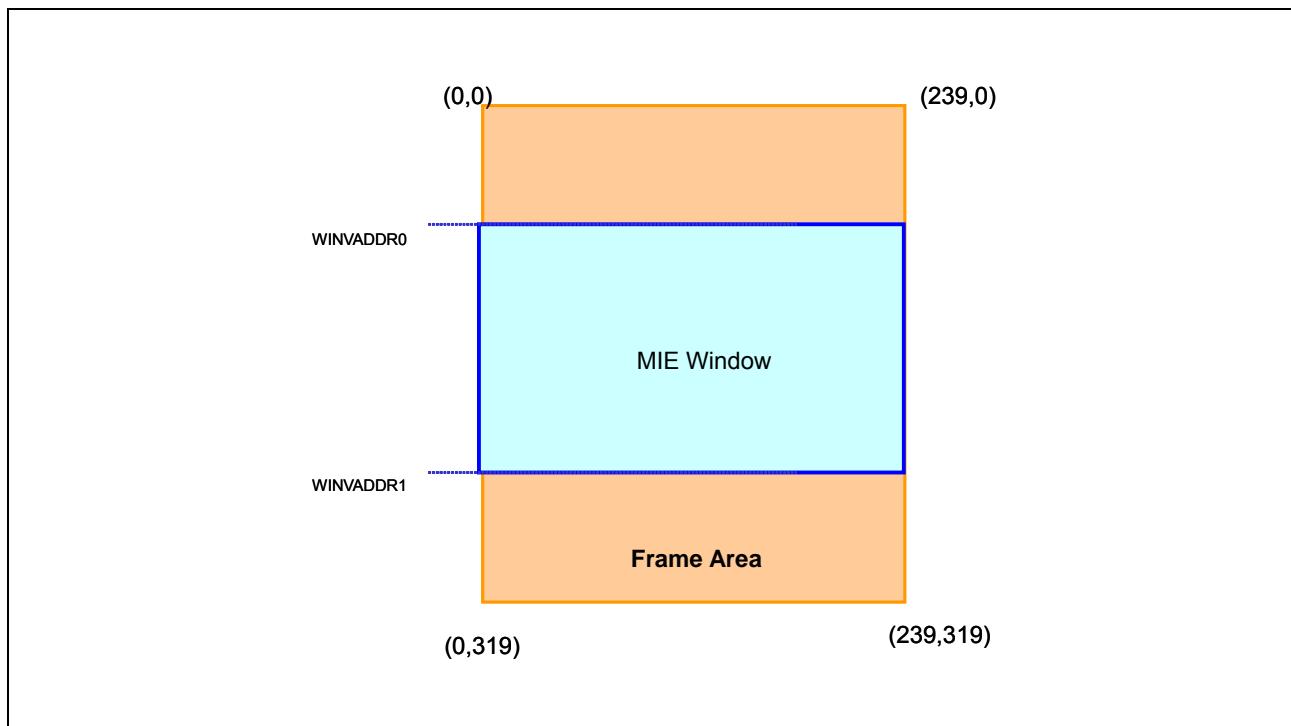


Figure 143. MIE window

### 5.3.3. MIE Control3 (CDh) : Write BL Control

Inst/Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MIECTL3	W	0	1	1	0	0	1	1	0	1	CD
1 <sup>st</sup> para		1	0	BC_ FRQ_ SEL[6]	BC_ FRQ_ SEL[5]	BC_ FRQ_ SEL[4]	BC_ FRQ_ SEL[3]	BC_ FRQ_ SEL[2]	BC_ FRQ_ SEL[1]	BC_ FRQ_ SEL[0]	-
2 <sup>nd</sup> para		1	BL_ MODE_ INSLP	0	DT [2]	DT [1]	DT [0]	BL_ DRV_EN	BL_ DIMM_ STEP[1]	BL_ DIMM_ STEP[0]	-

#### 5.3.3.1. BC\_FRQ\_SEL[6:0]

This register is used to select the frequency of BC. To select the BC frequency, two registers are needed. Those register are BC\_FRQ\_SEL[6:0] and BL\_DIMM\_STEP[1:0].

For details, refer to the table of BC frequency.

Status	Default Value
Initial	BC_FRQ_SEL[6:0] = 000_0001

#### 5.3.3.2. BL\_MODE\_IN\_SLP

This register is used to select the state of BC when driver IC is sleep in mode.

Table 129. BL\_MODE\_IN\_SLP

BL_MODE_IN_SLP	State of BC
0	Low
1	High

Status	Default Value
Initial	BL_MODE_IN_SLP = 0

Table 130. State of BC

Pin	State					
	Hard Reset	SW Reset	SLPIN		SPLOUT	
			Display On	Display Off	Display On	Display Off
BC	Low	Low	Fixed as BL_MODE_IN_SLP		Active	Low

### 5.3.3.3. DT[2:0]

This register is used to select the transition time of the manual dimming function.

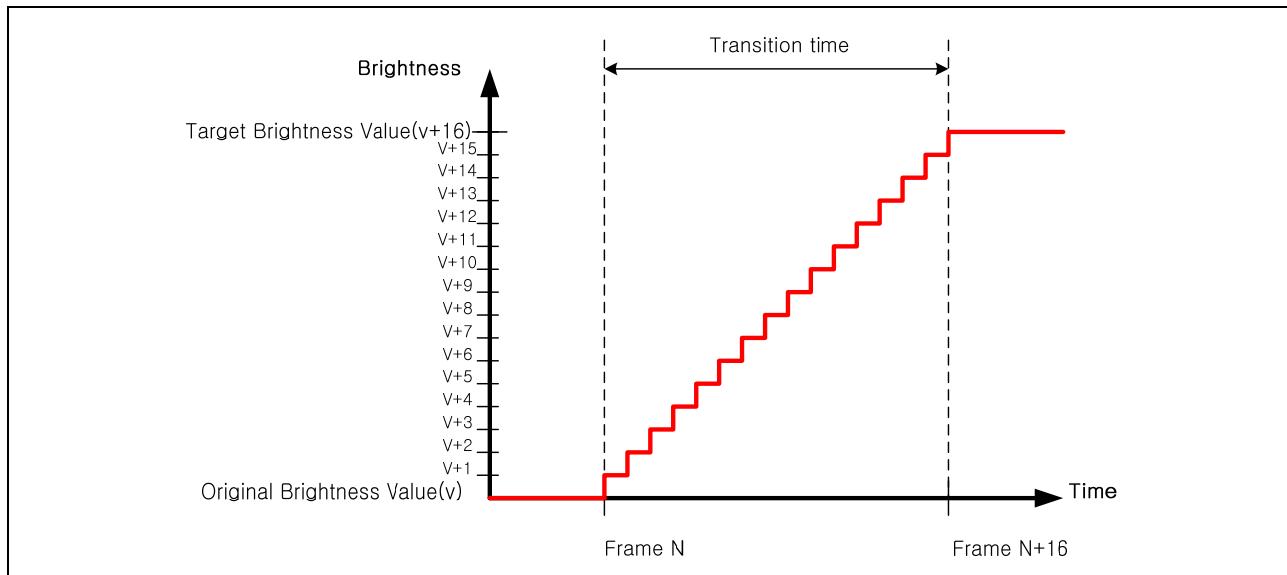
**Table 131. DT[2:0]**

DT[2:0]	Transition Time	Dimming Step
000	16 frames	16
001	24 frames	24
010	32 frames	32
011	40 frames	40
100	48 frames	48
101	56 frames	56
110	64 frames	64
111	72 frames	72

$$\text{Transition Time} = (\text{DT}[2:0] + 2) \times 8 \times \frac{1}{\text{Display Frequency}}$$

**Figure 144. Transition time of manual dimming function**

Status	Default Value
Initial	DT[2:0] = 010



**Figure 145. Example of dimming function (DT[2:0] = 000)**

### 5.3.3.4. BL\_DRV\_EN

This register is used to enable the LED driver IC when the IC needs the chip enable signal. This signal is outputted to BC\_CTL pad.

**Table 132. BL\_DRV\_EN**

BL_DRV_EN	State of BC_CTL Pad
0	Low
1	High

Status	Default Value
Initial	BL_DRV_EN = 1

### 5.3.3.5. BL\_DIMM\_STEP[1:0]

This register is used to select the dimming step of BC level. It is used to select the frequency of BC with BC\_FRQ\_SEL[6:0].

**Table 133. BL\_DIMM\_STEP[1:0]**

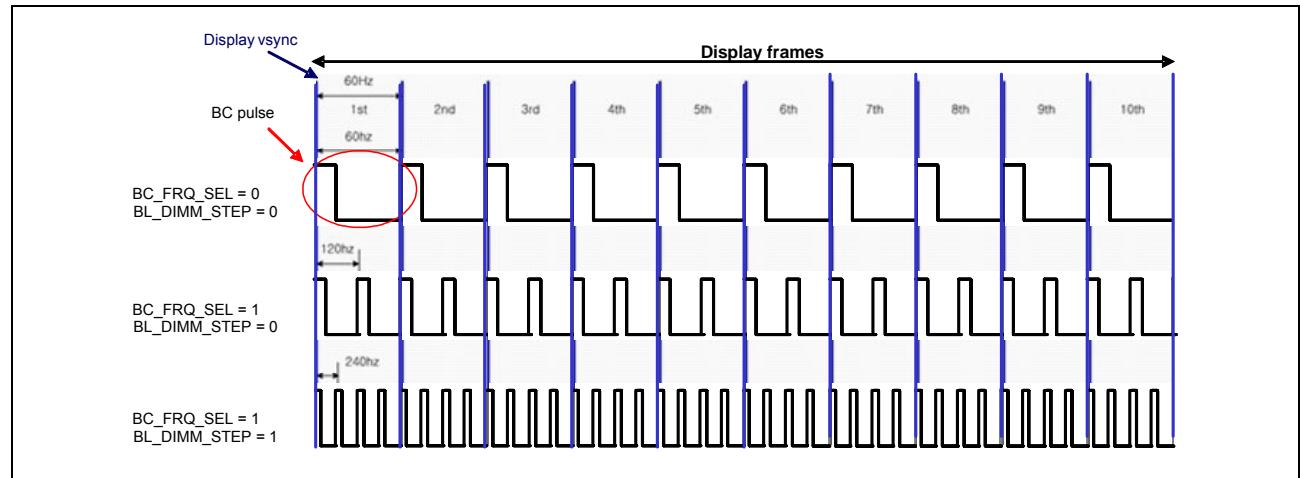
BL_DIMM_STEP[1:0]	Dimming Steps of BC
00	256
01	128
10	64
11	Setting Disable

Status	Default Value
Initial	BL_DIMM_STEP[1:0] = 00

The BC frequency is calculated with the following formula.

$$\text{Num. of BC/1 frame} = (\text{BC\_FRQ\_SEL} + 1) \times 2^{\text{BL\_DIMM\_STEP}}$$

**Figure 146. Calculation formula of BC frequency**



**Figure 147. Example of BC frequency selection**

Table 134. BC frequency

		BC Frequency [Hz]					BC Frequency [Hz]				
BL_DIMM STEP[1:0]		00	01	10	BL_DIMM STEP[1:0]		00	01	10		
Dimming Step No.	256	128	64	Dimming Step No.	256	128	64	Dimming Step No.	256	128	64
0000000	F.F. x 1	F.F. x 2	F.F. x 4	0000000	F.F. x 65	F.F. x 130	F.F. x 260	0000000	F.F. x 65	F.F. x 130	F.F. x 260
0000001	F.F. x 2	F.F. x 4	F.F. x 8	0000001	F.F. x 66	F.F. x 132	F.F. x 264	0000001	F.F. x 66	F.F. x 132	F.F. x 264
0000010	F.F. x 3	F.F. x 6	F.F. x 12	0000010	F.F. x 67	F.F. x 134	F.F. x 268	0000010	F.F. x 67	F.F. x 134	F.F. x 268
0000011	F.F. x 4	F.F. x 8	F.F. x 16	0000011	F.F. x 68	F.F. x 136	F.F. x 272	0000011	F.F. x 68	F.F. x 136	F.F. x 272
0000100	F.F. x 5	F.F. x 10	F.F. x 20	0000100	F.F. x 69	F.F. x 138	F.F. x 276	0000100	F.F. x 69	F.F. x 138	F.F. x 276
0000101	F.F. x 6	F.F. x 12	F.F. x 24	0000101	F.F. x 70	F.F. x 140	F.F. x 280	0000101	F.F. x 70	F.F. x 140	F.F. x 280
0000110	F.F. x 7	F.F. x 14	F.F. x 28	0000110	F.F. x 71	F.F. x 142	F.F. x 284	0000110	F.F. x 71	F.F. x 142	F.F. x 284
0000111	F.F. x 8	F.F. x 16	F.F. x 32	0000111	F.F. x 72	F.F. x 144	F.F. x 288	0000111	F.F. x 72	F.F. x 144	F.F. x 288
0001000	F.F. x 9	F.F. x 18	F.F. x 36	0001000	F.F. x 73	F.F. x 146	F.F. x 292	0001000	F.F. x 73	F.F. x 146	F.F. x 292
0001001	F.F. x 10	F.F. x 20	F.F. x 40	0001001	F.F. x 74	F.F. x 148	F.F. x 296	0001001	F.F. x 74	F.F. x 148	F.F. x 296
0001010	F.F. x 11	F.F. x 22	F.F. x 44	0001010	F.F. x 75	F.F. x 150	F.F. x 300	0001010	F.F. x 75	F.F. x 150	F.F. x 300
0001011	F.F. x 12	F.F. x 24	F.F. x 48	0001011	F.F. x 76	F.F. x 152	F.F. x 304	0001011	F.F. x 76	F.F. x 152	F.F. x 304
0001100	F.F. x 13	F.F. x 26	F.F. x 52	0001100	F.F. x 77	F.F. x 154	F.F. x 308	0001100	F.F. x 77	F.F. x 154	F.F. x 308
0001101	F.F. x 14	F.F. x 28	F.F. x 56	0001101	F.F. x 78	F.F. x 156	F.F. x 312	0001101	F.F. x 78	F.F. x 156	F.F. x 312
0001110	F.F. x 15	F.F. x 30	F.F. x 60	0001110	F.F. x 79	F.F. x 158	F.F. x 316	0001110	F.F. x 79	F.F. x 158	F.F. x 316
0001111	F.F. x 16	F.F. x 32	F.F. x 64	0001111	F.F. x 80	F.F. x 160	F.F. x 320	0001111	F.F. x 80	F.F. x 160	F.F. x 320
0010000	F.F. x 17	F.F. x 34	F.F. x 68	0010000	F.F. x 81	F.F. x 162	F.F. x 324	0010000	F.F. x 81	F.F. x 162	F.F. x 324
0010001	F.F. x 18	F.F. x 36	F.F. x 72	0010001	F.F. x 82	F.F. x 164	F.F. x 328	0010001	F.F. x 82	F.F. x 164	F.F. x 328
0010010	F.F. x 19	F.F. x 38	F.F. x 76	0010010	F.F. x 83	F.F. x 166	F.F. x 332	0010010	F.F. x 83	F.F. x 166	F.F. x 332
0010011	F.F. x 20	F.F. x 40	F.F. x 80	0010011	F.F. x 84	F.F. x 168	F.F. x 336	0010011	F.F. x 84	F.F. x 168	F.F. x 336
0010100	F.F. x 21	F.F. x 42	F.F. x 84	0010100	F.F. x 85	F.F. x 170	F.F. x 340	0010100	F.F. x 85	F.F. x 170	F.F. x 340
0010101	F.F. x 22	F.F. x 44	F.F. x 88	0010101	F.F. x 86	F.F. x 172	F.F. x 344	0010101	F.F. x 86	F.F. x 172	F.F. x 344
0010110	F.F. x 23	F.F. x 46	F.F. x 92	0010110	F.F. x 87	F.F. x 174	F.F. x 348	0010110	F.F. x 87	F.F. x 174	F.F. x 348
0010111	F.F. x 24	F.F. x 48	F.F. x 96	0010111	F.F. x 88	F.F. x 176	F.F. x 352	0010111	F.F. x 88	F.F. x 176	F.F. x 352
0011000	F.F. x 25	F.F. x 50	F.F. x 100	0011000	F.F. x 89	F.F. x 178	F.F. x 356	0011000	F.F. x 89	F.F. x 178	F.F. x 356
0011001	F.F. x 26	F.F. x 52	F.F. x 104	0011001	F.F. x 90	F.F. x 180	F.F. x 360	0011001	F.F. x 90	F.F. x 180	F.F. x 360
0011010	F.F. x 27	F.F. x 54	F.F. x 108	0011010	F.F. x 91	F.F. x 182	F.F. x 364	0011010	F.F. x 91	F.F. x 182	F.F. x 364
0011011	F.F. x 28	F.F. x 56	F.F. x 112	0011011	F.F. x 92	F.F. x 184	F.F. x 368	0011011	F.F. x 92	F.F. x 184	F.F. x 368
0011100	F.F. x 29	F.F. x 58	F.F. x 116	0011100	F.F. x 93	F.F. x 186	F.F. x 372	0011100	F.F. x 93	F.F. x 186	F.F. x 372
0011101	F.F. x 30	F.F. x 60	F.F. x 120	0011101	F.F. x 94	F.F. x 188	F.F. x 376	0011101	F.F. x 94	F.F. x 188	F.F. x 376
0011110	F.F. x 31	F.F. x 62	F.F. x 124	0011110	F.F. x 95	F.F. x 190	F.F. x 380	0011110	F.F. x 95	F.F. x 190	F.F. x 380
0011111	F.F. x 32	F.F. x 64	F.F. x 128	0011111	F.F. x 96	F.F. x 192	F.F. x 384	0011111	F.F. x 96	F.F. x 192	F.F. x 384
0100000	F.F. x 33	F.F. x 66	F.F. x 132	0100000	F.F. x 97	F.F. x 194	F.F. x 388	0100000	F.F. x 97	F.F. x 194	F.F. x 388
0100001	F.F. x 34	F.F. x 68	F.F. x 136	0100001	F.F. x 98	F.F. x 196	F.F. x 392	0100001	F.F. x 98	F.F. x 196	F.F. x 392
0100010	F.F. x 35	F.F. x 70	F.F. x 140	0100010	F.F. x 99	F.F. x 198	F.F. x 396	0100010	F.F. x 99	F.F. x 198	F.F. x 396
0100011	F.F. x 36	F.F. x 72	F.F. x 144	0100011	F.F. x 100	F.F. x 200	F.F. x 400	0100011	F.F. x 100	F.F. x 200	F.F. x 400
0100100	F.F. x 37	F.F. x 74	F.F. x 148	0100100	F.F. x 101	F.F. x 202	F.F. x 404	0100100	F.F. x 101	F.F. x 202	F.F. x 404
0100101	F.F. x 38	F.F. x 76	F.F. x 152	0100101	F.F. x 102	F.F. x 204	F.F. x 408	0100101	F.F. x 102	F.F. x 204	F.F. x 408
0100110	F.F. x 39	F.F. x 78	F.F. x 156	0100110	F.F. x 103	F.F. x 206	F.F. x 412	0100110	F.F. x 103	F.F. x 206	F.F. x 412
0100111	F.F. x 40	F.F. x 80	F.F. x 160	0100111	F.F. x 104	F.F. x 208	F.F. x 416	0100111	F.F. x 104	F.F. x 208	F.F. x 416
0101000	F.F. x 41	F.F. x 82	F.F. x 164	0101000	F.F. x 105	F.F. x 210	F.F. x 420	0101000	F.F. x 105	F.F. x 210	F.F. x 420
0101001	F.F. x 42	F.F. x 84	F.F. x 168	0101001	F.F. x 106	F.F. x 212	F.F. x 424	0101001	F.F. x 106	F.F. x 212	F.F. x 424
0101010	F.F. x 43	F.F. x 86	F.F. x 172	0101010	F.F. x 107	F.F. x 214	F.F. x 428	0101010	F.F. x 107	F.F. x 214	F.F. x 428
0101011	F.F. x 44	F.F. x 88	F.F. x 176	0101011	F.F. x 108	F.F. x 216	F.F. x 432	0101011	F.F. x 108	F.F. x 216	F.F. x 432
0101100	F.F. x 45	F.F. x 90	F.F. x 180	0101100	F.F. x 109	F.F. x 218	F.F. x 436	0101100	F.F. x 109	F.F. x 218	F.F. x 436
0101101	F.F. x 46	F.F. x 92	F.F. x 184	0101101	F.F. x 110	F.F. x 220	F.F. x 440	0101101	F.F. x 110	F.F. x 220	F.F. x 440
0101110	F.F. x 47	F.F. x 94	F.F. x 188	0101110	F.F. x 111	F.F. x 222	F.F. x 444	0101110	F.F. x 111	F.F. x 222	F.F. x 444
0101111	F.F. x 48	F.F. x 96	F.F. x 192	0101111	F.F. x 112	F.F. x 224	F.F. x 448	0101111	F.F. x 112	F.F. x 224	F.F. x 448
0110000	F.F. x 49	F.F. x 98	F.F. x 196	0110000	F.F. x 113	F.F. x 226	F.F. x 452	0110000	F.F. x 113	F.F. x 226	F.F. x 452
0110001	F.F. x 50	F.F. x 100	F.F. x 200	0110001	F.F. x 114	F.F. x 228	F.F. x 456	0110001	F.F. x 114	F.F. x 228	F.F. x 456
0110010	F.F. x 51	F.F. x 102	F.F. x 204	0110010	F.F. x 115	F.F. x 230	F.F. x 460	0110010	F.F. x 115	F.F. x 230	F.F. x 460
0110011	F.F. x 52	F.F. x 104	F.F. x 208	0110011	F.F. x 116	F.F. x 232	F.F. x 464	0110011	F.F. x 116	F.F. x 232	F.F. x 464
0110100	F.F. x 53	F.F. x 106	F.F. x 212	0110100	F.F. x 117	F.F. x 234	F.F. x 468	0110100	F.F. x 117	F.F. x 234	F.F. x 468
0110101	F.F. x 54	F.F. x 108	F.F. x 216	0110101	F.F. x 118	F.F. x 236	F.F. x 472	0110101	F.F. x 118	F.F. x 236	F.F. x 472
0110110	F.F. x 55	F.F. x 110	F.F. x 220	0110110	F.F. x 119	F.F. x 238	F.F. x 476	0110110	F.F. x 119	F.F. x 238	F.F. x 476
0110111	F.F. x 56	F.F. x 112	F.F. x 224	0110111	F.F. x 120	F.F. x 240	F.F. x 480	0110111	F.F. x 120	F.F. x 240	F.F. x 480
0111000	F.F. x 57	F.F. x 114	F.F. x 228	0111000	F.F. x 121	F.F. x 242	F.F. x 484	0111000	F.F. x 121	F.F. x 242	F.F. x 484
0111001	F.F. x 58	F.F. x 116	F.F. x 232	0111001	F.F. x 122	F.F. x 244	F.F. x 488	0111001	F.F. x 122	F.F. x 244	F.F. x 488
0111010	F.F. x 59	F.F. x 118	F.F. x 236	0111010	F.F. x 123	F.F. x 246	F.F. x 492	0111010	F.F. x 123	F.F. x 246	F.F. x 492
0111011	F.F. x 60	F.F. x 120	F.F. x 240	0111011	F.F. x 124	F.F. x 248	F.F. x 496	0111011	F.F. x 124	F.F. x 248	F.F. x 496
0111100	F.F. x 61	F.F. x 122	F.F. x 244	0111100	F.F. x 125	F.F. x 250	F.F. x 500	0111100	F.F. x 125	F.F. x 250	F.F. x 500
0111101	F.F. x 62	F.F. x 124	F.F. x 248	0111101	F.F. x 126	F.F. x 252	F.F. x 504	0111101	F.F. x 126	F.F. x 252	F.F. x 504
0111110	F.F. x 63	F.F. x 126	F.F. x 252	0111110	F.F. x 127	F.F. x 254	F.F. x 508	0111110	F.F. x 127	F.F. x 254	F.F. x 508
0111111	F.F. x 64	F.F. x 128	F.F. x 256	0111111	F.F. x 128	F.F. x 256	F.F. x 512	0111111	F.F. x 128	F.F. x 256	F.F. x 512

Note: F.F. means Frame Frequency.

When the display frame frequency is 60Hz, BC frequency is represented at the table below.

Table 135. Example of BC frequency selection

		BC Frequency [Hz]					BC Frequency [Hz]		
BL_DIMM STEP[1:0]		00	01	10	BL_DIMM STEP[1:0]		00	01	10
Dimming Step No.		256	128	64	Dimming Step No.		256	128	64
BC_FRQ_SEL[6:0]	0000000	60	120	240	1000000	3900	7800	15600	
	0000001	120	240	480	1000001	3960	7920	15840	
	0000010	180	360	720	1000010	4020	8040	16080	
	0000011	240	480	960	1000011	4080	8160	16320	
	0000100	300	600	1200	1000100	4140	8280	16560	
	0000101	360	720	1440	1000101	4200	8400	16800	
	0000110	420	840	1680	1000110	4260	8520	17040	
	0000111	480	960	1920	1000111	4320	8640	17280	
	0001000	540	1080	2160	1001000	4380	8760	17520	
	0001001	600	1200	2400	1001001	4440	8880	17760	
	0001010	660	1320	2640	1001010	4500	9000	18000	
	0001011	720	1440	2880	1001011	4560	9120	18240	
	0001100	780	1560	3120	1001100	4620	9240	18480	
	0001101	840	1680	3360	1001101	4680	9360	18720	
	0001110	900	1800	3600	1001110	4740	9480	18960	
	0001111	960	1920	3840	1001111	4800	9600	19200	
	0010000	1020	2040	4080	1010000	4860	9720	19440	
	0010001	1080	2160	4320	1010001	4920	9840	19680	
	0010010	1140	2280	4560	1010010	4980	9960	19920	
	0010011	1200	2400	4800	1010011	5040	10080	20160	
	0010100	1260	2520	5040	1010100	5100	10200	20400	
	0010101	1320	2640	5280	1010101	5160	10320	20640	
	0010110	1380	2760	5520	1010110	5220	10440	20880	
	0010111	1440	2880	5760	1010111	5280	10560	21120	
	0011000	1500	3000	6000	1011000	5340	10680	21360	
	0011001	1560	3120	6240	1011001	5400	10800	21600	
	0011010	1620	3240	6480	1011010	5460	10920	21840	
	0011011	1680	3360	6720	1011011	5520	11040	22080	
	0011100	1740	3480	6960	1011100	5580	11160	22320	
	0011101	1800	3600	7200	1011101	5640	11280	22560	
	0011110	1860	3720	7440	1011110	5700	11400	22800	
	0011111	1920	3840	7680	1011111	5760	11520	23040	
	0100000	1980	3960	7920	1100000	5820	11640	23280	
	0100001	2040	4080	8160	1100001	5880	11760	23520	
	0100010	2100	4200	8400	1100010	5940	11880	23760	
	0100011	2160	4320	8640	1100011	6000	12000	24000	
	0100100	2220	4440	8880	1100100	6060	12120	24240	
	0100101	2280	4560	9120	1100101	6120	12240	24480	
	0100110	2340	4680	9360	1100110	6180	12360	24720	
	0100111	2400	4800	9600	1100111	6240	12480	24960	
	0101000	2460	4920	9840	1101000	6300	12600	25200	
	0101001	2520	5040	10080	1101001	6360	12720	25440	
	0101010	2580	5160	10320	1101010	6420	12840	25680	
	0101011	2640	5280	10560	1101011	6480	12960	25920	
	0101100	2700	5400	10800	1101100	6540	13080	26160	
	0101101	2760	5520	11040	1101101	6600	13200	26400	
	0101110	2820	5640	11280	1101110	6660	13320	26640	
	0101111	2880	5760	11520	1101111	6720	13440	26880	
	0110000	2940	5880	11760	1110000	6780	13560	27120	
	0110001	3000	6000	12000	1110001	6840	13680	27360	
	0110010	3060	6120	12240	1110010	6900	13800	27600	
	0110011	3120	6240	12480	1110011	6960	13920	27840	
	0110100	3180	6360	12720	1110100	7020	14040	28080	
	0110101	3240	6480	12960	1110101	7080	14160	28320	
	0110110	3300	6600	13200	1110110	7140	14280	28560	
	0110111	3360	6720	13440	1110111	7200	14400	28800	
	0111000	3420	6840	13680	1111000	7260	14520	29040	
	0111001	3480	6960	13920	1111001	7320	14640	29280	
	0111010	3540	7080	14160	1111010	7380	14760	29520	
	0111011	3600	7200	14400	1111011	7440	14880	29760	
	0111100	3660	7320	14640	1111100	7500	15000	30000	
	0111101	3720	7440	14880	1111101	7560	15120	30240	
	0111110	3780	7560	15120	1111110	7620	15240	30480	
	0111111	3840	7680	15360	1111111	7680	15360	30720	

### 5.3.4. MTPCTL: MTP Control Command (D0h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MTPCTL	R/W	0	1	1	0	1	0	0	0	0	D0h
1 <sup>st</sup> para		1	0	0	0	0	ID_SEL	MTP_SEL	MTP_MODE	MTP_EX	
2 <sup>nd</sup> para		1	0	0	0	0	0	MTP_ERB	MTP_LOAD	MTP_WRB	

#### 5.3.4.1. ID\_SEL/ MTP\_SEL/ MTP\_MODE/ MTP\_EX

**ID\_SEL:** Select the ID register.

**Table 136.ID\_SEL**

ID_SEL	ID1/ID2/ID3 Data
0	ID1/ID2/ID3 Register
1	MTP data

**MTP\_SEL:** Select the VCOMH voltage setting register.

**Table 137.MTP\_SEL**

MTP_SEL	VCOMH Control Data
0	VCMOC/VMLOC/GVDDOC Register
1	MTP data

**MTP\_MODE:** Set the 2<sup>nd</sup> booster operating condition. When MTP\_MODE = 0, the 2<sup>nd</sup> booster operates as a user-specified condition. VGH/VGL voltages are generated as a designated level by BT2-0 setting. If MTP\_MODE = 1, available BT2-0 settings are limited only '010' & '101'.

**Table 138.MTP\_MODE**

MTP_MODE	MTP operation mode
0	All BT2-0 settings are available (Normal operating condition)
1	Setting of BT2-0 is limited. (An MTP-programming / erasing condition)

Note. Do not execute MTP programming / erasing operation when MTP\_MODE = 0.



**MTP\_EX:** Select MTP power supply source.

When MTP\_EX = 0, Internally generated VGH voltage is used as a MTP-programming / erasing potential.

If MTP\_EX = 1, External power should be applied for programming / erasing MTP via VGH pad.

**Table 139. MTP\_EX**

MTP_EX	Erase / Initial / Program supply
0	Used internally generated VGH
1	Needed external power supply

Note. MTP\_EX register is valid only in case that MTP\_MODE = 1. Do not access MTP\_EX register when MTP\_MODE = 0.

Status	Default Value
Initial	ID_SEL = 1 MTP_SEL = 1 MTP_MODE = 0 MTP_EX = 0

#### 5.3.4.2. MTP\_ERB/ MTP\_LOAD/ MTP\_WRB

**MTP\_ERB:** Enable bit for MTP initialization or erasure.

When MTP\_ERB = 0, MTP initialization or erasure is enabled.

**MTP\_LOAD:** When MTP\_LOAD is High, MTP data is loaded into an internal register.

**MTP\_WRB:** MTP Write enable bit. If MTP cell is to be written, set MTP\_WRB = 0

Status	Default Value
Initial	MTP_ERB = 1 MTP_LOAD = 0 MTP_WRB = 1

### 5.3.5. WRVCMOC : Set VCOM Offset Control (D1h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRVCM OC	R/W	0	1	1	0	1	0	0	0	1	D1h
1 <sup>st</sup> para		1	0	0	0	VCMO C4	VCMO C3	VCMO C2	VCMO C1	VCMO C0	

#### 5.3.5.1. VCMOC [4:0]

VCMOC4-0 contains VCM Offset data. This MTP data and VCM register determine VCOMH level.

$$\text{TOTAL\_VCM}[6:0] = \text{VCM}[6:0](\text{NVCM or IPVCM}) + \text{VCMOC4-0}$$

**Table 140. VCMOC[4:0]**

VCMOC4-0	VCM_OFFSET	VCMOC4-0	VCM_OFFSET
00000	0	10000	0
00001	+1	10001	-1
00010	+2	10010	-2
00011	+3	10011	-3
00100	+4	10100	-4
00101	+5	10101	-5
00110	+6	10110	-6
00111	+7	10111	-7
01000	+8	11000	-8
01001	+9	11001	-9
01010	+10	11010	-10
01011	+11	11011	-11
01100	+12	11100	-12
01101	+13	11101	-13
01110	+14	11110	-14
01111	+15	11111	-15

For example, if VCM[6:0] = 0001011 and VCMOC4-0 = 10001 are selected, then VCM\_OFFSET is "-1," and therefore TOTAL\_VCM is "0001010," which results in VCOMH voltage = 2.6969 from NVCM6-0/IPVCM6-0 table.

Note1. TOTAL\_VCM [6:0] cannot be set to the value above "111111" or below "000000," that is,  $128 \geq \text{VCM}[6:0] + \text{VCMOC4-0} \geq 0$ .

Note2. TOTAL\_VCM[6:0] is  $\text{VCM}[6:0] + \text{VCM\_OFFSET\_MTP}[4:0]$  when MTP\_SEL=0 and is  $\text{VCM}[6:0] + \text{VCMOC4-0}$  when MTP\_SEL=1.

Status	Default Value
Initial	VCMOC[4:0] = 00000



### 5.3.6. RVMLOC : Set VCOML Offset Control (D2h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRVMLOC	R/W	0	1	1	0	1	0	0	1	0	D2h
1 <sup>st</sup> para	R/W	1	0	0	0	VMLO C4	VMLO C3	VMLO C2	VMLO C1	VMLO C0	

#### 5.3.6.1. VMLOC[4:0]

VMLOC4-0 contain VCOM amplitude Offset data. This MTP data and VML register determine VCOML amplitude.

TOTAL\_VML[6:0] = VML[6:0](NVML or IPVML) + VMLOC4-0.

**Table 141. VMLOC[4:0]**

VMLOC4-0	VML_OFFSET	VMLOC4-0	VML_OFFSET
00000	0	10000	0
00001	+1	10001	-1
00010	+2	10010	-2
00011	+3	10011	-3
00100	+4	10100	-4
00101	+5	10101	-5
00110	+6	10110	-6
00111	+7	10111	-7
01000	+8	11000	-8
01001	+9	11001	-9
01010	+10	11010	-10
01011	+11	11011	-11
01100	+12	11100	-12
01101	+13	11101	-13
01110	+14	11110	-14
01111	+15	11111	-15

For example, if VML[6:0] = 0010101 and VMLOC4-0 = 10001 are selected, then VML\_OFFSET is "-1," and therefore TOTAL\_VML is "0010100," which results in VCOM amplitude voltage = 3.4724V from NVML6-0/IPVML6-0 table.

Note1. TOTAL\_VML[6:0] cannot be set to the value above "1111111" or below "0000000," that is,  $127 \geq \text{VML}[6:0] + \text{VMLOC4-0} \geq 0$ .

Note2. TOTAL\_VML[6:0] is VML[6:0] + VML\_OFFSET\_MTP[4:0] when MTP\_SEL=0 and is VML[6:0] + VMLOC4-0 when MTP\_SEL=1

Status	Default Value
Initial	VMLOC[4:0] = 00000



### 5.3.7. WRGVDOC : Set GVDD Offset Control (D3h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRGVDOC	R/W	0	1	1	0	1	0	0	1	1	D3h
1 <sup>st</sup> param		1	0	0	0	GVDO C4	GVDO C3	GVDO C2	GVDO C1	GVDO C0	

#### 5.3.7.1. GVDOC[4:0]

GVDOC4-0 contains GVD Offset data. This MTP data and GVD register determine GVDD level.

TOTAL\_GVD[6:0] = GVD[6:0](NGVD or IPGVD) + GVDOC4-0.

**Table 142. GVDOC[4:0]**

GVDOC4-0	GVD_OFFSET	GVDOC4-0	GVD_OFFSET
00000	0	10000	0
00001	+1	10001	-1
00010	+2	10010	-2
00011	+3	10011	-3
00100	+4	10100	-4
00101	+5	10101	-5
00110	+6	10110	-6
00111	+7	10111	-7
01000	+8	11000	-8
01001	+9	11001	-9
01010	+10	11010	-10
01011	+11	11011	-11
01100	+12	11100	-12
01101	+13	11101	-13
01110	+14	11110	-14
01111	+15	11111	-15

For example, if GVD[6:0] = 0001011 and GVCOC4-0 = 10001 are selected, then MTP\_OFFSET is “-1,” and therefore TOTAL\_GVD is “0001010,” which results in GVDD voltage = 2.6969V from NGVD6-0/IPGVD6-0 table.

Note1. TOTAL\_GVD[6:0] cannot be set to the value above “111111” or below “0000000,” that is,  $127 \geq \text{GVD}[6:0] + \text{GVDOC4-0} \geq 0$ .

Note2. TOTAL\_GVD[6:0] is GVD[6:0] + GVD\_OFFSET\_MTP[4:0] when MTP\_SEL=0 and is GVD[6:0]+ GVDOC4-0 when MTP\_SEL=1.

Status	Default Value
Initial	GVDOC[4:0] = 00000



### 5.3.8. WRID : ID Definition (D4h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRID	R/W	0	1	1	0	1	0	1	0	0	D4h
1 <sup>st</sup> para		1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
2 <sup>nd</sup> para		1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
3 <sup>rd</sup> para		1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

#### 5.3.8.1. ID1/ ID2/ ID3

**ID1:** LCD module/driver manufacturers ID (specified by user)

**ID2:** LCD module/driver version ID(specified by module supplier)

**ID3 :** Project ID(specified by handset company)

Status	Default Value
Intial	ID1 = 00h ID2 = 00h ID3 = 00h

### 5.3.9. RDOFFSETC : Read Offset Control (D5h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDOFFSETC	R	0	1	1	0	1	0	1	0	1	D5h
Dummy Read		1	X	X	X	X	X	X	X	X	X
1 <sup>st</sup> para		1	0	0	0	VCMOC _MTP4	VCMOC _MTP3	VCMOC _MTP2	VCMOC _MTP1	VCMOC _MTP0	
2 <sup>nd</sup> para		1	0	0	0	VMLOC _ MTP 4	VMLOC _ MTP 3	VMLOC _ MTP 2	VMLOC _ MTP 1	VMLOC _ MTP0	
3 <sup>rd</sup> para		1	0	0	0	GVDOC _ MTP 4	GVDOC _ MTP 3	GVDOC _ MTP 2	GVDOC _ MTP 1	GVDOC _ MTP0	

Note: "X" denotes "Don't care"

#### 5.3.9.1. VCMOC\_MTP/ VMLOC\_MTP/ GVDOC\_MTP

**VCMOC\_MTP:** Read VCMOC Values from MTP

**VMLOC\_MTP:** Read VMLOC Values from MTP

**GVDOC\_MTP:** Read GVDOC Values from MTP

Status	Default Value
Initial	MTP[39:24]

### 5.3.10. WRPWD: Level 2 Command Control Test Key (F0h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRPWD	R/W	0	1	1	1	1	0	0	0	0	F0h
1 <sup>st</sup> para		1	TEST W7	TEST W6	TEST W5	TEST W4	TEST W3	TEST W2	TEST W1	TEST W0	
2 <sup>nd</sup> para		1	TEST7	TEST6	TEST5	TEST4	TEST3	TEST2	TEST1	TEST0	

#### 5.3.10.1. TESTW[7:0]/ TEST[7:0]

**TESTW7-0:** Level 2 Command Protection TEST\_KEY in MCU Type I Interface. If interface mode is 80 MCU Type I, this Register should be set to “5Ah” for writing Level 2 registers.

**TEST7-0:** MTP Function Protection TEST\_KEY. When Test Key Command =5Ah, MTP\_WRB and MTP\_ERB are valid.

Status	Default Value
Initial	TESTW[7:0] = 04h TEST[7:0] = 30h

### 5.3.11. RDPWD: Level 2 Read Test Key (F1h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDPWD	R/W	0	1	1	1	1	0	0	0	1	F1h
1 <sup>st</sup> Para		1	TEST R7	TEST R6	TEST R5	TEST R4	TEST R3	TEST R2	TEST R1	TEST R0	

#### 5.3.11.1. TESTR[7:0]

**TESTR:** Level 2 Read Function Protection TEST\_KEY. If interface mode is 80 MCU Type I, This Register should be set to “5Ah” for reading Level 2 registers

Status	Default Value
Initial	TESTR[7:0] = 04h

## 5.3.12. DISCTL: Display Control Register (F2h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISCTL	R/W	0	1	1	1	1	0	0	1	0	F2h
1 <sup>st</sup> para		1	0	0	0	NRTN4	NRTN3	NRTN2	NRTN1	NRTN0	
2 <sup>nd</sup> para		1	0	0	0	IPRTN4	IPRTN3	IPRTN2	IPRTN1	IPRTN0	
3 <sup>rd</sup> para		1	0	0	0	IPINV	IINV	PINV	NINV		
4 <sup>th</sup> para		1	NVBP7	NVBP6	NVBP5	NVBP4	NVBP3	NVBP2	NVBP1	NVBP0	
5 <sup>th</sup> para		1	NVFP7	NVFP6	NVFP5	NVFP4	NVFP3	NVFP2	NVFP1	NVFP0	
6 <sup>th</sup> para		1	IPVBP	IPVBP	IPVBP	IPVBP	IPVBP	IPVBP	IPVBP	IPVBP	
7 <sup>th</sup> para		1	IPVFP7	IPVFP6	IPVFP5	IPVFP4	IPVFP3	IPVFP2	IPVFP1	IPVFP0	
8 <sup>th</sup> para		1	0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	
9 <sup>th</sup> para		1	0	0	0	0	0	SM	GS	REV	
10 <sup>th</sup> para		1	0	0	0	NCRTN 4	NCRTN 3	NCRTN 2	NCRTN 1	NCRTN 0	
11 <sup>th</sup> para		1	0	0	0	IPCRTN 4	IPCRTN 3	IPCRTN 2	IPCRTN 1	IPCRTN 0	

## 5.3.12.1. NRTN[4:0] / IPRTN[4:0]

Set the 1H period (1 raster-row) register. NRTN is valid in Normal mode, and IPRTN is applied in Idle Partial mode.

**Table 143. NRTN[4:0]/IPRTN[4:0]**

NRTN4/IP RTN4	NRTN3/IP RTN3	NRTN2/IP RTN2	NRTN1/IP RTN1	NRTN0/IP RTN0	1 Horizontal clock cycle (CL1)
0	0	0	0	0	Setting Disable
0	0	0	0	1	Setting Disable
0	0	0	1	0	Setting Disable
0	0	0	1	1	Setting Disable
0	0	1	0	0	Setting Disable
0	0	1	0	1	Setting Disable
0	0	1	1	0	Setting Disable
0	0	1	1	1	Setting Disable
0	1	0	0	0	8 INCLK
0	1	0	0	1	9 INCLK
0	1	0	1	0	10 INCLK
0	1	0	1	1	11 INCLK
0	1	1	0	0	12 INCLK
0	1	1	0	1	13 INCLK
0	1	1	1	0	14 INCLK
0	1	1	1	1	15 INCLK
1	0	0	0	0	16 INCLK
1	0	0	0	1	17 INCLK
1	0	0	1	0	18 INCLK
1	0	0	1	1	19 INCLK
1	0	1	0	0	20 INCLK
1	0	1	0	1	21 INCLK
1	0	1	1	0	22 INCLK
1	0	1	1	1	23 INCLK
1	1	0	0	0	24 INCLK
1	1	0	0	1	25 INCLK
1	1	0	1	0	26 INCLK
1	1	0	1	1	27 INCLK
1	1	1	0	0	28 INCLK
1	1	1	0	1	29 INCLK
1	1	1	1	0	30 INCLK
1	1	1	1	1	31 INCLK

Note1. RTN x CRTN must be bigger than 260 in MPU-IF.

- 24/ 18/ 16-bit RGB-IF : DOTCLK >= 260
- 9/ 8-bit RGB-IF : DOTCLK >= 260 x 3

Note2. INCLK : Internal clock (= OSC\_CK x CRTN)

Note3. IPNO, IPSDT, VCIRA, VCIR register values must be smaller than the half of IPRTN values.

NNO, NSDT, VCIRA, VCIR register values must be smaller than the half of NRTN values.

Status	Default Value
Initial	NRTN[4:0] = 10110 IPRTN[4:0] = 10110



## 5.3.12.2. IPINV/IINV/PINV/INV

Display inversion mode control register.

**IPINV** : Inversion setting on partial idle mode (Partial mode on / Idle mode on)

**IINV** : Inversion setting on Idle mode (Idle mode on)

**PINV** : Inversion setting on partial mode (Partial mode on)

**NINV** : Inversion setting on full color normal mode (Normal mode on)

**Table 144. IPINV/IINV/PINV/NINV**

IPINV/IINV/PINV/NINV	Inversion
0	Frame inversion
1	Line inversion

Status	Default Value
Initial	IPINV = 0 IINV = 0 PINV = 1 NINV = 1

## 5.3.12.3. NVBP[7:0]/IPVBP[7:0]/NVFP[7:0]/IPVFP[7:0]

Control vertical back and front porch in MCU I/F or RGB I/F mode

**NVBP/ IPVBP** : The number of lines for the back porch of VS(Vertical Sync) register.

IPVBP is applied in Idle Partial mode

**Table 145. NVBP[7:0]/IPVBP[7:0]**

NVBP[7:0] / IPVBP[7:0]	No. of clock cycle of HS (horizontal Sync)
00d	Setting Disable
01d	Setting Disable
02d	2
03d	3
04d	4
05d	5
.	.
.	.
254d	254
255d	255

Note 1. When BCTRL does ON, establish VBP and VFP by same value.

**NVFP/ IPVFP**: The number of lines for the front porch of VS. NVFP/IPVFP must be bigger than 2.

IPVFP is applied in Idle Partial mode.

**Table 146. NVFP[7:0]/IPVFP[7:0]**

NVFP[7:0] / IPVFP[7:0]	No. of clock cycle of HS
00d	Setting Disable
01d	Setting Disable
02d	Setting Disable
03d	3
04d	4
05d	5
.	.
.	.
254d	254
255d	255

Status	Default Value
Initial	NVBP[7:0] = 08h IPVBP[7:0] = 08h NVFP[7:0] = 08h IPVFP[7:0] = 08h



## 5.3.12.4. HBP[6:0]

The number of internal clocks for TE's Horizontal timing high width

**Table 147. HBP[6:0]**

HBP[6:0]	No. of clock cycle of INCLK
00d	2
01d	3
02d	4
03d	5
.	.
126d	128
127d	129

Status	Default Value
Initial	HBP[6:0] = 01_0000

## 5.3.12.5. SM/ GS/ REV

**SM** : Select the division drive method of the gate driver. When SM=0, even/odd division is selected; SM =1, upper/lower division drive is selected by (total gate line)/2 and (total gate line)/2. Various connections between TFT panel and the IC can be supported with the combination of SM and GS bit.

**GS** : Set the order of Gate Clock generation. When GS = 0, the order of GATE\_ON is from G1 to G320, and then GS = 1, from G320 to G1.

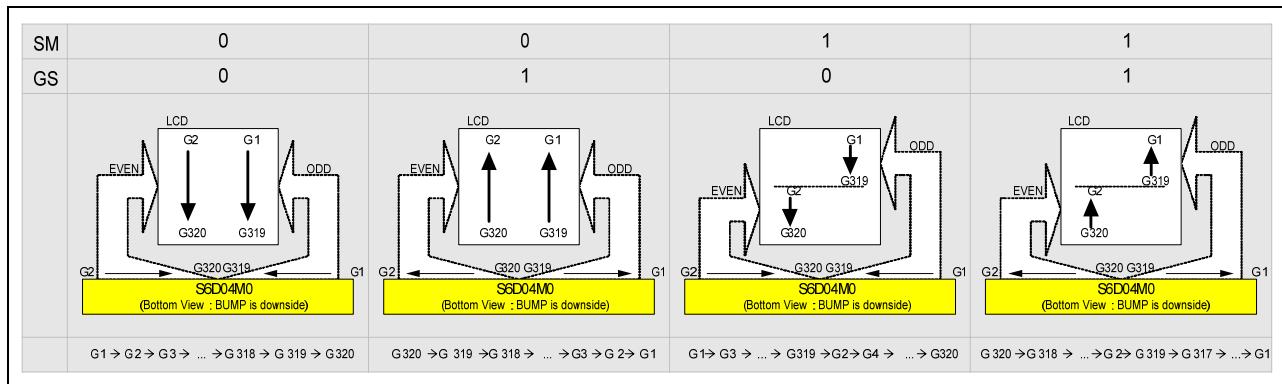


Figure 148. Gate clock generation order selection using GS and SM

**REV**: Display all character and graphics display sections with reversal when REV=1.

Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels.

Table 148.REV

REV	GRAM Data	Display Area	
		Positive	Negative
0	8'b000000	V255	V0
	⋮	⋮	⋮
1	8'b111111	V0	V255
	⋮	⋮	⋮
	8'b000000	V0	V255
	⋮	⋮	⋮
	8'b111111	V255	V0

Status	Default Value
Initial	SM = 0 GS = 0 REV = 0

## 5.3.12.6. NCRTN[4:0] / IPCRTN[4:0]

Set the 1 raster-row. IPCRTN is applied in Idle Partial mode.

Table 149. NCRTN[4:0] / IPCRTN[4:0]

NCRTN4/ IPCRTN4	NCRTN3/ IPCRTN3	NCRTN2/ IPCRTN2	NCRTN1/ IPCRTN1	NCRTN0/ IPCRTN0	INCLK
0	0	0	0	0	Setting Disable
0	0	0	0	1	Setting Disable
0	0	0	1	0	Setting Disable
0	0	0	1	1	Setting Disable
0	0	1	0	0	Setting Disable
0	0	1	0	1	Setting Disable
0	0	1	1	0	Setting Disable
0	0	1	1	1	Setting Disable
0	1	0	0	0	8 OSC_CLK
0	1	0	0	1	9 OSC_CLK
0	1	0	1	0	10 OSC_CLK
0	1	0	1	1	11 OSC_CLK
0	1	1	0	0	12 OSC_CLK
0	1	1	0	1	13 OSC_CLK
0	1	1	1	0	14 OSC_CLK
0	1	1	1	1	15 OSC_CLK
1	0	0	0	0	16 OSC_CLK
1	0	0	0	1	17 OSC_CLK
1	0	0	1	0	18 OSC_CLK
1	0	0	1	1	19 OSC_CLK
1	0	1	0	0	20 OSC_CLK
1	0	1	0	1	21 OSC_CLK
1	0	1	1	0	22 OSC_CLK
1	0	1	1	1	23 OSC_CLK
1	1	0	0	0	24 OSC_CLK
1	1	0	0	1	25 OSC_CLK
1	1	0	1	0	26 OSC_CLK
1	1	0	1	1	27 OSC_CLK
1	1	1	0	0	28 OSC_CLK
1	1	1	0	1	29 OSC_CLK
1	1	1	1	0	30 OSC_CLK
1	1	1	1	1	31 OSC_CLK

Note. RTN x CRTN must be bigger than 260.

Status	Default Value
Initial	NCRTN[4:0] = 10110 IPCRTN[4:0] = 10110

### 5.3.13. PWRCTL: Power Control Register (F3h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWRCTL	R/W	0	1	1	1	1	0	0	1	1	F3h
1 <sup>st</sup> para		1	AP ON	GON	AON	PON3	PON2	PON1	PON	VCI1_EN	
2 <sup>nd</sup> para		1	0	0	NDC31	NDC30	NDC21	NDC20	NDC11	NDC10	
3 <sup>rd</sup> para		1	0	0	IPDC31	IPDC30	IPDC21	IPDC20	IPDC11	IPDC10	
4 <sup>th</sup> para		1	0	0	0	0	VC3	VC2	VC1	VC0	
5 <sup>th</sup> para		1	0	IPBT2	IPBT1	IPBT0	0	NBT2	NBT1	NBT0	
6 <sup>th</sup> para		1	0	GVD6	GVD5	GVD4	GVD3	GVD2	GVD1	GVD0	
7 <sup>th</sup> para		1	0	IPGVD6	IPGVD5	IPGVD4	IPGVD3	IPGVD2	IPGVD1	IPGVD0	
8 <sup>th</sup> para		1	0	0	VGH_FL AG_EN	AB_VCI 1	NAB2A_ G	IPAB2A_ G	NAB2A	IPAB2A	

#### 5.3.13.1. APON

**APON:** This is an automatic-boosting-operation-starting bit for the booster circuits. In case of APON=0, the automatic boosting sequence starter is halted and the booster circuits are operated independently by PON, PON1, PON2 and PON3 bits. In case of APON=1, booster circuits are operated automatically and sequentially. For further information about timing, please refer to the Section 4.1.6, 4.1.7

Status	Default Value
Initial	APON = 1

## 5.3.13.2. GON/AON/PON3/PON2/PON1/PON/VCI1\_EN

**GON:** Gate on/off control bit. All gate outputs are set to be VSS level when GON = 0.

When GON = 1, gate driver is working: G1 to G320 output is either VGH or VGL level.

See the Instruction set-up flow for further description on the display on/off flow.

**Table 150. GON**

GON	Gate Output	
0	PON2=0	All gates goes to VSS
	PON2=1	All gates goes to VGL
1	Gate on(VGH / VGL)	

**AON:** This is an operation-starting bit for GVDD/VCOMH/VCOML amplifiers. In case of AON = 0, the amplifier circuits are stopped. On the other hand, the operation of the amplifiers is getting started when AON = 1. For further information about timing for adjusting to AON= 1, refer to the Section 4.1.6, 4.1.7

**PON3:** This is an operation-starting bit for the booster circuit 3(VCL). In case of PON3 = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON3= 1, please refer to the Section 4.1.6, 4.1.7

**PON2:** This is an operation-starting bit for the booster circuit 2(VGL). In case of PON2 = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON2= 1, please refer to the Section 4.1.6, 4.1.7

**PON1:** This is an operation-starting bit for the booster circuit 2(VGH). In case of PON1 = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON1= 1, please refer to the Section 4.1.6, 4.1..7

**PON:** This is an operation-starting bit for the booster circuit1. In case of PON = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON = 1, please refer to the Section 4.1.6, 4.1.7

**VCI1\_EN:** Internal VCI1 generation amplifier operation control bit. When VCI1\_EN=0, VCI1 voltage is not generated.

Status	Default Value
Initial	GON = 0 AON = 0 PON3 = 0 PON2 =0 PON1 = 0 PON = 0 VCI1_EN = 0

## 5.3.13.3. NDC3/IPDC3/NDC2/IPDC2/NDC1/IPDC1

**NDC31-30/ IPDC31-30:** The operating frequency in the booster circuit 3 is selected.

IPDC3 is applied in Idle Partial mode.

**Table 151.NDC3[1:0]/ IPDC3[1:0]**

NDC31 IPDC31	NDC30 IPDC30	Internal Operation (synchronized with internal clock)
		f(CL1) : f(DCCLK3)
0	0	1:4
0	1	1:2
1	0	1:1
1	1	Setting disabled

Note. DCCLK3 is pumping clock for booster circuit3

**NDC21-20/ IPDC21-20:** The operating frequency in the booster circuit 2 is selected.

IPDC2 is applied in Idle Partial mode.

**Table 152.NDC2[1:0]/ IPDC2[1:0]**

NDC21 IPDC21	NDC20 IPDC20	Internal Operation (synchronized with internal clock)
		f(CL1) : f(DCCLK2)
0	0	1:2
0	1	1:1
1	0	1:0.5
1	1	1:0.25

Note. DCCLK2 is pumping clock for booster circuit2

**NDC11-10/IPDC11-10:** The operating frequency in the booster circuit1 is selected. When the boosting operating frequency is high, the driving ability of the booster circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

IPDC1 is applied in Idle Partial mode.

**Table 153.NDC1[1:0]/ IPDC1[1:0]**

<b>NDC11 IPDC11</b>	<b>NDC10 IPDC11</b>	<b>Internal Operation (synchronized with internal clock)</b>
		<b>f(CL1) : f(DCCLK1)</b>
0	0	1:4
0	1	1:2
1	0	1:1
1	1	Setting disabled

Note. DCCLK1 is pumping clock for booster circuit1. f(1H) is horizontal frequency (1 raster-row)

<b>Status</b>	<b>Default Value</b>
Initial	NDC3[1 :0] = 00, NDC2[1 :0] = 00, NDC1[1 :0] = 00 IPDC3[1 :0] = 00, IPDC2[1 :0] = 00, IPDC1[1 :0] = 00

## 5.3.13.4. V3[3:0]

**VC3-0** : Set the VCI1 voltage. These bits set the VCI1 voltage up to 3V as the nominal output (upper limit value may depend on VCI voltage)

**Table 154. VC[3:0]**

VC3	VC2	VC1	VC0	VCI1
0	0	0	0	1.35
0	0	0	1	1.75
0	0	1	0	2.07
0	0	1	1	2.16
0	1	0	0	2.25
0	1	0	1	2.34
0	1	1	0	2.43
0	1	1	1	2.52
1	0	0	0	2.58
1	0	0	1	2.64
1	0	1	0	2.70
1	0	1	1	2.76
1	1	0	0	2.82
1	1	0	1	2.88
1	1	1	0	2.94
1	1	1	1	3

Note. Do not set any higher VCI1 level than VCI -0.15V.

Status	Default Value
Initial	VC[3:0] = 0001

## 5.3.13.5. NBT[2:0]/ IPBT[2:0]

**NBT/ IPBT** : The output factor of booster is switched. Adjust scale factor of the booster circuit by the voltage used. When the boosting operating frequency is high, the driving ability of the booster circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption. IPBT is applied in Idle Partial mode.

**Table 155. NBT[2:0]/IPBT[2:0]**

IPBT1/NBT2	IPBT1/NBT1	IPBP0/NBT0	VGH	VGL	Notes*	
0	0	0	5 X VCI1	-3X VCI1	13.75V	-8.25V
0	0	1	5 X VCI1	-4X VCI1	13.75V	-11V
0	1	0	6 X VCI1	-3X VCI1	16.5V	-8.25V
0	1	1	6 X VCI1	-4X VCI1	16.5V	-11V
1	0	0	6 X VCI1	-5X VCI1	16.5V	-13.75V
1	0	1	7 X VCI1	-4X VCI1	19.25V	-11V
1	1	0		Setting disabled		
1	1	1		Setting disabled		

Note.

The values in table above are example of nominal upper-limit by register setting when VCI1=2.75V.

Do not set any higher VGH level than 16.5V. **Do not set | VGH – VGL | voltage difference over 30.0V.**

Status	Default Value
Initial	NBT[2:0] = 010, IPBT[2:0] = 010

## 5.3.13.6. NGVD[6:0]/IPGVD[6:0]

**NGVD6-0:** Set the amplifying factor of the GVDD voltage on Normal Mode (the voltage for the Gamma voltage). It allows ranging from 2.5V to 5.0V.

**Table 156. NGVD[6:0]**

NGVD6-0	GVDD Voltage						
0000000	2.5000	0100000	3.1299	1000000	3.7598	1100000	4.3898
0000001	2.5197	0100001	3.1496	1000001	3.7795	1100001	4.4094
0000010	2.5394	0100010	3.1693	1000010	3.7992	1100010	4.4291
0000011	2.5591	0100011	3.1890	1000011	3.8189	1100011	4.4488
0000100	2.5787	0100100	3.2087	1000100	3.8386	1100100	4.4685
0000101	2.5984	0100101	3.2283	1000101	3.8583	1100101	4.4882
0000110	2.6181	0100110	3.2480	1000110	3.8780	1100110	4.5079
0000111	2.6378	0100111	3.2677	1000111	3.8976	1100111	4.5276
0001000	2.6575	0101000	3.2874	1001000	3.9173	1101000	4.5472
0001001	2.6772	0101001	3.3071	1001001	3.9370	1101001	4.5669
0001010	2.6969	0101010	3.3268	1001010	3.9567	1101010	4.5866
0001011	2.7165	0101011	3.3465	1001011	3.9764	1101011	4.6063
0001100	2.7362	0101100	3.3661	1001100	3.9961	1101100	4.6260
0001101	2.7559	0101101	3.3858	1001101	4.0157	1101101	4.6457
0001110	2.7756	0101110	3.4055	1001110	4.0354	1101110	4.6654
0001111	2.7953	0101111	3.4252	1001111	4.0551	1101111	4.6850
0010000	2.8150	0110000	3.4449	1010000	4.0748	1110000	4.7047
0010001	2.8346	0110001	3.4646	1010001	4.0945	1110001	4.7244
0010010	2.8543	0110010	3.4843	1010010	4.1142	1110010	4.7441
0010011	2.8740	0110011	3.5039	1010011	4.1339	1110011	4.7638
0010100	2.8937	0110100	3.5236	1010100	4.1535	1110100	4.7835
0010101	2.9134	0110101	3.5433	1010101	4.1732	1110101	4.8031
0010110	2.9331	0110110	3.5630	1010110	4.1929	1110110	4.8228
0010111	2.9528	0110111	3.5827	1010111	4.2126	1110111	4.8425
0011000	2.9724	0111000	3.6024	1011000	4.2323	1111000	4.8622
0011001	2.9921	0111001	3.6220	1011001	4.2520	1111001	4.8819
0011010	3.0118	0111010	3.6417	1011010	4.2717	1111010	4.9016
0011011	3.0315	0111011	3.6614	1011011	4.2913	1111011	4.9213
0011100	3.0512	0111100	3.6811	1011100	4.3110	1111100	4.9409
0011101	3.0709	0111101	3.7008	1011101	4.3307	1111101	4.9606
0011110	3.0906	0111110	3.7205	1011110	4.3504	1111110	4.9803
0011111	3.1102	0111111	3.7402	1011111	4.3701	1111111	5.0000

Note. Do not set any higher GVDD level than AVDD-0.3V



**IPGVD6-0:** Set the amplifying factor of the GVDD voltage on partial idle mode.

**Table 157. IPGVD[6:0]**

IPGVD6-0	GVDD Voltage						
0000000	2.5000	0100000	3.1299	1000000	3.7598	1100000	4.3898
0000001	2.5197	0100001	3.1496	1000001	3.7795	1100001	4.4094
0000010	2.5394	0100010	3.1693	1000010	3.7992	1100010	4.4291
0000011	2.5591	0100011	3.1890	1000011	3.8189	1100011	4.4488
0000100	2.5787	0100100	3.2087	1000100	3.8386	1100100	4.4685
0000101	2.5984	0100101	3.2283	1000101	3.8583	1100101	4.4882
0000110	2.6181	0100110	3.2480	1000110	3.8780	1100110	4.5079
0000111	2.6378	0100111	3.2677	1000111	3.8976	1100111	4.5276
0001000	2.6575	0101000	3.2874	1001000	3.9173	1101000	4.5472
0001001	2.6772	0101001	3.3071	1001001	3.9370	1101001	4.5669
0001010	2.6969	0101010	3.3268	1001010	3.9567	1101010	4.5866
0001011	2.7165	0101011	3.3465	1001011	3.9764	1101011	4.6063
0001100	2.7362	0101100	3.3661	1001100	3.9961	1101100	4.6260
0001101	2.7559	0101101	3.3858	1001101	4.0157	1101101	4.6457
0001110	2.7756	0101110	3.4055	1001110	4.0354	1101110	4.6654
0001111	2.7953	0101111	3.4252	1001111	4.0551	1101111	4.6850
0010000	2.8150	0110000	3.4449	1010000	4.0748	1110000	4.7047
0010001	2.8346	0110001	3.4646	1010001	4.0945	1110001	4.7244
0010010	2.8543	0110010	3.4843	1010010	4.1142	1110010	4.7441
0010011	2.8740	0110011	3.5039	1010011	4.1339	1110011	4.7638
0010100	2.8937	0110100	3.5236	1010100	4.1535	1110100	4.7835
0010101	2.9134	0110101	3.5433	1010101	4.1732	1110101	4.8031
0010110	2.9331	0110110	3.5630	1010110	4.1929	1110110	4.8228
0010111	2.9528	0110111	3.5827	1010111	4.2126	1110111	4.8425
0011000	2.9724	0111000	3.6024	1011000	4.2323	1111000	4.8622
0011001	2.9921	0111001	3.6220	1011001	4.2520	1111001	4.8819
0011010	3.0118	0111010	3.6417	1011010	4.2717	1111010	4.9016
0011011	3.0315	0111011	3.6614	1011011	4.2913	1111011	4.9213
0011100	3.0512	0111100	3.6811	1011100	4.3110	1111100	4.9409
0011101	3.0709	0111101	3.7008	1011101	4.3307	1111101	4.9606
0011110	3.0906	0111110	3.7205	1011110	4.3504	1111110	4.9803
0011111	3.1102	0111111	3.7402	1011111	4.3701	1111111	5.0000

Status	Default Value
Initial	GVD[6:0] = 00_0000 IPGVD[6:0] = 00_0000



## 5.3.13.7. VGH\_FLAG\_EN/ AB\_VCL1

**VGH\_FLAG\_EN** : VGH-level-detecting-function enables register.

**AB\_VCI1**: Set VCI1 output equal to VCI. VCI1 output is internally connected to VCI via switching circuit when AB\_VCI="H."

Status	Default Value
Initial	VGH_FLAG_EN = 1 AB_VCI1 = 0

## 5.3.13.8. NAB2A\_G/ IPAB2A\_G/ NAB2A/ IPAB2A

**NAB2A\_G/ IPAB2A\_G** : GVDD amplifier output stage selection register.

IPAB2A\_G is applied in Idle Partial mode.

NAB2A_G/IPAB2A_G	Description
0	The output stage of GVDD amplifier operates as a Class-AB type
1	The output stage of GVDD amplifier operates as a Class-A type

**NAB2A/ IPAB2A** : VCOMH amplifier output stage selection register.

IPAB2A is applied in Idle Partial mode.

NAB2A/ IPAB2A	Description
0	The output stage of VCOMH amplifier operates as a Class-AB type
1	The output stage of VCOMH amplifier operates as a Class-A type

Status	Default Value
Initial	NAB2A_G = 1, IPAB2A_G = 1 NAB2A = 0, IPAB2A = 0

## 5.3.14. VCMCTL : VCOM Control Register (F4h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VCMCTL	R/W	0	1	1	1	1	0	1	0	0	F4h
1 <sup>st</sup> para		1	0	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	
2 <sup>nd</sup> para		1		IPVCM6	IPVCM5	IPVCM4	IPVCM3	IPVCM2	IPVCM1	IPVCM0	
3 <sup>rd</sup> para		1	VCOMG	VML6	VML5	VML4	VML3	VML2	VML1	VML0	
4 <sup>th</sup> para		1	0	IPVML6	IPVML5	IPVML4	IPVML3	IPVML2	IPVML1	IPVML0	



5 <sup>th</sup> para	1	0	VCIRA2	VCIRA1	VCIRAO	0	VCIR2	VCIR1	VCIR0	
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## 5.3.14.1. VCM[6:0]/ IPVCM[6:0]

**VCM6-0:** Set the upper level of VCOM on Normal Mode (VCOMH).

Table 158. VCM[6:0] (Vref=2.0V, unit =V)

VCM[6:0]	VCOMH Voltage	VCM[6:0]	VCOMH Voltage	VCM[6:0]	VCOMH Voltage	VCM[6:0]	VCOMH Voltage
0000000	2.5000	0100000	3.1299	1000000	3.7598	1100000	4.3898
0000001	2.5197	0100001	3.1496	1000001	3.7795	1100001	4.4094
0000010	2.5394	0100010	3.1693	1000010	3.7992	1100010	4.4291
0000011	2.5591	0100011	3.1890	1000011	3.8189	1100011	4.4488
0000100	2.5787	0100100	3.2087	1000100	3.8386	1100100	4.4685
0000101	2.5984	0100101	3.2283	1000101	3.8583	1100101	4.4882
0000110	2.6181	0100110	3.2480	1000110	3.8780	1100110	4.5079
0000111	2.6378	0100111	3.2677	1000111	3.8976	1100111	4.5276
0001000	2.6575	0101000	3.2874	1001000	3.9173	1101000	4.5472
0001001	2.6772	0101001	3.3071	1001001	3.9370	1101001	4.5669
0001010	2.6969	0101010	3.3268	1001010	3.9567	1101010	4.5866
0001011	2.7165	0101011	3.3465	1001011	3.9764	1101011	4.6063
0001100	2.7362	0101100	3.3661	1001100	3.9961	1101100	4.6260
0001101	2.7559	0101101	3.3858	1001101	4.0157	1101101	4.6457
0001110	2.7756	0101110	3.4055	1001110	4.0354	1101110	4.6654
0001111	2.7953	0101111	3.4252	1001111	4.0551	1101111	4.6850
0010000	2.8150	0110000	3.4449	1010000	4.0748	1110000	4.7047
0010001	2.8346	0110001	3.4646	1010001	4.0945	1110001	4.7244
0010010	2.8543	0110010	3.4843	1010010	4.1142	1110010	4.7441
0010011	2.8740	0110011	3.5039	1010011	4.1339	1110011	4.7638
0010100	2.8937	0110100	3.5236	1010100	4.1535	1110100	4.7835
0010101	2.9134	0110101	3.5433	1010101	4.1732	1110101	4.8031
0010110	2.9331	0110110	3.5630	1010110	4.1929	1110110	4.8228
0010111	2.9528	0110111	3.5827	1010111	4.2126	1110111	4.8425
0011000	2.9724	0111000	3.6024	1011000	4.2323	1111000	4.8622
0011001	2.9921	0111001	3.6220	1011001	4.2520	1111001	4.8819
0011010	3.0118	0111010	3.6417	1011010	4.2717	1111010	4.9016
0011011	3.0315	0111011	3.6614	1011011	4.2913	1111011	4.9213
0011100	3.0512	0111100	3.6811	1011100	4.3110	1111100	4.9409
0011101	3.0709	0111101	3.7008	1011101	4.3307	1111101	4.9606
0011110	3.0906	0111110	3.7205	1011110	4.3504	1111110	4.9803
0011111	3.1102	0111111	3.7402	1011111	4.3701	1111111	5.0000

Note. Don't set any higher VCOMH level than AVDD-0.3V



**IPVCM6-0:** Set the upper level of VCOM (VCOMH) on partial idle mode.

Table 159. IPVCM[6:0] (Vref=2.0V, unit =V)

IPVCM[6:0]	VCOMH Voltage	IPVCM[6:0]	VCOMH Voltage	IPVCM[6:0]	VCOMH Voltage	IPVCM[6:0]	VCOMH Voltage
0000000	2.5000	0100000	3.1299	1000000	3.7598	1100000	4.3898
0000001	2.5197	0100001	3.1496	1000001	3.7795	1100001	4.4094
0000010	2.5394	0100010	3.1693	1000010	3.7992	1100010	4.4291
0000011	2.5591	0100011	3.1890	1000011	3.8189	1100011	4.4488
0000100	2.5787	0100100	3.2087	1000100	3.8386	1100100	4.4685
0000101	2.5984	0100101	3.2283	1000101	3.8583	1100101	4.4882
0000110	2.6181	0100110	3.2480	1000110	3.8780	1100110	4.5079
0000111	2.6378	0100111	3.2677	1000111	3.8976	1100111	4.5276
0001000	2.6575	0101000	3.2874	1001000	3.9173	1101000	4.5472
0001001	2.6772	0101001	3.3071	1001001	3.9370	1101001	4.5669
0001010	2.6969	0101010	3.3268	1001010	3.9567	1101010	4.5866
0001011	2.7165	0101011	3.3465	1001011	3.9764	1101011	4.6063
0001100	2.7362	0101100	3.3661	1001100	3.9961	1101100	4.6260
0001101	2.7559	0101101	3.3858	1001101	4.0157	1101101	4.6457
0001110	2.7756	0101110	3.4055	1001110	4.0354	1101110	4.6654
0001111	2.7953	0101111	3.4252	1001111	4.0551	1101111	4.6850
0010000	2.8150	0110000	3.4449	1010000	4.0748	1110000	4.7047
0010001	2.8346	0110001	3.4646	1010001	4.0945	1110001	4.7244
0010010	2.8543	0110010	3.4843	1010010	4.1142	1110010	4.7441
0010011	2.8740	0110011	3.5039	1010011	4.1339	1110011	4.7638
0010100	2.8937	0110100	3.5236	1010100	4.1535	1110100	4.7835
0010101	2.9134	0110101	3.5433	1010101	4.1732	1110101	4.8031
0010110	2.9331	0110110	3.5630	1010110	4.1929	1110110	4.8228
0010111	2.9528	0110111	3.5827	1010111	4.2126	1110111	4.8425
0011000	2.9724	0111000	3.6024	1011000	4.2323	1111000	4.8622
0011001	2.9921	0111001	3.6220	1011001	4.2520	1111001	4.8819
0011010	3.0118	0111010	3.6417	1011010	4.2717	1111010	4.9016
0011011	3.0315	0111011	3.6614	1011011	4.2913	1111011	4.9213
0011100	3.0512	0111100	3.6811	1011100	4.3110	1111100	4.9409
0011101	3.0709	0111101	3.7008	1011101	4.3307	1111101	4.9606
0011110	3.0906	0111110	3.7205	1011110	4.3504	1111110	4.9803
0011111	3.1102	0111111	3.7402	1011111	4.3701	1111111	5.0000

Note. Don't set any higher VCOMH level than AVDD-0.3V

Status	Default Value
Initial	VCM[6:0] = 00_0000 IPVCM [6:0]= 00_0000



## 5.3.14.2. VCOMG/ VML[6:0]/ IPVML[6:0]

**VCOMG:** When VCOMG = 1, low level of VCOM signal is to be fixed at AVSS. Therefore, the amplitude of VCOM signal is determined as  $|VCOMH - AVSS|$  regardless of VML setting. In this case, VCOML pad should be connected to GND, because VCOML amp is off and VCOML output is floated. When VCOMG=0, the amplitude of VCOM signal is determined as  $|VCOMH - VCOML|$

**VML6-0 :** Set the Amplitude of the VCOM voltage on Normal Mode. VCOML is adjusted automatically by setting the Amplitude of VCOM voltage.

**Table 160. VML[6:0] (Vref=2.0V, unit =V)**

VML[6:0]	Amplitude Voltage						
0000000	3.0000	0100000	3.7559	1000000	4.5118	1100000	5.2677
0000001	3.0236	0100001	3.7795	1000001	4.5354	1100001	5.2913
0000010	3.0472	0100010	3.8031	1000010	4.5591	1100010	5.3150
0000011	3.0709	0100011	3.8268	1000011	4.5827	1100011	5.3386
0000100	3.0945	0100100	3.8504	1000100	4.6063	1100100	5.3622
0000101	3.1181	0100101	3.8740	1000101	4.6299	1100101	5.3858
0000110	3.1417	0100110	3.8976	1000110	4.6535	1100110	5.4094
0000111	3.1654	0100111	3.9213	1000111	4.6772	1100111	5.4331
0001000	3.1890	0101000	3.9449	1001000	4.7008	1101000	5.4567
0001001	3.2126	0101001	3.9685	1001001	4.7244	1101001	5.4803
0001010	3.2362	0101010	3.9921	1001010	4.7480	1101010	5.5039
0001011	3.2598	0101011	4.0157	1001011	4.7717	1101011	5.5276
0001100	3.2835	0101100	4.0394	1001100	4.7953	1101100	5.5512
0001101	3.3071	0101101	4.0630	1001101	4.8189	1101101	5.5748
0001110	3.3307	0101110	4.0866	1001110	4.8425	1101110	5.5984
0001111	3.3543	0101111	4.1102	1001111	4.8661	1101111	5.6220
0010000	3.3780	0110000	4.1339	1010000	4.8898	1110000	5.6457
0010001	3.4016	0110001	4.1575	1010001	4.9134	1110001	5.6693
0010010	3.4252	0110010	4.1811	1010010	4.9370	1110010	5.6929
0010011	3.4488	0110011	4.2047	1010011	4.9606	1110011	5.7165
0010100	3.4724	0110100	4.2283	1010100	4.9843	1110100	5.7402
0010101	3.4961	0110101	4.2520	1010101	5.0079	1110101	5.7638
0010110	3.5197	0110110	4.2756	1010110	5.0315	1110110	5.7874
0010111	3.5433	0110111	4.2992	1010111	5.0551	1110111	5.8110
0011000	3.5669	0111000	4.3228	1011000	5.0787	1111000	5.8346
0011001	3.5906	0111001	4.3465	1011001	5.1024	1111001	5.8583
0011010	3.6142	0111010	4.3701	1011010	5.1260	1111010	5.8819
0011011	3.6378	0111011	4.3937	1011011	5.1496	1111011	5.9055
0011100	3.6614	0111100	4.4173	1011100	5.1732	1111100	5.9291
0011101	3.6850	0111101	4.4409	1011101	5.1969	1111101	5.9528
0011110	3.7087	0111110	4.4646	1011110	5.2205	1111110	5.9764
0011111	3.7323	0111111	4.4882	1011111	5.2441	1111111	6.0000

Note. Available setting range of VCOML is from VCL+0.5V to 0V. The Amplitude of VCOM cannot exceed 6V.



**IPVML6-0** : Set the Amplitude of the VCOM voltage on partial idle mode.

**Table 161. IPVML[6:0] (Vref=2.0V, unit =V)**

IPVMLINUX[6:0]	Amplitude Voltage						
00000000	3.0000	01000000	3.7559	10000000	4.5118	11000000	5.2677
00000001	3.0236	01000001	3.7795	10000001	4.5354	11000001	5.2913
00000010	3.0472	01000010	3.8031	10000010	4.5591	11000010	5.3150
00000011	3.0709	01000011	3.8268	10000011	4.5827	11000011	5.3386
00000100	3.0945	01000100	3.8504	10000100	4.6063	11000100	5.3622
00000101	3.1181	01000101	3.8740	10000101	4.6299	11000101	5.3858
00000110	3.1417	01000110	3.8976	10000110	4.6535	11000110	5.4094
00000111	3.1654	01000111	3.9213	10000111	4.6772	11000111	5.4331
00010000	3.1890	01010000	3.9449	10010000	4.7008	11010000	5.4567
00010001	3.2126	01010001	3.9685	10010001	4.7244	11010001	5.4803
00010010	3.2362	01010010	3.9921	10010010	4.7480	11010010	5.5039
00010011	3.2598	01010011	4.0157	10010011	4.7717	11010011	5.5276
00011000	3.2835	01011000	4.0394	10011000	4.7953	11011000	5.5512
00011001	3.3071	01011001	4.0630	10011001	4.8189	11011001	5.5748
00011010	3.3307	01011010	4.0866	10011010	4.8425	11011010	5.5984
00011011	3.3543	01011011	4.1102	10011011	4.8661	11011011	5.6220
00100000	3.3780	01100000	4.1339	10100000	4.8898	11100000	5.6457
00100001	3.4016	01100001	4.1575	10100001	4.9134	11100001	5.6693
00100010	3.4252	01100010	4.1811	10100010	4.9370	11100010	5.6929
00100011	3.4488	01100011	4.2047	10100011	4.9606	11100011	5.7165
00101000	3.4724	01101000	4.2283	10101000	4.9843	11101000	5.7402
00101001	3.4961	01101001	4.2520	10101001	5.0079	11101001	5.7638
00101010	3.5197	01101010	4.2756	10101010	5.0315	11101010	5.7874
00101011	3.5433	01101011	4.2992	10101011	5.0551	11101011	5.8110
00110000	3.5669	01110000	4.3228	10110000	5.0787	11110000	5.8346
00110001	3.5906	01110001	4.3465	10110001	5.1024	11110001	5.8583
00110010	3.6142	01110010	4.3701	10110010	5.1260	11110010	5.8819
00110011	3.6378	01110011	4.3937	10110011	5.1496	11110011	5.9055
00111000	3.6614	01111000	4.4173	10111000	5.1732	11111000	5.9291
00111001	3.6850	01111001	4.4409	10111001	5.1969	11111001	5.9528
00111010	3.7087	01111010	4.4646	10111010	5.2205	11111010	5.9764
00111011	3.7323	01111011	4.4882	10111011	5.2441	11111011	6.0000

Note. Available setting range of VCOML is from VCL+0.5V to 0V. The Amplitude of VCOM cannot exceed 6V.

Status	Default Value
Initial	VCOMG = 0 VML[6:0] = 00_0000 IPVML[6:0] = 00_0000



## 5.3.14.3. VCIRA[2:0]/ VCIR[2:0]

**VCIRA2-0** : VCI recycling period of Source is sustained for the number of clock cycle which is set on VCIRA2-0.

**VCIR2-0** : VCI recycling period of VCOM is sustained for the number of clock cycle which is set on VCIR2-0.

**Table 162. VCIRA[2:0]/ VCIR[2:0]**

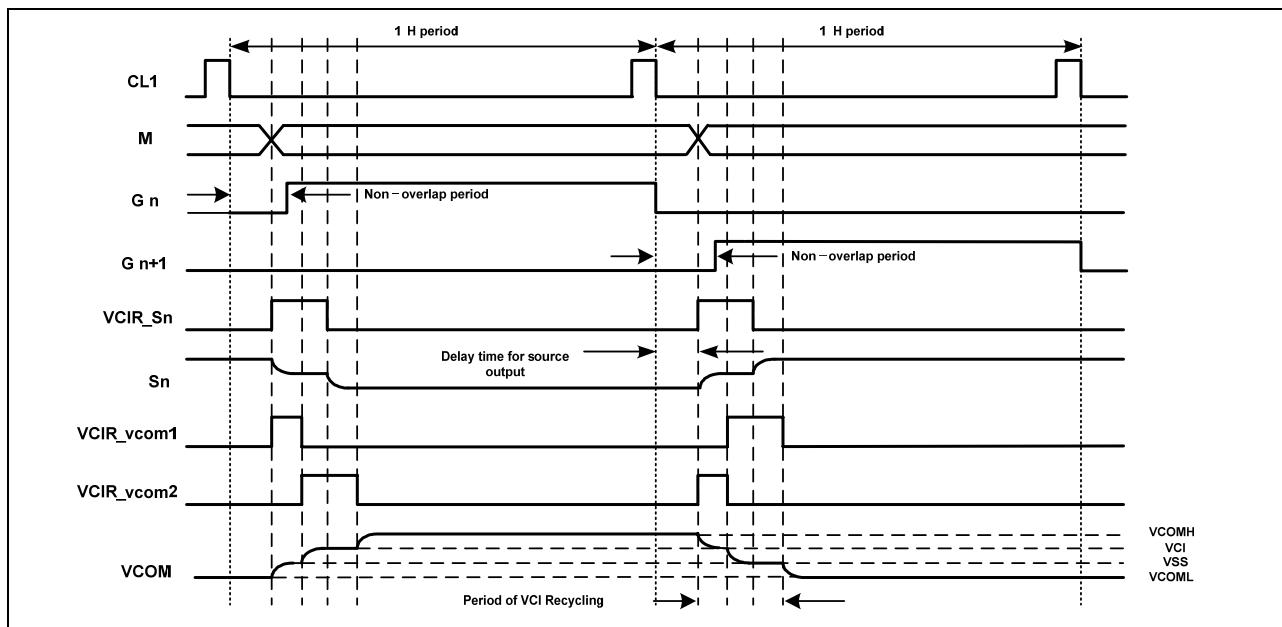
\*unit : INCLK

VCIRA2/ VCIR2	VCIRA1/ VCIR1	VCIRAO/ VCIRO	VCIR / VCI recycling period (Synchronized with INCLK)		
			Sn	Vcom1	Vcom2
0	0	0	0	0	0
0	0	1	1	0.5 / 1	1 / 0.5
0	1	0	2	1 / 2	2 / 1
0	1	1	3	1.5 / 3	3 / 1.5
1	0	0	4	2 / 4	4 / 2
1	0	1	5	2.5 / 5	5 / 2.5
1	1	0	6	3 / 6	6 / 3
1	1	1	7	3.5 / 7	7 / 3.5

Note1. When VCI Recycling is used, VCOMH level must be larger than VCI level.

Note2. INCLK means internal clock for display.

Note3. Do not use VCI Recycling at source driver block in case of Frame Inversion mode.(VCIRA2-0 = 000)

**Figure 149. Set delay from gate output to source output and VCIR signal**

Status	Default Value
Initial	VCIRA[2:0] = 100 VCIR[2:0] = 100

### 5.3.15. SRCCTL : Source Output Control Register (F5h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SRCCTL	R/W	0	1	1	1	1	0	1	0	1	F5h
1 <sup>st</sup> para		1	0	0	0	GS_EN	0	0	NGF	SG	
2 <sup>nd</sup> para		1	0	IPSDT2	IPSDT1	IPSDT0	0	NSDT2	NSDT1	NSDT0	
3 <sup>rd</sup> para		1	0	0	0	0	SAP3	SAP2	SAP1	SAP0	
4 <sup>th</sup> para		1	NBLK_V CIR1	NBLK_ VCIR0	IPBLK_ VCIR1	IPBLK_ VCIR0	NDISP_ CON1	NDISP_ CON0	IPDISP_ CON1	IPDISP_ CON0	
5 <sup>th</sup> para		1	0	VCOM_ BLK_OFF	1	1	NBLK_ CON1	NBLK_ CON0	IPBLK_ CON1	IPBLK_ CON0	
6 <sup>th</sup> para		1	0	0	0	GOCM2	GOCM1	GOCM0	OCM1	OCM0	

#### 5.3.15.1. GS\_EN/ NGF/SG

**GS\_EN:** Set the separated Gamma mode.

**Table 163.GS\_EN**

GS_EN	Gamma set	Description
0	Non- separated Gamma	Red Gamma apply to Green and Blue.
1 (default)	R/G/B Separated Gamma	Use R/G/B separated gamma.

Note: Separated Gamma set is only supported in Gamma Curve1 (GC0).

Note: The gamma command address is setted with below table by GS\_EN and BGR register

GS_EN	BGR	Gamma of red (pos./neg.)	Gamma of green (pos./neg.)	Gamma of blue (pos./neg.)
1	0	F7h / F8h	F9h / FAh	FBh / FCh
1	1	FBh / FCh	F9h / FAh	F7h / F8h
0	0	F7h / F8h	F7h / F8h	F7h / F8h
0	1	F7h / F8h	F7h / F8h	F7h / F8h

**NGF:** Set the negative polarity gamma register to positive polarity gamma register or user setting value. Please refer to the section 4.2

**SG:** Set the symmetric way of negative polarity gamma voltage to positive, X-axis or Y-axis.

Please refer to the section 4.2

Status	Default Value



Initial	GS_EN = 1 NGF = 0 SG = 0
---------	--------------------------------

## 5.3.15.2. IPSDT[2:0]/ NSDT[2:0]

**IPSDT/ NSDT** : Set delay amount from gate edge (end) to source output

IPSDT is applied in Idle Partial mode.

**Table 164. IPSDT[2:0]/NSDT[2:0]**

NSDT2/ IPSDT2	NSDT1/ IPSDT1	NSDT0/ IPSDT0	Delay amount of the source output
0	0	0	1 INCLK
0	0	1	2 INCLK
0	1	0	3 INCLK
0	1	1	4 INCLK
1	0	0	5 INCLK
1	0	1	6 INCLK
1	1	0	7 INCLK
1	1	1	Setting Disable

Note : INCLK means internal clock for display.

In MPU I/F, INCLK is decided by CRTN. (Refer to the section 5.3.12.6)

In RGB I/F, INCLK is decided by RGB\_DIV. (Refer to the section 5.3.16.5)

Status	Default Value
Initial	IPSDT[2:0] = 000 NSDT[2:0] = 000

## 5.3.15.3. SAP[3:0]

**SAP** : Adjust the slew-rate of the operational amplifier for the source driver. If higher SAP3-0 is set, LCD panel having higher resolution or higher frame frequency can be driven because the slew-rate of the operational amplifier is increased. But these bits must be set as adequate value because the amount of fixed current of the operational amplifier is also adjusted. During non-display, when SAP3-0 = "0000," operational amplifiers are turned off, so current consumption can be reduced.

**Table 165. SAP[3:0]**

SAP3	SAP2	SAP1	SAP0	Source Amp. Current Level	Slew rate[us/V]		Delay[us]			
					SG=0	SG=1	SG=0	SG=1		
0	0	0	0	Amp. Stop	-		-			
0	0	0	1	Setting Disable						
0	0	1	0	Setting Disable						
0	0	1	1	Slow 3	5.16		25.8			
0	1	0	0	Medium Slow 1	3.9		19.5			
0	1	0	1	Medium Slow 2	3.1		15.5			
0	1	1	0	Medium Slow 3	2.58		12.9			
0	1	1	1	Medium Slow 4	2.58	2.22	12.9	11.1		
1	0	0	0	Medium Fast 1	2.58	1.94	12.9	9.7		
1	0	0	1	Medium Fast 2	2.58	1.72	12.9	8.6		
1	0	1	0	Medium Fast 3	2.58	1.52	12.9	7.6		
1	0	1	1	Medium Fast 4	2.58	1.36	12.9	6.8		
1	1	0	0	Fast1	2.58	1.20	12.9	6.0		
1	1	0	1	Fast2	2.58	1.08	12.9	5.4		
1	1	1	0	Fast3	2.58	0.94	12.9	4.7		
1	1	1	1	Fast4 (the Fastest)	2.58	0.84	12.9	4.2		

Status	Default Value
Initial	SAP[3:0] = 0011

## 5.3.15.4. NBLK\_VCIR[1:0]/ IPBLK\_VCIR[1:0]/ NDISP\_CON[1:0] / IPDISP\_CON[1:0]

**NBLK\_VCIR/ IPBLK\_VCIR :** In porch period and non-display area VCOM/Source VCIR recycling control

IPBLK\_VCIR is applied in Idle Partial mode

**Table 166. NBLK\_VCIR[1:0]/ IPBLK\_VCIR[1:0]**

NBLK_VCIR1/ IPBLK_VCIR1/	NBLK_VCIR0/ IPBLK_VCIR0/	Porch period	Non-display area
0	0	Disable	Disable
0	1	Active	Disable
1	0	Disable	Active
1	1	Active	Active

**NDISP\_CON[1:0] / IPDISP\_CON [1:0]:** In non-display area, Source driver operation

IPDISP\_CON is applied in Idle Partial mode

**Table 167. NDISP\_CON[1:0]**

NDISP_CON1	NDISP_CON0	Operation
0	0	Amp operation
0	1	Binary operation
1	0	Setting Disable
1	1	Setting Disable

**Table 168. IPDISP\_CON [1:0]**

IPDISP_CON1	IPDISP_CON0	Operation
0	0	Binary operation
0	1	Binary operation
1	0	Setting Disable
1	1	Setting Disable

Status	Default Value
Initial	NBLK_VCIR1[1:0] = 11, IPBLK_VCIR1[1:0] = 11 NDISP_CON[1:0]=00, IPDISP_CON [1:0] = 00

### 5.3.15.5. VCOM\_BLK\_OFF/ NBLK\_CON/IPBLK\_CON

**VCOM\_BLK\_OFF:** If the VCOM\_BLK\_OFF is high, then in porch period VCOM does not toggle. Else, VCOM is continuously toggled in porch period.

**Table 169. VCOM\_BLK\_OFF**

VCOM_BLK_OFF	Operation
0	Operating in porch period
1	Not operation in porch period

**NBLK\_CON / IPBLK\_CON :** In porch period, Source driver operation method. IPBLK\_CON is applied in Idle partial mode

**Table 170. NBLK\_CON[1:0]**

NBLK_CON1	NBLK_CON0	Operation
0	0	AMP operation
0	1	Binary operation
1	0	GND
1	1	Hi-Z

**Table 171. IPBLK\_CON[1:0]**

IPBLK_CON1	IPBLK_CON0	Operation
0	0	Binary operation
0	1	Binary operation
1	0	GND
1	1	Hi-Z

Status	Default Value
Initial	VCOM_BLK_OFF = 1 NBLK_CON[1:0] = 00 IPBLK_CON[1:0] = 00

### 5.3.15.6. OCM[1:0]/GOCM[2:0]

**GOCM2-0:** The control bits to cancel the offset voltage of the gamma amp. This register supports the line and frame offset cancellation mode.

**Table 172. GOCM[2:0]**

GOCM2	GOCM1	GOCM0	Source amp. Offset cancellation mode selection
0	0	0	4 line and 8 frame offset cancellation mode
0	0	1	2 line and 8 frame offset cancellation mode
0	1	0	8 frame offset cancellation mode
0	1	1	4 frame offset cancellation mode
1	0	0	4 frame offset cancellation mode
1	0	1	2 line and 4 frame offset cancellation mode
1	1	0	1 line and 4 frame offset cancellation mode
1	1	1	GPOL="L" fix

Note : GPOL : The register bit for the Gamma amp. polarity.

**OCM1-0:** The control bits to cancel the offset voltage of the source amp. This register supports the line and frame offset cancellation mode.

**Table 173. OCM[1:0]**

OCM1	OCM0	Source amp. Offset cancellation mode selection
0	0	2 line and 4 frame offset cancellation mode
0	1	1 line and 4 frame offset cancellation mode
1	0	4 frame offset cancellation mode
1	1	POL="L" fix

Note : POL : The register bit for the source amp polarity.

Status	Default Value
Initial	GOCM[2:0] = 111 OCM[1:0] = 11

### 5.3.16. IFCTL : Interface Control Register (F6h)

<b>Inst / Para</b>	<b>R/W</b>	<b>DCX</b>	<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	<b>HEX</b>
IFCTL	<b>R/W</b>	0	1	1	1	1	0	1	1	0	F6h
1 <sup>st</sup> para		1	MY_EOR	MX_EOR	MV_EOR	ML_EOR	BGR_EOR	0	0	0	
2 <sup>nd</sup> para		1	IPM2	IPM1	IPM0	MDT1	MDT0	CM	VSM	DM	
3 <sup>rd</sup> para		1	VPL	HPL	DPL	EPL	ENDIAN	0	0	RIM	
4 <sup>th</sup> para		1	0	0	SPR_SEL1	SPR_SEL0	RGB_DIV3	RGB_DIV2	RGB_DIV1	RGB_DIV0	

#### 5.3.16.1. MY\_EOR/ MX\_EOR/ MV\_EOR/ ML\_EOR/ BGR\_EOR

Each of these register will be used inside the IC. The set value of MADCTL is used in the IC is derived as exclusive OR between 1<sup>st</sup> parameter of IFCTL and MADCTL parameter.

<b>Status</b>	<b>Default Value</b>
Initial	MY_EOR = 0, MX_EOR = 0, MV_EOR = 0 ML_EOR = 0, BGR_EOR = 0

## 5.3.16.2. IPM[2:0]/ MDT[1:0]/ CM/VSM/ DM

**IPM:** Select the method of display expansion when CM = low. (Default value = 100)

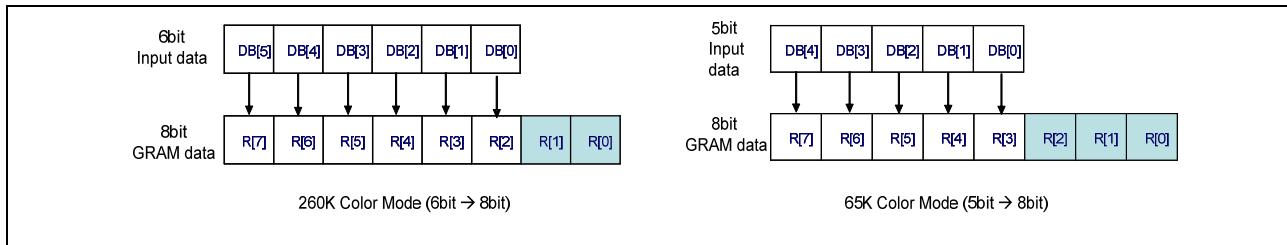


Figure 150. Data expansion by IPM (example of red color)

Table 174. IPM[2:0]

IPM	6bit → 8bit		5bit → 8bit		
	R[1]	R[0]	R[2]	R[1]	R[0]
000	0	0	DB[4]	0	0
001	0	1	DB[4]	0	1
010	1	0	DB[4]	1	0
011	1	1	DB[4]	1	1
100	DB[5]	DB[4]	DB[4]	DB[4]	DB[3]
101	DB[5]	0	DB[4]	DB[4]	0
110	DB[5]	1	DB[4]	DB[4]	1
111	Not defined		Not defined		

**MDT:** Select the method of display data transferring. (Refer to the 3.2 Display Data Format section.)

**CM :** Select the method of display data expansion in 260k, 65k color mode

Table 175. CM

CM	Display data expansion method
0	Decide by IPM[2:0]
1	Using Look Up Table

**VSM :** Select Vsync Interface mode.

When VSM="1", VSYNC interface is available. In this interface the internal display operation is synchronized with VSYNC. Data for display is written to RAM via the system interface with higher speed than for internal display operation. This method enables flicker-free display of motion pictures with the conventional interface. Refer to section 3.4.

**DM** : Specify the display operation mode. The interface can be set based on the bits of DM. This setting enables switching interface between internal operation and the external display interface.

**Table 176.DM**

DM	Display Operation Mode
0	Internal clock operation
1	RGB interface mode

Note1. Internal Clock Operation Mode with System Interface (DM=0)

Every operation in Internal Clock Operation mode is done in synchronization with the internal clock which is generated by internal OSC.

The signals input through RGB interface are all meaningless. Access to internal GRAM is done via system interface.

Note2. External Clock Operation Mode with RGB Interface (DM=1)

In External Clock Operation mode, frame sync signal (VSYNC), line sync signal (HSYNC) and DOTCLK are used for display operation.

Display data is transferred in the unit of pixel through DB bus and saved to GRAM.

Status	Default Value
Initial	IPM[2:0] = 100 MDT[1:0] = 00 CM = 0 VSM = 0 DM = 0

## 5.3.16.3. VPL/HPL/DPL/EPL

**VPL** : Reverses the polarity of the VSYNC signal.

VPL= "0": VSYNC is low active.

VPL= "1": VSYNC is high active.

**HPL** : Reverses the polarity of the HSYNC signal.

HPL= "0": HSYNC is low active.

HPL= "1": HSYNC is high active.

**DPL** : Reverses the polarity of the DOTCLK signal.

DPL= "0": Display data is fetched at DOTCLK's rising edge.

DPL= "1": Display data is fetched at DOTCLK's falling edge.

**EPL** : Set the polarity of ENABLE pad while using RGB interface.

- EPL = "0": ENABLE ="Low" / write data of DB23

ENABLE ="High" / do not write data of DB23

- EPL = "1": ENABLE ="High" / write data of DB23

ENABLE ="Low" / do not write data of DB23

Note : If Interface mode is RGB 6bit, EPL should be set to Low.

**Table 177. Relationship between EPL, ENABLE and RAM access**

EPL	ENABLE	RAM write	RAM address
0	0	Valid	Updated
0	1	Invalid	Held
1	1	Valid	Updated
1	0	Invalid	Held

Status	Default Value
Initial	VPL = 0 HPL = 0 DPL = 0 EPL = 0

## 5.3.16.4. ENDIAN/RIM

**ENDIAN:** Select Little Endian Interface bit. At Little Endian mode, the host sends LSB data first.

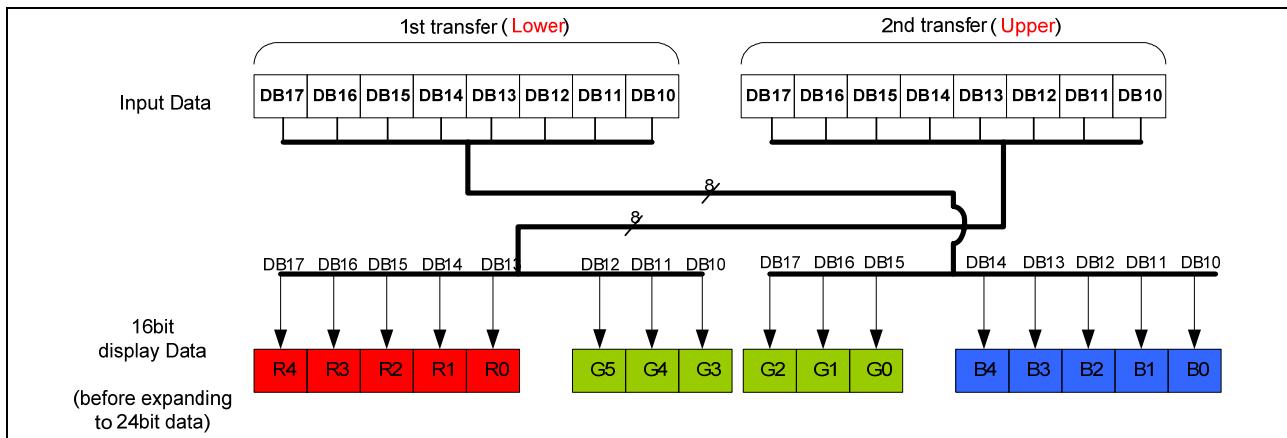


Figure 151. Little endian (65K 8bit I/F type )

Table 178.ENDIAN

ENDIAN	Data transfer mode
0	Normal (MSB first)
1	Little Endian (LSB first)

Note. Little Endian is valid on only 260K 9bit I/F(MDT=00), 65K 8bit, 9bit I/F mode.

**RIM:** Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.

Table 179.RIM

RIM	COLMOD[6:4]	RGB Interface Mode
0	111 (16M color)	24- bit RGB interface (1 transfer/pixel)
	110 (262k color)	18- bit RGB interface (1 transfer/pixel)
	101 (65k color)	16- bit RGB interface (1 transfer/pixel)
1	111 (16M color)	8- bit RGB interface (3 transfer/pixel)
	110 (262k color)	6- bit RGB interface (3 transfer/pixel)

Status	Default Value
Initial	ENDIAN = 0 RIM = 0

## 5.3.16.5. SPR\_SEL[1:0]/ RGB\_DIV[3:0]

**SPR\_SEL[1:0]**: Short Pulse Rejection (SPR) Selection bit. SPR\_SEL1 selects SPR time and SPR\_SEL0 selects SPR On/Off.

**Table 180. SPR\_SEL[1:0]**

SPR_SEL[1]	SPR_SEL[0]	Description
X	0	Disable SPR function to Logic input pad.
0	1	Activate 5ns SPR function to Logic input pad.
1	1	Activate 10ns SPR function to Logic input pad.

**RGB\_DIV3-0** : Select internal clock in RGB interface mode

**Table 181. RGB\_DIV[3:0]**

RGB_DIV[3:0]	INCLK	
	24/18/16- bit RGB	8/6- bit RGB
0000	16 DOTCLK	16 x 3 DOTCLK
0001	15 DOTCLK	15 x 3 DOTCLK
0010	14 DOTCLK	14 x 3 DOTCLK
0011	13 DOTCLK	13 x 3 DOTCLK
0100	12 DOTCLK	12 x 3 DOTCLK
0101	11 DOTCLK	11 x 3 DOTCLK
0110	10 DOTCLK	10 x 3 DOTCLK
0111	9 DOTCLK	9 x 3 DOTCLK
1000	16 DOTCLK	16 x 3 DOTCLK
1001	17 DOTCLK	17 x 3 DOTCLK
1010	18 DOTCLK	18 x 3 DOTCLK
1011	19 DOTCLK	19 x 3 DOTCLK
1100	20 DOTCLK	20 x 3 DOTCLK
1101	21 DOTCLK	21 x 3 DOTCLK
1110	22 DOTCLK	22 x 3 DOTCLK
1111	23 DOTCLK	23 x 3 DOTCLK

Note. INCLK means Internal Clock for display.

Status	Default Value
Initial	SPR_SEL = 01 RGB_DIV = 0000

## 5.3.17. RGAMCTL : Positive Gamma Control Register for Red (F7h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RPGAMCTL	R/W	0	1	1	1	1	0	1	1	1	F7h
1 <sup>st</sup> para		1	RGLP1	RGLP0	RRFP5	RRFP4	RRFP3	RRFP2	RRFP1	RRFP0	
2 <sup>nd</sup> para		1	0	0	ROSP5	ROSP4	ROSP3	ROSP2	ROSP1	ROSP0	
3 <sup>rd</sup> para		1	0	0	RPKP05	RPKP04	RRPKP3	RPKP02	RPKP01	RPKP0	
4 <sup>th</sup> para		1	0	0	RPKP15	RPKP14	RPKP13	RPKP12	RPKP11	RPKP10	
5 <sup>th</sup> para		1	0	0	RPKP25	RPKP24	RPKP23	RPKP22	RPKP21	PKP20	
6 <sup>th</sup> para		1	0	0	RPKP35	RPKP34	RPKP33	RPKP32	RPKP31	RPKP30	
7 <sup>th</sup> para		1	0	0	RPKP45	RPKP44	RPKP43	RPKP42	RPKP41	RPKP40	
8 <sup>th</sup> para		1	0	0	RPKP55	RPKP54	RPKP53	RPKP52	RPKP51	RPKP50	
9 <sup>th</sup> para		1	0	0	RPKP65	RPKP64	RPKP63	RPKP62	RPKP61	RPKP60	
10 <sup>th</sup> para		1	0	0	RPKP75	RPKP74	RPKP73	RPKP72	RPKP71	RPKP70	
11 <sup>th</sup> para		1	0	0	RPKP85	RPKP84	RPKP83	RPKP82	RPKP81	RPKP80	
12 <sup>th</sup> para		1	0	0	RPKP95	RPKP94	RPKP93	RPKP92	RPKP91	RPKP90	
13 <sup>th</sup> para		1	0	0	RPKP10	RPKP10	RPKP10	RPKP10	RPKP10	RPKP10	
14 <sup>th</sup> para		1	3	2	1	0	3	2	1	0	
15 <sup>th</sup> para		1	3	2	1	0	3	2	1	0	

**RGLP:** The positive voltage of red color grayscale number V1 or V254 is mainly adjusted.

**RRFP:** The positive voltage of red color grayscale number from V0 is mainly adjusted.

**ROSP:** The positive voltage of red color grayscale number from V255 is mainly adjusted.

**RPKP0~RPKP10:** The positive voltage of red color grayscale number from V1 to V254 is finely adjusted.

**RGSRP0:** The positive voltage of red color grayscale V5 is finely adjusted.

**RGSRP1:** The positive voltage of red color grayscale V55 is finely adjusted.

**RGSRP2:** The positive voltage of red color grayscale V200 is finely adjusted.

**RGSRP3:** The positive voltage of red color grayscale V250 is finely adjusted.

Status	Default Value
Initial	06_03_04_0A_10_1A_22_2C_13_12_1D_11_02_22_22h

note 1. when BGR=1, F7h command is BGMACTL



## 5.3.18. RNGAMCTL : Negative Gamma Control Register for Red (F8h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RNGAMCTL	R/W	0	1	1	1	1	1	0	0	0	F8h
1 <sup>st</sup> para		1	RGLN1	RGLN0	RRFN5	RRFN4	RRFN3	RRFN2	RRFN1	RRFN0	
2 <sup>nd</sup> para		1	0	0	ROSN5	ROSN4	ROSN3	ROSN2	ROSN1	ROSN0	
3 <sup>rd</sup> para		1	0	0	RPKN05	RPKN04	RPKN03	RPKN02	RPKN01	RPKN0	
4 <sup>th</sup> para		1	0	0	RPKN15	RPKN14	RPKN13	RPKN12	RPKN11	RPKN10	
5 <sup>th</sup> para		1	0	0	RPKN25	RPKN24	RPKN23	RPKN22	RPKN21	RPKN20	
6 <sup>th</sup> para		1	0	0	RPKN35	RPKN34	RPKN33	RPKN32	RPKN31	RPKN30	
7 <sup>th</sup> para		1	0	0	RPKN45	RPKN44	RPKN43	RPKN42	RPKN41	RPKN40	
8 <sup>th</sup> para		1	0	0	RPKN55	RPKN54	RPKN53	RPKN52	RPKN51	RPKN50	
9 <sup>th</sup> para		1	0	0	RPKN65	RPKN64	RPKN63	RPKN62	RPKN61	RPKN60	
10 <sup>th</sup> para		1	0	0	RPKN75	RPKN74	RPKN73	RPKN72	RPKN71	RPKN70	
11 <sup>th</sup> para		1	0	0	RPKN85	RPKN84	RPKN83	RPKN82	RPKN81	RPKN80	
12 <sup>th</sup> para		1	0	0	RPKN95	RPKN94	RPKN93	RPKN92	RPKN91	RPKN90	
13 <sup>th</sup> para		1	0	0	RPKN10	RPKN10	RPKN10	RPKN10	RPKN10	RPKN10	
14 <sup>th</sup> para		1	RGSRN 03	RGSRN 02	RGSRN 01	RGSRN 00	RGSRN 13	RGSRN 12	RGSRN1 1	RGSRN 10	
15 <sup>th</sup> para		1	RGSRN 23	RGSRN 22	RGSRN 21	RGSRN 20	RGSRN 33	RGSRN 32	RGSRN 31	RGSRN 30	

**RGLN:** The negative voltage of red color grayscale V1 or V254 is mainly adjusted.

**RRFN:** The negative voltage of red color grayscale number from V0 is mainly adjusted.

**ROSN:** The negative voltage of red color grayscale number from V255 is mainly adjusted.

**RPKN0~RPKN10:** The negative red color voltage of grayscale number from V1 to V254 is finely adjusted.

**RGSRN0:** The negative voltage of red color grayscale V5 is finely adjusted.

**RGSRN1:** The negative voltage of red color grayscale V55 is finely adjusted.

**RGSRN2:** The negative voltage of red color grayscale V200 is finely adjusted.

**RGSRN3:** The negative voltage of red color grayscale V250 is finely adjusted.

Status	Default Value
Initial	06_03_04_0A_10_1A_22_2C_13_12_1D_11_02_22_22h

note 1. when BGR=1, F8h command is BNGMACTL



## 5.3.19. GGAMCTL : Positive Gamma Control Register for Green (F9h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GPGAMCTL	R/W	0	1	1	1	1	1	0	0	1	F9h
1 <sup>st</sup> para		1	GGLP1	GGLP0	GRFP5	GRFP4	GRFP3	GRFP2	GRFP1	GRFP0	
2 <sup>nd</sup> para		1	0	0	GOSP5	GOSP4	GOSP3	GOSP2	GOSP1	GOSP0	
3 <sup>rd</sup> para		1	0	0	GPKP05	GPKP04	GPKP03	GPKP02	GPKP01	GPKP0	
4 <sup>th</sup> para		1	0	0	GPKP15	GPKP14	GPKP13	GPKP12	GPKP11	GPKP10	
5 <sup>th</sup> para		1	0	0	GPKP25	GPKP24	GPKP23	GPKP22	GPKP21	GPKP20	
6 <sup>th</sup> para		1	0	0	GPKP35	GPKP34	GPKP33	GPKP32	GPKP31	GPKP30	
7 <sup>th</sup> para		1	0	0	GPKP45	GPKP44	GPKP43	GPKP42	GPKP41	GPKP40	
8 <sup>th</sup> para		1	0	0	GPKP55	GPKP54	GPKP53	GPKP52	GPKP51	GPKP50	
9 <sup>th</sup> para		1	0	0	GPKP65	GPKP64	GPKP63	GPKP62	GPKP61	GPKP60	
10 <sup>th</sup> para		1	0	0	GPKP75	GPKP74	GPKP73	GPKP72	GPKP71	GPKP70	
11 <sup>th</sup> para		1	0	0	GPKP85	GPKP84	GPKP83	GPKP82	GPKP81	GPKP80	
12 <sup>th</sup> para		1	0	0	GPKP95	GPKP94	GPKP93	GPKP92	GPKP91	GPKP90	
13 <sup>th</sup> para		1	0	0	5	4	3	2	1	0	
14 <sup>th</sup> para		1	GGSRP 03	GGSRP 02	GGSRP 01	GGSRP 00	GGSRP 13	GGSRP 12	GGSRP1 1	GGSRP 10	
15 <sup>th</sup> para		1	GGSRP 23	GGSRP 22	GGSRP 21	GGSRP 20	GGSRP 33	GGSRP 32	GGSRP 31	GGSRP 30	

**GGLP:** The positive voltage of green color grayscale V1 or V254 is mainly adjusted.

**GRFP:** The positive voltage of green color grayscale number from V0 is mainly adjusted.

**GOSP:** The positive voltage of green color grayscale number from V255 is mainly adjusted.

**GPKP0~GPKP10:** The positive voltage of green color grayscale number from V1 to V254 is finely adjusted.

**GGSRP0:** The positive voltage of green color grayscale V5 is finely adjusted.

**GGSRP1:** The positive voltage of green color grayscale V55 is finely adjusted.

**GGSRP2:** The positive voltage of green color grayscale V200 is finely adjusted.

**GGSRP3:** The positive voltage of green color grayscale V250 is finely adjusted.

Status	Default Value
Initial	06_03_04_0A_10_1A_22_2C_13_12_1D_11_02_22_22h



### 5.3.20. GNGAMCTL : Negative Gamma Control Register for Green (FAh)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GNGAMCTL	R/W	0	1	1	1	1	1	0	1	0	FAh
1 <sup>st</sup> para		1	GGLN1	GGLN0	GRFN5	GRFN4	GRFN3	GRFN2	GRFN1	GRFN0	
2 <sup>nd</sup> para		1	0	0	GOSN5	GOSN4	GOSN3	GOSN2	GOSN1	GOSN0	
3 <sup>rd</sup> para		1	0	0	GPKN05	GPKN04	GPKN03	GPKN02	GPKN01	GPKN00	
4 <sup>th</sup> para		1	0	0	GPKN15	GPKN14	GPKN13	GPKN12	GPKN11	GPKN10	
5 <sup>th</sup> para		1	0	0	GPKN25	GPKN24	GPKN23	GPKN22	GPKN21	GPKN20	
6 <sup>th</sup> para		1	0	0	GPKN35	GPKN34	GPKN33	GPKN32	GPKN31	GPKN30	
7 <sup>th</sup> para		1	0	0	GPKN45	GPKN44	GPKN43	GPKN42	GPKN41	GPKN40	
8 <sup>th</sup> para		1	0	0	GPKN55	GPKN54	GPKN53	GPKN52	GPKN51	GPKN50	
9 <sup>th</sup> para		1	0	0	GPKN65	GPKN64	GPKN63	GPKN62	GPKN61	GPKN60	
10 <sup>th</sup> para		1	0	0	GPKN75	GPKN74	GPKN73	GPKN72	GPKN71	GPKN70	
11 <sup>th</sup> para		1	0	0	GPKN85	GPKN84	GPKN83	GPKN82	GPKN81	GPKN80	
12 <sup>th</sup> para		1	0	0	GPKN95	GPKN94	GPKN93	GPKN92	GPKN91	GPKN90	
13 <sup>th</sup> para		1	0	0	5	4	3	2	1	0	
14 <sup>th</sup> para		1	GGSRN 03	GGSRN0 2	GGSRN0 1	GGSRN0 0	GGSRN 13	GGSRN1 2	GGSRN1 1	GGSRN1 0	
15 <sup>th</sup> para		1	GGSRN 23	GGSRN2 2	GGSRN2 1	GGSRN2 0	GGSRN 33	GGSRN3 2	GGSRN3 1	GGSRN3 0	

**GGLN:** The negative voltage of green color grayscale V1 or V254 is mainly adjusted.

**GRFN:** The negative voltage of green color grayscale number from V0 is mainly adjusted.

**GOSN:** The negative voltage of green color grayscale number from V255 is mainly adjusted.

**GPKN0~GPKN10:** The negative green color voltage of grayscale number from V1 to V254 is finely adjusted.

**GGSRN0:** The negative voltage of green color grayscale V5 is finely adjusted.

**GGSRN1:** The negative voltage of green color grayscale V55 is finely adjusted.

**GGSRN2:** The negative voltage of green color grayscale V200 is finely adjusted.

**GGSRN3:** The negative voltage of green color grayscale V250 is finely adjusted.

Status	Default Value
Initial	06_03_04_0A_10_1A_22_2C_13_12_1D_11_02_22_22h

## 5.3.21. BGAMCTL : Positive Gamma Control Register for Blue (FBh)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BPGAMCTL	R/W	0	1	1	1	1	1	0	1	1	FBh
1 <sup>st</sup> para		1	BGLP1	BGLP0	BRFP5	BRFP4	BRFP3	BRFP2	BRFP1	BRFP0	
2 <sup>nd</sup> para		1	0	0	BOSP5	BOSP4	BOSP3	BOSP2	BOSP1	BOSP0	
3 <sup>rd</sup> para		1	0	0	BPKP05	BPKP04	BPKP3	BPKP02	BPKP01	BPKP0	
4 <sup>th</sup> para		1	0	0	BPKP15	BPKP14	BPKP13	BPKP12	BPKP11	BPKP10	
5 <sup>th</sup> para		1	0	0	BPKP25	BPKP24	BPKP23	BPKP22	BPKP21	BKP20	
6 <sup>th</sup> para		1	0	0	BPKP35	BPKP34	BPKP33	BPKP32	BPKP31	BPKP30	
7 <sup>th</sup> para		1	0	0	BPKP45	BPKP44	BPKP43	BPKP42	BPKP41	BPKP40	
8 <sup>th</sup> para		1	0	0	BPKP55	BPKP54	BPKP53	BPKP52	BPKP51	BPKP50	
9 <sup>th</sup> para		1	0	0	BPKP65	BPKP64	BPKP63	BPKP62	BPKP61	BPKP60	
10 <sup>th</sup> para		1	0	0	BPKP75	BPKP74	BPKP73	BPKP72	BPKP71	BPKP70	
11 <sup>th</sup> para		1	0	0	BPKP85	BPKP84	BPKP83	BPKP82	BPKP81	BPKP80	
12 <sup>th</sup> para		1	0	0	BPKP95	BPKP94	BPKP93	BPKP92	BPKP91	BPKP90	
13 <sup>th</sup> para		1	0	0	BPKP10	BPKP10	BPKP10	BPKP10	BPKP10	BPKP10	
14 <sup>th</sup> para		1	3	2	1	0	3	2	1	0	
15 <sup>th</sup> para		1	3	2	1	0	3	2	1	0	

**BGLP:** The positive voltage of blue color grayscale V1 or V254 is mainly adjusted.

**BRFP:** The positive voltage of blue color grayscale number from V0 is mainly adjusted.

**BOSP:** The positive voltage of blue color grayscale number from V255 is mainly adjusted.

**BPKP0~BPKP10:** The positive voltage of blue color grayscale number from V1 to V254 is finely adjusted.

**BGSRP0:** The positive voltage of blue color grayscale V5 is finely adjusted.

**BGSRP1:** The positive voltage of blue color grayscale V55 is finely adjusted.

**BGSRP2:** The positive voltage of blue color grayscale V200 is finely adjusted.

**BGSRP3:** The positive voltage of blue color grayscale V250 is finely adjusted.

Status	Default Value
Initial	06_03_04_0A_10_1A_22_2C_13_12_1D_11_02_22_22h

note 1. when BGR=1, FBh command is RGMACTL



## 5.3.22. BNGAMCTL : Negative Gamma Control Register for Blue(FCh)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BNGAMCTL	R/W	0	1	1	1	1	1	1	0	0	FCh
1 <sup>st</sup> para		1	BGLN1	BGLN0	BRFN5	BRFN4	BRFN3	BRFN2	BRFN1	BRFN0	
2 <sup>nd</sup> para		1	0	0	BOSN5	BOSN4	BOSN3	BOSN2	BOSN1	BOSN0	
3 <sup>rd</sup> para		1	0	0	BPKN05	BPKN04	BPKN03	BPKN02	BPKN01	BPKN0	
4 <sup>th</sup> para		1	0	0	BPKN15	BPKN14	BPKN13	BPKN12	BPKN11	BPKN10	
5 <sup>th</sup> para		1	0	0	BPKN25	BPKN24	BPKN23	BPKN22	BPKN21	BPKN20	
6 <sup>th</sup> para		1	0	0	BPKN35	BPKN34	BPKN33	BPKN32	BPKN31	BPKN30	
7 <sup>th</sup> para		1	0	0	BPKN45	BPKN44	BPKN43	BPKN42	BPKN41	BPKN40	
8 <sup>th</sup> para		1	0	0	BPKN55	BPKN54	BPKN53	BPKN52	BPKN51	BPKN50	
9 <sup>th</sup> para		1	0	0	BPKN65	BPKN64	BPKN63	BPKN62	BPKN61	BPKN60	
10 <sup>th</sup> para		1	0	0	BPKN75	BPKN74	BPKN73	BPKN72	BPKN71	BPKN70	
11 <sup>th</sup> para		1	0	0	BPKN85	BPKN84	BPKN83	BPKN82	BPKN81	BPKN80	
12 <sup>th</sup> para		1	0	0	BPKN95	BPKN94	BPKN93	BPKN92	BPKN91	BPKN90	
13 <sup>th</sup> para		1	0	0	BPKN10	BPKN10	BPKN10	BPKN10	BPKN10	BPKN10	
14 <sup>th</sup> para		1	3	2	1	0	3	2	1	0	
15 <sup>th</sup> para		1	3	2	1	0	3	2	1	0	

**BGLN:** The negative voltage of blue color grayscale number from V1 or V254 is mainly adjusted.

**BRFN:** The negative voltage of blue color grayscale number from V0 is mainly adjusted.

**BOSN:** The negative voltage of blue color grayscale number from V255 is mainly adjusted.

**BPKN0~BPKN10:** The negative blue color voltage of grayscale number from V1 to V254 is finely adjusted.

**BGSRN0:** The negative voltage of blue color grayscale V5 is finely adjusted.

**BGSRN1:** The negative voltage of blue color grayscale V55 is finely adjusted.

**BGSRN2:** The negative voltage of blue color grayscale V200 is finely adjusted.

**BGSRN3:** The negative voltage of blue color grayscale V250 is finely adjusted.

Status	Default Value
Initial	06_03_04_0A_10_1A_22_2C_13_12_1D_11_02_22_22h

note 1. when BGR=1, FCh command is RNGMACTL



### 5.3.23. GATECTL : Gate Control Register (FDh)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GATECTL	R/W	0	1	1	1	1	1	0	1	1	FDh
1 <sup>st</sup> param		1	0	IPNO2	IPNO1	IPNO0	0	NNO2	NNO1	NNO0	

**IPNO/NNO** : Set amount of non-overlap for the gate output.

IPNO is applied in Idle Partial mode.

**Table 182. IPNO[2:0]/ NNO[2:0]**

IPNO2 / NNO2	IPNO1 / NNO1	IPNO0 /NNO0	Amount of non-overlap
0	0	0	Setting disable
0	0	1	1 INCLK
0	1	0	2 INCLK
0	1	1	3 INCLK
1	0	0	4 INCLK
1	0	1	5 INCLK
1	1	0	6 INCLK
1	1	1	7 INCLK

Note1. The amount of non-overlap time is defined from starting time of 1H.

Note2. INCLK means internal clock for display.

In MPU I/F, INCLK is decided by CRTN. (Refer to the section 5.3.12.6)

In RGB I/F, INCLK is decided by RGB\_DIV. (Refer to the section 5.3.16.5)

Status	Default Value
Initial	IPNO[2:0] = 001 NNO[2:0] = 001

### 5.3.24. EDSTEST : EDS Test Register (FFh)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
EDSTEST	R/W	0	1	1	1	1	1	1	1	1	FFh
1 <sup>st</sup> param		1	-	-	0	0	0	0	0	0	
2 <sup>nd</sup> param		1	-	-	0	0	0	0	0	0	
3 <sup>rd</sup> param		1	-	-	0	0	0	0	0	0	
4th param		1	-	SD_EN	SD1	SD2	SD3	0	0	0	
5th param		1	-	-	0	0	0	0	0	0	

**SD\_EN** : Select S/D Free (shottky-diode-free) mode On/Off (0 : OFF, 1: ON)

**SD1** : S/D Free mode control register. At automatic power-up mode(APON=1), L → H after 1/4 frame.

**SD2** : S/D Free mode control register. At automatic power-up mode(APON=1), same as PON1.

**SD3** : S/D Free mode control register. At automatic power-up mode(APON=1), same as PON2.

Status	Default Value
Initial	1st para: 0000_0000 2nd para: 0000_0000 3rd para: 0000_0000 4th para: 0000_0000

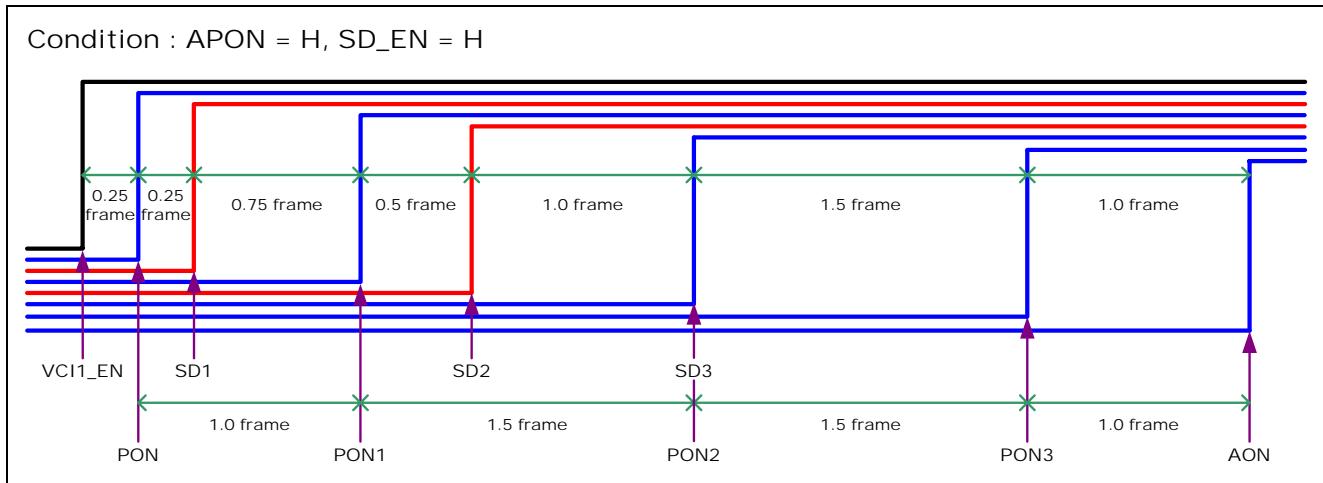


Figure 152. S/D Free Signal Timing Diagram in Automatic Power-up Sequence

note 1. In case of "APON=L", SD1,SD2 & SD3 should be issued exactly the same as Figure 152

### 5.3.25. DCON : Manual Display Control Register (D9h)

Inst / Para	R/W	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DCON	R/W	0	1	1	1	1	1	1	1	1	D9h
1 <sup>st</sup> param		1	0	0	0	0	0	0	0	0	
2 <sup>nd</sup> param		1	TESTK 7	TESTK 6	TESTK 5	TESTK 4	TESTK 3	TESTK 2	TESTK 1	TESTK 0	
3 <sup>rd</sup> param		1	0	0	0	0	0	0	0	0	

**TESTK7-0:** Level 3 Command Protection TEST\_KEY. If use Level 3 Command (FEh,FFh), this Register should be set to "5Ah" for writing Level 3 registers

Status	Default Value
Initial	TESTK[7:0]=0000_0000

## CHAPTER 6

# APPENDIX

- 6.1 Application Circuit
- 6.2 External Component
- 6.3 PAD Center Coordinates
- 6.4 Display Module Default Position

# 6 APPENDIX

## 6.1. APPLICATION CIRCUIT

A typical application circuit is shown in following figure.

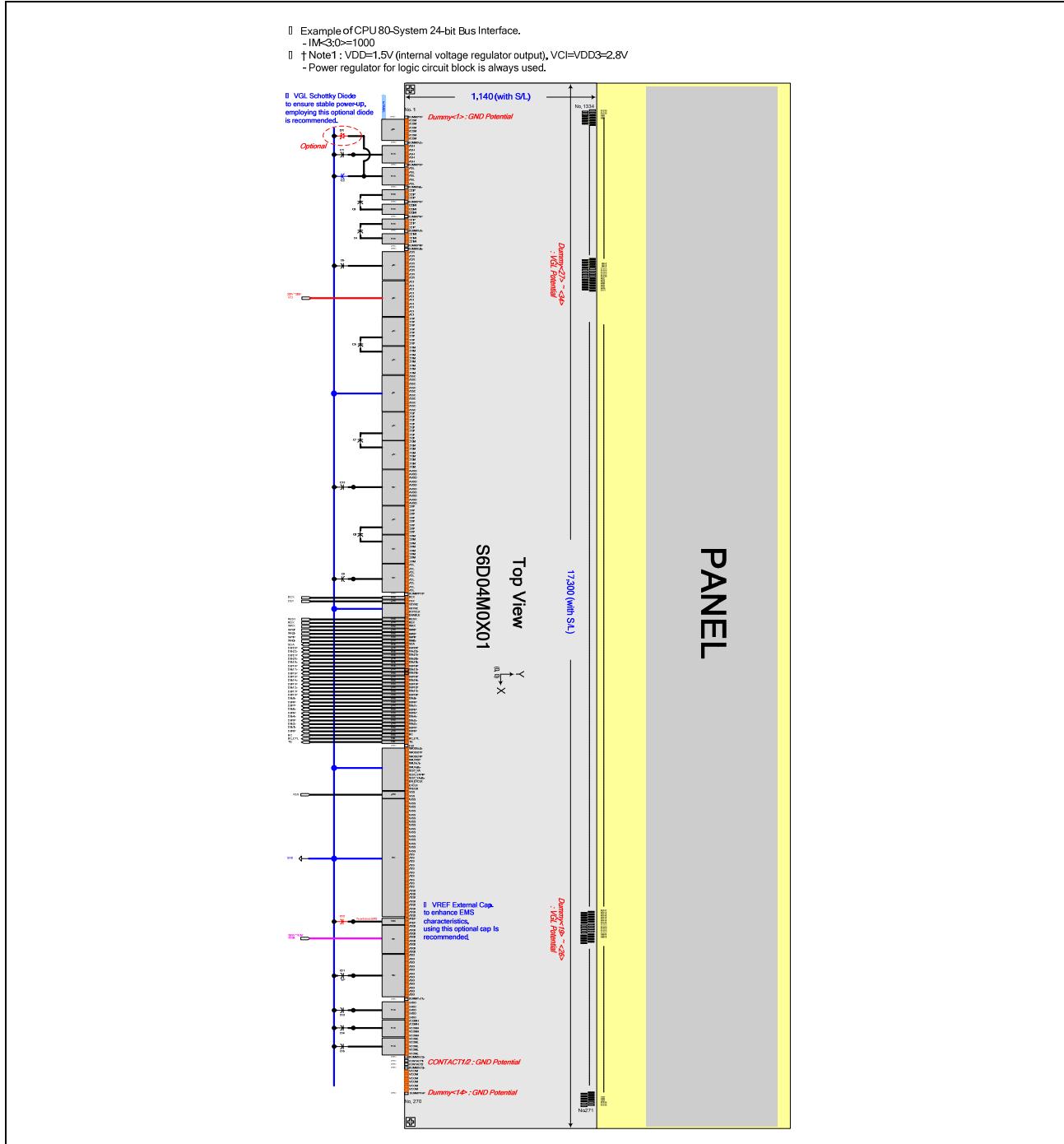


Figure 153. Application circuit

## 6.2. EXTERNAL COMPONENT

**Table 183. External components**

Name	Device	Value	Connection	Note	
C1	Capacitor	1uF	VGH – GND	Maximum Ratings Voltage	18V
C2	Capacitor	1uF	VGL – GND		18V
C3	Capacitor	1uF	C22M – C22P		18V
C4	Capacitor	1uF	C21M – C21P		18V
C5	Capacitor	1uF	VCI1 - GND		3V
C6	Capacitor	1uF	C11M – C11P		6V
C7	Capacitor	1uF	C12M – C12P		6V
C8	Capacitor	1uF	C31M – C31P		6V
C9	Capacitor	1uF	VCL – GND		3V
C10	Capacitor	1uF	AVDD – GND		10V
C11	Capacitor	1uF	VDD – GND		3V
C12	Capacitor	1uF	VREF – GND		3V
C13	Capacitor	1uF	GVDD – GND		6V
C14	Capacitor	1uF	VCOMH - GND		6V
C15	Capacitor	1uF	VCOML – GND		3V
D1	Diode	-	(+)VGL – GND(-)	VF < 0.4V (@ IF = 20mA, Ta = 25 ) VR ≥ max.25V	

Note. Component C12 (described in gray-color) is optional for this application.

### 6.3. PAD CENTER COORDINATES

**Table 184. Pad center coordinates [Unit: μm]**

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
1	DUMMY<1> GND	-8433	-495	51	VCI	-5433	-495	101	AVDD	-2433	-495
2	VCOM	-8373	-495	52	VCI	-5373	-495	102	AVDD	-2373	-495
3	VCOM	-8313	-495	53	VCI	-5313	-495	103	AVDD	-2313	-495
4	VCOM	-8253	-495	54	VCI	-5253	-495	104	AVDD	-2253	-495
5	VCOM	-8193	-495	55	VCI	-5193	-495	105	AVDD	-2193	-495
6	VCOM	-8133	-495	56	C11P	-5133	-495	106	AVDD	-2133	-495
7	VCOM	-8073	-495	57	C11P	-5073	-495	107	AVDD	-2073	-495
8	DUMMY<2>	-8013	-495	58	C11P	-5013	-495	108	C31P	-2013	-495
9	VGH	-7953	-495	59	C11P	-4953	-495	109	C31P	-1953	-495
10	VGH	-7893	-495	60	C11P	-4893	-495	110	C31P	-1893	-495
11	VGH	-7833	-495	61	C11P	-4833	-495	111	C31P	-1833	-495
12	VGH	-7773	-495	62	C11P	-4773	-495	112	C31P	-1773	-495
13	VGH	-7713	-495	63	C11P	-4713	-495	113	C31P	-1713	-495
14	DUMMY<3>	-7653	-495	64	C11M	-4653	-495	114	C31P	-1653	-495
15	VGL	-7593	-495	65	C11M	-4593	-495	115	C31P	-1593	-495
16	VGL	-7533	-495	66	C11M	-4533	-495	116	C31M	-1533	-495
17	VGL	-7473	-495	67	C11M	-4473	-495	117	C31M	-1473	-495
18	VGL	-7413	-495	68	C11M	-4413	-495	118	C31M	-1413	-495
19	VGL	-7353	-495	69	C11M	-4353	-495	119	C31M	-1353	-495
20	DUMMY<4>	-7293	-495	70	C11M	-4293	-495	120	C31M	-1293	-495
21	C22P	-7233	-495	71	C11M	-4233	-495	121	C31M	-1233	-495
22	C22P	-7173	-495	72	VSSC	-4173	-495	122	C31M	-1173	-495
23	C22P	-7113	-495	73	VSSC	-4113	-495	123	C31M	-1113	-495
24	DUMMY<5>	-7053	-495	74	VSSC	-4053	-495	124	VCL	-1053	-495
25	C22M	-6993	-495	75	VSSC	-3993	-495	125	VCL	-993	-495
26	C22M	-6933	-495	76	VSSC	-3933	-495	126	VCL	-933	-495
27	C22M	-6873	-495	77	VSSC	-3873	-495	127	VCL	-873	-495
28	DUMMY<6>	-6813	-495	78	VSSC	-3813	-495	128	VCL	-813	-495
29	C21P	-6753	-495	79	VSSC	-3753	-495	129	VCL	-753	-495
30	C21P	-6693	-495	80	VSSC	-3693	-495	130	VCL	-693	-495
31	C21P	-6633	-495	81	VSSC	-3633	-495	131	VCL	-633	-495
32	DUMMY<7>	-6573	-495	82	C12P	-3573	-495	132	DUMMY<10>	-573	-495
33	C21M	-6513	-495	83	C12P	-3513	-495	133	DCX	-513	-495
34	C21M	-6453	-495	84	C12P	-3453	-495	134	CSX	-453	-495
35	C21M	-6393	-495	85	C12P	-3393	-495	135	VSYNC	-393	-495
36	DUMMY<8>	-6333	-495	86	C12P	-3333	-495	136	HSYNC	-333	-495
37	DUMMY<9>	-6273	-495	87	C12P	-3273	-495	137	DOTCLK	-273	-495
38	VCI1	-6213	-495	88	C12P	-3213	-495	138	ENABLE	-213	-495
39	VCI1	-6153	-495	89	C12P	-3153	-495	139	RESX	-153	-495
40	VCI1	-6093	-495	90	C12M	-3093	-495	140	RDX	-93	-495
41	VCI1	-6033	-495	91	C12M	-3033	-495	141	WRX	-33	-495
42	VCI1	-5973	-495	92	C12M	-2973	-495	142	IM<3>	27	-495
43	VCI1	-5913	-495	93	C12M	-2913	-495	143	IM<2>	87	-495
44	VCI1	-5853	-495	94	C12M	-2853	-495	144	IM<1>	147	-495
45	VCI1	-5793	-495	95	C12M	-2793	-495	145	IM<0>	207	-495
46	VCI	-5733	-495	96	C12M	-2733	-495	146	SDA	267	-495
47	VCI	-5673	-495	97	C12M	-2673	-495	147	DB<23>	352	-495
48	VCI	-5613	-495	98	AVDD	-2613	-495	148	DB<22>	437	-495
49	VCI	-5553	-495	99	AVDD	-2553	-495	149	DB<21>	522	-495
50	VCI	-5493	-495	100	AVDD	-2493	-495	150	DB<20>	607	-495

Note. Dummy<1> pin shows ground potential during power-on status.



Table 185. Pad center coordinates [Unit:  $\mu\text{m}$ ]

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
151	DB<19>	692	-495	201	AVSS	4292	-495	251	VCOMH	7292	-495
152	DB<18>	777	-495	202	AVSS	4352	-495	252	VCOMH	7352	-495
153	DB<17>	862	-495	203	AVSS	4412	-495	253	VCOMH	7412	-495
154	DB<16>	947	-495	204	VSS	4472	-495	254	VCOMH	7472	-495
155	DB<15>	1032	-495	205	VSS	4532	-495	255	VCOML	7532	-495
156	DB<14>	1117	-495	206	VSS	4592	-495	256	VCOML	7592	-495
157	DB<13>	1202	-495	207	VSS	4652	-495	257	VCOML	7652	-495
158	DB<12>	1287	-495	208	VSS	4712	-495	258	VCOML	7712	-495
159	DB<11>	1372	-495	209	VSS	4772	-495	259	VCOML	7772	-495
160	DB<10>	1457	-495	210	VSS	4832	-495	260	DUMMY<12>	7832	-495
161	DB<9>	1542	-495	211	VSS	4892	-495	261	CONTACT1_GND	7892	-495
162	DB<8>	1627	-495	212	VSS	4952	-495	262	CONTACT2_GND	7952	-495
163	DB<7>	1712	-495	213	VSS	5012	-495	263	DUMMY<13>	8012	-495
164	DB<6>	1797	-495	214	VSS3	5072	-495	264	VCOM	8072	-495
165	DB<5>	1882	-495	215	VSS3	5132	-495	265	VCOM	8132	-495
166	DB<4>	1967	-495	216	VSS3	5192	-495	266	VCOM	8192	-495
167	DB<3>	2052	-495	217	VSS3	5252	-495	267	VCOM	8252	-495
168	DB<2>	2137	-495	218	VSS3	5312	-495	268	VCOM	8312	-495
169	DB<1>	2222	-495	219	VSS3	5372	-495	269	VCOM	8372	-495
170	DB<0>	2307	-495	220	VSS3	5432	-495	270	DUMMY<14> GND	8432	-495
171	BC	2392	-495	221	VSS3	5492	-495	271	DUMMY<15>	8504	338
172	BC_CTL	2477	-495	222	VREF	5552	-495	272	DUMMY<16>	8488	473
173	TE	2562	-495	223	VREF	5612	-495	273	DUMMY<17>	8472	338
174	CL1	2647	-495	224	VDD3	5672	-495	274	DUMMY<18>	8456	473
175	TMODE<2>	2732	-495	225	VDD3	5732	-495	275	G<2>	8440	338
176	TMODE<1>	2792	-495	226	VDD3	5792	-495	276	G<4>	8424	473
177	TMODE<0>	2852	-495	227	VDD3	5852	-495	277	G<6>	8408	338
178	TMUX<2>	2912	-495	228	VDD3	5912	-495	278	G<8>	8392	473
179	TMUX<1>	2972	-495	229	VDD3	5972	-495	279	G<10>	8376	338
180	TMUX<0>	3032	-495	230	VDD3	6032	-495	280	G<12>	8360	473
181	TEST_XA	3092	-495	231	VDD3	6092	-495	281	G<14>	8344	338
182	TEST_YA<1>	3152	-495	232	VDD	6152	-495	282	G<16>	8328	473
183	TEST_YA<0>	3212	-495	233	VDD	6212	-495	283	G<18>	8312	338
184	EN_EXCLK	3272	-495	234	VDD	6272	-495	284	G<20>	8296	473
185	EXCLK	3332	-495	235	VDD	6332	-495	285	G<22>	8280	338
186	TREGB	3392	-495	236	VDD	6392	-495	286	G<24>	8264	473
187	VGS	3452	-495	237	VDD	6452	-495	287	G<26>	8248	338
188	VGS	3512	-495	238	VDD	6512	-495	288	G<28>	8232	473
189	AVSS	3572	-495	239	VDD	6572	-495	289	G<30>	8216	338
190	AVSS	3632	-495	240	VDD	6632	-495	290	G<32>	8200	473
191	AVSS	3692	-495	241	VDD	6692	-495	291	G<34>	8184	338
192	AVSS	3752	-495	242	VDD	6752	-495	292	G<36>	8168	473
193	AVSS	3812	-495	243	VDD	6812	-495	293	G<38>	8152	338
194	AVSS	3872	-495	244	DUMMY<11>	6872	-495	294	G<40>	8136	473
195	AVSS	3932	-495	245	GVDD	6932	-495	295	G<42>	8120	338
196	AVSS	3992	-495	246	GVDD	6992	-495	296	G<44>	8104	473
197	AVSS	4052	-495	247	GVDD	7052	-495	297	G<46>	8088	338
198	AVSS	4112	-495	248	GVDD	7112	-495	298	G<48>	8072	473
199	AVSS	4172	-495	249	GVDD	7172	-495	299	G<50>	8056	338
200	AVSS	4232	-495	250	VCOMH	7232	-495	300	G<52>	8040	473

Note. Contact1, Contact2 and Dummy<14> pins show ground potential during power-on status.

Table 186. Pad center coordinates [Unit:  $\mu\text{m}$ ]

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
301	G<54>	8024	338	351	G<154>	7224	338	401	G<254>	6424	338
302	G<56>	8008	473	352	G<156>	7208	473	402	G<256>	6408	473
303	G<58>	7992	338	353	G<158>	7192	338	403	G<258>	6392	338
304	G<60>	7976	473	354	G<160>	7176	473	404	G<260>	6376	473
305	G<62>	7960	338	355	G<162>	7160	338	405	G<262>	6360	338
306	G<64>	7944	473	356	G<164>	7144	473	406	G<264>	6344	473
307	G<66>	7928	338	357	G<166>	7128	338	407	G<266>	6328	338
308	G<68>	7912	473	358	G<168>	7112	473	408	G<268>	6312	473
309	G<70>	7896	338	359	G<170>	7096	338	409	G<270>	6296	338
310	G<72>	7880	473	360	G<172>	7080	473	410	G<272>	6280	473
311	G<74>	7864	338	361	G<174>	7064	338	411	G<274>	6264	338
312	G<76>	7848	473	362	G<176>	7048	473	412	G<276>	6248	473
313	G<78>	7832	338	363	G<178>	7032	338	413	G<278>	6232	338
314	G<80>	7816	473	364	G<180>	7016	473	414	G<280>	6216	473
315	G<82>	7800	338	365	G<182>	7000	338	415	G<282>	6200	338
316	G<84>	7784	473	366	G<184>	6984	473	416	G<284>	6184	473
317	G<86>	7768	338	367	G<186>	6968	338	417	G<286>	6168	338
318	G<88>	7752	473	368	G<188>	6952	473	418	G<288>	6152	473
319	G<90>	7736	338	369	G<190>	6936	338	419	G<290>	6136	338
320	G<92>	7720	473	370	G<192>	6920	473	420	G<292>	6120	473
321	G<94>	7704	338	371	G<194>	6904	338	421	G<294>	6104	338
322	G<96>	7688	473	372	G<196>	6888	473	422	G<296>	6088	473
323	G<98>	7672	338	373	G<198>	6872	338	423	G<298>	6072	338
324	G<100>	7656	473	374	G<200>	6856	473	424	G<300>	6056	473
325	G<102>	7640	338	375	G<202>	6840	338	425	G<302>	6040	338
326	G<104>	7624	473	376	G<204>	6824	473	426	G<304>	6024	473
327	G<106>	7608	338	377	G<206>	6808	338	427	G<306>	6008	338
328	G<108>	7592	473	378	G<208>	6792	473	428	G<308>	5992	473
329	G<110>	7576	338	379	G<210>	6776	338	429	G<310>	5976	338
330	G<112>	7560	473	380	G<212>	6760	473	430	G<312>	5960	473
331	G<114>	7544	338	381	G<214>	6744	338	431	G<314>	5944	338
332	G<116>	7528	473	382	G<216>	6728	473	432	G<316>	5928	473
333	G<118>	7512	338	383	G<218>	6712	338	433	G<318>	5912	338
334	G<120>	7496	473	384	G<220>	6696	473	434	G<320>	5896	473
335	G<122>	7480	338	385	G<222>	6680	338	435	DUMMY<19> VGL	5880	338
336	G<124>	7464	473	386	G<224>	6664	473	436	DUMMY<20> VGL	5864	473
337	G<126>	7448	338	387	G<226>	6648	338	437	DUMMY<21>	5848	338
338	G<128>	7432	473	388	G<228>	6632	473	438	DUMMY<22>	5832	473
339	G<130>	7416	338	389	G<230>	6616	338	439	DUMMY<23>	5816	338
340	G<132>	7400	473	390	G<232>	6600	473	440	DUMMY<24>	5800	473
341	G<134>	7384	338	391	G<234>	6584	338	441	DUMMY<25>	5784	338
342	G<136>	7368	473	392	G<236>	6568	473	442	DUMMY<26>	5768	473
343	G<138>	7352	338	393	G<238>	6552	338	443	SOUT<720>	5752	338
344	G<140>	7336	473	394	G<240>	6536	473	444	SOUT<719>	5736	473
345	G<142>	7320	338	395	G<242>	6520	338	445	SOUT<718>	5720	338
346	G<144>	7304	473	396	G<244>	6504	473	446	SOUT<717>	5704	473
347	G<146>	7288	338	397	G<246>	6488	338	447	SOUT<716>	5688	338
348	G<148>	7272	473	398	G<248>	6472	473	448	SOUT<715>	5672	473
349	G<150>	7256	338	399	G<250>	6456	338	449	SOUT<714>	5656	338
350	G<152>	7240	473	400	G<252>	6440	473	450	SOUT<713>	5640	473

Note. Dummy<19> and Dummy<20> pins show VGL potential during normal operating condition.

Table 187. Pad center coordinates [Unit:  $\mu\text{m}$ ]

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
451	SOUT<712>	5624	338	501	SOUT<662>	4824	338	551	SOUT<612>	4024	338
452	SOUT<711>	5608	473	502	SOUT<661>	4808	473	552	SOUT<611>	4008	473
453	SOUT<710>	5592	338	503	SOUT<660>	4792	338	553	SOUT<610>	3992	338
454	SOUT<709>	5576	473	504	SOUT<659>	4776	473	554	SOUT<609>	3976	473
455	SOUT<708>	5560	338	505	SOUT<658>	4760	338	555	SOUT<608>	3960	338
456	SOUT<707>	5544	473	506	SOUT<657>	4744	473	556	SOUT<607>	3944	473
457	SOUT<706>	5528	338	507	SOUT<656>	4728	338	557	SOUT<606>	3928	338
458	SOUT<705>	5512	473	508	SOUT<655>	4712	473	558	SOUT<605>	3912	473
459	SOUT<704>	5496	338	509	SOUT<654>	4696	338	559	SOUT<604>	3896	338
460	SOUT<703>	5480	473	510	SOUT<653>	4680	473	560	SOUT<603>	3880	473
461	SOUT<702>	5464	338	511	SOUT<652>	4664	338	561	SOUT<602>	3864	338
462	SOUT<701>	5448	473	512	SOUT<651>	4648	473	562	SOUT<601>	3848	473
463	SOUT<700>	5432	338	513	SOUT<650>	4632	338	563	SOUT<600>	3832	338
464	SOUT<699>	5416	473	514	SOUT<649>	4616	473	564	SOUT<599>	3816	473
465	SOUT<698>	5400	338	515	SOUT<648>	4600	338	565	SOUT<598>	3800	338
466	SOUT<697>	5384	473	516	SOUT<647>	4584	473	566	SOUT<597>	3784	473
467	SOUT<696>	5368	338	517	SOUT<646>	4568	338	567	SOUT<596>	3768	338
468	SOUT<695>	5352	473	518	SOUT<645>	4552	473	568	SOUT<595>	3752	473
469	SOUT<694>	5336	338	519	SOUT<644>	4536	338	569	SOUT<594>	3736	338
470	SOUT<693>	5320	473	520	SOUT<643>	4520	473	570	SOUT<593>	3720	473
471	SOUT<692>	5304	338	521	SOUT<642>	4504	338	571	SOUT<592>	3704	338
472	SOUT<691>	5288	473	522	SOUT<641>	4488	473	572	SOUT<591>	3688	473
473	SOUT<690>	5272	338	523	SOUT<640>	4472	338	573	SOUT<590>	3672	338
474	SOUT<689>	5256	473	524	SOUT<639>	4456	473	574	SOUT<589>	3656	473
475	SOUT<688>	5240	338	525	SOUT<638>	4440	338	575	SOUT<588>	3640	338
476	SOUT<687>	5224	473	526	SOUT<637>	4424	473	576	SOUT<587>	3624	473
477	SOUT<686>	5208	338	527	SOUT<636>	4408	338	577	SOUT<586>	3608	338
478	SOUT<685>	5192	473	528	SOUT<635>	4392	473	578	SOUT<585>	3592	473
479	SOUT<684>	5176	338	529	SOUT<634>	4376	338	579	SOUT<584>	3576	338
480	SOUT<683>	5160	473	530	SOUT<633>	4360	473	580	SOUT<583>	3560	473
481	SOUT<682>	5144	338	531	SOUT<632>	4344	338	581	SOUT<582>	3544	338
482	SOUT<681>	5128	473	532	SOUT<631>	4328	473	582	SOUT<581>	3528	473
483	SOUT<680>	5112	338	533	SOUT<630>	4312	338	583	SOUT<580>	3512	338
484	SOUT<679>	5096	473	534	SOUT<629>	4296	473	584	SOUT<579>	3496	473
485	SOUT<678>	5080	338	535	SOUT<628>	4280	338	585	SOUT<578>	3480	338
486	SOUT<677>	5064	473	536	SOUT<627>	4264	473	586	SOUT<577>	3464	473
487	SOUT<676>	5048	338	537	SOUT<626>	4248	338	587	SOUT<576>	3448	338
488	SOUT<675>	5032	473	538	SOUT<625>	4232	473	588	SOUT<575>	3432	473
489	SOUT<674>	5016	338	539	SOUT<624>	4216	338	589	SOUT<574>	3416	338
490	SOUT<673>	5000	473	540	SOUT<623>	4200	473	590	SOUT<573>	3400	473
491	SOUT<672>	4984	338	541	SOUT<622>	4184	338	591	SOUT<572>	3384	338
492	SOUT<671>	4968	473	542	SOUT<621>	4168	473	592	SOUT<571>	3368	473
493	SOUT<670>	4952	338	543	SOUT<620>	4152	338	593	SOUT<570>	3352	338
494	SOUT<669>	4936	473	544	SOUT<619>	4136	473	594	SOUT<569>	3336	473
495	SOUT<668>	4920	338	545	SOUT<618>	4120	338	595	SOUT<568>	3320	338
496	SOUT<667>	4904	473	546	SOUT<617>	4104	473	596	SOUT<567>	3304	473
497	SOUT<666>	4888	338	547	SOUT<616>	4088	338	597	SOUT<566>	3288	338
498	SOUT<665>	4872	473	548	SOUT<615>	4072	473	598	SOUT<565>	3272	473
499	SOUT<664>	4856	338	549	SOUT<614>	4056	338	599	SOUT<564>	3256	338
500	SOUT<663>	4840	473	550	SOUT<613>	4040	473	600	SOUT<563>	3240	473



Table 188. Pad center coordinates [Unit:  $\mu\text{m}$ ]

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
601	SOUT<562>	3224	338	651	SOUT<512>	2424	338	701	SOUT<462>	1624	338
602	SOUT<561>	3208	473	652	SOUT<511>	2408	473	702	SOUT<461>	1608	473
603	SOUT<560>	3192	338	653	SOUT<510>	2392	338	703	SOUT<460>	1592	338
604	SOUT<559>	3176	473	654	SOUT<509>	2376	473	704	SOUT<459>	1576	473
605	SOUT<558>	3160	338	655	SOUT<508>	2360	338	705	SOUT<458>	1560	338
606	SOUT<557>	3144	473	656	SOUT<507>	2344	473	706	SOUT<457>	1544	473
607	SOUT<556>	3128	338	657	SOUT<506>	2328	338	707	SOUT<456>	1528	338
608	SOUT<555>	3112	473	658	SOUT<505>	2312	473	708	SOUT<455>	1512	473
609	SOUT<554>	3096	338	659	SOUT<504>	2296	338	709	SOUT<454>	1496	338
610	SOUT<553>	3080	473	660	SOUT<503>	2280	473	710	SOUT<453>	1480	473
611	SOUT<552>	3064	338	661	SOUT<502>	2264	338	711	SOUT<452>	1464	338
612	SOUT<551>	3048	473	662	SOUT<501>	2248	473	712	SOUT<451>	1448	473
613	SOUT<550>	3032	338	663	SOUT<500>	2232	338	713	SOUT<450>	1432	338
614	SOUT<549>	3016	473	664	SOUT<499>	2216	473	714	SOUT<449>	1416	473
615	SOUT<548>	3000	338	665	SOUT<498>	2200	338	715	SOUT<448>	1400	338
616	SOUT<547>	2984	473	666	SOUT<497>	2184	473	716	SOUT<447>	1384	473
617	SOUT<546>	2968	338	667	SOUT<496>	2168	338	717	SOUT<446>	1368	338
618	SOUT<545>	2952	473	668	SOUT<495>	2152	473	718	SOUT<445>	1352	473
619	SOUT<544>	2936	338	669	SOUT<494>	2136	338	719	SOUT<444>	1336	338
620	SOUT<543>	2920	473	670	SOUT<493>	2120	473	720	SOUT<443>	1320	473
621	SOUT<542>	2904	338	671	SOUT<492>	2104	338	721	SOUT<442>	1304	338
622	SOUT<541>	2888	473	672	SOUT<491>	2088	473	722	SOUT<441>	1288	473
623	SOUT<540>	2872	338	673	SOUT<490>	2072	338	723	SOUT<440>	1272	338
624	SOUT<539>	2856	473	674	SOUT<489>	2056	473	724	SOUT<439>	1256	473
625	SOUT<538>	2840	338	675	SOUT<488>	2040	338	725	SOUT<438>	1240	338
626	SOUT<537>	2824	473	676	SOUT<487>	2024	473	726	SOUT<437>	1224	473
627	SOUT<536>	2808	338	677	SOUT<486>	2008	338	727	SOUT<436>	1208	338
628	SOUT<535>	2792	473	678	SOUT<485>	1992	473	728	SOUT<435>	1192	473
629	SOUT<534>	2776	338	679	SOUT<484>	1976	338	729	SOUT<434>	1176	338
630	SOUT<533>	2760	473	680	SOUT<483>	1960	473	730	SOUT<433>	1160	473
631	SOUT<532>	2744	338	681	SOUT<482>	1944	338	731	SOUT<432>	1144	338
632	SOUT<531>	2728	473	682	SOUT<481>	1928	473	732	SOUT<431>	1128	473
633	SOUT<530>	2712	338	683	SOUT<480>	1912	338	733	SOUT<430>	1112	338
634	SOUT<529>	2696	473	684	SOUT<479>	1896	473	734	SOUT<429>	1096	473
635	SOUT<528>	2680	338	685	SOUT<478>	1880	338	735	SOUT<428>	1080	338
636	SOUT<527>	2664	473	686	SOUT<477>	1864	473	736	SOUT<427>	1064	473
637	SOUT<526>	2648	338	687	SOUT<476>	1848	338	737	SOUT<426>	1048	338
638	SOUT<525>	2632	473	688	SOUT<475>	1832	473	738	SOUT<425>	1032	473
639	SOUT<524>	2616	338	689	SOUT<474>	1816	338	739	SOUT<424>	1016	338
640	SOUT<523>	2600	473	690	SOUT<473>	1800	473	740	SOUT<423>	1000	473
641	SOUT<522>	2584	338	691	SOUT<472>	1784	338	741	SOUT<422>	984	338
642	SOUT<521>	2568	473	692	SOUT<471>	1768	473	742	SOUT<421>	968	473
643	SOUT<520>	2552	338	693	SOUT<470>	1752	338	743	SOUT<420>	952	338
644	SOUT<519>	2536	473	694	SOUT<469>	1736	473	744	SOUT<419>	936	473
645	SOUT<518>	2520	338	695	SOUT<468>	1720	338	745	SOUT<418>	920	338
646	SOUT<517>	2504	473	696	SOUT<467>	1704	473	746	SOUT<417>	904	473
647	SOUT<516>	2488	338	697	SOUT<466>	1688	338	747	SOUT<416>	888	338
648	SOUT<515>	2472	473	698	SOUT<465>	1672	473	748	SOUT<415>	872	473
649	SOUT<514>	2456	338	699	SOUT<464>	1656	338	749	SOUT<414>	856	338
650	SOUT<513>	2440	473	700	SOUT<463>	1640	473	750	SOUT<413>	840	473



Table 189. Pad center coordinates [Unit:  $\mu\text{m}$ ]

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
751	SOUT<412>	824	338	801	SOUT<362>	24	338	851	SOUT<312>	-776	338
752	SOUT<411>	808	473	802	SOUT<361>	8	473	852	SOUT<311>	-792	473
753	SOUT<410>	792	338	803	SOUT<360>	-8	338	853	SOUT<310>	-808	338
754	SOUT<409>	776	473	804	SOUT<359>	-24	473	854	SOUT<309>	-824	473
755	SOUT<408>	760	338	805	SOUT<358>	-40	338	855	SOUT<308>	-840	338
756	SOUT<407>	744	473	806	SOUT<357>	-56	473	856	SOUT<307>	-856	473
757	SOUT<406>	728	338	807	SOUT<356>	-72	338	857	SOUT<306>	-872	338
758	SOUT<405>	712	473	808	SOUT<355>	-88	473	858	SOUT<305>	-888	473
759	SOUT<404>	696	338	809	SOUT<354>	-104	338	859	SOUT<304>	-904	338
760	SOUT<403>	680	473	810	SOUT<353>	-120	473	860	SOUT<303>	-920	473
761	SOUT<402>	664	338	811	SOUT<352>	-136	338	861	SOUT<302>	-936	338
762	SOUT<401>	648	473	812	SOUT<351>	-152	473	862	SOUT<301>	-952	473
763	SOUT<400>	632	338	813	SOUT<350>	-168	338	863	SOUT<300>	-968	338
764	SOUT<399>	616	473	814	SOUT<349>	-184	473	864	SOUT<299>	-984	473
765	SOUT<398>	600	338	815	SOUT<348>	-200	338	865	SOUT<298>	-1000	338
766	SOUT<397>	584	473	816	SOUT<347>	-216	473	866	SOUT<297>	-1016	473
767	SOUT<396>	568	338	817	SOUT<346>	-232	338	867	SOUT<296>	-1032	338
768	SOUT<395>	552	473	818	SOUT<345>	-248	473	868	SOUT<295>	-1048	473
769	SOUT<394>	536	338	819	SOUT<344>	-264	338	869	SOUT<294>	-1064	338
770	SOUT<393>	520	473	820	SOUT<343>	-280	473	870	SOUT<293>	-1080	473
771	SOUT<392>	504	338	821	SOUT<342>	-296	338	871	SOUT<292>	-1096	338
772	SOUT<391>	488	473	822	SOUT<341>	-312	473	872	SOUT<291>	-1112	473
773	SOUT<390>	472	338	823	SOUT<340>	-328	338	873	SOUT<290>	-1128	338
774	SOUT<389>	456	473	824	SOUT<339>	-344	473	874	SOUT<289>	-1144	473
775	SOUT<388>	440	338	825	SOUT<338>	-360	338	875	SOUT<288>	-1160	338
776	SOUT<387>	424	473	826	SOUT<337>	-376	473	876	SOUT<287>	-1176	473
777	SOUT<386>	408	338	827	SOUT<336>	-392	338	877	SOUT<286>	-1192	338
778	SOUT<385>	392	473	828	SOUT<335>	-408	473	878	SOUT<285>	-1208	473
779	SOUT<384>	376	338	829	SOUT<334>	-424	338	879	SOUT<284>	-1224	338
780	SOUT<383>	360	473	830	SOUT<333>	-440	473	880	SOUT<283>	-1240	473
781	SOUT<382>	344	338	831	SOUT<332>	-456	338	881	SOUT<282>	-1256	338
782	SOUT<381>	328	473	832	SOUT<331>	-472	473	882	SOUT<281>	-1272	473
783	SOUT<380>	312	338	833	SOUT<330>	-488	338	883	SOUT<280>	-1288	338
784	SOUT<379>	296	473	834	SOUT<329>	-504	473	884	SOUT<279>	-1304	473
785	SOUT<378>	280	338	835	SOUT<328>	-520	338	885	SOUT<278>	-1320	338
786	SOUT<377>	264	473	836	SOUT<327>	-536	473	886	SOUT<277>	-1336	473
787	SOUT<376>	248	338	837	SOUT<326>	-552	338	887	SOUT<276>	-1352	338
788	SOUT<375>	232	473	838	SOUT<325>	-568	473	888	SOUT<275>	-1368	473
789	SOUT<374>	216	338	839	SOUT<324>	-584	338	889	SOUT<274>	-1384	338
790	SOUT<373>	200	473	840	SOUT<323>	-600	473	890	SOUT<273>	-1400	473
791	SOUT<372>	184	338	841	SOUT<322>	-616	338	891	SOUT<272>	-1416	338
792	SOUT<371>	168	473	842	SOUT<321>	-632	473	892	SOUT<271>	-1432	473
793	SOUT<370>	152	338	843	SOUT<320>	-648	338	893	SOUT<270>	-1448	338
794	SOUT<369>	136	473	844	SOUT<319>	-664	473	894	SOUT<269>	-1464	473
795	SOUT<368>	120	338	845	SOUT<318>	-680	338	895	SOUT<268>	-1480	338
796	SOUT<367>	104	473	846	SOUT<317>	-696	473	896	SOUT<267>	-1496	473
797	SOUT<366>	88	338	847	SOUT<316>	-712	338	897	SOUT<266>	-1512	338
798	SOUT<365>	72	473	848	SOUT<315>	-728	473	898	SOUT<265>	-1528	473
799	SOUT<364>	56	338	849	SOUT<314>	-744	338	899	SOUT<264>	-1544	338
800	SOUT<363>	40	473	850	SOUT<313>	-760	473	900	SOUT<263>	-1560	473



Table 190. Pad center coordinates [Unit:  $\mu\text{m}$ ]

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
901	SOUT<262>	-1576	338	951	SOUT<212>	-2376	338	1001	SOUT<162>	-3176	338
902	SOUT<261>	-1592	473	952	SOUT<211>	-2392	473	1002	SOUT<161>	-3192	473
903	SOUT<260>	-1608	338	953	SOUT<210>	-2408	338	1003	SOUT<160>	-3208	338
904	SOUT<259>	-1624	473	954	SOUT<209>	-2424	473	1004	SOUT<159>	-3224	473
905	SOUT<258>	-1640	338	955	SOUT<208>	-2440	338	1005	SOUT<158>	-3240	338
906	SOUT<257>	-1656	473	956	SOUT<207>	-2456	473	1006	SOUT<157>	-3256	473
907	SOUT<256>	-1672	338	957	SOUT<206>	-2472	338	1007	SOUT<156>	-3272	338
908	SOUT<255>	-1688	473	958	SOUT<205>	-2488	473	1008	SOUT<155>	-3288	473
909	SOUT<254>	-1704	338	959	SOUT<204>	-2504	338	1009	SOUT<154>	-3304	338
910	SOUT<253>	-1720	473	960	SOUT<203>	-2520	473	1010	SOUT<153>	-3320	473
911	SOUT<252>	-1736	338	961	SOUT<202>	-2536	338	1011	SOUT<152>	-3336	338
912	SOUT<251>	-1752	473	962	SOUT<201>	-2552	473	1012	SOUT<151>	-3352	473
913	SOUT<250>	-1768	338	963	SOUT<200>	-2568	338	1013	SOUT<150>	-3368	338
914	SOUT<249>	-1784	473	964	SOUT<199>	-2584	473	1014	SOUT<149>	-3384	473
915	SOUT<248>	-1800	338	965	SOUT<198>	-2600	338	1015	SOUT<148>	-3400	338
916	SOUT<247>	-1816	473	966	SOUT<197>	-2616	473	1016	SOUT<147>	-3416	473
917	SOUT<246>	-1832	338	967	SOUT<196>	-2632	338	1017	SOUT<146>	-3432	338
918	SOUT<245>	-1848	473	968	SOUT<195>	-2648	473	1018	SOUT<145>	-3448	473
919	SOUT<244>	-1864	338	969	SOUT<194>	-2664	338	1019	SOUT<144>	-3464	338
920	SOUT<243>	-1880	473	970	SOUT<193>	-2680	473	1020	SOUT<143>	-3480	473
921	SOUT<242>	-1896	338	971	SOUT<192>	-2696	338	1021	SOUT<142>	-3496	338
922	SOUT<241>	-1912	473	972	SOUT<191>	-2712	473	1022	SOUT<141>	-3512	473
923	SOUT<240>	-1928	338	973	SOUT<190>	-2728	338	1023	SOUT<140>	-3528	338
924	SOUT<239>	-1944	473	974	SOUT<189>	-2744	473	1024	SOUT<139>	-3544	473
925	SOUT<238>	-1960	338	975	SOUT<188>	-2760	338	1025	SOUT<138>	-3560	338
926	SOUT<237>	-1976	473	976	SOUT<187>	-2776	473	1026	SOUT<137>	-3576	473
927	SOUT<236>	-1992	338	977	SOUT<186>	-2792	338	1027	SOUT<136>	-3592	338
928	SOUT<235>	-2008	473	978	SOUT<185>	-2808	473	1028	SOUT<135>	-3608	473
929	SOUT<234>	-2024	338	979	SOUT<184>	-2824	338	1029	SOUT<134>	-3624	338
930	SOUT<233>	-2040	473	980	SOUT<183>	-2840	473	1030	SOUT<133>	-3640	473
931	SOUT<232>	-2056	338	981	SOUT<182>	-2856	338	1031	SOUT<132>	-3656	338
932	SOUT<231>	-2072	473	982	SOUT<181>	-2872	473	1032	SOUT<131>	-3672	473
933	SOUT<230>	-2088	338	983	SOUT<180>	-2888	338	1033	SOUT<130>	-3688	338
934	SOUT<229>	-2104	473	984	SOUT<179>	-2904	473	1034	SOUT<129>	-3704	473
935	SOUT<228>	-2120	338	985	SOUT<178>	-2920	338	1035	SOUT<128>	-3720	338
936	SOUT<227>	-2136	473	986	SOUT<177>	-2936	473	1036	SOUT<127>	-3736	473
937	SOUT<226>	-2152	338	987	SOUT<176>	-2952	338	1037	SOUT<126>	-3752	338
938	SOUT<225>	-2168	473	988	SOUT<175>	-2968	473	1038	SOUT<125>	-3768	473
939	SOUT<224>	-2184	338	989	SOUT<174>	-2984	338	1039	SOUT<124>	-3784	338
940	SOUT<223>	-2200	473	990	SOUT<173>	-3000	473	1040	SOUT<123>	-3800	473
941	SOUT<222>	-2216	338	991	SOUT<172>	-3016	338	1041	SOUT<122>	-3816	338
942	SOUT<221>	-2232	473	992	SOUT<171>	-3032	473	1042	SOUT<121>	-3832	473
943	SOUT<220>	-2248	338	993	SOUT<170>	-3048	338	1043	SOUT<120>	-3848	338
944	SOUT<219>	-2264	473	994	SOUT<169>	-3064	473	1044	SOUT<119>	-3864	473
945	SOUT<218>	-2280	338	995	SOUT<168>	-3080	338	1045	SOUT<118>	-3880	338
946	SOUT<217>	-2296	473	996	SOUT<167>	-3096	473	1046	SOUT<117>	-3896	473
947	SOUT<216>	-2312	338	997	SOUT<166>	-3112	338	1047	SOUT<116>	-3912	338
948	SOUT<215>	-2328	473	998	SOUT<165>	-3128	473	1048	SOUT<115>	-3928	473
949	SOUT<214>	-2344	338	999	SOUT<164>	-3144	338	1049	SOUT<114>	-3944	338
950	SOUT<213>	-2360	473	1000	SOUT<163>	-3160	473	1050	SOUT<113>	-3960	473



Table 191. Pad center coordinates [Unit:  $\mu\text{m}$ ]

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
1051	SOUT<112>	-3976	338	1101	SOUT<62>	-4776	338	1151	SOUT<12>	-5576	338
1052	SOUT<111>	-3992	473	1102	SOUT<61>	-4792	473	1152	SOUT<11>	-5592	473
1053	SOUT<110>	-4008	338	1103	SOUT<60>	-4808	338	1153	SOUT<10>	-5608	338
1054	SOUT<109>	-4024	473	1104	SOUT<59>	-4824	473	1154	SOUT<9>	-5624	473
1055	SOUT<108>	-4040	338	1105	SOUT<58>	-4840	338	1155	SOUT<8>	-5640	338
1056	SOUT<107>	-4056	473	1106	SOUT<57>	-4856	473	1156	SOUT<7>	-5656	473
1057	SOUT<106>	-4072	338	1107	SOUT<56>	-4872	338	1157	SOUT<6>	-5672	338
1058	SOUT<105>	-4088	473	1108	SOUT<55>	-4888	473	1158	SOUT<5>	-5688	473
1059	SOUT<104>	-4104	338	1109	SOUT<54>	-4904	338	1159	SOUT<4>	-5704	338
1060	SOUT<103>	-4120	473	1110	SOUT<53>	-4920	473	1160	SOUT<3>	-5720	473
1061	SOUT<102>	-4136	338	1111	SOUT<52>	-4936	338	1161	SOUT<2>	-5736	338
1062	SOUT<101>	-4152	473	1112	SOUT<51>	-4952	473	1162	SOUT<1>	-5752	473
1063	SOUT<100>	-4168	338	1113	SOUT<50>	-4968	338	1163	DUMMY<27>	-5768	338
1064	SOUT<99>	-4184	473	1114	SOUT<49>	-4984	473	1164	DUMMY<28>	-5784	473
1065	SOUT<98>	-4200	338	1115	SOUT<48>	-5000	338	1165	DUMMY<29>	-5800	338
1066	SOUT<97>	-4216	473	1116	SOUT<47>	-5016	473	1166	DUMMY<30>	-5816	473
1067	SOUT<96>	-4232	338	1117	SOUT<46>	-5032	338	1167	DUMMY<31>	-5832	338
1068	SOUT<95>	-4248	473	1118	SOUT<45>	-5048	473	1168	DUMMY<32>	-5848	473
1069	SOUT<94>	-4264	338	1119	SOUT<44>	-5064	338	1169	DUMMY<33> VGL	-5864	338
1070	SOUT<93>	-4280	473	1120	SOUT<43>	-5080	473	1170	DUMMY<34> VGL	-5880	473
1071	SOUT<92>	-4296	338	1121	SOUT<42>	-5096	338	1171	G<319>	-5896	338
1072	SOUT<91>	-4312	473	1122	SOUT<41>	-5112	473	1172	G<317>	-5912	473
1073	SOUT<90>	-4328	338	1123	SOUT<40>	-5128	338	1173	G<315>	-5928	338
1074	SOUT<89>	-4344	473	1124	SOUT<39>	-5144	473	1174	G<313>	-5944	473
1075	SOUT<88>	-4360	338	1125	SOUT<38>	-5160	338	1175	G<311>	-5960	338
1076	SOUT<87>	-4376	473	1126	SOUT<37>	-5176	473	1176	G<309>	-5976	473
1077	SOUT<86>	-4392	338	1127	SOUT<36>	-5192	338	1177	G<307>	-5992	338
1078	SOUT<85>	-4408	473	1128	SOUT<35>	-5208	473	1178	G<305>	-6008	473
1079	SOUT<84>	-4424	338	1129	SOUT<34>	-5224	338	1179	G<303>	-6024	338
1080	SOUT<83>	-4440	473	1130	SOUT<33>	-5240	473	1180	G<301>	-6040	473
1081	SOUT<82>	-4456	338	1131	SOUT<32>	-5256	338	1181	G<299>	-6056	338
1082	SOUT<81>	-4472	473	1132	SOUT<31>	-5272	473	1182	G<297>	-6072	473
1083	SOUT<80>	-4488	338	1133	SOUT<30>	-5288	338	1183	G<295>	-6088	338
1084	SOUT<79>	-4504	473	1134	SOUT<29>	-5304	473	1184	G<293>	-6104	473
1085	SOUT<78>	-4520	338	1135	SOUT<28>	-5320	338	1185	G<291>	-6120	338
1086	SOUT<77>	-4536	473	1136	SOUT<27>	-5336	473	1186	G<289>	-6136	473
1087	SOUT<76>	-4552	338	1137	SOUT<26>	-5352	338	1187	G<287>	-6152	338
1088	SOUT<75>	-4568	473	1138	SOUT<25>	-5368	473	1188	G<285>	-6168	473
1089	SOUT<74>	-4584	338	1139	SOUT<24>	-5384	338	1189	G<283>	-6184	338
1090	SOUT<73>	-4600	473	1140	SOUT<23>	-5400	473	1190	G<281>	-6200	473
1091	SOUT<72>	-4616	338	1141	SOUT<22>	-5416	338	1191	G<279>	-6216	338
1092	SOUT<71>	-4632	473	1142	SOUT<21>	-5432	473	1192	G<277>	-6232	473
1093	SOUT<70>	-4648	338	1143	SOUT<20>	-5448	338	1193	G<275>	-6248	338
1094	SOUT<69>	-4664	473	1144	SOUT<19>	-5464	473	1194	G<273>	-6264	473
1095	SOUT<68>	-4680	338	1145	SOUT<18>	-5480	338	1195	G<271>	-6280	338
1096	SOUT<67>	-4696	473	1146	SOUT<17>	-5496	473	1196	G<269>	-6296	473
1097	SOUT<66>	-4712	338	1147	SOUT<16>	-5512	338	1197	G<267>	-6312	338
1098	SOUT<65>	-4728	473	1148	SOUT<15>	-5528	473	1198	G<265>	-6328	473
1099	SOUT<64>	-4744	338	1149	SOUT<14>	-5544	338	1199	G<263>	-6344	338
1100	SOUT<63>	-4760	473	1150	SOUT<13>	-5560	473	1200	G<261>	-6360	473

Note. Dummy<33> and Dummy<34> pins show VGL potential during normal operating condition.



Table 192. Pad center coordinates [Unit:  $\mu\text{m}$ ]

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
1201	G<259>	-6376	338	1251	G<159>	-7176	338	1301	G<59>	-7976	338
1202	G<257>	-6392	473	1252	G<157>	-7192	473	1302	G<57>	-7992	473
1203	G<255>	-6408	338	1253	G<155>	-7208	338	1303	G<55>	-8008	338
1204	G<253>	-6424	473	1254	G<153>	-7224	473	1304	G<53>	-8024	473
1205	G<251>	-6440	338	1255	G<151>	-7240	338	1305	G<51>	-8040	338
1206	G<249>	-6456	473	1256	G<149>	-7256	473	1306	G<49>	-8056	473
1207	G<247>	-6472	338	1257	G<147>	-7272	338	1307	G<47>	-8072	338
1208	G<245>	-6488	473	1258	G<145>	-7288	473	1308	G<45>	-8088	473
1209	G<243>	-6504	338	1259	G<143>	-7304	338	1309	G<43>	-8104	338
1210	G<241>	-6520	473	1260	G<141>	-7320	473	1310	G<41>	-8120	473
1211	G<239>	-6536	338	1261	G<139>	-7336	338	1311	G<39>	-8136	338
1212	G<237>	-6552	473	1262	G<137>	-7352	473	1312	G<37>	-8152	473
1213	G<235>	-6568	338	1263	G<135>	-7368	338	1313	G<35>	-8168	338
1214	G<233>	-6584	473	1264	G<133>	-7384	473	1314	G<33>	-8184	473
1215	G<231>	-6600	338	1265	G<131>	-7400	338	1315	G<31>	-8200	338
1216	G<229>	-6616	473	1266	G<129>	-7416	473	1316	G<29>	-8216	473
1217	G<227>	-6632	338	1267	G<127>	-7432	338	1317	G<27>	-8232	338
1218	G<225>	-6648	473	1268	G<125>	-7448	473	1318	G<25>	-8248	473
1219	G<223>	-6664	338	1269	G<123>	-7464	338	1319	G<23>	-8264	338
1220	G<221>	-6680	473	1270	G<121>	-7480	473	1320	G<21>	-8280	473
1221	G<219>	-6696	338	1271	G<119>	-7496	338	1321	G<19>	-8296	338
1222	G<217>	-6712	473	1272	G<117>	-7512	473	1322	G<17>	-8312	473
1223	G<215>	-6728	338	1273	G<115>	-7528	338	1323	G<15>	-8328	338
1224	G<213>	-6744	473	1274	G<113>	-7544	473	1324	G<13>	-8344	473
1225	G<211>	-6760	338	1275	G<111>	-7560	338	1325	G<11>	-8360	338
1226	G<209>	-6776	473	1276	G<109>	-7576	473	1326	G<9>	-8376	473
1227	G<207>	-6792	338	1277	G<107>	-7592	338	1327	G<7>	-8392	338
1228	G<205>	-6808	473	1278	G<105>	-7608	473	1328	G<5>	-8408	473
1229	G<203>	-6824	338	1279	G<103>	-7624	338	1329	G<3>	-8424	338
1230	G<201>	-6840	473	1280	G<101>	-7640	473	1330	G<1>	-8440	473
1231	G<199>	-6856	338	1281	G<99>	-7656	338	1331	DUMMY<35>	-8456	338
1232	G<197>	-6872	473	1282	G<97>	-7672	473	1332	DUMMY<36>	-8472	473
1233	G<195>	-6888	338	1283	G<95>	-7688	338	1333	DUMMY<37>	-8488	338
1234	G<193>	-6904	473	1284	G<93>	-7704	473	1334	DUMMY<38>	-8504	473
1235	G<191>	-6920	338	1285	G<91>	-7720	338				
1236	G<189>	-6936	473	1286	G<89>	-7736	473				
1237	G<187>	-6952	338	1287	G<87>	-7752	338				
1238	G<185>	-6968	473	1288	G<85>	-7768	473				
1239	G<183>	-6984	338	1289	G<83>	-7784	338				
1240	G<181>	-7000	473	1290	G<81>	-7800	473				
1241	G<179>	-7016	338	1291	G<79>	-7816	338				
1242	G<177>	-7032	473	1292	G<77>	-7832	473				
1243	G<175>	-7048	338	1293	G<75>	-7848	338				
1244	G<173>	-7064	473	1294	G<73>	-7864	473				
1245	G<171>	-7080	338	1295	G<71>	-7880	338				
1246	G<169>	-7096	473	1296	G<69>	-7896	473				
1247	G<167>	-7112	338	1297	G<67>	-7912	338				
1248	G<165>	-7128	473	1298	G<65>	-7928	473				
1249	G<163>	-7144	338	1299	G<63>	-7944	338				
1250	G<161>	-7160	473	1300	G<61>	-7960	473				

## 6.4. DISPLAY MODULE DEFAULT POSITION

The default position (display driver, glass, filter order, etc) of the display module is always as follow, when MADCTL's (36h) parameter is 00h. The color filter is always RGB (if color filters are used).

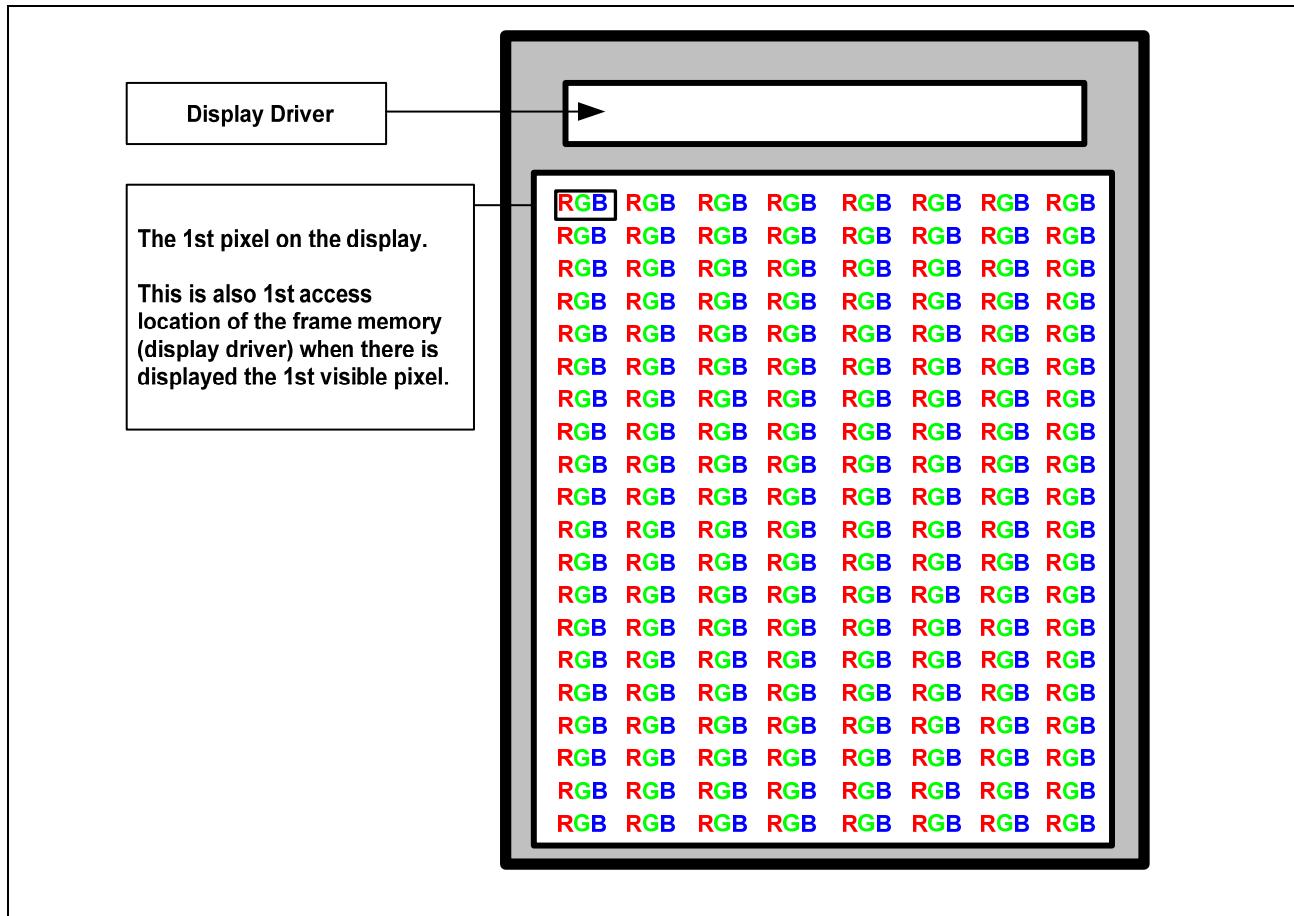


Figure 154. Display module default position