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(1) Application

This literature applies to LS020A8DX02.

(2) Overview

This module is a color transfective and active matrix LCD module incorporating CG silicon TFT (Thin Film Transistor), named mASV-TFT(mobile-ASV TFT). It is composed of a color TFT-LCD panel, a driver IC, a FPC, and a back light.

Graphics and texts can be displayed on a 960×240 dots panel with 16,777,216 colors by supplying.

(3) General specifications

Table 1

Parameter	Specifications	Remarks
Screen size (Diagonal)	1.96" Diagonal	inch
Pixel format	$960(\text{H}) \times 240(\text{V})$ (1 pixel = R+G+B dots)	
Pixel pitch	0.0415 (H) \times 0.1245 (V)	mm
Top Polarizer	3H Hardcoat	
Interface	8bit serial RGB I/F (HSYNC, VSYNC, DCK, D0-D7)	
Display active area	$39.82(\text{H}) \times 29.88(\text{V})$	mm
Unit outline dimension	$45.8(\text{W}) \times 40.2(\text{H}) \times 1.76(\text{D})$	【Note3-1】
Mass	5.6 grams	(TYP.)

【Note 3-1】

Excluding protrusion. For detailed measurements and tolerances, please refer to Fig. 1.

(4) Absolute Maximum Ratings

Table 2

Ta=25°C

Parameter	Symbol	Condition	Ratings	Unit	Remark
Supply voltage for LCD	VDD	—	-0.3~+5.5	V	
Input voltage (Digital)	VIN	—	-0.3~VDD+0.3	V	【Note4-1】
LED Power dissipation	P _{D LED}	—	123	mW	【Note4-2】
LED current	IL	—	30	mA	
Operating temperature (panel surface)	T _{op}	—	-10~60	°C	【Note4-3】
Storage temperature	T _{stg}	—	-20~70	°C	

【Note4-1】 Applies to RESETB, CSB, SI, SCLK, VSYNC, HSYNC, DCLK, D0~D7

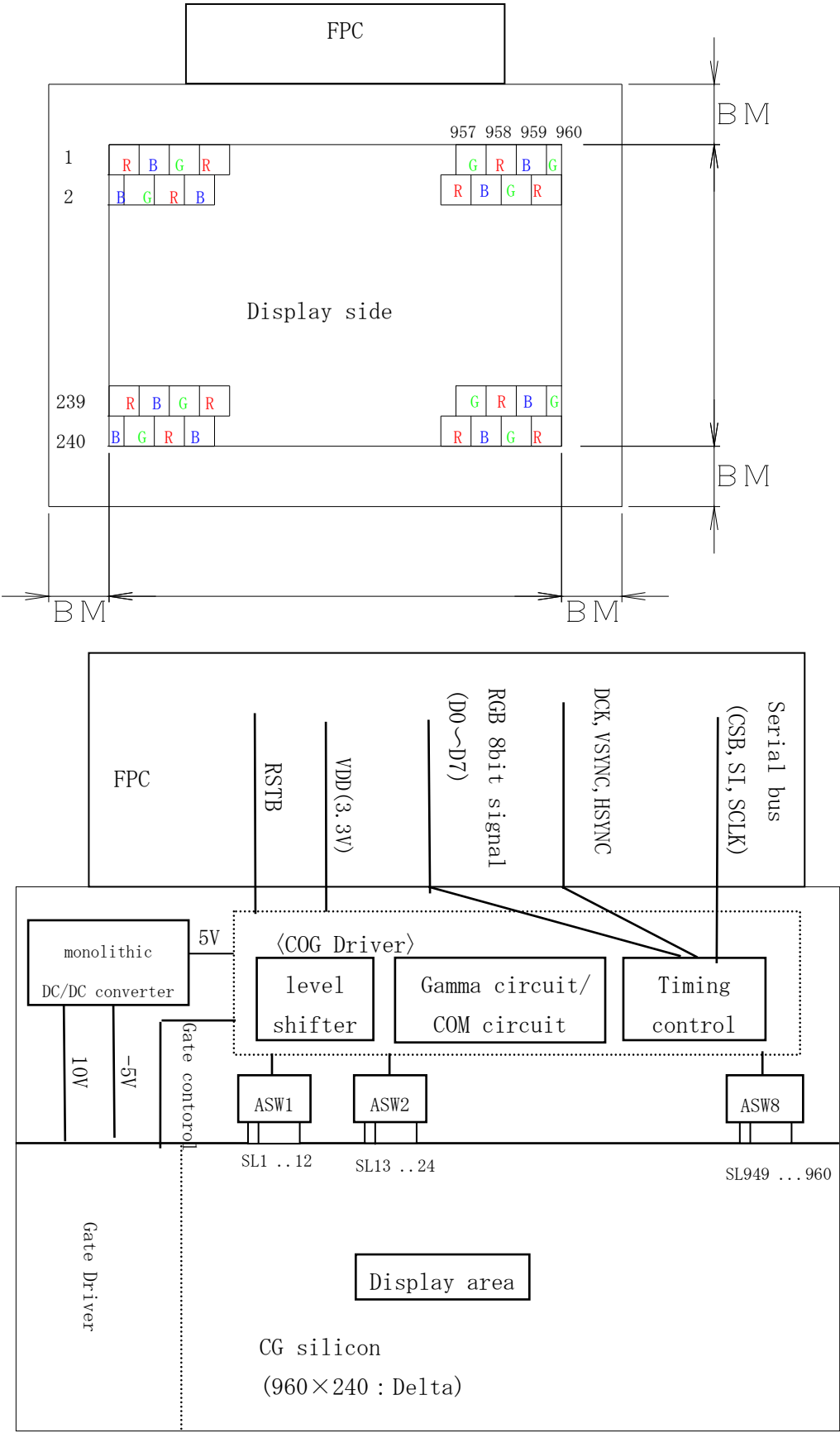
【Note4-2】 Specification for LED per 1pcs

【Note4-3】 Humidity: 95%RH Max.

(at Ta \leq 40°C). Maximum wet-bulb temperature is less than 39°C

(at Ta > 40°C). Condensation of dew must be avoided.

(5)Pixel configuration



(6)Input/Output terminal

6-1)TFT-LCD panel driving section

Table3

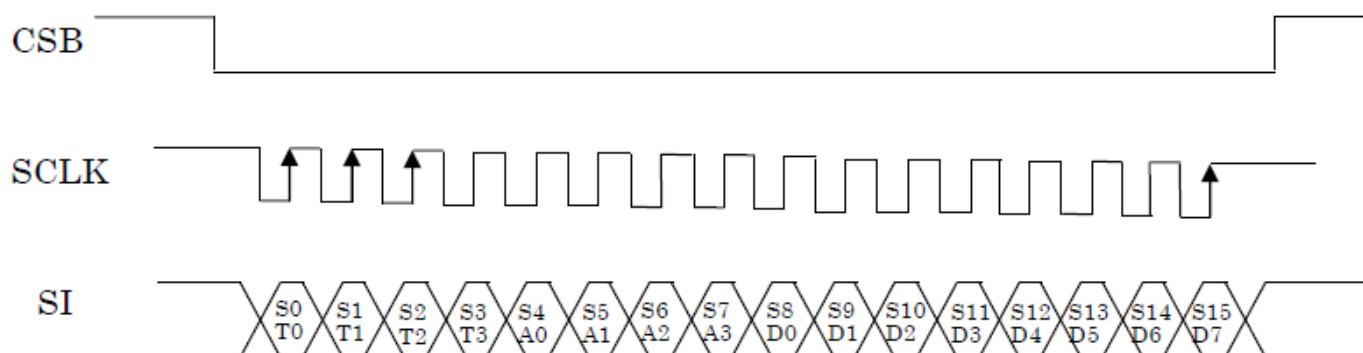
Pin No.	Symbol	I/O	Description	Remarks
1	LED_AN	I	LED Anode	-
2	LED_AN	I	LED Anode	-
3	LED_CA	-	LED Cathode	-
4	LED_CA	-	LED Cathode	-
5	GND	-	GND	
6	RSTB	I	Reset signal input	“L” active
7	CSB	I	Chip select input for serial interface	“L” active
8	SI	I	Data input for serial interface	
9	SCLK	I	Serial clock input for serial interface	
10	VSNC	I	Vertical Sync. input	
11	HSNC	I	Horizontal Sync. Input	
12	GND	-	GND	
13	DCK	I	Dot clock input	
14	GND	-	GND	
15	D7	I	Display data input	-
16	D6	I	D0 : LSB, D7 : MSB	-
17	D5	I	RGB data input according to the pixel arrangement.	-
18	D4	I		-
19	D3	I		-
20	D2	I		-
21	D1	I		-
22	D0	I		-
23	GND	-	GND	
24	VDD	I	LCD power supply	-
25	VDD	I	LCD power supply	-

Used connetion: 0.3mm pitch FPC connector

Correspondable connector: FF02S25SV1 (JAE)

(7)Serial setting at control portion

7-1) timing chart



[Operation for serial interface]

- The SPI data are 16 bits, and should be latched at rising edge of SCLK.
- Start of data latched is at the falling edge of CSB and End of data latched is at the rising edge of CSB.
- Any write operation less than 16 SCLK rising edge during a CSB low period will be ignored by SPI engine.
- Any write operation with more than 16 SCLK rising edge during a CSB low period will be latched last 16 bit data.
- The SPI block operates by SCLK pulses.
- The SPI block can be written during standby mode.(SPI block won't be power saved during standby mode)
- Register setting is reflected from the following VSYNC that the serial communication completed and that data was captured.
- If setting other than recommended setting is temporarily read due to disturbance, etc., it recovers the normal display by re-setting recommended setting.

7-2) register map

Address	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
00	COMAC	VCOM Amp. adjust	—	—	COMAC					
01	COMDC	VCOMDC adjust	COMDC							
02	—	Reserve	—	—	—	—	—	—	—	—
03	VDISP	Vertical timing setting	NORBLK	COMTST	—	VPOSITION				
04	HDISP	Horizontal timing setting	HPOSITION							
05	PANEL	Panel setting	—	PANEL_SELECT		—	PAIR	—	SLFR	—
06	FUNC1	FUNCTION1	—	—	—	XPSAVE	—	RGT	DWN	—
07	FUNC2	FUNCTION2	PALTYPE	PALMODE	VFORMAT	—	—	CLKPOL	VDPOL	HDPOL
08	FUNC3	FUNCTION3	—	—	—	—	—	—	LPFSEL	
09	VP_CNT	V255+／V0+ setting	—	V255P_SEL			—	VOP_SEL		
0A	VM_CNT	V255-／V0- setting	—	V255M_SEL			—	VOM_SEL		
0B-0F	—	Reserve	—	—	—	—	—	—	—	—
10	VCNT1	Internal voltage setting	—	—	VS_SEL		—	—	VDDL_CTRL	
11	VCNT2	Panel voltage setting	—	—	VR2_SEL		—	—	VR1_SEL	
12	DCDC1	External DCDC setting	—	—	—	—	—	—	FSDIV	
13	DCDC2	Internal DCDC setting	—	—	FSINT		—	—	—	—
14	TIMING1	LCD driving timing setting1	SSWS				SSWW			
15	TIMING2	LCD driving timing setting2	COMC		—	—	—	SSWP		
16	TIMING3	LCD driving timing setting3	PSWS		—	—	PSWW			
17	CGS	CGS panel setting	PCLVL2		PCLVL1		—	—	SSDSW	
18-1F	—	reserve	—	—	—	—	—	—	—	—

7-3) serial setting explanation

7-3-1) COMDC register

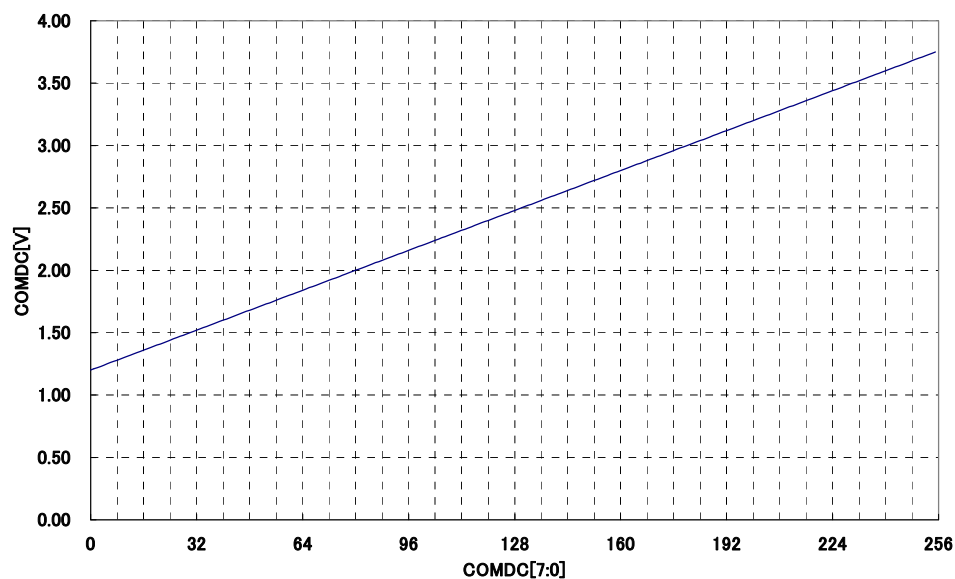
COMDC[7:0] register is to adjust center voltage of VCOM within 256 level setting.

The value is when VS=5.0V (VS_SEL[1:0]=01) without loading condition.

The value depends on output loading condition.

COMDC default value : 6Fh (01101111b) (2.31V)

COMDC change per step : 10.0mV/LSB



7-3-2) PANEL register

Bit	Name	Function	Description
D0	—	—	Don't care
D1	SLFR	Setting for inversion driving method	Change inversion driving method. It will be used for testing or debug purpose. 0 : 1Hinversion (default) 1 : n/a
D2	—	—	Don't care
D3	PAIR	Setting for display start position in Even Field	0 : 285LINEstart (default) 1 : n/a
D4	—	—	Don't care
D5	PanelSelect	Setting for panel type	Change panel resolution/timing setting.
D6			
D7	—	—	Don't care

• PAIR (Setting for V-start position in Odd/Even Field)

It is to set display start position of half line out of total 525 lines under NTSC timing.

In NTSC timing, Odd Field starts from 22LINE and Even Field starts from 285LINE.

0 : 285Line (Default)

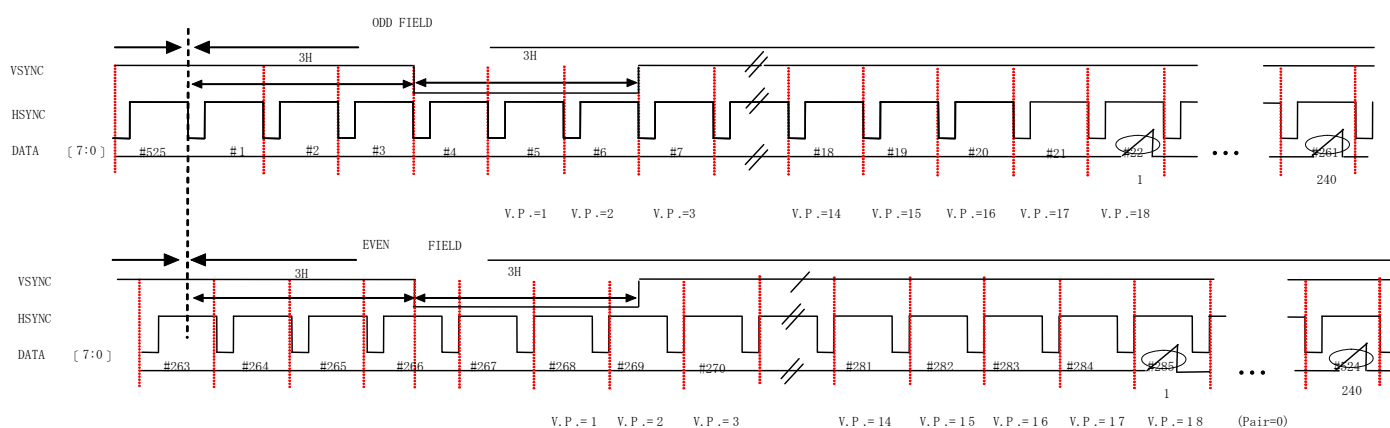
1 : 284Line (n/a)

Display start position is defined by register value for V-retrace period(VPOSITION). When VPOSITION=18, EVEN field starts from above line.

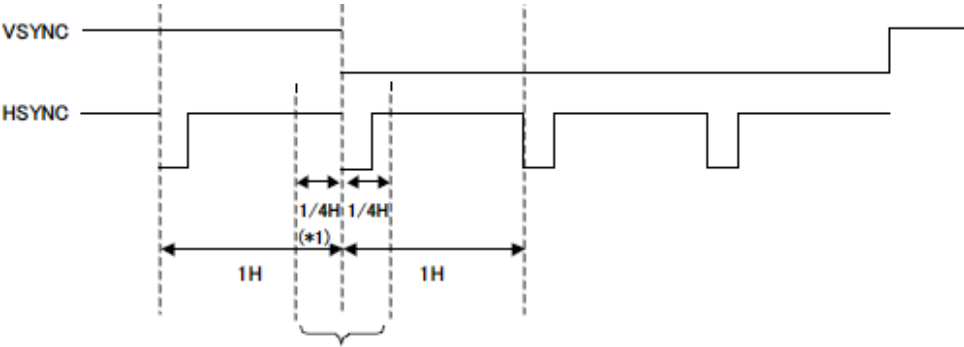
Relation between line number (#xxx) and Vertical sync(VSYNC) is shown as follows which complies with NTSC .

Register setting for vertical retrace period (V.P.) is also described.

When Pair = 1, V.P only in Even Field is to be counted one line earlier



[ODD/EVEN FIELD detect method]



HSYNC edge is detected within 1/4 horizontal period before/after VSYNC edge => ODD FIELD

HSYNC edge is NOT detected within 1/4 horizontal period before/after VSYNC edge => ENEN

Video valid line(VPOSITION=18)

[Pair=0]

FIELD \ LINE	START	END
ODD	22	261
EVEN	285	524

Panel select

Panel select		Resolution	DCLK frequency	Note
D6	D5			
0	1	960 x 240	27MHz	Delta (default)

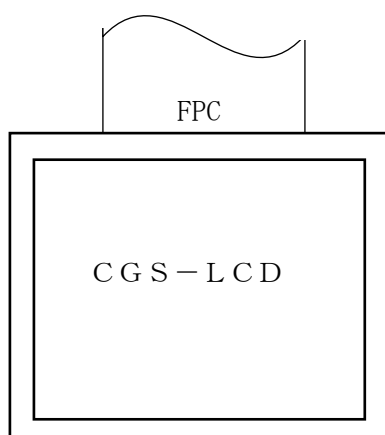
7-3-3) FUNC1 register

Bit	Name	Function	Description
D0	—	—	Don't care
D1	DWN	UP/DOWN inversion	Change UP/DOWN 0 : n/a (default value when H/W reset) 1 : UP/DOWN inversion
D2	RGT	LEFT/RIGHT inversion	Change LEFT/RIGHT 0 : n/a (default value when H/W reset) 1 : LEFT/RIGHT inversion
D3	—	—	Don't care
D4	XPSAVE	Standby control	Change standby or normal operation 0 : Stand by (default value when H/W reset) 1 : Normal
D5	—	—	Don't care
D6	—	—	Don't care
D7	—	—	Don't care

※DO NOT write into XPSAVE register during ON/OFF sequence.

DWN, RGT (UP/DOWN, LEFT/RIGHT setting)

- UP/DOWN , LEFT/RIGHT inversion display (DWN/RGT)



LEFT/RIGHT, UP/DOWN inverted display
DWN=1
RGT=1

- Standby control function(XPSAVE)

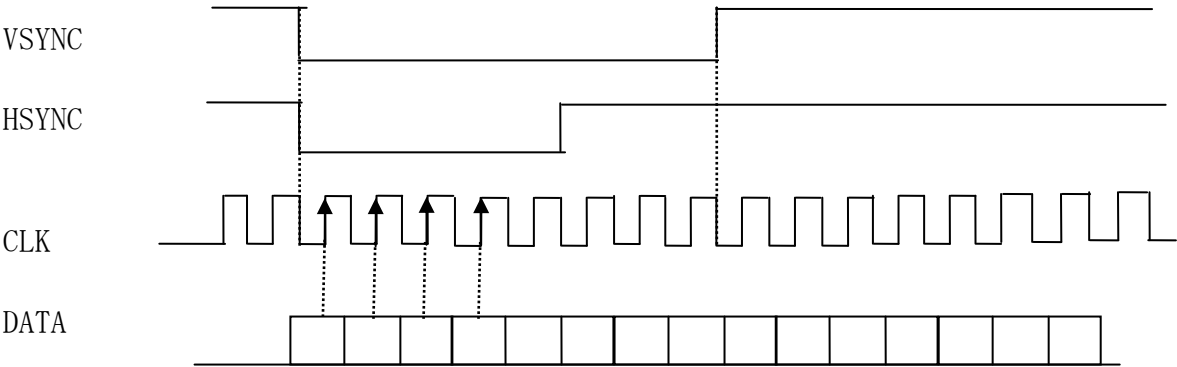
Circuit block other than serial interface is suspended during standby mode.

7-3-4) FUNC2 register

Bit	Name	Function	Description
D0	Hdpol	Change polarity in HSYNC	0 : n/a 1 : Negative (default value when H/W reset)
D1	Vdpol	Change polarity in VSYNC	0 : n/a 1 : Negative (default value when H/W reset)
D2	CLKpol	Change polarity in CLK	0 : Rising edge (default value when H/W reset) 1 : n/a
D3	—	—	Don't care
D4	—	—	Don't care
D5	VFORMAT	VIDEO input format	Setting for Video input format 0 : RGB(default value when H/W reset) 1 : n/a
D6	PALMODE	Change NTSC or PAL	0 : NTSC (default value when H/W reset) 1 : n/a
D7	PALTYPE	Change PAL line number	0 : default 1 : n/a

- Hdpol, Vdpol, CLKpol (Polarity change on sync signal, CLK signal)

D0=1,D1=1,D2=0



(8)Electrical characteristics

8-1)Recommended operating conditions

A) TFT-LCD panel driving section

Table 4

VSS=0V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable Pin
Supply voltage for LCD	VDD-VSS	Ta=-10~60 °C	2.85	3.3	3.6	V	VDD
Input leakage current	I _{LI}	Ta=-10~60 °C V _{IN} = VSS or VDD	-	-	10	μ A	【Note8-1】
”H” level input voltage	V _{IH}	Ta=-10~60 °C	0.7V _{DD}	-	V _{DD}	V	
”L” level input voltage	V _{IL}		0	-	0.3V _{DD}	V	

【Note8-1】 Applies to RESETB,CSB,SI,SCLK,VSYN,HSYN,DCLK,D0~D7

B) Back light driving section

Table 5

Ta=25 °C

Parameter	Symbol	MIN	TYP	MAX	Units	Remarks terminal
LED voltage	VL1-VL2	—	12.8	14	V	
LED current	IL	—	20	25	mA	
Power consumption	WL	—	256	350	mW	【Note 8-4】

【Note 8-4】 Measurement Conditions

3.2V(Typ) applied to 4 LED's in series.

Calculated reference value(IL(TYP)×(VL1−VL2))

8-2)Power consumption

Table 6

Ta=25 °C

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Remarks
Power consumption, Panel	P _{LCD}	VDD=3.3V VSS=0V	-	33	46	mW	【Note 8-5】
Power consumption, Standby	P _{ST}		-	-	400	μ W	【Note 8-6】

【Note 8-5】 Measurement Conditions

frame frequency= 60 Hz

All white pattern

【Note 8-6】 Measurement Conditions

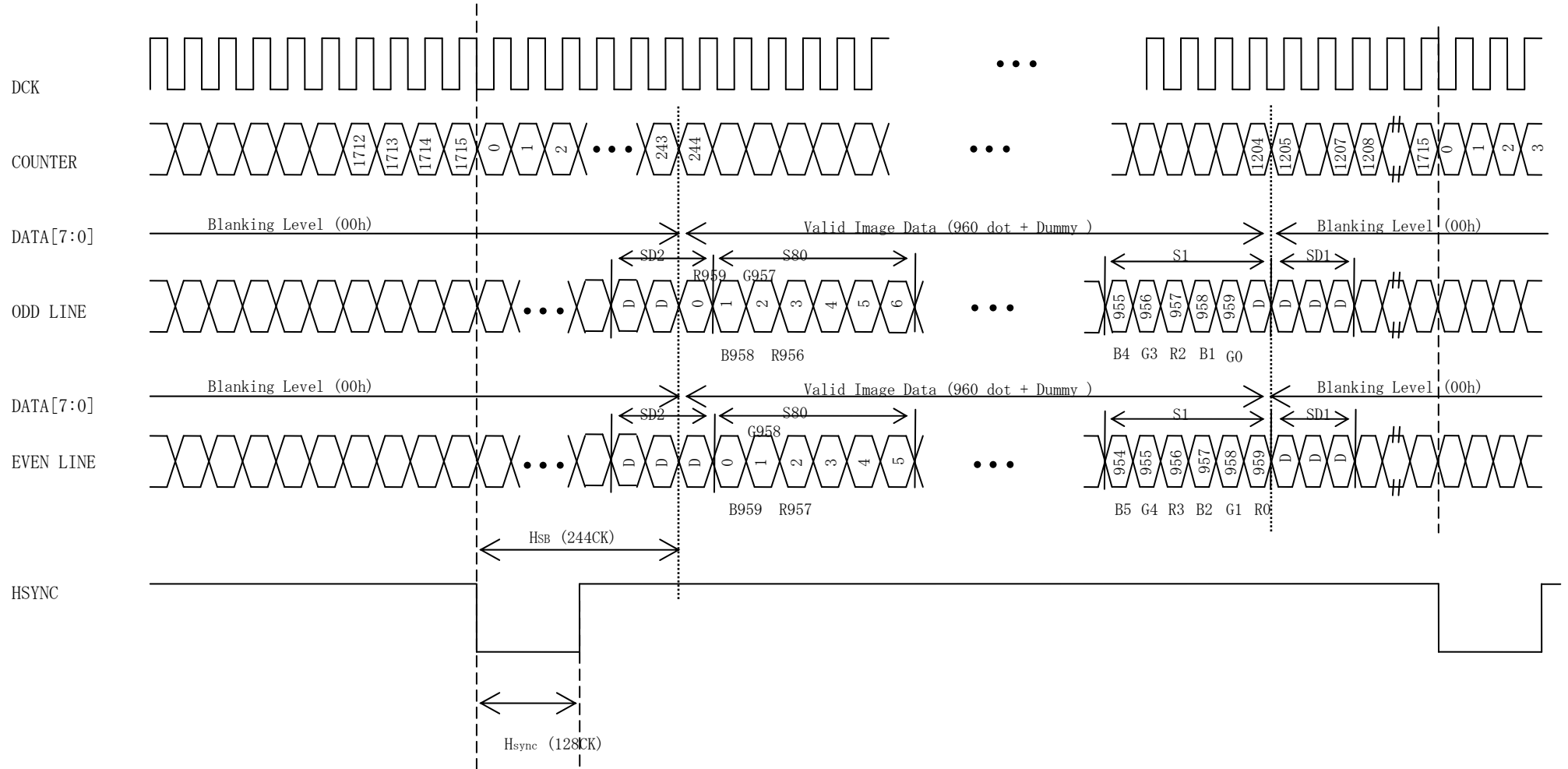
Standby mode (XPSAVE=0)

There are not DCLK, HSYN and VSYN input.

8-3) Digital signal processing

8-3-1) Horizontal timing

○RGB Mode 27MHz (same color writing: Horizontal 960dots, vertically and horizontally inverted scan)

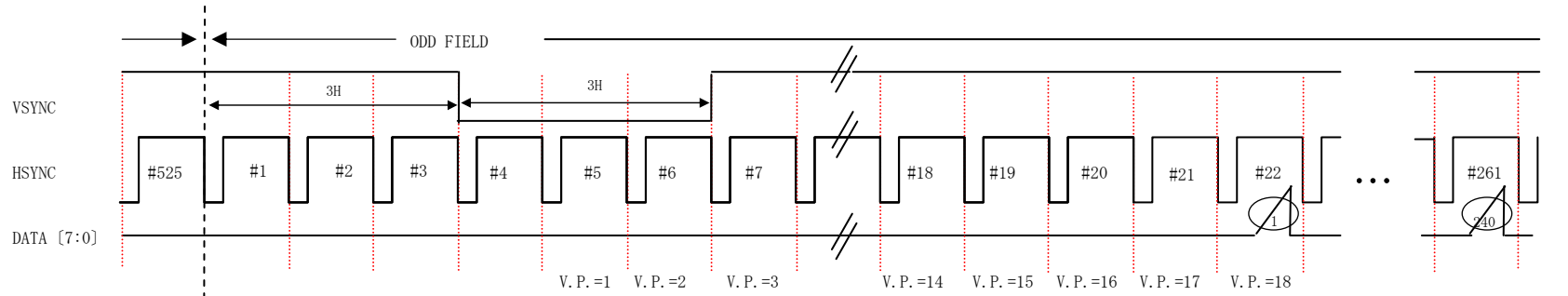


8-3-2) Vertical timing (NTSC Compliant)

○ ...Valid Display Line No.

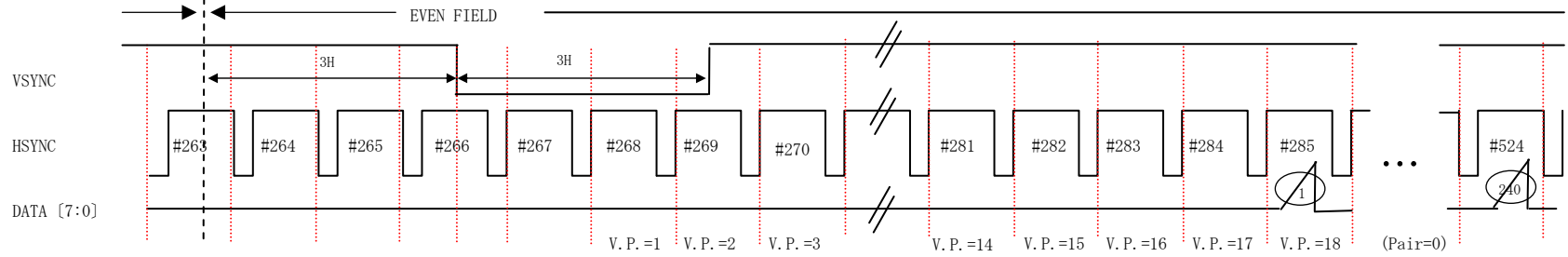
<ODD FIELD>

22~261LINE



<EVEN FIELD>

285~524LINE



【Remarks】

- Output is NTSC (59.94Hz)
- V.P. : VPOSITION

Video Valid Line

(VPOSITION=18, Pair=0)

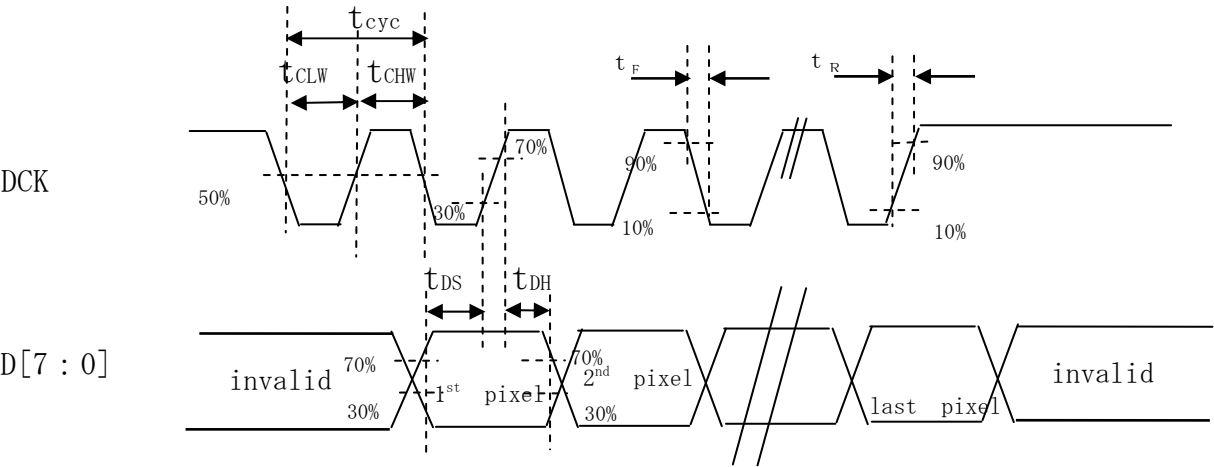
	START	END
ODD FIELD	22	261
EVEN FIELD	285	524

8－4). Input signal timing characteristics

Following figure shows input timing characteristics

8－4－1) Timing characteristics

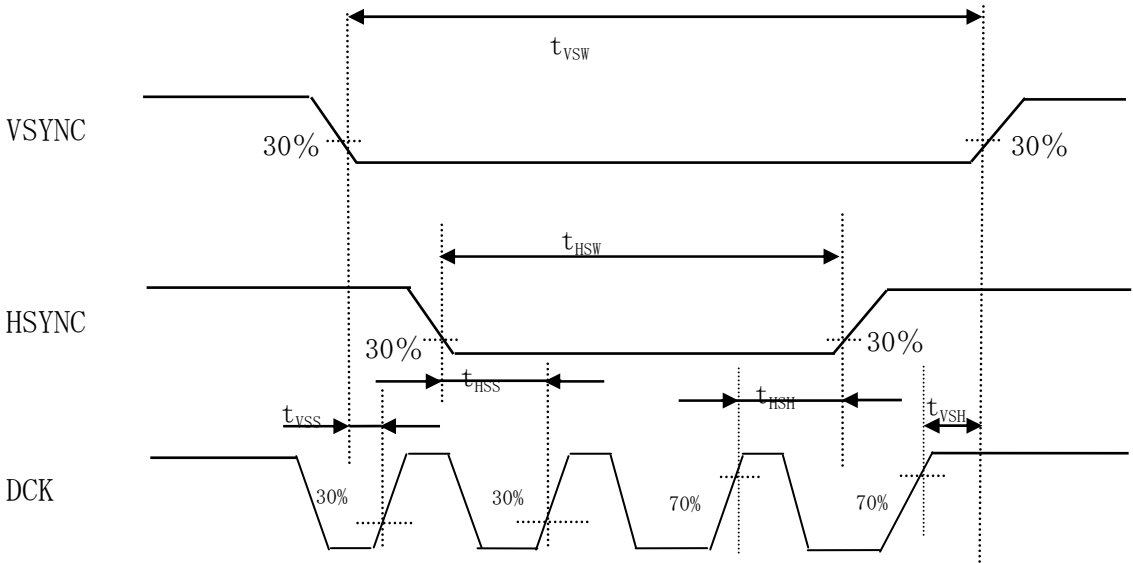
Input video signal timing 1 (In the case of DCK rising edge scan, HYSNC, VSYNC negative polarity)



(VDD=3.3V, Ta=25°C)

Item	ref	Condition	Min	Typ	Max	Unit
DCK duty	tcyc		37			ns
DCK high duration	tCHW		8			ns
DCK low duration	tCLW		8			ns
DCK duty ratio	tH2	tCHW:tCLW	45	50	55	%
DCK rising time	tR				10	ns
DCK falling time	tF				10	ns
Data setup time	tDS		4			ns
Data hold time	tDH		6			ns

Input video signal timing 2 (In the case of DCK rising edge scan, HYSNC, VSYNC negative polarity)



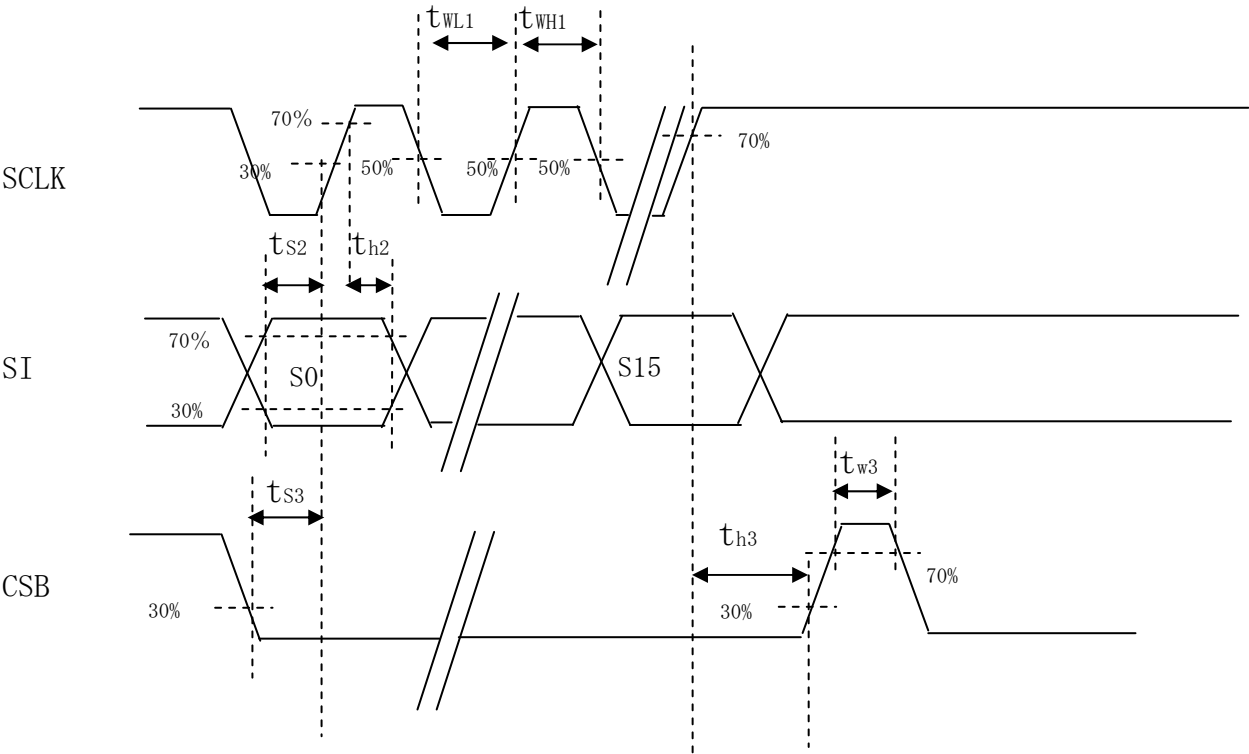
(VDD=3.3V, Ta=25°C)

Item	ref	Condition	Min	Typ	Max	Unit
HSYNC setup time	tHSS		4			ns
HSYNC hold time	tHSH		6			ns
VSYNC setup time	tVSS		4			ns
VSYNC hold time	tVSH		6			ns
HSYNC period	tHS W		1×DCLK			
VSYNC period	tVSW		1×DCLK			

Serial interface timing

(VDD=3.3V, Ta=25°C)

Item	ref	Condition	Min	Typ	Max	Unit
CSB setup	tS3		15			ns
SI setup	tS2		15			ns
CSB hold	th3		15			ns
SI hold	th2		15			ns
SCLK pulse low width	tWL1		30			ns
SCLK pulse high width	tWH1		30			ns
CSB pulse high width	tW3		20			ns



(9)Software Flow & Register Settings

9-1) Register Settings

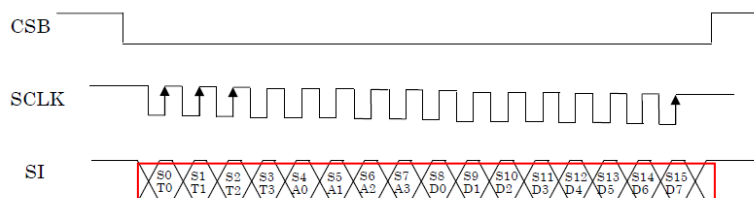
■ Power ON

Step	Address	Value	Sending hex	Comment
1	RSTB=L			
2	VDD : OFF=>ON			Supply voltage for LCD ON
3	Wait min10ms			
4	RSTB=H			RESET Release
5	Wait min10ms			
6	00h	1Ch	0038	
7	01h	6Fh	08F6	
8	03h	92h	0C49	
9	04h	F1h	028F	
10	05h	20h	0A04	
11	06h	06h	0660	DWN=1, RGT=1
12	07h	03h	0EC0	
13	08h	00h	0100	
14	09h	21h	0984	
15	0Ah	45h	05A2	
16	10h	32h	804C	
17	11h	22h	8844	
18	12h	02h	8440	
19	13h	20h	8C04	
20	14h	3Ah	825C	
21	15h	44h	8A22	
22	16h	CCh	8633	
23	17h	F2h	8E4F	
24	06h	16h	0668	XPSAVE=1
25	DCK, VSYNC, HSYNC start (signal on)			

■ Power OFF

Step	Address	Value	Sending hex	Comment
1	06h	06h	0660	XPSAVE=0
2	Wait 8Vsync			8Vsync after off-sequence condition, DCK, HSYNC and VSYNC must input
3	DCK, VSYNC, HSYNC: ON=>OFF			Signal off
4	RSTB=L			RESET
5	VDD: ON=>OFF			Supply voltage for LCD Off

note) Please pay attention to the sending order of the serial data.



For example (in case of Address=01h, Value=6F→sending data=08F6)															
Address(01h)								Value(6Fh)							
T3	T2	T1	T0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	1	1	0	1	1	1	1
T0	T1	T2	T3	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0

(10)Optical characteristics

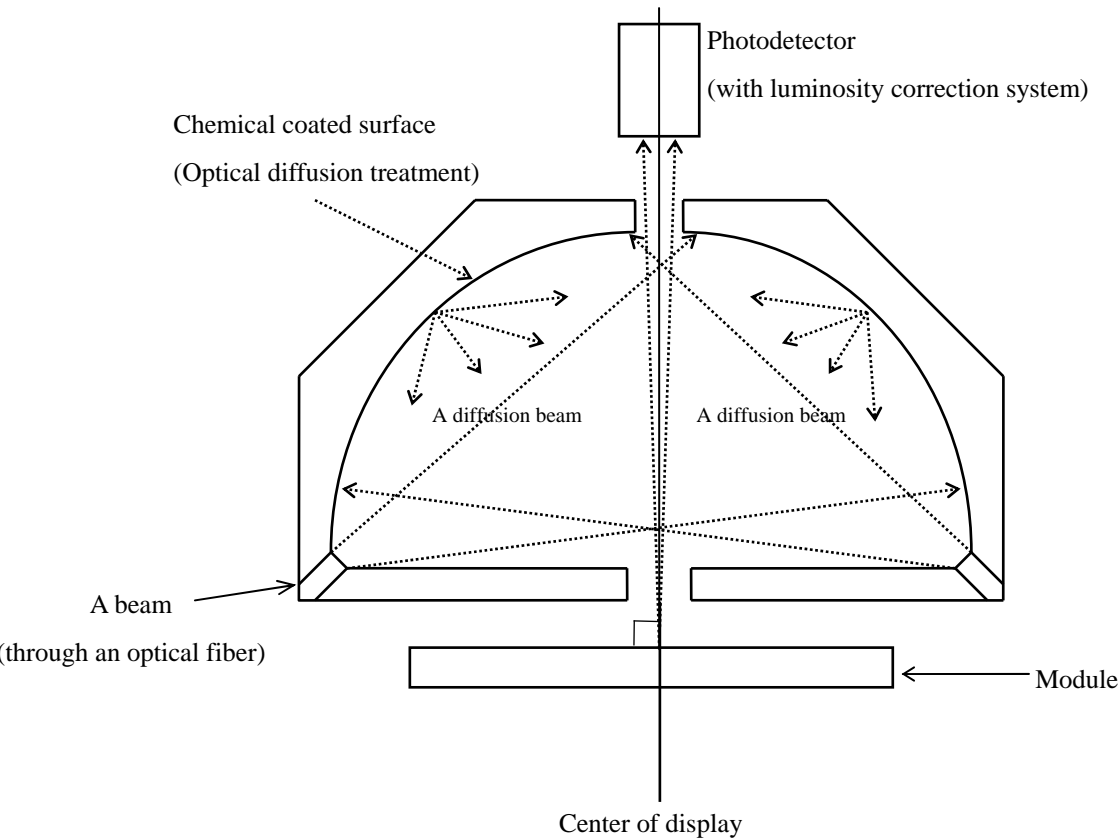
10-1)Not driving the Back light condition

Table 7 VDD=3.3V

Ta=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Contrast ratio	CR	$\theta = 0^{\circ}$	15	20	-	-	[Note 10-2,3]
White chromaticity	x	$\theta = 0^{\circ}$	-	0.31	-	-	
	y		-	0.33	-	-	
Reflection ratio	R	$\theta = 0^{\circ}$	3.0	4.0	-	%	[Note 10-5]

- * The measuring method of the optical characteristics is shown by the following figure.
- * A measurement device is Otsuka luminance meter LCD5200.(With the diffusion reflection unit.)



Measuring method (a) for optical characteristics

10-2)Driving the Back light condition

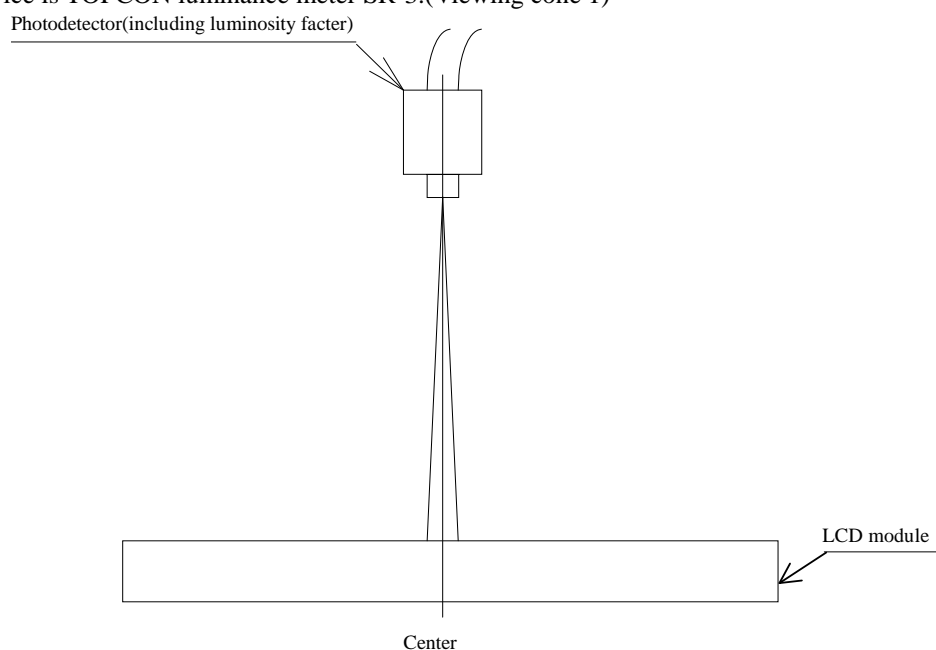
Table 8 VDD=3.3V

Ta=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Viewing angle range	θ11	CR≥10	60	80	-	degree	[Note 10-1,2]
	θ12		60	80	-	degree	
	θ21		60	80	-	degree	
	θ22		60	80	-	degree	
Contrast ratio	CR	$\theta = 0^\circ$	300	400	-	-	[Note 10-2]
Response time	Rise	$\theta = 0^\circ$	-	25	30	ms	[Note 10-4]
	Fall		-	15	20	ms	
White chromaticity	x	$\theta = 0^\circ$	0.25	0.30	0.35	-	
	y		0.27	0.32	0.37	-	
Brightness	Y	$\theta = 0^\circ$	300	400	-	cd/m ²	IL=20mA
NTSC ratio			-	50	-	%	

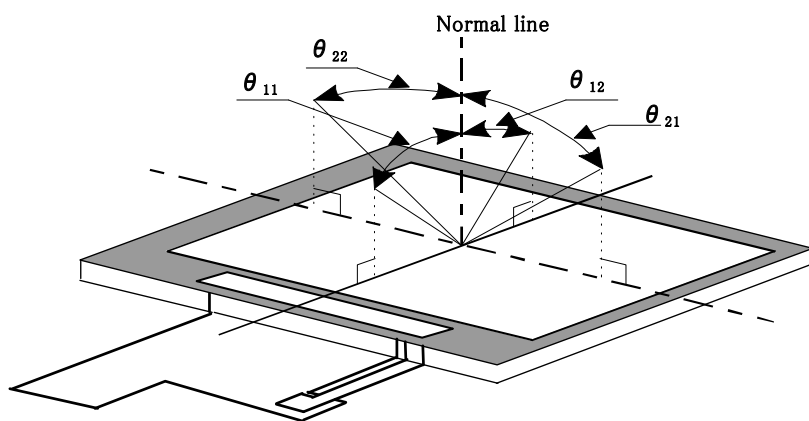
* The measuring method of the optical characteristics is shown by the following figure.

* A measurement device is TOPCON luminance meter SR-3.(Viewing cone 1)



Measuring method (c) for optical characteristics

[Note 10-1] Viewing angle range is defined as follows.



Definition for viewing angle

[Note10-2] Definition of contrast ratio:

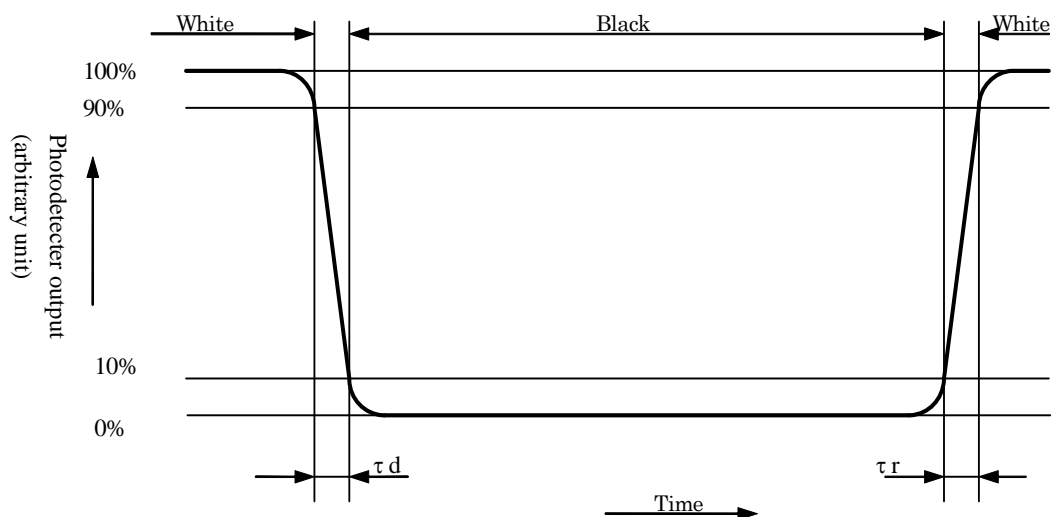
The contrast ratio is defined as follows:

$$\text{Contrast ratio (CR)} = \frac{\text{Photodetector output with all pixels white (GS63)}}{\text{Photodetector output with all pixels black (GS0)}}$$

[Note10-3] A measurement device is Minolta CM-2002.

[Note10-4] Definition of response time:

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white".



[Note10-5] Definition of reflection ratio

$$\text{Reflection ratio} = \frac{\text{Light detected level of the reflection by the LCD module}}{\text{Light detected level of the reflection by the standard white board}}$$

(11) Display quality

The display quality of the color TFT-LCD module shall be in compliance with the Incoming Inspection Standards for TFT-LCD.

(12) Mechanical characteristics

12-1) External appearance

See Fig. 1

12-2) FPC (for LCD panel) characteristics

(1) Specific connector

FF02S25SV1 (JAE)

(13) Handling Precautions

13-1) Insertion and taking out of FPCs

Be sure insert and take out of the FPC into the connector of the set after turning off the power supply on the set side.

13-2) Handling of FPCs

The FPC for LCD panel shall be bent only slit portion. The bending slit shall be bent uniformly on the whole slit portion with bending radius larger than 0.6mm ,and only inner side (back side of the module). Don't bend it outer side (display surface side).

Don't give the FPCs too large force, for example, hanging the module with holding FPC.

13-3) Installation of the module

On mounting the module, be sure to fix the module on the same plane. Taking care not to warp or twist the module.

13-4) Precaution when mounting

- (1) If water droplets and oil attaches to it for a long time, discoloration and staining occurs.

Wipe them off immediately.

- (2) Glass is used for the TFT-LCD panel. If it is dropped or bumped against a hard object, it may be broken. Handle it with sufficient care.

- (3) As the CMOS IC is used in this module, pay attention to static electricity when handling it.

Take a measure for grounding on the human body.

13-5) Others

- (1) The liquid-crystal is deteriorated by ultraviolet rays. Do not leave it in direct sunlight and strong ultraviolet rays for many hours.
- (2) If it is kept at a temperature below the rated storage temperature, it becomes coagulated and the panel may be broken. Also, if it is kept at a temperature above the rated storage temperature, it becomes isotropic liquid and does not return to its original state. Therefore, it is desirable to keep it at room temperature as much as possible.
- (3) If the LCD breaks, don't put internal liquid crystal into the mouth. When the liquid crystal sticks to the hands, feet and clothes, wash it out immediately.
- (4) Wipe off water drop or finger grease immediately. Long contact with water may cause discoloration or spots.
- (5) Observe general precautions for all electronic components.
- (6) Epoxy resin (amine series curing agent), silicone adhesive material (dealcoholization series and oxime series), tray forming agent (azo compound) etc, in the cabinet or the packing materials may induce abnormal display with polarizer film deterioration regardless of contact or noncontact to polarizer film. Be sure to confirm the component of them.
- (7) Use after you examine it fully because when liquid crystal is included into the product, stress such as a twist is added, and it becomes the cause which glass broken and brightness occasion unevenness occur in when condition is taken.

(14) Reliability Test Conditions for TFT-LCD Module

Table 9

No.	Test items	Test conditions	
1	Low temperature storage test	Ta=-20℃	240h
2	High temperature storage test	Ta=+70℃	240h
3	Thermal Shock storage test	Ta=-20℃:1h~70℃:1h	50cycles
4	Low temperature operating test	Ta=-10℃	240h
5	High temperature operating test	Ta=+60℃	240h
6	High temperature and high humidity operating test	Ta=+40℃ , 95%RH (But no condensation of dew)	240h
7	Electro static discharge test	$\pm 2\text{kV} \cdot 100\text{pF}(1.5\text{k}\Omega)$ 1 time for each terminals	
8	Shock test	980 m/s ² , 6 ms $\pm X, \pm Y, \pm Z$ 3 times for each direction (JIS C0041, A-7 Condition C)	
9	Vibration test	Frequency range: 10Hz~55Hz Stroke: 1.5 mm Sweep: 10Hz~55Hz X,Y,Z 2 hours for each direction (total 6 hours) (JIS C0040,A-10 Condition A)	

【Note】 Ta = Ambient temperature

【Check items】 Test No.1~9 : In the standard condition, there shall be no practical problems that may affect the display function.

(15) Others

15-1) Indication of lot number

The lot number is printed in the position shown in Fig. 1. (Outline Dimensions).

LS020A8DX02 ○○○○○○○○○○
 ① ②

①model name

②serial number

15-2) Used Regulation of Chemical Substances Breaking Ozone Stratum

Substances with the object of regulating : CFCS, Carbon tetrachloride, Halon

1,1,1-Trichloro ethane (Methyl chloroform)

- (a) This LCD module, Constructed part and Parts don't contain the above substances.
- (b) This LCD module, Constructed part and Parts don't contain the above substances in processes of manufacture.

15-3) If some problems arise about mentioned items in this document and other items, the user of the TFT-LCD module and Sharp will cooperate and make efforts to solve the problems with mutual respect and good will.

(16) Forwarding form

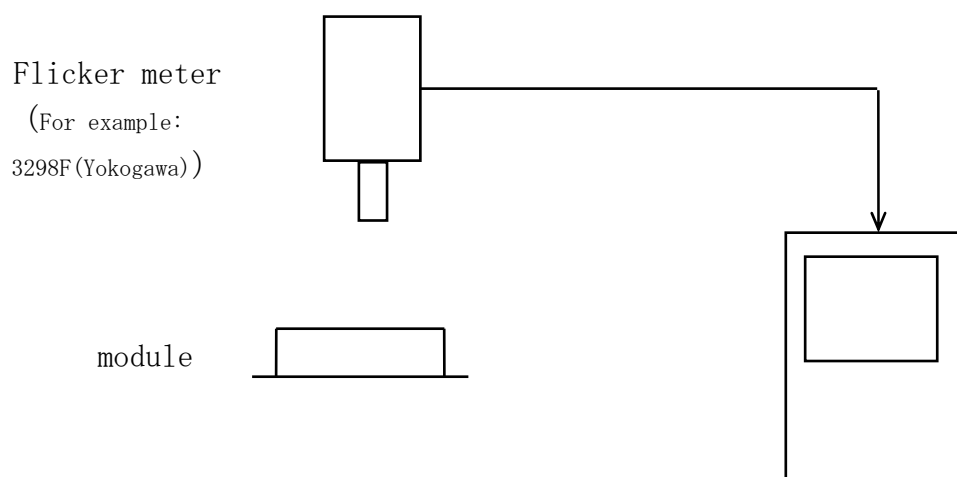
- a) Piling number of cartons : 8 deep
- b) Package quantity in one cartons : 400(pcs)
- c) Carton size : (w) 382×(D) 578×(H) 255 (mm)
- d) Total mass of 1 carton filled with full modules : approximately 8 (Kg)

Conditions for storage

Environment

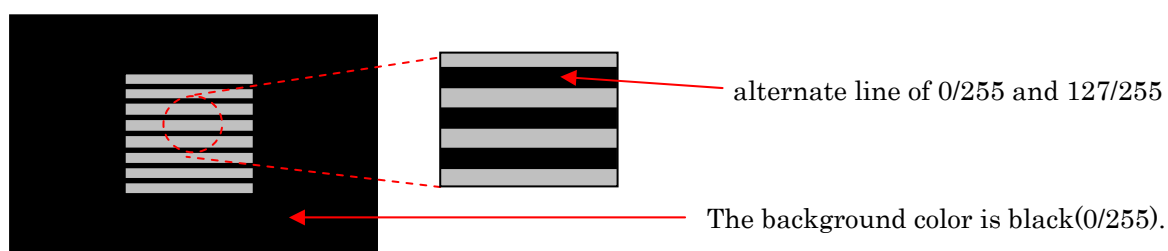
- (1)Temperature : 0~40°C
- (2)Humidity : 60%RH or less (at 40°C)
 No dew condensation at low temperature and high humidity.
- (3)Atmosphere : Harmful gas, such as acid or alkali which bites electronic components and/or wires, must not be detected.
- (4)Period : about 3 months
- (5)Opening of the package : In order to prevent the LCD module from breakdown by electrostatic charges, please control the room humidity over 50%RH and open the package taking sufficient countermeasures against electrostatic charges, such as earth, etc.

(Appendix) Flicker adjustment



図A Flicker adjustment system

Image for flicker adjustment



- When flicker meter is used for flicker adjustment, please adjust the COMDC (R01h) register to minimize the value of flicker meter.
- When visual method is used for flicker adjustment, please adjust the COMDC (R01h) register to minimize visual flicker on the display.

