

A Brighter Solution

AMP DISPLAY INC.

SPECIFICATIONS

CUSTOMER	
CUSTOMER PART NO.	
AMP PART NO.	AM-480800CTZQW-00H
APPROVED BY	
DATE	

☐ Approved For Specifications

☒ Approved For Specifications & Sample

AMP DISPLAY INC

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Revision Date	Page	Contents	Editor
2011/09/19	--	New Release	Kain
2012/06/14	5	Modification of Forward voltage	Kain

1 Features

LCD 3.5 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) for mobile-phone or handy electrical equipments.

(1) Construction: 3.5" a-Si color TFT-LCD, White LED driver & Backlight.

(2) Main LCD : 2.1 Amorphous-TFT 3.5 inch display, **Normally Black** type (MVA).

2.2 480(RGB)X800 dots Matrix

2.4 Main LCD Driver IC: HX8363

2.5 262K: Red-6bit, Green-6bit, Blue-6bit(18-bit interface)

(3) Interface: RGB Interface

2 Mechanical specifications

Dimensions and weight

Item		Specifications	Unit
External shape dimensions		*1 53.6 (W) x 88.75(H) X 7.06(D) .	mm
Main LCD	Pixel size	31.5 (W) x 94.5 (H)	um
	Active area	45.36 (W) x 75.6 (H)	mm
	Number of Pixels	480(H)x800(V) pixels	mm
View direction (Gray inversion)		MVA	
brightness		500	nits
Weight		42	g

*1. This specification is about External shape on shipment from AMPIRE.

3 Absolute max. ratings and environment

3-1 Absolute Max. ratings

Ta=25°C GND=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power voltage	VCC – GND	-0.3	+4.6	V	
Power voltage	VLED – GND	-0.3	+6.5	V	
Input voltage	VIN	-0.5	VCC+0.3	V	

3-2 Environment

Item	Specifications	Remarks
Storage temperature	Max. +80 °C Min. -30 °C	Note 1: Non-condensing
Operating temperature	Max. +70 °C Min. -20 °C	Note 1: Non-condensing

Note 1 : $T_a \leq +40\text{ °C}$ Max.85%RH

$T_a > +40\text{ °C}$ The max. humidity should not exceed the humidity with 40 °C 85%RH.

4 Electrical specifications

4-1 Electrical characteristics of LCM

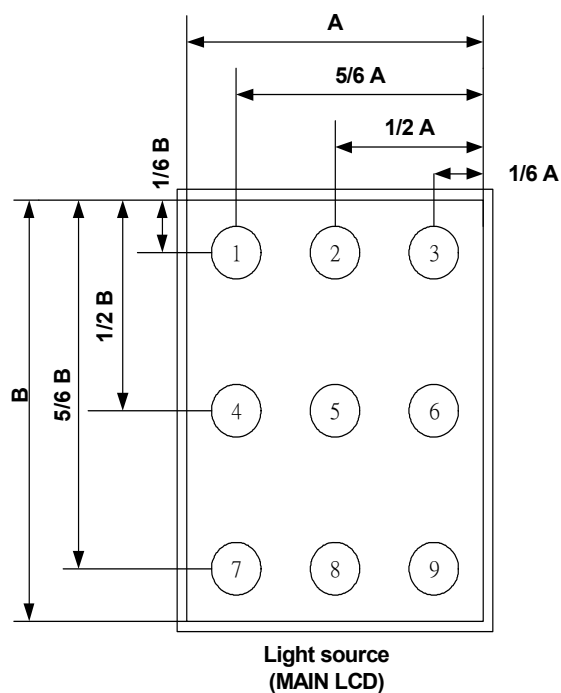
($V_{CC}=3.0V$, $T_a=25\text{ °C}$)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input power voltage	V_{CC}		2.8	3.3	3.8	V
LED driver input voltage	V_{LED}		2.5	5	6	
High-level input voltage	V_{IHC}		$0.7 \cdot V_{CC}$		V_{CC}	V
Low-level input voltage	V_{ILC}		0		$0.3 \cdot V_{CC}$	V
Consumption current of VCC	I_{CC}	LED OFF	-	TBD	-	mA
Consumption current of VLED	I_{LED}	$V_{LED}=5V$	-	TBD	-	mA

4-2 LED back light specification

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	V_f	$I_f = 80\text{mA}$	--	19.2	--	V
Forward current	I_f		--	80	--	mA
Luminous color	White					

Bare LED measure position:



*1 Uniformity (LT): $\frac{\text{Min}(P1 \sim P9)}{\text{Max}(P1 \sim P9)} \times 100 \geq 80\%$

5 Optical characteristics

Main LCD

5.1 Optical characteristics

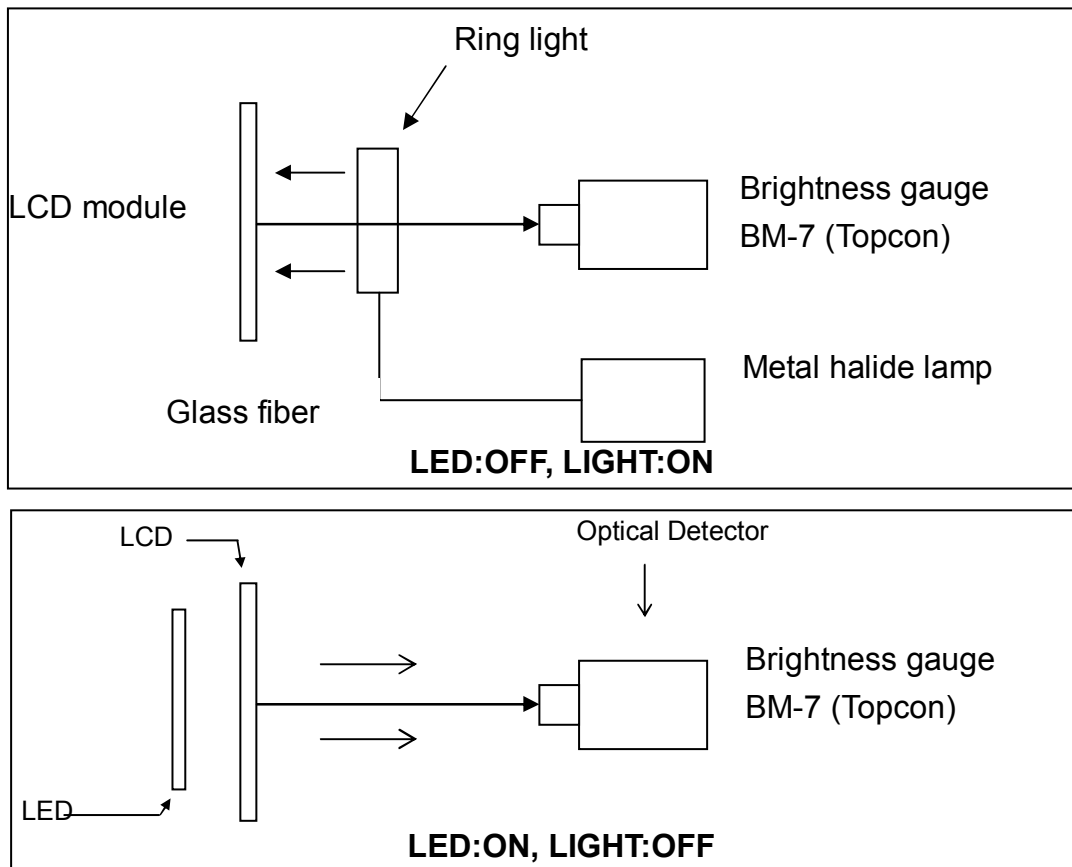
LED backlight transmissive module:

Item	Symbol	Temp.	Min.	Std.	Max.	Unit	Conditions
Response time	Tr+Tf	25 °C	--	30	--	ms	$\theta=0^{\circ}$, $\varphi=0^{\circ}$ (Note 2)
Contrast ratio	CR	25 °C	--	500	-	-	$\theta=0^{\circ}$, $\varphi=0^{\circ}$ LED:ON, LIGHT:OFF (Note 4)
Transmittance	T	25 °C	-	3	-	%	
Visual angle range front and rear	θ	25 °C	(θf) 80 (θb) 80			De-gree	$\varphi=0^{\circ}$, $CR \geq 10$ LED:ON LIGHT:OFF (Note 3)
Visual angle range left and right	θ	25 °C	(θl) 80 (θr) 80			De-gree	$\varphi=90^{\circ}$, $CR \geq 10$ LED:ON LIGHT:OFF (Note 3)
Brightness		25 °C	--	500	--	Cd/m ²	80mA Full White pattern
Life time		25 °C	--	30k	--	Hrs	

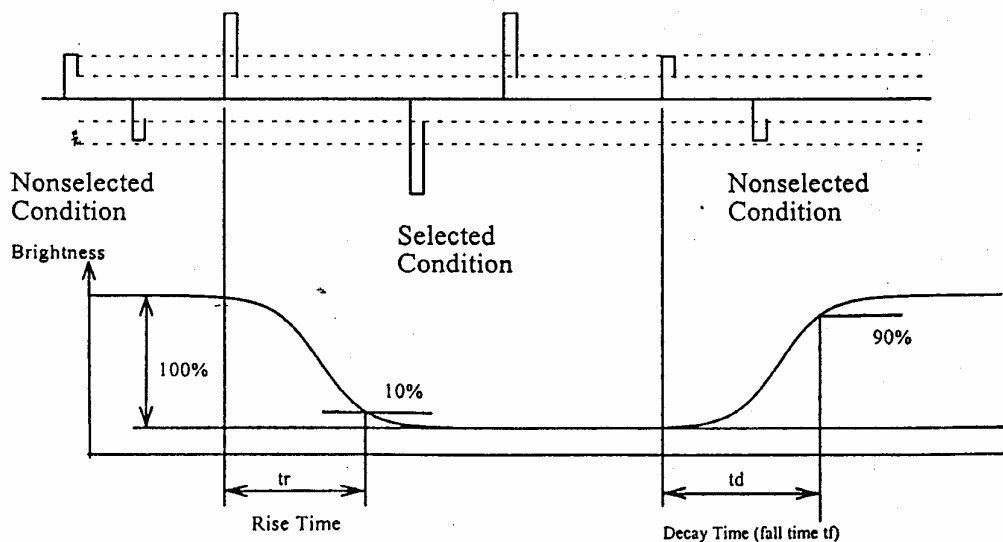
5.2 CIE (x, y) chromaticity (1/320 Duty Ta = 25°C)

Item	Symbol	Transmissive			Conditions
		Min.	Typ.	Max.	
Red	X	0.634	0.665	0.694	$\theta=0^{\circ}$, $\varphi=0^{\circ}$
	Y	0.292	0.332	0.352	
Green	X	0.242	0.271	0.302	$\theta=0^{\circ}$, $\varphi=0^{\circ}$
	Y	0.563	0.595	0.623	
Blue	X	0.106	0.136	0.166	$\theta=0^{\circ}$, $\varphi=0^{\circ}$
	Y	0.062	0.136	0.122	
White	X	0.268	0.297	0.328	$\theta=0^{\circ}$, $\varphi=0^{\circ}$
	Y	0.295	0.322	0.355	

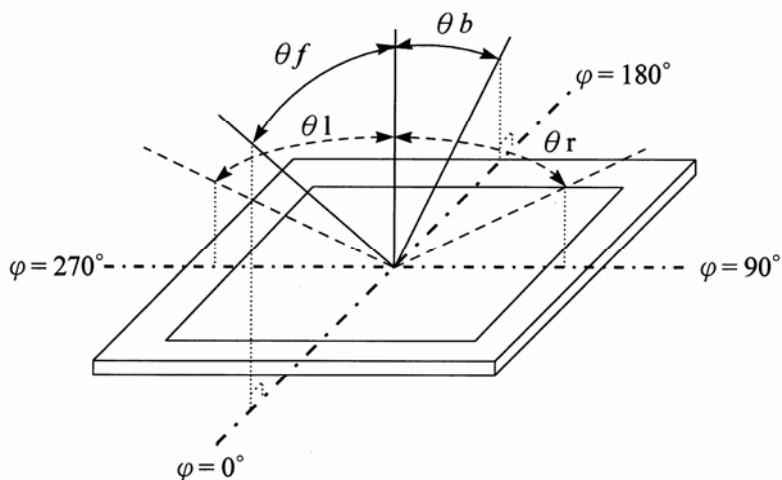
NOTE 1: Optical characteristic measurement system



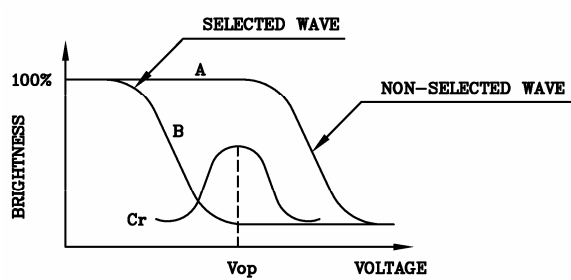
NOTE 2: Response time definition



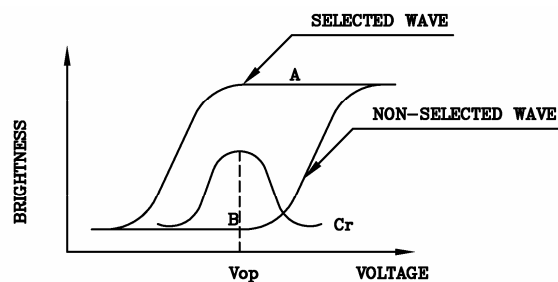
NOTE 3: φ 、 θ definition



NOTE 4: Contrast definition



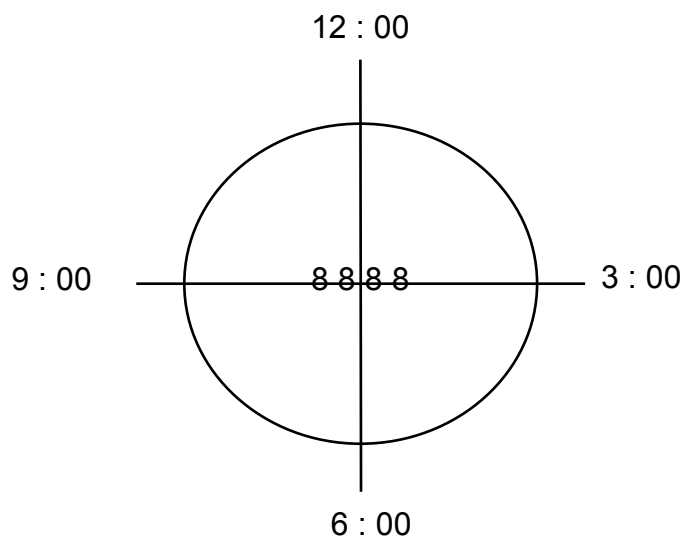
(positive type)



(negative type)

Contrast Ratio : $Cr = A/B$

NOTE 5: Visual angle direction priority



6. Electrical Specifications

6.1 LCD Interface (J1)

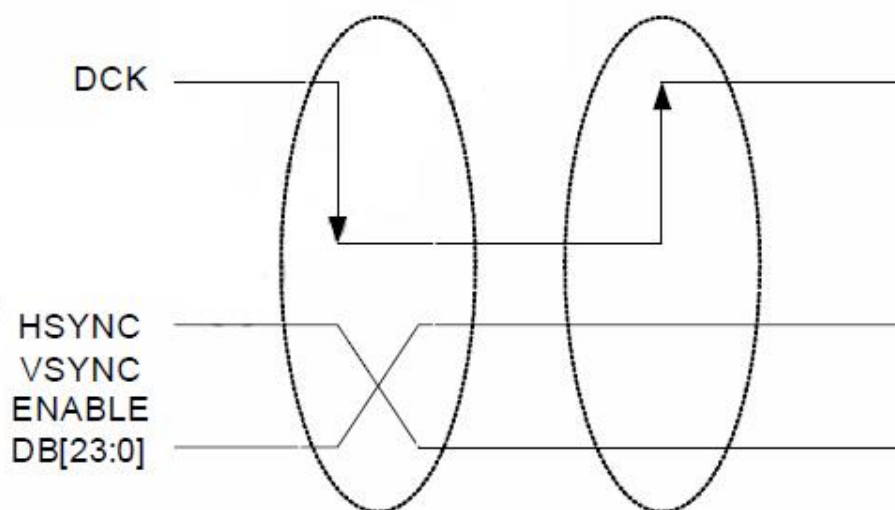
1	PVSS	External high voltage pin used in OTP mode and operates at 7.5V If not be used, let it open.												
2	DB23	<div>RGB interface</div> <table><tr><th>Data bus</th><th>Used</th><th>Unused</th></tr><tr><td>16-bit bus</td><td>DB21~17, DB13~8, DB5~1</td><td>DB23-22, DB16-14, DB7-6, DB0</td></tr><tr><td>18-bit bus</td><td>DB21~16, DB13~8, DB5~0</td><td>DB23-22, DB15-14, DB7-6</td></tr><tr><td>24-bit bus</td><td>DB23-D0</td><td>--</td></tr></table> <p>Let the unused pins open for each mode.</p>	Data bus	Used	Unused	16-bit bus	DB21~17, DB13~8, DB5~1	DB23-22, DB16-14, DB7-6, DB0	18-bit bus	DB21~16, DB13~8, DB5~0	DB23-22, DB15-14, DB7-6	24-bit bus	DB23-D0	--
Data bus	Used		Unused											
16-bit bus	DB21~17, DB13~8, DB5~1		DB23-22, DB16-14, DB7-6, DB0											
18-bit bus	DB21~16, DB13~8, DB5~0		DB23-22, DB15-14, DB7-6											
24-bit bus	DB23-D0		--											
3	DB22													
4	DB21													
5	DB20													
6	DB19													
7	DB18													
8	DB17													
9	DB16													
10	DB15													
11	DB14													
12	DB13													
13	DB12													
14	DB11													
15	DB10													
16	DB9													
17	DB8													
18	DB7													
19	DB6													
20	DB5													
21	DB4													
22	DB3													
23	DB2													
24	DB1													
25	DB0													
26	HSYNC	Line synchronizing signal. Must be connected to GND or IOVCC												
27	VSYNC	Frame synchronizing signal. Must be connected to GND or IOVCC												
28	ENABLE	A data ENABLE signal in RGB I/F mode. Has to be fixed to VSSD level in MPU interface mode.												
29	GND	Ground												
30	DCLK	Dot clock signal. Must be connected to GND or IOVCC												
31	GND	Ground												
32	NCS	Chip select signal “0” can be accessed “1” cannot be accessed. If this pin not used, please connect to GND or IOVCC												
33	SCL	Serves as a write signal and writes data at the rising edge. When operate in serial interface, it serves as SCL (serial Clock). If not be used, let it open or connected to IOVCC												
34	SDI	Serial data input pin in serial interface operation												
35	SDO	Serial data output. Let it to open in MPU interface mode.												

36	CABC_PWM_Out	Backlight On/Off control pin. If use CABC function, the pin can connect to external LED driver IC. The output voltage range = 0~VDD1
37	RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied (Must be connected to GND or IOVCC) (Latch Type)
38	IOVCC	A power supply for the IO circuit. Voltage 1.65~3.3V
39	VCC	A power supply for analog and DC/DC circuit. Voltage 2.3~3.3V
40	GND	Ground

Note. Please refer to the HX8363-A Datasheet

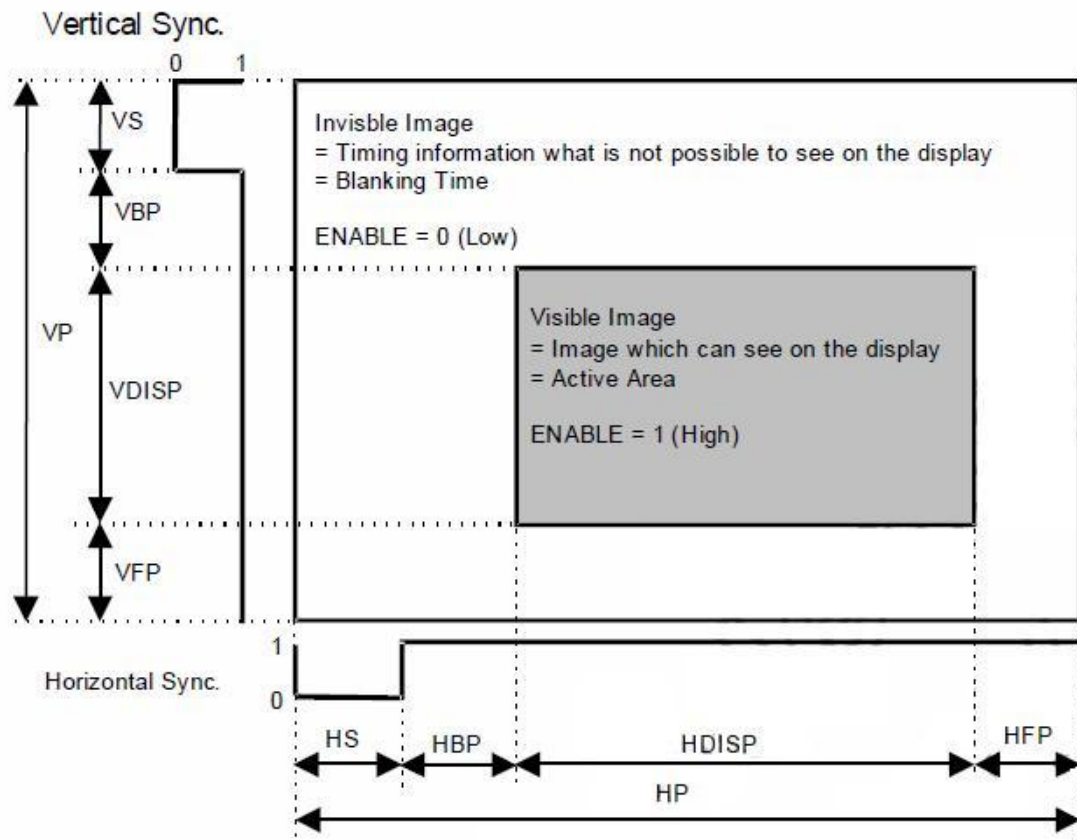
7. Electrical Characteristics

7.1 RGB Interface



The interface is active after power on sequence. Pixel clock (DCK) runs all the time with out stopping and it is used to enter HSYNC, VSYNC, ENABLE, DB[23:0],- lines state when there is a rising edge of the DCK. The DCK cannot be used as continues internal clock for other functions of the display module e.g. Sleep in-mode etc.

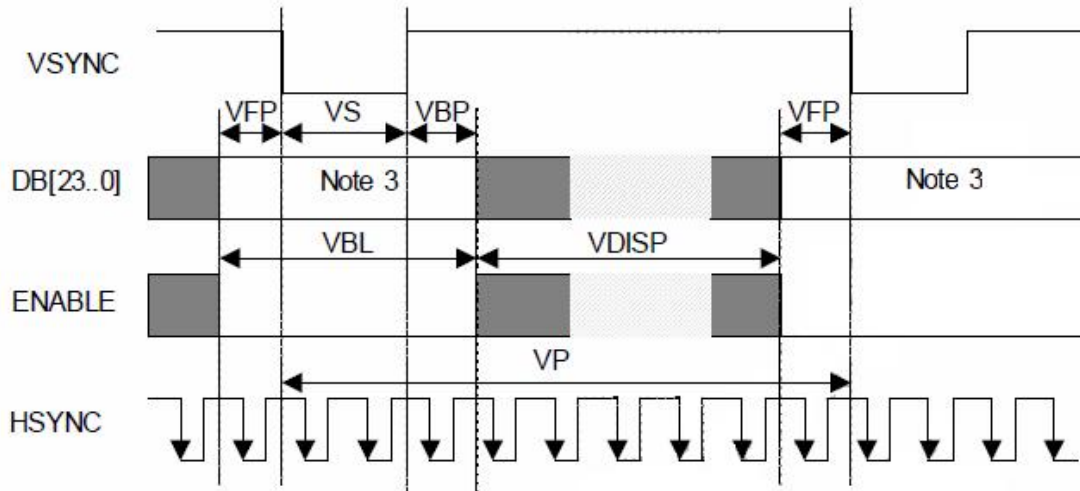
7.2 AC Characteristics (RGB Interface Timing Characteristics)



Note. The image information must be correct on the display, when the timings are in range on the interface. However, the image information might be incorrect on the display, when timings are out of the range on the interface (Out of range timings cannot cause any damage on the display module or it cannot cause damage on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync), when there is returned from out of the range to range interface timings.

7.3 RGB Interface Characteristics

Vertical Timings for RGB I/F



Resolution=480x800, VCC=2.3~3.3V, Ta=-30~70°C

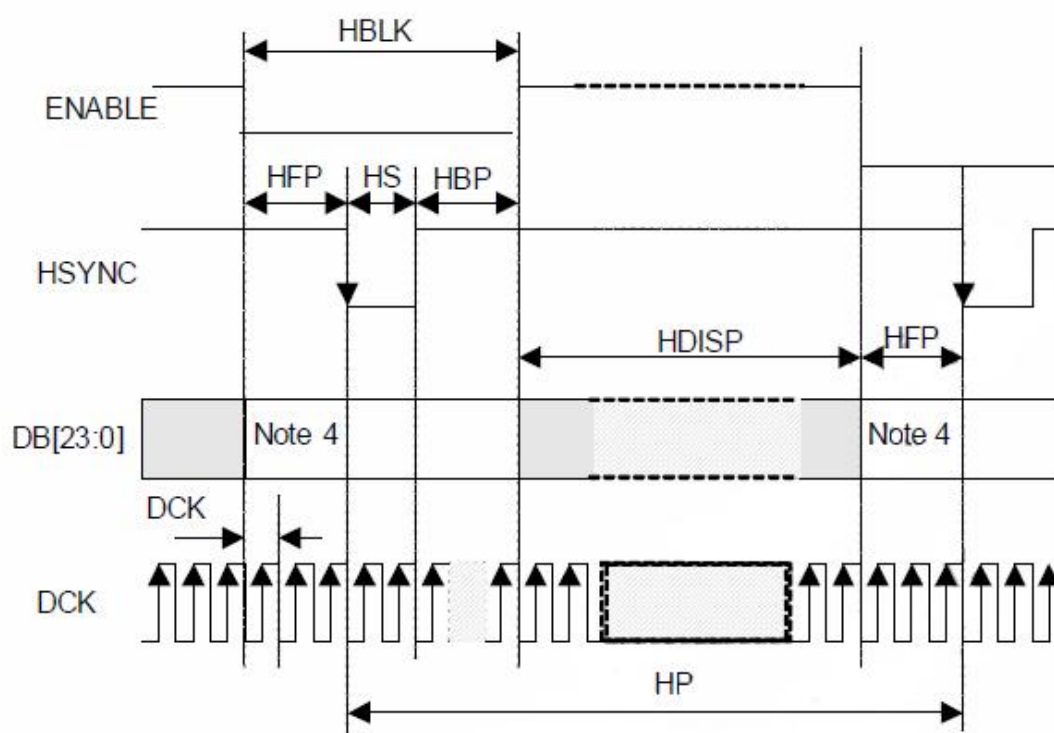
Item	Symbol	Condition	Min.	Typ.	Max	Unit
Vertical cycle	VP	--	806	--	810	Line
Vertical low pulse width	VS	--	2	--	4	Line
Vertical front porch	VFP	--	2	--	4	Line
Vertical back porch	VBP	--	2	--	4	Line
Vertical data start point	--	VS+VBP	4	--	8	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	--	10	Line
Vertical active area	--	VDSIP	--	800	--	Line
Vertical Refresh rate	VRR	--	50	--	70	Hz

Note: (1) Signal rise and fall times are equal to or less than 20ns.

(2) Input signal are measured by 0.30 x VCC for low state and 0.70 x VCC for high state.

(3) Data Lines can be set to "High" or "Low" during blanking time-Don't care

(4) VRR must keep from 50Hz to 70Hz when adjust other items



Resolution=480x800, VCC=2.3~3.3V, Ta=-30~70°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS cycle	HP	--	504	--	568	DCK
HS pulse width	HS	--	5	--	78	DCK
Horizontal front porch	HFP	--	5	--	78	DCK
Horizontal back porch	HBP		5	--	78	DCK
Horizontal data start point	--	HS+HBP	19	--	83	DCK
			700	--	--	ns
Horizontal blanking period	HBLK	HS+HBP+HFP	24	--	88	Line
Horizontal active area	HDISP	--	--	480	--	Line
Horizontal Refresh rate	DCK	VRR=Min.50Hz -Max.70Hz	20.3	--	32.2	MHz
			31		49.2	ns

Note: (1) Signal rise and fall times are equal to or less than 20ns.

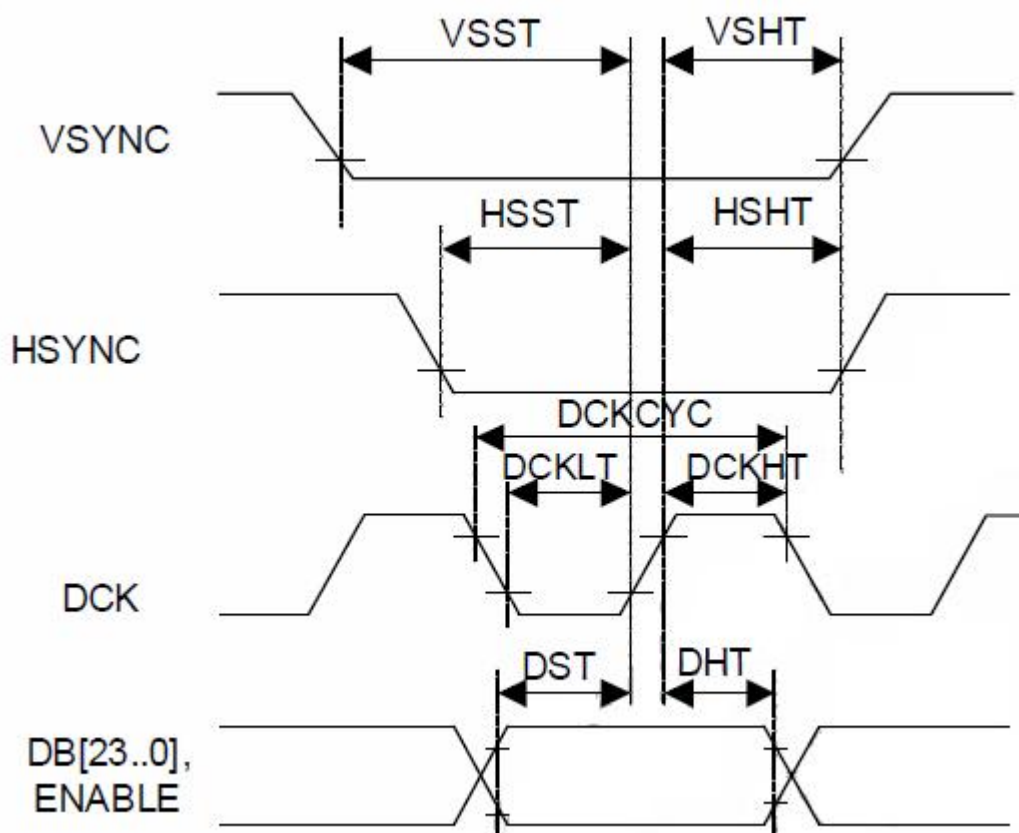
(2) Input signal are measured by 0.30 x VCC for low state and 0.70 x VCC for high state.

(3) Data Lines can be set to "High" or "Low" during blanking time-Don't care

(4) DCK must keep from 20.3Hz to 32.2Hz when adjust other items.

(5) HP is multiples of eight DCK.

7.4 General Timings for RGB I/F



Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. Step time	VSST	--	5	--	--	ns
Vertical sync. Hold time	VSHT	--	5	--	--	ns
Horizontal sync. Step time	HSST	--	5	--	--	ns
Horizontal sync. Hold time	HSHT	--	5	--	--	ns
Pixel clock cycle when RGB I/F is running	DCKCYC	VRR=Min.50Hz -Max.70Hz	31 Note3	--	49.2 Note4	ns
Pixel clock low time	DCKLT	--	5	--	--	ns
Pixel clock high time	DCKHT	--	5	--	--	ns
Data Setup time DB[23:0]	DST	--	5	--	--	MHz
Data Hold time DB[23:0]	DHT	--	5	--	--	ns

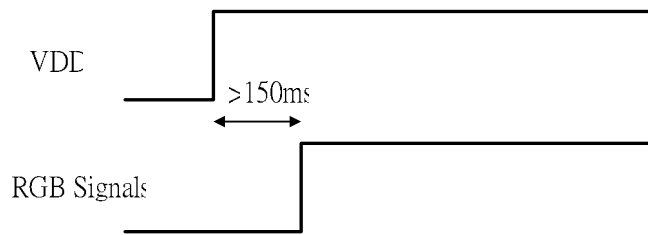
Note: (1) Signal rise and fall times are equal to or less than 20ns.

(2) Input signal are measured by 0.30 x VCC for low state and 0.70 x VCC for high state.

(3) 32.2 MHz

(4) 20.3 MHz

7.5 Power sequence for RGB I/F



Note: RGB Signals must less than VDD 150ms for initialize HX8363.

7.6 Initial Code

```
void HX8363A_HX5186_init_CMO(void)
{
//RESET();
Delay_HX8363(10);    //----- 10ms

//Set_EXTC
SPI_3W_SET_CMD(0xB9);    //Enable extention command
SPI_3W_SET_PAs(0xFF);
SPI_3W_SET_PAs(0x83);
SPI_3W_SET_PAs(0x63);

//Set_POWER
SPI_3W_SET_CMD(0xB1);    //Set power
SPI_3W_SET_PAs(0x81);    //Enter standby mode
SPI_3W_SET_PAs(0x30);
SPI_3W_SET_PAs(0x07);
SPI_3W_SET_PAs(0x34);
SPI_3W_SET_PAs(0x02);
SPI_3W_SET_PAs(0x13);
SPI_3W_SET_PAs(0x11);
SPI_3W_SET_PAs(0x00);
SPI_3W_SET_PAs(0x3A);
SPI_3W_SET_PAs(0x42);
SPI_3W_SET_PAs(0x3F);
```

```
SPI_3W_SET_PAs(0x3F);

//Sleep_Out
SPI_3W_SET_CMD(0x11);
Delay_HX8363(120);//----- 120ms

//Set_COLMOD
SPI_3W_SET_CMD(0x3A);
SPI_3W_SET_PAs(0x50); //Set data bit

//Set_RGBIF
SPI_3W_SET_CMD(0xB3);
SPI_3W_SET_PAs(0x01); //Enable RGB I/F

//Set_CYC
SPI_3W_SET_CMD(0xB4); //refer DS page 168
SPI_3W_SET_PAs(0x08);
SPI_3W_SET_PAs(0x12);
SPI_3W_SET_PAs(0x72);
SPI_3W_SET_PAs(0x12);
SPI_3W_SET_PAs(0x06);
SPI_3W_SET_PAs(0x03);
SPI_3W_SET_PAs(0x54);
SPI_3W_SET_PAs(0x03);
SPI_3W_SET_PAs(0x4E);
SPI_3W_SET_PAs(0x00);
SPI_3W_SET_PAs(0x00);

//Set_PTBA
SPI_3W_SET_CMD(0xBF);
SPI_3W_SET_PAs(0x00);
SPI_3W_SET_PAs(0x10);

//Set_VCOM
SPI_3W_SET_CMD(0xB6); //Set VOM
SPI_3W_SET_PAs(0x12);
```

```
//Set_PANEL
SPI_3W_SET_CMD(0xCC);
SPI_3W_SET_PAs(0x03); // bit0 "0" RGB Type , "1" BGR Type
                        // bit1 "0" Normal-White , "1" Normal-Black
Delay_HX8363(10); //-----10ms
//Set Gamma 2.2
SPI_3W_SET_CMD(0xE0);
SPI_3W_SET_PAs(0x00);
SPI_3W_SET_PAs(0x80);
SPI_3W_SET_PAs(0x00);
SPI_3W_SET_PAs(0x8C);
SPI_3W_SET_PAs(0x13);
SPI_3W_SET_PAs(0xA7);
SPI_3W_SET_PAs(0x05);
SPI_3W_SET_PAs(0x0D);
SPI_3W_SET_PAs(0x50);
SPI_3W_SET_PAs(0x14);
SPI_3W_SET_PAs(0x16);
SPI_3W_SET_PAs(0x55);
SPI_3W_SET_PAs(0x16);
SPI_3W_SET_PAs(0x87);
SPI_3W_SET_PAs(0x03);
SPI_3W_SET_PAs(0x00);
SPI_3W_SET_PAs(0x80);
SPI_3W_SET_PAs(0x00);
SPI_3W_SET_PAs(0x8C);
SPI_3W_SET_PAs(0x13);
SPI_3W_SET_PAs(0xA7);
SPI_3W_SET_PAs(0x05);
SPI_3W_SET_PAs(0x0D);
SPI_3W_SET_PAs(0x50);
SPI_3W_SET_PAs(0x14);
SPI_3W_SET_PAs(0x16);
SPI_3W_SET_PAs(0x55);
SPI_3W_SET_PAs(0x16);
```

```
SPI_3W_SET_PAs(0x87);  
SPI_3W_SET_PAs(0x03);  
Delay_HX8363(10);    //-----10ms
```

```
//Display On  
SPI_3W_SET_CMD(0x29);  
}
```

8.QUALITY AND RELIABILITY

8.1. Scope

Specifications contain

8.1.1 Display Quality Evaluation

8.1.2 Mechanics Specification

8.2. Sampling Plan

Unless there is other agreement, the sampling plan for incoming inspection shall

follow MIL-STD-105E LEVEL II.

8.2.1 Lot size: Quantity per shipment as one lot

(different model as different lot).

8.2.2 Sampling type: Normal inspection, single sampling.

8.2.3 Sampling level: Level II.

8.2.4 AQL: Acceptable Quality Level

Major defect: AQL=0.65

Minor defect: AQL=1.0

8.3. Panel Inspection Condition

8.3.1 Environment:

Room Temperature: $25\pm 5^{\circ}\text{C}$.

Humidity: $65\pm 5\%$ RH.

Illumination: 300 ~ 700 Lux.

8.3.2 Inspection Distance:

35-40 cm

8.3.3 Inspection Angle:

The vision of inspector should be perpendicular to the surface of the Module.

8.3.4 Inspection time :

Perceptibility Test Time: 20 seconds max.

8.4. Display Quality

8.4.1 Function Related:

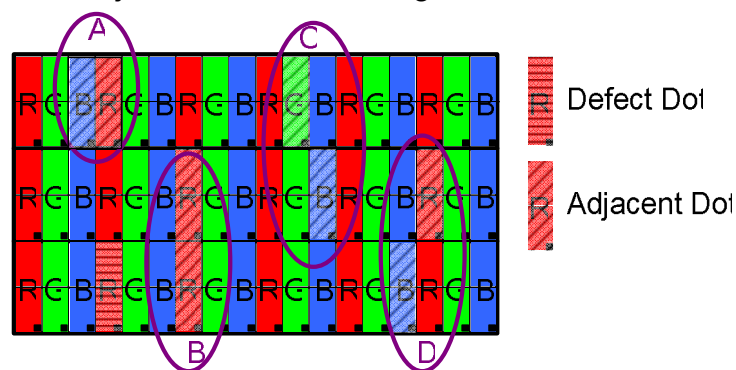
The function defects of line defect, abnormal display, and no display are considered Major defects.

8.4.2 Bright/Dark Dots:

Defect Type / Specification	G0 Grade	A Grade
Bright Dots	0	$N \leq 1$
Dark Dots	0	$N \leq 3$
Total Bright and Dark Dots	0	$N \leq 3$

[Note 1]

Judge defect dot and adjacent dot as following.

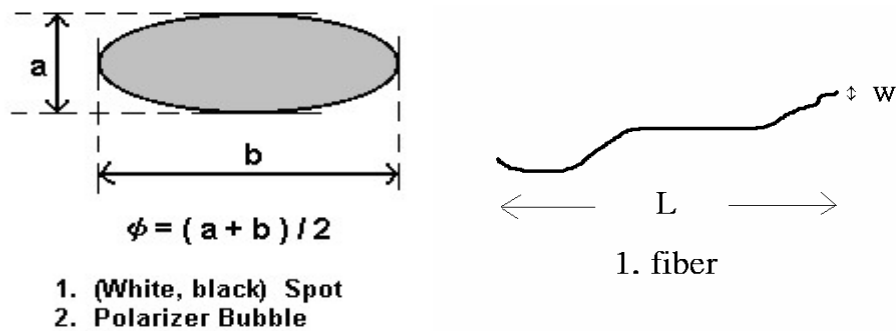


- (1) One pixel consists of 3 sub-pixels, including R,G, and B dot.(Sub-pixel = Dot)
- (2) The definition of dot: The size of a defective dot over 1/2 of whole dot is regarded as one defective dot.
- (3) Allow above (as A, B, C and D status) adjacent defect dots, including bright and dart adjacent dot. And they will be counted 2 defect dots in total quantity.
- (4) Defects on the Black Matrix, out of Display area, are not considered as a defect or counted.
- (5) There should be no distinct non-uniformity visible through 6% ND Filter within 2 sec inspection times.

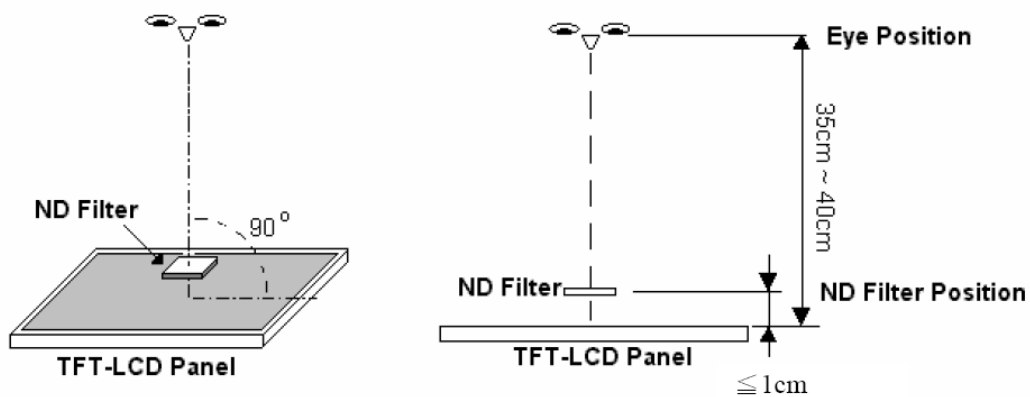
8.4.3 Visual Inspection specifications:

Defect Type	Specification	Count(N)
Dot Shape (Particle, Scratch and Bubbles in display area)	$D \leq 0.15\text{mm}$	Ignored
	$0.15\text{mm} < D \leq 0.3\text{mm}$	$N \leq 3$
	$D > 0.3\text{mm}$	$N=0$
Line Shape (Particles, Scratch, Lint and Bubbles in display area)	$W \leq 0.05\text{mm}$	Ignored
	$0.05\text{mm} < W \leq 0.1\text{mm}$, $L \leq 3\text{mm}$	$N \leq 3$
	$W > 0.1\text{mm}$, $L > 3\text{mm}$	$N=0$

[Note 2] W : Width[mm], L : Length[mm], N : Number, ϕ : Average Diameter



[Note 3] Bright dot is defined through 6% transmission ND Filter as following.



9 RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=72 hrs	
Low Temperature Operation	-20±3°C , t=72 hrs	
High Temperature Storage	80±3°C , t=72hrs	1,2
Low Temperature Storage	-30±3°C , t=72 hrs	1,2
Humidity Test	TBD	1,2
Thermal Shock Test	TBD	1,2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

10 USE PRECAUTIONS

10.1 Handling precautions

- 1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
- 2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
- 3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
- 4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

10.2 Installing precautions

- 1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. $1M\Omega$ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
- 2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
- 3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
- 4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

10.3 Storage precautions

- 1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
- 2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
- 3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

10.4 Operating precautions

- 1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
- 2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
- 3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC drive voltage.
- 4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
- 5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
- 6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.

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- 7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.
 - 8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

10.5 Other

- 1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
- 2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.
- 3) AMIPRE will provide one year warrantee for all products and three months warrantee for all repairing products.

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