

DATA SHEET



OTM9608A

**1620-channel 8-bit Source Driver and
960 Gate Driver with System-on-chip
for Color Amorphous TFT-LCDs**

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1620-CHANNEL Source DRIVER and 640 Gate Driver WITH SYSTEM-ON-CHIP (SOC) FOR Color Amorphous TFT LCD

1. GENERAL DESCRIPTION

The OTM9608A, a 16,777,216-color System-on-Chip (SoC) driver LSI designed for small and medium sizes of TFT LCD display, is capable of supporting up to 540xRGBx960 (qHD) in resolution which can be achieved by the integrated RAM for graphic data. The 540-channel source driver has true 8-bit resolution, which generates 256 Gamma-corrected values by an internal D/A converter.

The OTM9608A is able to operate with low IO interface power supply and incorporate with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and source driver.

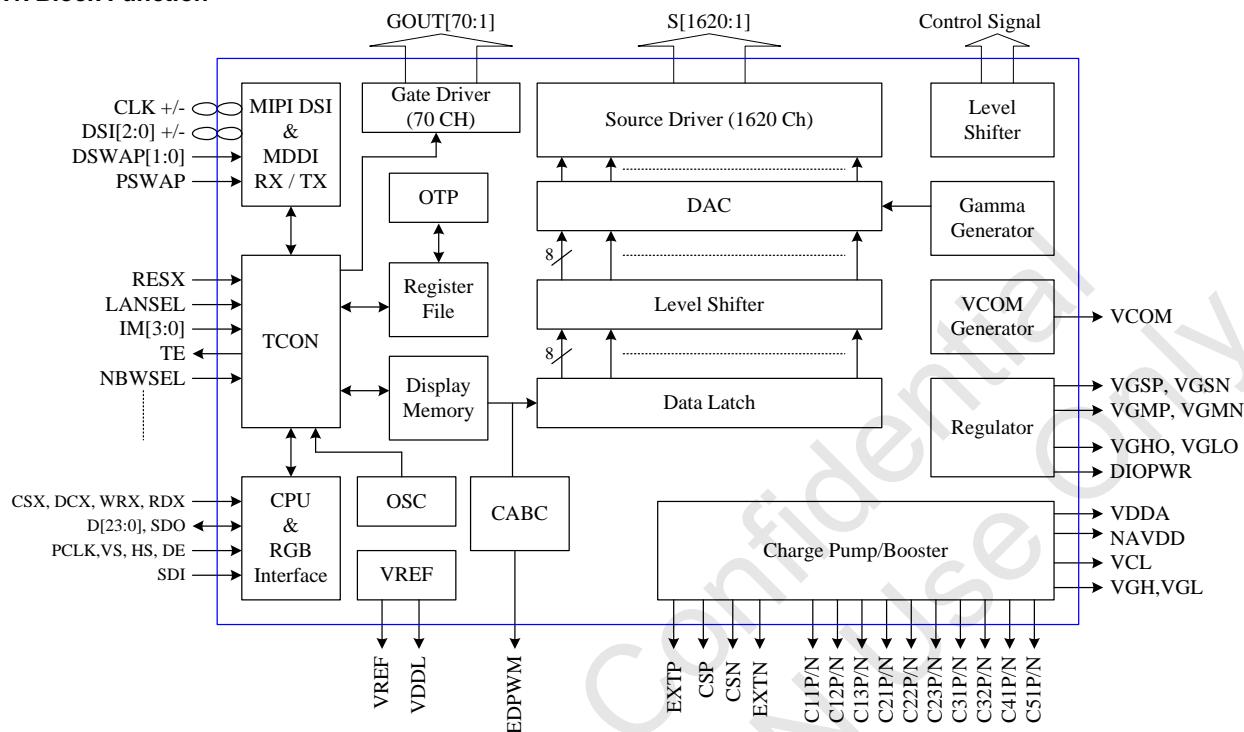
The built-in timing controller in OTM9608A can support several interfaces for the diverse request of medium or small size portable display. OTM9608A provides several system interfaces, which include MIPI/MDDI/CPU/RGB. Not only can the system interfaces be used to configure system, they can also access RAM at high speed for still picture display. The OTM9608A also supports a function to display eight colors and a standby mode for power control consideration. For further power control, the dynamic backlight control function basing on displaying image content is also supported.

2. FEATURES

- One-chip solution for color amorphous TFT-LCD.
- Support various resolution
 - 540XRGBX960(qHD).
 - 480XRGBX960
 - 480XRGBX800(WVGA).
 - 480XRGBX854(WVGA)
 - 480XRGBx864(WVGA)
- Outputs 256y-corrected values using an internal true 8-bit resolution D/A converter to achieve 16,777,216 colors
- Built-in digital separate RGB gamma
- Built-in single full video RAM with support up to qHD.
- Built-in DC-VCOM.
- System interfaces
 - MIPI DSI (1/2/3 data lane) : transmission bit rate up to 550 Mb/s per data channel.
*MIPI DSI (DSI v1.01.00, D-PHY v1.00.00 and DCS v1.01).
 - MDDI (2 lane) : . transmission bit rate up to 550 Mb/s per data channel.
 - CPU (8/16/24) interface
 - RGB (24) interface
- Diverse RAM accessing for functional display
 - Window address function to display at any area on the screen via a moving picture display interface
 - Window address function to limit the data rewriting area and reduce data transfer
 - Moving and still picture can display at the same time.
 - Partial / Window screen display
- Power supply
 - Logic power supply voltage (VDDIO): 1.1 ~ 1.3 V : 1.65 ~ 3.3V
 - Analog power supply voltage (VPNL): 2.3 ~ 4.8V
- On-chip power management system
 - Power saving mode (standby / 8-color mode, etc)
 - Low power consumption structure for source driver.
 - Dynamic backlight control function.
- Built-in Charge Pump circuits
 - Source output voltage level GVDD-GVSS: 3.1125 ~ 6.3V
NGVDD-NGVSS: -3.1125 ~ --6.3V
- Built-in internal oscillator and hardware reset.
- Built-in MTP (4 Times) to store VCOM calibration and ID1~ID3.

3. BLOCK DIAGRAM

3.1. Block Function



3.1.1. System interface

The OTM9608A supports the high-speed system interface, MIPI (Mobile Industry Processor Interface), and MDDI, also support I²S and RGB interface.

The OTM9608A has a index register (IR) for MIPI (8-bit) and two data registers, a write-data register (WDR) and a read-data register (RDR). The IR register is used to store index information from control registers. The WDR register is used to temporarily store data to be written for register control and internal GRAM. The RDR register is used to temporarily store data read from the GRAM. When graphic data is written to the internal GRAM from MCU/graphic engine, the data is first written to the WDR and then automatically written to the internal GRAM in internal operation. When graphic data read operation is executed, graphic data is first read to the RDR from the internal GRAM by internal generated read operation pulse. Therefore, valid data can be read out right after the OTM9608A executes the 1nd read operation.

3.1.2. Address Counter (AC)

OTM9608A features an Address Counter (AC) giving an address to the internal GRAM. The address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

3.1.3. Graphics RAM (GRAM)

OTM9608A features a 1555200-byte (540 x 960 x 24 / 8) Graphic RAM (GRAM).

3.1.4. Grayscale voltage generating circuit

OTM9608A has true 8-bit resolution D/A converter, which generates 256 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the y-correction register and RGB can be adjusted separately.

3.1.5. Timing controller

OTM9608A has a timing controller, which can generate a timing signal for internal circuit operation such as gate output timing, RAM accessing timing, etc.

3.1.6. Oscillator (OSC)

The OTM9608A also features an internal oscillator to generate RC oscillation with an internal resistor. In standby mode, RC oscillation is halted to reduce power consumption.

3.1.7. Source driver circuit

OTM9608A consists of a 1620-output source driver circuit (S1 ~ S1620). Data in the GRAM are latched when a single line data has been accumulated. And, then the latched data controls the source driver and generates a drive waveform.

3.1.8. Gate driver circuit

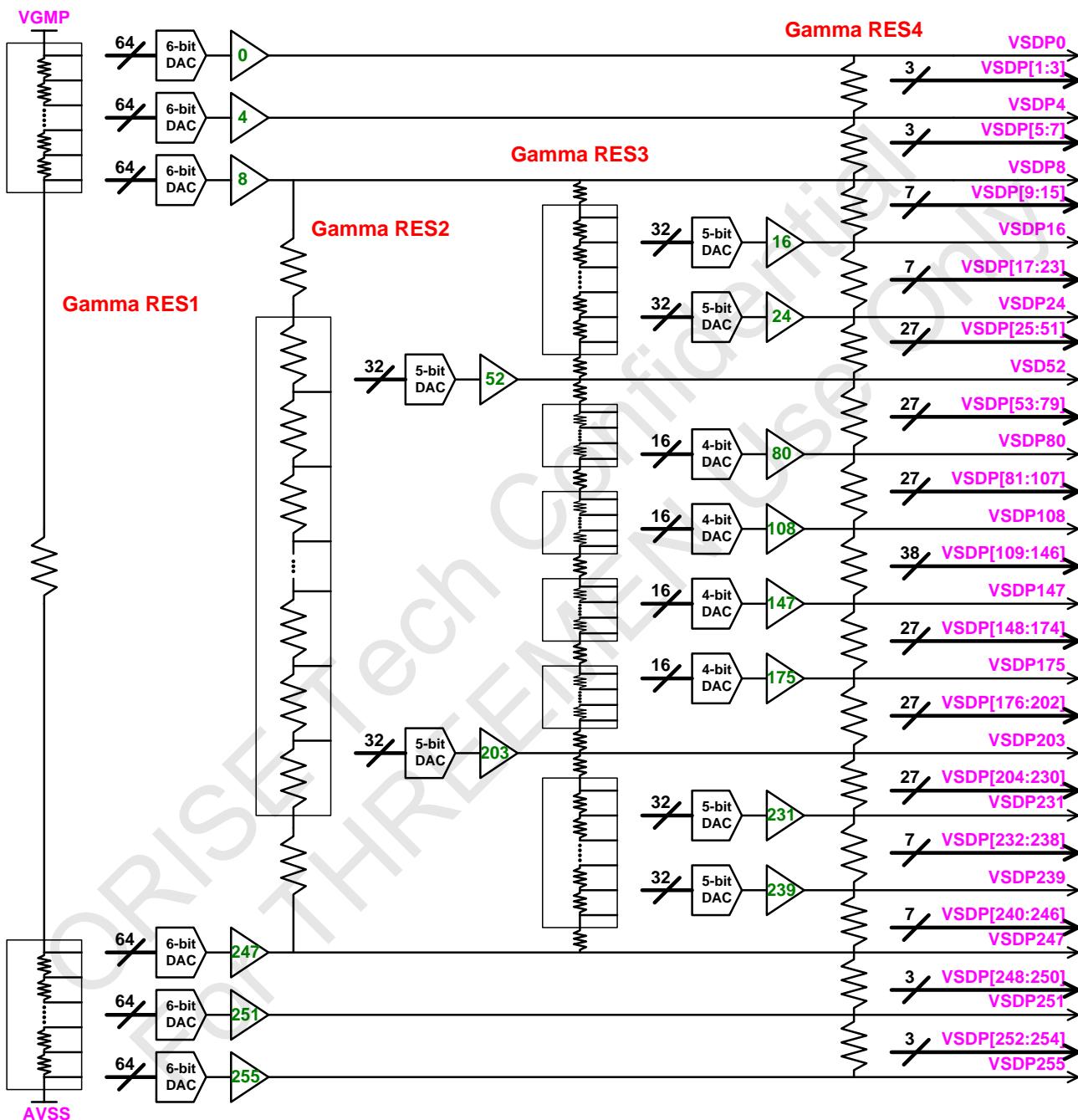
OTM9608A consists of output gate driver control circuit. The gate driver circuit outputs gate driver signals at either VGH or VGL level.

3.1.9. LCD driving power supply circuit

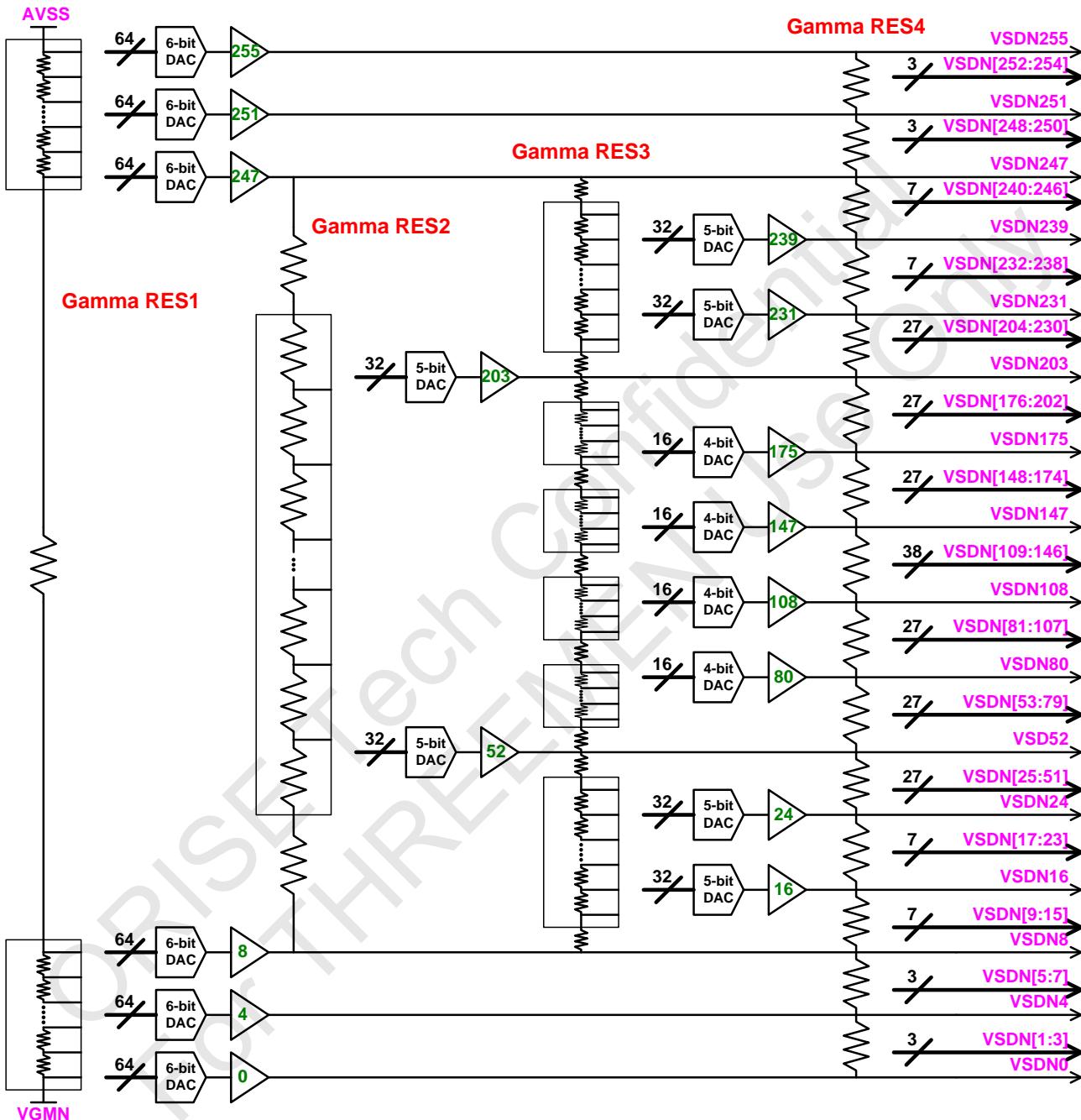
The LCD driving power supply circuit generates the voltage levels AVDD, VGH, VGL and VCOM for driving an LCD. All this voltages can be adjusted by register setting.

3.2. Gamma Correction Circuit

3.2.1. Positive gamma correction circuit



3.2.2. Negative gamma correction circuit



4. SIGNAL DESCRIPTIONS

4.1. Pin Definition

Signal	I/O	PAD Type (Voltage Level)	Function			
Global Control Signal						
IM[3:0]	I	Digital (VDDIO)	Interface mode select pins. Notes: (1). Frame buffer writing by MDDI and register reading (or writing) by SPI(or I2C) could work at the same time. (2). When MDDI is in stand-by mode, the SPI(or I2C) can also read / write registers and frame buffer. (3). MDDI could read / write registers and frame buffer only when SPI (or I2C) is inactive.			
			External Pad Set			
			IM3	IM2	IM1	IM0
			0	0	0	0
			0	0	0	1
			0	0	1	0
			0	0	1	1
			1	0	1	1
			0	1	0	0
			0	1	0	1
			0	1	1	0
			1	1	1	0
			0	1	1	1
			Interface format			
			CPU 8bit			
			CPU 16bit			
			CPU 24bit			
			RGB + Serial Interface (SCL rising edge trigger)			
			RGB + Serial Interface (SCL falling edge trigger)			
			MIPI-DSI			
			MDDI + SPI (SCL rising edge trigger)			
			MDDI + SPI (SCL falling edge trigger)			
			MDDI + I2C			
			RGB + I2C			
LANSEL	I	Digital	MIPI-DSI Lane no. Select Lane_SEL = "1", MIPI-DSI is 3 Lane mode Lane_SEL = "0", MIPI-DSI is 2 Lane mode			
ERR	O	Digital	ECC and CRC error flag for MIPI-DSI. It outputs high if ECC/CRC error occurs. It outputs Low always if not activated. Let it open if not used.			
RESX	I	Digital	Global Reset Signal. Active Low. If not used please let it floating.			
TE_L	O	Digital	Tearing effect output pin to synchronizes MCU to frame writing, activated by S/W command. When this pin is not activated (TE function OFF), this pin is VSS level.			
TE_R	O	Digital	Tearing effect output pin to synchronizes MCU to frame writing, activated by S/W command. When this pin is not activated (TE function OFF), this pin is VSS level.			
LEDPWM	O	Digital	LCD backlight control PWM output pin			
LEDON	O	Digital	Enable pulse for the backlight driver			
VSEL	I	Digital	DIOPWR voltage select "Low" = 1.2V IO mode "High" = 1.8V IO mode			

Signal	I/O	PAD Type (Voltage Level)	Function										
EXBIT	I	Digital	DCDC mode for VDDA										
			<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>EXBIT</th><th>Mode</th></tr> <tr> <td>0</td><td>Charge pump mode</td></tr> <tr> <td>1</td><td>Coil Booster mode</td></tr> </table>					EXBIT	Mode	0	Charge pump mode	1	Coil Booster mode
EXBIT	Mode												
0	Charge pump mode												
1	Coil Booster mode												
I2C_SA0	I	Digital	Selection of I2C slave address Connect to VSS if not used. 0 : slave address=1001100, 1 : slave address=1001101										
NBWSEL	I	Digital	Selection for NB(Normally Black)/NW(Normally White) panel. 0 : NW, 1 : NB										
DSTB_SEL	I	Digital	Control pin for DIOPWR regulator. 0 : not used , 1 : used for TE/LEDON/LEDPWM.										
PSWAP	I	Digital	Polarity swapping										
DSWAP[1:0]	I	Digital	Data Lanes swapping The attached is Polarity/Data-bus swap table for 2/3 lanes										
MIPI/MDDI 3CH				DSWAP[1:0]		DSWAP[1:0]							
				00	10	00	10						
3-lane				PSWAP		0							
				CH2	DP	D2P	D1P						
				DN	D2N	D1N	D2P						
				CH0	DP	D0P	D0P						
				DN	D0N	D0N	D0P						
				CLK	CLKP	CLKP	CLKN						
				CLKN	CLKN	CLKN	CLKP						
				CH1	DP	D1P	D2P						
				DN	D1N	D2N	D1P						
				DN	D2P	D1N	D2N						
				DN	D1P	D2N	D2P						
MIPI/MDDI 2CH				DSWAP[1:0]		DSWAP[1:0]							
				00	01	00	01						
2-lane				PSWAP		0							
				CH2	DP								
				DN									

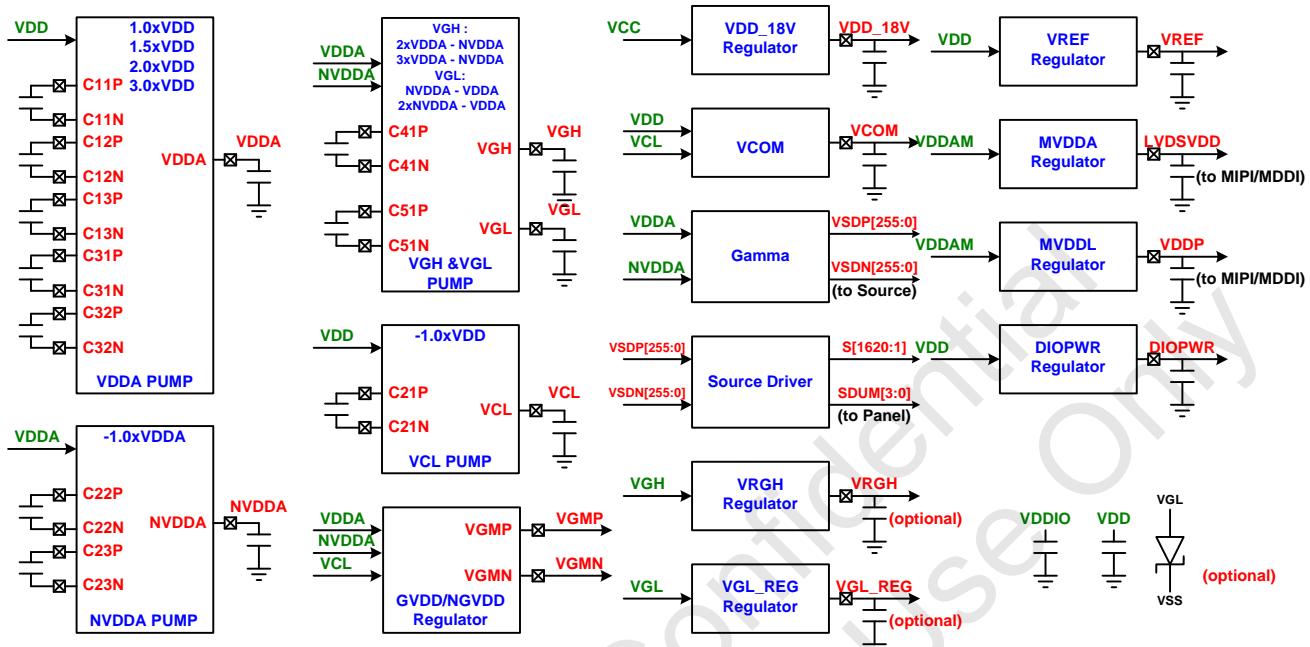
Signal	I/O	PAD Type (Voltage Level)	Function						
			CH0	DP	D0P	D1P	D0N	D1N	
				DN	D0N	D1N	D0P	D1P	
			CLK	CLKP	CLKP	CLKP	CLKN	CLKN	
				CLKN	CLKN	CLKN	CLKP	CLKP	
			CH1	DP	D1P	D0P	D1N	D0N	
				DN	D1N	D0N	D1P	D0P	
GPO[3:0]	I/O	Digital	GPO2 is used as Hsync output. The other pins can be open.						
MIPI-DSI/ MDDI Interface Signals									
CLK-STB+	I	MIPI/MDDI (LVDSVDD)	MIPI-DSI clock Lane positive-end input pin/ MDDI strobe Lane positive-end input pin						
CLK-STB-	I	MIPI/MDDI (LVDSVDD)	MIPI-DSI clock Lane negative-end input pin/ MDDI strobe Lane negative-end input pin						
DSI-D0+	I/O	MIPI/MDDI (LVDSVDD)	MIPI-DSI data Lane 0 positive-end input/output pin/ MDDI data Lane 0 positive-end input/output pin * Please connected to LVDSVSS if not used						
DSI-D0-	I/O	MIPI/MDDI (LVDSVDD)	MIPI-DSI data Lane 0 negative-end input/output pin/ MDDI data Lane 0 negative-end input/output pin * Please connected to LVDSVSS if not used						
DSI-D1+	I	MIPI/MDDI (LVDSVDD)	MIPI-DSI data Lane 1 positive-end input pin/ MDDI data Lane 1 positive-end input pin * Please connected to LVDSVSS if not used						
DSI-D1-	I	MIPI/MDDI (LVDSVDD)	MIPI-DSI data Lane 1 negative-end input pin/ MDDI data Lane 1 negative-end input pin * Please connected to LVDSVSS if not used						
DSI-D2+	I	MIPI/MDDI (LVDSVDD)	MIPI-DSI data Lane 2 positive-end input pin/ MDDI data Lane 2 positive-end input pin * Please connected to LVDSVSS if not used						
DSI-D2-	I	MIPI/MDDI (LVDSVDD)	MIPI-DSI data Lane 2 negative-end input pin/ MDDI data Lane 2 negative-end input pin * Please connected to LVDSVSS if not used						
MPU/ RGB/ SPI/ I2C Interface									
CSX	I	Digital (VDDIO)	Chip select signal. "0" : the OTM9608A is accessible "1" : the OTM9608A is not accessible This pin can be permanently fixed "0" in MCU interface mode only.						
DCX	I	Digital (VDDIO)	Display data / Command selection pin in parallel interface "0" : Command data "1" : Display data Must connect to the VSS or VDDIO level when not used.						
WRX/ R_WX/ SCL/ I2C_SCL	I	Digital (VDDIO)	In MPU interface mode, a write strobe signal can be input via this pin and initializes a write operation when the signal is low. Must connect to the VSS or VDDIO level when not used. [Serial-IF] SCL: Serial interface Clock Input						

Signal	I/O	PAD Type (Voltage Level)	Function
			[I2C-IF]I2C_SCL:Serial Clock input
RDX/E	I	Digital (VDDIO)	In MPU interface mode, a read strobe signal can be input via this pin and initializes a read operation when the signal is low. Must connect to the VSS or VDDIO level when not in use.
D[23:0]	I/O	Digital (VDDIO)	MPU/RGB I/F Data Input/Output. If not in use, it can be open or connect them to ground
DE	I	Digital (VDDIO)	RGB interface Data Enable Input. If not in use, it can be open or connect it to ground
PCLK	I	Digital (VDDIO)	RGB interface Pixel clock Input. If not in use, it can be open or connect it to ground
HS	I	Digital (VDDIO)	RGB interface Hsync. Input. If not in use, it can be open or connect it to ground
VS	I	Digital (VDDIO)	RGB interface Vsync. Input. If not in use, it can be open or connect it to ground
SDI/ I2C_SDA	I	Digital (VDDIO)	[Serial-IF]SDI :Serial interface DATA Input [I2C-IF]I2C_SDA:Serial data input. If not in use, it can be open or connect it to ground
SDO	O	Digital (VDDIO)	Serial interface DATA output
Source/Panel control and VCOM Signals			
S[1620:1]	O	Analog	Output source driver signals. The D/A converted 256-gray-scale analog voltage is output.
GOUT[70:1]	O	Analog	Gate control signals for panel
SDUM0 ~SDUM3	O	Analog	Source dummy output
VCOM	O	Analog	VCOM signal output
Test/ Debugging/ Dummy Pins			
PADA[7:1]	I/O		For bonding resistance measurement. There are two groups of pins, they are(1). (PADA1, PADA2). (2). (PADA3, PADA5, PADA6) and (PADA4, PADA7). The pins in each groups are short together.
PADB[7:1]	I/O		For bonding resistance measurement. There are two groups of pins, they are (1). (PADB1, PADB2) (2). (PADB3, PADB5, PADB6), and (PADB4, PADB7). The pins in each groups are short together.
TEST[7:0]	I/O		Test pin. please let them float.
OSC_TEST	I/O		Test pin. please let them float.
GDUM[12:1]			Dummy pins, Hi-Z state
VSSIDUM[1:0]	O		Dummy pins, with VSS potential
AVSSDUM[36:0]	O		Dummy pins, with AVSS potential
VREFCP		Analog	Dummy pin, no driving
LVGL		Analog	Dummy pin, no driving.
RGBBP	I	Digital	Test pin. Connect it with fixed VDDIO/VSS voltage level.
VGSW[3:0]	I	Digital	Test pin. Connect it with fixed VDDIO/VSS voltage level.
3D_CLK0	O	Digital	Test pin. If not in use, please let it open.
3D_CLK1	O	Digital	Test pin. If not in use, please let it open
3D_CLK2	O	Digital	Test pin. If not in use, please let it open
3D_CLK3	O	Digital	Test pin. If not in use, please let it open

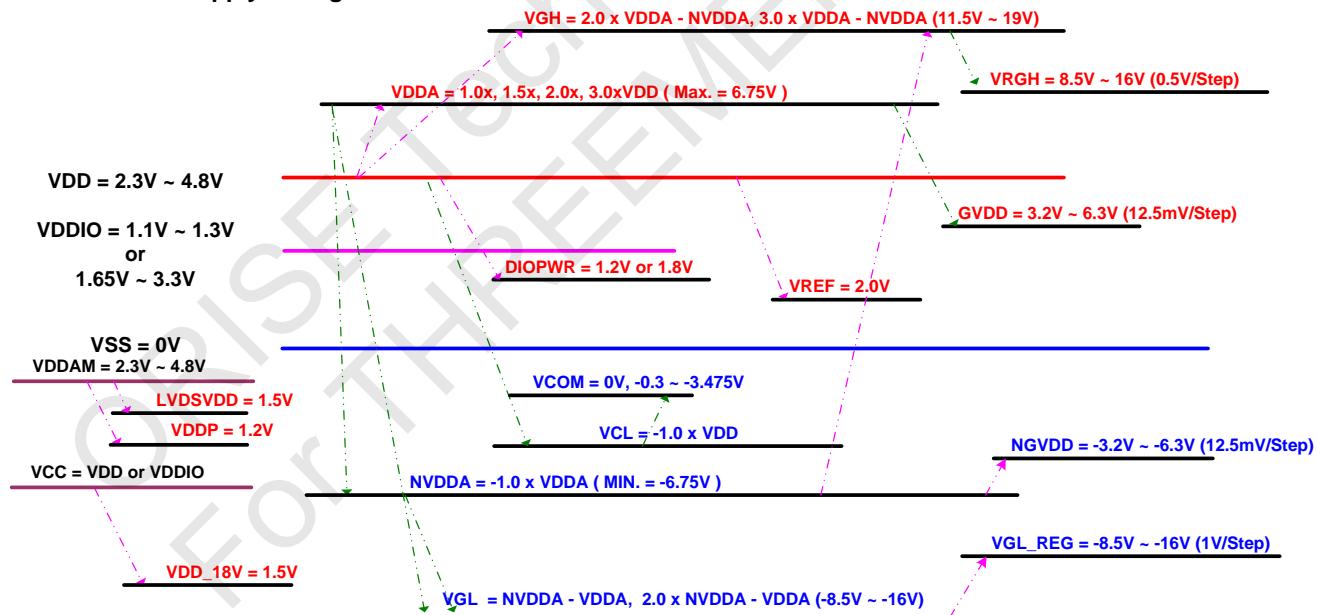
Signal	I/O	PAD Type (Voltage Level)	Function
D22P/N	O	Analog	Dummy pins
Charge Pump Capacitor			
C11P/N, C12P/N C13P/N, C21P/N C22P/N, C23P/N, C31P/N C32P/N, C41P/N, C51P/N	C	Step-up capacitor	Connect boost capacitors for the internal DC/DC converter circuit to these pins. Leave the pins open when DC/DC converter circuits are not used.
Power Supply and Regulator pins			
VCC	I	Power Supply	Power supply to the internal logic power regulator circuit (VCC=2.3 to 4.8V)
VDD	I	Power Supply	Power Supply input for analog circuit.
VDDIO (VDDIOL)	I	Power Supply	External Power Supply for Digital Circuits and IO pads. VDDIO=1.65 to 3.3V VDDIOL=1.1V to 1.3V
MTP_PWR	I	Power Supply	- Input power for NV memory programming - Input power range : 7.25 ~ 7.75V (Typical=7.5V) - When not under programming, MTP_PWR pin can be float or tied to ground.
VDDAM	I	Power Supply	Power Supply for MIPI/MDDI regulator circuits.(VDDAM=2.3 to 4.8V)
AVSS	I	Ground	Analog Ground
VSS	I	Ground	Digital Ground
LVDSVSS	I	Ground	MIPI/ MDDI Ground
VDD_18V	O	Analog Output	Internal Power Supply for Digital Logic Circuits. Connect to a stabilizing capacitor. VDD_18V=1.5V
LVDSVDD	O	Analog Output	Internal Power Supply for MIPI/ MDDI. Connect to a stabilizing capacitor.
VDDP	O	Analog Output	LDO output for MIPI YX use(LPDT). VDDP=1.2V(Typical)
VREF	O	Analog Output	Reference Voltage Connect to a stabilizing capacitor. VREF=2.0V
DIOPWR	O	Analog Output	Internal voltage regulator output for Dual I/O. DIOPWR=1.8V or 1.2V Must connect a capacitor for stabilizing . Please refer to VSEL pin description. - Let it open if Dual I/O are NOT used
Charge Pump/ Booster / Regulator Related pins			
VDDA	O	Analog	Positive Output voltage from the step-up circuit Connect to a stabilizing capacitor.
NVDDA	O	Analog	Negative Output voltage from the step-up circuit Connect to a stabilizing capacitor.
VGH	O	Analog	Positive Output voltage from the step-up circuit
VGHO	O	Analog	Positive Power supply to gate control signal and circuit in Panel
VRGH	O	Analog	Regulator output voltage generated from VGH Connect with a stabilizing capacitor.
VGL	O	Analog	Negative Output voltage from the step-up circuit
VGLO	O	Analog	Negative Power supply to gate control signal and circuit in Panel

Signal	I/O	PAD Type (Voltage Level)	Function
VGL_REG	O	Analog	Regulator output voltage generated from VGL Connect with a stabilizing capacitor.
VGMP	O	Analog	Output voltage generated from from VDDA. It's used for positive gamma voltage.
VGMN	O	Analog	Output voltage generated from from NVDDA. It's used for negative gamma voltage.
VGSP	O	Analog	Output voltage generated from from VDDA. It's used for positive gray scale voltage.
VGSN	O	Analog	Output voltage generated from from NVDDA. It's used for negative gray scale voltage.
VCL	O	Analog	Output voltage from the step-up circuit
CSP	I	Analog	Coil Booster sensing input to generate VDDA
CSN	I	Analog	Coil Booster sensing input to generate NVDDA
EXTP	O	Analog	Coil Booster output to generate VDDA
EXTN	O	Analog	Coil Booster output to generate NVDDA
BVP3D	O	Analog	Positive regulator output voltage for 3D pins Connect with a stabilizing capacitor
BVN3D	O	Analog	Negative regulator output voltage for 3D pins Connect with a stabilizing capacitor

4.2. Power Architecture



4.3. Power Supply Configuration



4.4. BOM List

OTM9608A BOM LISTS				
NO.	Signal Name	Value	Max. Ability	Note
1	VDDIO	1.0uF	4V	I/O and Digital Power
2	VDD	2.2uF	6.3V	Analog Power
3	C11P/C11N	1.0~2.2 uF	6.3V	
4	C12P/C12N	1.0~2.2 uF	6.3V	
5	C13P/C13N	1.0~2.2 uF	6.3V	VDDA Pump
6	VDDA	2.2uF	10V	
7	C21P/C21N	1.0~2.2 uF	6.3V	VCL Pump
8	C22P/C22N	1.0~2.2 uF	6.3V	
9	C23P/C23N	1.0~2.2 uF	6.3V	NVDDA Pump
10	NVDDA	2.2uF	10V	
11	C31P/C31N	1.0~2.2 uF	6.3V	VDDA Pump
12	C32P/C32N	1.0~2.2 uF	6.3V	
13	VCL	2.2uF	6.3V	VCL Pump
14	C41P/C41N	1.0uF	16V	
15	VGH	1.0uF	25V	VGH Pump
16	C51P/C51N	1.0uF	16V	
17	VGL	1.0uF	20V	VGL Pump
18	VREF	1.0uF	4V	Regulator
19	VCOM	2.2uF	4V	VCOM
20	VDD_18V	2.2uF	4V	TCON Power
21	DIOPWR	1.0uF	4V	BC, TE, RESX Power
22	LVDSVDD	1.0uF	4V	
23	VDDP	1.0uF	4V	Mipi, RX, DSI Power
24	VGL	Schottky Diode		Optional
25	VRGH	1.0uF	20V	Optional
26	VGL_REG	1.0uF	20V	Optional

5. INSTRUCTIONS

5.1. Outline

The OTM9608A supports high speed serial interface, MIPI, MDDI, to configure system via accessing command register. When the command register is executed, sending the command information to specify which index register would be accessed and following the data to that control register. The MIPI-DSI is compliant with MIPI Alliance Standard for Display Serial Interface(DSI), Version 1.01.00 and D-PHY Version 1.00.00. And command instruction can be accomplished using all supporting system interfaces (MIPI, and I-80 24-bit parallel bus interface).

The OTM9608A has the following major categories of instructions:

- (1) System function instructions (User Command Set).
- (2) Customer Command List and Description (Manufacturer Command Set / Command 2).

These instructions are asynchronous to the OTM9608A internal clock, requiring no wait cycles. Because the writing of instruction data does not interfere with the host controller processing, instructions can be handled smoothly and efficiently. The following describes details of instruction settings.

5.1.1. System function command list and description

Table 6.1 lists all the system function commands. After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section). Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h, and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTR (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh), and Read Display Self Diagnostic Result (0Fh) of these commands are updated immediately both in Sleep In mode and Sleep Out mode.

Table 5-1 System Function command List

Command	(Hex)	Write/Read/Command	Function	Parameter Number	MIPI Transmission Mode
NOP	00	C	No Operation	0	LPDT/HSDT
SWRESET	01	C	Software reset	0	LPDT/HSDT
RDNUMED	05	R	Read Number of the Errors on DSI	1	LPDT/HSDT
RDDPM	0A	R	Read Display Power Mode	1	LPDT/HSDT
RDDMADCTL	0B	R	Read Display MADCTL	1	LPDT/HSDT
RDDCOLMOD	0C	R	Read Display Pixel Format	1	LPDT/HSDT
RDDIM	0D	R	Read Display Image Mode	1	LPDT/HSDT
RDDSM	0E	R	Read Display Signal Mode	1	LPDT/HSDT
RDDSDR	0F	R	Read Display Self Diagnostic Result	1	LPDT/HSDT
SLPIN	10	C	Sleep in	0	LPDT/HSDT
SLPOUT	11	C	Sleep out	0	LPDT/HSDT
PTLON	12	C	Partial Mode On	0	LPDT/HSDT
NORON	13	C	Normal Display Mode On	0	LPDT/HSDT
INVOFF	20	C	Display Inversion Off	0	LPDT/HSDT
INVON	21	C	Display Inversion On	0	LPDT/HSDT
ALLPOFF	22	C	All Pixels Off	0	LPDT/HSDT
ALLPON	23	C	All Pixels On	0	LPDT/HSDT
GAMSET	26	W	Gamma Set	1	LPDT/HSDT
DISPOFF	28	C	Display off	0	LPDT/HSDT
DISPON	29	C	Display on	0	LPDT/HSDT
CASET	2A	W	Column Address Set	4	LPDT/HSDT
PASET	2B	W	Page Address Set	4	LPDT/HSDT
RAMWR	2C	W	Memory Write	Any Length	LPDT/HSDT
RAMRD	2E	R	Memory Read	Any Length	LPDT/HSDT

PLTAR	30	W	Partial area	4	LPDT/HSDT
TEOFF	34	C	Tearing Effect Line Off	0	LPDT/HSDT
TEEON	35	W	Tearing Effect Line On	1	LPDT/HSDT
MADCTL	36	W	Memory Access Control	1	LPDT/HSDT
IDMOFF	38	C	Idle Mode off	0	LPDT/HSDT
IDMON	39	C	Idle Mode on	0	LPDT/HSDT
COLMOD	3A	C	Interface Pixel Format	1	LPDT/HSDT
RAMWRC	3C	W	Memory Write Continue	Any Length	LPDT/HSDT
RAMRDC	3E	R	Memory Read Continue	Any Length	LPDT/HSDT
WRTESCN	44	W	Write TE Scan Line	2	LPDT/HSDT
RDSCNL	45	R	Read Scan Line	2	LPDT/HSDT
WRDISBV	51	W	Write Display Brightness	1	LPDT/HSDT
RDDISBV	52	R	Read Display Brightness Value	1	LPDT/HSDT
WRCTRLD	53	W	Write CTRL Display	1	LPDT/HSDT
RDCTRLD	54	R	Read CTRL Display	1	LPDT/HSDT
WRCABC	55	W	Write Content Adaptive Brightness Control	1	LPDT/HSDT
RDCABC	56	R	Read Content Adaptive Brightness Control	1	LPDT/HSDT
WRCABCMB	5E	W	Write CABC Minimum Brightness	1	LPDT/HSDT
RDCABCMB	5F	R	Read CABC Minimum Brightness	1	LPDT/HSDT
RDABCSDR	68	R	Read Automatic Brightness Control Self-diagnostics Result	1	LPDT/HSDT
RDBWLB	70	R	Read Black/White Low Bits	1	LPDT/HSDT
RDBKx	71	R	Read Bkx	1	LPDT/HSDT
RDBKy	72	R	Read Bky	1	LPDT/HSDT
RDWx	73	R	Read Wx	1	LPDT/HSDT
RDWy	74	R	Read Wy	1	LPDT/HSDT
RDRGLB	75	R	Read Red/Green Low Bits	1	LPDT/HSDT
RDRx	76	R	Read Rx	1	LPDT/HSDT
RDRy	77	R	Read Ry	1	LPDT/HSDT
RDGx	78	R	Read Gx	1	LPDT/HSDT
RDGy	79	R	Read Gy	1	LPDT/HSDT
RDBALB	7A	R	Read Blue/AColour Low Bits	1	LPDT/HSDT
RDBx	7B	R	Read Bx	1	LPDT/HSDT
RDBy	7C	R	Read By	1	LPDT/HSDT
RDAx	7D	R	Read Ax	1	LPDT/HSDT
RDAy	7E	R	Read Ay	1	LPDT/HSDT
RDDDBS	A1	R	Read DDB Start	5	LPDT/HSDT
RDDDBC	A8	R	Read DDB Continue	Any Length	LPDT/HSDT
RDFCS	AA	R	Read First Checksum	1	LPDT/HSDT
RDCCS	AF	R	Read Continue Checksum	1	LPDT/HSDT
RDID1	DA	R	Read ID1	1	LPDT/HSDT
RDID2	DB	R	Read ID2	1	LPDT/HSDT
RDID3	DC	R	Read ID3	1	LPDT/HSDT

Note : LPDT (Low Power Mode), HSDT (High Speed Mode)

Table 5-2 command2 List

Command	(Hex)	Write/Read /Command	Function	Parameter Number	MIPI Transmission Mode
ADRSFT	0000	W	Address Shift Function	1	LPDT
Command 2 Mode	FF00	W	Enable Access Command2“CMD2”	3	LPDT
OTPSEL	A000	R/W	OTP select region	1	LPDT
PGCHK	AE8F	R	OTP programming status check	1	LPDT
MIPISET1	B080	R/W	MIPI Setting1	4	LPDT
MIPISET2	B0A1	R/W	MIPI Setting2	5	LPDT
IF_PARA1	B280	R/W	IF Parameter 1	1	LPDT
IF PARA3	B282	R/W	IF Parameter 3	1	LPDT
CMD PARA1	B380	R/W	Command Set Option Parameter 1	1	LPDT
CMD PARA2	B381	R/W	Command Set Option Parameter 2	1	LPDT
CMD PARA3	B382	R/W	Command Set Option Parameter 3	1	LPDT
CMD PARA4	B383	R/W	Command Set Option Parameter 4	1	LPDT
CMD PARA5	B384	R/W	Command Set Option Parameter 5	1	LPDT
PAD PARA1	B390	R/W	IOPAD Parameter 1	1	LPDT
PAD PARA2	B391	R/W	IOPAD Parameter 2	1	LPDT
PAD PARA3	B392	R/W	IOPAD Parameter 3	1	LPDT
RAM Power Control	B3C0	R/W	SRAM setting 2	2	LPDT
TSP1	C080	R/W	TCON Setting Parameter1	9	LPDT
PTSP1	C092	R/W	Panel Timing Setting Parameter1	2	LPDT
PTSP2	C094	R/W	Panel Timing Setting Parameter2	1	LPDT
PTSP3	C0A2	R/W	Panel Timing Setting Parameter3	1	LPDT
PTSP4	C0A3	R/W	Panel Timing Setting Parameter4	1	LPDT
TE_width	C0B0	R/W	TE width Setting	2	LPDT
ISC	C0B3	R/W	Interval Scan Frame Setting	1	LPDT
P_DRV_M	C0B4	R/W	Panel driving mode	1	LPDT
OSC_ADJ1	C181	R/W	Oscillator Adjustment for Idle/Normal Mode	1	LPDT
SD_PCH_CTRL	C480	R/W	Source Driver Precharge Control	9	LPDT
DC2DCSET	C4A0	R/W	DC2DC setting 1	8	LPDT
PWR_CTRL1	C580	R/W	Power Control Setting 1	4	LPDT
PWR_CTRL2	C590	R/W	Power Control Setting 2 for Normal Mode	7	LPDT
PWR_CTRL3	C5A0	R/W	Power Control Setting 3 for Idle Mode	7	LPDT
PWR_CTRL4	C5B0	R/W	Power Control Setting 4 for DC Voltage Settings	2	LPDT
ABC PARA1	C680	R/W	ABC PARA1 (C680H) ABC Parameter 1	1	LPDT
ABC PARA2	C6B0	R/W	ABC PARA2 (C6B0H) ABC Parameter 2	1	LPDT
ABC PARA3	C6B1	R/W	ABC PARA3 (C6B1H) ABC Parameter 3	2	LPDT
ABC PARA4	C6B3	R/W	ABC PARA4 (C6B3H) ABC Parameter 4	1	LPDT
ABC PARA5	C6B4	R/W	ABC PARA5 (C6B4H) ABC Parameter 5	1	LPDT
ABC PARA6	C6B5	R/W	ABC PARA6 (C6B5H) ABC Parameter 6	1	LPDT
CABCSET1	C700	R/W	CABC setting	1	LPDT
CABCSET2	C800	R/W	CABC gamma curve setting	18	LPDT
AIESET	C900	R/W	AIE Setting	18	LPDT
GOAVST	CE80	R/W	GOA VST Setting	12	LPDT

GOAVEND	CE90	R/W	GOA VEND Setting	12	LPDT
GOAGPSET	CE9C	R/W	GOA Group Setting	2	LPDT
GOACLKA1	CEA0	R/W	GOA CLKA1 Setting	7	LPDT
GOACLKA2	CEA7	R/W	GOA CLKA2 Setting	7	LPDT
GOACLKA3	CEB0	R/W	GOA CLKA3 Setting	7	LPDT
GOACLKA4	CEB7	R/W	GOA CLKA4 Setting	7	LPDT
GOACLKB1	CEC0	R/W	GOA CLKB1 Setting	7	LPDT
GOACLKB2	CEC7	R/W	GOA CLKB2 Setting	7	LPDT
GOACLKB3	CED0	R/W	GOA CLKB3 Setting	7	LPDT
GOACLKB4	CED7	R/W	GOA CLKB4 Setting	7	LPDT
GOCLKC1	CF80	R/W	GOA CLKC1 Setting	7	LPDT
GOCLKC2	CF87	R/W	GOA CLKC2 Setting	7	LPDT
GOCLKC3	CF90	R/W	GOA CLKC3 Setting	7	LPDT
GOCLKC4	CF97	R/W	GOA CLKC4 Setting	7	LPDT
GOCLKD1	CFA0	R/W	GOA CLKD1 Setting	7	LPDT
GOCLKD2	CFA7	R/W	GOA CLKD2 Setting	7	LPDT
GOCLKD3	CFB0	R/W	GOA CLKD3 Setting	7	LPDT
GOCLKD4	CFB7	R/W	GOA CLKD4 Setting	7	LPDT
GOAECLK	CFC0	R/W	GOA ECLK Setting	6	LPDT
GOAOPT1	CFC6	R/W	GOA Other Options 1	1	LPDT
GOATGOPT	CFC7	R/W	GOA Signal Toggle Option Setting	2	LPDT
GOAGNDPRD	CFC9	R/W	GOA Precharge to GND Period	1	LPDT
ID1	D000	R/W	ID1 (Can program 4 times)	1	LPDT
ID2, ID3	D100	R/W	ID2, ID3 (Can program 4 times)	2	LPDT
DDB	D200	R/W	DDB (Can program 4 times)	4	LPDT
OTPDET	D300	R/W	OTP information	1	LPDT
CESET1	D400	R/W	CE Correction Characteristics Setting1	360	LPDT
CESET2	D500	R/W	CE Correction Characteristics Setting2	360	LPDT
CEEN	D680	R/W	CE Enable	1	LPDT
AIEEN	D700	R/W	AIE Enable	1	LPDT
GVDDSET	D800	R/W	GVDD/NGVDD/	2	LPDT
VCOMDC	D900	R/W	VCOM voltage setting	1	LPDT
GMCT22P	E100	R/W	Gamma Correction Characteristics Setting (2.2 +)	16	LPDT
GMCT22N	E200	R/W	Gamma Correction Characteristics Setting (2.2 -)	16	LPDT
GMCT18P	E300	R/W	Gamma Correction Characteristics Setting (1.8 +)	16	LPDT
GMCT18N	E400	R/W	Gamma Correction Characteristics Setting (1.8 -)	16	LPDT
GMCT25P	E500	R/W	Gamma Correction Characteristics Setting (2.5 +)	16	LPDT
GMCT25N	E600	R/W	Gamma Correction Characteristics Setting (2.5 -)	16	LPDT
GMCT10P	E700	R/W	Gamma Correction Characteristics Setting (1.0 +)	16	LPDT
GMCT10N	E800	R/W	Gamma Correction Characteristics Setting (1.0 -)	16	LPDT

NVMIN	EB00	W	NV Memory Write Mode	1	LPDT
DGAMR	EC00	R/W	Digital Gamma Correction Characteristics Setting (Red)	17	LPDT
DGAMG	ED00	R/W	Digital Gamma Correction Characteristics Setting (Green)	17	LPDT
DGAMB	EE00	R/W	Digital Gamma Correction Characteristics Setting (Blue)	17	LPDT
RNVMI	F101	R	Read NVM programming Information	3	LPDT
Orisefunction	FF80	W	Enable Orise function	6	LPDT

Note : LPDT (Low Power Mode), HSDT (High Speed Mode)

5.2. System Command Description

5.2.1. NOP (00h)

NOP (No Operation)											
00H											
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NOP	Write		0	0	0	0	0	0	0	0	(00H)
Parameter	No Parameter										

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> - This command is empty command. It does not have effect on the display module. - However it can be used to terminate RAM data write or read as described in RAMWR (Memory Write), RAMRD (Memory Read) and parameter write commands. 													
Restriction	-													
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
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Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>N/A</td></tr> <tr> <td>S/W Reset</td><td>N/A</td></tr> <tr> <td>H/W Reset</td><td>N/A</td></tr> </tbody> </table>		Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
Status	Default Value													
Power On Sequence	N/A													
S/W Reset	N/A													
H/W Reset	N/A													

5.2.2. SWRESET (01h): Software Reset

SWRESET (Software Reset)												
01H	Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SWRESET	Write			0	0	0	0	0	0	0	1	(01H)
Parameter	No Parameter											-

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> - When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all source & gate outputs are set to VSS (display off). (See default tables in each command description) <p>Note: The Frame Memory contents are not affected by this command.</p>													
Restriction	<ul style="list-style-type: none"> - It will be necessary to wait 5msec before sending new command following software reset. -The display module loads all display supplier’s factory default values to the registers during 5msec. - If Software Reset is applied during Sleep Out mode, it will be necessary to wait <u>120msec</u> before sending Sleep Out command. -Software Reset command cannot be sent during Sleep Out sequence. 													
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
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Partial Mode On, Idle Mode On, Sleep Out	Yes													
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Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">N/A</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">N/A</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">N/A</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
Status	Default Value													
Power On Sequence	N/A													
S/W Reset	N/A													
H/W Reset	N/A													

5.2.3. RDNUMED (05H) Read Number of the Errors on DSI

05H		RDNUMED (Read Number of the Errors on DSI)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDNUMED	Write		0	0	0	0	0	1	0	1	(05H)
1 st Parameter	Read		P7	P6	P5	P4	P3	P2	P1	P0	-

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> - The first parameter is telling a number of the errors on DSI. The more detailed description of the bits is below. - P[6..0] bits are telling a number of the errors. - P[7] is set to ‘1’ if there is overflow with P[6..0] bits. - P[7..0] bits are set to ‘0’s (as well as RDDSM(0EH)’s D0 is set ‘0’ at the same time) after there is sent the second parameter information (= The read function is completed). - See Read Display Signal Mode (0EH). 												
Restriction													
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

5.2.4. RDDPM (0AH): Read Display Power Mode

0AH		RDDPM (Read Display Power Mode)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDPM	Write		0	0	0	0	1	0	1	0	(0AH)
1 st Parameter	Read		BSTON	IDMON	PTLON	SLP OUT	NOR ON	DISON	D1	D0	08h

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	-This command indicates the current status of the display as described in the table below:		
	Bit	Description	Value
	BSTON	Booster Voltage Status	“1”=Booster on, “0”=Booster off
	IDMON	Idle Mode On/Off	“1” = Idle Mode On, “0” = Idle Mode Off
	PTLON	Partial Mode On/Off	“1” = Partial Mode On, “0” = Partial Mode Off
	SLPON	Sleep In/Out	“1” = Sleep Out, “0” = Sleep In
	NORON	Display Normal Mode On/Off	“1” = Normal Display, “0” = Partial Display
	DISON	Display On/Off	“1” = Display On, “0” = Display Off
	D1	Not Used	“0”
	D0	Not Used	“0”
Restriction	-		
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value (D7 to D0)	
	Power On Sequence	08h	
	S/W Reset	08h	
	H/W Reset	08h	

5.2.5. RDDMADCTR (0BH): Read Display MADCTR

0BH		RDDMADCTR (Read Display MADCTR)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDMADCTR	Write		0	0	0	0	1	0	1	1	(0BH)
1 st Parameter	Read		MY	MX	MV	ML	RGB	MH	D1	D0	00h

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	-This command indicates the current status of the display as described in the table below:														
	Bit	Description	Value												
	MY	Row Address Order	‘1’ =Decrement, ‘0’=Increment												
	MX	Column Address Order	‘1’ =Decrement, ‘0’=Increment												
	MV	Row/Column Order (MV)	‘1’ = Row/column exchange (MV=1) ‘0’ = Normal (MV=0)												
	ML	Vertical Refresh Order	‘1’ =LCD Refresh Top to Bottom ‘0’ =LCD Refresh Bottom to Top												
	RGB	RGB/BGR Order	‘1’ =BGR, ‘0’=RGB												
	MH	Reserved	Don’t care												
	D1	Not Used	‘0’												
	D0	Not Used	‘0’												
Restriction															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability														
Normal Mode On, Idle Mode Off, Sleep Out	Yes														
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Status	Default Value (D7 to D0)														
Power On Sequence	00h														
S/W Reset	00h														
H/W Reset	00h														

5.2.6. RDDCOLMOD (0CH): Read Display Pixel Format

0CH		RDDCOLMOD (Read Display Pixel Format)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDCOLMOD	Write		0	0	0	0	1	1	0	0	(0CH)
1 st Parameter	Read		0	0	0	0	0	IFPF2	IFPF1	IFPF0	07h

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	-This command indicates the current status of the display as described in the table below: <table border="1"> <thead> <tr> <th colspan="2">IFPF[2:0]</th><th colspan="9">MCU Interface Color Format</th></tr> </thead> <tbody> <tr> <td>011</td><td>3</td><td colspan="9">12-bits/pixel</td></tr> <tr> <td>101</td><td>5</td><td colspan="9">16-bits/pixel</td></tr> <tr> <td>110</td><td>6</td><td colspan="9">18-bits/pixel</td></tr> <tr> <td>111</td><td>7</td><td colspan="9" rowspan="22">24-bits/pixel</td></tr> </tbody> </table> Others are no define and invalid	IFPF[2:0]		MCU Interface Color Format									011	3	12-bits/pixel									101	5	16-bits/pixel									110	6	18-bits/pixel									111	7	24-bits/pixel								
IFPF[2:0]		MCU Interface Color Format																																																						
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111	7	24-bits/pixel																																																						
Restriction																																																								
Register Availability																																																								
Default																																																								

5.2.7. RDDIM (0DH): Read Display Image Mode

0DH		RDDIM (Read Display Image Mode)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDIM	Write		0	0	0	0	1	1	0	1	(0DH)
1 st Parameter	Read		0	D6	INVON	ALLPX ON	ALLPX OFF	GCS2	GCS1	GCS0	00h

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	-This command indicates the current status of the display as described in the table below: <table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Value</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Not used</td><td></td></tr> <tr> <td>D6</td><td>For Future Use</td><td>“0” (Not used)</td></tr> <tr> <td>INVON</td><td>Inversion On/Off</td><td>“1” = Inversion is On, “0” = Inversion is Off</td></tr> <tr> <td>ALLPXON</td><td>All Pixel On</td><td>“1” = All pixel on is On “0” = All pixel on is Off</td></tr> <tr> <td>ALLPXOFF</td><td>All Pixel Off</td><td>“1” = All pixel off is On “0” = All pixel off is Off</td></tr> <tr> <td>GCS2</td><td rowspan="3">Gamma Curve Selection</td><td>“000” = GC0,</td></tr> <tr> <td>GCS1</td><td>“001” = GC1,</td></tr> <tr> <td>GCS0</td><td>“010” = GC2, “011” = GC3, “100” to “111” = Not defined</td></tr> </tbody> </table>								Bit	Description	Value	D7	Not used		D6	For Future Use	“0” (Not used)	INVON	Inversion On/Off	“1” = Inversion is On, “0” = Inversion is Off	ALLPXON	All Pixel On	“1” = All pixel on is On “0” = All pixel on is Off	ALLPXOFF	All Pixel Off	“1” = All pixel off is On “0” = All pixel off is Off	GCS2	Gamma Curve Selection	“000” = GC0,	GCS1	“001” = GC1,	GCS0	“010” = GC2, “011” = GC3, “100” to “111” = Not defined
Bit	Description	Value																															
D7	Not used																																
D6	For Future Use	“0” (Not used)																															
INVON	Inversion On/Off	“1” = Inversion is On, “0” = Inversion is Off																															
ALLPXON	All Pixel On	“1” = All pixel on is On “0” = All pixel on is Off																															
ALLPXOFF	All Pixel Off	“1” = All pixel off is On “0” = All pixel off is Off																															
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GCS1		“001” = GC1,																															
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Power On Sequence	00h																																
S/W Reset	00h																																
H/W Reset	00h																																

5.2.8. RDDSM (0EH): Read Display Signal Mode

0EH		RDDSM (Read Display Signal Mode)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDSM	Write		0	0	0	0	1	1	1	0	(0EH)
1 st Parameter	Read	TEON	TELOM	D5	D4	D3	D2	D1	D0	00h	

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	-This command indicates the current status of the display as described in the table below: <table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Value</th></tr> </thead> <tbody> <tr> <td>TEON</td><td>Tearing Effect Line On/Off</td><td>“1” = On, “0” = Off</td></tr> <tr> <td>TELOM</td><td>Tearing effect line mode</td><td>“0” = mode1, “1” = mode2</td></tr> <tr> <td>D5</td><td>Not Used</td><td></td></tr> <tr> <td>D4</td><td>Not Used</td><td></td></tr> <tr> <td>D3</td><td>Not Used</td><td></td></tr> <tr> <td>D2</td><td>Not Used</td><td></td></tr> <tr> <td>D1</td><td>Not Used</td><td></td></tr> <tr> <td>D0</td><td>Not Used</td><td></td></tr> </tbody> </table>		Bit	Description	Value	TEON	Tearing Effect Line On/Off	“1” = On, “0” = Off	TELOM	Tearing effect line mode	“0” = mode1, “1” = mode2	D5	Not Used		D4	Not Used		D3	Not Used		D2	Not Used		D1	Not Used		D0	Not Used	
Bit	Description	Value																											
TEON	Tearing Effect Line On/Off	“1” = On, “0” = Off																											
TELOM	Tearing effect line mode	“0” = mode1, “1” = mode2																											
D5	Not Used																												
D4	Not Used																												
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D0	Not Used																												
Restriction																													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																
Status	Availability																												
Normal Mode On, Idle Mode Off, Sleep Out	Yes																												
Normal Mode On, Idle Mode On, Sleep Out	Yes																												
Partial Mode On, Idle Mode Off, Sleep Out	Yes																												
Partial Mode On, Idle Mode On, Sleep Out	Yes																												
Sleep In	Yes																												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value (D7 to D0)</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00h</td></tr> <tr> <td>S/W Reset</td><td>00h</td></tr> <tr> <td>H/W Reset</td><td>00h</td></tr> </tbody> </table>	Status	Default Value (D7 to D0)	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h																				
Status	Default Value (D7 to D0)																												
Power On Sequence	00h																												
S/W Reset	00h																												
H/W Reset	00h																												

5.2.9. RDDSDR (0FH): Read Display Self-Diagnostic Result

0FH		RDDSDR (Read Display Self-Diagnostic Result)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDSDR	Write		0	0	0	0	1	1	1	1	(0FH)
1 st Parameter	Read	RELD	FUND	D5	D4	D3	D2	D1	D0	00h	

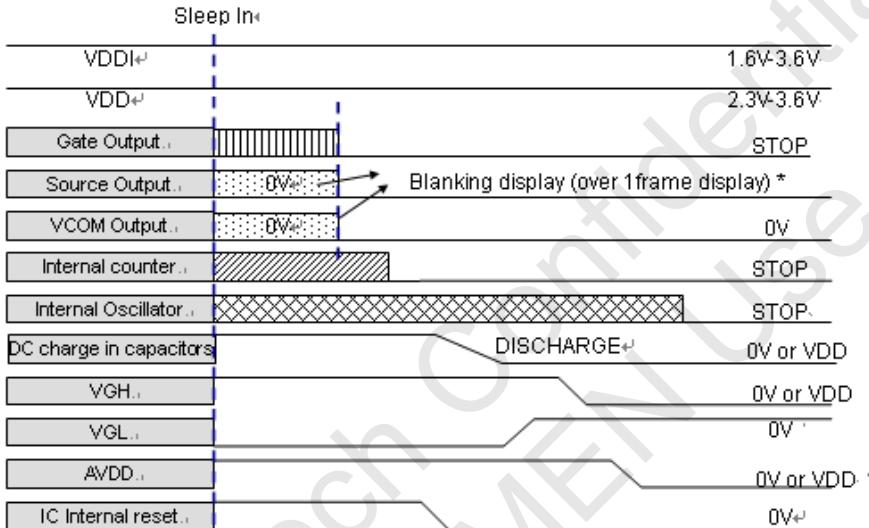
NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	-This command indicates the current status of the display as described in the table below:														
	Bit	Description	Value												
	RELD	Register Loading Detection	See section 6.8.1												
	FUND	Functionality Detection	See section 6.8.2												
	D5	Not Used	“0”												
	D4	Not Used	“0”												
	D3	Not Used	“0”												
	D2	Not Used	“0”												
	D1	Not Used	“0”												
	D0	Not Used	“0”												
Restriction															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability														
Normal Mode On, Idle Mode Off, Sleep Out	Yes														
Normal Mode On, Idle Mode On, Sleep Out	Yes														
Partial Mode On, Idle Mode Off, Sleep Out	Yes														
Partial Mode On, Idle Mode On, Sleep Out	Yes														
Sleep In	Yes														
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value (D7 to D0)</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00h</td></tr> <tr> <td>S/W Reset</td><td>00h</td></tr> <tr> <td>H/W Reset</td><td>00h</td></tr> </tbody> </table>			Status	Default Value (D7 to D0)	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value (D7 to D0)														
Power On Sequence	00h														
S/W Reset	00h														
H/W Reset	00h														

5.2.10. SLPIN (10H): Sleep In

10H		SLPIN (Sleep In)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPIN	Write		0	0	0	1	0	0	0	0	(10H)
1 st Parameter	No parameter										-

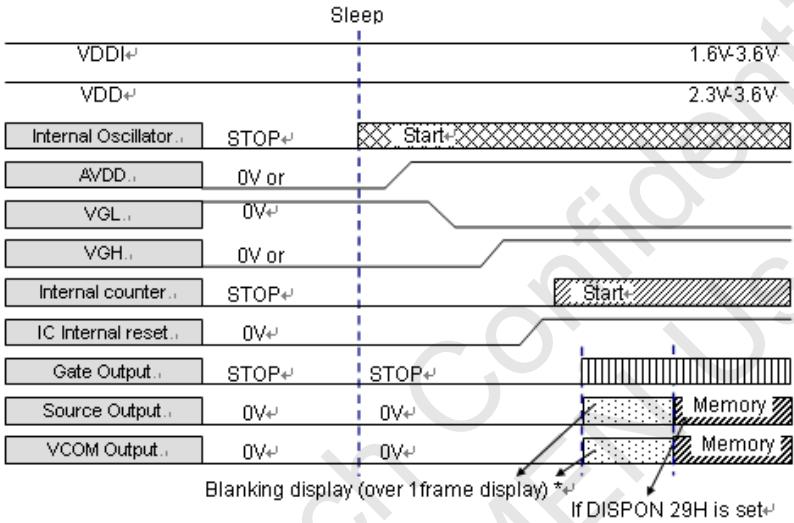
NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> -This command causes the LCD module to enter the minimum power consumption mode. -In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.  <p>The diagram illustrates the state of various signals during Sleep In mode. A vertical blue line marks the transition from normal operation to Sleep In. - VDDI₊: 1.6V-3.6V - VDD₊: 2.3V-3.6V - Gate Output..: STOP - Source Output..: Blanking display (over 1frame display) * - VCOM Output..: 0V - Internal counter..: STOP - Internal Oscillator..: STOP - DC charge in capacitors: DISCHARGE → 0V or VDD - VGH..: 0V or VDD - VGL..: 0V - AVDD..: 0V or VDD - IC Internal reset..: 0V₊ </p> <p>* Note: complete 1 frame display (ex: continue 2-falling edges of VS)..</p>											
	-MCU interface and memory are still working and the memory keeps its contents											
	<ul style="list-style-type: none"> -This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11H). -It will be necessary to wait <u>5msec</u> before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. -It will be necessary to wait <u>120msec</u> after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent. 											
	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In
Status	Availability											
Normal Mode On, Idle Mode Off, Sleep Out	Yes											
Normal Mode On, Idle Mode On, Sleep Out	Yes											
Partial Mode On, Idle Mode Off, Sleep Out	Yes											
Partial Mode On, Idle Mode On, Sleep Out	Yes											
Sleep In	Yes											
<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep In mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep In mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep In mode</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Sleep In mode	S/W Reset	Sleep In mode	H/W Reset	Sleep In mode				
Status	Default Value											
Power On Sequence	Sleep In mode											
S/W Reset	Sleep In mode											
H/W Reset	Sleep In mode											

5.2.11. SLPOUT (11H): Sleep Out

SLPOUT (Sleep Out)												
11H	Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
SLPOUT	Write			0	0	0	1	0	0	0	1	(11H)
1 st Parameter	No Parameter											-

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.  <p>The diagram illustrates the transition from Sleep mode to Sleep Out mode. A vertical dashed line marks the transition point. After the transition, the following signals change: <ul style="list-style-type: none"> VDDI_o: 1.6V-3.6V VDD_o: 2.3V-3.6V Internal Oscillator: STOP → Start (indicated by a cross-hatched bar) AVDD_o: 0V or VGL_o: 0V VGH_o: 0V or Internal counter: STOP → Start (indicated by a hatched bar) IC Internal reset: 0V Gate Output: STOP → Start (indicated by a bar with vertical lines) Source Output: 0V → 0V → Memory (indicated by a dotted bar) VCOM Output: 0V → 0V → Memory (indicated by a hatched bar) A note at the bottom states: "Blanking display (over 1frame display) * If DISPON 29H is set". </p> <p>* Note: complete 1 frame display (ex: continue 2-falling edges of VS).</p>												
Restriction	<ul style="list-style-type: none"> This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10H). It will be necessary to wait <u>5msec</u> before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. DRIVER loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the DRIVER is already Sleep Out mode. DRIVER is doing self-diagnostic functions during this <u>5msec</u>. It will be necessary to wait <u>120msec</u> after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent 												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												

Default	Status		Default Value							
	Power On Sequence		Sleep In mode							
	S/W Reset		Sleep In mode							
	H/W Reset		Sleep In mode							

5.2.12. PTLON (12H): Partial Display Mode On

12H		PTLON (Partial Display Mode On)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLON	Write		0	0	0	1	0	0	1	0	(12H)
1 st Parameter	No Parameter										-

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	-This command turns on Partial mode. The partial mode window is described by the Partial Area command (30H) -To leave Partial mode, the Normal Display Mode On command (13H) should be written. -There is no abnormal visual effect during mode change between Normal mode On <-> Partial mode On.													
Restriction	This command has no effect when Partial mode is active.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Mode On</td> </tr> <tr> <td>S/W Reset</td> <td>Normal Mode On</td> </tr> <tr> <td>H/W Reset</td> <td>Normal Mode On</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Normal Mode On	S/W Reset	Normal Mode On	H/W Reset	Normal Mode On				
Status	Default Value													
Power On Sequence	Normal Mode On													
S/W Reset	Normal Mode On													
H/W Reset	Normal Mode On													
Flow Chart	See Partial Area (30H)													

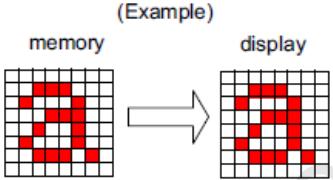
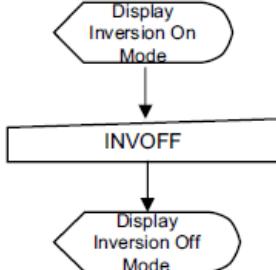
5.2.13. NORON (13H): Normal Display Mode On

NORON (Normal Display Mode On)												
13H	Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
NORON	Write			0	0	0	1	0	0	1	1	(13H)
1 st Parameter	No Parameter											-

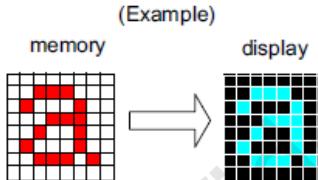
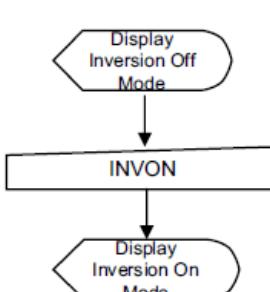
NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> -This command returns the display to normal mode. -Normal display mode on means <u>Partial mode off</u>, <u>Scroll mode Off</u>. -Exit from NORON by the Partial mode On command (12H) -There is no abnormal visual effect during mode change from Normal mode On to Partial mode On. 													
Restriction	<ul style="list-style-type: none"> -This command has no effect when Normal Display mode is active. 													
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">Normal Mode On</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">Normal Mode On</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">Normal Mode On</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Normal Mode On	S/W Reset	Normal Mode On	H/W Reset	Normal Mode On				
Status	Default Value													
Power On Sequence	Normal Mode On													
S/W Reset	Normal Mode On													
H/W Reset	Normal Mode On													
Flow Chart	<p>-See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command</p>													

5.2.14. INVOFF (20h) : Display Inversion Off

20H		INVOFF (Display Inversion Off)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	0	1	0	0	0	0	0	20													
Parameter	No parameter																						
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status.																						
	 X = Don't care																						
Restrictions	This command has no effect when module is already in inversion off mode. This command is ignored when "21H_REV_DIS=1". (This command reacts as "NOP".)																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode, Idle Mode Off, Sleep Out	Yes	Normal Mode, Idle Mode On, Sleep Out	Yes	Partial Mode, Idle Mode Off, Sleep Out	Yes	Partial Mode, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
Normal Mode, Idle Mode Off, Sleep Out	Yes																						
Normal Mode, Idle Mode On, Sleep Out	Yes																						
Partial Mode, Idle Mode Off, Sleep Out	Yes																						
Partial Mode, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion Off</td> </tr> <tr> <td>SW Reset</td> <td>Display Inversion Off</td> </tr> <tr> <td>HW Reset</td> <td>Display Inversion Off</td> </tr> </tbody> </table>											Status	Default value	Power On Sequence	Display Inversion Off	SW Reset	Display Inversion Off	HW Reset	Display Inversion Off				
Status	Default value																						
Power On Sequence	Display Inversion Off																						
SW Reset	Display Inversion Off																						
HW Reset	Display Inversion Off																						
Flow chart	 <pre> graph TD A([Display Inversion On Mode]) --> B[INVOFF] B --> C([Display Inversion Off Mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																						

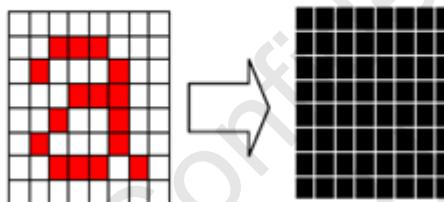
5.2.15. INVON (21h) : Display Inversion On

21H		INVON (Display Inversion On)																					
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	Write	0	0	1	0	0	0	0	1	21													
1 st parameter																							
Parameter	No parameter																						
Description	<p>This command is used to enter into display inversion mode.</p> <p>This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.</p> <p>This command does not change any other status.</p> <p>(Example)</p>  <p>X = Don't care</p>																						
Restrictions	<p>This command has no effect when module is already in inversion on mode.</p> <p>This command is ignored when "21H_REV_DIS=1". (This command reacts as "NOP".)</p>																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode, Idle Mode Off, Sleep Out	Yes	Normal Mode, Idle Mode On, Sleep Out	Yes	Partial Mode, Idle Mode Off, Sleep Out	Yes	Partial Mode, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
Normal Mode, Idle Mode Off, Sleep Out	Yes																						
Normal Mode, Idle Mode On, Sleep Out	Yes																						
Partial Mode, Idle Mode Off, Sleep Out	Yes																						
Partial Mode, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion Off</td> </tr> <tr> <td>SW Reset</td> <td>Display Inversion Off</td> </tr> <tr> <td>HW Reset</td> <td>Display Inversion Off</td> </tr> </tbody> </table>											Status	Default value	Power On Sequence	Display Inversion Off	SW Reset	Display Inversion Off	HW Reset	Display Inversion Off				
Status	Default value																						
Power On Sequence	Display Inversion Off																						
SW Reset	Display Inversion Off																						
HW Reset	Display Inversion Off																						
Flow chart	 <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div>																						

5.2.16. ALLPOFF (22H): All Pixels Off

22H		ALLPOOF (All Pixels Off)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
ALLPOOFF	Write		0	0	1	0	0	0	1	0	(22H)
1 st Parameter	No Parameter										-

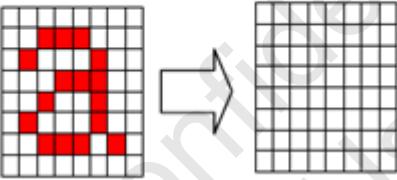
NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> - This command turns the display panel black in ‘Sleep Out’ –mode and a status of the ‘Display On/Off’ –register can be ‘on’ or ‘off’. - This command makes no change of contents of frame memory (or MIP). This command does not change any other status. <p style="text-align: center;">(Example).. Memory (or MIP) → display..</p>  <ul style="list-style-type: none"> - ‘All Pixels On’, ‘Normal Display Mode On’ or ‘Partial Mode On’ – commands are used to leave this mode. - The display panel is showing the content of the frame memory after ‘Normal Display Mode On’ and ‘Partial Mode On’ –commands. 												
Restriction	<ul style="list-style-type: none"> - This command has no effect when module is already in all pixels off mode. 												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">Off</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">Off</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">Off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off				
Status	Default Value												
Power On Sequence	Off												
S/W Reset	Off												
H/W Reset	Off												

5.2.17. ALLPON (23H): All Pixels On

23H		ALLPOON (All Pixels On)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
ALLPOON	Write		0	0	1	0	0	0	1	1	(23H)
1 st Parameter	No Parameter										-

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> - This command turns the display panel white in ‘Sleep out’ –mode and a status of the ‘Display On/Off’ –register can be ‘on’ or ‘off’. - This command makes no change of contents of frame memory (or MIP). - This command does not change any other status. <p style="text-align: center;">(Example):</p> <p style="text-align: center;">Memory (or MIP) display:</p>  <ul style="list-style-type: none"> - ‘All Pixels Off’, ‘Normal Display Mode On’ or ‘Partial Mode On’ – commands are used to leave this mode. - The display is showing the content of the frame memory after ‘Normal Display Mode On’ and ‘Partial Mode On’ –commands. 												
Restriction	<ul style="list-style-type: none"> - This command has no effect when module is already in all pixels on mode. 												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">Off</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">Off</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">Off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off				
Status	Default Value												
Power On Sequence	Off												
S/W Reset	Off												
H/W Reset	Off												

5.2.18. GAMSET (26H): Gamma Set

26H		GAMSET (Gamma Set)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GAMSET	Write		0	0	1	0	0	1	1	0	(26H)
1 st Parameter	Write		GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	01h

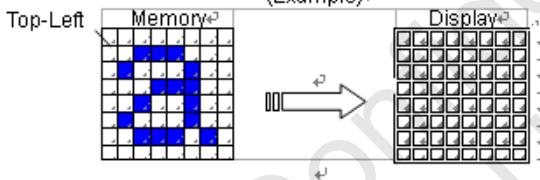
NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<p>-This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.</p> <table border="1"> <thead> <tr> <th>GC [7:0]</th><th>Parameter</th><th>Curve Selected</th></tr> </thead> <tbody> <tr> <td>01h</td><td>GC0</td><td>Gamma Curve 1 (G2.2)</td></tr> <tr> <td>02h</td><td>GC1</td><td>Gamma Curve 2 (G1.8)</td></tr> <tr> <td>04h</td><td>GC2</td><td>Gamma Curve 3 (G2.5)</td></tr> <tr> <td>08h</td><td>GC3</td><td>Gamma Curve 4 (G1.0)</td></tr> </tbody> </table> <p><i>Note:</i></p> <ol style="list-style-type: none"> 1. All other values are undefined. 2. In the Gamma separate mode ignore this command. 				GC [7:0]	Parameter	Curve Selected	01h	GC0	Gamma Curve 1 (G2.2)	02h	GC1	Gamma Curve 2 (G1.8)	04h	GC2	Gamma Curve 3 (G2.5)	08h	GC3	Gamma Curve 4 (G1.0)
GC [7:0]	Parameter	Curve Selected																	
01h	GC0	Gamma Curve 1 (G2.2)																	
02h	GC1	Gamma Curve 2 (G1.8)																	
04h	GC2	Gamma Curve 3 (G2.5)																	
08h	GC3	Gamma Curve 4 (G1.0)																	
Restriction																			
<p>-Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid is received.</p>																			
Register Availability																			
<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes					
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Partial Mode On, Idle Mode Off, Sleep Out	Yes																		
Partial Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default																			
<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>01h</td> </tr> <tr> <td>S/W Reset</td> <td>01h</td> </tr> <tr> <td>H/W Reset</td> <td>01h</td> </tr> </tbody> </table>			Status	Default Value	Power On Sequence	01h	S/W Reset	01h	H/W Reset	01h									
Status	Default Value																		
Power On Sequence	01h																		
S/W Reset	01h																		
H/W Reset	01h																		

5.2.19. DISPOFF (28H): Display Off

28H		DISPOFF (Display Off)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPOFF	Write		0	0	1	0	1	0	0	0	(28H)
1 st Parameter	No Parameter										-

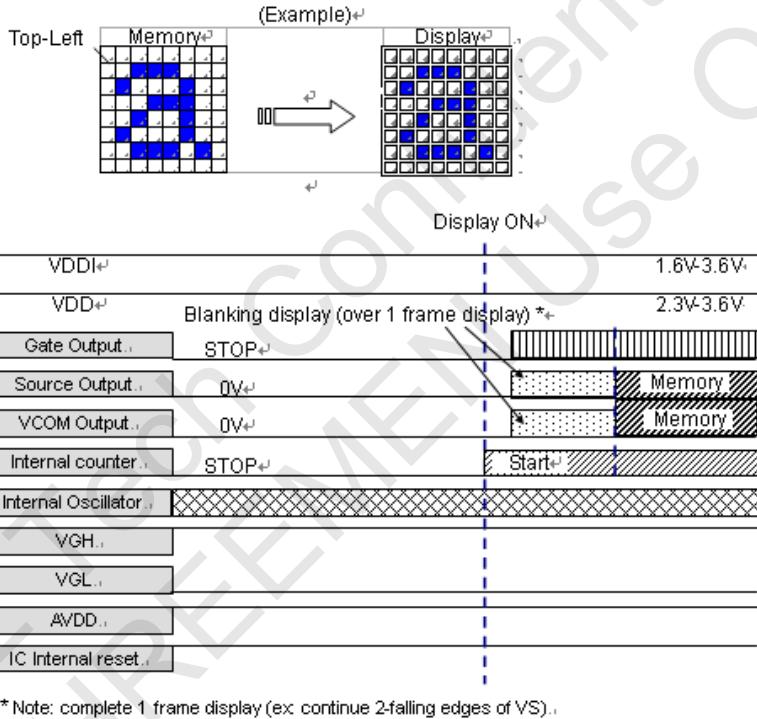
NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> -This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. -This command makes no change of contents of frame memory. -This command does not change any other status. -There will be no abnormal visible effect on the display. -Exit from this command by Display On (29H) <div style="text-align: center;"> <p>(Example)</p>  <p>Display OFF</p> <table border="1"> <tr><td>VDDI</td><td>1.6V-3.6</td></tr> <tr><td>VDD</td><td>2.3V-3.6</td></tr> <tr><td>Gate Output</td><td>STOP+</td></tr> <tr><td>Source Output</td><td>0V → Blanking display (over 1 frame display) *</td></tr> <tr><td>VCOM Output</td><td>0V</td></tr> <tr><td>Internal counter</td><td>STOP+</td></tr> <tr><td>Internal Oscillator</td><td>STOP+</td></tr> <tr><td>VGH</td><td></td></tr> <tr><td>VGL</td><td></td></tr> <tr><td>AVDD</td><td></td></tr> <tr><td>IC Internal reset</td><td></td></tr> </table> <p>* Note: complete 1 frame display (ex: continue 2-falling edges of VS).</p> </div>	VDDI	1.6V-3.6	VDD	2.3V-3.6	Gate Output	STOP+	Source Output	0V → Blanking display (over 1 frame display) *	VCOM Output	0V	Internal counter	STOP+	Internal Oscillator	STOP+	VGH		VGL		AVDD		IC Internal reset	
VDDI	1.6V-3.6																						
VDD	2.3V-3.6																						
Gate Output	STOP+																						
Source Output	0V → Blanking display (over 1 frame display) *																						
VCOM Output	0V																						
Internal counter	STOP+																						
Internal Oscillator	STOP+																						
VGH																							
VGL																							
AVDD																							
IC Internal reset																							
Restriction	-This command has no effect when module is already in Display Off mode.																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes										
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr><td>Power On Sequence</td><td>Display off</td></tr> <tr><td>S/W Reset</td><td>Display off</td></tr> <tr><td>H/W Reset</td><td>Display off</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off														
Status	Default Value																						
Power On Sequence	Display off																						
S/W Reset	Display off																						
H/W Reset	Display off																						

5.2.20. DISPON (29H): Display On

29H		DISPON (Display On)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DISPON	Write		0	0	1	0	1	0	0	1	(29H)
1 st Parameter	No Parameter										-

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> -This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. -This command makes no change of contents of frame memory. -This command does not change any other status. <div style="text-align: center; margin-top: 10px;">  <p style="margin-top: 10px;">* Note: complete 1 frame display (ex: continue 2-falling edges of VS).</p> </div>												
Restriction	-This command has no effect when module is already in Display On mode.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">Display off</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">Display off</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">Display off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off				
Status	Default Value												
Power On Sequence	Display off												
S/W Reset	Display off												
H/W Reset	Display off												

5.2.21. CASET (2AH): Column Address Set

2AH		CASET (Column Address Set)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
CASET	Write		0	0	1	0	1	0	1	0	(2AH)
1 st Parameter	Write		XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	00h
2 nd Parameter	Write		XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	00h
3 rd Parameter	Write		XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	02h
4 th Parameter	Write		XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	1Bh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

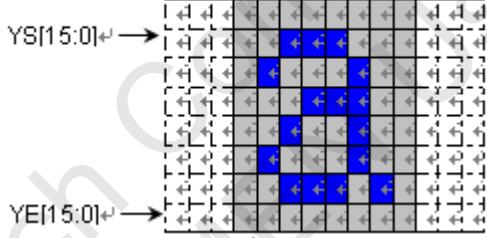
Description	<ul style="list-style-type: none"> -This command is used to define area of frame memory where MCU can access. -This command makes no change on the other driver status. -The value of XS [15:0] and XE [15:0] are referred when RAMWR command comes. -Each value represents one column line in the Frame Memory. <p style="text-align: center;">(Example)</p>												
Restriction	<p>XS [15:0] always must be equal to or less than XE [15:0]</p> <p>When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored.</p>												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Sleep In</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												

Default	540x960 Resolution (IC Default Setting)			
	Status	Default Value		
		XS [15:0]	XE [15:0] (MV='0')	XE [15:0] (MV='1')
	Power On Sequence	0000h	021Bh (539d)	
	S/W Reset		021Bh (539d)	03BFh (959d)
	H/W Reset		021Bh (539d)	
480x960 Resolution				
Default	Status	Default Value		
		XS [15:0]	XE [15:0] (MV='0')	XE [15:0] (MV='1')
	Power On Sequence	0000h	01DFh (479d)	
	S/W Reset		01DFh (479d)	03BFh (959d)
	H/W Reset		01DFh (479d)	
480x864 Resolution				
Default	Status	Default Value		
		XS [15:0]	XE [15:0] (MV='0')	XE [15:0] (MV='1')
	Power On Sequence	0000h	01DFh (479d)	
	S/W Reset		01DFh (479d)	035Fh (863d)
	H/W Reset		01DFh (479d)	
480x854 Resolution				
Default	Status	Default Value		
		XS [15:0]	XE [15:0] (MV='0')	XE [15:0] (MV='1')
	Power On Sequence	0000h	01DFh (479d)	
	S/W Reset		01DFh (479d)	0355h (853d)
	H/W Reset		0257h (599d)	
480x800 Resolution				
Default	Status	Default Value		
		XS [15:0]	XE [15:0] (MV='0')	XE [15:0] (MV='1')
	Power On Sequence	0000h	01DFh (479d)	
	S/W Reset		01DFh (479d)	031Fh (799d)
	H/W Reset		01DFh (479d)	

5.2.22. PASET (2BH): Page Address Set

2BH		PASET (Page Address Set)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RASET	Write		0	0	1	0	1	0	1	1	(2BH)
1 st Parameter	Write		YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	00h
2 nd Parameter	Write		YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	00h
3 rd Parameter	Write		YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	03h
4 th Parameter	Write		YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	BFh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> -This command is used to define area of frame memory where MCU can access. -This command makes no change on the other driver status. -The value of YS [15:0] and YE [15:0] are referred when RAMWR command comes. -Each value represents one column line in the Frame Memory. <p style="text-align: center;">(Example)</p> 												
Restriction	<p>YS [15:0] always must be equal to or less than YE [15:0]</p> <p>When YS [15:0] or YE [15:0] are greater than maximum row address like below, data of out of range will be ignored.</p>												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Sleep In</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												

Default	540x960 Resolution (IC Default Setting)					
	Status	Default Value				
		YS [15:0]	YE [15:0] (MV='0')	YE [15:0] (MV='1')		
	Power On Sequence		03BFh (959d)			
	S/W Reset	0000h	03BFh (959d)	021Bh (539d)		
	H/W Reset		03BFh (959d)			
480x960 Resolution						
	Status	Default Value				
		YS [15:0]	YE [15:0] (MV='0')	YE [15:0] (MV='1')		
	Power On Sequence		03BFh (959d)			
	S/W Reset	0000h	03BFh (959d)	01DFh (479d)		
	H/W Reset		03BFh (959d)			
	480x864 Resolution					
	Status	Default Value				
		YS [15:0]	YE [15:0] (MV='0')	YE [15:0] (MV='1')		
	Power On Sequence		035Fh (863d)			
	S/W Reset	0000h	035Fh (863d)	01DFh (479d)		
	H/W Reset		035Fh (863d)			
	480x854 Resolution					
	Status	Default Value				
		YS [15:0]	YE [15:0] (MV='0')	YE [15:0] (MV='1')		
	Power On Sequence		0355h (853d)			
	S/W Reset	0000h	0355h (853d)	01DFh (479d)		
	H/W Reset		0355h (853d)			
	480x800 Resolution					
	Status	Default Value				
		YS [15:0]	YE [15:0] (MV='0')	YE [15:0] (MV='1')		
	Power On Sequence		031Fh (799d)			
	S/W Reset	0000h	031Fh (799d)	01DFh (479d)		
	H/W Reset		031Fh (799d)			

5.2.23. RAMWR (2CH): Memory Write

2CH		RAMWR (Memory Write)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMWR	Write		0	0	1	0	1	1	0	0	(2CH)
1 st Parameter	Write		D7	D6	D5	D4	D3	D2	D1	D0	-
	Write										
N th Parameter	Write		D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	-This command is used to transfer data from MCU to frame memory. -This command makes no change to the other driver status. -When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. -The Start Column/Start Row positions are different in accordance with MADCTR setting. -Sending any other command can stop Frame Write.												
Restriction	In all color modes, there is no restriction on length of parameters. 540x960 Resolution 540x960x24-bits memory can be written by this command Memory range: (0000h,0000h) -> (021Bh, 03BFh)												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared				
Status	Default Value												
Power On Sequence	Contents of memory is set randomly												
S/W Reset	Contents of memory is not cleared												
H/W Reset	Contents of memory is not cleared												

5.2.24. RAMRD (2EH): Memory Read

2EH		RAMRD (Memory Read)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMRD	Write		0	0	1	0	1	1	1	0	(2EH)
1 st Parameter	Read		D7	D6	D5	D4	D3	D2	D1	D0	-
	Read										
(N+1) th Parameter	Read		D7	D6	D5	D4	D3	D2	D1	D0	-

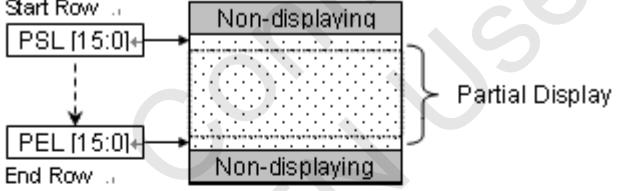
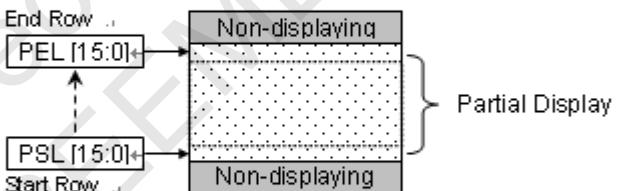
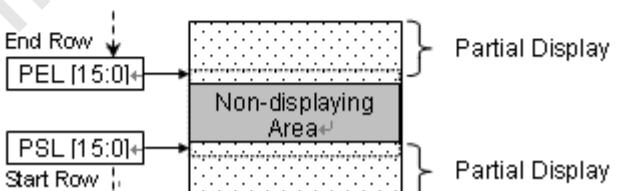
NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> -This command is used to transfer data from frame memory to MCU. -This command makes no change to the other driver status. -When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. -The Start Column/Start Row positions are different in accordance with MADCTR setting. -Then D[23:0] is read back from the frame memory and the column register and the row register incremented. -Frame Read can be canceled by sending any other command. . 												
Restriction	<ul style="list-style-type: none"> -In all color modes, the Frame Read is always 24-bits and there is no restriction on length of parameters. 												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">Contents of memory is set randomly</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">Contents of memory is not cleared</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">Contents of memory is not cleared</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared				
Status	Default Value												
Power On Sequence	Contents of memory is set randomly												
S/W Reset	Contents of memory is not cleared												
H/W Reset	Contents of memory is not cleared												

5.2.25. PTLAR (30H): Partial Area

30H		PTLAR (Partial Area)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PTLAR	Write		0	0	1	1	0	0	0	0	(30H)
1 st Parameter	Write		PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	00h
2 nd Parameter	Write		PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	00h
3 rd Parameter	Write		PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	
4 th Parameter	Write		PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	<p>-This command defines the partial mode's display area.</p> <p>-There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.</p> <p>-If End Row > Start Row, when MADCTL ML='0'↓</p>  <p>-If End Row > Start Row, when MADCTL ML='1'↑</p>  <p>-If End Row < Start Row, when MADCTL ML='0'↓</p>  <p>-If End Row = Start Row then the Partial Area will be one row deep.</p>

Restriction	<p>-PEL [15:0] always must be equal to or less than PSL [15:0]</p> <p>-When PEL [15:0] or PSL [15:0] are greater than maximum row address like below, data of out of range will be ignored.</p> <p>540x960 memory base</p> <p>(Parameter range: $0d \leq PSL[15:0] \leq PEL[15:0] \leq 959d$ (3BFh))</p> <p>If the “PSL” or “PEL” are large then 959d, it become 959d</p>														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes		
Status	Availability														
Normal Mode On, Idle Mode Off, Sleep Out	Yes														
Normal Mode On, Idle Mode On, Sleep Out	Yes														
Partial Mode On, Idle Mode Off, Sleep Out	Yes														
Partial Mode On, Idle Mode On, Sleep Out	Yes														
Sleep In	Yes														
Default	<p>540x960 memory base</p> <table border="1"> <thead> <tr> <th rowspan="2">Status</th><th colspan="2">Default Value</th></tr> <tr> <th>PSL [15:0]</th><th>PEL [15:0]</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td></td><td></td></tr> <tr> <td>S/W Reset</td><td>0000h</td><td>03BFh</td></tr> <tr> <td>H/W Reset</td><td></td><td></td></tr> </tbody> </table>	Status	Default Value		PSL [15:0]	PEL [15:0]	Power On Sequence			S/W Reset	0000h	03BFh	H/W Reset		
Status	Default Value														
	PSL [15:0]	PEL [15:0]													
Power On Sequence															
S/W Reset	0000h	03BFh													
H/W Reset															

5.2.26. TEOFF (34H): Tearing Effect Line OFF

34H		TEOFF (Tearing Effect Line OFF)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEOFF	Write		0	0	1	1	0	1	0	0	(34H)
1 st Parameter	No Parameter										-

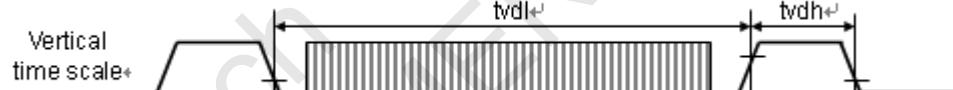
NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.	
Restriction	-This command has no effect when Tearing Effect output is already OFF.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	OFF
	S/W Reset	
	H/W Reset	

5.2.27. TEON (35H): Tearing Effect Line ON

35H		TEON (Tearing Effect Line ON)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEON	Write		0	0	1	1	0	1	0	1	(35H)
1 st Parameter	Write		0	0	0	0	0	0	0	TELOM	00h

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

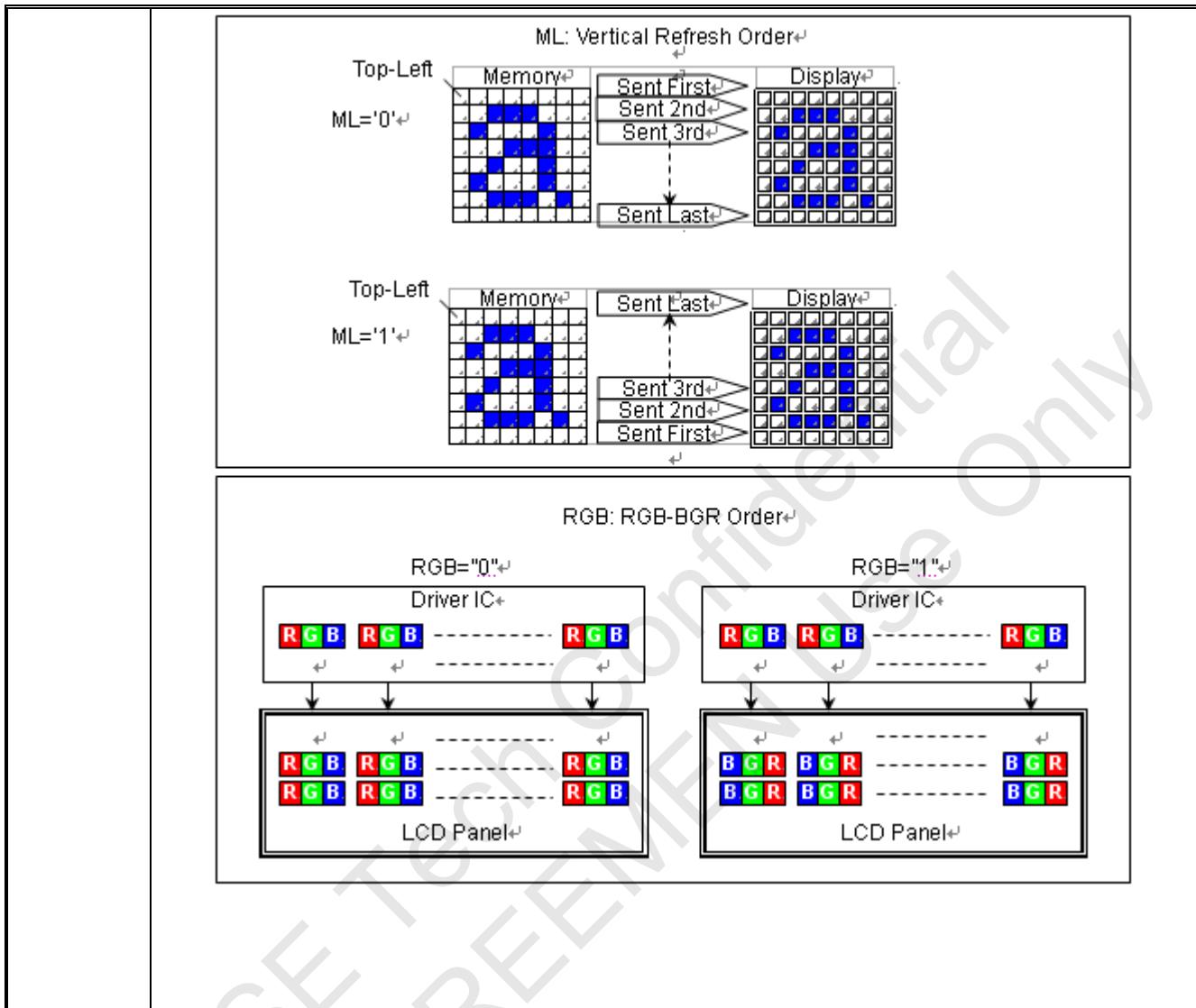
Description	<ul style="list-style-type: none"> -This command is used to turn ON the Tearing Effect output signal from the TE signal line. -This output is not affected by changing MADCTR bit ML. -The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. (“-”=Don’t Care). – When M='0': <p>The Tearing Effect Output line consists of V-Blanking information only.</p>  – When M='1': <p>The Tearing Effect Output line consists of both V-Blanking and H-Blinking information.</p>  <p>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.</p>												
Restriction	<ul style="list-style-type: none"> -This command has no effect when Tearing Effect output is already OFF. -In MIPI mode, only the Tearing Effect Output line consists of V-Blanking information is available (M='0'). 												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td rowspan="3">OFF & TELOM=0</td> </tr> <tr> <td>S/W Reset</td> </tr> <tr> <td>H/W Reset</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	OFF & TELOM=0	S/W Reset	H/W Reset						
Status	Default Value												
Power On Sequence	OFF & TELOM=0												
S/W Reset													
H/W Reset													

5.2.28. MADCTR (36H): Memory Data Access Control

36H		MADCTR (Memory Data Access Control)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
MADCTR	Write		0	0	1	1	0	1	1	0	(36H)
1 st Parameter	Write		MY	MX	MV	ML	RGB	MH	0	0	00h

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	- This command has no effect for driver output, only register value is updated. -This command defines read/ write scanning direction of frame memory. -This command makes no change on the other driver status. -Bit Assignment							
	Bit	NAME		DESCRIPTION				
	MY	Row Address Order		These 3bits controls MCU to memory write/read direction.				
	MX	Column Address Order						
	MV	Row/Column Exchange		LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top				
	ML	Vertical Refresh Order						
	RGB	RGB-BGR ORDER		Color selector switch control '0' =RGB color filter panel, '1' =BGR color filter panel				
	MH	Reserved		Keep '0'				



Restriction	D2, D1 and D0 of the 1 st parameter are set to "00" internally.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0</td></tr> <tr> <td>S/W Reset</td><td>MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0</td></tr> <tr> <td>H/W Reset</td><td>MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0	S/W Reset	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0	H/W Reset	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0				
Status	Default Value												
Power On Sequence	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0												
S/W Reset	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0												
H/W Reset	MY=0,MX=0,MV=0,ML=0,RGB=0,MH=0												

5.2.29. IDMOFF (38H): Idle Mode Off

38H		IDMOFF (Idle Mode Off)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMOFF	Write		0	0	1	1	1	0	0	0	(38H)
1 st Parameter	No Parameter										-

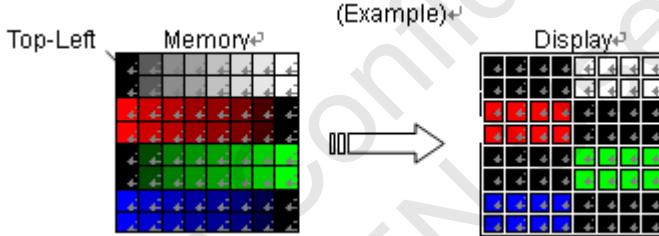
NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> -This command is used to recover from Idle mode on. -There will be no abnormal visible effect on the display mode change transition. -In the idle off mode, <ol style="list-style-type: none"> 1. LCD can display 4k, 65k, 262k and 16.7M –colors. 2. Normal frame frequency is applied. 													
Restriction	<ul style="list-style-type: none"> -This command has no effect when module is already in idle off mode. 													
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">Idle Mode Off</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">Idle Mode Off</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">Idle Mode Off</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Idle Mode Off	S/W Reset	Idle Mode Off	H/W Reset	Idle Mode Off				
Status	Default Value													
Power On Sequence	Idle Mode Off													
S/W Reset	Idle Mode Off													
H/W Reset	Idle Mode Off													

5.2.30. IDMON (39H) : Idle Mode On

39H		IDMON (Idle Mode On)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
IDMON	Write		0	0	1	1	1	0	0	1	(39H)
1 st Parameter	No Parameter										-

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> -This command is used to enter into Idle mode on. -There will be no abnormal visible effect on the display mode change transition. -In the idle on mode, <ol style="list-style-type: none"> 1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed. 2. 8-Color mode frame frequency is applied. 3. Exit from IDMON by Idle Mode Off (38H) command <div style="text-align: center; margin-top: 10px;">  <p style="text-align: center;">(Example) ↗</p> </div> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>Color</th><th>R₇ R₆ R₅ R₄ R₃ R₂ R₁ R₀</th><th>G₇ G₆ G₅ G₄ G₃ G₂ G₁ G₀</th><th>B₇ B₆ B₅ B₄ B₃ B₂ B₁ B₀</th></tr> </thead> <tbody> <tr> <td>Black</td><td>0xxxxxx</td><td>0xxxxxx</td><td>0xxxxxx</td></tr> <tr> <td>Blue</td><td>0xxxxxx</td><td>0xxxxxx</td><td>1xxxxxx</td></tr> <tr> <td>Red</td><td>1xxxxxx</td><td>0xxxxxx</td><td>0xxxxxx</td></tr> <tr> <td>Magenta</td><td>1xxxxxx</td><td>0xxxxxx</td><td>1xxxxxx</td></tr> <tr> <td>Green</td><td>0xxxxxx</td><td>1xxxxxx</td><td>0xxxxxx</td></tr> <tr> <td>Cyan</td><td>0xxxxxx</td><td>1xxxxxx</td><td>1xxxxxx</td></tr> <tr> <td>Yellow</td><td>1xxxxxx</td><td>1xxxxxx</td><td>0xxxxxx</td></tr> <tr> <td>White</td><td>1xxxxxx</td><td>1xxxxxx</td><td>1xxxxxx</td></tr> </tbody> </table> <p style="text-align: right; margin-top: 10px;">“x” Don’t care</p>	Color	R ₇ R ₆ R ₅ R ₄ R ₃ R ₂ R ₁ R ₀	G ₇ G ₆ G ₅ G ₄ G ₃ G ₂ G ₁ G ₀	B ₇ B ₆ B ₅ B ₄ B ₃ B ₂ B ₁ B ₀	Black	0xxxxxx	0xxxxxx	0xxxxxx	Blue	0xxxxxx	0xxxxxx	1xxxxxx	Red	1xxxxxx	0xxxxxx	0xxxxxx	Magenta	1xxxxxx	0xxxxxx	1xxxxxx	Green	0xxxxxx	1xxxxxx	0xxxxxx	Cyan	0xxxxxx	1xxxxxx	1xxxxxx	Yellow	1xxxxxx	1xxxxxx	0xxxxxx	White	1xxxxxx	1xxxxxx	1xxxxxx
Color	R ₇ R ₆ R ₅ R ₄ R ₃ R ₂ R ₁ R ₀	G ₇ G ₆ G ₅ G ₄ G ₃ G ₂ G ₁ G ₀	B ₇ B ₆ B ₅ B ₄ B ₃ B ₂ B ₁ B ₀																																		
Black	0xxxxxx	0xxxxxx	0xxxxxx																																		
Blue	0xxxxxx	0xxxxxx	1xxxxxx																																		
Red	1xxxxxx	0xxxxxx	0xxxxxx																																		
Magenta	1xxxxxx	0xxxxxx	1xxxxxx																																		
Green	0xxxxxx	1xxxxxx	0xxxxxx																																		
Cyan	0xxxxxx	1xxxxxx	1xxxxxx																																		
Yellow	1xxxxxx	1xxxxxx	0xxxxxx																																		
White	1xxxxxx	1xxxxxx	1xxxxxx																																		
Restriction	This command has no effect when module is already in idle on mode.																																				
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																								
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Default	<table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Idle Mode Off</td></tr> <tr> <td>S/W Reset</td><td>Idle Mode Off</td></tr> <tr> <td>H/W Reset</td><td>Idle Mode Off</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	Idle Mode Off	S/W Reset	Idle Mode Off	H/W Reset	Idle Mode Off																												
Status	Default Value																																				
Power On Sequence	Idle Mode Off																																				
S/W Reset	Idle Mode Off																																				
H/W Reset	Idle Mode Off																																				

5.2.31. COLMOD (3AH): Interface Pixel Format

3AH		COLMOD (Interface Pixel Format)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
COLMOD	Write		0	0	1	1	1	0	1	0	(3AH)
1 st Parameter	Write		VIPF3	VIPF2	VIPF1	VIPF0	D3	IFPF2	IFPF1	IFPF0	77h

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<p>This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface and RGB interface. The formats are shown in the table:</p> <table border="1"> <thead> <tr> <th colspan="2">IFPF[2:0]</th><th colspan="3">MCU Interface Color Format</th></tr> </thead> <tbody> <tr> <td>011</td><td>3</td><td colspan="3">12-bits/pixel</td></tr> <tr> <td>101</td><td>5</td><td colspan="3">16-bits/pixel</td></tr> <tr> <td>110</td><td>6</td><td colspan="3">18-bits/pixel</td></tr> <tr> <td>111</td><td>7</td><td colspan="3">24-bits/pixel</td></tr> </tbody> </table> <p>Others are no define and invalid</p> <table border="1"> <thead> <tr> <th colspan="2">VIPF[3:0]</th><th colspan="3">RGB Interface Color Format</th></tr> </thead> <tbody> <tr> <td>0101</td><td>5</td><td colspan="3">16-bits/pixel (1-times data transfer)</td></tr> <tr> <td>0110</td><td>6</td><td colspan="3">18-bits/pixel (1-times data transfer)</td></tr> <tr> <td>0111</td><td>7</td><td colspan="3">24-bits/pixel (1-times data transfer)</td></tr> <tr> <td>1110</td><td>14</td><td colspan="3">24-bits/pixel (3-times data transfer)</td></tr> </tbody> </table> <p>Others are no define and invalid</p> <p>Note1: In 12-bits/Pixel, 16-bits/Pixel or 18-bits/Pixel mode, the LUT is applied to transfer data into the Frame Memory.</p> <p>Note2: When RGB I/F the 12-bit/pixel don’t care</p> <p>Note 3: When VIPF[3:0] = “1110”, 8-bits data width of 3-times transfer is used to transmit 1 pixel data with the 24-bits color depth information.</p>	IFPF[2:0]		MCU Interface Color Format			011	3	12-bits/pixel			101	5	16-bits/pixel			110	6	18-bits/pixel			111	7	24-bits/pixel			VIPF[3:0]		RGB Interface Color Format			0101	5	16-bits/pixel (1-times data transfer)			0110	6	18-bits/pixel (1-times data transfer)			0111	7	24-bits/pixel (1-times data transfer)			1110	14	24-bits/pixel (3-times data transfer)		
IFPF[2:0]		MCU Interface Color Format																																																	
011	3	12-bits/pixel																																																	
101	5	16-bits/pixel																																																	
110	6	18-bits/pixel																																																	
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VIPF[3:0]		RGB Interface Color Format																																																	
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0110	6	18-bits/pixel (1-times data transfer)																																																	
0111	7	24-bits/pixel (1-times data transfer)																																																	
1110	14	24-bits/pixel (3-times data transfer)																																																	
Restriction	There is no visible effect until the Frame Memory is written to.																																																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																																						
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Sleep In	Yes																																																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="2">Default Value</th> </tr> </thead> <tbody> <tr> <td></td><td>IFPF[2:0]</td><td>VIPF[3:0]</td></tr> <tr> <td>Power On Sequence</td><td>111 (24-bits/pixel)</td><td>0111 (24-bits/pixel)</td></tr> <tr> <td>S/W Reset</td><td>111 (24-bits/pixel)</td><td>0111 (24-bits/pixel)</td></tr> <tr> <td>H/W Reset</td><td>111 (24-bits/pixel)</td><td>0111 (24-bits/pixel)</td></tr> </tbody> </table>	Status	Default Value			IFPF[2:0]	VIPF[3:0]	Power On Sequence	111 (24-bits/pixel)	0111 (24-bits/pixel)	S/W Reset	111 (24-bits/pixel)	0111 (24-bits/pixel)	H/W Reset	111 (24-bits/pixel)	0111 (24-bits/pixel)																																			
Status	Default Value																																																		
	IFPF[2:0]	VIPF[3:0]																																																	
Power On Sequence	111 (24-bits/pixel)	0111 (24-bits/pixel)																																																	
S/W Reset	111 (24-bits/pixel)	0111 (24-bits/pixel)																																																	
H/W Reset	111 (24-bits/pixel)	0111 (24-bits/pixel)																																																	

5.2.32. RAMWRCNT (3CH): Memory Write Continue

3CH		RAMWRCNT (Memory Write Continue)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMWRCNT	Write		0	0	1	1	1	1	0	0	(3CH)
1 st Parameter	Write		D7	D6	D5	D4	D3	D2	D1	D0	-
	Write										
N th Parameter	Write		D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	-This command is used to transfer data from MCU to frame memory continuing from the pixel location following the previous 2CH or 3CH command -This command makes no change to the other driver status. -When this command is accepted, the column register and the row register are not reset to the Start Column/Start Row positions. -The Start Column/Start Row positions are different in accordance with MADCTR setting. -Sending any other command can stop Frame Write.												
Restriction	In all color modes, there is no restriction on length of parameters. 540x960 memory base 540x960x24-bits memory can be written by this command Memory range: (0000h,0000h) -> (021Bh, 03BFh)												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr> <tr> <td>S/W Reset</td><td>Contents of memory is not cleared</td></tr> <tr> <td>H/W Reset</td><td>Contents of memory is not cleared</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared				
Status	Default Value												
Power On Sequence	Contents of memory is set randomly												
S/W Reset	Contents of memory is not cleared												
H/W Reset	Contents of memory is not cleared												

5.2.33. RAMRDCNT (3EH): Memory Read Continue

3EH		RAMRDCNT (Memory Read Continue)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RAMRDCNT	Write		0	0	1	1	1	1	1	0	(3EH)
1 st Parameter	Read		D7	D6	D5	D4	D3	D2	D1	D0	-
	Read										
(N+1) th Parameter	Read		D7	D6	D5	D4	D3	D2	D1	D0	-

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> -This command is used to transfer data from frame memory to MCU if there is wanted to continue memory write after 2EH command. -This command makes no change to the other driver status. -When this command is accepted, the column register and the row register are not reset to the Start Column/Start Row positions. -The Start Column/Start Row positions are different in accordance with MADCTR setting. -Then D[23:0] is read back from the frame memory and the column register and the row register incremented. -Frame Read can be canceled by sending any other command. . 												
Restriction	<ul style="list-style-type: none"> -In all color modes, the Frame Read is always 24-bits and there is no restriction on length of parameters. 												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">Contents of memory is set randomly</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">Contents of memory is not cleared</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">Contents of memory is not cleared</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared				
Status	Default Value												
Power On Sequence	Contents of memory is set randomly												
S/W Reset	Contents of memory is not cleared												
H/W Reset	Contents of memory is not cleared												

5.2.34. WRTESCN (44H): Write TE Scan Line

44H		WRTESCN (Write TE Scan Line)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRTESCN	Write		0	1	0	0	0	1	0	0	(44H)
1 st Parameter	Write		N15	N14	N13	N12	N11	N10	N9	N8	-
2 nd Parameter	Write		N7	N6	N5	N4	N3	N2	N1	N0	-

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	-This command turns on the display module's TE signal when the display module reaches line N. - When setting N=0, it is equivalent to 35H, M=0.													
Restriction	-The command takes affect with the end of one frame.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>0000h</td></tr> <tr> <td>S/W Reset</td><td>0000h</td></tr> <tr> <td>H/W Reset</td><td>0000h</td></tr> </tbody> </table>		Status	Default Value	Power On Sequence	0000h	S/W Reset	0000h	H/W Reset	0000h				
Status	Default Value													
Power On Sequence	0000h													
S/W Reset	0000h													
H/W Reset	0000h													

5.2.35. RDSCNL (45H): Read Scan Line

45H		RDSCNL (Read Scan Line)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDSCNL	Write		0	1	0	0	0	1	0	1	(45H)
1 st Parameter	Read		N15	N14	N13	N12	N11	N10	N9	N8	xxh
2 nd Parameter	Read		N7	N6	N5	N4	N3	N2	N1	N0	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	-This read byte returns the current scan line. -The 1 st parameter: N line MSB -The 2 nd parameter: N line LSB													
Restriction	None													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>xxh</td></tr> <tr> <td>S/W Reset</td><td>xxh</td></tr> <tr> <td>H/W Reset</td><td>xxh</td></tr> </tbody> </table>		Status	Default Value	Power On Sequence	xxh	S/W Reset	xxh	H/W Reset	xxh				
Status	Default Value													
Power On Sequence	xxh													
S/W Reset	xxh													
H/W Reset	xxh													

5.2.36. WRDISBV (51H) Write Display Brightness

51H		WRDISBV (Write Display Brightness)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRDISBV	Write		0	1	0	1	0	0	0	1	(51H)
1 st Parameter	Write		DBV 7	DBV 6	DBV 5	DBV 4	DBV 3	DBV 2	DBV 1	DBV 0	00 FF

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This command is used to adjust the brightness value of the display. - It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. - In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction	-												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

5.2.37. RDDISBV (52H) Read Display Brightness Value

52H		RDDISBV (Read Display Brightness Value)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDISBV	Write		0	1	0	1	0	0	1	0	(52H)
1 st Parameter	Read		DBV 7	DBV 6	DBV 5	DBV 4	DBV 3	DBV 2	DBV 1	DBV 0	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> - This command returns the brightness value of the display. - It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification. - In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. - See command “Write Display Brightness (51H)”. - This command can be used to read the brightness value of the display also when Display brightness control is in automatic mode. - Write CTRL Display (53H) bit DB = ‘1’. - DBV[7:0] is reset when display is in sleep-in mode. - DBV[7:0] is ‘0’ when bit BCTRL of “Write CTRL Display (53H)” command is ‘0’. - DBV[7:0] is manual set brightness specified with “Write CTRL Display (53H)” command when bit BCTRL is ‘1’ and bit A of “Write CTRL Display (53H)” command is ‘0’. 												
Restriction													
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
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Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

5.2.38. WRCTRLD (53H) Write CTRL Display

53H		WRCTRLD (Write CTRL Display)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRCTRLD	Write		0	1	0	1	0	0	1	1	(53H)
1 st Parameter	Write		-	-	BCTRL	-	DD	BL	-	-	00 FF

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> This command is used to control ambient light, brightness and gamma settings. <p>BCTRL : Brightness Control Block On/Off. This bit is always used to switch brightness for display and keyboard. '0' = Off (Brightness registers are 00h, DBV[7..0] and KBV[7..0]) '1' = On (Brightness registers are active, according to the other parameters.)</p> <p>DD : Display Dimming '0' = Display Dimming is off '1' = Display Dimming is on</p> <p>BL : Backlight On/Off '0' = Off (Completely turn off backlight circuit. Control lines must be low.) '1' = On</p> <ul style="list-style-type: none"> - Dimming function is adapted to the brightness registers for display and keyboard when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0. - When BL bit change from “On” to “Off”, backlight is turned off 												
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

5.2.39. RDCTRLD (54H) Read CTRL Display

54H		RDCTRLD (Read CTRL Display)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDCTRLD	Write		0	1	0	1	0	1	0	0	(54H)
1 st Parameter	Read		-	-	BCTRL	-	DD	BL	-	-	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<p>- This command returns ambient light and brightness control values, see command “9.2.35 Write CTRL Display (53H) ”.</p> <p>BCTRL: Brightness Control Block On/Off. This bit is always used to switch brightness for display and keyboard. '0' = Off '1' = On</p> <p>DD: Display Dimming '0' = Display Dimming is off '1' = Display Dimming is on</p> <p>BL: Backlight On/Off, This bit is always controlled by the user '0' = Off (completely turn off backlight circuit) '1' = On</p>												
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

5.2.40. WRCABC (55H) Write Content Adaptive Brightness Control

WRCABC (Write Content Adaptive Brightness Control)												
55H	Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRCABD	Write			0	1	0	1	0	1	0	1	(55H)
1 st Parameter	Write			-	-	-	-	-	C2	C1	C0	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> - This command is used to set parameters for image content based adaptive brightness control functionality. - There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. <table border="1" style="margin-top: 10px;"> <thead> <tr> <th>C2</th><th>C1</th><th>C0</th><th>Function</th></tr> </thead> <tbody> <tr> <td rowspan="4">Reserved</td><td>0</td><td>0</td><td>Off</td></tr> <tr> <td>0</td><td>1</td><td>User Interface Image (UI)</td></tr> <tr> <td>1</td><td>0</td><td>Still Picture (ST)</td></tr> <tr> <td>1</td><td>1</td><td>Moving Image (MV)</td></tr> </tbody> </table> <p>C2 bit is reserved bit. Please set it to be '0'</p>	C2	C1	C0	Function	Reserved	0	0	Off	0	1	User Interface Image (UI)	1	0	Still Picture (ST)	1	1	Moving Image (MV)
C2	C1	C0	Function															
Reserved	0	0	Off															
	0	1	User Interface Image (UI)															
	1	0	Still Picture (ST)															
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Restriction																		
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Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Partial Mode On, Idle Mode Off, Sleep Out	Yes																	
Partial Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">00h</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">00h</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h									
Status	Default Value																	
Power On Sequence	00h																	
S/W Reset	00h																	
H/W Reset	00h																	

5.2.41. RDCABC (56H) Read Content Adaptive Brightness Control

56H		RDCABC (Read Content Adaptive Brightness Control)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDCABC	Write		0	1	0	1	0	1	1	0	(56H)
1 st Parameter	Read		-	-	-	-	-	-	C1	C0	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> - This command is used to read the settings for image content based adaptive brightness control functionality. - There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. <table border="1" style="margin-top: 10px;"> <thead> <tr> <th>C1</th><th>C0</th><th>Function</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>Off</td></tr> <tr> <td>0</td><td>1</td><td>User Interface Image (UI)</td></tr> <tr> <td>1</td><td>0</td><td>Still Picture (ST)</td></tr> <tr> <td>1</td><td>1</td><td>Moving Image (MV)</td></tr> </tbody> </table>			C1	C0	Function	0	0	Off	0	1	User Interface Image (UI)	1	0	Still Picture (ST)	1	1	Moving Image (MV)
C1	C0	Function																
0	0	Off																
0	1	User Interface Image (UI)																
1	0	Still Picture (ST)																
1	1	Moving Image (MV)																
Restriction																		
Register Availability																		
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Status	Availability																	
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Status	Default Value																	
Power On Sequence	00h																	
S/W Reset	00h																	
H/W Reset	00h																	

5.2.42. WRCABCMB (5EH) Write CABC Minimum Brightness

5EH		WRCABCMB (Write CABC Minimum Brightness)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
WRCABCMB	Write		0	1	0	1	1	1	1	0	(5EH)
1 st Parameter	Write		CMB 7	CMB 6	CMB 5	CMB 4	CMB 3	CMB 2	CMB 1	CMB 0	00 FF

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> - This command is used to set the minimum brightness value of the display for CABC function. - In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. 													
Restriction	-													
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													

5.2.43. RDCABCMB (5FH) Read CABC Minimum Brightness

5FH		RDCABCMB (Read CABC Minimum Brightness)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDCABCMB	Write		0	1	0	1	1	1	1	1	(5FH)
1 st Parameter	Read		CMB 7	CMB 6	CMB 5	CMB 4	CMB 3	CMB 2	CMB 1	CMB 0	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This command returns the minimum brightness value of CABC function. - In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. - See command “Write CABC Minimum Brightness (5EH)”.												
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
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Sleep In	Yes												
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Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

5.2.44. RDABCSDR (68H) Read Automatic Brightness Control Self-diagnostics Result

68H		RDABCSDR (Read Automatic Brightness Control Self-diagnostics Result)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDABCSDR	Write		0	1	1	0	1	0	0	0	(68H)
1 st Parameter	Read		D7	D6	0	0	0	0	0	0	x0h

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> - This command indicates the status of the display self-diagnostic results for automatic brightness control after Sleep Out command as described as below: D7 : Register Loading Detection D6 : Functionality Detection - When “Read Display Self-Diagnostic Result (0FH)” command covers the function for “Read Automatic Brightness Control Self-Diagnostic Result (68H)” command, it is not necessary to implement. 												
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Sleep In	Yes												
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Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

5.2.45. RDBWLB (70H) Read Back/White Low Bits

70H		RDBWLB (Read Black/White Low Bits)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDBWLB	Write		0	1	1	1	0	0	0	0	(70H)
1 st Parameter	Read		Bkx 1	Bkx 0	Bky 1	Bky 0	Wx 1	Wx 0	Wy 1	Wy 0	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This command returns the lowest bits of black and white color characteristics. Black: Bkx and Bky White: Wx and Wy												
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
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Normal Mode On, Idle Mode On, Sleep Out	Yes												
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Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>xxh</td> </tr> <tr> <td>S/W Reset</td> <td>xxh</td> </tr> <tr> <td>H/W Reset</td> <td>xxh</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	xxh	S/W Reset	xxh	H/W Reset	xxh				
Status	Default Value												
Power On Sequence	xxh												
S/W Reset	xxh												
H/W Reset	xxh												

5.2.46. RDBkx (71H) Read Bkx

71H		RDBkx (Read Bkx)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDBkx	Write		0	1	1	1	0	0	0	1	(71H)
1 st Parameter	Read		Bkx 9	Bkx 8	Bkx 7	Bkx 6	Bkx 5	Bkx 4	Bkx 3	Bkx 2	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This command returns the Bkx bits (Bkx[9:2]) of black color characteristics.													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>xxh</td> </tr> <tr> <td>S/W Reset</td> <td>xxh</td> </tr> <tr> <td>H/W Reset</td> <td>xxh</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	xxh	S/W Reset	xxh	H/W Reset	xxh				
Status	Default Value													
Power On Sequence	xxh													
S/W Reset	xxh													
H/W Reset	xxh													

5.2.47. RDBky (72H) Read Bky

72H		0									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDBky	Write		0	1	1	1	0	0	1	0	(72H)
1 st Parameter	Read		Bky 9	Bky 8	Bky 7	Bky 6	Bky 5	Bky 4	Bky 3	Bky 2	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This command returns the Bky bits (Bky[9:2]) of black color characteristics.													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>xxh</td> </tr> <tr> <td>S/W Reset</td> <td>xxh</td> </tr> <tr> <td>H/W Reset</td> <td>xxh</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	xxh	S/W Reset	xxh	H/W Reset	xxh				
Status	Default Value													
Power On Sequence	xxh													
S/W Reset	xxh													
H/W Reset	xxh													

5.2.48. RDWx (73H) Read Wx

73H		RDWx (Read Wx)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDWx	Write		0	1	1	1	0	0	1	1	(73H)
1 st Parameter	Read		Wx 9	Wx 8	Wx 7	Wx 6	Wx 5	Wx 4	Wx 3	Wx 2	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This command returns the Wx bits (Wx[9:2]) of white color characteristics.													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>xxh</td> </tr> <tr> <td>S/W Reset</td> <td>xxh</td> </tr> <tr> <td>H/W Reset</td> <td>xxh</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	xxh	S/W Reset	xxh	H/W Reset	xxh				
Status	Default Value													
Power On Sequence	xxh													
S/W Reset	xxh													
H/W Reset	xxh													

5.2.49. RDWy (74H) Read Wy

74H		RDWy (read Wy)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDWy	Write		0	1	1	1	0	1	0	0	(74H)
1 st Parameter	Read		Wy 9	Wy 8	Wy 7	Wy 6	Wy 5	Wy 4	Wy 3	Wy 2	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This command returns the Wy bits (Wy[9:2]) of white color characteristics.													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>xxh</td> </tr> <tr> <td>S/W Reset</td> <td>xxh</td> </tr> <tr> <td>H/W Reset</td> <td>xxh</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	xxh	S/W Reset	xxh	H/W Reset	xxh				
Status	Default Value													
Power On Sequence	xxh													
S/W Reset	xxh													
H/W Reset	xxh													

5.2.50. RDRGLB (75H) Read Red/Green Low Bits

75H		RDRGLB (Read Red/Green Low Bits)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDRGLB	Write		0	1	1	1	0	1	0	1	(75H)
1 st Parameter	Read		Rx 1	Rx 0	Ry 1	Ry 0	Gx 1	Gx 0	Gy 1	Gy 0	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This command returns the lowest bits of red and green color characteristics. Red: Rx and Ry Green: Gx and Gy												
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
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Status	Default Value												
Power On Sequence	xxh												
S/W Reset	xxh												
H/W Reset	xxh												

5.2.51. RDRx (76H) Read Rx

76H		Read Rx (Read Rx)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDRx	Write		0	1	1	1	0	1	1	0	(76H)
1 st Parameter	Read		Rx 9	Rx 8	Rx 7	Rx 6	Rx 5	Rx 4	Rx 3	Rx 2	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This command returns the Rx bits (Rx[9:2]) of red color characteristics.													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>xxh</td> </tr> <tr> <td>S/W Reset</td> <td>xxh</td> </tr> <tr> <td>H/W Reset</td> <td>xxh</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	xxh	S/W Reset	xxh	H/W Reset	xxh				
Status	Default Value													
Power On Sequence	xxh													
S/W Reset	xxh													
H/W Reset	xxh													

5.2.52. RDRy (77H) Read Ry

77H		RDRy (Read Ry)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDRy	Write		0	1	1	1	0	1	1	1	(77H)
1 st Parameter	Read		Ry 9	Ry 8	Ry 7	Ry 6	Ry 5	Ry 4	Ry 3	Ry 2	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This command returns the Ry bits (Ry[9:2]) of red color characteristics.													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>xxh</td> </tr> <tr> <td>S/W Reset</td> <td>xxh</td> </tr> <tr> <td>H/W Reset</td> <td>xxh</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	xxh	S/W Reset	xxh	H/W Reset	xxh				
Status	Default Value													
Power On Sequence	xxh													
S/W Reset	xxh													
H/W Reset	xxh													

5.2.53. RDGx (78H) Read Gx

78H		RDGx (Read Gx)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDGx	Write		0	1	1	1	1	0	0	0	(78H)
1 st Parameter	Read		Gx 9	Gx 8	Gx 7	Gx 6	Gx 5	Gx 4	Gx 3	Gx 2	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This command returns the Gx bits (Gx[9:2]) of green color characteristics.													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>xxh</td> </tr> <tr> <td>S/W Reset</td> <td>xxh</td> </tr> <tr> <td>H/W Reset</td> <td>xxh</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	xxh	S/W Reset	xxh	H/W Reset	xxh				
Status	Default Value													
Power On Sequence	xxh													
S/W Reset	xxh													
H/W Reset	xxh													

5.2.54. RDGy (79H) Read Gy

79H		RDGy (Read Gy)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDGy	Write		0	1	1	1	1	0	0	1	(79H)
1 st Parameter	Read		Gy 9	Gy 8	Gy 7	Gy 6	Gy 5	Gy 4	Gy 3	Gy 2	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This command returns the Gy bits (Gy[9:2]) of green color characteristics.													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
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Status	Default Value													
Power On Sequence	xxh													
S/W Reset	xxh													
H/W Reset	xxh													

5.2.55. RDBALB (7AH) Read Blue/Acolour Low Bits

7AH		RDBALB (Read Blue/Acolour Low Bits)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDBALB	Write		0	1	1	1	1	0	1	0	(7AH)
1 st Parameter	Read		Bx 1	Bx 0	By 1	By 0	Ax 1	Ax 0	Ay 1	Ay 0	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This command returns the lowest bits of blue and A color characteristics. Blue: Bx and By A: Ax and Ay - If A is not used Ax[1:0] and Ay[1:0] bits are set to '0's.												
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>xxh</td> </tr> <tr> <td>S/W Reset</td> <td>xxh</td> </tr> <tr> <td>H/W Reset</td> <td>xxh</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	xxh	S/W Reset	xxh	H/W Reset	xxh				
Status	Default Value												
Power On Sequence	xxh												
S/W Reset	xxh												
H/W Reset	xxh												

5.2.56. RDBx (7BH) Read Bx

7BH		RDBx (Read Bx)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDBx	Write		0	1	1	1	1	0	1	1	(7BH)
1 st Parameter	Read		Bx 9	Bx 8	Bx 7	Bx 6	Bx 5	Bx 4	Bx 3	Bx 2	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This command returns the Bx bits (Bx[9:2]) of blue color characteristics.													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
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Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>xxh</td> </tr> <tr> <td>S/W Reset</td> <td>xxh</td> </tr> <tr> <td>H/W Reset</td> <td>xxh</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	xxh	S/W Reset	xxh	H/W Reset	xxh				
Status	Default Value													
Power On Sequence	xxh													
S/W Reset	xxh													
H/W Reset	xxh													

5.2.57. RDBy (7CH) Read By

7CH		RDBy (Read By)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDBy	Write		0	1	1	1	1	1	0	0	(7CH)
1 st Parameter	Read		By 9	By 8	By 7	By 6	By 5	By 4	By 3	By 2	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This command returns the By bits (By[9:2]) of blue color characteristics.													
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>xxh</td> </tr> <tr> <td>S/W Reset</td> <td>xxh</td> </tr> <tr> <td>H/W Reset</td> <td>xxh</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	xxh	S/W Reset	xxh	H/W Reset	xxh				
Status	Default Value													
Power On Sequence	xxh													
S/W Reset	xxh													
H/W Reset	xxh													

5.2.58. RDAX (7DH) Read Ax

7DH		RDAX (Read Ax)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDAX	Write		0	1	1	1	1	1	0	1	(7DH)
1 st Parameter	Read	Ax 9	Ax 8	Ax 7	Ax 6	Ax 5	Ax 4	Ax 3	Ax 2	xxh	

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> - This command returns the Ax bits (Ax[9:2]) of A color characteristics. - Ax[9:2] are set to ‘0’s if they are not used. 													
Restriction														
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">xxh</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">xxh</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">xxh</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	xxh	S/W Reset	xxh	H/W Reset	xxh				
Status	Default Value													
Power On Sequence	xxh													
S/W Reset	xxh													
H/W Reset	xxh													

5.2.59. RDAY (7EH) Read Ay

7EH		RDAY (Read Ay)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDAY	Write		0	1	1	1	1	1	1	0	(7EH)
1 st Parameter	Read	Ay 9	Ay 8	Ay 7	Ay 6	Ay 5	Ay 4	Ay 3	Ay 2	xxh	

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> - This command returns the Ay bits (Ay[9:2]) of A color characteristics. - Ay[9:2] are set to ‘0’s if they are not used. 													
Restriction														
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">xxh</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">xxh</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">xxh</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	xxh	S/W Reset	xxh	H/W Reset	xxh				
Status	Default Value													
Power On Sequence	xxh													
S/W Reset	xxh													
H/W Reset	xxh													

5.2.60. RDDDBSTR (A1H): Read DDB Start

A1H		RDDDBSTR (Read DDB Start)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDDBSTR	Write		1	0	1	0	0	0	0	1	(A1H)
1 st Parameter	Read		ID41 15	ID41 14	ID41 13	ID41 12	ID41 11	ID41 10	ID41 9	ID41 8	01h
2 nd Parameter	Read		ID41 7	ID41 6	ID41 5	ID41 4	ID41 3	ID41 2	ID41 1	ID41 0	8Bh
3 rd Parameter	Read		ID42 15	ID42 14	ID42 13	ID42 12	ID42 11	ID42 10	ID42 9	ID42 8	12h
4 th Parameter	Read		ID42 7	ID42 6	ID42 5	ID42 4	ID42 3	ID42 2	ID42 1	ID42 0	81h
5 th Parameter	Read		1	1	1	1	1	1	1	1	FFh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> - The command reads identifying and descriptive information from the peripheral. This information is organized in the Device Descriptor Block(DDB) stored on the peripheral. - The format of returned data is as follows: Parameter 1: MSB byte of Supplier ID. Parameter 2: LSB byte of Supplier ID. Parameter 3: MSB byte of Display module ID. Parameter 4: LSB byte of Display module ID. Parameter 5: FFh <p>The read sequence can be interrupted by any command and it can be continued by A8H command.</p>												
Restriction													
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">XXh</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">XXh</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">XXh</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	XXh	S/W Reset	XXh	H/W Reset	XXh				
Status	Default Value												
Power On Sequence	XXh												
S/W Reset	XXh												
H/W Reset	XXh												

5.2.61. RDDDBCNT (A8H): Read DDB Continue

A8H		RDDDBCNT (Read DDB Continue)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDDDBCNT	Write		1	0	1	0	1	0	0	0	(A8H)
1 st Parameter	Read		Idxx nn	xxh							
2 nd Parameter	Read		Idxx nn	xxh							
..	Read		-	-	-	-	-	-	-	-	xxh
N th Parameter	Read		Idxx nn	xxh							

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> - This command returns supplier's identification and display module model/revision information from the point where RDDDBSTR command was interrupted by an other command. - See more on A1H command. 													
Restriction														
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
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Status	Default Value													
Power On Sequence	XXh													
S/W Reset	XXh													
H/W Reset	XXh													

5.2.62. RDFCS (AAH): Read First Checksum

AAH		RDFCS (Read First Checksum)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDFCS	Write		1	0	1	0	1	0	1	0	(AAH)
1 st Parameter	Read		FCS 7	FCS 6	FCS 5	FCS 4	FCS 3	FCS 2	FCS 1	FCS 0	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> - This command returns the first checksum what has been calculated from area registers and the frame memory after the write access to those registers and/or frame memory has been done. 													
Restriction	<ul style="list-style-type: none"> - It will be necessary to wait 150ms after there is the last write access on area registers before there can read this checksum value. 													
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">00h</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">00h</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													

5.2.63. RDCCS (AFH): Read Continue Checksum

AFH		RDCCS (Read Continue Checksum)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDCCS	Write		1	0	1	0	1	1	1	1	(AFH)
1 st Parameter	Read		CCS 7	CCS 6	CCS 5	CCS 4	CCS 3	CCS 2	CCS 1	CCS 0	xxh

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from area registers and the frame memory after the write access to those registers and/or frame memory has been done.												
Restriction	- It will be necessary to wait 300ms after there is the last write access on area registers before there can read this checksum value in the first time.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

5.2.64. RDID1 (DAH): Read ID1

DAH		RDID1 (Read ID1)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID1	Write		1	1	0	1	1	0	1	0	(DAH)
1 st Parameter	Read		ID1 7	ID1 6	ID1 5	ID1 4	ID1 3	ID1 2	ID1 1	ID1 0	40h

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This read byte identifies the display module's manufacturer.													
Restriction	- None													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>40h</td> </tr> <tr> <td>S/W Reset</td> <td>40h</td> </tr> <tr> <td>H/W Reset</td> <td>40h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	40h	S/W Reset	40h	H/W Reset	40h				
Status	Default Value													
Power On Sequence	40h													
S/W Reset	40h													
H/W Reset	40h													

5.2.65. RDID2 (DBH): Read ID2

DBH		RDID2 (Read ID2)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID2	Write		1	1	0	1	1	0	1	1	(DBH)
1 st Parameter	Read		ID2 7	ID2 6	ID2 5	ID2 4	ID2 3	ID2 2	ID2 1	ID2 0	00h

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This read byte is used to track the display module/driver version. It is defined by display supplier (with agreement) and changes each time a revision is made to the display, material or construction specifications.													
Restriction	- None													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													

5.2.66. RDID3 (DBH): Read ID3

DCH		RDID3 (Read ID3)									
Inst / Para	Write/Read		D7	D6	D5	D4	D3	D2	D1	D0	(Code)
RDID3	Write		1	1	0	1	1	1	0	0	(DCH)
1 st Parameter	Read		ID3 7	ID3 6	ID3 5	ID3 4	ID3 3	ID3 2	ID3 1	ID3 0	00h

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	- This read byte identifies the display module/driver.	
Restriction	- None	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h

5.3. Command 2

5.3.1. ADRSFT (0000h): Address Shift Function

Address	00h										
Address (SPI/I2C/MDDI)	0000h (0x01 st parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	0	0	0	0	0	0	0	0	00h
Parameter	Write		SFT7	SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0	00h

Description	<ul style="list-style-type: none"> - Address shift function can be enable when EXTC=1. (EXTC bit at \$FF00h) - SFT[7:0] can define the parameter counter number of command 2 register 							
Restriction								
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>OTP un-programmed</td> <td>Set as default value</td> </tr> <tr> <td>OTP Programmed</td> <td>Set as OTP value</td> </tr> </tbody> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value	
Status	Default Value							
OTP un-programmed	Set as default value							
OTP Programmed	Set as OTP value							

5.3.2. Command 2 Mode (FF00h): Enable Access Command 2 “CMD2”

Address	FFh										
Address (SPI/I2C/MDDI)	FF00h ~ FF02h (0x01 st ~ 0x03 rd parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	1	1	1	1	1	1	FFh
1 st Parameter	Write		PW15	PW14	PW13	PW12	PW11	PW10	PW9	PW8	00h
2 nd Parameter	Write		PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0	00h
3 rd Parameter	Write		0	0	0	0	0	0	0	EXTC	00h

Description	<ul style="list-style-type: none"> - To enter in Command 2 Mode, please let PW[15:8] = 96h and PW[7:0] = 08h - To enable write function of Command 2 & enable parameter shift function, please let EXTC = 1h. 							
Restriction	<ul style="list-style-type: none"> - Read and Write, Only access when Orise mode enable. 							
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>OTP un-programmed</td> <td>Set as default value</td> </tr> <tr> <td>OTP Programmed</td> <td>Set as OTP value</td> </tr> </tbody> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value	
Status	Default Value							
OTP un-programmed	Set as default value							
OTP Programmed	Set as OTP value							

5.3.3. OTPSEL (A000h): OTP select region

Address	A0h										
Address (SPI/I2C/MDDI)	A000h (0x01 st parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	0	1	0	0	0	0	0	A0h
Parameter	Write/Read		-	-	-	reg_cm d2_swr st_ena	-	-	-	reg_gm a_otp_s el	00h

Description	Command 2 software reset enable 0 : disable cmd2 software reset 1 : enable cmd2 software reset Select Gamma OTP Region 0 : Select Gamma OTP Area 1 to program 1 : Select Gamma OTP Area 2 to program						
Restriction	- Read and Write, Only access when Orise mode enable.						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>OTP un-programmed</td> <td>Set as default value</td> </tr> <tr> <td>OTP Programmed</td> <td>Set as OTP value</td> </tr> </tbody> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value
Status	Default Value						
OTP un-programmed	Set as default value						
OTP Programmed	Set as OTP value						

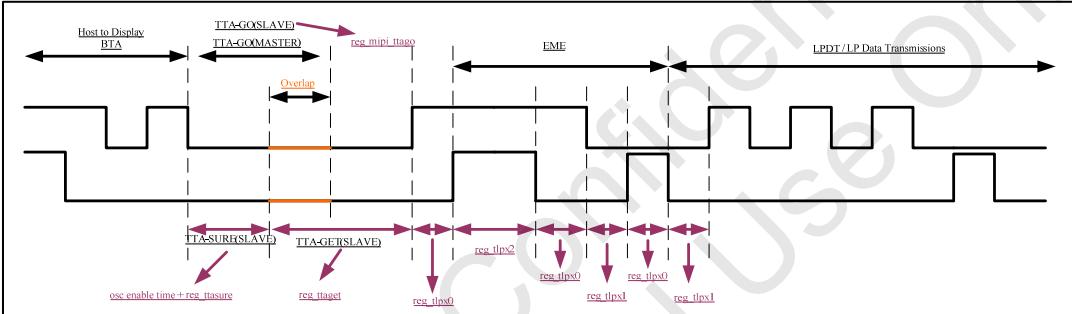
5.3.4. PGCHK (AE8Fh): OTP Programming status check

Address	Aeh										
Address (SPI/I2C/MDDI)	AE8Fh (0x90 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Read	00h	1	0	1	0	1	1	1	0	Aeh
Parameter	Write/Read				Analog Gamma	Digital Gamma	CABC	AIE	FCA1	FCA2	00h

Description	Status "0" : Never Programming Status "1" : Finish Programming Use (Aeh,D5) +(A0h,D0) together to check Analog Gamma programming status										
	Analog Gamma	OTP_SEL	Programming status								
<table border="1"> <tr> <td>0</td><td>x</td><td>No</td></tr> <tr> <td>1</td><td>0</td><td>1st</td></tr> <tr> <td>1</td><td>1</td><td>2nd</td></tr> </table>			0	x	No	1	0	1st	1	1	2nd
0	x	No									
1	0	1st									
1	1	2nd									
Restriction	- Read only, Only access when Orise mode enable.										
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>OTP un-programmed</td><td>Read as default value</td></tr> <tr> <td>OTP Programmed</td><td>Read as OTP value</td></tr> </tbody> </table>			Status	Default Value	OTP un-programmed	Read as default value	OTP Programmed	Read as OTP value		
Status	Default Value										
OTP un-programmed	Read as default value										
OTP Programmed	Read as OTP value										

5.3.5. MIPISET1 (B080h): MIPI Setting 1

Address	B0h										
Address (SPI/I2C/MDDI)	B080h ~ B083h (0x81 st ~ 0x84 rd parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	0	1	1	0	0	0	0	B0h
129 th Parameter	Write/Read		0	0	0	0			reg_mipi_tlpox0		00h
130 th Parameter	Write/Read				reg_mipi_tlpox1			reg_mipi_tlpox2			01h
131 th Parameter	Write/Read				reg_mipi_ttago			reg_mipi_ttasure			30h
132 th Parameter	Write/Read					reg_mipi_ttaget					04h

	<p>Description</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #f2e0bd;">Bit</th><th style="background-color: #f2e0bd;">Description</th><th style="background-color: #f2e0bd;">Value</th></tr> </thead> <tbody> <tr> <td>reg_mipi_tlpox0</td><td>Rx Ipm state timeout signal</td><td>step: 4'h0~4'hF (osc x (1+step))</td></tr> <tr> <td>reg_mipi_tlpox1</td><td>Rx Ipm state timeout signal</td><td>step: 4'h0~4'hF (osc x (1+step))</td></tr> <tr> <td>reg_mipi_tlpox2</td><td>RX_to_TX LP11</td><td>step: 4'h0~4'hF (osc x (1+step))</td></tr> <tr> <td>reg_mipi_ttago</td><td>Tx->Rx BTA timeout signal</td><td>step: 4'h0~4'hF (osc x (1+step))</td></tr> <tr> <td>reg_mipi_ttasure</td><td>Rx->Tx BTA timeout signal</td><td>step: 4'h0~4'hF (osc x (1+step))</td></tr> <tr> <td>reg_mipi_ttaget</td><td>Tx BTA settle timeout signal</td><td>step: 8'h0~8'hFF (osc x (1+step))</td></tr> </tbody> </table>	Bit	Description	Value	reg_mipi_tlpox0	Rx Ipm state timeout signal	step: 4'h0~4'hF (osc x (1+step))	reg_mipi_tlpox1	Rx Ipm state timeout signal	step: 4'h0~4'hF (osc x (1+step))	reg_mipi_tlpox2	RX_to_TX LP11	step: 4'h0~4'hF (osc x (1+step))	reg_mipi_ttago	Tx->Rx BTA timeout signal	step: 4'h0~4'hF (osc x (1+step))	reg_mipi_ttasure	Rx->Tx BTA timeout signal	step: 4'h0~4'hF (osc x (1+step))	reg_mipi_ttaget	Tx BTA settle timeout signal	step: 8'h0~8'hFF (osc x (1+step))	<p>Host to Display BTA</p> <p>TTA-GOMSLAVE</p> <p>TTA-GOMMASTER</p> <p>Overlap</p> <p>EME</p> <p>LPDT / LP Data Transmissions</p> <p>reg_mipi_ttago</p> <p>reg_mipi_ttaget</p> <p>reg_tpox</p> <p>reg_tpox2</p> <p>reg_tpox3</p> <p>reg_tpox4</p> <p>reg_tpox5</p> <p>reg_tpox6</p>
Bit	Description	Value																					
reg_mipi_tlpox0	Rx Ipm state timeout signal	step: 4'h0~4'hF (osc x (1+step))																					
reg_mipi_tlpox1	Rx Ipm state timeout signal	step: 4'h0~4'hF (osc x (1+step))																					
reg_mipi_tlpox2	RX_to_TX LP11	step: 4'h0~4'hF (osc x (1+step))																					
reg_mipi_ttago	Tx->Rx BTA timeout signal	step: 4'h0~4'hF (osc x (1+step))																					
reg_mipi_ttasure	Rx->Tx BTA timeout signal	step: 4'h0~4'hF (osc x (1+step))																					
reg_mipi_ttaget	Tx BTA settle timeout signal	step: 8'h0~8'hFF (osc x (1+step))																					
Restriction	<p>- Read and Write, Only access when Orise mode enable.</p>																						
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d9e1f2;">Status</th><th style="background-color: #d9e1f2;">Default Value</th></tr> </thead> <tbody> <tr> <td>OTP un-programmed</td><td>Set as default value</td></tr> <tr> <td>OTP Programmed</td><td>Set as OTP value</td></tr> </tbody> </table>		Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value															
Status	Default Value																						
OTP un-programmed	Set as default value																						
OTP Programmed	Set as OTP value																						

5.3.6. MIPISET2 (B0A1h): MIPI Setting 2

Address	B0h										
Address (SPI/I2C/MDDI)	B0A1h ~ B0A5h (0xA2 st ~ 0xA6 rd parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	0	1	1	0	0	0	0	B0h
162 th Parameter	Write/Read		0	0	reg_mipi_mp_clk_dly_sel						01h
163 th Parameter	Write/Read		0	0	reg_mipi_mp_ch0_dly_sel						00h
164 st Parameter	Write/Read		0	0	reg_mipi_mp_ch1_dly_sel						00h
165 nd Parameter	Write/Read		0	0	reg_mipi_mp_ch2_dly_sel						00h

Description	Bit			Description		Value								
	reg_mipi_mp_clk_dly_sel	MIPI clock lane delay		1step = 30pS										
	reg_mipi_mp_ch0_dly_sel	MIPI D0 lane delay		1step = 30pS										
	reg_mipi_mp_ch1_dly_sel	MIPI D1 lane delay		1step = 30pS										
	reg_mipi_mp_ch2_dly_sel	MIPI D2 lane delay		1step = 30pS										
Restriction	- Read and Write, Only access when Orise mode enable.													
Default	Status		Default Value											
	OTP un-programmed		Set as default value											
	OTP Programmed		Set as OTP value											

5.3.7. IF PARA1 (B280H) IF Parameter 1

Address	B2h										
Address (SPI/I2C/MDDI)	B280h (0x81 st parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	0	1	1	0	0	1	0	B2h
129 th Parameter	Write/Read		0	0			0	LUT_IP M[2]	LUT_IP M[1]	LUT_IP M[0]	24h

- **LUT_IPM[2:0]** : This register is used to expand data selection in 16bit mode and 18bit mode.

Data expansion table in case of Green of 16bit Mode and 18bit Mode.

IPM	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	
0	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	0	0	
1	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	0	1	
2	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	1	0	
3	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	1	1	
4	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	D[5]	D[4]	default
5	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	D[5]	0	
6	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	D[5]	1	
7	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	0	0	

Description

Data expansion table in case of Red and Blue of 16bit Mode.

IPM	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	
0	D[4]	D[3]	D[2]	D[1]	D[0]	D[4]	0	0	
1	D[4]	D[3]	D[2]	D[1]	D[0]	D[4]	0	1	
2	D[4]	D[3]	D[2]	D[1]	D[0]	D[4]	1	0	
3	D[4]	D[3]	D[2]	D[1]	D[0]	D[4]	1	1	
4	D[4]	D[3]	D[2]	D[1]	D[0]	D[4]	D[3]	D[2]	default
5	D[4]	D[3]	D[2]	D[1]	D[0]	D[4]	D[4]	0	
6	D[4]	D[3]	D[2]	D[1]	D[0]	D[4]	D[4]	1	
7	D[4]	D[3]	D[2]	D[1]	D[0]	D[4]	0	0	

Restriction

- Read and Write, Only access when Orise mode enable.
- Using parameter shift function to access 81hth parameter.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	24h
S/W Reset	24h
H/W Reset	24h

5.3.8. IF PARA3 (B282H) IF Parameter 3

Address	B2h										
Address (SPI/I2C/MDDI)	B282h (0x83 st parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	0	1	1	0	0	1	0	B2h
131 th Parameter	Write/Read		RGB_V SP	RGB_H SP	RGB_D P	RGB_E P	0	0	RGB_u pdata_f req[1]	RGB_u pdata_f req[0]	00h

Description	<p>- This command is used to set RGB IF Function.</p> <table border="1"> <tr><td>RGB_VSP</td><td>0 Vsync pulse is recognized at low</td></tr> <tr><td></td><td>1 Vsync pulse is recognized at high</td></tr> <tr><td>RGB_HSP</td><td>0 Hsync pulse is recognized at low</td></tr> <tr><td></td><td>1 Hsync pulse is recognized at high</td></tr> <tr><td>RGB_DP</td><td>0 PCLK</td></tr> <tr><td></td><td>1 PCLK inverse</td></tr> <tr><td>RGB_EP</td><td>0 DE is recognized at high</td></tr> <tr><td></td><td>1 DE is recognized at low</td></tr> </table> <p>- RGB_UPDATA_FREQ[1:0] : User could set frequency of RAM update from interface.</p> <table border="1"> <tr><td>RGB_UPDAT_FREQ[1:0] Frequency(Frame)</td></tr> <tr><td>00</td><td>1</td></tr> <tr><td>01</td><td>2</td></tr> <tr><td>10</td><td>3</td></tr> <tr><td>11</td><td>4</td></tr> </table>	RGB_VSP	0 Vsync pulse is recognized at low		1 Vsync pulse is recognized at high	RGB_HSP	0 Hsync pulse is recognized at low		1 Hsync pulse is recognized at high	RGB_DP	0 PCLK		1 PCLK inverse	RGB_EP	0 DE is recognized at high		1 DE is recognized at low	RGB_UPDAT_FREQ[1:0] Frequency(Frame)	00	1	01	2	10	3	11	4
RGB_VSP	0 Vsync pulse is recognized at low																									
	1 Vsync pulse is recognized at high																									
RGB_HSP	0 Hsync pulse is recognized at low																									
	1 Hsync pulse is recognized at high																									
RGB_DP	0 PCLK																									
	1 PCLK inverse																									
RGB_EP	0 DE is recognized at high																									
	1 DE is recognized at low																									
RGB_UPDAT_FREQ[1:0] Frequency(Frame)																										
00	1																									
01	2																									
10	3																									
11	4																									
<ul style="list-style-type: none"> - Read and Write, Only access when Orise mode enable. - Using parameter shift function to access 83hth parameter. 																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes													
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
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Status	Default Value																									
Power On Sequence	00h																									
S/W Reset	00h																									
H/W Reset	00h																									

5.3.9. CMD_PARA1 (B380H) Command Set Option Parameter 1

Address	B3h										
Address (SPI/I2C/MDDI)	B380h (0x81 st parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	0	1	1	0	0	1	1	B3h
129 th Parameter	Write/Read		Errprt_DIS	TE_DIS	I_SHUT_ENA	I_IDM_ENA	0	Getsac_n_hi[2]	Getsac_n_hi[1]	Getsac_n_hi[0]	00h

Description	<p>- This function is use to Disable/Enable Command Set Function</p> <table border="1"> <tr> <td rowspan="2">Errprt_DIS</td><td>0</td><td>Enable Error report function</td></tr> <tr> <td>1</td><td>Disable Error report function</td></tr> <tr> <td rowspan="2">TE_DIS</td><td>0</td><td>Enable TE function</td></tr> <tr> <td>1</td><td>Disable TE function</td></tr> <tr> <td rowspan="2">I_SHUT_ENA</td><td>0</td><td>Enable Power on function by SW register (11h)</td></tr> <tr> <td>1</td><td>Enable Power on function by HW pin</td></tr> <tr> <td rowspan="4">I_IDM_ENA</td><td>0</td><td>Enable Idle mode function by SW register(39h)</td></tr> <tr> <td>1</td><td>Enable Idle mode function by HW pin</td></tr> </table> <p>Note :</p> <p>(1). Errprt_DIS, Error report function means that the MIPI-DSI error-report can be read from 0Eh D0.</p> <p>- Getscan_hi[2:0] : Set TE scan line High byte</p>		Errprt_DIS	0	Enable Error report function	1	Disable Error report function	TE_DIS	0	Enable TE function	1	Disable TE function	I_SHUT_ENA	0	Enable Power on function by SW register (11h)	1	Enable Power on function by HW pin	I_IDM_ENA	0	Enable Idle mode function by SW register(39h)	1	Enable Idle mode function by HW pin
Errprt_DIS	0	Enable Error report function																				
	1	Disable Error report function																				
TE_DIS	0	Enable TE function																				
	1	Disable TE function																				
I_SHUT_ENA	0	Enable Power on function by SW register (11h)																				
	1	Enable Power on function by HW pin																				
I_IDM_ENA	0	Enable Idle mode function by SW register(39h)																				
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Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
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Power On Sequence	00h																					
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S/W Reset	00h																					
H/W Reset	00h																					
<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00h</td></tr> <tr> <td>S/W Reset</td><td>00h</td></tr> <tr> <td>H/W Reset</td><td>00h</td></tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h													
Status	Default Value																					
Power On Sequence	00h																					
S/W Reset	00h																					
H/W Reset	00h																					

5.3.10. CMD_PARA2 (B381H) Command Set Option Parameter 2

Address	B3h										
Address (SPI/I2C/MDDI)	B381h (0x82 st parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	0	1	1	0	0	1	1	B3h
130 th Parameter	Write/Read		Getsac n_lo[7]	Getsac n_lo[6]	Getsac n_lo[5]	Getsac n_lo[4]	Getsac n_lo[3]	Getsac n_lo[2]	Getsac n_lo[1]	Getsac n_lo[0]	00h

Description	- This function is use to Disable/Enable Command Set Function - Getscan_lo[7:0] : Set TE scan line Low byte												
Restriction	- Read and Write, Only access when Orise mode enable. - Using parameter shift function to access 82h th parameter.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

5.3.11. CMD PARA3 (B382H) Command Set Option Parameter 3

Address	B3h										
Address (SPI/I2C/MDDI)	B382h (0x83 st parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	0	1	1	0	0	1	1	B3h
131 th Parameter	Write/Read		36h_ML_DIS	36h_LS_B_OPT	36h_LS_B_ENA	36h_SWRST_OPT	0	3Ah_MSBR_EA_d_ena	3Ah_LSB_Only	3AH_SW_RST_OPT	00h

Description	- This function is use to Disable/Enable Command Set Function <table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td style="background-color: #ffff00;">36h_ML_DIS</td><td>0 Enable "36h" ML function</td></tr> <tr><td style="background-color: #ffff00;">36h_ML_DIS</td><td>1 Disable "36h" ML function</td></tr> <tr><td style="background-color: #ffff00;">36h_LSB_OPT</td><td>0 Image Flip at Latch</td></tr> <tr><td style="background-color: #ffff00;">36h_LSB_OPT</td><td>1 Image Flip at RAM writing</td></tr> <tr><td style="background-color: #ffff00;">36h_LSB_ENA</td><td>0 Enable Image Flip function</td></tr> <tr><td style="background-color: #ffff00;">36h_LSB_ENA</td><td>1 Disable Image Flip function</td></tr> <tr><td style="background-color: #ffff00;">36h_SW_RST_OPT</td><td>0 Command Set "36h" can be reset by Software reset (01h)</td></tr> <tr><td style="background-color: #ffff00;">36h_SW_RST_OPT</td><td>1 Command Set "36h" can not be reset by Software reset (01h)</td></tr> </table>		36h_ML_DIS	0 Enable "36h" ML function	36h_ML_DIS	1 Disable "36h" ML function	36h_LSB_OPT	0 Image Flip at Latch	36h_LSB_OPT	1 Image Flip at RAM writing	36h_LSB_ENA	0 Enable Image Flip function	36h_LSB_ENA	1 Disable Image Flip function	36h_SW_RST_OPT	0 Command Set "36h" can be reset by Software reset (01h)	36h_SW_RST_OPT	1 Command Set "36h" can not be reset by Software reset (01h)
36h_ML_DIS	0 Enable "36h" ML function																	
36h_ML_DIS	1 Disable "36h" ML function																	
36h_LSB_OPT	0 Image Flip at Latch																	
36h_LSB_OPT	1 Image Flip at RAM writing																	
36h_LSB_ENA	0 Enable Image Flip function																	
36h_LSB_ENA	1 Disable Image Flip function																	
36h_SW_RST_OPT	0 Command Set "36h" can be reset by Software reset (01h)																	
36h_SW_RST_OPT	1 Command Set "36h" can not be reset by Software reset (01h)																	
- Read and Write, Only access when Orise mode enable. - Using parameter shift function to access 83h th parameter.																		
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes					
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Partial Mode On, Idle Mode Off, Sleep Out	Yes																	
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Sleep In	Yes																	
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Status	Default Value																	
Power On Sequence	00h																	
S/W Reset	00h																	
H/W Reset	00h																	

5.3.12. CMD_PARA4 (B383H) Command Set Option Parameter 4

Address	B3h										
Address (SPI/I2C/MDDI)	B383h (0x84 st parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	0	1	1	0	0	1	1	B3h
132 th Parameter	Write/Read		21H_R EV_DIS	22H_P XOFF_DIS	26H_G M_DIS	2DH_L UT_DIS	37H_V S_DIS	44H_TE ADDR_DIS	3AH_26 2K_DIS	3AH_4 K_DIS	00h

	<p>- These registers are used to disable part of Command Set.</p> <table border="1"> <thead> <tr> <th>Bit</th><th>Name</th><th>Value</th><th colspan="2">Description</th></tr> </thead> <tbody> <tr> <td rowspan="2">D7</td><td rowspan="2">21H_REV_DIS</td><td>0</td><td colspan="2">Enable "21h" Reverse Function</td></tr> <tr> <td>1</td><td colspan="2">Disable "21h" Reverse Function</td></tr> <tr> <td rowspan="2">D6</td><td rowspan="2">22H_PXOFF_DIS</td><td>0</td><td colspan="2">Enable "22h", "23h" All Pixel On/Off Function</td></tr> <tr> <td>1</td><td colspan="2">Disable "22h", "23h" All Pixel On/Off Function</td></tr> <tr> <td rowspan="2">D5</td><td rowspan="2">26H_GM_DIS</td><td>0</td><td colspan="2">Enable "26h" Gamma Select Function</td></tr> <tr> <td>1</td><td colspan="2">Disable "26h" Gamma Select Function</td></tr> <tr> <td>D4</td><td>Reserved</td><td>0</td><td colspan="2">N/A</td></tr> <tr> <td>D3</td><td>Reserved</td><td>0</td><td colspan="2">N/A</td></tr> <tr> <td rowspan="2">D2</td><td rowspan="2">44H_TEADDR_DIS</td><td>0</td><td colspan="2">Enable TE Start Address Function</td></tr> <tr> <td>1</td><td colspan="2">Disable TE Start Address Function</td></tr> <tr> <td rowspan="2">D1</td><td rowspan="2">3AH_262K_DIS</td><td>0</td><td colspan="2">Enable 262K Color format</td></tr> <tr> <td>1</td><td colspan="2">Disable 262K Color format</td></tr> <tr> <td rowspan="2">D0</td><td rowspan="2">3AH_4K_DIS</td><td>0</td><td colspan="2">Enable 4K Color format</td></tr> <tr> <td>1</td><td colspan="2" rowspan="3">Disable 4K Color format</td></tr> </tbody> </table>	Bit	Name	Value	Description		D7	21H_REV_DIS	0	Enable "21h" Reverse Function		1	Disable "21h" Reverse Function		D6	22H_PXOFF_DIS	0	Enable "22h", "23h" All Pixel On/Off Function		1	Disable "22h", "23h" All Pixel On/Off Function		D5	26H_GM_DIS	0	Enable "26h" Gamma Select Function		1	Disable "26h" Gamma Select Function		D4	Reserved	0	N/A		D3	Reserved	0	N/A		D2	44H_TEADDR_DIS	0	Enable TE Start Address Function		1	Disable TE Start Address Function		D1	3AH_262K_DIS	0	Enable 262K Color format		1	Disable 262K Color format		D0	3AH_4K_DIS	0	Enable 4K Color format		1	Disable 4K Color format		
Bit	Name	Value	Description																																																														
D7	21H_REV_DIS	0	Enable "21h" Reverse Function																																																														
		1	Disable "21h" Reverse Function																																																														
D6	22H_PXOFF_DIS	0	Enable "22h", "23h" All Pixel On/Off Function																																																														
		1	Disable "22h", "23h" All Pixel On/Off Function																																																														
D5	26H_GM_DIS	0	Enable "26h" Gamma Select Function																																																														
		1	Disable "26h" Gamma Select Function																																																														
D4	Reserved	0	N/A																																																														
D3	Reserved	0	N/A																																																														
D2	44H_TEADDR_DIS	0	Enable TE Start Address Function																																																														
		1	Disable TE Start Address Function																																																														
D1	3AH_262K_DIS	0	Enable 262K Color format																																																														
		1	Disable 262K Color format																																																														
D0	3AH_4K_DIS	0	Enable 4K Color format																																																														
		1	Disable 4K Color format																																																														
Restriction	<ul style="list-style-type: none"> - Read and Write, Only access when Orise mode enable. - Using parameter shift function to access 84hth parameter. 																																																																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>				Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																																																	
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Sleep In	Yes																																																																
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Status	Default Value																																																																
Power On Sequence	00h																																																																
S/W Reset	00h																																																																
H/W Reset	00h																																																																

5.3.13. CMD_PARA5 (B384H) Command Set Option Parameter 5

Address	B3h										
Address (SPI/I2C/MDDI)	B384h (0x85 st parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	0	1	1	0	0	1	1	B3h
133 th Parameter	Write/Read		12H_Partial_O PT	Chksum _ram_o pt[1]	Chksum _ram_o pt[0]	0	0	0	0	0	00h

Description	<ul style="list-style-type: none"> - These registers are used to disable part of Command Set. <table border="1"> <tr> <td>12H_Partial_Opt</td><td>0 Enable All pixel on/off function in Partial mode</td></tr> <tr> <td></td><td>1 Disable All pixel on/off function in Partial mode</td></tr> </table>	12H_Partial_Opt	0 Enable All pixel on/off function in Partial mode		1 Disable All pixel on/off function in Partial mode								
12H_Partial_Opt	0 Enable All pixel on/off function in Partial mode												
	1 Disable All pixel on/off function in Partial mode												
Restriction	<ul style="list-style-type: none"> - Read and Write, Only access when Orise mode enable. - Using parameter shift function to access 85hth parameter. 												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00h</td></tr> <tr> <td>S/W Reset</td><td>00h</td></tr> <tr> <td>H/W Reset</td><td>00h</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

5.3.14. PAD PARA1 (B390H) IOPAD Parameter 1

Address	B3h										
Address (SPI/I2C/MDDI)	B390h (0x91 st parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	0	1	1	0	0	1	1	B3h
145 th Parameter	Write/Read		HW_IM[3] 3]	HW_IM[2] 2]	HW_IM[1] 1]	HW_IM[0] 0]	HW_G M[3] M[3]	HW_G M[2] M[2]	HW_G M[1] M[1]	HW_G M[0] M[0]	00h

Description	<ul style="list-style-type: none"> - These registers are used to replace the Hardware PIN. - HW_IM[3:0] : When HW_EXPEN[3] = 1 , this setting replace the Hardware PIN IM. - HW_GM[3:0] : When HW_EXPEN[2] = 1 , this setting replace the Hardware PIN GM. 													
Restriction	<ul style="list-style-type: none"> - Read and Write, Only access when Orise mode enable. - Using parameter shift function to access 85hth parameter. 													
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">00h</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">00h</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													

5.3.15. PAD PARA2 (B391H) IOPAD Parameter 2

Address	B3h										
Address (SPI/I2C/MDDI)	B391h (0x92 st parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	0	1	1	0	0	1	1	B3h
146 th Parameter	Write/Read		HW_S MX	HW_S MY	HW_SR GB	HW_C M	HW_P6 8_SW	0	HW_I2 C_SA	HW_I2 C_SA	00h

<p>- These registers are used to replace the Hardware PIN.</p>											
		Bit	Description		Value						
Description		HW_SMX	Row address order		0 : Write/Read RAM Direction from Left to Right 1 : Write/Read RAM Direction from Right to Left ※ The function only can be applied when HW_EXPEN[1] = 1. If HW_EXPEN[1] = 0, The Write/Read RAM Direction is Left to Right.						
		HW_SMY	Column address order		0 : Write/Read RAM Direction from Up to Down 1 : Write/Read RAM Direction from Down to Up ※ The function only can be applied when HW_EXPEN[1] = 1. If HW_EXPEN[1] = 0, The Write/Read RAM Direction is Up to Down.						
		HW_SRGB	RGB-BGR Order		0 : For RGB filter panel 1 : For BGR filter panel ※ The function only can be applied when HW_EXPEN[1] = 1. If HW_EXPEN[1] = 0, The order is RGB.						
		HW_CM	RAM data format Selection		0 : 24-bits/pixel (16.7M color) 1 : 18-bits/pixel(262K color) ※ The function only can be applied when COLMOD(3Ah) no setting. If COLMOD has been set, the color pixel format follow COLMOD setting. The default order is 24 bits/pixel.						
		HW_P68_SW	PIN selection at M68 I/F		0 : RWX signal is input by WRX PAD , E signal is input by RDX PAD 1 : RWX signal is input by RDX PAD , E signal is input by WRX PAD ※ The function only can be applied at M68 I/F and HW_EXPEN[1] = 1.						
Restriction		HW_I2C_SA[1:0]	Slave address at I2C I/F		00 : 1001100 01 : 1001101 10 : 1001100 11 : 1001101 ※ The function only can be applied when HW_EXPEN[1] = 1.						
		<ul style="list-style-type: none"> - Read and Write, Only access when Orise mode enable. - Using parameter shift function to access 85th parameter. 									

		Status	Availability
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
	Sleep In		Yes
		Status	Default Value
Default	Power On Sequence		00h
	S/W Reset		00h
	H/W Reset		00h

5.3.16. PAD PARA3 (B392H) IOPAD Parameter 3

Address	B3h										
Address (SPI/I2C/MDDI)	B392h (0x93 st parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	0	1	1	0	0	1	1	B3h
147 th Parameter	Write/Read		HW_EX PEN[3]	HW_EX PEN[2]	HW_EX PEN[1]	HW_EX PEN[0]	0	0	HW_md di_lane[1]	HW_md di_lane[0]	01h

Description	- These registers are used to replace the Hardware PIN. - HW_EXPEN[3:0] : Enable External Pin replacement function. - HW_mddi_lane[1:0] : 00 = MDDI 1 Lane. 01 = MDDI 2 Lane.												
Restriction	- Read and Write, Only access when Orise mode enable. - Using parameter shift function to access 85h th parameter.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>01h</td> </tr> <tr> <td>S/W Reset</td> <td>01h</td> </tr> <tr> <td>H/W Reset</td> <td>01h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	01h	S/W Reset	01h	H/W Reset	01h				
Status	Default Value												
Power On Sequence	01h												
S/W Reset	01h												
H/W Reset	01h												

5.3.17. RAM Power Control (B3C0h): SRAM setting 2

Address	B3h										
Address (SPI/I2C/MDDI)	B3C0h (0xC1 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	0	1	1	0	0	1	1	B3h
193 th Parameter	Write/Read		0	0	0	RAMOFF[1:0]		0	0	1	09h
194 th Parameter	Write/Read		rampwr on_mdd i_spi	rampwr on_mdd i_i2c	rampwr on_mdd i	rampwr on_mipi	rampwr on_i2c	rampwr on_rgb	rampwr on_spi	rampwr on_cpu	00h

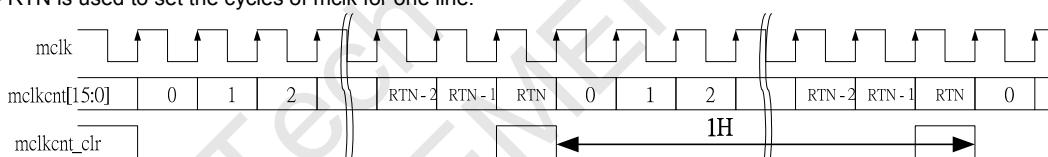
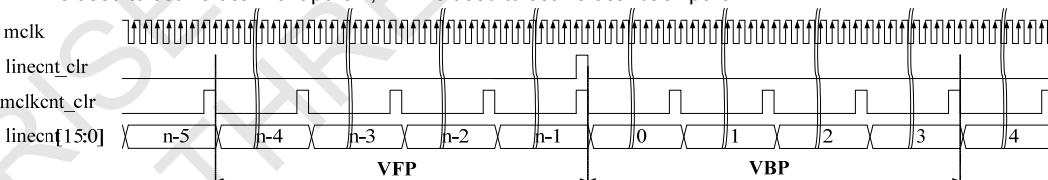
Description	Bit	Description	Value
	RAMOFF[1:0]	Turn off SRAM power condition	2'b00 : Turn off SRAM power only when reset keeps low 2'b01 : Turn off SRAM power when reset keeps low or Ultra Low Power Mode in sleep-in 2'b10 : Turn off SRAM power when reset keeps low or sleep-in
	rampwron_mddi_spi	Force turn on SRAM power during mddi_spi IF mode	1: Turn on SRAM power during sleep in mode when IM = 0100 and 1010 0: Turn off SRAM power during sleep in mode when IM = 0100 and 1010
	rampwron_mddi_i2c	Force turn on SRAM power during mddi_i2c mode	1: Turn on SRAM power during sleep in mode when IM = 1110 0: Turn off SRAM power during sleep in mode when IM = 1110
	rampwron_mddi	Force turn on SRAM power during mddi IF mode	No USE in OTM9608A
	rampwron_mipi	Force turn on SRAM power during mipi IF mode	1: Turn on SRAM power during sleep in mode when IM = 0100 0: Turn off SRAM power during sleep in mode when IM = 0100
	rampwron_i2c	Force turn on SRAM power during i2c IF mode	No USE in OTM9608A
	rampwron_rgb	Force turn on SRAM power during rgb IF mode	1: Turn on SRAM power during sleep in mode when IM = 0011, 1011 and 0111 0: Turn off SRAM power during sleep in mode when IM = 0011, 1011 and 0111
	rampwron_spi	Force turn on SRAM power during spi IF mode	No USE in OTM9608A
	rampwron_cpu	Force turn on SRAM power during cpu IF mode	1: Turn on SRAM power during sleep in mode when IM = 0000, 0001 and 0010 0: Turn off SRAM power during sleep in mode when IM = 0000, 0001 and 0010

Restriction	- Read and Write, Only access when Orise mode enable.	
Default	Status	Default Value
	OTP un-programmed	Set as default value
	OTP Programmed	Set as OTP value

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5.3.18. TSP1(C080h) TCON Setting Parameter 1

Address	C0h										
Address (SPI/I2C/MDDI)	C080h ~ C088h (0x81 st ~ 0x89 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	0	0	0	C0h
129 th Parameter	Write/Read		rtn[15]	rtn[14]	rtn[13]	rtn[12]	rtn[11]	rtn[10]	rtn[9]	rtn[8]	00h
130 th Parameter	Write/Read		rtn[7]	rtn[6]	rtn[5]	rtn[4]	rtn[3]	rtn[2]	rtn[1]	rtn[0]	48h
131 st Parameter	Write/Read		vfp[15]	vfp[14]	vfp[13]	vfp[12]	vfp[11]	vfp[10]	vfp[9]	vfp[8]	00h
132 nd Parameter	Write/Read		vfp[7]	vfp[6]	vfp[5]	vfp[4]	vfp[3]	vfp[2]	vfp[1]	vfp[0]	10h
133 rd Parameter	Write/Read		vbp[7]	vbp[6]	vbp[5]	vbp[4]	vbp[3]	vbp[2]	vbp[1]	vbp[0]	10h
134 th Parameter	Write/Read		pwrseq rtn[15]	pwrseq rtn[14]	pwrseq rtn[13]	pwrseq rtn[12]	pwrseq rtn[11]	pwrseq rtn[10]	pwrseq rtn[9]	pwrseq rtn[8]	00h
135 th Parameter	Write/Read		pwrseq rtn[7]	pwrseq rtn[6]	pwrseq rtn[5]	pwrseq rtn[4]	pwrseq rtn[3]	pwrseq rtn[2]	pwrseq rtn[1]	pwrseq rtn[0]	47h
136 th Parameter	Write/Read		pwrseq vfp[7]	pwrseq vfp[6]	pwrseq vfp[5]	pwrseq vfp[4]	pwrseq vfp[3]	pwrseq vfp[2]	pwrseq vfp[1]	pwrseq vfp[0]	10h
137 th Parameter	Write/Read		pwrseq vbp[7]	pwrseq vbp[6]	pwrseq vbp[5]	pwrseq vbp[4]	pwrseq vbp[3]	pwrseq vbp[2]	pwrseq vbp[1]	pwrseq vbp[0]	10h

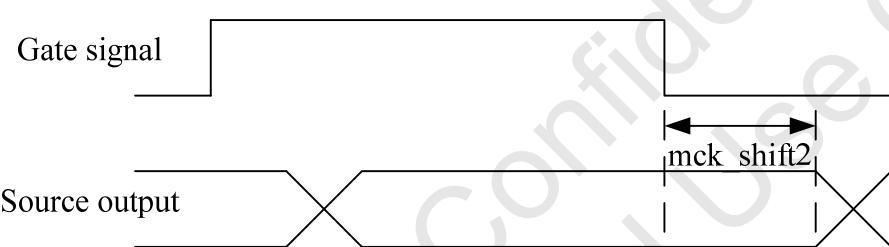
Description	- RTN is used to set the cycles of mclk for one line. 												
	- VFP is used to set Vertical front porch ; VBP is used to set Vertical back porch. 												
Restriction	- Read and Write, Only access when Orise mode enable.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												

Default	Status	Default Value
	OTP un-programmed	Set as default value
	OTP Programmed	Set as OTP value

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5.3.19. PTSP1(C092h) Panel Timing Setting Parameter 1

Address	C0h										
Address (SPI/I2C/MDDI)	C092h ~ C093h (0x93 st ~ 0x94 nd parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	0	0	0	C0h
147 th Parameter	Write/Read		mck_ shift2[1 5]	mck_ shift2[1 4]	mck_ shift2[1 3]	mck_ shift2[1 2]	mck_ shift2[1 1]	mck_ shift2[1 0]	mck_ shift2[9]	mck_ shift2[8]	00h
148 th Parameter	Write/Read		mck_ shift2[7]	mck_ shift2[6]	mck_ shift2[5]	mck_ shift2[4]	mck_ shift2[3]	mck_ shift2[2]	mck_ shift2[1]	mck_ shift2[0]	10h

Description	<ul style="list-style-type: none"> - mck_shift2 is used to control the hold timing of source output  <table border="1"> <thead> <tr> <th>mck shift2[15:0]</th><th>time unit (mclk)</th></tr> </thead> <tbody> <tr> <td>0000h</td><td>1</td></tr> <tr> <td>0001h</td><td>2</td></tr> <tr> <td>0002h</td><td>3</td></tr> <tr> <td>...</td><td>...</td></tr> <tr> <td>FFFFh</td><td>65536</td></tr> </tbody> </table>	mck shift2[15:0]	time unit (mclk)	0000h	1	0001h	2	0002h	3	FFFFh	65536
mck shift2[15:0]	time unit (mclk)												
0000h	1												
0001h	2												
0002h	3												
...	...												
FFFFh	65536												
Restriction	<ul style="list-style-type: none"> - Read and Write, Only access when Orise mode enable. 												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00h/10h</td></tr> <tr> <td>S/W Reset</td><td>00h/10h</td></tr> <tr> <td>H/W Reset</td><td>00h/10h</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h/10h	S/W Reset	00h/10h	H/W Reset	00h/10h				
Status	Default Value												
Power On Sequence	00h/10h												
S/W Reset	00h/10h												
H/W Reset	00h/10h												

5.3.20. PTSP2 (C094h) Panel Timing Setting Parameter 2

Address	C0h										
Address (SPI/I2C/MDDI)	C094h ~ C095h (0x95 st ~ 0x96 nd parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	0	0	0	C0h
149 th Parameter	Write/Read		mck_ shift3[1 5]	mck_ shift3[1 4]	mck_ shift3[1 3]	mck_ shift3[1 2]	mck_ shift3[1 1]	mck_ shift3[1 0]	mck_ shift3[9]	mck_ shift3[8]	00h
150 th Parameter	Write/Read		mck_ shift3[7]	mck_ shift3[6]	mck_ shift3[5]	mck_ shift3[4]	mck_ shift3[3]	mck_ shift3[2]	mck_ shift3[1]	mck_ shift3[0]	13h

Description	- mck_shift3 is used to control the loda location for latch control - The difference between mck_shift2 and mck_shift3 must keep three.												
	<table border="1"> <thead> <tr> <th>Mck_shift2[15:0]</th><th>time unit (mclk)</th></tr> </thead> <tbody> <tr> <td>0000h</td><td>1</td></tr> <tr> <td>0001h</td><td>2</td></tr> <tr> <td>0002h</td><td>3</td></tr> <tr> <td>...</td><td>...</td></tr> <tr> <td>FFFFh</td><td>65536</td></tr> </tbody> </table>	Mck_shift2[15:0]	time unit (mclk)	0000h	1	0001h	2	0002h	3	FFFFh	65536
Mck_shift2[15:0]	time unit (mclk)												
0000h	1												
0001h	2												
0002h	3												
...	...												
FFFFh	65536												
-													
- Read and Write, Only access when Orise mode enable.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00h/13h</td></tr> <tr> <td>S/W Reset</td><td>00h/13h</td></tr> <tr> <td>H/W Reset</td><td>00h/13h</td></tr> <tr> <td></td><td></td></tr> <tr> <td></td><td></td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h/13h	S/W Reset	00h/13h	H/W Reset	00h/13h				
Status	Default Value												
Power On Sequence	00h/13h												
S/W Reset	00h/13h												
H/W Reset	00h/13h												

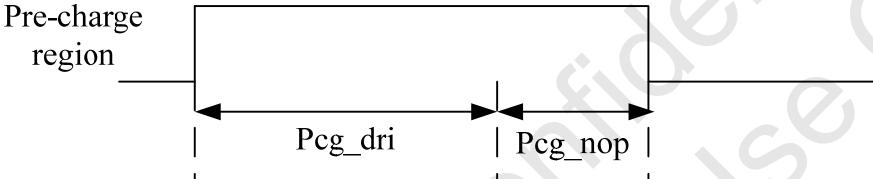
5.3.21. PTSP3 (C0A2h) Panel Timing Setting Parameter 3

C0h											
C0A2h (0xA3 rd parameter)											
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	0	0	0	C0h
163 rd Parameter	Write/Read		pl_width [7]	pl_width [6]	pl_width [5]	pl_width [4]	pl_width [3]	pl_width [2]	pl_width [1]	pl_width [0]	0Ch

Description	<ul style="list-style-type: none"> - pl_width[7:0] is used to control source driver pull low region <table border="1" style="margin-top: 5px;"> <tr> <th>pl_width[7:0]</th><th>time unit (mclk)</th></tr> <tr> <td>00h</td><td>1</td></tr> <tr> <td>01h</td><td>2</td></tr> <tr> <td>02h</td><td>3</td></tr> <tr> <td>...</td><td>...</td></tr> <tr> <td>FFh</td><td>256</td></tr> </table> 	pl_width[7:0]	time unit (mclk)	00h	1	01h	2	02h	3	FFh	256
pl_width[7:0]	time unit (mclk)												
00h	1												
01h	2												
02h	3												
...	...												
FFh	256												
Restriction	<ul style="list-style-type: none"> - Read and Write, Only access when Orise mode enable. 												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">01h</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">01h</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">01h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	01h	S/W Reset	01h	H/W Reset	01h				
Status	Default Value												
Power On Sequence	01h												
S/W Reset	01h												
H/W Reset	01h												

5.3.22. PTSP4 (C0A3h) Panel Timing Setting Parameter 4

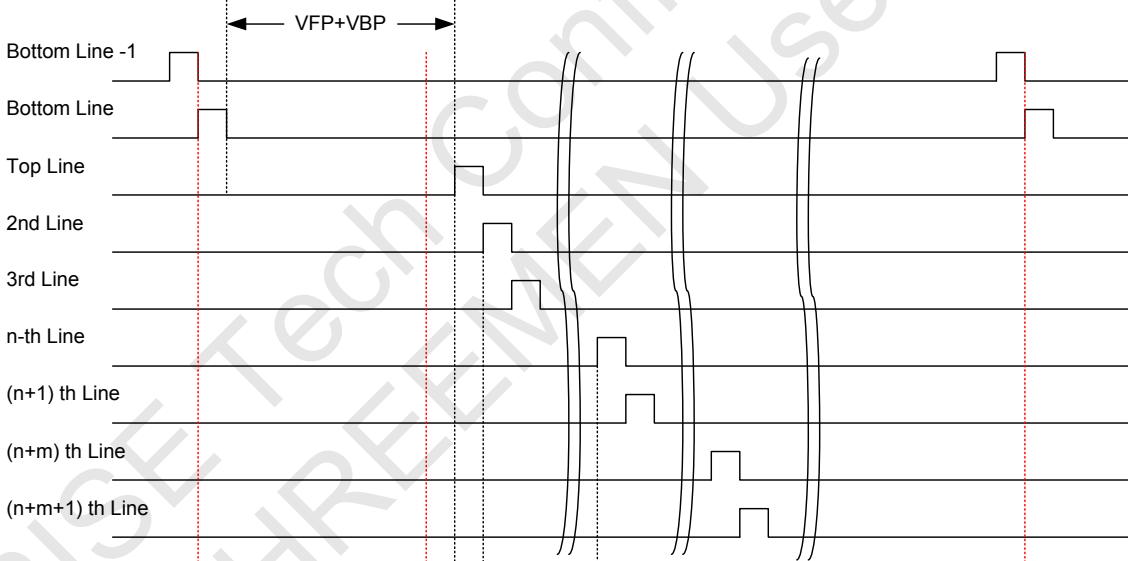
Address	C0h										
Address (SPI/I2C/MDDI)	C0A3~C0A5h (0xA4 th ~ 0xA5 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	0	0	0	C0h
164 th Parameter	Write/Read		pcg_dri [7]	pcg_dri [6]	pcg_dri [5]	pcg_dri [4]	pcg_dri [3]	pcg_dri [2]	pcg_dri [1]	pcg_dri [0]	05h
165 th Parameter	Write/Read		pcg_nop [7]	pcg_nop [6]	pcg_nop [5]	pcg_nop [4]	pcg_nop [3]	pcg_nop [2]	pcg_nop [1]	pcg_nop [0]	02h

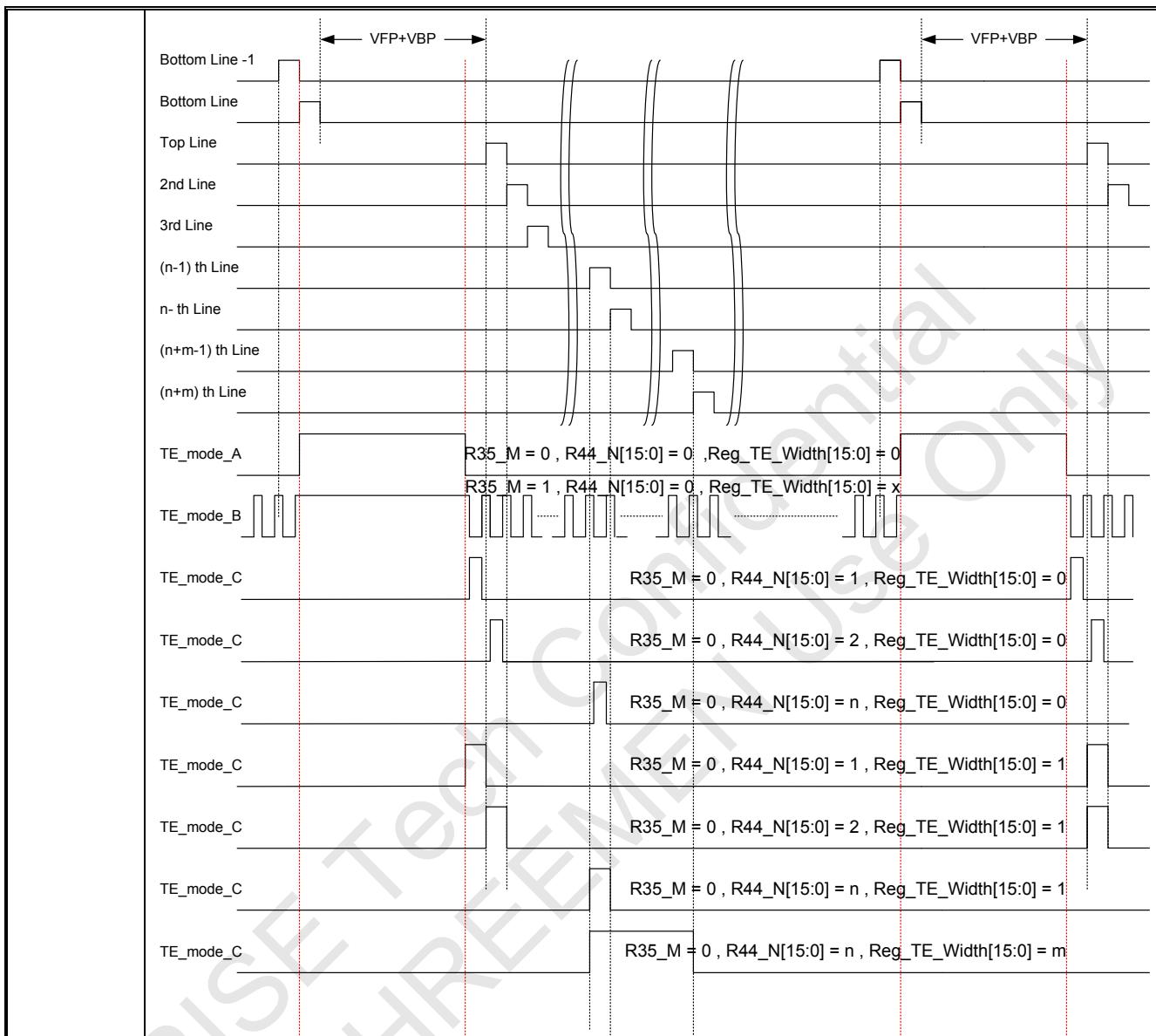
Description	<ul style="list-style-type: none"> The pcg_dri and pcg_nop command are used to define the source driver pre-charge region. 												
	<table border="1"> <thead> <tr> <th>pcg_dri[7:0]</th> <th>time unit (mclk)</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>1</td> </tr> <tr> <td>01h</td> <td>2</td> </tr> <tr> <td>02h</td> <td>3</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>FFh</td> <td>256</td> </tr> </tbody> </table>	pcg_dri[7:0]	time unit (mclk)	00h	1	01h	2	02h	3	FFh	256
pcg_dri[7:0]	time unit (mclk)												
00h	1												
01h	2												
02h	3												
...	...												
FFh	256												
Restriction	- Read and Write, Only access when Orise mode enable.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>05h/02h</td> </tr> <tr> <td>S/W Reset</td> <td>05h/02h</td> </tr> <tr> <td>H/W Reset</td> <td>05h/02h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	05h/02h	S/W Reset	05h/02h	H/W Reset	05h/02h				
Status	Default Value												
Power On Sequence	05h/02h												
S/W Reset	05h/02h												
H/W Reset	05h/02h												

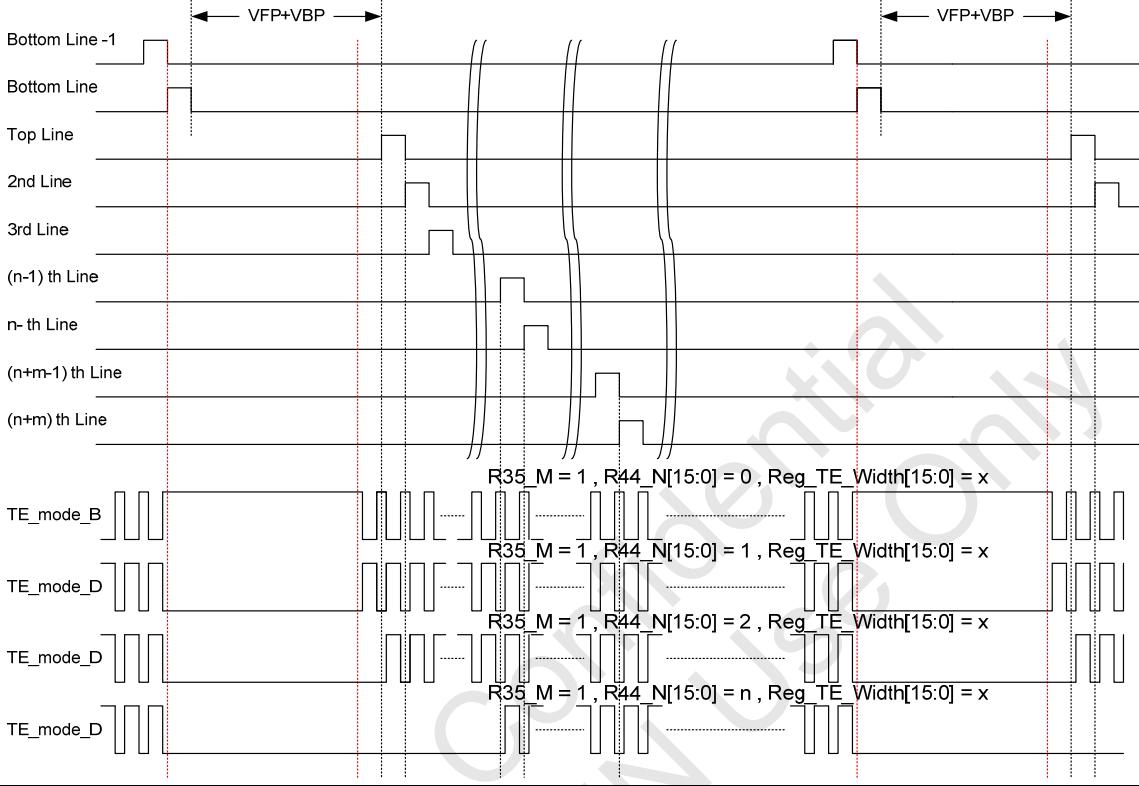
5.3.23. TE_width(C0B0)TE width Setting

Address	C0										
Address (SPI/I2C/MDDI)	C0B0h ~ C0B1h (0xB1 th ~ 0xB2 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	0	0	0	
0xB1 th Parameter	Write/Read		reg_te_width [15:8]								
0xB2 th Parameter	Write/Read		reg_te_width [7:0]								

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	There parameter are used to adjust the width of TE signal.											
	R35_M	R44_N[15:0]	TE_MODE									
	0	N == 0	Mode A									
	0	N != 0	Mode B									
	1	N == 0	Mode C									
	1	N != 0	Mode D									
												
	Bottom Line -1			VFP+VBP								
	Bottom Line											
	Top Line											
	2nd Line											
	3rd Line											
	n-th Line											
	(n+1) th Line											
	(n+m) th Line											
	(n+m+1) th Line											
	TE_mode_A			R35_M = 0 , R44_N[15:0] = 0,Reg_TE_Width[15:0] = 0								
	TE_mode_A			R35_M = 0 , R44_N[15:0] = 0,Reg_TE_Width[15:0] = 1								
	TE_mode_A			R35_M = 0 , R44_N[15:0] = 0,Reg_TE_Width[15:0] = 2								
	TE_mode_A			R35_M = 0 , R44_N[15:0] = 0,Reg_TE_Width[15:0] = n								



													
Restriction	- Read and Write, Only accessible when Orise mode is enabled												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>OTP un-programmed</td><td>Set as default value</td></tr> <tr> <td>OTP Programmed</td><td>Set as OTP value</td></tr> </tbody> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value						
Status	Default Value												
OTP un-programmed	Set as default value												
OTP Programmed	Set as OTP value												

5.3.24. TESET (C0B2)TE state Setting

Address	C0										
Address (SPI/I2C/MDDI)	C0B2h (0xB3 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	0	0	0	
0xB3 th Parameter	Write/Read		te_rev	-	-	-	-	-	-	te_disp off_opt	01h

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	There parameter are used to adjust the state of TE signal.														
	Bit	Description													
	te_rev	Reverse TE signal													
	te_dispoff_opt	TE signal state during DISPLAY OFF state													
Restriction	- Read and Write, Only accessible when Orise mode is enabled														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability														
Normal Mode On, Idle Mode Off, Sleep Out	Yes														
Normal Mode On, Idle Mode On, Sleep Out	Yes														
Partial Mode On, Idle Mode Off, Sleep Out	Yes														
Partial Mode On, Idle Mode On, Sleep Out	Yes														
Sleep In	Yes														
<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>OTP un-programmed</td><td>Set as default value</td></tr> <tr> <td>OTP Programmed</td><td>Set as OTP value</td></tr> </tbody> </table>			Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value							
Status	Default Value														
OTP un-programmed	Set as default value														
OTP Programmed	Set as OTP value														

5.3.25. ISC(C0B3h) : Interval Scan Frame Setting

Address	C0h										
Address (SPI/I2C/MDDI)	C0B3h (0xB4 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	0	0	0	C0h
180 th Parameter	Write/Read			ISC_NUM1[2:0]				ISC_NUM2[3:0]			0Fh

Description	<ul style="list-style-type: none"> - This command is used to set the interval scan frame in partial mode. - <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>ISC_NUM1[2:0]</th><th>ISC1</th><th>ISC_NUM2[3:0]</th><th>ISC2</th></tr> </thead> <tbody> <tr><td>000</td><td>0 frame</td><td>0000</td><td>0 frame</td></tr> <tr><td>001</td><td>2 frames</td><td>0001</td><td>2 frames</td></tr> <tr><td>010</td><td>4 frames</td><td>0010</td><td>4 frames</td></tr> <tr><td>011</td><td>8 frames</td><td>0011</td><td>6 frames</td></tr> <tr><td>100</td><td>16 frames</td><td>0100</td><td>8 frames</td></tr> <tr><td>101</td><td>32 frames</td><td>0101</td><td>10 frames</td></tr> <tr><td>110</td><td>64 frames</td><td>0110</td><td>12 frames</td></tr> <tr><td>111</td><td>128 frames</td><td>0111</td><td>14 frames</td></tr> <tr><td></td><td></td><td>1000</td><td>16 frames</td></tr> <tr><td></td><td></td><td>1001</td><td>18 frames</td></tr> <tr><td></td><td></td><td>1010</td><td>20 frames</td></tr> <tr><td></td><td></td><td>1011</td><td>22 frames</td></tr> <tr><td></td><td></td><td>1100</td><td>24 frames</td></tr> <tr><td></td><td></td><td>1101</td><td>26 frames</td></tr> <tr><td></td><td></td><td>1110</td><td>28 frames</td></tr> <tr><td></td><td></td><td>1111</td><td>30 frames</td></tr> </tbody> </table>	ISC_NUM1[2:0]	ISC1	ISC_NUM2[3:0]	ISC2	000	0 frame	0000	0 frame	001	2 frames	0001	2 frames	010	4 frames	0010	4 frames	011	8 frames	0011	6 frames	100	16 frames	0100	8 frames	101	32 frames	0101	10 frames	110	64 frames	0110	12 frames	111	128 frames	0111	14 frames			1000	16 frames			1001	18 frames			1010	20 frames			1011	22 frames			1100	24 frames			1101	26 frames			1110	28 frames			1111	30 frames
ISC_NUM1[2:0]	ISC1	ISC_NUM2[3:0]	ISC2																																																																		
000	0 frame	0000	0 frame																																																																		
001	2 frames	0001	2 frames																																																																		
010	4 frames	0010	4 frames																																																																		
011	8 frames	0011	6 frames																																																																		
100	16 frames	0100	8 frames																																																																		
101	32 frames	0101	10 frames																																																																		
110	64 frames	0110	12 frames																																																																		
111	128 frames	0111	14 frames																																																																		
		1000	16 frames																																																																		
		1001	18 frames																																																																		
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		1111	30 frames																																																																		
Note. Interval scan frame = ISC1 + ISC2.																																																																					
Restriction																																																																					
<ul style="list-style-type: none"> - Read and Write, Only access when Orise mode enable. 																																																																					
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Status	Default Value																																																																				
Power On Sequence	0Fh																																																																				
S/W Reset	0Fh																																																																				
H/W Reset	0Fh																																																																				

5.3.26. P_DRV_M(C0B4h) : Panel driving mode

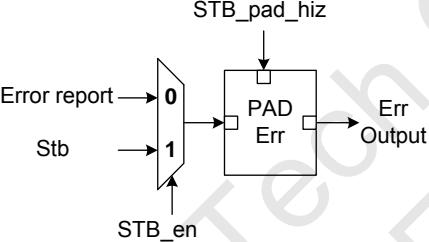
Address	C0h										
Address (SPI/I2C/MDDI)	C0B4h (0xB5 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	0	0	0	C0h
181 st Parameter	Write/Read		INV_M ODE[3]	INV_M ODE[2]	INV_M ODE[1]	INV_M ODE[0]	0	0	0	0	10h

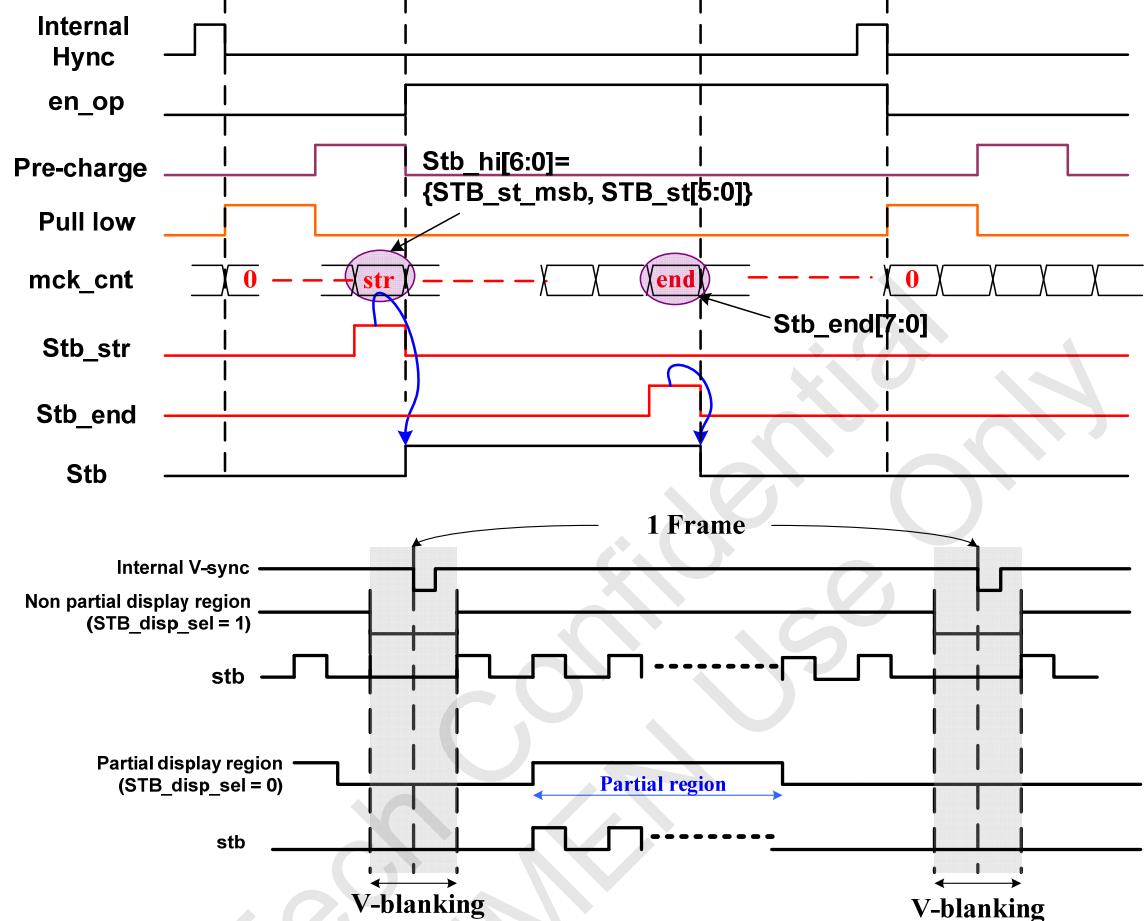
Description	<ul style="list-style-type: none"> - This command is used to set the inversion type and mode - Only Valid when following two condition is active at the same time <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #90EE90;"> <th>181th Parameter</th><th>Value</th><th>Inversion Mode Selection</th></tr> </thead> <tbody> <tr> <td rowspan="9" style="text-align: center;">INV_MODE[3:0]</td><td>0000</td><td>1 Dot Inversion</td></tr> <tr> <td>0001</td><td>1+2 Dot Inversion</td></tr> <tr> <td>0011</td><td>Pixel Inversion</td></tr> <tr> <td>0101</td><td>Column Inversion</td></tr> <tr> <td>1001</td><td>Div4 Inversion</td></tr> <tr> <td>1010</td><td>Div8 Inversion</td></tr> <tr> <td>1011</td><td>Div16 Inversion</td></tr> <tr> <td>1100</td><td>Div32 Inversion</td></tr> <tr> <td>Others</td><td>Reserved</td></tr> </tbody> </table> <p>Note : Div4/8/16/32 Inversion means polarity change per 1/4, 1/8, 1/16, 1/32 frame</p>	181 th Parameter	Value	Inversion Mode Selection	INV_MODE[3:0]	0000	1 Dot Inversion	0001	1+2 Dot Inversion	0011	Pixel Inversion	0101	Column Inversion	1001	Div4 Inversion	1010	Div8 Inversion	1011	Div16 Inversion	1100	Div32 Inversion	Others	Reserved
181 th Parameter	Value	Inversion Mode Selection																					
INV_MODE[3:0]	0000	1 Dot Inversion																					
	0001	1+2 Dot Inversion																					
	0011	Pixel Inversion																					
	0101	Column Inversion																					
	1001	Div4 Inversion																					
	1010	Div8 Inversion																					
	1011	Div16 Inversion																					
	1100	Div32 Inversion																					
	Others	Reserved																					
Restriction	<ul style="list-style-type: none"> - Read and Write, Only access when Orise mode enable. 																						
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #D9D9D9;"> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes								
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #D9D9D9;"> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>04h</td></tr> <tr> <td>S/W Reset</td><td>04h</td></tr> <tr> <td>H/W Reset</td><td>04h</td></tr> </tbody> </table>			Status	Default Value	Power On Sequence	04h	S/W Reset	04h	H/W Reset	04h												
Status	Default Value																						
Power On Sequence	04h																						
S/W Reset	04h																						
H/W Reset	04h																						

5.3.27. HSYNCOUT (C0E1h): HSYNC Output Control

Address	C0h										
Address (SPI/I2C/MDDI)	C0E1h ~ C0E3h (0xE2 th ~ 0xE4 th Parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	0	0	0	C0h
0xE2 th Parameter	Write/Read		-	STB_di sp_sel	STB_st msb	reg_stb dispoft	-	-	-	-	10h
0xE3 th Parameter	Write/Read		STB_en	STB_pa d_hiz	STB_st[5:0]					16h	
0xE4 th Parameter	Write/Read				STB_end[7:0]					48h	

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	<p>reg_stb_dispoft : Define the STB Hsync is active or not in display-off region. 0:active in display-off 1:inactive in display-off.</p> <p>Hsync start point : Register STB_st_msb & STB_st[5:0] define the start point in mck counter number.</p> <p>Hsync end point : Register STB_end[7:0] defines end point in mck counter number.</p> <p>Hsync output : Register STB_en & STB_pad_hiz control Hsync signal PAD output.</p> <p>Hsync partial mode : Register STB_disp_sel control Hsync is active or not in partial blanking area.</p>  <pre> graph LR ER[Error report 0] --> P[PAD Err] S1[Stb 1] --> P SE[STB_en] --> P P -- Err --> EO[Err Output] </pre>
-------------	--

	 <p>Internal Hync</p> <p>en_op</p> <p>Pre-charge</p> <p>Pull low</p> <p>mck_cnt</p> <p>Stb_hi[6:0]= {STB_st_msb, STB_st[5:0]}</p> <p>Stb_str</p> <p>Stb_end</p> <p>Stb</p> <p>Internal V-sync</p> <p>Non partial display region (STB_disp_sel = 1)</p> <p>Partial display region (STB_disp_sel = 0)</p> <p>stb</p> <p>stb</p> <p>1 Frame</p> <p>Partial region</p> <p>V-blanking</p> <p>V-blanking</p>						
Restriction	Only access when Orise mode enable.						
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>OTP un-programmed</td><td>Set as default value</td></tr> <tr> <td>OTP Programmed</td><td>Set as default value</td></tr> </tbody> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as default value
Status	Default Value						
OTP un-programmed	Set as default value						
OTP Programmed	Set as default value						

5.3.28. OSC_ADJ1(C181h) : Oscillator Adjustment for Idle/Normal Mode

Address	C1h										
Address (SPI/I2C/MDDI)	C181h (0x82 nd parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	0	0	1	C1h
130 th Parameter	Write/Read		0	OSC_IDLE[1]	OSC_IDLE[0]	1	0	OSC_NORM[1]	OSC_NORM[0]	1	55h

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	<ul style="list-style-type: none"> - This command is used to set the Oscillator frequency in Normal mode and Idle mode. - OSC_Idle[1:0] : Define Oscillator frequency in Idle mode. <table border="1" style="margin-left: 20px; border-collapse: collapse;"> <thead> <tr> <th>OSC_Idle[1:0]</th><th>Frame rate</th></tr> </thead> <tbody> <tr> <td>00</td><td>40Hz</td></tr> <tr> <td>01</td><td>50Hz</td></tr> <tr> <td>10</td><td>60Hz</td></tr> <tr> <td>11</td><td>70Hz</td></tr> </tbody> </table> <ul style="list-style-type: none"> - OSC_Norm[1:0] : Define Oscillator frequency in Normal mode. <table border="1" style="margin-left: 20px; border-collapse: collapse;"> <thead> <tr> <th>OSC_Norm[1:0]</th><th>Frame rate</th></tr> </thead> <tbody> <tr> <td>00</td><td>40Hz</td></tr> <tr> <td>01</td><td>50Hz</td></tr> <tr> <td>10</td><td>60Hz</td></tr> <tr> <td>11</td><td>70Hz</td></tr> </tbody> </table>	OSC_Idle[1:0]	Frame rate	00	40Hz	01	50Hz	10	60Hz	11	70Hz	OSC_Norm[1:0]	Frame rate	00	40Hz	01	50Hz	10	60Hz	11	70Hz
OSC_Idle[1:0]	Frame rate																				
00	40Hz																				
01	50Hz																				
10	60Hz																				
11	70Hz																				
OSC_Norm[1:0]	Frame rate																				
00	40Hz																				
01	50Hz																				
10	60Hz																				
11	70Hz																				
Restriction	- Read and Write, Only access when Orise mode enable.																				
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes								
Status	Availability																				
Normal Mode On, Idle Mode Off, Sleep Out	Yes																				
Normal Mode On, Idle Mode On, Sleep Out	Yes																				
Partial Mode On, Idle Mode Off, Sleep Out	Yes																				
Partial Mode On, Idle Mode On, Sleep Out	Yes																				
Sleep In	Yes																				
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>05h</td> </tr> <tr> <td>S/W Reset</td> <td>05h</td> </tr> <tr> <td>H/W Reset</td> <td>05h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	05h	S/W Reset	05h	H/W Reset	05h												
Status	Default Value																				
Power On Sequence	05h																				
S/W Reset	05h																				
H/W Reset	05h																				

5.3.29. SD_PCH_CTRL(C480h): Source Driver Precharge Control

Address	C4h										
Address (SPI/I2C/MDDI)	C480h (0x81 st parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	1	0	0	C4h
129 th Parameter	Write/Read		0	SD_PT [2]	SD_PT [1]	SD_PT [0]	0				00h
130 th Parameter	Write/Read		0	0	0	0	0	sd_sap [2:0]		04h	

	<table border="1"> <thead> <tr> <th>129rd Parameter</th><th>Value</th><th colspan="2">Source output levels during porch and non-display area</th></tr> </thead> <tbody> <tr> <td rowspan="9">SD_PT [2:0]</td><td>000</td><td colspan="2">Minimum voltage difference</td></tr> <tr> <td>001</td><td colspan="2">Maximum voltage difference</td></tr> <tr> <td>010</td><td colspan="2">Hi-Z</td></tr> <tr> <td>011</td><td colspan="2">GND</td></tr> <tr> <td>100</td><td colspan="2">Reserved</td></tr> <tr> <td>101</td><td colspan="2">Reserved</td></tr> <tr> <td>110</td><td colspan="2">Reserved</td></tr> <tr> <td>111</td><td colspan="2">Reserved</td></tr> </tbody> </table>		129 rd Parameter	Value	Source output levels during porch and non-display area		SD_PT [2:0]	000	Minimum voltage difference		001	Maximum voltage difference		010	Hi-Z		011	GND		100	Reserved		101	Reserved		110	Reserved		111	Reserved	
129 rd Parameter	Value	Source output levels during porch and non-display area																													
SD_PT [2:0]	000	Minimum voltage difference																													
	001	Maximum voltage difference																													
	010	Hi-Z																													
	011	GND																													
	100	Reserved																													
	101	Reserved																													
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5.3.30. DC2DCSET(C4A0h): DC2DC setting 1

Address (MIPI)		C4h									
Address (Other I/F)		C4A1h~ C4A8h(0xA1 th ~0xA8 th parameter)									
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	1	0	0	C4h
161 th Parameter	Write/Read		ddc_pf mdb_p [2:0]			ddc_dt2p [4:0]					33h
162 th Parameter	Write/Read		0	ddc_dt1pmin [1:0]		ddc_dt1p [4:0]					09h
163 th Parameter	Write/Read		ddc_dt1pmax [3:0]				0	ddc_dc_p_ena	ddc_sm_p_p	ddc_fix_duty_p	94h
164 th Parameter	Write/Read		ddc_drvp_p [1:0]		ddc_vref_sel_p [4:0]						2bh
165 th Parameter	Write/Read		ddc_pf mdb_n [2:0]			ddc_dt2n [4:0]					33h
166 th Parameter	Write/Read			ddc_dt1nmin [1:0]	ddc_dt1n [4:0]					09h	
167 th Parameter	Write/Read		ddc_dt1nmax [3:0]				0	ddc_dc_n_ena	ddc_sm_p_n	ddc_fix_duty_n	94h
168 th Parameter	Write/Read			ddc_drvp_n[1:0]	ddc_vref_sel_n [4:0]					54h	

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	Control register for		
	Bit	Description	Value
	ddc_pf mdb_p[2:0]	DC2DC PFM detect de-bounce time setting	3'b000 : 4pclk 3'b001 : 8pclk 3'b110 : 28pclk 3'b111 : 30pclk
	ddc_dt2p[4:0]	DC2DC (T2) Postive PFM operating frequency select	5'b00000 : 1pclk 5'b00001 : 2pclk 5'b11111 : 32pclk
	ddc_dt1pmin[1:0]	DC2DC Set the minimum duty of PFM operating frequency when I_PFM_COMP_P=L	2'b00 : 0pclk (Default) 2'b01 : 1pclk 2'b10 : 2pclk 2'b11 : 3pclk
	ddc_dt1p[4:0]	DC2DC (T1) Postive PFM Duty	5'b00000 : 1pclk 5'b00001 : 2pclk 5'b11111 : 32pclk
	ddc_dt1pmax[3:0]	DC2DC Max. T1 setting	4'b0000 : 1pclk 4'b0001 : 2pclk

		4'b1111 : 16pclk																																																																								
ddc_dcp_ena	DC2DC PFM_P Enable	0 : Disable Positive DC2DC 1 : Enable Positive EC2DC																																																																								
ddc_smp_p	DC2DC PFM_P SMP/HOLD Mode select	0 : Not Gating PFM Duty Clock when SMP=H 1 : Gating PFM Duty Clock when SMP=H																																																																								
ddc_fix_duty_p	DC2DC Fix DC2DC_P Duty Adjust(1)	0 : Adjust PFM Duty 1 : Not Adjust PFM Duty																																																																								
ddc_drvp_p[1:0]	DC2DC Driving capacity of DC2DCP driver	2'b00 : Level 1 (Weak) 2'b01 : Level 2 (Default) 2'b10 : Level 3 2'b11 : Level (Strong)																																																																								
ddc_vref_sel_p[4:0]	DC2DC Voltage setting of VDDA	<table border="1"> <thead> <tr> <th>VREF_SEL [4:0]</th> <th>VDDA</th> <th>VREF_SEL [4:0]</th> <th>VDDA</th> <th>VREF_SEL [4:0]</th> <th>VDDA</th> <th>VREF_SEL [4:0]</th> <th>VDDA</th> </tr> </thead> <tbody> <tr><td>1F</td><td>7</td><td>17</td><td>6.2</td><td>F</td><td>5.4</td><td>7</td><td>4.6</td></tr> <tr><td>1E</td><td>6.9</td><td>16</td><td>6.1</td><td>E</td><td>5.3</td><td>6</td><td>4.5</td></tr> <tr><td>1D</td><td>6.8</td><td>15</td><td>6</td><td>D</td><td>5.2</td><td>5</td><td>4.4</td></tr> <tr><td>1C</td><td>6.7</td><td>14</td><td>5.9</td><td>C</td><td>5.1</td><td>4</td><td>4.3</td></tr> <tr><td>1B</td><td>6.6</td><td>13</td><td>5.8</td><td>B</td><td>5</td><td>3</td><td>4.2</td></tr> <tr><td>1A</td><td>6.5</td><td>12</td><td>5.7</td><td>A</td><td>4.9</td><td>2</td><td>4.1</td></tr> <tr><td>19</td><td>6.4</td><td>11</td><td>5.6</td><td>9</td><td>4.8</td><td>1</td><td>4</td></tr> <tr><td>18</td><td>6.3</td><td>10</td><td>5.5</td><td>8</td><td>4.7</td><td>0</td><td>3.9</td></tr> </tbody> </table>	VREF_SEL [4:0]	VDDA	VREF_SEL [4:0]	VDDA	VREF_SEL [4:0]	VDDA	VREF_SEL [4:0]	VDDA	1F	7	17	6.2	F	5.4	7	4.6	1E	6.9	16	6.1	E	5.3	6	4.5	1D	6.8	15	6	D	5.2	5	4.4	1C	6.7	14	5.9	C	5.1	4	4.3	1B	6.6	13	5.8	B	5	3	4.2	1A	6.5	12	5.7	A	4.9	2	4.1	19	6.4	11	5.6	9	4.8	1	4	18	6.3	10	5.5	8	4.7	0	3.9
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ddc_dt1n[4:0]	DC2DC (T1) Negative PFM Duty	5'b00000 : 1pclk 5'b00001 : 2pclk 5'b11111 : 32pclk																																																																								
ddc_dt1nmax[3:0]	DC2DC Max. T1 setting	4'b0000 : 1pclk 4'b0001 : 2pclk 4'b1111 : 16pclk																																																																								
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ddc_drvp_n[1:0]	DC2DC Driving capacity of DC2DCN driver	2'b00 : Level 1 (Weak) 2'b01 : Level 2 (Default) 2'b10 : Level 3 2'b11 : Level (Strong)																																																																															
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5.3.31. PWR_CTRL1(C580h): Power Control Setting 1

Address (MIPI)		C5h											
Address (Other I/F)		C581h~ C588h(0x81st ~ 0x88th parameter)											
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default		
Instruction	Write	00h	1	1	0	0	0	1	0	1	C5h		
129 th Parameter	Write/Read		pump1_en_asdm	pump1_en_asdm_pwron	pump1_en_asdm_m2	pump4_en_asdm_hv	pump1_soft_dm [1:0]		pump1_det_frm [1:0]		F3h		
130 th Parameter	Write/Read			pump1_max_dm[2:0]			0	pump1_min_dm[2:0]			00h		
131 th Parameter	Write/Read			pump1_ss_width [1:0]		pump1_clamp [1:0]		goa_vgho_s [2:0]			90h		
132 th Parameter	Write/Read		0	goa_vgh2_s[2:0]			0	goa_vglo_s [2:0]			00h		

Description	<ul style="list-style-type: none"> - This command is used to adjust analog power behavior. - Pump ratio value will be adjusted automatically when auto setting function is active. When auto setting function is off, pump ratio will be decided by manual setting. 														
	129th Parameter	Value	Description												
	pump1_en_asdm	0	Disable AVDD Pump auto setting for LVD condition after Power on sequence												
		1	Enable AVDD Pump auto setting for LVD condition after Power on sequence												
	pump1_en_asdm_pwron	0	Disable AVDD Pump auto setting for LVD condition in Power on sequence												
		1	Enable AVDD Pump auto setting for LVD condition in Power on sequence												
	pump1_en_asdm2	0	Disable AVDD Pump auto setting for DLVD condition												
		1	Enable AVDD Pump auto setting for DLVD condition												
	pump4_en_asdm_hv	0	Disable VGH Pmp4 auto setting												
		1	Enable VGH Pmp4 auto setting												
	pump1_soft_dm [1:0]	0~3	AVDD PUMP power-on dm increase max. value												
			<table border="1" style="width: 100%;"><tr> <td>pump1_soft_dm [1]</td> <td>pump1_soft_dm [0]</td> <td>VDDA pump-ratio</td> </tr> <tr> <td>0</td> <td>0</td> <td>1.0*VDD</td> </tr> <tr> <td>0</td> <td>1</td> <td>1.5*VDD</td> </tr> <tr> <td>1</td> <td>0</td> <td>2.0*VDD</td> </tr> <tr> <td>1</td> <td>1</td> <td>3.0*VDD</td> </tr></table>	pump1_soft_dm [1]	pump1_soft_dm [0]	VDDA pump-ratio	0	0	1.0*VDD	0	1	1.5*VDD	1	0	2.0*VDD
pump1_soft_dm [1]	pump1_soft_dm [0]	VDDA pump-ratio													
0	0	1.0*VDD													
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1	0	2.0*VDD													
1	1	3.0*VDD													
<table border="1" style="width: 100%;"><tr> <td>pump1_det_frm [1]</td> <td>pump1_det_frm [0]</td> <td>Detect Counter</td> </tr> <tr> <td>0</td> <td>0</td> <td>512 Frames</td> </tr> <tr> <td>0</td> <td>1</td> <td>2048 Frames</td> </tr> <tr> <td>1</td> <td>0</td> <td>8192 Frames</td> </tr> <tr> <td>1</td> <td>1</td> <td>32768 Frames</td> </tr></table>	pump1_det_frm [1]	pump1_det_frm [0]	Detect Counter	0	0	512 Frames	0	1	2048 Frames	1	0	8192 Frames	1	1	32768 Frames
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130th Parameter	Value	Description													
pump1_max_dm[2:0]	0~7	PUMP1 max DM after Power On Sequence													
pump1_min_dm[2:0]	0~7	PUMP1 min DM after Power On Sequence													

131 st Parameter	Value	Max. AVDDP1 Pump Ratio for auto setting (Normal Display)		
pump1_ss_width [1:0]	0~3	PUMP1 soft ware start pulse width pump1_ss_width [1] pump1_ss_width [0]	Soft Start Pulse width	
		0 0	25 Lines	
		0 1	27 Lines	
		1 0	29 Lines	
		1 1	BP+FP-2 Lines	
pump1_clamp [1:0]	0~3	Setting the clamp level of VDDA		
		pump1_clamp [1]	pump1_clamp [0]	Clamp voltage of VDDA
		0 0	5.75 V	
		0 1	6.00 V	
		1 0	6.25 V	
		1 1	6.50 V	
goa_vgho_s [2:0]	0~7	GOA_EN_VGHO="1"		
		GOA_VGHO_S[2]	VGHO	
		0 VGH		
		1 VRGH		
		GOA_EN_VGHO="0"		
		GOA_VGHO_S[1:0]	VGHO	
		2'b00 VGH		
		2'b01 VSS		
		2'b10 Hi-Z		
		2'b11 Hi-Z		
132 Parameter	Value	Min. AVDDP1 Pump Ratio for auto setting (Normal Display)		
goa_vgh2_s[2:0]	0~7	GOA_EN_VGH2="1"		
		GOA_VGH2_S[2]	VGH2	
		0 VGH		
		1 VRGH		
		GOA_EN_VGH2="0"		
		GOA_VGH2_S[1:0]	VGH2	
		2'b00 VGH		
		2'b01 VSS		
		2'b10 Hi-Z		
		2'b11 Hi-Z		
goa_vglo_s [2:0]	0~7	GOA_EN_VGLO="1"		
		GOA_VGLO_S[2]	VGLO	
		0 VGL		
		1 VGL_REG		
		GOA_EN_VGLO="0"		
		GOA_VGLO_S[1:0]	VGLO	
		2'b00 VGL		
		2'b01 VSS		
		2'b10 Hi-Z		
		2'b11 Hi-Z		

Restriction	- Read and Write, Only access when Orise mode enable.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>OTP un-programmed</td><td>Set as default value</td></tr> <tr> <td>OTP Programmed</td><td>Set as OTP value</td></tr> </tbody> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value						
Status	Default Value												
OTP un-programmed	Set as default value												
OTP Programmed	Set as OTP value												

5.3.32. PWR_CTRL2(C590h): Power Control Setting 2 for Normal Mode

Address	C5h										
Address (SPI/I2C/MDDI)	C591h~ C597h (0x91 st ~ 0x97 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	1	0	1	C5h
145 th Parameter	Write/Read		pump1_dm_n [1:0]	pump1_det_n [1:0]	0		pump1_dlvd_sel_n [2:0]				84h
146 th Parameter	Write/Read		pump4_vghs_n [3:0]			pump5_vgls_n [3:0]					79h
147 th Parameter	Write/Read		pump1_ck_end_sel [1:0]	pump2_ck_end_sel [1:0]	0	pump4_x6_n	pump5_x4_n	pump45_x6_n			00h
148 th Parameter	Write/Read		hvreg_vrhs_n [3:0]			hvreg_vglreg_s_n [3:0]					33h
149 th Parameter	Write/Read		0	pump1_clk_ratio_n [2:0]		0	pump2_clk_ratio_n [2:0]				33h
150 th Parameter	Write/Read		0	pump3_clk_ratio_n [2:0]		0	pump4_clk_ratio_n [2:0]				33h
151 th Parameter	Write/Read			analog_ibias_gp_n [2:0]		0	analog_ibias_ap_n [2:0]				34h

Description	- This command is used to adjust various pump settings for Normal Mode .									
	145 th Parameter	Value	Description							
	pump1_dm_n [1:0]	0~3	PUMP1 DM in normal display region and DM auto setting disable in Normal Mode							
			pump1_dm_n [1]		pump1_dm_n [0]		VDDA pump-ratio			
			0	0	0	1	1.0*VDD			
			0	1	0	1	1.5*VDD			
			1	0	1	0	2.0*VDD			
	pump1_det_n [1:0]	0~3	PUMP1 VDDA low-voltage detection in Normal Mode							
			pump1_det_n [1]		pump1_det_n [0]		LVD level of VDDA			
			0	0	0	1	GVDD+0.3V			
			0	1	1	0	GVDD+0.4V			
			1	0	0	1	GVDD+0.5V			
	pump1_dlvd_sel_n [2:0]	0~7	PUMP1 VDDA Dlow-voltage detection in Normal Mode							
			pump1_dlvd_sel_n [2]		pump1_dlvd_sel_n [1]		pump1_dlvd_sel_n [0]		DLVD level of VDDA	
			0	0	0	1	0	1	1	GVDD+1.4V
			0	0	1	0	1	0	0	GVDD+1.3V
			0	1	0	1	0	1	0	GVDD+1.2V
			0	1	1	0	1	1	0	GVDD+1.1V
			1	0	0	1	0	0	1	GVDD+1.0V
			1	0	1	0	1	1	0	GVDD+0.9V
			1	1	1	0	0	1	1	GVDD+0.8V
			1	1	1	1	1	0	1	GVDD+0.7V

146 th Parameter				Value	Description				
PUMP4 VGH voltage select in Normal Mode									
pump4_vghs_n [3:0]		0~15	pump4_vghs_n[3:0]	VGH Voltage	pump4_vghs_n[3:0]	VGH Voltage			
			4'b0000	11.5 V	4'b1000	15.5 V			
			4'b0001	12.0 V	4'b1001	16.0 V			
			4'b0010	12.5 V	4'b1010	16.5 V			
			4'b0011	13.0 V	4'b1011	17.0 V			
			4'b0100	13.5 V	4'b1100	17.5 V			
			4'b0101	14.0 V	4'b1101	18.0 V			
			4'b0110	14.5 V	4'b1110	18.5 V			
			4'b0111	15.0 V	4'b1111	19.0 V			
pump5_vgls_n [3:0]			PUMP5 VGL voltage select in Normal Mode						
			pump5_vgls_n[3:0]	VGL Voltage	pump5_vgls_n[3:0]	VGL Voltage			
			4'b0000	-7.0 V	4'b1000	-11.5 V			
			4'b0001	-7.5 V	4'b1001	-12.0 V			
			4'b0010	-8.0 V	4'b1010	-12.5 V			
			4'b0011	-8.5 V	4'b1011	-13.0 V			
			4'b0100	-9.0 V	4'b1100	-14.0 V			
			4'b0101	-9.5 V	4'b1101	-14.5 V			
			4'b0110	-10.0 V	4'b1110	-15.0 V			
			4'b0111	-11.0 V	4'b1111	-15.5 V			

147 th Parameter				Value	Description						
When EXBIT pin =1 , AVDD Pump clock still active until Pump clock end. It's used for the fine-tuning of booster control timing.											
pump1_ck_end_sel [1:0]		0~3	pump1_ck_end_sel [1]	pump1_ck_end_sel [0]	Additional AVDD Pump Clock						
			0	0	5 Pump Clock						
			0	1	7 Pump Clock						
			1	0	9 Pump Clock						
pump2_ck_end_sel [1:0]		0~3	When EXBIT pin=1, NAVDD Pump clock still active until Pump clock end It's used for the fine-tuning of booster control timing.								
			pump2_ck_end_sel [1]	pump2_ck_end_sel [0]	Additional NAVDD Pump Clock						
			0	0	5 Pump Clock						
			0	1	7 Pump Clock						
pump4_x6_n		0	VGH = 8 X VDD, Only Valid when PUMP4_EN_ASDM_HV = "0"								
		1	VGH = 6 X VDD, Only Valid when PUMP4_EN_ASDM_HV = "0"								
pump5_x4_n		0	VGL = -6 X VDD, Only Valid when PUMP4_EN_ASDM_HV = "0"								
		1	VGL = -4 X VDD, Only Valid when PUMP4_EN_ASDM_HV = "0"								
pump45_x6_n		0	Set VGH by pump4_x6_n & set VGL by pump5_x4_n, Only Valid when PUMP4_EN_ASDM_HV = "0"								
		1	Set VGH = 6 X VDD & VGL = -6 X VDD , Only Valid when PUMP4_EN_ASDM_HV = "0"								

148 th Parameter	Value	Description			
hvreg_vrgh_s_n [3:0]	0~7	HV-regulator VRGH voltage select in Normal Mode			
		HVREG_VRGH_S[3:0]	VRGH Voltage	HVREG_VRGH_S[3:0]	VRGH Voltage
		4'b0000	8.5 V	4'b1000	12.5 V
		4'b0001	9 V	4'b1001	13 V
		4'b0010	9.5 V	4'b1010	13.5 V
		4'b0011	10 V	4'b1011	14 V
		4'b0100	10.5 V	4'b1100	14.5 V
		4'b0101	11 V	4'b1101	15 V
		4'b0110	11.5 V	4'b1110	15.5 V
		4'b0111	12 V	4'b1111	16 V
hvreg_vglreg_s_n [3:0]	0~7	HV-regulator VGL-REG voltage select in Normal Mode			
		HVREG_VGLREG_S[3:0]	VGL_REG Voltage	HVREG_VGLREG_S[3:0]	VGL_REG Voltage
		4'b0000	-7.0 V	4'b1000	-11.5 V
		4'b0001	-7.5 V	4'b1001	-12.0 V
		4'b0010	-8.0 V	4'b1010	-12.5 V
		4'b0011	-8.5 V	4'b1011	-13.0 V
		4'b0100	-9.0 V	4'b1100	-14.0 V
		4'b0101	-9.5 V	4'b1101	-14.5 V
		4'b0110	-10.0 V	4'b1110	-15.0 V
		4'b0111	-11.0 V	4'b1111	-15.5 V
149 th Parameter	Value	Description			
pump1_clk_ratio_n [2:0]	0~7	PUMP1 set pump clock ratio			
		pump1_clk_ratio_n [2:0]	VDDA Pump Clock Frequency		
		3'b000	8 Lines		
		3'b001	4 Lines		
		3'b010	2 Lines		
		3'b011	1 Line		
		3'b100	1 / 2 Line		
		3'b101	1 / 4 Line		
		3'b110	1 / 8 Line		
		3'b111	1 / 16 Line		
pump2_clk_ratio_n [2:0]	0~7	PUMP2 set pump clock ratio			
		pump2_clk_ratio_n [2:0]	NVDDA Pump Clock Frequency		
		3'b000	8 Lines		
		3'b001	4 Lines		
		3'b010	2 Lines		
		3'b011	1 Line		
		3'b100	1 / 2 Line		
		3'b101	1 / 4 Line		
		3'b110	1 / 8 Line		
		3'b111	1 / 16 Line		

150th Parameter	Value	Description																			
pump3_clk_ratio_n [2:0]	0~7	PUMP3 set pump clock ratio <table border="1"> <tr> <td>pump3_clk_ratio_n [2:0]</td><td>VCL Pump Clock Frequency</td></tr> <tr> <td>3'b000</td><td>8 Lines</td></tr> <tr> <td>3'b001</td><td>4 Lines</td></tr> <tr> <td>3'b010</td><td>2 Lines</td></tr> <tr> <td>3'b011</td><td>1 Line</td></tr> <tr> <td>3'b100</td><td>1 / 2 Line</td></tr> <tr> <td>3'b101</td><td>1 / 4 Line</td></tr> <tr> <td>3'b110</td><td>1 / 8 Line</td></tr> <tr> <td>3'b111</td><td>1 / 16 Line</td></tr> </table>		pump3_clk_ratio_n [2:0]	VCL Pump Clock Frequency	3'b000	8 Lines	3'b001	4 Lines	3'b010	2 Lines	3'b011	1 Line	3'b100	1 / 2 Line	3'b101	1 / 4 Line	3'b110	1 / 8 Line	3'b111	1 / 16 Line
pump3_clk_ratio_n [2:0]	VCL Pump Clock Frequency																				
3'b000	8 Lines																				
3'b001	4 Lines																				
3'b010	2 Lines																				
3'b011	1 Line																				
3'b100	1 / 2 Line																				
3'b101	1 / 4 Line																				
3'b110	1 / 8 Line																				
3'b111	1 / 16 Line																				
pump4_clk_ratio_n [2:0]	0~7	PUMP4 set pump clock ratio <table border="1"> <tr> <td>pump4_clk_ratio_n [2:0]</td><td>VGH/VGL Pump Clock Frequency</td></tr> <tr> <td>3'b000</td><td>8 Lines</td></tr> <tr> <td>3'b001</td><td>4 Lines</td></tr> <tr> <td>3'b010</td><td>2 Lines</td></tr> <tr> <td>3'b011</td><td>1 Line</td></tr> <tr> <td>3'b100</td><td>1 / 2 Line</td></tr> <tr> <td>3'b101</td><td>1 / 4 Line</td></tr> <tr> <td>3'b110</td><td>1 / 8 Line</td></tr> <tr> <td>3'b111</td><td>1 / 16 Line</td></tr> </table>		pump4_clk_ratio_n [2:0]	VGH/VGL Pump Clock Frequency	3'b000	8 Lines	3'b001	4 Lines	3'b010	2 Lines	3'b011	1 Line	3'b100	1 / 2 Line	3'b101	1 / 4 Line	3'b110	1 / 8 Line	3'b111	1 / 16 Line
pump4_clk_ratio_n [2:0]	VGH/VGL Pump Clock Frequency																				
3'b000	8 Lines																				
3'b001	4 Lines																				
3'b010	2 Lines																				
3'b011	1 Line																				
3'b100	1 / 2 Line																				
3'b101	1 / 4 Line																				
3'b110	1 / 8 Line																				
3'b111	1 / 16 Line																				
151th Parameter	Value	Bias Current Selection																			
analog_ibias_gp_n [2:0]	000	2.0 uA																			
	001	2.5 uA																			
	010	3.0 uA																			
	011	3.5 uA																			
	100	4.0 uA																			
	101	4.5 uA																			
	110	5.0 uA																			
	111	5.5 uA																			
151th Parameter	Value	Trim Bias Current																			
analog_ibias_ap_n [2:0]	000	60%																			
	001	60%																			
	010	70%																			
	011	85%																			
	100	100%																			
	101	120%																			
	110	140%																			
	111	160%																			
Restriction	- Read and Write, Only access when Orise mode enable.																				
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>OTP un-programmed</td><td>Set as default value</td></tr> <tr> <td>OTP Programmed</td><td>Set as OTP value</td></tr> </tbody> </table>			Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value												
Status	Default Value																				
OTP un-programmed	Set as default value																				
OTP Programmed	Set as OTP value																				

5.3.33. PWR_CTRL3(C5A0h): Power Control Setting 3 for Idle Mode

Address	C5h										
Address (SPI/I2C/MDDI)	C5A1h~ C5A7h (0xA1 st ~ 0xA7 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	1	0	1	C5h
161 th Parameter	Write/Read		pump1_dm_i [1:0]	pump1_det_i [1:0]	0		pump1_dlvd_sel_i [2:0]				84h
162 th Parameter	Write/Read		pump4_vghs_i [3:0]			pump5_vgls_i [3:0]					79h
163 th Parameter	Write/Read		0		0		0	pump4_x6_i	pump5_x4_i	pump45_x6_i	00h
164 th Parameter	Write/Read		hvreg_vrhs_s_i [3:0]			hvreg_vglreg_s_i [3:0]					33h
165 th Parameter	Write/Read		0	pump1_clk_ratio_i [2:0]		0	pump2_clk_ratio_i [2:0]				33h
166 th Parameter	Write/Read		0	pump3_clk_ratio_i [2:0]		0	pump4_clk_ratio_i [2:0]				33h
167 th Parameter	Write/Read		analog_ibias_gp_i [2:0]			0	analog_ibias_ap_i [2:0]				34h

Description	- This command is used to adjust various pump settings for IDLE Mode .									
	161 th Parameter	Value	Description							
	pump1_dm_i [1:0]	0~3	PUMP1 DM in idle display region and DM auto setting disable in idle Mode							
			pump1_dm_i [1]	pump1_dm_i [0]	VDDA pump-ratio					
			0	0	1.0*VDD					
			0	1	1.5*VDD					
			1	0	2.0*VDD					
	pump1_det_i [1:0]	0~3	PUMP1 VDDA low-voltage detection in IDLE Mode							
			pump1_det_i [1]	pump1_det_i [0]	LVD level of VDDA					
			0	0	GVDD+0.3V					
			0	1	GVDD+0.4V					
			1	0	GVDD+0.5V					
	pump1_dlvd_sel_i [2:0]	0~7	PUMP1 VDDA Dlow-voltage detection in IDLEMode							
			pump1_dlvd_sel_i [2]	pump1_dlvd_sel_i [1]	pump1_dlvd_sel_i [0]	DLVD level of VDDA				
			0	0	0	GVDD+1.4V				
			0	0	1	GVDD+1.3V				
			0	1	0	GVDD+1.2V				
			0	1	1	GVDD+1.1V				
			1	0	0	GVDD+1.0V				
			1	0	1	GVDD+0.9V				
			1	1	0	GVDD+0.8V				
			1	1	1	GVDD+0.7V				

162 th Parameter	Value	Description			
pump4_vghs_i [3:0]	0~15	PUMP4 VGH voltage select in Idle Mode			
		pump4_vghs_i[3:0]	VGH Voltage	pump4_vghs_i[3:0]	VGH Voltage
		4'b0000	11.5 V	4'b1000	15.5 V
		4'b0001	12.0 V	4'b1001	16.0 V
		4'b0010	12.5 V	4'b1010	16.5 V
		4'b0011	13.0 V	4'b1011	17.0 V
		4'b0100	13.5 V	4'b1100	17.5 V
		4'b0101	14.0 V	4'b1101	18.0 V
		4'b0110	14.5 V	4'b1110	18.5 V
		4'b0111	15.0 V	4'b1111	19.0 V
pump5_vgls_i [3:0]	0~15	PUMP5 VGL voltage select in Idle Mode			
		pump5_vgls_i[3:0]	VGL Voltage	pump5_vgls_i[3:0]	VGL Voltage
		4'b0000	-7.0 V	4'b1000	-11.5 V
		4'b0001	-7.5 V	4'b1001	-12.0 V
		4'b0010	-8.0 V	4'b1010	-12.5 V
		4'b0011	-8.5 V	4'b1011	-13.0 V
		4'b0100	-9.0 V	4'b1100	-14.0 V
		4'b0101	-9.5 V	4'b1101	-14.5 V
		4'b0110	-10.0 V	4'b1110	-15.0 V
		4'b0111	-11.0 V	4'b1111	-15.5 V
163 th Parameter	Value	Description			
pump4_x6_i	0	VGH = 8 X VDD, Only Valid when PUMP4_EN_ASMD_HV = "0" & "Idle Mode On"			
	1	VGH = 6 X VDD, Only Valid when PUMP4_EN_ASMD_HV = "0" & "Idle Mode On"			
pump5_x4_i	0	VGL = -6 X VDD, Only Valid when PUMP4_EN_ASMD_HV = "0" & "Idle Mode On"			
	1	VGL = -4 X VDD, Only Valid when PUMP4_EN_ASMD_HV = "0" & "Idle Mode On"			
pump45_x6_i	0	Set VGH by pump4_x6_n & set VGL by pump5_x4_n, Only Valid when PUMP4_EN_ASMD_HV = "0" & "Idle Mode On"			
	1	Set VGH = 6 X VDD & VGL = -6 X VDD , Only Valid when PUMP4_EN_ASMD_HV = "0" & "Idle Mode On"			
164 th Parameter	Value	Description			
hvreg_vrgh_s_i [3:0]	0~7	HV-regulator VRGH voltage select in Idle Mode			
		HVREG_VRGH_S[3:0]	VRGH Voltage	HVREG_VRGH_S[3:0]	VRGH Voltage
		4'b0000	8.5 V	4'b1000	12.5 V
		4'b0001	9 V	4'b1001	13 V
		4'b0010	9.5 V	4'b1010	13.5 V
		4'b0011	10 V	4'b1011	14 V
		4'b0100	10.5 V	4'b1100	14.5 V
		4'b0101	11 V	4'b1101	15 V
		4'b0110	11.5 V	4'b1110	15.5 V
		4'b0111	12 V	4'b1111	16 V
hvreg_vglreg_s_i [3:0]	0~7	HV-regulator VGL-REG voltage select in Idle Mode			

HVREG_VGLREG_S[3:0]	VGL_REG Voltage	HVREG_VGLREG_S[3:0]	VGL_REG Voltage
4'b0000	-7.0 V	4'b1000	-11.5 V
4'b0001	-7.5 V	4'b1001	-12.0 V
4'b0010	-8.0 V	4'b1010	-12.5 V
4'b0011	-8.5 V	4'b1011	-13.0 V
4'b0100	-9.0 V	4'b1100	-14.0 V
4'b0101	-9.5 V	4'b1101	-14.5 V
4'b0110	-10.0 V	4'b1110	-15.0 V
4'b0111	-11.0 V	4'b1111	-15.5 V

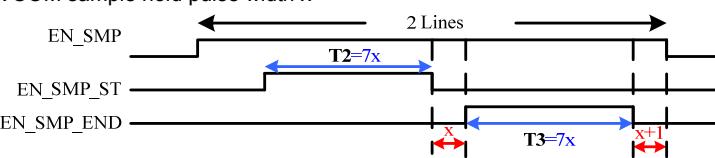
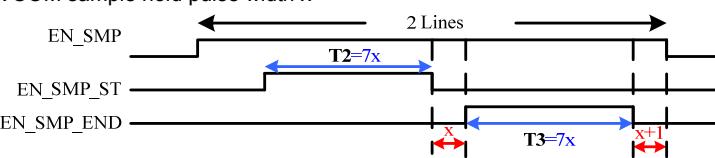
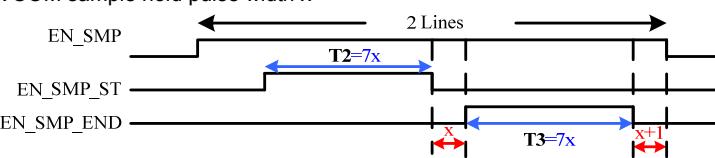
165 th Parameter	Value	Description	
pump1_clk_ratio_i [2:0]	0~7	PUMP1 set pump clock ratio	
		pump1_clk_ratio_i [2:0]	VDDA Pump Clock Frequency
		3'b000	8 Lines
		3'b001	4 Lines
		3'b010	2 Lines
		3'b011	1 Line
		3'b100	1 / 2 Line
		3'b101	1 / 4 Line
		3'b110	1 / 8 Line
		3'b111	1 / 16 Line
pump2_clk_ratio_i [2:0]	0~7	PUMP2 set pump clock ratio	
		pump2_clk_ratio_i [2:0]	NVDDA Pump Clock Frequency
		3'b000	8 Lines
		3'b001	4 Lines
		3'b010	2 Lines
		3'b011	1 Line
		3'b100	1 / 2 Line
		3'b101	1 / 4 Line
		3'b110	1 / 8 Line
		3'b111	1 / 16 Line

166 th Parameter	Value	Description	
pump3_clk_ratio_i [2:0]	0~7	PUMP3 set pump clock ratio	
		pump3_clk_ratio_i [2:0]	VCL Pump Clock Frequency
		3'b000	8 Lines
		3'b001	4 Lines
		3'b010	2 Lines
		3'b011	1 Line
		3'b100	1 / 2 Line
		3'b101	1 / 4 Line
		3'b110	1 / 8 Line
		3'b111	1 / 16 Line
pump4_clk_ratio_i [2:0]	0~7	PUMP4 set pump clock ratio	

			pump4_clk_ratio_i [2:0]	VGH/VGL Pump Clock Frequency																																									
			3'b000	8 Lines																																									
			3'b001	4 Lines																																									
			3'b010	2 Lines																																									
			3'b011	1 Line																																									
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			3'b110	1 / 8 Line																																									
			3'b111	1 / 16 Line																																									
<table border="1"> <thead> <tr> <th>167th Parameter</th> <th>Value</th> <th>Bias Current Selection</th> </tr> </thead> <tbody> <tr> <td rowspan="8">analog_ibias_gp_i [2:0]</td><td>000</td><td>2.0 uA</td></tr> <tr> <td>001</td><td>2.5 uA</td></tr> <tr> <td>010</td><td>3.0 uA</td></tr> <tr> <td>011</td><td>3.5 uA</td></tr> <tr> <td>100</td><td>4.0 uA</td></tr> <tr> <td>101</td><td>4.5 uA</td></tr> <tr> <td>110</td><td>5.0 uA</td></tr> <tr> <td>111</td><td>5.5 uA</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>167th Parameter</th> <th>Value</th> <th>Trim Bias Current</th> </tr> </thead> <tbody> <tr> <td rowspan="8">analog_ibias_ap_i [2:0]</td><td>000</td><td>60%</td></tr> <tr> <td>001</td><td>60%</td></tr> <tr> <td>010</td><td>70%</td></tr> <tr> <td>011</td><td>85%</td></tr> <tr> <td>100</td><td>100%</td></tr> <tr> <td>101</td><td>120%</td></tr> <tr> <td>110</td><td>140%</td></tr> <tr> <td>111</td><td>160%</td></tr> </tbody> </table>						167 th Parameter	Value	Bias Current Selection	analog_ibias_gp_i [2:0]	000	2.0 uA	001	2.5 uA	010	3.0 uA	011	3.5 uA	100	4.0 uA	101	4.5 uA	110	5.0 uA	111	5.5 uA	167 th Parameter	Value	Trim Bias Current	analog_ibias_ap_i [2:0]	000	60%	001	60%	010	70%	011	85%	100	100%	101	120%	110	140%	111	160%
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5.3.34. PWR_CTRL4(C5B0h): Power Control Setting 4 for DC Voltage Settings

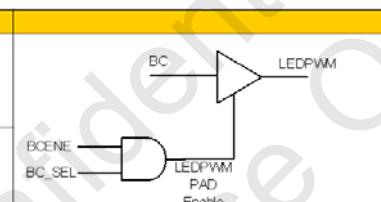
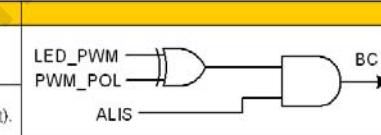
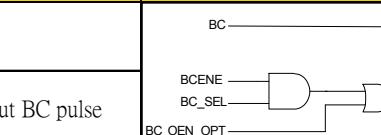
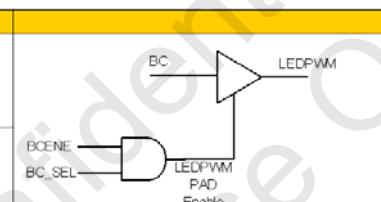
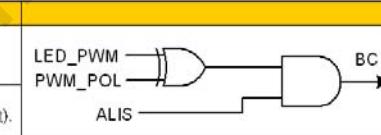
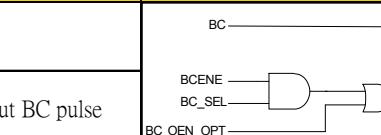
Address	C5h										
Address (SPI/I2C/MDDI)	C5B1h ~ C5B2h (0xB1 st ~ 0xB2 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	1	0	1	C5h
177 th Parameter	Write/Read		pwr_te_ sel	pwr_led_ sel	smpwid [4:0]					04h	
178 th Parameter	Write/Read		vdd18v_sel [1:0]	lvds vdd_ sel [1:0]	diopwr_ sel	1	gvdd_v com_gn d	gvdd_e n_test	Ach		

Description	<ul style="list-style-type: none"> - pwr_te_sel : select TE output voltage level - pwr_led_sel : select LEDON/LEDPWM output voltage level <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th rowspan="2">DSTB_SEL</th><th rowspan="2">VDDIO</th><th rowspan="2">VSEL</th><th rowspan="2">DIOPWR</th><th colspan="3">Output voltage level</th></tr> <tr> <th>TE</th><th colspan="2">LEDON, LEDPWM</th></tr> </thead> <tbody> <tr> <td rowspan="2">0</td><td rowspan="2">1.65~3.3v or 1.1~1.3v</td><td rowspan="2"></td><td rowspan="2"></td><td>VOH=VDDIO VOL=VSS</td><td>VOH=VDDIO VOL=VSS</td><td>VOH=VDD VOL=VSS</td></tr> <tr> <td>VOH=VDDIO VOL=VSS</td><td>VOH=VDDIO VOL=VSS</td><td>VOH=VDD VOL=VSS</td></tr> <tr> <td rowspan="2">1</td><td rowspan="2">1.65~3.3v</td><td rowspan="2"></td><td rowspan="2"></td><td>VOH=DIOPWR VOL=VSS</td><td>VOH=DIOPWR VOL=VSS</td><td>VOH=VDD VOL=VSS</td></tr> <tr> <td>VOH=VDDIO VOL=VSS</td><td>VOH=VDD VOL=VSS</td><td>VOH=VDD VOL=VSS</td></tr> <tr> <td rowspan="3">1</td><td rowspan="2">1.1~1.3v</td><td rowspan="2"></td><td rowspan="2"></td><td>VOH=DIOPWR VOL=VSS</td><td>VOH=DIOPWR VOL=VSS</td><td>VOH=DIOPWR VOL=VSS</td></tr> <tr> <td>VOH=DIOPWR VOL=VSS</td><td>VOH=DIOPWR VOL=VSS</td><td>VOH=DIOPWR VOL=VSS</td></tr> </tbody> </table>	DSTB_SEL	VDDIO	VSEL	DIOPWR	Output voltage level			TE	LEDON, LEDPWM		0	1.65~3.3v or 1.1~1.3v			VOH=VDDIO VOL=VSS	VOH=VDDIO VOL=VSS	VOH=VDD VOL=VSS	VOH=VDDIO VOL=VSS	VOH=VDDIO VOL=VSS	VOH=VDD VOL=VSS	1	1.65~3.3v			VOH=DIOPWR VOL=VSS	VOH=DIOPWR VOL=VSS	VOH=VDD VOL=VSS	VOH=VDDIO VOL=VSS	VOH=VDD VOL=VSS	VOH=VDD VOL=VSS	1	1.1~1.3v			VOH=DIOPWR VOL=VSS	VOH=DIOPWR VOL=VSS	VOH=DIOPWR VOL=VSS	VOH=DIOPWR VOL=VSS	VOH=DIOPWR VOL=VSS	VOH=DIOPWR VOL=VSS
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		TE	LEDON, LEDPWM																																						
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	10	1.60V																																							
	11	1.55V																																							

	178 th Parameter			Value	Description	
diopwr_sel				0	1.2 V	
				1	1.8 V	
gvdd_vcom_gnd				0	VCOMDC voltage be set by vcom_vmdc[7:0]	
				1	VCOMDC voltage set to GND	
gvdd_en_test				0	Disable VCOM test mode	
				1	Enable VCOM test mode	
Restriction	- Read and Write, Only access when Orise mode enable.					
Register Availability	Status	Availability				
	Normal Mode On, Idle Mode Off, Sleep Out	Yes				
	Normal Mode On, Idle Mode On, Sleep Out	Yes				
	Partial Mode On, Idle Mode Off, Sleep Out	Yes				
	Partial Mode On, Idle Mode On, Sleep Out	Yes				
	Sleep In	Yes				
Default	Status	Default Value				
	OTP un-programmed	Set as default value				
	OTP Programmed	Set as OTP value				

5.3.35. ABC_PARA1 (C680H) ABC Parameter 1

Address	C6h										
Address (SPI/I2C/MDDI)	C680h (0x81 st parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	1	1	0	C6h
129 th Parameter	Write/Read		0	BCENE	CABC_EN	ALIS	0	BC_SE_L	0	0	F4h

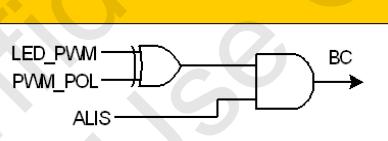
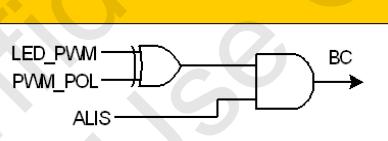
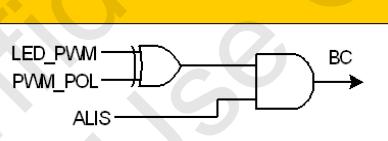
<p>- This command is used to set the internal function block of LABC.</p> <p>- BCENE : This bit combine with BC_SEL register to control LEDPWM PIN output.</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <tr> <th colspan="2">BCENE[D6] Control LEDPWM</th> </tr> <tr> <td>0</td> <td>Disable, LEDPWM=0.</td> </tr> <tr> <td>1</td> <td>Enable, if BC_SEL=1, LEDPWM output BC pulse</td> </tr> </table>  <p>- CABC_EN : This bit is used to control CABC related Command enable (include: \$51,\$53, \$55, \$5E)</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <tr> <th colspan="2">CABC_EN5[D5] CABC related Command</th> </tr> <tr> <td>0</td> <td>Disable</td> </tr> <tr> <td>1</td> <td>Enable(Default)</td> </tr> </table> <p>- ALIS : LEDPWM Function Enable</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <tr> <th colspan="2">ALIS[D4] KBBC / LEDPWM Function</th> </tr> <tr> <td>0</td> <td>Disable, KBBC / LEDPWM Function disable</td> </tr> <tr> <td>1</td> <td>Enable, KBBC / LEDPWM Function enable (Default).</td> </tr> </table>  <p>- BC_SEL : This bit combine with BCENE and BC_OEN_OPT register to control LEDPWM PIN output.</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <tr> <th colspan="2">BC_SEL Control LEDPWM</th> </tr> <tr> <td>0</td> <td>Disable, LEDPWM=0</td> </tr> <tr> <td>1</td> <td>Enable, if BC_SEL=1, LEDPWM output BC pulse</td> </tr> </table> 	BCENE[D6] Control LEDPWM		0	Disable, LEDPWM=0.	1	Enable, if BC_SEL=1, LEDPWM output BC pulse	CABC_EN5[D5] CABC related Command		0	Disable	1	Enable(Default)	ALIS[D4] KBBC / LEDPWM Function		0	Disable, KBBC / LEDPWM Function disable	1	Enable, KBBC / LEDPWM Function enable (Default).	BC_SEL Control LEDPWM		0	Disable, LEDPWM=0	1	Enable, if BC_SEL=1, LEDPWM output BC pulse	<p>- Read and Write, Only access when Orise mode enable.</p> <p>- Using parameter shift function to access 81hth parameter.</p>
BCENE[D6] Control LEDPWM																									
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<table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <tr> <th colspan="2">Status</th> <th colspan="2">Availability</th> </tr> <tr> <td colspan="2">Normal Mode On, Idle Mode Off, Sleep Out</td> <td colspan="2">Yes</td> </tr> <tr> <td colspan="2">Normal Mode On, Idle Mode On, Sleep Out</td> <td colspan="2">Yes</td> </tr> <tr> <td colspan="2">Partial Mode On, Idle Mode Off, Sleep Out</td> <td colspan="2">Yes</td> </tr> <tr> <td colspan="2">Partial Mode On, Idle Mode On, Sleep Out</td> <td colspan="2">Yes</td> </tr> <tr> <td colspan="2">Sleep In</td> <td colspan="2">Yes</td> </tr> </table>	Status		Availability		Normal Mode On, Idle Mode Off, Sleep Out		Yes		Normal Mode On, Idle Mode On, Sleep Out		Yes		Partial Mode On, Idle Mode Off, Sleep Out		Yes		Partial Mode On, Idle Mode On, Sleep Out		Yes		Sleep In		Yes		
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Status		Availability																							
Normal Mode On, Idle Mode Off, Sleep Out		Yes																							
Normal Mode On, Idle Mode On, Sleep Out		Yes																							
Partial Mode On, Idle Mode Off, Sleep Out		Yes																							
Partial Mode On, Idle Mode On, Sleep Out		Yes																							
Sleep In		Yes																							

Default	Status	Default Value
	Power On Sequence	F4h
	S/W Reset	F4h
	H/W Reset	F4h

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5.3.36. ABC_PARA2 (C6B0H) ABC Parameter 2

Address	C6h										
Address (SPI/I2C/MDDI)	C6B0h (0xB1 st parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	1	1	0	C6h
177 th Parameter	Write/Read		PWM_ POL	0	0	0	BC_MO D[1]	BC_MO D[0]	1	1	03h

Description	<p>- BC_MOD[1:0] :</p> <p>00 : BC pulse will not be clear by Vsync signal.</p> <p>01 : BC pulse will be clear by Vsync pulse signal.</p>													
	<p>- PWM_POL : Polarity of LEDPWM output.</p> <table border="1"> <tr> <td>PWM_POL[D7]</td> <td>Polarity of LEDPWM output.</td> <td></td> </tr> <tr> <td>0</td> <td>Non-Inversion, LEDPWM=0.</td> <td></td> </tr> <tr> <td>1</td> <td>Inversion.</td> <td></td> </tr> </table>		PWM_POL[D7]	Polarity of LEDPWM output.		0	Non-Inversion, LEDPWM=0.		1	Inversion.				
PWM_POL[D7]	Polarity of LEDPWM output.													
0	Non-Inversion, LEDPWM=0.													
1	Inversion.													
Restriction	- Read and Write, Only access when Orise mode enable.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>03 h</td> </tr> <tr> <td>S/W Reset</td> <td>03 h</td> </tr> <tr> <td>H/W Reset</td> <td>03 h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	03 h	S/W Reset	03 h	H/W Reset	03 h				
Status	Default Value													
Power On Sequence	03 h													
S/W Reset	03 h													
H/W Reset	03 h													

5.3.37. ABC_PARA3 (C6B1H) ABC Parameter 3

Address	C6h										
Address (SPI/I2C/MDDI)	C6B1h~C7B2h (0xB2 th ~ 0xB3 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	1	1	0	C6h
178 th Parameter	Write/Read		DBF[7]	DBF[6]	DBF[5]	DBF[4]	DBF[3]	DBF[2]	DBF[1]	DBF[0]	10h
179 th Parameter	Write/Read		Reserved								00h

Description	- This command is used to adjust PWM Freq. The PWM Freq can be set by DBF and PWM_FREQ_SEL as following table. unit : (KHz)																																																																																																																																																																																																																																					
	<table border="1"> <thead> <tr> <th>DBF[7:0]</th><th colspan="4">PWM_FREQ_SEL[1:0]</th></tr> <tr> <th></th><th>00</th><th>01</th><th>10</th><th>11</th></tr> </thead> <tbody> <tr><td>0</td><td>68.359</td><td>136.718</td><td>34.179</td><td>17.089</td></tr> <tr><td>1</td><td>34.179</td><td>68.359</td><td>17.089</td><td>8.544</td></tr> <tr><td>2</td><td>22.786</td><td>45.572</td><td>11.393</td><td>5.696</td></tr> <tr><td>3</td><td>17.089</td><td>34.179</td><td>8.544</td><td>4.272</td></tr> <tr><td>4</td><td>13.671</td><td>27.343</td><td>6.835</td><td>3.417</td></tr> <tr><td>5</td><td>11.393</td><td>22.786</td><td>5.696</td><td>2.848</td></tr> <tr><td>6</td><td>9.765</td><td>19.531</td><td>4.882</td><td>2.441</td></tr> <tr><td>7</td><td>8.544</td><td>17.089</td><td>4.272</td><td>2.136</td></tr> <tr><td>8</td><td>7.595</td><td>15.19</td><td>3.797</td><td>1.898</td></tr> <tr><td>9</td><td>6.835</td><td>13.671</td><td>3.417</td><td>1.708</td></tr> <tr><td>10</td><td>6.214</td><td>12.428</td><td>3.107</td><td>1.553</td></tr> <tr><td>11</td><td>5.696</td><td>11.393</td><td>2.848</td><td>1.424</td></tr> <tr><td>12</td><td>5.258</td><td>10.516</td><td>2.629</td><td>1.314</td></tr> <tr><td>13</td><td>4.882</td><td>9.765</td><td>2.441</td><td>1.22</td></tr> <tr><td>14</td><td>4.557</td><td>9.114</td><td>2.278</td><td>1.139</td></tr> <tr><td>15</td><td>4.272</td><td>8.544</td><td>2.136</td><td>1.068</td></tr> <tr><td>16</td><td>4.021</td><td>8.042</td><td>2.01</td><td>1.005</td></tr> <tr><td>17</td><td>3.797</td><td>7.595</td><td>1.898</td><td>0.949</td></tr> <tr><td>18</td><td>3.597</td><td>7.195</td><td>1.798</td><td>0.899</td></tr> <tr><td>19</td><td>3.417</td><td>6.835</td><td>1.708</td><td>0.854</td></tr> <tr><td>20</td><td>3.255</td><td>6.51</td><td>1.627</td><td>0.813</td></tr> <tr><td>21</td><td>3.107</td><td>6.214</td><td>1.553</td><td>0.776</td></tr> <tr><td>22</td><td>2.972</td><td>5.944</td><td>1.486</td><td>0.743</td></tr> <tr><td>23</td><td>2.848</td><td>5.696</td><td>1.424</td><td>0.712</td></tr> <tr><td>24</td><td>2.734</td><td>5.468</td><td>1.367</td><td>0.683</td></tr> <tr><td>25</td><td>2.629</td><td>5.258</td><td>1.314</td><td>0.657</td></tr> <tr><td>26</td><td>2.531</td><td>5.063</td><td>1.265</td><td>0.632</td></tr> <tr><td>27</td><td>2.441</td><td>4.882</td><td>1.22</td><td>0.61</td></tr> <tr><td>28</td><td>2.357</td><td>4.714</td><td>1.178</td><td>0.589</td></tr> <tr><td>29</td><td>2.278</td><td>4.557</td><td>1.139</td><td>0.569</td></tr> <tr><td>30</td><td>2.205</td><td>4.41</td><td>1.102</td><td>0.551</td></tr> <tr><td>31</td><td>2.136</td><td>4.272</td><td>1.068</td><td>0.534</td></tr> <tr><td>32</td><td>2.071</td><td>4.142</td><td>1.035</td><td>0.517</td></tr> <tr><td>33</td><td>2.01</td><td>4.021</td><td>1.005</td><td>0.502</td></tr> <tr><td>34</td><td>1.953</td><td>3.906</td><td>0.976</td><td>0.488</td></tr> <tr><td>35</td><td>1.898</td><td>3.797</td><td>0.949</td><td>0.474</td></tr> <tr><td>36</td><td>1.847</td><td>3.695</td><td>0.923</td><td>0.461</td></tr> <tr><td>37</td><td>1.798</td><td>3.597</td><td>0.899</td><td>0.449</td></tr> <tr><td>38</td><td>1.752</td><td>3.505</td><td>0.876</td><td>0.438</td></tr> <tr><td>39</td><td>1.708</td><td>3.417</td><td>0.854</td><td>0.427</td></tr> <tr><td>40</td><td>1.667</td><td>3.334</td><td>0.833</td><td>0.416</td></tr> <tr><td>41</td><td>1.627</td><td>3.255</td><td>0.813</td><td>0.406</td></tr> <tr><td>42</td><td>1.589</td><td>3.179</td><td>0.794</td><td>0.397</td></tr> <tr><td>43</td><td>1.553</td><td>3.107</td><td>0.776</td><td>0.388</td></tr> </tbody> </table>	DBF[7:0]	PWM_FREQ_SEL[1:0]					00	01	10	11	0	68.359	136.718	34.179	17.089	1	34.179	68.359	17.089	8.544	2	22.786	45.572	11.393	5.696	3	17.089	34.179	8.544	4.272	4	13.671	27.343	6.835	3.417	5	11.393	22.786	5.696	2.848	6	9.765	19.531	4.882	2.441	7	8.544	17.089	4.272	2.136	8	7.595	15.19	3.797	1.898	9	6.835	13.671	3.417	1.708	10	6.214	12.428	3.107	1.553	11	5.696	11.393	2.848	1.424	12	5.258	10.516	2.629	1.314	13	4.882	9.765	2.441	1.22	14	4.557	9.114	2.278	1.139	15	4.272	8.544	2.136	1.068	16	4.021	8.042	2.01	1.005	17	3.797	7.595	1.898	0.949	18	3.597	7.195	1.798	0.899	19	3.417	6.835	1.708	0.854	20	3.255	6.51	1.627	0.813	21	3.107	6.214	1.553	0.776	22	2.972	5.944	1.486	0.743	23	2.848	5.696	1.424	0.712	24	2.734	5.468	1.367	0.683	25	2.629	5.258	1.314	0.657	26	2.531	5.063	1.265	0.632	27	2.441	4.882	1.22	0.61	28	2.357	4.714	1.178	0.589	29	2.278	4.557	1.139	0.569	30	2.205	4.41	1.102	0.551	31	2.136	4.272	1.068	0.534	32	2.071	4.142	1.035	0.517	33	2.01	4.021	1.005	0.502	34	1.953	3.906	0.976	0.488	35	1.898	3.797	0.949	0.474	36	1.847	3.695	0.923	0.461	37	1.798	3.597	0.899	0.449	38	1.752	3.505	0.876	0.438	39	1.708	3.417	0.854	0.427	40	1.667	3.334	0.833	0.416	41	1.627	3.255	0.813	0.406	42	1.589	3.179	0.794	0.397	43	1.553	3.107	0.776
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<table border="1"> <thead> <tr> <th>DBF[7:0]</th><th colspan="4">PWM_FREQ_SEL[1:0]</th></tr> <tr> <th></th><th>00</th><th>01</th><th>10</th><th>11</th></tr> </thead> <tbody> <tr><td>44</td><td>1.519</td><td>3.038</td><td>0.759</td><td>0.379</td></tr> <tr><td>45</td><td>1.486</td><td>2.972</td><td>0.743</td><td>0.371</td></tr> <tr><td>46</td><td>1.454</td><td>2.908</td><td>0.727</td><td>0.363</td></tr> <tr><td>47</td><td>1.424</td><td>2.848</td><td>0.712</td><td>0.356</td></tr> <tr><td>48</td><td>1.395</td><td>2.79</td><td>0.697</td><td>0.348</td></tr> <tr><td>49</td><td>1.367</td><td>2.734</td><td>0.683</td><td>0.341</td></tr> <tr><td>50</td><td>1.34</td><td>2.68</td><td>0.67</td><td>0.335</td></tr> <tr><td>51</td><td>1.314</td><td>2.629</td><td>0.657</td><td>0.328</td></tr> <tr><td>52</td><td>1.289</td><td>2.579</td><td>0.644</td><td>0.322</td></tr> <tr><td>53</td><td>1.265</td><td>2.531</td><td>0.632</td><td>0.316</td></tr> <tr><td>54</td><td>1.242</td><td>2.485</td><td>0.621</td><td>0.31</td></tr> <tr><td>55</td><td>1.22</td><td>2.441</td><td>0.61</td><td>0.305</td></tr> <tr><td>56</td><td>1.199</td><td>2.398</td><td>0.599</td><td>0.299</td></tr> <tr><td>57</td><td>1.178</td><td>2.357</td><td>0.589</td><td>0.294</td></tr> <tr><td>58</td><td>1.158</td><td>2.317</td><td>0.579</td><td>0.289</td></tr> <tr><td>59</td><td>1.139</td><td>2.278</td><td>0.569</td><td>0.284</td></tr> <tr><td>60</td><td>1.12</td><td>2.241</td><td>0.56</td><td>0.28</td></tr> <tr><td>61</td><td>1.102</td><td>2.205</td><td>0.551</td><td>0.275</td></tr> <tr><td>62</td><td>1.085</td><td>2.17</td><td>0.542</td><td>0.271</td></tr> <tr><td>63</td><td>1.068</td><td>2.136</td><td>0.534</td><td>0.267</td></tr> <tr><td>64</td><td>1.051</td><td>2.103</td><td>0.525</td><td>0.262</td></tr> <tr><td>65</td><td>1.035</td><td>2.071</td><td>0.517</td><td>0.258</td></tr> <tr><td>66</td><td>1.02</td><td>2.04</td><td>0.51</td><td>0.255</td></tr> <tr><td>67</td><td>1.005</td><td>2.01</td><td>0.502</td><td>0.251</td></tr> <tr><td>68</td><td>0.99</td><td>1.981</td><td>0.495</td><td>0.247</td></tr> <tr><td>69</td><td>0.976</td><td>1.953</td><td>0.488</td><td>0.244</td></tr> <tr><td>70</td><td>0.962</td><td>1.925</td><td>0.481</td><td>0.24</td></tr> <tr><td>71</td><td>0.949</td><td>1.898</td><td>0.474</td><td>0.237</td></tr> <tr><td>72</td><td>0.936</td><td>1.872</td><td>0.468</td><td>0.234</td></tr> <tr><td>73</td><td>0.923</td><td>1.847</td><td>0.461</td><td>0.23</td></tr> <tr><td>74</td><td>0.911</td><td>1.822</td><td>0.455</td><td>0.227</td></tr> <tr><td>75</td><td>0.899</td><td>1.798</td><td>0.449</td><td>0.224</td></tr> <tr><td>76</td><td>0.887</td><td>1.775</td><td>0.443</td><td>0.221</td></tr> <tr><td>77</td><td>0.876</td><td>1.752</td><td>0.438</td><td>0.219</td></tr> <tr><td>78</td><td>0.865</td><td>1.73</td><td>0.432</td><td>0.216</td></tr> <tr><td>79</td><td>0.854</td><td>1.708</td><td>0.427</td><td>0.213</td></tr> <tr><td>80</td><td>0.843</td><td>1.687</td><td>0.421</td><td>0.21</td></tr> <tr><td>81</td><td>0.833</td><td>1.667</td><td>0.416</td><td>0.208</td></tr> <tr><td>82</td><td>0.823</td><td>1.647</td><td>0.411</td><td>0.205</td></tr> <tr><td>83</td><td>0.813</td><td>1.627</td><td>0.406</td><td>0.203</td></tr> <tr><td>84</td><td>0.804</td><td>1.608</td><td>0.402</td><td>0.201</td></tr> <tr><td>85</td><td>0.794</td><td>1.589</td><td>0.397</td><td>0.198</td></tr> <tr><td>86</td><td>0.785</td><td>1.571</td><td>0.392</td><td>0.196</td></tr> <tr><td>87</td><td>0.776</td><td>1.553</td><td>0.388</td><td>0.194</td></tr> </tbody> </table>	DBF[7:0]	PWM_FREQ_SEL[1:0]					00	01	10	11	44	1.519	3.038	0.759	0.379	45	1.486	2.972	0.743	0.371	46	1.454	2.908	0.727	0.363	47	1.424	2.848	0.712	0.356	48	1.395	2.79	0.697	0.348	49	1.367	2.734	0.683	0.341	50	1.34	2.68	0.67	0.335	51	1.314	2.629	0.657	0.328	52	1.289	2.579	0.644	0.322	53	1.265	2.531	0.632	0.316	54	1.242	2.485	0.621	0.31	55	1.22	2.441	0.61	0.305	56	1.199	2.398	0.599	0.299	57	1.178	2.357	0.589	0.294	58	1.158	2.317	0.579	0.289	59	1.139	2.278	0.569	0.284	60	1.12	2.241	0.56	0.28	61	1.102	2.205	0.551	0.275	62	1.085	2.17	0.542	0.271	63	1.068	2.136	0.534	0.267	64	1.051	2.103	0.525	0.262	65	1.035	2.071	0.517	0.258	66	1.02	2.04	0.51	0.255	67	1.005	2.01	0.502	0.251	68	0.99	1.981	0.495	0.247	69	0.976	1.953	0.488	0.244	70	0.962	1.925	0.481	0.24	71	0.949	1.898	0.474	0.237	72	0.936	1.872	0.468	0.234	73	0.923	1.847	0.461	0.23	74	0.911	1.822	0.455	0.227	75	0.899	1.798	0.449	0.224	76	0.887	1.775	0.443	0.221	77	0.876	1.752	0.438	0.219	78	0.865	1.73	0.432	0.216	79	0.854	1.708	0.427	0.213	80	0.843	1.687	0.421	0.21	81	0.833	1.667	0.416	0.208	82	0.823	1.647	0.411	0.205	83	0.813	1.627	0.406	0.203	84	0.804	1.608	0.402	0.201	85	0.794	1.589	0.397	0.198	86	0.785	1.571	0.392	0.196	87	0.776	1.553	0.388	0.194
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88	0.768	1.536	0.384	0.192																																																																																																																																																																																																																																		
89	0.759	1.519	0.379	0.189																																																																																																																																																																																																																																		
90	0.751	1.502	0.375	0.187																																																																																																																																																																																																																																		
91	0.743	1.486	0.371	0.185																																																																																																																																																																																																																																		
92	0.735	1.47	0.367	0.183																																																																																																																																																																																																																																		
93	0.727	1.454	0.363	0.181																																																																																																																																																																																																																																		
94	0.719	1.439	0.359	0.179																																																																																																																																																																																																																																		
95	0.712	1.424	0.356	0.178																																																																																																																																																																																																																																		
96	0.704	1.409	0.352	0.176																																																																																																																																																																																																																																		
97	0.697	1.395	0.348	0.174																																																																																																																																																																																																																																		
98	0.69	1.38	0.345	0.172																																																																																																																																																																																																																																		
99	0.683	1.367	0.341	0.17																																																																																																																																																																																																																																		
100	0.676	1.353	0.338	0.169																																																																																																																																																																																																																																		
101	0.67	1.34	0.335	0.167																																																																																																																																																																																																																																		
102	0.663	1.327	0.331	0.165																																																																																																																																																																																																																																		
103	0.657	1.314	0.328	0.164																																																																																																																																																																																																																																		
104	0.651	1.302	0.325	0.162																																																																																																																																																																																																																																		
105	0.644	1.289	0.322	0.161																																																																																																																																																																																																																																		
106	0.638	1.277	0.319	0.159																																																																																																																																																																																																																																		
107	0.632	1.265	0.316	0.158																																																																																																																																																																																																																																		
108	0.627	1.254	0.313	0.156																																																																																																																																																																																																																																		
109	0.621	1.242	0.31	0.155																																																																																																																																																																																																																																		
110	0.615	1.231	0.307	0.153																																																																																																																																																																																																																																		
111	0.61	1.22	0.305	0.152																																																																																																																																																																																																																																		
112	0.604	1.209	0.302	0.151																																																																																																																																																																																																																																		
113	0.599	1.199	0.299	0.149																																																																																																																																																																																																																																		
114	0.594	1.188	0.297	0.148																																																																																																																																																																																																																																		
115	0.589	1.178	0.294	0.147																																																																																																																																																																																																																																		
116	0.584	1.168	0.292	0.146																																																																																																																																																																																																																																		
117	0.579	1.158	0.289	0.144																																																																																																																																																																																																																																		
118	0.574	1.148	0.287	0.143																																																																																																																																																																																																																																		
119	0.569	1.139	0.284	0.142																																																																																																																																																																																																																																		
120	0.564	1.129	0.282	0.141																																																																																																																																																																																																																																		
121	0.56	1.12	0.28	0.14																																																																																																																																																																																																																																		
122	0.555	1.111	0.277	0.138																																																																																																																																																																																																																																		
123	0.551	1.102	0.275	0.137																																																																																																																																																																																																																																		
124	0.546	1.093	0.273	0.136																																																																																																																																																																																																																																		
125	0.542	1.085	0.271	0.135																																																																																																																																																																																																																																		
126	0.538	1.076	0.269	0.134																																																																																																																																																																																																																																		
127	0.534	1.068	0.267	0.133																																																																																																																																																																																																																																		
128	0.529	1.059	0.264	0.132																																																																																																																																																																																																																																		
129	0.525	1.051	0.262	0.131																																																																																																																																																																																																																																		
130	0.521	1.043	0.26	0.13																																																																																																																																																																																																																																		
131	0.517	1.035	0.258	0.129																																																																																																																																																																																																																																		

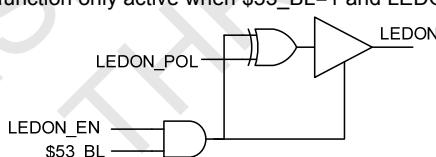
		unit : (KHz)			
		PWM_FREQ_SEL[1:0]			
DBF[7:0]		00	01	10	11
132	0.513	1.027	0.256	0.128	
133	0.51	1.02	0.255	0.127	
134	0.506	1.012	0.253	0.126	
135	0.502	1.005	0.251	0.125	
136	0.498	0.997	0.249	0.124	
137	0.495	0.99	0.247	0.123	
138	0.491	0.983	0.245	0.122	
139	0.488	0.976	0.244	0.122	
140	0.484	0.969	0.242	0.121	
141	0.481	0.962	0.24	0.12	
142	0.478	0.956	0.239	0.119	
143	0.474	0.949	0.237	0.118	
144	0.471	0.942	0.235	0.117	
145	0.468	0.936	0.234	0.117	
146	0.465	0.93	0.232	0.116	
147	0.461	0.923	0.23	0.115	
148	0.458	0.917	0.229	0.114	
149	0.455	0.911	0.227	0.113	
150	0.452	0.905	0.226	0.113	
151	0.449	0.899	0.224	0.112	
152	0.446	0.893	0.223	0.111	
153	0.443	0.887	0.221	0.11	
154	0.441	0.882	0.22	0.11	
155	0.438	0.876	0.219	0.109	
156	0.435	0.87	0.217	0.108	
157	0.432	0.865	0.216	0.108	
158	0.429	0.859	0.214	0.107	
159	0.427	0.854	0.213	0.106	
160	0.424	0.849	0.212	0.106	
161	0.421	0.843	0.21	0.105	
162	0.419	0.838	0.209	0.104	
163	0.416	0.833	0.208	0.104	
164	0.414	0.828	0.207	0.103	
165	0.411	0.823	0.205	0.102	
166	0.409	0.818	0.204	0.102	
167	0.406	0.813	0.203	0.101	
168	0.404	0.808	0.202	0.101	
169	0.402	0.804	0.201	0.1	
170	0.399	0.799	0.199	0.099	
171	0.397	0.794	0.198	0.099	
172	0.395	0.79	0.197	0.098	
173	0.392	0.785	0.196	0.098	
174	0.39	0.781	0.195	0.097	
175	0.388	0.776	0.194	0.097	

		Status		Availability	
Register Availability		Normal Mode On, Idle Mode Off, Sleep Out		Yes	
		Normal Mode On, Idle Mode On, Sleep Out		Yes	
		Partial Mode On, Idle Mode Off, Sleep Out		Yes	
		Partial Mode On, Idle Mode On, Sleep Out		Yes	
		Sleep In		Yes	

		Status	Default Value
Default		Power On Sequence	10 h
		S/W Reset	10 h
		H/W Reset	10 h

5.3.38. ABC_PARA4 (C6B3H) ABC Parameter 4

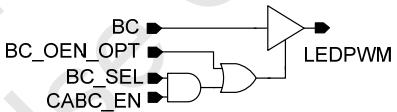
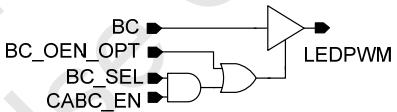
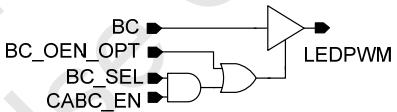
Address	C6h										
Address (SPI/I2C/MDDI)	C6B3h (0xB4 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	1	1	0	C6h
180 th Parameter	Write/Read		DFBC	LEDON _EN	LEDON _POL	LABC_ DIM_ FRM[4]	LABC_ DIM_ FRM[3]	LABC_ DIM_ FRM[2]	LABC_ DIM_ FRM[1]	LABC_ DIM_ FRM[0]	5Fh

Description	- This command is used to set LEDPWM setting.											
	- DFBC :Default BC status before Power-ON.											
	<table border="1"> <thead> <tr> <th>DFBC[D7]</th><th>Default BC status before Power-ON.</th></tr> </thead> <tbody> <tr> <td>0</td><td>LEDPWM='low'</td></tr> <tr> <td>1</td><td>LEDPWM='High'</td></tr> </tbody> </table>	DFBC[D7]	Default BC status before Power-ON.	0	LEDPWM='low'	1	LEDPWM='High'					
DFBC[D7]	Default BC status before Power-ON.											
0	LEDPWM='low'											
1	LEDPWM='High'											
Note. It also XOR with "LABC Parameter 9" PWM_POL.												
- LEDON_EN : Enable LEDON PAD for external LED Driver												
<table border="1"> <thead> <tr> <th>LEDON_EN[D6]</th><th>LEDON PAD for external LED Driver</th></tr> </thead> <tbody> <tr> <td>0</td><td>Disable</td></tr> <tr> <td>1</td><td>Enable(Default)</td></tr> </tbody> </table>	LEDON_EN[D6]	LEDON PAD for external LED Driver	0	Disable	1	Enable(Default)						
LEDON_EN[D6]	LEDON PAD for external LED Driver											
0	Disable											
1	Enable(Default)											
Note. This function only active when \$53_BL=1.												
- LEDON_POL: Polarity of LEDON Control Signal												
<table border="1"> <thead> <tr> <th>LEDON_POL[D5]</th><th>Polarity of LEDON Control Signal</th></tr> </thead> <tbody> <tr> <td>0</td><td>Noraml(Default).</td></tr> <tr> <td>1</td><td>Inversion.</td></tr> </tbody> </table>	LEDON_POL[D5]	Polarity of LEDON Control Signal	0	Noraml(Default).	1	Inversion.						
LEDON_POL[D5]	Polarity of LEDON Control Signal											
0	Noraml(Default).											
1	Inversion.											
Note. This function only active when \$53_BL=1 and LEDON_EN='1'.												
												
- LABC_DIM_FRM[4:0] : LABC Dimming frame, Default is 32 Frame.												
<table border="1"> <thead> <tr> <th>LABC_DIM_FRM[4:0]</th><th>Frame</th></tr> </thead> <tbody> <tr> <td>00h</td><td>1</td></tr> <tr> <td>01h</td><td>2</td></tr> <tr> <td>...</td><td>...</td></tr> <tr> <td>1Eh</td><td>31</td></tr> <tr> <td>1Fh</td><td>32</td></tr> </tbody> </table>	LABC_DIM_FRM[4:0]	Frame	00h	1	01h	2	1Eh	31	1Fh	32
LABC_DIM_FRM[4:0]	Frame											
00h	1											
01h	2											
...	...											
1Eh	31											
1Fh	32											
Restriction	- Read and Write, Only access when Orise mode enable.											

		Status	Availability
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
	Sleep In		Yes
Default	Status		Default Value
	Power On Sequence		5F h
	S/W Reset		5F h
	H/W Reset		5F h

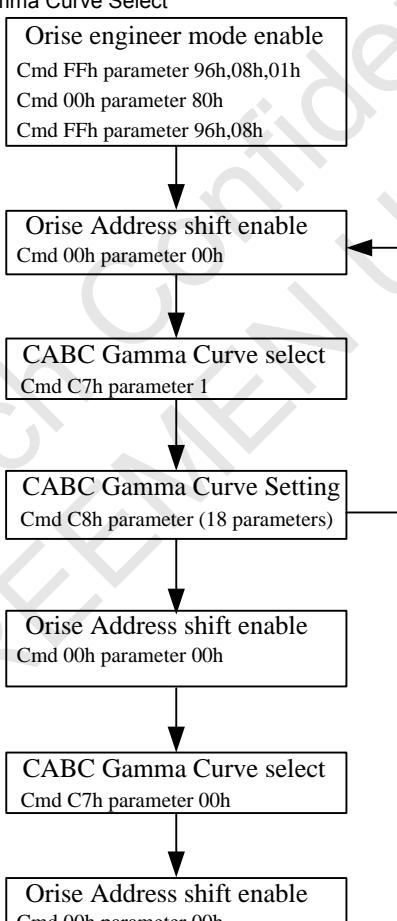
5.3.39. ABC_PARA5 (C6B4H) ABC Parameter 5

Address	C6h										
Address (SPI/I2C/MDDI)	C6B4h (0xB5 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	1	1	0	C6h
181 th Parameter	Write/Read		0	0	0	BC_OE_N_OPT	0	PWM_FREQ_SEL[1]	PWM_FREQ_SEL[0]	CABC_DUTY_FORCE	12h

Description	<ul style="list-style-type: none"> - This command is used to set PWM Frequency setting. - BC_OEN_OPT : If BC_OEN_OPT=1, the LCDPWM pad always output. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #f2e0aa;">BC_SEL</th><th colspan="3" style="background-color: #f2e0aa;">Control LEDPWM</th><th colspan="8"></th></tr> </thead> <tbody> <tr> <td>0</td><td colspan="3">Disable LEDPWM=0</td><td colspan="8" rowspan="4">  </td></tr> <tr> <td>1</td><td colspan="11">Enable if BC_SEL=1. LEDPWM output to BC pulse</td></tr> </tbody> </table>											BC_SEL	Control LEDPWM											0	Disable LEDPWM=0											1	Enable if BC_SEL=1. LEDPWM output to BC pulse										
BC_SEL	Control LEDPWM																																														
0	Disable LEDPWM=0																																														
1	Enable if BC_SEL=1. LEDPWM output to BC pulse																																														
Restriction	<ul style="list-style-type: none"> - Read and Write, Only access when Orise mode enable. 																																														
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d3d3d3;">Status</th> <th style="background-color: #d3d3d3;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																								
Status	Availability																																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																														
Normal Mode On, Idle Mode On, Sleep Out	Yes																																														
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																														
Partial Mode On, Idle Mode On, Sleep Out	Yes																																														
Sleep In	Yes																																														
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #d3d3d3;">Status</th> <th style="background-color: #d3d3d3;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>12 h</td> </tr> <tr> <td>S/W Reset</td> <td>12 h</td> </tr> <tr> <td>H/W Reset</td> <td>12 h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	12 h	S/W Reset	12 h	H/W Reset	12 h																												
Status	Default Value																																														
Power On Sequence	12 h																																														
S/W Reset	12 h																																														
H/W Reset	12 h																																														

5.3.40. CABCSET1 (C700h): CABC setting

Address	C7h										
Address (SPI/I2C/MDDI)	C700h (0x01 st parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	0	1	1	1	C7h
Parameter 1	Write		0	0	0	CABC_SEL_E NA	CABC_SEL[3:0]				0Fh

Description	<ul style="list-style-type: none"> - CABC_SEL_ENA: CABC Manual Setting Enable - CABC_SEL[3:0]: CABC Manual Gamma Curve Select 						
Restriction	- Write, Only access when Orise mode enable.						
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">OTP un-programmed</td> <td style="text-align: center;">Set as default value</td> </tr> <tr> <td style="text-align: center;">OTP Programmed</td> <td style="text-align: center;">Set as OTP value</td> </tr> </tbody> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value
Status	Default Value						
OTP un-programmed	Set as default value						
OTP Programmed	Set as OTP value						

5.3.41. CABCSET2 (C800h): CABC gamma curve setting

Address	C8h										
Address (SPI/I2C/MDDI)	C800h~C811 (0x01 st ~0x12 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	0	0	0	C8h
Parameter 1	Write/Read		CABC2[3:0]				CABC1[3:0]				80h
Parameter 2	Write/Read		CABC4[3:0]				CABC3[3:0]				88h
Parameter 3	Write/Read		CABC6[3:0]				CABC5[3:0]				88h
Parameter 4	Write/Read		CABC8[3:0]				CABC7[3:0]				88h
Parameter 5	Write/Read		CABC10[3:0]				CABC9[3:0]				88h
Parameter 6	Write/Read		CABC12[3:0]				CABC11[3:0]				88h
Parameter 7	Write/Read		CABC14[3:0]				CABC13[3:0]				88h
Parameter 8	Write/Read		CABC16[3:0]				CABC15[3:0]				88h
Parameter 9	Write/Read		CABC18[3:0]				CABC17[3:0]				88h
Parameter 10	Write/Read		CABC20[3:0]				CABC19[3:0]				88h
Parameter 11	Write/Read		CABC22[3:0]				CABC21[3:0]				88h
Parameter 12	Write/Read		CABC24[3:0]				CABC23[3:0]				88h
Parameter 13	Write/Read		CABC26[3:0]				CABC25[3:0]				88h
Parameter 14	Write/Read		CABC28[3:0]				CABC27[3:0]				88h
Parameter 15	Write/Read		CABC30[3:0]				CABC29[3:0]				88h
Parameter 16	Write/Read		CABC32[3:0]				CABC31[3:0]				88h
Parameter 17	Write/Read		CABC34[3:0]				CABC33[3:0]				88h
Parameter 18	Write/Read		CABC36[3:0]				CABC35[3:0]				88h

Description	- CABCx[3:0] (x=1~36): Command C8h totally has 18 parameters, these parameters are settings for CABC gamma curve							
Restriction	<ul style="list-style-type: none"> - Read and Write, Only access when Orise mode enable. - CABC Gamma value is readable only after the register has been written or the OTP has been programmed 							
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #cccccc;">Status</th> <th style="background-color: #cccccc;">Default Value</th> </tr> </thead> <tbody> <tr> <td>OTP un-programmed</td> <td>Set as default value</td> </tr> <tr> <td>OTP Programmed</td> <td>Set as OTP value</td> </tr> </tbody> </table>		Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value
Status	Default Value							
OTP un-programmed	Set as default value							
OTP Programmed	Set as OTP value							

5.3.42. AIESET(C900h): AIE Setting

Address (MIPI)		C9h									
Address (Other I/F)		C900h									
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	0	0	1	C9h
1 st Parameter	Write/Read		AIE2[3:0]			AIE1[3:0]			80h		
2 nd Parameter	Write/Read		AIE4[3:0]			AIE3[3:0]			88h		
:	Write/Read		:			:			88h		
17 th Parameter	Write/Read		AIE34[3:0]			AIE33[3:0]			88h		
18 th Parameter	Write/Read		AIE36[3:0]			AIE35[3:0]			88h		

Description	<ul style="list-style-type: none"> - Command C9h totally has 18 parameters, these parameters are settings for AIE gamma curve - 													
Restriction	<ul style="list-style-type: none"> - Read and Write, Only access when Orise mode enable. - AIE Gamma value is readable only after the register has been written or the OTP has been programmed 													
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default														

5.3.43. CABC_AIE_PWMDMYSET (CAA3) CABC_AIE PWM dummy Setting

Address		CA									
Address (SPI/I2C/MDDI)		CAA3h (0xA4 th parameter)									
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	0	1	0	
0xA4 th Parameter	Write/Read		-	-	-	aie_opt-	-	-	-	pwm_di_spoff_opt	10h

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	Bit	Description		Value	
	aie_opt-	AIE function compensate mode		0 : 1bit compensation 1 : 2bit compensation	
	pwm_dispooff_opt	PWM signal state during DISPLAY OFF state		0 : Keep toggle 1 : Keep Low	
Restriction	- Read and Write, Only accessible when Orise mode is enabled				
Register Availability	Status		Availability		
	Normal Mode On, Idle Mode Off, Sleep Out		Yes		
	Normal Mode On, Idle Mode On, Sleep Out		Yes		
	Partial Mode On, Idle Mode Off, Sleep Out		Yes		
	Partial Mode On, Idle Mode On, Sleep Out		Yes		
Default	Status		Default Value		
	OTP un-programmed		Set as default value		
	OTP Programmed		Set as OTP value		

5.3.44. GOAVST(CE80h~CE8Bh) GOA VST Setting

Address	CEh										
Address (SPI/I2C/MDDI)	CE80h ~ CE8Bh (0x81 st ~ 0x8C th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	0	
0x81 st Parameter	Write/Read				vst1_shift[7:0]						86h
0x82 nd Parameter	Write/Read		0	0	0	0		vst1_width[3:0]			03h
0x83 rd Parameter	Write/Read				vst1_tchop[7:0]						18h
0x84 th Parameter	Write/Read				vst2_shift[7:0]						85h
0x85 th Parameter	Write/Read		0	0	0	0		vst2_width[3:0]			03h
0x86 th Parameter	Write/Read				vst2_tchop[7:0]						18h
0x87 th Parameter	Write/Read				vst3_shift[7:0]						00h
0x88 th Parameter	Write/Read		0	0	0	0		vst3_width[3:0]			0Fh
0x89 th Parameter	Write/Read				vst3_tchop[7:0]						00h
0x8A th Parameter	Write/Read				vst4_shift[7:0]						00h
0x8B th Parameter	Write/Read		0	0	0	0		vst4_width[3:0]			0Fh
0x8C th Parameter	Write/Read				vst4_tchop[7:0]						00h

NOTE: “-” Don't care, can be set to VDDIO or VSS level

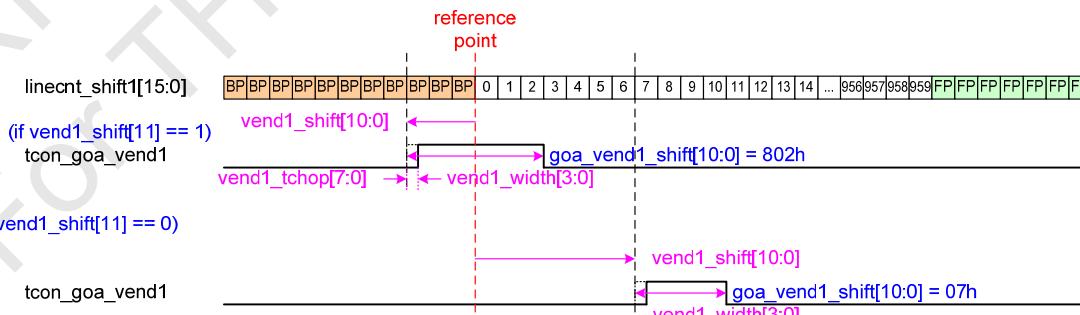
Description	These parameters are used to create single pulse type signals tcon_goa_vst1, tcon_goa_vst2, tcon_goa_vst3 and tcon_goa_vst4.																			
	Parameters	Description																		
	vst1_shift[7]	0: tcon_goa_vst1 rising edge locates after reference point 1: tcon_goa_vst1 rising edge locates before reference point, in BP region																		
	vst1_shift[6:0]	Set starting position of the tcon_goa_vst1 pulse with respect to the reference point																		
	vst1_width[3:0]	Set tcon_goa_vst1 pulse width = vst1_width[3:0] + 1 (unit = line)																		
	vst1_tchop[7:0]	Delay rising edge of tcon_goa_vst1 signal (unit = mclk)																		
	linecnt_shift1[15:0]	reference point																		
	(if vst1_shift[7] == 1) tcon_goa_vst1																			
	(If vst1_shift[7] == 0) tcon_goa_vst1																			
	- Use other parameters and apply the same method to create tcon_goa_vst2, tcon_goa_vst3 and tcon_goa_vst4 signals																			
Restriction	- Read and Write, Only accessible when Orise mode is enabled.																			

		Status	Availability
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
	Sleep In		Yes
		Status	Default Value
Default	OTP un-programmed		Set as default value
	OTP Programmed		Set as OTP value

5.3.45. GOAVEND(CE90h~CE9Bh) GOA VEND Setting

Address	CEh										
Address (SPI/I2C/MDDI)	CE90h ~ CE9Bh (0x91 st ~ 0x9C th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	0	
0x91 st Parameter	Write/Read		vend1_width[3:0]				vend1_shift[11:8]				33h
0x92 nd Parameter	Write/Read		vend1_tchop[7:0]								BFh
0x93 rd Parameter	Write/Read		vend1_tchop[7:0]								18h
0x94 th Parameter	Write/Read		vend2_width[3:0]				vend2_shift[11:8]				33h
0x95 th Parameter	Write/Read		vend2_tchop[7:0]								C0h
0x96 th Parameter	Write/Read		vend2_tchop[7:0]								18h
0x97 th Parameter	Write/Read		vend3_width[3:0]				vend3_shift[11:8]				F0h
0x98 th Parameter	Write/Read		vend3_tchop[7:0]								00h
0x99 th Parameter	Write/Read		vend3_tchop[7:0]								00h
0x9A th Parameter	Write/Read		vend4_width[3:0]				vend4_shift[11:8]				F0h
0x9B th Parameter	Write/Read		vend4_tchop[7:0]								00h
0x9C th Parameter	Write/Read		vend4_tchop[7:0]								00h

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

	These parameters are used to create single pulse type signals tcon_goa_vst1, tcon_goa_vst2, tcon_goa_vst3 and tcon_goa_vst4.									
	<table border="1"> <thead> <tr> <th>Parameters</th><th>Description</th></tr> </thead> <tbody> <tr> <td>vend1_shift[11]</td><td>0: tcon_goa_vend1 rising edge locates after reference point 1: tcon_goa_vend1 rising edge locates before reference point, in BP region</td></tr> <tr> <td>vend1_shift[10:0]</td><td>Set starting position of the tcon_goa_vend1 pulse with respect to the reference point</td></tr> <tr> <td>vend1_width[3:0]</td><td>Set tcon_goa_vend1 pulse width = vend1_width[3:0] + 1 (unit = line)</td></tr> <tr> <td>vend1_tchop[7:0]</td><td>Delay rising edge of tcon_goa_vend1 signal (unit = mclk)</td></tr> </tbody> </table>	Parameters	Description	vend1_shift[11]	0: tcon_goa_vend1 rising edge locates after reference point 1: tcon_goa_vend1 rising edge locates before reference point, in BP region	vend1_shift[10:0]	Set starting position of the tcon_goa_vend1 pulse with respect to the reference point	vend1_width[3:0]	Set tcon_goa_vend1 pulse width = vend1_width[3:0] + 1 (unit = line)	vend1_tchop[7:0]
Parameters	Description									
vend1_shift[11]	0: tcon_goa_vend1 rising edge locates after reference point 1: tcon_goa_vend1 rising edge locates before reference point, in BP region									
vend1_shift[10:0]	Set starting position of the tcon_goa_vend1 pulse with respect to the reference point									
vend1_width[3:0]	Set tcon_goa_vend1 pulse width = vend1_width[3:0] + 1 (unit = line)									
vend1_tchop[7:0]	Delay rising edge of tcon_goa_vend1 signal (unit = mclk)									
Description	<p>reference point</p>  <p>- Use other parameters and apply the same method to create tcon_goa_vend2, tcon_goa_vend3 and tcon_goa_vend4 signals</p>									
Restriction	- Read and Write, Only accessible when Orise mode is enabled.									

		Status	Availability
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
	Sleep In		Yes
		Status	Default Value
Default	OTP un-programmed		Set as default value
	OTP Programmed		Set as OTP value

5.3.46. GOAGPSET(CE9Ch~CE9Dh) GOA Group Setting

Address	CEh										
Address (SPI/I2C/MDDI)	CE9Ch ~ CE9Dh (0x9D st ~ 0x9E th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	0	
0x9D st Parameter	Write/Read		clka1_group1	clka2_group1	clka3_group1	clka4_group1	clkb1_group1	clkb2_group1	clkb3_group1	clkb4_group1	00h
0x9E nd Parameter	Write/Read		clkc1_group1	clkc2_group1	clkc3_group1	clkc4_group1	clkd1_group1	clkd2_group1	clkd3_group1	clkd4_group1	00h

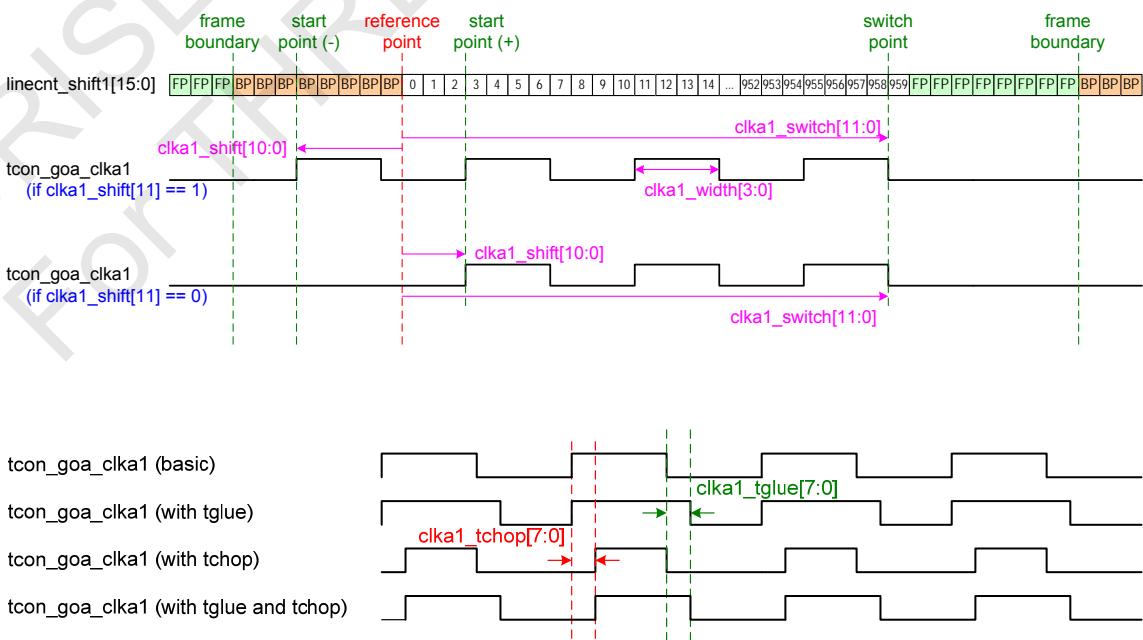
NOTE: “-” Don’t care, can be set to VDDIO or VSS level

Description	These parameters are used to control the tcon_goa_clkx timing in the head and tail region as to where the rising or falling edge should align to.													
	Parameters	Description												
	clka1_group1	0: the edge of tcon_goa_clka1 head and tail region aligns with edges of tcon_goa_vst2 1: the edge of tcon_goa_clka1 head and rail region aligns with edges of tcon_goa_vst1												
	clka2_group1	0: the edge of tcon_goa_clka2 head and tail region aligns with edges of tcon_goa_vst2 1: the edge of tcon_goa_clka2 head and rail region aligns with edges of tcon_goa_vst1												
	clka3_group1	0: the edge of tcon_goa_clka3 head and tail region aligns with edges of tcon_goa_vst2 1: the edge of tcon_goa_clka3 head and rail region aligns with edges of tcon_goa_vst1												
	clka4_group1	0: the edge of tcon_goa_clka4 head and tail region aligns with edges of tcon_goa_vst2 1: the edge of tcon_goa_clka4 head and rail region aligns with edges of tcon_goa_vst1												
Restriction	Use the remaining parameters and apply the same method control signal behavior of tcon_goa_clkb1~b4, tcon_goa_clkc1~c4, tcon_goa_clkd1~d4.													
	Please refer to figures in 5.3.47 for definition of head and tail region of the clock signals and other parameters that controls the signal behavior in the head and tail region.													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>OTP un-programmed</td><td>Set as default value</td></tr> <tr> <td>OTP Programmed</td><td>Set as OTP value</td></tr> </tbody> </table>		Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value						
Status	Default Value													
OTP un-programmed	Set as default value													
OTP Programmed	Set as OTP value													

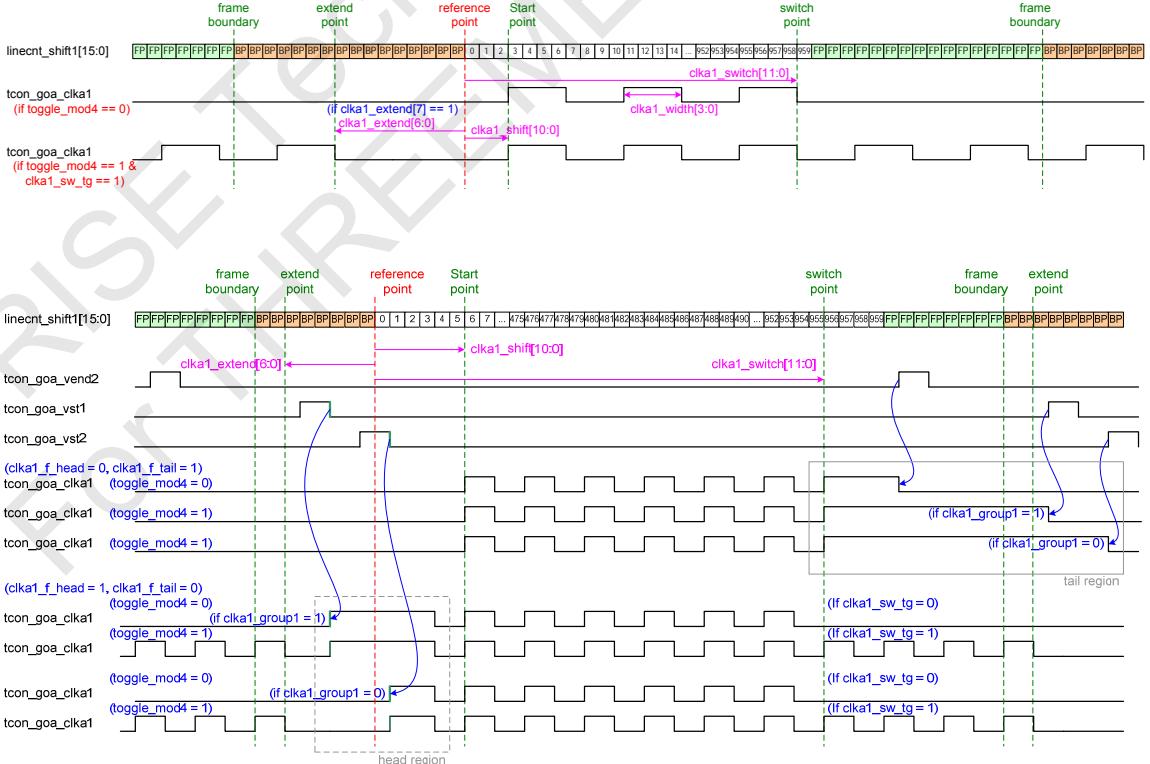
5.3.47. GOACLKA1(CEA0h~CEA6h) GOA CLKA1 Setting

Address	CEh											
Address (SPI/I2C/MDDI)	CEA0h ~ CEA6h (0xA1 st ~ 0xA7 th parameter)											
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default	
Instruction	Write	00h	1	1	0	0	1	1	1	0		
0xA1 st Parameter	Write/Read		clka1_width[3:0]				clka1_shift[11:8]				38h	
0xA2 nd Parameter	Write/Read		clka1_shift[7:0]								02h	
0xA3 rd Parameter	Write/Read		clka1_sw_tq	clka1_odd_hi	clka1_f_head	clka1_f_tail	clka1_switch[11:8]					83h
0xA4 th Parameter	Write/Read		clka1_switch[7:0]								C1h	
0xA5 th Parameter	Write/Read		clka1_extend[7:0]								86h	
0xA6 th Parameter	Write/Read		clka1_tchop[7:0]								18h	
0xA7 th Parameter	Write/Read		clka1_tglue[7:0]								00h	

NOTE: “-” Don't care, can be set to VDDIO or VSS level

	These parameters are used to create clock type signal tcon_goa_clka1																								
	<table border="1"> <thead> <tr> <th>Basic Setting Parameters</th><th>Description</th></tr> </thead> <tbody> <tr> <td>clka1_shift[11]</td><td>0: tcon_goa_clka1 rising edge starting point locates after reference point 1: tcon_goa_clka1 rising edge starting point locates before reference point, in BP region</td></tr> <tr> <td>clka1_shift[10:0]</td><td>Specifies start point of tcon_goa_clka1 where the clock starts to toggle</td></tr> <tr> <td>clka1_width[3:0]</td><td>Set half-period of the tcon_goa_clka1 signal, half period = clka1_width[3:0] + 1 (unit = line)</td></tr> <tr> <td>clka1_switch[11:0]</td><td>Set ending position of the tcon_goa_clka1 signal with respect to the reference point</td></tr> <tr> <td>clka1_tchop[7:0]</td><td>Delay rising edge of tcon_goa_clka1 signal (unit = mclk)</td></tr> <tr> <td>clka1_tglue[7:0]</td><td>Delay falling edge of tcon_goa_clka1 signal (unit = mclk)</td></tr> </tbody> </table>											Basic Setting Parameters	Description	clka1_shift[11]	0: tcon_goa_clka1 rising edge starting point locates after reference point 1: tcon_goa_clka1 rising edge starting point locates before reference point, in BP region	clka1_shift[10:0]	Specifies start point of tcon_goa_clka1 where the clock starts to toggle	clka1_width[3:0]	Set half-period of the tcon_goa_clka1 signal, half period = clka1_width[3:0] + 1 (unit = line)	clka1_switch[11:0]	Set ending position of the tcon_goa_clka1 signal with respect to the reference point	clka1_tchop[7:0]	Delay rising edge of tcon_goa_clka1 signal (unit = mclk)	clka1_tglue[7:0]	Delay falling edge of tcon_goa_clka1 signal (unit = mclk)
Basic Setting Parameters	Description																								
clka1_shift[11]	0: tcon_goa_clka1 rising edge starting point locates after reference point 1: tcon_goa_clka1 rising edge starting point locates before reference point, in BP region																								
clka1_shift[10:0]	Specifies start point of tcon_goa_clka1 where the clock starts to toggle																								
clka1_width[3:0]	Set half-period of the tcon_goa_clka1 signal, half period = clka1_width[3:0] + 1 (unit = line)																								
clka1_switch[11:0]	Set ending position of the tcon_goa_clka1 signal with respect to the reference point																								
clka1_tchop[7:0]	Delay rising edge of tcon_goa_clka1 signal (unit = mclk)																								
clka1_tglue[7:0]	Delay falling edge of tcon_goa_clka1 signal (unit = mclk)																								
Description	 <p>The diagram illustrates the generation of the tcon_goa_clka1 signal. It shows two main signals: tcon_goa_clka1 (if clka1_shift[11] == 1) and tcon_goa_clka1 (if clka1_shift[11] == 0). The timing is defined by the linecnt_shift1[15:0] register, which defines frame boundaries and line numbers (0 to 959). The clka1_shift[10:0] parameter specifies the start point relative to the reference point. The clka1_width[3:0] parameter defines the half-period of the signal. The clka1_switch[11:0] parameter defines the end point. The tcon_goa_clka1 signal is generated with specific delays (clka1_tchop[7:0] for rising edge, clka1_tglue[7:0] for falling edge) relative to the reference point.</p>																								

Special Setting Parameters	Description
clka1_sw_tg	Specifies tcon_goa_clka1 behavior in the non-operating area defined as the area after switch point and before start point. 0: tcon_goa_clka1 does not toggle in non-operating area 1: tcon_goa_clka1 continues to toggle in non-operating area, the toggling behaviour may also be controlled by other special setting parameters
clka1_f_head	0: tcon_goa_clka1 stays low in the head area 1: tcon_goa_clka1 goes high in the head area every other frame (decided by clka1_odd_hi)
clka1_f_tail	0: tcon_goa_clka1 stays low in the tail area 1: tcon_goa_clka1 goes high in the tail area every other frame (decided by clka1_odd_hi)
clka1_odd_hi	0: tcon_goa_clka1 goes high in head or tail area during even frames 1: tcon_goa_clka1 goes high in head or tail area during odd frames
clka1_extend[7]	0: tcon_goa_clka1 extend point locates after reference point 1: tcon_goa_clka1 extend point locates before reference point, in BP region
clka1_extend[6:0]	Specifies extend point where tcon_goa_clka1 continues to toggle past line boundary if clka1_sw_tg == 1 and toggle_mod4 == 1 (Note1)



 Note1: Please refer to 5.3.65 for related goa signal toggle option

Restriction - Read and Write, Only accessible when Orise mode is enabled

		Status	Availability
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
	Sleep In		Yes
		Status	Default Value
Default	OTP un-programmed		Set as default value
	OTP Programmed		Set as OTP value

5.3.48. GOACLKA2(CEA7h~CEADh) GOA CLKA2 Setting

Address	CEh										
Address (SPI/I2C/MDDI)	CEA7h ~ CEADh (0xA8 th ~ 0xAE th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	0	
0xA8 th Parameter	Write/Read		clka2_width[3:0]				clka2_shift[11:8]				38h
0xA9 th Parameter	Write/Read		clka2_shift[7:0]				clka2_switch[11:8]				01h
0xAA th Parameter	Write/Read		clka2_sw_tq	clka2_odd_hi	clka2_f_head	clka2_f_tail	clka2_switch[11:8]				83h
0xAB th Parameter	Write/Read		clka2_switch[7:0]				clka2_extend[7:0]				C2h
0xAC th Parameter	Write/Read		clka2_extend[7:0]				clka2_tchop[7:0]				85h
0xAD th Parameter	Write/Read		clka2_tchop[7:0]				clka2_tglue[7:0]				18h
0xAE th Parameter	Write/Read		clka2_tglue[7:0]				clka2_tglue[7:0]				00h

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	These parameters are used to create clock type signal tcon_goa_clka2. Please refer to 5.3.47 for description and function of each tcon_goa_clka2 parameters, and apply the same method to adjust tcon_goa_clka2 signal behavior.													
Restriction	- Read and Write, Only accessible when Orise mode is enabled													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>OTP un-programmed</td><td>Set as default value</td></tr> <tr> <td>OTP Programmed</td><td>Set as OTP value</td></tr> </tbody> </table>		Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value							
Status	Default Value													
OTP un-programmed	Set as default value													
OTP Programmed	Set as OTP value													

5.3.49. GOACLKA3(CEB0h~CEB6h) GOA CLKA3 Setting

Address	CEh										
Address (SPI/I2C/MDDI)	CEB0h ~ CEB6h (0xB1 st ~ 0xB7 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	0	
0xB1 st Parameter	Write/Read		clka3_width[3:0]				clka3_shift[11:8]				30h
0xB2 nd Parameter	Write/Read		clka3_shift[7:0]				clka3_switch[11:8]				01h
0xB3 rd Parameter	Write/Read		clka3_sw_tq	clka3_odd_hi	clka3_f_head	clka3_f_tail	clka3_switch[11:8]				83h
0xB4 th Parameter	Write/Read		clka3_switch[7:0]				clka3_extend[7:0]				C5h
0xB5 th Parameter	Write/Read		clka3_extend[7:0]				clka3_tchop[7:0]				86h
0xB6 th Parameter	Write/Read		clka3_tchop[7:0]				clka3_tglue[7:0]				18h
0xB7 th Parameter	Write/Read		clka3_tglue[7:0]				clka3_tglue[7:0]				00h

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	These parameters are used to create clock type signal tcon_goa_clka3. Please refer to 5.3.47 for description and function of each tcon_goa_clka3 parameters, and apply the same method to adjust tcon_goa_clka3 signal behavior.	
Restriction	- Read and Write, Only accessible when Orise mode is enabled	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	OTP un-programmed	Set as default value
	OTP Programmed	Set as OTP value

5.3.50. GOACLKA4(CEB7h~CEBDh) GOA CLKA4 Setting

Address	CEh										
Address (SPI/I2C/MDDI)	CEB7h ~ CEBDh (0xB8 th ~ 0xBE th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	0	
0xB8 th Parameter	Write/Read		clka4_width[3:0]				clka4_shift[11:8]				30h
0xB9 th Parameter	Write/Read		clka4_shift[7:0]				clka4_switch[11:8]				02h
0xBA th Parameter	Write/Read		clka4_sw_tq	clka4_odd_hi	clka4_f_head	clka4_f_tail	clka4_switch[11:8]				83h
0xBB th Parameter	Write/Read		clka4_switch[7:0]				clka4_extend[7:0]				C6h
0xBC th Parameter	Write/Read		clka4_extend[7:0]				clka4_tchop[7:0]				85h
0xBD th Parameter	Write/Read		clka4_tchop[7:0]				clka4_tglue[7:0]				18h
0xBE th Parameter	Write/Read		clka4_tglue[7:0]				clka4_tglue[7:0]				00h

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	These parameters are used to create clock type signal tcon_goa_clka4. Please refer to 5.3.47 for description and function of each tcon_goa_clka4 parameters, and apply the same method to adjust tcon_goa_clka4 signal behavior.	
Restriction	- Read and Write, Only accessible when Orise mode is enabled	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	OTP un-programmed	Set as default value
	OTP Programmed	Set as OTP value

5.3.51. GOACLKB1(CEC0h~CEC6h) GOA CLKB1 Setting

Address	CEh										
Address (SPI/I2C/MDDI)	CEC0h ~ CEC6h (0xC1 st ~ 0xC7 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	0	
0xC1 st Parameter	Write/Read		clkb1_width[3:0]				clkb1_shift[11:8]				38h
0xC2 nd Parameter	Write/Read		clkb1_shift[7:0]				clkb1_switch[11:8]				00h
0xC3 rd Parameter	Write/Read		clkb1_sw_tq	clkb1_odd_hi	clkb1_f_head	clkb1_f_tail	clkb1_switch[11:8]				83h
0xC4 th Parameter	Write/Read		clkb1_switch[7:0]				clkb1_extend[7:0]				C3h
0xC5 th Parameter	Write/Read		clkb1_extend[7:0]				clkb1_tchop[7:0]				86h
0xC6 th Parameter	Write/Read		clkb1_tchop[7:0]				clkb1_tglue[7:0]				18h
0xC7 th Parameter	Write/Read		clkb1_tglue[7:0]				clkb1_tglue[7:0]				00h

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	These parameters are used to create clock type signal tcon_goa_clkb1. Please refer to 5.3.47 for description and function of each tcon_goa_clkb1 parameters, and apply the same method to adjust tcon_goa_clkb1 signal behavior.	
Restriction	- Read and Write, Only accessible when Orise mode is enabled	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	OTP un-programmed	Set as default value
	OTP Programmed	Set as OTP value

5.3.52. GOACLKB2(CEC7h~CECDh) GOA CLKB2 Setting

Address	CEh										
Address (SPI/I2C/MDDI)	CEC7h ~ CECDh (0xC8 th ~ 0xCE th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	0	
0xC8 th Parameter	Write/Read		clk2_width[3:0]				clk2_shift[11:8]				30h
0xC9 th Parameter	Write/Read		clk2_shift[7:0]				clk2_switch[11:8]				00h
0xCA th Parameter	Write/Read		clk2_sw_tq	clk2_odd_hi	clk2_f_head	clk2_f_tail	clk2_switch[11:8]				83h
0xCB th Parameter	Write/Read		clk2_switch[7:0]				clk2_extend[7:0]				C4h
0xCC th Parameter	Write/Read		clk2_extend[7:0]				clk2_tchop[7:0]				85h
0xCD th Parameter	Write/Read		clk2_tchop[7:0]				clk2_tglue[7:0]				18h
0xCE th Parameter	Write/Read		clk2_tglue[7:0]				clk2_tglue[7:0]				10h

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	These parameters are used to create clock type signal tcon_goa_clk2. Please refer to 5.3.47 for description and function of each tcon_goa_clk2 parameters, and apply the same method to adjust tcon_goa_clk2 signal behavior.													
Restriction	- Read and Write, Only accessible when Orise mode is enabled													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>OTP un-programmed</td><td>Set as default value</td></tr> <tr> <td>OTP Programmed</td><td>Set as OTP value</td></tr> </tbody> </table>		Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value						
Status	Default Value													
OTP un-programmed	Set as default value													
OTP Programmed	Set as OTP value													

5.3.53. GOACLKB3(CED0h~CED6h) GOA CLKB3 Setting

Address	CEh										
Address (SPI/I2C/MDDI)	CED0h ~ CED6h (0xD1 st ~ 0xD7 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	0	
0xD1 st Parameter	Write/Read		clkb3_width[3:0]				clkb3_shift[11:8]				30h
0xD2 nd Parameter	Write/Read		clkb3_shift[7:0]				clkb3_switch[11:8]				03h
0xD3 rd Parameter	Write/Read		clkb3_sw_tq	clkb3_odd_hi	clkb3_f_head	clkb3_f_tail	clkb3_switch[11:8]				83h
0xD4 th Parameter	Write/Read		clkb3_switch[7:0]				clkb3_extend[7:0]				C7h
0xD5 th Parameter	Write/Read		clkb3_extend[7:0]				clkb3_tchop[7:0]				86h
0xD6 th Parameter	Write/Read		clkb3_tchop[7:0]				clkb3_tglue[7:0]				18h
0xD7 th Parameter	Write/Read		clkb3_tglue[7:0]				clkb3_tglue[7:0]				00h

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	These parameters are used to create clock type signal tcon_goa_clkb3. Please refer to 5.3.47 for description and function of each tcon_goa_clkb3 parameters, and apply the same method to adjust tcon_goa_clkb3 signal behavior.	
Restriction	- Read and Write, Only accessible when Orise mode is enabled	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	OTP un-programmed	Set as default value
	OTP Programmed	Set as OTP value

5.3.54. GOACLKB4(CED7h~CEDDh) GOA CLKB4 Setting

Address	CEh										
Address (SPI/I2C/MDDI)	CED7h ~ CEDDh (0xD8 th ~ 0xDE th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	0	
0xD8 th Parameter	Write/Read		clkb4_width[3:0]					clkb4_shift[11:8]			30h
0xD9 th Parameter	Write/Read		clkb4_shift[7:0]					clkb4_switch[11:8]			
0xDA th Parameter	Write/Read		clkb4_sw_tq	clkb4_odd_hi	clkb4_f_head	clkb4_f_tail	clkb4_switch[11:8]				
0xDB th Parameter	Write/Read		clkb4_switch[7:0]					clkb4_extend[7:0]			
0xDC th Parameter	Write/Read		clkb4_extend[7:0]					clkb4_tchop[7:0]			
0xDD th Parameter	Write/Read		clkb4_tchop[7:0]					clkb4_tglue[7:0]			
0xDE th Parameter	Write/Read		clkb4_tglue[7:0]					clkb4_tglue[7:0]			

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	These parameters are used to create clock type signal tcon_goa_clkb4. Please refer to 5.3.47 for description and function of each tcon_goa_clkb4 parameters, and apply the same method to adjust tcon_goa_clkb4 signal behavior.	
Restriction	- Read and Write, Only accessible when Orise mode is enabled	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	OTP un-programmed	Set as default value
	OTP Programmed	Set as OTP value

5.3.55. GOACLKC1(CF80h~CF86h) GOA CLKC1 Setting

Address	CFh															
Address (SPI/I2C/MDDI)	CF80h ~ CF86h (0x81 st ~ 0x87 th parameter)															
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default					
Instruction	Write	00h	1	1	0	0	1	1	1	1						
0x81 st Parameter	Write/Read		clkc1_width[3:0]				clkc1_shift[11:8]				F0h					
0x82 nd Parameter	Write/Read		clkc1_shift[7:0]													
0x83 rd Parameter	Write/Read		clkc1_sw_tq	clkc1_odd_hi	clkc1_f_head	clkc1_f_tail	clkc1_switch[11:8]									
0x84 th Parameter	Write/Read		clkc1_switch[7:0]													
0x85 th Parameter	Write/Read		clkc1_extend[7:0]													
0x86 th Parameter	Write/Read		clkc1_tchop[7:0]													
0x87 th Parameter	Write/Read		clkc1_tglue[7:0]													

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	These parameters are used to create clock type signal tcon_goa_clkc1. Please refer to 5.3.47 for description and function of each tcon_goa_clkc1 parameters, and apply the same method to adjust tcon_goa_clkc1 signal behavior.	
Restriction	- Read and Write, Only accessible when Orise mode is enabled	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	OTP un-programmed	Set as default value
	OTP Programmed	Set as OTP value

5.3.56. GOACLKC2(CF87h~CF8Dh) GOA CLKC2 Setting

Address	CFh										
Address (SPI/I2C/MDDI)	CF87h ~ CF8Dh (0x88 th ~ 0x8E th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	1	
0x88 th Parameter	Write/Read		clkc2_width[3:0]				clkc2_shift[11:8]				F0h
0x89 th Parameter	Write/Read		clkc2_shift[7:0]				clkc2_switch[11:8]				00h
0x8A th Parameter	Write/Read		clkc2_sw_tq	clkc2_odd_hi	clkc2_f_head	clkc2_f_tail	clkc2_switch[11:8]				00h
0x8B th Parameter	Write/Read		clkc2_switch[7:0]				clkc2_extend[7:0]				10h
0x8C th Parameter	Write/Read		clkc2_extend[7:0]				clkc2_tchop[7:0]				00h
0x8D th Parameter	Write/Read		clkc2_tchop[7:0]				clkc2_tglue[7:0]				00h
0x8E th Parameter	Write/Read		clkc2_tglue[7:0]				clkc2_tglue[7:0]				00h

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	These parameters are used to create clock type signal tcon_goa_clkc2. Please refer to 5.3.47 for description and function of each tcon_goa_clkc2 parameters, and apply the same method to adjust tcon_goa_clkc2 signal behavior.	
Restriction	- Read and Write, Only accessible when Orise mode is enabled	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	OTP un-programmed	Set as default value
	OTP Programmed	Set as OTP value

5.3.57. GOACLKC3(CF90h~CF96h) GOA CLKC3 Setting

Address	CFh															
Address (SPI/I2C/MDDI)	CF90h ~ CF96h (0x91 st ~ 0x97 th parameter)															
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default					
Instruction	Write	00h	1	1	0	0	1	1	1	1						
0x91 st Parameter	Write/Read		clkc3_width[3:0]				clkc3_shift[11:8]				F0h					
0x92 nd Parameter	Write/Read		clkc3_shift[7:0]													
0x93 rd Parameter	Write/Read		clkc3_sw_tq	clkc3_odd_hi	clkc3_f_head	clkc3_f_tail	clkc3_switch[11:8]									
0x94 th Parameter	Write/Read		clkc3_switch[7:0]													
0x95 th Parameter	Write/Read		clkc3_extend[7:0]													
0x96 th Parameter	Write/Read		clkc3_tchop[7:0]													
0x97 th Parameter	Write/Read		clkc3_tglue[7:0]													

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	These parameters are used to create clock type signal tcon_goa_clkc3. Please refer to 5.3.47 for description and function of each tcon_goa_clkc3 parameters, and apply the same method to adjust tcon_goa_clkc3 signal behavior.	
Restriction	- Read and Write, Only accessible when Orise mode is enabled	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	OTP un-programmed	Set as default value
	OTP Programmed	Set as OTP value

5.3.58. GOACLKC4(CF97h~CF9Dh) GOA CLKC4 Setting

Address	CFh										
Address (SPI/I2C/MDDI)	CF97h ~ CF9Dh (0x98 th ~ 0x9E th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	1	
0x98 th Parameter	Write/Read		clkc4_width[3:0]				clkc4_shift[11:8]				F0h
0x99 th Parameter	Write/Read		clkc4_shift[7:0]				clkc4_switch[11:8]				00h
0x9A th Parameter	Write/Read		clkc4_sw_tq	clkc4_odd_hi	clkc4_f_head	clkc4_f_tail	clkc4_switch[11:8]				00h
0x9B th Parameter	Write/Read		clkc4_switch[7:0]				clkc4_extend[7:0]				10h
0x9C th Parameter	Write/Read		clkc4_extend[7:0]				clkc4_tchop[7:0]				00h
0x9D th Parameter	Write/Read		clkc4_tchop[7:0]				clkc4_tglue[7:0]				00h
0x9E th Parameter	Write/Read		clkc4_tglue[7:0]				clkc4_tglue[7:0]				00h

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	These parameters are used to create clock type signal tcon_goa_clkc4. Please refer to 5.3.47 for description and function of each tcon_goa_clkc4 parameters, and apply the same method to adjust tcon_goa_clkc4 signal behavior.	
Restriction	- Read and Write, Only accessible when Orise mode is enabled	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	OTP un-programmed	Set as default value
	OTP Programmed	Set as OTP value

5.3.59. GOACLKD1(CFA0h~CFA6h) GOA CLKD1 Setting

Address	CFh										
Address (SPI/I2C/MDDI)	CFA0h ~ CFA6h (0xA1 st ~ 0xA7 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	1	
0xA1 st Parameter	Write/Read		clkd1_width[3:0]				clkd1_shift[11:8]				F0h
0xA2 nd Parameter	Write/Read		clkd1_shift[7:0]				clkd1_switch[11:8]				00h
0xA3 rd Parameter	Write/Read		clkd1_sw_tq	clkd1_odd_hi	clkd1_f_head	clkd1_f_tail	clkd1_switch[11:8]				00h
0xA4 th Parameter	Write/Read		clkd1_switch[7:0]				clkd1_extend[7:0]				10h
0xA5 th Parameter	Write/Read		clkd1_extend[7:0]				clkd1_tchop[7:0]				00h
0xA6 th Parameter	Write/Read		clkd1_tchop[7:0]				clkd1_tglue[7:0]				00h
0xA7 th Parameter	Write/Read		clkd1_tglue[7:0]				clkd1_tglue[7:0]				00h

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	These parameters are used to create clock type signal tcon_goa_clkd1. Please refer to 5.3.47 for description and function of each tcon_goa_clkd1 parameters, and apply the same method to adjust tcon_goa_clkd1 signal behavior.	
Restriction	- Read and Write, Only accessible when Orise mode is enabled	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	OTP un-programmed	Set as default value
	OTP Programmed	Set as OTP value

5.3.60. GOACLKD2(CFA7h~CFADh) GOA CLKD2 Setting

Address	CFh										
Address (SPI/I2C/MDDI)	CFA7h ~ CFADh (0xA8 th ~ 0xAE th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	1	
0xA8 th Parameter	Write/Read		clkd2_width[3:0]				clkd2_shift[11:8]				F0h
0xA9 th Parameter	Write/Read		clkd2_shift[7:0]				clkd2_switch[11:8]				00h
0xAA th Parameter	Write/Read		clkd2_sw_tq	clkd2_odd_hi	clkd2_f_head	clkd2_f_tail	clkd2_switch[11:8]				00h
0xAB th Parameter	Write/Read		clkd2_switch[7:0]				clkd2_extend[7:0]				10h
0xAC th Parameter	Write/Read		clkd2_extend[7:0]				clkd2_tchop[7:0]				00h
0xAD th Parameter	Write/Read		clkd2_tchop[7:0]				clkd2_tglue[7:0]				00h
0xAE th Parameter	Write/Read		clkd2_tglue[7:0]				clkd2_tglue[7:0]				00h

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	These parameters are used to create clock type signal tcon_goa_clkd2. Please refer to 5.3.47 for description and function of each tcon_goa_clkd2 parameters, and apply the same method to adjust tcon_goa_clkd2 signal behavior.													
Restriction	- Read and Write, Only accessible when Orise mode is enabled													
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #cccccc;">Status</th> <th style="background-color: #cccccc;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #cccccc;">Status</th> <th style="background-color: #cccccc;">Default Value</th> </tr> </thead> <tbody> <tr> <td>OTP un-programmed</td><td>Set as default value</td></tr> <tr> <td>OTP Programmed</td><td>Set as OTP value</td></tr> </tbody> </table>		Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value							
Status	Default Value													
OTP un-programmed	Set as default value													
OTP Programmed	Set as OTP value													

5.3.61. GOACLKD3(CFB0h~CFB6h) GOA CLKD3 Setting

Address	CFh										
Address (SPI/I2C/MDDI)	CFB0h ~ CFB6h (0xB1 st ~ 0xB7 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	1	
0xB1 st Parameter	Write/Read		clkd3_width[3:0]				clkd3_shift[11:8]				F0h
0xB2 nd Parameter	Write/Read		clkd3_shift[7:0]				clkd3_switch[11:8]				00h
0xB3 rd Parameter	Write/Read		clkd3_sw_tq	clkd3_odd_hi	clkd3_f_head	clkd3_f_tail	clkd3_switch[11:8]				00h
0xB4 th Parameter	Write/Read		clkd3_switch[7:0]				clkd3_extend[7:0]				10h
0xB5 th Parameter	Write/Read		clkd3_extend[7:0]				clkd3_tchop[7:0]				00h
0xB6 th Parameter	Write/Read		clkd3_tchop[7:0]				clkd3_tglue[7:0]				00h
0xB7 th Parameter	Write/Read		clkd3_tglue[7:0]				clkd3_tglue[7:0]				00h

NOTE: “-” Don't care, can be set to VDDIO or VSS level

Description	These parameters are used to create clock type signal tcon_goa_clkd3. Please refer to 5.3.47 for description and function of each tcon_goa_clkd3 parameters, and apply the same method to adjust tcon_goa_clkd3 signal behavior.	
Restriction	- Read and Write, Only accessible when Orise mode is enabled	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	OTP un-programmed	Set as default value
	OTP Programmed	Set as OTP value

5.3.62. GOACLKD4(CFB7h~CFBDh) GOA CLKD4 Setting

Address	CFh										
Address (SPI/I2C/MDDI)	CFB7h ~ CFBDh (0xB8 th ~ 0xBE th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	1	
0xB8 th Parameter	Write/Read		clkd4_width[3:0]				clkd4_shift[11:8]				F0h
0xB9 th Parameter	Write/Read		clkd4_shift[7:0]				clkd4_switch[11:8]				00h
0xBA th Parameter	Write/Read		clkd4_sw_tq	clkd4_odd_hi	clkd4_f_head	clkd4_f_tail	clkd4_switch[11:8]				00h
0xBB th Parameter	Write/Read		clkd4_switch[7:0]				clkd4_extend[7:0]				10h
0xBC th Parameter	Write/Read		clkd4_extend[7:0]				clkd4_tchop[7:0]				00h
0xBD th Parameter	Write/Read		clkd4_tchop[7:0]				clkd4_tglue[7:0]				00h
0xBE th Parameter	Write/Read		clkd4_tglue[7:0]				clkd4_tglue[7:0]				00h

NOTE: “-” Don't care, can be set to VDDIO or VSS level

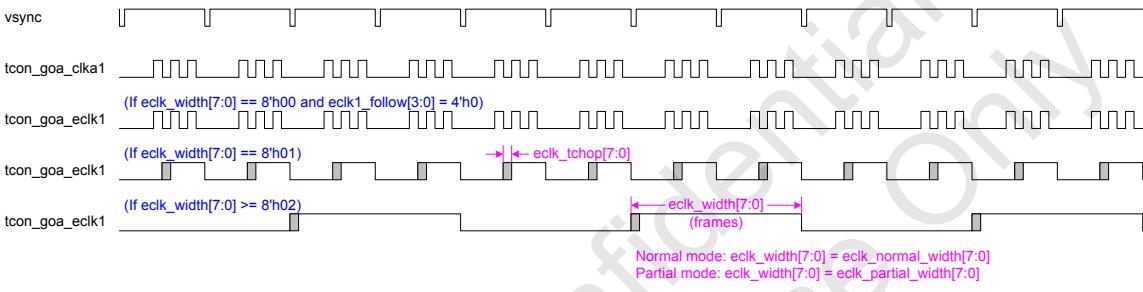
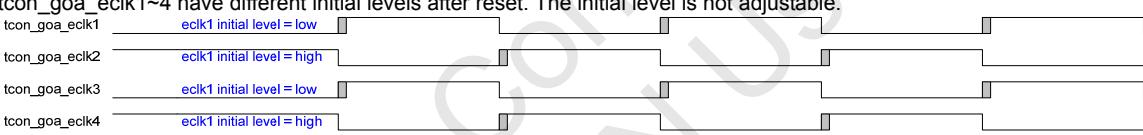
Description	These parameters are used to create clock type signal tcon_goa_clkd4. Please refer to 5.3.47 for description and function of each tcon_goa_clkd4 parameters, and apply the same method to adjust tcon_goa_clkd4 signal behavior.	
Restriction	- Read and Write, Only accessible when Orise mode is enabled	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	OTP un-programmed	Set as default value
	OTP Programmed	Set as OTP value

5.3.63. GOAECLK(CFC0h~CFC5h) GOA ECLK Setting

Address	CFh										
Address (SPI/I2C/MDDI)	CFC0h ~ CFC5h (0xC1 th ~ 0xC6 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	1	
0xC1 st Parameter	Write/Read		eclk_normal_width[7:0]						01h		
0xC2 nd Parameter	Write/Read		eclk_partial_width[7:0]						01h		
0xC3 rd Parameter	Write/Read		all_normal_tchop[7:0]						20h		
0xC4 th Parameter	Write/Read		all_partial_tchop[7:0]						20h		
0xC5 th Parameter	Write/Read		eclk1_follow[3:0]				eclk2_follow[3:0]				00h
0xC6 th Parameter	Write/Read		eclk3_follow[3:0]				eclk4_follow[3:0]				00h

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

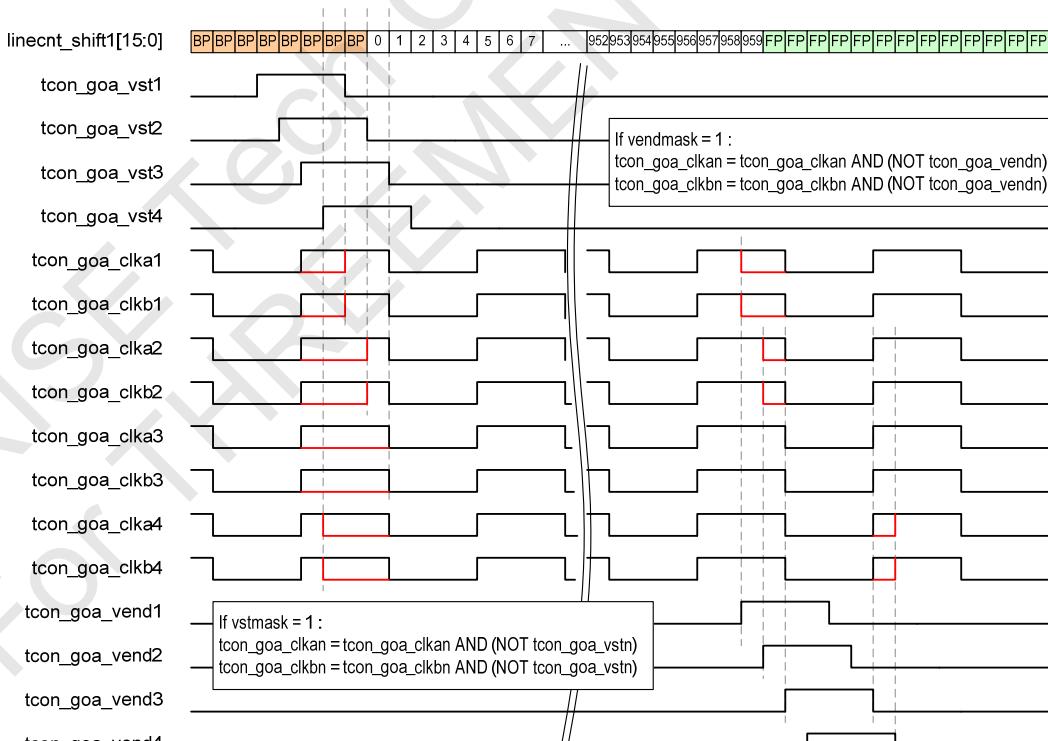
Description	These parameters are used to create eclk type signal and tcon_goa_eclk1~4																							
	Parameters	Description																						
	eclk_normal_width[7:0]	Determines the half-period of tcon_goa_eclk1~4 signals in normal mode, half-period = eclk_normal_width[7:0] – 1 (unit = frames) (Note 1)																						
	eclk_partial_width[7:0]	Determines the half-period of tcon_goa_eclk1~4 signals in partial mode, half-period = eclk_partial_width[7:0] – 1 (unit = frames) (Note 1)																						
	all_normal_tchop[7:0]	Set the tchop (rising edge delay) time for tcon_goa_eclk1~4 signals in normal mode If panel_mode[2:0] = 3'h1, this parameter will override tchop[7:0] parameters for all other goa signals (vstx, vendx, clkax, clkbx, clkdx)																						
	all_partial_tchop[7:0]	Set the tchop (rising edge delay) time for tcon_goa_eclk1~4 signals in partial mode If panel_mode[2:0] = 3'h1, this parameter will override tchop[7:0] parameters for all other goa signals (vstx, vendx, clkax, clkbx, clkdx)																						
	eclk1_follow[3:0]	If eclk_normal_width[7:0] or eclk_partial_width[7:0] = 0, tcon_goa_clk1 outputs the same waveform as one of the tcon_goa_clkx signals according to eclk1_follow[3:0] selection																						
	eclk2_follow[3:0]	If eclk_normal_width[7:0] or eclk_partial_width[7:0] = 0, tcon_goa_clk2 outputs the same waveform as one of the tcon_goa_clkx signals according to eclk2_follow[3:0] selection																						
	eclk3_follow[3:0]	If eclk_normal_width[7:0] or eclk_partial_width[7:0] = 0, tcon_goa_clk3 outputs the same waveform as one of the tcon_goa_clkx signals according to eclk3_follow[3:0] selection																						
	eclk4_follow[3:0]	If eclk_normal_width[7:0] or eclk_partial_width[7:0] = 0, tcon_goa_clk4 outputs the same waveform as one of the tcon_goa_clkx signals according to eclk4_follow[3:0] selection																						
Note 1: Except when eclk_width[7:0] or eclk_width[7:0] is set to 0 or 1.																								
<table border="1"> <tr> <td>eclkx_follow[3:0]</td> <td>tcon_goa_eclkx is the same as:</td> </tr> <tr> <td>0</td> <td>tcno_goa_clk1</td> </tr> <tr> <td>1</td> <td>tcno_goa_clk2</td> </tr> <tr> <td>2</td> <td>tcno_goa_clk3</td> </tr> <tr> <td>3</td> <td>tcno_goa_clk4</td> </tr> <tr> <td>4</td> <td>tcno_goa_clkb1</td> </tr> <tr> <td>5</td> <td>tcno_goa_clkb2</td> </tr> <tr> <td>6</td> <td>tcno_goa_clkb3</td> </tr> <tr> <td>7</td> <td>tcno_goa_clkb4</td> </tr> <tr> <td>8</td> <td>tcno_goa_clkc1</td> </tr> <tr> <td>9</td> <td>tcno_goa_clkc2</td> </tr> </table>			eclkx_follow[3:0]	tcon_goa_eclkx is the same as:	0	tcno_goa_clk1	1	tcno_goa_clk2	2	tcno_goa_clk3	3	tcno_goa_clk4	4	tcno_goa_clkb1	5	tcno_goa_clkb2	6	tcno_goa_clkb3	7	tcno_goa_clkb4	8	tcno_goa_clkc1	9	tcno_goa_clkc2
eclkx_follow[3:0]	tcon_goa_eclkx is the same as:																							
0	tcno_goa_clk1																							
1	tcno_goa_clk2																							
2	tcno_goa_clk3																							
3	tcno_goa_clk4																							
4	tcno_goa_clkb1																							
5	tcno_goa_clkb2																							
6	tcno_goa_clkb3																							
7	tcno_goa_clkb4																							
8	tcno_goa_clkc1																							
9	tcno_goa_clkc2																							

	<table border="1"> <tr><td>10</td><td>tcno_goa_clkc3</td></tr> <tr><td>11</td><td>tcno_goa_clkc4</td></tr> <tr><td>12</td><td>tcno_goa_clkd1</td></tr> <tr><td>13</td><td>tcno_goa_clkd2</td></tr> <tr><td>14</td><td>tcno_goa_clkd3</td></tr> <tr><td>15</td><td>tcno_goa_clkd4</td></tr> </table>	10	tcno_goa_clkc3	11	tcno_goa_clkc4	12	tcno_goa_clkd1	13	tcno_goa_clkd2	14	tcno_goa_clkd3	15	tcno_goa_clkd4
10	tcno_goa_clkc3												
11	tcno_goa_clkc4												
12	tcno_goa_clkd1												
13	tcno_goa_clkd2												
14	tcno_goa_clkd3												
15	tcno_goa_clkd4												
	 <p>Normal mode: $eclk_width[7:0] = eclk_normal_width[7:0]$ Partial mode: $eclk_width[7:0] = eclk_partial_width[7:0]$</p> <p>tcon_goa_eclk1~4 have different initial levels after reset. The initial level is not adjustable.</p> 												
Restriction	- Read and Write, Only accessible when Orise mode is enabled												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr><td>OTP un-programmed</td><td>Set as default value</td></tr> <tr><td>OTP Programmed</td><td>Set as OTP value</td></tr> </tbody> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value						
Status	Default Value												
OTP un-programmed	Set as default value												
OTP Programmed	Set as OTP value												

5.3.64. GOAOPT1(CFC6h) GOA Other Options 1

Address	CFh										
Address (SPI/I2C/MDDI)	CFC6h (0xC7 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	1	
0xC7 th Parameter	Write/Read		0	0	vstmask	vendmask	0	0	dir1_level	dir2_level	01h

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

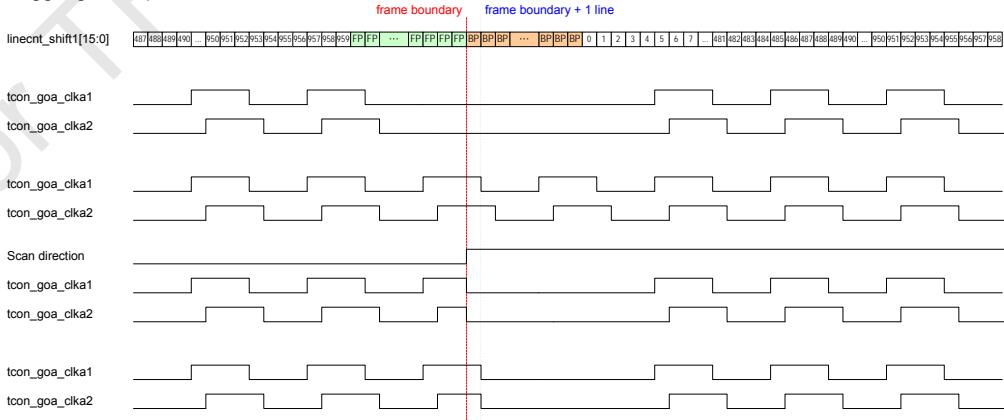
	There parameters are used to adjust additional goa signal options.																				
	<table border="1"> <thead> <tr> <th>Parameters</th><th>Description</th></tr> </thead> <tbody> <tr> <td>vstmask</td><td>0: tcon_goa_clk1~a4, tcon_goa_clkb1~b4 output normal clock waveform 1: tcon_goa_clk1~a4, tcon_goa_clkb4~b4 are logically gated with tcon_goa_vst1~4</td></tr> <tr> <td>vendmask</td><td>0: tcon_goa_clk1~a4, tcon_goa_clkb1~b4 output normal clock waveform 1: tcon_goa_clk1~a4, tcon_goa_clkb4~b4 are logically gated with tcon_goa_vend1~4</td></tr> <tr> <td>dir1_level</td><td>Select DC signal tcon_goa_dir1 output level</td></tr> <tr> <td>dir2_level</td><td>Select DC signal tcon_goa_dir2 output level</td></tr> </tbody> </table>											Parameters	Description	vstmask	0: tcon_goa_clk1~a4, tcon_goa_clkb1~b4 output normal clock waveform 1: tcon_goa_clk1~a4, tcon_goa_clkb4~b4 are logically gated with tcon_goa_vst1~4	vendmask	0: tcon_goa_clk1~a4, tcon_goa_clkb1~b4 output normal clock waveform 1: tcon_goa_clk1~a4, tcon_goa_clkb4~b4 are logically gated with tcon_goa_vend1~4	dir1_level	Select DC signal tcon_goa_dir1 output level	dir2_level	Select DC signal tcon_goa_dir2 output level
Parameters	Description																				
vstmask	0: tcon_goa_clk1~a4, tcon_goa_clkb1~b4 output normal clock waveform 1: tcon_goa_clk1~a4, tcon_goa_clkb4~b4 are logically gated with tcon_goa_vst1~4																				
vendmask	0: tcon_goa_clk1~a4, tcon_goa_clkb1~b4 output normal clock waveform 1: tcon_goa_clk1~a4, tcon_goa_clkb4~b4 are logically gated with tcon_goa_vend1~4																				
dir1_level	Select DC signal tcon_goa_dir1 output level																				
dir2_level	Select DC signal tcon_goa_dir2 output level																				
Description																					

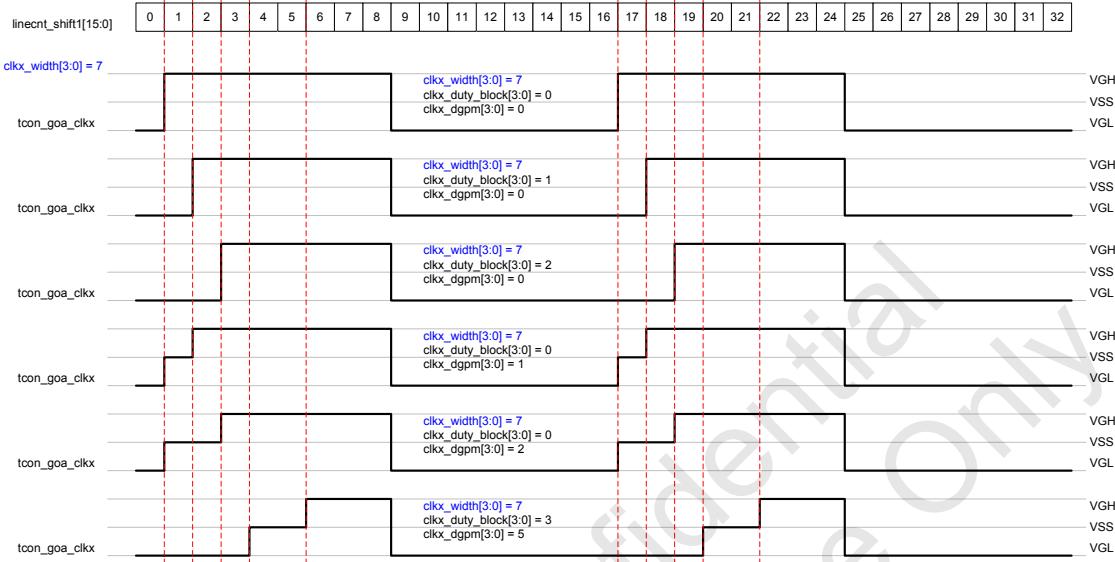
Restriction	- Read and Write, Only accessible when Orise mode is enabled	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	OTP un-programmed	Set as default value
	OTP Programmed	Set as OTP value

5.3.65. GOATGOPT(CFC7h~CFC8h) GOA Signal Toggle Option Setting

Address	CFh										
Address (SPI/I2C/MDDI)	CFC7h ~ CFC8h (0xC8 th ~ 0xC9 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	1	
0xC8 th Parameter	Write/Read		gnd_option	0	0	0	toggle_mod1	toggle_mod2	toggle_mod3	toggle_mod4	01h
0xC9 th Parameter	Write/Read		duty_block[3:0]				dgpm[3:0]				00h

NOTE: “-” Don't care, can be set to VDDIO or VSS level

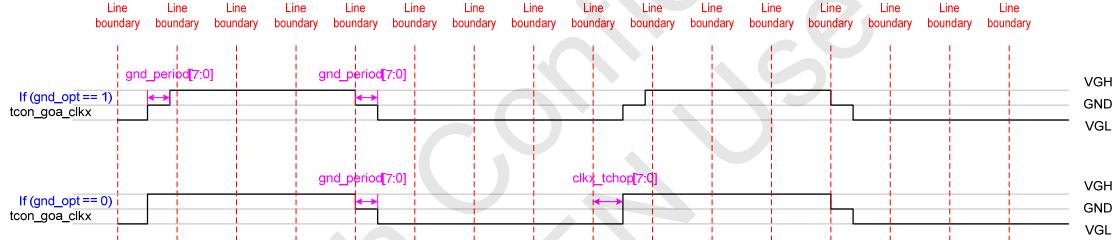
Description	These parameters are used to define global signal behavior for tcon_goa_vstx, tcon_goa_vendx, and tcon_goa_clkx										
	Parameters	Description									
	gnd_option	0: Rising edge of all gate signals goes from VGL to VGH directly 1: Rising edge of all gate signals first pre-charge to GND before reaching VGH. (Note 1)									
	toggle_mod1	0: toggle_mod1 has no effect 1: all tcon_goa_clkx signals will toggle continuously through display region and porch region									
	toggle_mod2	0: toggle_mod2 has no effect 1: all tcon_goa_clkx signals will toggle continuously through display region and porch region except when scan direction changes (normal to reverse, or reverse to normal)									
	toggle_mod3	0: toggle_mod3 has no effect 1: all tcon_goa_clkx signals will toggle continuously until frame boundary + 1 line. The clock signal will stop and restart at the position specified by clkx_shift[11:0]									
	toggle_mod4	0: toggle_mod4 has no effect 1: all tcon_goa_clkx signals will toggle according to behavior specified by clkx_sw_tg, clkx_f_head, clkx_f_tail, clkx_odd_hi, clkx_extend[7:0] and clkx_switch[11:0]									
	duty_block[3:0]	Changes tcon_goa_clkx high-low duty ratio while maintaining clk period									
	dgpm[3:0]	Determines the number of lines GOA signals output VSS before outputting VGH									
	tcon_goa_clkx toggling example:										
											

	<p>tcon_goa_clkx duty ration and VSS time control example:</p> <table border="1"> <tr> <td>linecnt_shift1[15:0]</td><td>0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32</td></tr> </table> 	linecnt_shift1[15:0]	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32										
linecnt_shift1[15:0]	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32												
Restriction	- Read and Write, Only accessible when Orise mode is enabled.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
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Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>OTP un-programmed</td><td>Set as default value</td></tr> <tr> <td>OTP Programmed</td><td>Set as OTP value</td></tr> </tbody> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value						
Status	Default Value												
OTP un-programmed	Set as default value												
OTP Programmed	Set as OTP value												

5.3.66. GOAGNDPRD(CFC9h) GOA Precharge to GND Period

Address	CFh										
Address (SPI/I2C/MDDI)	CFC9h (0xCA th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	0	1	1	1	1	
0xCA th Parameter	Write/Read	gnd_period[7:0]								00h	

NOTE: “-” Don’t care, can be set to VDDIO or VSS level

	<p>These parameters are used to define rising and falling edge pre-charge behaviour for tcon_goa_vstx, tcon_goa_vendx, and tcon_goa_clkx</p> <table border="1"> <thead> <tr> <th>Parameters</th><th>Description</th></tr> </thead> <tbody> <tr> <td>gnd_period[7:0]</td><td>Determines the pre-charge to GND period. (unit = mclk)</td></tr> </tbody> </table> <p>Description</p>  <p>Restriction</p> <ul style="list-style-type: none"> - Read and Write, Only accessible when Orise mode is enabled. <p>Register Availability</p> <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table> <p>Default</p> <table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>OTP un-programmed</td><td>Set as default value</td></tr> <tr> <td>OTP Programmed</td><td>Set as OTP value</td></tr> </tbody> </table>	Parameters	Description	gnd_period[7:0]	Determines the pre-charge to GND period. (unit = mclk)	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value
Parameters	Description																						
gnd_period[7:0]	Determines the pre-charge to GND period. (unit = mclk)																						
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Status	Default Value																						
OTP un-programmed	Set as default value																						
OTP Programmed	Set as OTP value																						

5.3.67. ID1 (D000h): ID1 (Can program 4 times)

Address	D0h										
Address (SPI/I2C/MDDI)	D000h(0x01 st ~ 0x04 th Parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	1	0	0	0	0	D0h
1 st Parameter	Write/Read		ID1[7:0]								40h

Description	- ID1: Module ID 1 (Can program 4 times)																
Restriction	Only access when Orise mode enable.																
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <td>OTP un-programmed</td> <td>Set as default value</td> </tr> <tr> <td>OTP Programmed</td> <td>Set as default value</td> </tr> </table>											Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as default value
Status	Default Value																
OTP un-programmed	Set as default value																
OTP Programmed	Set as default value																

5.3.68. ID2, ID3 (D100h): (Can program 4 times)

Address	D1h										
Address (SPI/I2C/MDDI)	D100h ~ D10Bh (0x01 st ~ 0x0C th Parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	1	0	0	0	1	D1h
1 st Parameter	Write/Read		ID2[7:0]								00h
2 nd Parameter	Write/Read		ID3[7:0]								00h

Description	<ul style="list-style-type: none"> - ID2: Module ID 2 (Can program 4 times) - ID3: Module ID 3 (Can program 4 times) 																
Restriction	Only access when Orise mode enable.																
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <td>OTP un-programmed</td> <td>Set as default value</td> </tr> <tr> <td>OTP Programmed</td> <td>Set as default value</td> </tr> </table>											Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as default value
Status	Default Value																
OTP un-programmed	Set as default value																
OTP Programmed	Set as default value																

5.3.69. DDB (D200h): (Can program 4 times)

Address	D2h										
Address (SPI/I2C/MDDI)	D200h(0x01 st ~ 0x04 th Parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	1	0	0	1	0	D2h
1 st Parameter	Write/Read						DDB1[7:0]				01h
2 nd Parameter	Write/Read						DDB2[7:0]				8Bh
3 rd Parameter	Write/Read						DDB3[7:0]				96h
4 th Parameter	Write/Read						DDB4[7:0]				08h

Description	<ul style="list-style-type: none"> - DDB1[7:0] : For A1/A8 Parameter 1 Read (Can program 4 times) - DDB2[7:0] : For A1/A8 Parameter 2 Read (Can program 4 times) - DDB3[7:0] : For A1/A8 Parameter 3 Read (Can program 4 times) - DDB4[7:0] : For A1/A8 Parameter 4 Read (Can program 4 times) 						
Restriction	Only access when Orise mode enable.						
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">OTP un-programmed</td> <td style="text-align: center;">Set as default value</td> </tr> <tr> <td style="text-align: center;">OTP Programmed</td> <td style="text-align: center;">Set as default value</td> </tr> </tbody> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as default value
Status	Default Value						
OTP un-programmed	Set as default value						
OTP Programmed	Set as default value						

5.3.70. OTPDET (D300h): OTP information

Address	D3h										
Address (SPI/I2C/MDDI)	D300h (0x01 st parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	1	0	0	1	1	D3h
1 st Parameter	Read	00h							votp_det	reg_extc	00h

Description	Bit			Description			Value					
	votp_det			Detect OTP Voltage Flag			0 : OTP Voltage<7.5V 1 : OTP Voltage>7.5V					
	reg_extc			Internal EXTC Value			0 : Internal EXTC = 0 1 : Internal EXTC = 1					
Restriction	- Read, Only access when Orise mode enable.											
Default	Status				Default Value							
	OTP un-programmed				Set as default value							
	OTP Programmed				Set as OTP value							

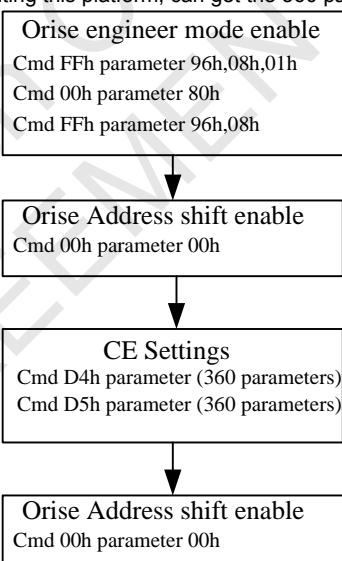
5.3.71. CESET1 (D400h): CE Correction Characteristics Setting 1

Address (MIPI)	D4h										
Address (Other I/F)	D400h										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	1	0	1	0	0	D4h
1 st Parameter	Write/Read					CE1_1[7:0]					00h
2 nd Parameter	Write/Read					CE1_2[7:0]					40h
:	Write/Read					:					
179 th Parameter	Write/Read					CE1_179[7:0]					00h
180 th Parameter	Write/Read					CE1_180[7:0]					40h
181 th Parameter	Write/Read					CE1_181[7:0]					00h
182 th Parameter	Write/Read					CE1_182[7:0]					40h
:	Write/Read					:					
359 th Parameter	Write/Read					CE1_359[7:0]					00h
360 th Parameter	Write/Read					CE1_360[7:0]					40h

Description	<ul style="list-style-type: none"> - Command D4 totally has 360 parameters, these parameters are produced from the "ORISE Color Enhancement SW Platform—OTM9608A.exe". After executing this platform, can get the 360 parameters. 												
	<pre> Orise engineer mode enable Cmd FFh parameter 96h,08h,01h Cmd 00h parameter 80h Cmd FFh parameter 96h,08h ↓ Orise Address shift enable Cmd 00h parameter 00h ↓ CE Settings Cmd D4h parameter (360 parameters) Cmd D5h parameter (360 parameters) ↓ Orise Address shift enable Cmd 00h parameter 00h </pre>												
Restriction	<ul style="list-style-type: none"> - These 360 numbers are the intermediate parameters for the CE algorithm calculation. 												
Availability	<p>Read and Write, Only access when Orise mode enable.</p> <table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>1st、3th~359th : 0x00 ; 2st、4th~360th : 0x40</td></tr> <tr> <td>S/W Reset</td><td>1st、3th~359th : 0x00 ; 2st、4th~360th : 0x40</td></tr> <tr> <td>H/W Reset</td><td>1st、3th~359th : 0x00 ; 2st、4th~360th : 0x40</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	1 st 、3 th ~359 th : 0x00 ; 2 st 、4 th ~360 th : 0x40	S/W Reset	1 st 、3 th ~359 th : 0x00 ; 2 st 、4 th ~360 th : 0x40	H/W Reset	1 st 、3 th ~359 th : 0x00 ; 2 st 、4 th ~360 th : 0x40				
Status	Default Value												
Power On Sequence	1 st 、3 th ~359 th : 0x00 ; 2 st 、4 th ~360 th : 0x40												
S/W Reset	1 st 、3 th ~359 th : 0x00 ; 2 st 、4 th ~360 th : 0x40												
H/W Reset	1 st 、3 th ~359 th : 0x00 ; 2 st 、4 th ~360 th : 0x40												

5.3.72. CESET2(D500h): CE Correction Characteristics Setting 2

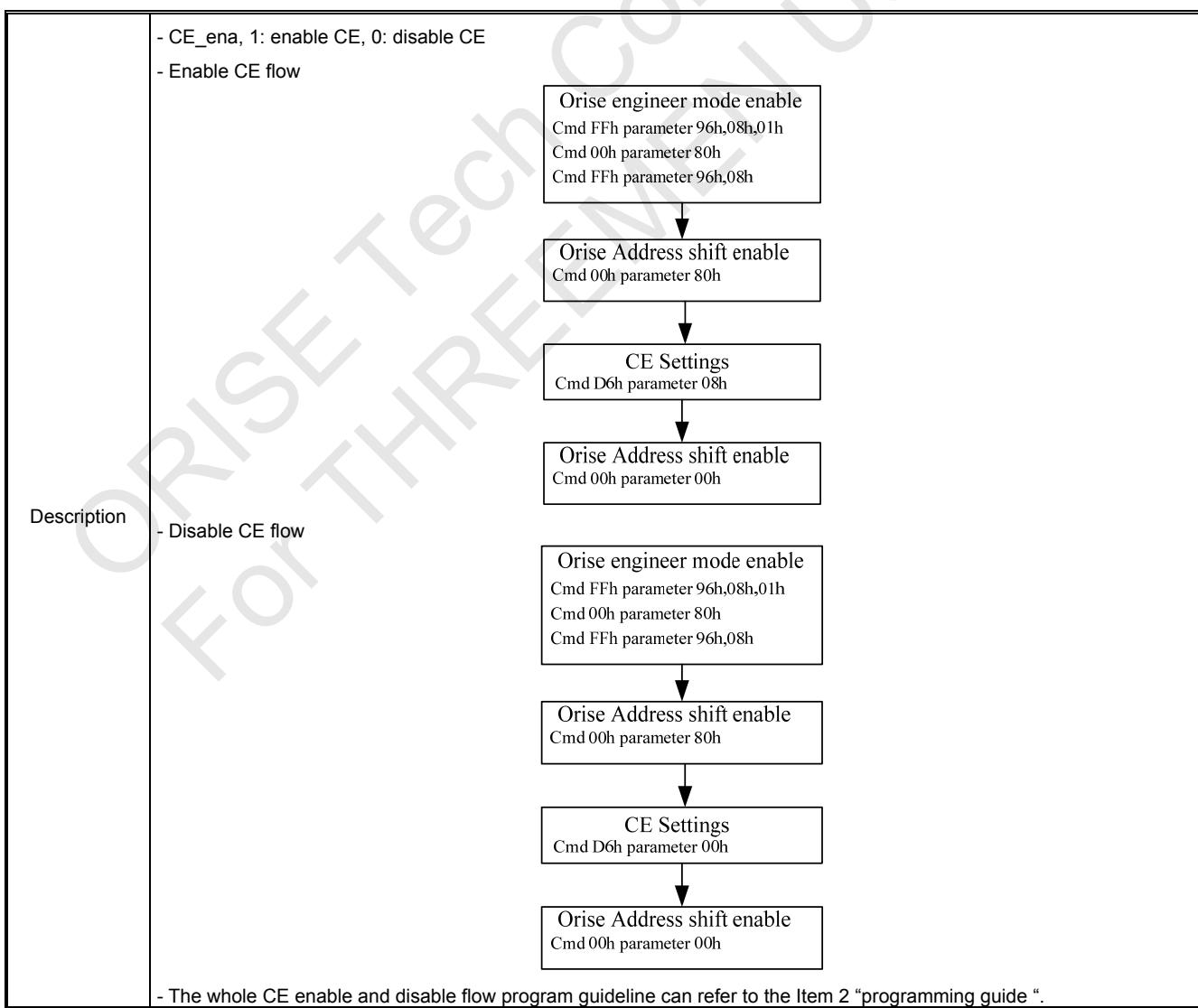
Address (MIPI)	D5h										
Address (Other I/F)	D500h										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	1	0	1	0	1	D5h
1 st Parameter	Write/Read						CE1_1[7:0]				00h
2 nd Parameter	Write/Read						CE1_2[7:0]				40h
:	Write/Read						:				
179 th Parameter	Write/Read						CE1_179[7:0]				00h
180 th Parameter	Write/Read						CE1_180[7:0]				40h
181 th Parameter	Write/Read						CE1_181[7:0]				00h
182 th Parameter	Write/Read						CE1_182[7:0]				40h
:	Write/Read						:				
359 th Parameter	Write/Read						CE1_359[7:0]				00h
360 th Parameter	Write/Read						CE1_360[7:0]				40h

Description	<p>- Command D4 totally has 360 parameters, these parameters are produced from the "ORISE Color Enhancement SW Platform—OTM9608A.exe". After executing this platform, can get the 360 parameters.</p>  <p>- These 360 numbers are the intermediate parameters for the CE algorithm calculation.</p>												
	<p>- Read and Write, Only access when Orise mode enable.</p>												
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												

Default	Status		Default Value							
	Power On Sequence		1 st ~3 th : 0x00 ; 2 st ~4 th : 0x40							
	S/W Reset		1 st ~3 th : 0x00 ; 2 st ~4 th : 0x40							
	H/W Reset		1 st ~3 th : 0x00 ; 2 st ~4 th : 0x40							

5.3.73. CEEN(D680h): CE Enable

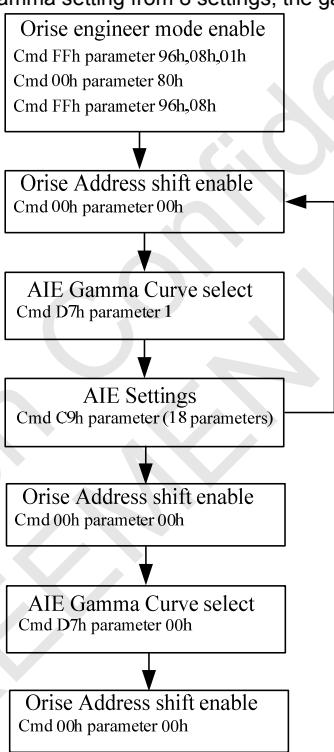
Address (MIPI)	D6h										
Address (Other I/F)	D680h										
Inst. / Para.	Write/Read	D[15:8] 1	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	1	0	1	1	0	D6h
81 Parameter	Write/Read		-	-	-	-	CE_ena	-	-	-	08h



Restriction	- Read and Write, Only access when Orise mode enable.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h

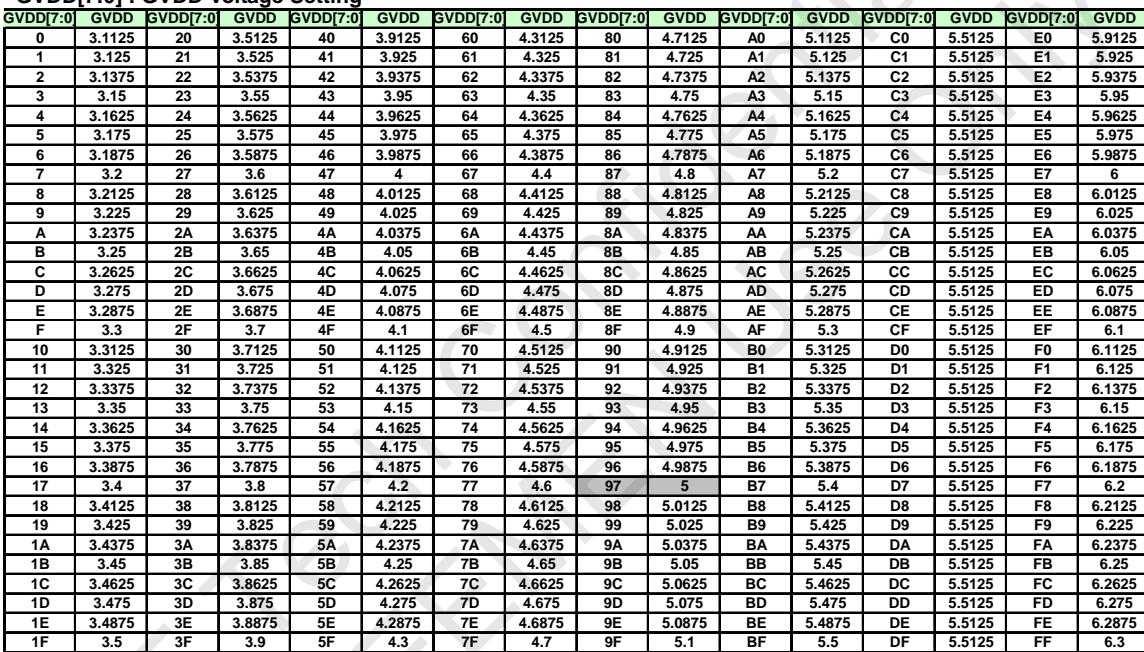
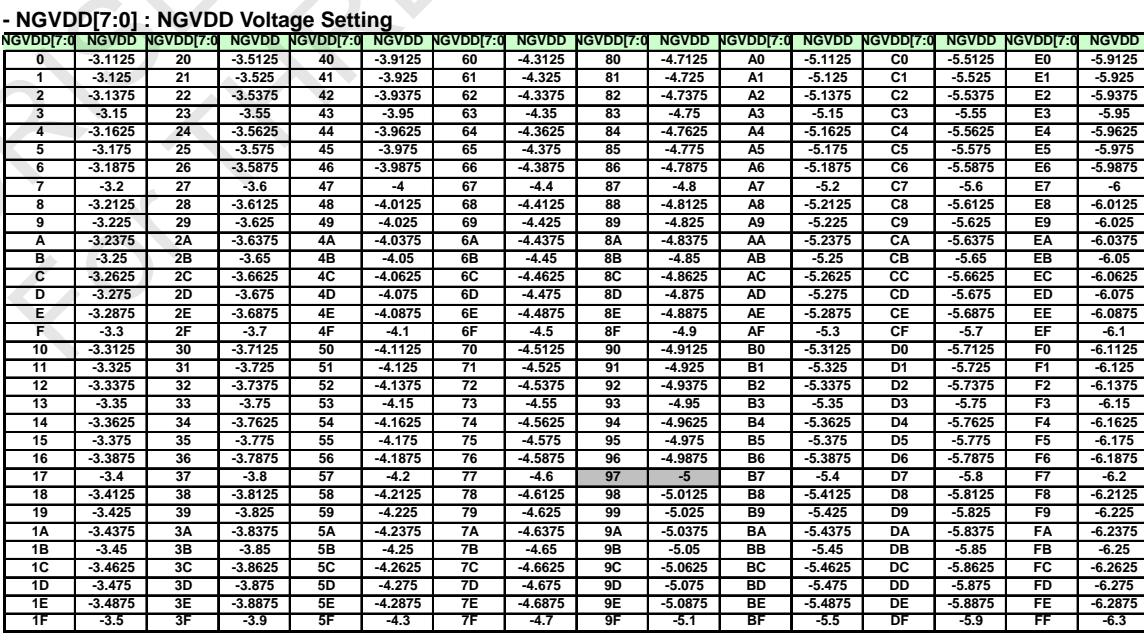
5.3.74. AIEEN(D700h): AIE Enable

Address (MIPI)	D7h									
Address (Other I/F)	D700h									
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
Instruction	Write	00h	1	1	0	1	0	1	1	1
Parameter	Write		-	-	-	-	AIE_ena	AIE_SEL [2:0]		00h

Description	<ul style="list-style-type: none"> - AIE_ena, 1: enable AIE, 0: disable AIE - AIE_SEL [2:0]: AIE_SEL to select one Gamma setting from 8 settings, the gamma need been select by user manual. 												
Restriction	- Write, Only access when Orise mode enable.												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Power On Sequence</td> <td style="text-align: center;">00h</td> </tr> <tr> <td style="text-align: center;">S/W Reset</td> <td style="text-align: center;">00h</td> </tr> <tr> <td style="text-align: center;">H/W Reset</td> <td style="text-align: center;">00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

5.3.75. GVDDSET (D800h): GVDD/NGVDD

Address	D8h										
Address (SPI/I2C/MDDI)	D8001h ~ D802h (0x01 st ~ 0x02 th parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	1	1	0	0	0	D8h
1 st Parameter	Write/Read		GVDD[7:0]								97h
2 nd Parameter	Write/Read		NGVDD[7:0]								97h

- GVDD[7:0] : GVDD Voltage Setting 	Description
- NGVDD[7:0] : NGVDD Voltage Setting 	
	Restriction - Read and Write, Only access when Orise mode enable.

Default	Status	Default Value
	OTP un-programmed	Set as default value
	OTP programmed	Set as OTP value

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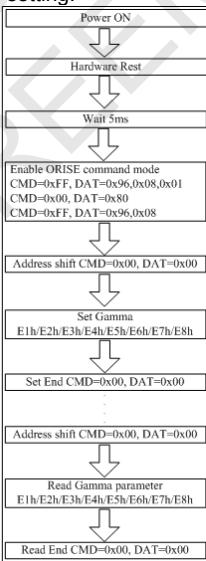
5.3.76. VCOMDC (D900h): VCOM voltage setting

Address	D9h										
Address (SPI/I2C/MDDI)	D900h										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	0	1	1	0	0	1	D9h
1 st Parameter	Write/Read						VCOMDC				39h

Description	- VCOMDC represent the VCOMDC voltage																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																															
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<table border="1"> <thead> <tr> <th>VCOM[7:0]</th><th>VCOM</th><th>VCOM[7:0]</th><th>VCOM</th><th>VCOM[7:0]</th><th>VCOM</th><th>VCOM[7:0]</th><th>VCOM</th><th>VCOM[7:0]</th><th>VCOM</th><th>VCOM[7:0]</th><th>VCOM</th><th>VCOM[7:0]</th><th>VCOM</th><th>VCOM[7:0]</th><th>VCOM</th> </tr> </thead> <tbody> <tr><td>0</td><td>0.0000</td><td>20</td><td>-0.6875</td><td>40</td><td>-1.0875</td><td>60</td><td>-1.4875</td><td>80</td><td>-1.8875</td><td>A0</td><td>-2.2875</td><td>C0</td><td>-2.6875</td><td>E0</td><td>-3.0875</td></tr> <tr><td>1</td><td>-0.3000</td><td>21</td><td>-0.7000</td><td>41</td><td>-1.1000</td><td>61</td><td>-1.5000</td><td>81</td><td>-1.9000</td><td>A1</td><td>-2.3000</td><td>C1</td><td>-2.7000</td><td>E1</td><td>-3.1000</td></tr> <tr><td>2</td><td>-0.3125</td><td>22</td><td>-0.7125</td><td>42</td><td>-1.1125</td><td>62</td><td>-1.5125</td><td>82</td><td>-1.9125</td><td>A2</td><td>-2.3125</td><td>C2</td><td>-2.7125</td><td>E2</td><td>-3.1125</td></tr> <tr><td>3</td><td>-0.3250</td><td>23</td><td>-0.7250</td><td>43</td><td>-1.1250</td><td>63</td><td>-1.5250</td><td>83</td><td>-1.9250</td><td>A3</td><td>-2.3250</td><td>C3</td><td>-2.7250</td><td>E3</td><td>-3.1250</td></tr> <tr><td>4</td><td>-0.3375</td><td>24</td><td>-0.7375</td><td>44</td><td>-1.1375</td><td>64</td><td>-1.5375</td><td>84</td><td>-1.9375</td><td>A4</td><td>-2.3375</td><td>C4</td><td>-2.7375</td><td>E4</td><td>-3.1375</td></tr> <tr><td>5</td><td>-0.3500</td><td>25</td><td>-0.7500</td><td>45</td><td>-1.1500</td><td>65</td><td>-1.5500</td><td>85</td><td>-1.9500</td><td>A5</td><td>-2.3500</td><td>C5</td><td>-2.7500</td><td>E5</td><td>-3.1500</td></tr> <tr><td>6</td><td>-0.3625</td><td>26</td><td>-0.7625</td><td>46</td><td>-1.1625</td><td>66</td><td>-1.5625</td><td>86</td><td>-1.9625</td><td>A6</td><td>-2.3625</td><td>C6</td><td>-2.7625</td><td>E6</td><td>-3.1625</td></tr> <tr><td>7</td><td>-0.3750</td><td>27</td><td>-0.7750</td><td>47</td><td>-1.1750</td><td>67</td><td>-1.5750</td><td>87</td><td>-1.9750</td><td>A7</td><td>-2.3750</td><td>C7</td><td>-2.7750</td><td>E7</td><td>-3.1750</td></tr> <tr><td>8</td><td>-0.3875</td><td>28</td><td>-0.7875</td><td>48</td><td>-1.1875</td><td>68</td><td>-1.5875</td><td>88</td><td>-1.9875</td><td>A8</td><td>-2.3875</td><td>C8</td><td>-2.7875</td><td>E8</td><td>-3.1875</td></tr> <tr><td>9</td><td>-0.4000</td><td>29</td><td>-0.8000</td><td>49</td><td>-1.2000</td><td>69</td><td>-1.6000</td><td>89</td><td>-2.0000</td><td>A9</td><td>-2.4000</td><td>C9</td><td>-2.8000</td><td>E9</td><td>-3.2000</td></tr> <tr><td>A</td><td>-0.4125</td><td>2A</td><td>-0.8125</td><td>4A</td><td>-1.2125</td><td>6A</td><td>-1.6125</td><td>8A</td><td>-2.0125</td><td>AA</td><td>-2.4125</td><td>CA</td><td>-2.8125</td><td>EA</td><td>-3.2125</td></tr> <tr><td>B</td><td>-0.4250</td><td>2B</td><td>-0.8250</td><td>4B</td><td>-1.2250</td><td>6B</td><td>-1.6250</td><td>8B</td><td>-2.0250</td><td>AB</td><td>-2.4250</td><td>CB</td><td>-2.8250</td><td>EB</td><td>-3.2250</td></tr> <tr><td>C</td><td>-0.4375</td><td>2C</td><td>-0.8375</td><td>4C</td><td>-1.2375</td><td>6C</td><td>-1.6375</td><td>8C</td><td>-2.0375</td><td>AC</td><td>-2.4375</td><td>CC</td><td>-2.8375</td><td>EC</td><td>-3.2375</td></tr> <tr><td>D</td><td>-0.4500</td><td>2D</td><td>-0.8500</td><td>4D</td><td>-1.2500</td><td>6D</td><td>-1.6500</td><td>8D</td><td>-2.0500</td><td>AD</td><td>-2.4500</td><td>CD</td><td>-2.8500</td><td>ED</td><td>-3.2500</td></tr> <tr><td>E</td><td>-0.4625</td><td>2E</td><td>-0.8625</td><td>4E</td><td>-1.2625</td><td>6E</td><td>-1.6625</td><td>8E</td><td>-2.0625</td><td>AE</td><td>-2.4625</td><td>CE</td><td>-2.8625</td><td>EE</td><td>-3.2625</td></tr> <tr><td>F</td><td>-0.4750</td><td>2F</td><td>-0.8750</td><td>4F</td><td>-1.2750</td><td>6F</td><td>-1.6750</td><td>8F</td><td>-2.0750</td><td>AF</td><td>-2.4750</td><td>CF</td><td>-2.8750</td><td>EF</td><td>-3.2750</td></tr> <tr><td>10</td><td>-0.4875</td><td>30</td><td>-0.8875</td><td>50</td><td>-1.2875</td><td>70</td><td>-1.6875</td><td>90</td><td>-2.0875</td><td>B0</td><td>-2.4875</td><td>D0</td><td>-2.8875</td><td>F0</td><td>-3.2875</td></tr> <tr><td>11</td><td>-0.5000</td><td>31</td><td>-0.9000</td><td>51</td><td>-1.3000</td><td>71</td><td>-1.7000</td><td>91</td><td>-2.1000</td><td>B1</td><td>-2.5000</td><td>D1</td><td>-2.9000</td><td>F1</td><td>-3.3000</td></tr> <tr><td>12</td><td>-0.5125</td><td>32</td><td>-0.9125</td><td>52</td><td>-1.3125</td><td>72</td><td>-1.7125</td><td>92</td><td>-2.1125</td><td>B2</td><td>-2.5125</td><td>D2</td><td>-2.9125</td><td>F2</td><td>-3.3125</td></tr> <tr><td>13</td><td>-0.5250</td><td>33</td><td>-0.9250</td><td>53</td><td>-1.3250</td><td>73</td><td>-1.7250</td><td>93</td><td>-2.1250</td><td>B3</td><td>-2.5250</td><td>D3</td><td>-2.9250</td><td>F3</td><td>-3.3250</td></tr> <tr><td>14</td><td>-0.5375</td><td>34</td><td>-0.9375</td><td>54</td><td>-1.3375</td><td>74</td><td>-1.7375</td><td>94</td><td>-2.1375</td><td>B4</td><td>-2.5375</td><td>D4</td><td>-2.9375</td><td>F4</td><td>-3.3375</td></tr> <tr><td>15</td><td>-0.5500</td><td>35</td><td>-0.9500</td><td>55</td><td>-1.3500</td><td>75</td><td>-1.7500</td><td>95</td><td>-2.1500</td><td>B5</td><td>-2.5500</td><td>D5</td><td>-2.9500</td><td>F5</td><td>-3.3500</td></tr> <tr><td>16</td><td>-0.5625</td><td>36</td><td>-0.9625</td><td>56</td><td>-1.3625</td><td>76</td><td>-1.7625</td><td>96</td><td>-2.1625</td><td>B6</td><td>-2.5625</td><td>D6</td><td>-2.9625</td><td>F6</td><td>-3.3625</td></tr> <tr><td>17</td><td>-0.5750</td><td>37</td><td>-0.9750</td><td>57</td><td>-1.3750</td><td>77</td><td>-1.7750</td><td>97</td><td>-2.1750</td><td>B7</td><td>-2.5750</td><td>D7</td><td>-2.9750</td><td>F7</td><td>-3.3750</td></tr> <tr><td>18</td><td>-0.5875</td><td>38</td><td>-0.9875</td><td>58</td><td>-1.3875</td><td>78</td><td>-1.7875</td><td>98</td><td>-2.1875</td><td>B8</td><td>-2.5875</td><td>D8</td><td>-2.9875</td><td>F8</td><td>-3.3875</td></tr> <tr><td>19</td><td>-0.6000</td><td>39</td><td>-1.0000</td><td>59</td><td>-1.4000</td><td>79</td><td>-1.8000</td><td>99</td><td>-2.2000</td><td>B9</td><td>-2.6000</td><td>D9</td><td>-3.0000</td><td>F9</td><td>-3.4000</td></tr> <tr><td>1A</td><td>-0.6125</td><td>3A</td><td>-1.0125</td><td>5A</td><td>-1.4125</td><td>7A</td><td>-1.8125</td><td>9A</td><td>-2.2125</td><td>BA</td><td>-2.6125</td><td>DA</td><td>-3.0125</td><td>FA</td><td>-3.4125</td></tr> <tr><td>1B</td><td>-0.6250</td><td>3B</td><td>-1.0250</td><td>5B</td><td>-1.4250</td><td>7B</td><td>-1.8250</td><td>9B</td><td>-2.2250</td><td>BB</td><td>-2.6250</td><td>DB</td><td>-3.0250</td><td>FB</td><td>-3.4250</td></tr> <tr><td>1C</td><td>-0.6375</td><td>3C</td><td>-1.0375</td><td>5C</td><td>-1.4375</td><td>7C</td><td>-1.8375</td><td>9C</td><td>-2.2375</td><td>BC</td><td>-2.6375</td><td>DC</td><td>-3.0375</td><td>FC</td><td>-3.4375</td></tr> <tr><td>1D</td><td>-0.6500</td><td>3D</td><td>-1.0500</td><td>5D</td><td>-1.4500</td><td>7D</td><td>-1.8500</td><td>9D</td><td>-2.2500</td><td>BD</td><td>-2.6500</td><td>DD</td><td>-3.0500</td><td>FD</td><td>-3.4500</td></tr> <tr><td>1E</td><td>-0.6625</td><td>3E</td><td>-1.0625</td><td>5E</td><td>-1.4625</td><td>7E</td><td>-1.8625</td><td>9E</td><td>-2.2625</td><td>BE</td><td>-2.6625</td><td>DE</td><td>-3.0625</td><td>FE</td><td>-3.4625</td></tr> <tr><td>1F</td><td>-0.6750</td><td>3F</td><td>-1.0750</td><td>5F</td><td>-1.4750</td><td>7F</td><td>-1.8750</td><td>9F</td><td>-2.2750</td><td>BF</td><td>-2.6750</td><td>DF</td><td>-3.0750</td><td>FF</td><td>-3.4750</td></tr> </tbody></table>	VCOM[7:0]	VCOM	VCOM[7:0]	VCOM	VCOM[7:0]	VCOM	VCOM[7:0]	VCOM	VCOM[7:0]	VCOM	VCOM[7:0]	VCOM	VCOM[7:0]	VCOM	VCOM[7:0]	VCOM	0	0.0000	20	-0.6875	40	-1.0875	60	-1.4875	80	-1.8875	A0	-2.2875	C0	-2.6875	E0	-3.0875	1	-0.3000	21	-0.7000	41	-1.1000	61	-1.5000	81	-1.9000	A1	-2.3000	C1	-2.7000	E1	-3.1000	2	-0.3125	22	-0.7125	42	-1.1125	62	-1.5125	82	-1.9125	A2	-2.3125	C2	-2.7125	E2	-3.1125	3	-0.3250	23	-0.7250	43	-1.1250	63	-1.5250	83	-1.9250	A3	-2.3250	C3	-2.7250	E3	-3.1250	4	-0.3375	24	-0.7375	44	-1.1375	64	-1.5375	84	-1.9375	A4	-2.3375	C4	-2.7375	E4	-3.1375	5	-0.3500	25	-0.7500	45	-1.1500	65	-1.5500	85	-1.9500	A5	-2.3500	C5	-2.7500	E5	-3.1500	6	-0.3625	26	-0.7625	46	-1.1625	66	-1.5625	86	-1.9625	A6	-2.3625	C6	-2.7625	E6	-3.1625	7	-0.3750	27	-0.7750	47	-1.1750	67	-1.5750	87	-1.9750	A7	-2.3750	C7	-2.7750	E7	-3.1750	8	-0.3875	28	-0.7875	48	-1.1875	68	-1.5875	88	-1.9875	A8	-2.3875	C8	-2.7875	E8	-3.1875	9	-0.4000	29	-0.8000	49	-1.2000	69	-1.6000	89	-2.0000	A9	-2.4000	C9	-2.8000	E9	-3.2000	A	-0.4125	2A	-0.8125	4A	-1.2125	6A	-1.6125	8A	-2.0125	AA	-2.4125	CA	-2.8125	EA	-3.2125	B	-0.4250	2B	-0.8250	4B	-1.2250	6B	-1.6250	8B	-2.0250	AB	-2.4250	CB	-2.8250	EB	-3.2250	C	-0.4375	2C	-0.8375	4C	-1.2375	6C	-1.6375	8C	-2.0375	AC	-2.4375	CC	-2.8375	EC	-3.2375	D	-0.4500	2D	-0.8500	4D	-1.2500	6D	-1.6500	8D	-2.0500	AD	-2.4500	CD	-2.8500	ED	-3.2500	E	-0.4625	2E	-0.8625	4E	-1.2625	6E	-1.6625	8E	-2.0625	AE	-2.4625	CE	-2.8625	EE	-3.2625	F	-0.4750	2F	-0.8750	4F	-1.2750	6F	-1.6750	8F	-2.0750	AF	-2.4750	CF	-2.8750	EF	-3.2750	10	-0.4875	30	-0.8875	50	-1.2875	70	-1.6875	90	-2.0875	B0	-2.4875	D0	-2.8875	F0	-3.2875	11	-0.5000	31	-0.9000	51	-1.3000	71	-1.7000	91	-2.1000	B1	-2.5000	D1	-2.9000	F1	-3.3000	12	-0.5125	32	-0.9125	52	-1.3125	72	-1.7125	92	-2.1125	B2	-2.5125	D2	-2.9125	F2	-3.3125	13	-0.5250	33	-0.9250	53	-1.3250	73	-1.7250	93	-2.1250	B3	-2.5250	D3	-2.9250	F3	-3.3250	14	-0.5375	34	-0.9375	54	-1.3375	74	-1.7375	94	-2.1375	B4	-2.5375	D4	-2.9375	F4	-3.3375	15	-0.5500	35	-0.9500	55	-1.3500	75	-1.7500	95	-2.1500	B5	-2.5500	D5	-2.9500	F5	-3.3500	16	-0.5625	36	-0.9625	56	-1.3625	76	-1.7625	96	-2.1625	B6	-2.5625	D6	-2.9625	F6	-3.3625	17	-0.5750	37	-0.9750	57	-1.3750	77	-1.7750	97	-2.1750	B7	-2.5750	D7	-2.9750	F7	-3.3750	18	-0.5875	38	-0.9875	58	-1.3875	78	-1.7875	98	-2.1875	B8	-2.5875	D8	-2.9875	F8	-3.3875	19	-0.6000	39	-1.0000	59	-1.4000	79	-1.8000	99	-2.2000	B9	-2.6000	D9	-3.0000	F9	-3.4000	1A	-0.6125	3A	-1.0125	5A	-1.4125	7A	-1.8125	9A	-2.2125	BA	-2.6125	DA	-3.0125	FA	-3.4125	1B	-0.6250	3B	-1.0250	5B	-1.4250	7B	-1.8250	9B	-2.2250	BB	-2.6250	DB	-3.0250	FB	-3.4250	1C	-0.6375	3C	-1.0375	5C	-1.4375	7C	-1.8375	9C	-2.2375	BC	-2.6375	DC	-3.0375	FC	-3.4375	1D	-0.6500	3D	-1.0500	5D	-1.4500	7D	-1.8500	9D	-2.2500	BD	-2.6500	DD	-3.0500	FD	-3.4500	1E	-0.6625	3E	-1.0625	5E	-1.4625	7E	-1.8625	9E	-2.2625	BE	-2.6625	DE	-3.0625	FE	-3.4625	1F	-0.6750	3F	-1.0750	5F	-1.4750	7F	-1.8750	9F	-2.2750	BF	-2.6750	DF	-3.0750	FF	-3.4750
VCOM[7:0]	VCOM	VCOM[7:0]	VCOM	VCOM[7:0]	VCOM	VCOM[7:0]	VCOM	VCOM[7:0]	VCOM	VCOM[7:0]	VCOM	VCOM[7:0]	VCOM	VCOM[7:0]	VCOM																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
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2	-0.3125	22	-0.7125	42	-1.1125	62	-1.5125	82	-1.9125	A2	-2.3125	C2	-2.7125	E2	-3.1125																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
3	-0.3250	23	-0.7250	43	-1.1250	63	-1.5250	83	-1.9250	A3	-2.3250	C3	-2.7250	E3	-3.1250																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
4	-0.3375	24	-0.7375	44	-1.1375	64	-1.5375	84	-1.9375	A4	-2.3375	C4	-2.7375	E4	-3.1375																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
5	-0.3500	25	-0.7500	45	-1.1500	65	-1.5500	85	-1.9500	A5	-2.3500	C5	-2.7500	E5	-3.1500																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
6	-0.3625	26	-0.7625	46	-1.1625	66	-1.5625	86	-1.9625	A6	-2.3625	C6	-2.7625	E6	-3.1625																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
7	-0.3750	27	-0.7750	47	-1.1750	67	-1.5750	87	-1.9750	A7	-2.3750	C7	-2.7750	E7	-3.1750																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
8	-0.3875	28	-0.7875	48	-1.1875	68	-1.5875	88	-1.9875	A8	-2.3875	C8	-2.7875	E8	-3.1875																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
9	-0.4000	29	-0.8000	49	-1.2000	69	-1.6000	89	-2.0000	A9	-2.4000	C9	-2.8000	E9	-3.2000																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
A	-0.4125	2A	-0.8125	4A	-1.2125	6A	-1.6125	8A	-2.0125	AA	-2.4125	CA	-2.8125	EA	-3.2125																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
B	-0.4250	2B	-0.8250	4B	-1.2250	6B	-1.6250	8B	-2.0250	AB	-2.4250	CB	-2.8250	EB	-3.2250																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
C	-0.4375	2C	-0.8375	4C	-1.2375	6C	-1.6375	8C	-2.0375	AC	-2.4375	CC	-2.8375	EC	-3.2375																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
D	-0.4500	2D	-0.8500	4D	-1.2500	6D	-1.6500	8D	-2.0500	AD	-2.4500	CD	-2.8500	ED	-3.2500																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
E	-0.4625	2E	-0.8625	4E	-1.2625	6E	-1.6625	8E	-2.0625	AE	-2.4625	CE	-2.8625	EE	-3.2625																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
F	-0.4750	2F	-0.8750	4F	-1.2750	6F	-1.6750	8F	-2.0750	AF	-2.4750	CF	-2.8750	EF	-3.2750																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
10	-0.4875	30	-0.8875	50	-1.2875	70	-1.6875	90	-2.0875	B0	-2.4875	D0	-2.8875	F0	-3.2875																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
11	-0.5000	31	-0.9000	51	-1.3000	71	-1.7000	91	-2.1000	B1	-2.5000	D1	-2.9000	F1	-3.3000																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
12	-0.5125	32	-0.9125	52	-1.3125	72	-1.7125	92	-2.1125	B2	-2.5125	D2	-2.9125	F2	-3.3125																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
13	-0.5250	33	-0.9250	53	-1.3250	73	-1.7250	93	-2.1250	B3	-2.5250	D3	-2.9250	F3	-3.3250																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
14	-0.5375	34	-0.9375	54	-1.3375	74	-1.7375	94	-2.1375	B4	-2.5375	D4	-2.9375	F4	-3.3375																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
15	-0.5500	35	-0.9500	55	-1.3500	75	-1.7500	95	-2.1500	B5	-2.5500	D5	-2.9500	F5	-3.3500																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
16	-0.5625	36	-0.9625	56	-1.3625	76	-1.7625	96	-2.1625	B6	-2.5625	D6	-2.9625	F6	-3.3625																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
17	-0.5750	37	-0.9750	57	-1.3750	77	-1.7750	97	-2.1750	B7	-2.5750	D7	-2.9750	F7	-3.3750																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
18	-0.5875	38	-0.9875	58	-1.3875	78	-1.7875	98	-2.1875	B8	-2.5875	D8	-2.9875	F8	-3.3875																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
19	-0.6000	39	-1.0000	59	-1.4000	79	-1.8000	99	-2.2000	B9	-2.6000	D9	-3.0000	F9	-3.4000																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
1A	-0.6125	3A	-1.0125	5A	-1.4125	7A	-1.8125	9A	-2.2125	BA	-2.6125	DA	-3.0125	FA	-3.4125																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
1B	-0.6250	3B	-1.0250	5B	-1.4250	7B	-1.8250	9B	-2.2250	BB	-2.6250	DB	-3.0250	FB	-3.4250																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
1C	-0.6375	3C	-1.0375	5C	-1.4375	7C	-1.8375	9C	-2.2375	BC	-2.6375	DC	-3.0375	FC	-3.4375																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
1D	-0.6500	3D	-1.0500	5D	-1.4500	7D	-1.8500	9D	-2.2500	BD	-2.6500	DD	-3.0500	FD	-3.4500																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
1E	-0.6625	3E	-1.0625	5E	-1.4625	7E	-1.8625	9E	-2.2625	BE	-2.6625	DE	-3.0625	FE	-3.4625																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
1F	-0.6750	3F	-1.0750	5F	-1.4750	7F	-1.8750	9F	-2.2750	BF	-2.6750	DF	-3.0750	FF	-3.4750																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																	
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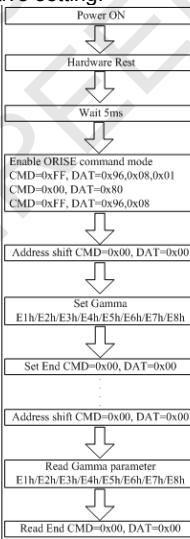
5.3.77. GMCT2.2P (E100h): Gamma Correction Characteristics Setting (2.2 +)

Address	E1h										
Address (SPI/I2C/MDDI)	E100h ~ E10Fh (0x01 st ~0x16 nd Parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	1	0	0	0	0	1	E1h
1 st Parameter	Write/Read		0	0	G22P1	G22P1	G22P1	G22P1	G22P1	G22P1	05h
2 nd Parameter	Write/Read		0	0	G22P2	G22P2	G22P2	G22P2	G22P2	G22P2	0Bh
3 rd Parameter	Write/Read		0	0	G22P3	G22P3	G22P3	G22P3	G22P3	G22P3	1Ah
4 th Parameter	Write/Read		0	0	-	G22P4	G22P4	G22P4	G22P4	G22P4	15h
5 th Parameter	Write/Read		0	0	-	G22P5	G22P5	G22P5	G22P5	G22P5	0Eh
6 th Parameter	Write/Read		0	0	-	G22P6	G22P6	G22P6	G22P6	G22P6	06h
7 th Parameter	Write/Read		0	0	-	-	G22P7	G22P7	G22P7	G22P7	0Eh
8 th Parameter	Write/Read		0	0	-	-	G22P8	G22P8	G22P8	G22P8	0Bh
9 th Parameter	Write/Read		0	0	-	-	G22P9	G22P9	G22P9	G22P9	0Bh
10 th Parameter	Write/Read		0	0	-	-	G22P10	G22P10	G22P10	G22P10	04h
11 st Parameter	Write/Read		0	0	-	G22P11	G22P11	G22P11	G22P11	G22P11	06h
12 nd Parameter	Write/Read		0	0	-	G22P12	G22P12	G22P12	G22P12	G22P12	14h
13 rd Parameter	Write/Read		0	0	-	G22P13	G22P13	G22P13	G22P13	G22P13	0Ah
14 th Parameter	Write/Read		0	0	G22P14	G22P14	G22P14	G22P14	G22P14	G22P14	10h
15 th Parameter	Write/Read		0	0	G22P15	G22P15	G22P15	G22P15	G22P15	G22P15	22h
16 th Parameter	Write/Read		0	0	G22P16	G22P16	G22P16	G22P16	G22P16	G22P16	17h

Description	<p>- Gamma adjustment for 2.2 positive setting.</p> <table border="1"> <tr><th colspan="2">Gamma adjustment for 2.2 positive setting</th></tr> <tr><td>G22P1</td><td>+ Level 0</td></tr> <tr><td>G22P2</td><td>+ Level 4</td></tr> <tr><td>G22P3</td><td>+ Level 8</td></tr> <tr><td>G22P4</td><td>+ Level 16</td></tr> <tr><td>G22P5</td><td>+ Level 24</td></tr> <tr><td>G22P6</td><td>+ Level 52</td></tr> <tr><td>G22P7</td><td>+ Level 80</td></tr> <tr><td>G22P8</td><td>+ Level 108</td></tr> <tr><td>G22P9</td><td>+ Level 147</td></tr> <tr><td>G22P10</td><td>+ Level 175</td></tr> <tr><td>G22P11</td><td>+ Level 203</td></tr> <tr><td>G22P12</td><td>+ Level 231</td></tr> <tr><td>G22P13</td><td>+ Level 239</td></tr> <tr><td>G22P14</td><td>+ Level 247</td></tr> <tr><td>G22P15</td><td>+ Level 251</td></tr> <tr><td>G22P16</td><td>+ Level 255</td></tr> </table> 											Gamma adjustment for 2.2 positive setting		G22P1	+ Level 0	G22P2	+ Level 4	G22P3	+ Level 8	G22P4	+ Level 16	G22P5	+ Level 24	G22P6	+ Level 52	G22P7	+ Level 80	G22P8	+ Level 108	G22P9	+ Level 147	G22P10	+ Level 175	G22P11	+ Level 203	G22P12	+ Level 231	G22P13	+ Level 239	G22P14	+ Level 247	G22P15	+ Level 251	G22P16	+ Level 255
Gamma adjustment for 2.2 positive setting																																													
G22P1	+ Level 0																																												
G22P2	+ Level 4																																												
G22P3	+ Level 8																																												
G22P4	+ Level 16																																												
G22P5	+ Level 24																																												
G22P6	+ Level 52																																												
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G22P8	+ Level 108																																												
G22P9	+ Level 147																																												
G22P10	+ Level 175																																												
G22P11	+ Level 203																																												
G22P12	+ Level 231																																												
G22P13	+ Level 239																																												
G22P14	+ Level 247																																												
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G22P16	+ Level 255																																												
Restriction	<ul style="list-style-type: none"> - Read and Write, Only access when Orise mode enable. - Gamma value is readable only after the register has been written or the OTP has been programmed. 																																												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>OTP un-programmed</td> <td>Set as default value</td> </tr> <tr> <td>OTP Programmed</td> <td>Set as OTP value</td> </tr> </tbody> </table>											Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value																												
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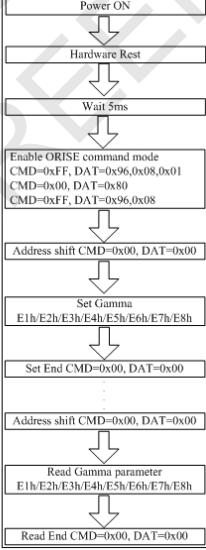
5.3.78. GMCT2.2N (E200h): Gamma Correction Characteristics Setting (2.2 -)

Address	E2h										
Address (SPI/I2C/MDDI)	E200h ~ E20Fh (0x01 st ~0x16 nd Parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	1	0	0	0	1	0	E2h
1 st Parameter	Write/Read		0	0	G22N1	G22N1	G22N1	G22N 1	G22N 1	G22N 1	05h
2 nd Parameter	Write/Read		0	0	G22N2	G22N2	G22N2	G22N2	G22N2	G22N2	0Bh
3 rd Parameter	Write/Read		0	0	G22N3	G22N3	G22N3	G22N3	G22N3	G22N3	1Ah
4 th Parameter	Write/Read		0	0	-	G22N4	G22N4	G22N4	G22N4	G22N4	15h
5 th Parameter	Write/Read		0	0	-	G22N5	G22N5	G22N5	G22N5	G22N5	0Eh
6 th Parameter	Write/Read		0	0	-	G22N6	G22N6	G22N6	G22N6	G22N6	06h
7 th Parameter	Write/Read		0	0	-	-	G22N7	G22N7	G22N7	G22N7	0Eh
8 th Parameter	Write/Read		0	0	-	-	G22N8	G22N8	G22N8	G22N8	0Bh
9 th Parameter	Write/Read		0	0	-	-	G22N9	G22N9	G22N9	G22N9	0Bh
10 th Parameter	Write/Read		0	0	-	-	G22N 10	G22N 10	G22N 10	G22N 10	04h
11 st Parameter	Write/Read		0	0	-	G22N 11	G22N 11	G22N11	G22N11	G22N11	06h
12 nd Parameter	Write/Read		0	0	-	G22N 12	G22N 12	G22N12	G22N12	G22N12	14h
13 rd Parameter	Write/Read		0	0	-	G22N 13	G22N 13	G22N13	G22N13	G22N13	0Ah
14 th Parameter	Write/Read		0	0	G22N 14	G22N 14	G22N 14	G22N14	G22N14	G22N14	10h
15 th Parameter	Write/Read		0	0	G22N 15	G22N 15	G22N 15	G22N15	G22N15	G22N15	22h
16 th Parameter	Write/Read		0	0	G22N 16	G22N 16	G22N 16	G22N16	G22N16	G22N16	17h

Description	- Gamma adjustment for 2.2 negative setting. Gamma adjustment for 2.2 negative setting G22N1 - Level 0 G22N2 - Level 4 G22N3 - Level 8 G22N4 - Level 16 G22N5 - Level 24 G22N6 - Level 52 G22N7 - Level 80 G22N8 - Level 108 G22N9 - Level 147 G22N10 - Level 175 G22N11 - Level 203 G22N12 - Level 231 G22N13 - Level 239 G22N14 - Level 247 G22N15 - Level 251 G22N16 - Level 255					
	- Read and Write, Only access when Orise mode enable.					
	- Gamma value is readable only after the register has been written or the OTP has been programmed.					
	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>OTP un-programmed</td> <td>Set as default value</td> </tr> <tr> <td>OTP Programmed</td> <td>Set as OTP value</td> </tr> </tbody> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed
Status	Default Value					
OTP un-programmed	Set as default value					
OTP Programmed	Set as OTP value					

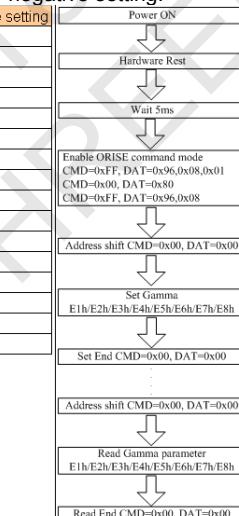
5.3.79. GMCT1.8P (E300h): Gamma Correction Characteristics Setting (1.8 +)

Address	E3h										
Address (SPI/I2C/MDDI)	E300h ~ E311h (0x01 st ~0x12 nd Parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	1	0	0	0	1	1	E3h
1 st Parameter	Write		0	0	G18P1	G18P1	G18P1	G18P1	G18P1	G18P1	05h
2 nd Parameter	Write/Read		0	0	G18P2	G18P2	G18P2	G18P2	G18P2	G18P2	0Bh
3 rd Parameter	Write/Read		0	0	G18P3	G18P3	G18P3	G18P3	G18P3	G18P3	1Ah
4 th Parameter	Write/Read		0	0	0	G18P4	G18P4	G18P4	G18P4	G18P4	15h
5 th Parameter	Write/Read		0	0	0	G18P5	G18P5	G18P5	G18P5	G18P5	0Eh
6 th Parameter	Write/Read		0	0	0	G18P6	G18P6	G18P6	G18P6	G18P6	06h
7 th Parameter	Write/Read		0	0	0	0	G18P7	G18P7	G18P7	G18P7	0Eh
8 th Parameter	Write/Read		0	0	0	0	G18P8	G18P8	G18P8	G18P8	0Bh
9 th Parameter	Write/Read		0	0	0	0	G18P9	G18P9	G18P9	G18P9	0Bh
10 th Parameter	Write/Read		0	0	0	0	G18P10	G18P10	G18P10	G18P10	04h
11 st Parameter	Write/Read		0	0	0	G18P11	G18P11	G18P11	G18P11	G18P11	06h
12 nd Parameter	Write/Read		0	0	0	G18P12	G18P12	G18P12	G18P12	G18P12	14h
13 rd Parameter	Write/Read		0	0	0	G18P13	G18P13	G18P13	G18P13	G18P13	0Ah
14 th Parameter	Write/Read		0	0	G18P14	G18P14	G18P14	G18P14	G18P14	G18P14	10h
15 th Parameter	Write/Read		0	0	G18P15	G18P15	G18P15	G18P15	G18P15	G18P15	22h
16 th Parameter	Write/Read		0	0	G18P16	G18P16	G18P16	G18P16	G18P16	G18P16	17h

Description	- Gamma adjustment for 1.8 positive setting. <table border="1" style="border-collapse: collapse; width: 100%;"> <tr><th colspan="2">Gamma adjustment for 1.8 positive setting</th></tr> <tr><td>G18P1</td><td>+ Level 0</td></tr> <tr><td>G18P2</td><td>+ Level 4</td></tr> <tr><td>G18P3</td><td>+ Level 8</td></tr> <tr><td>G18P4</td><td>+ Level 16</td></tr> <tr><td>G18P5</td><td>+ Level 24</td></tr> <tr><td>G18P6</td><td>+ Level 52</td></tr> <tr><td>G18P7</td><td>+ Level 80</td></tr> <tr><td>G18P8</td><td>+ Level 108</td></tr> <tr><td>G18P9</td><td>+ Level 147</td></tr> <tr><td>G18P10</td><td>+ Level 175</td></tr> <tr><td>G18P11</td><td>+ Level 203</td></tr> <tr><td>G18P12</td><td>+ Level 231</td></tr> <tr><td>G18P13</td><td>+ Level 239</td></tr> <tr><td>G18P14</td><td>+ Level 247</td></tr> <tr><td>G18P15</td><td>+ Level 251</td></tr> <tr><td>G18P16</td><td>+ Level 255</td></tr> </table>		Gamma adjustment for 1.8 positive setting		G18P1	+ Level 0	G18P2	+ Level 4	G18P3	+ Level 8	G18P4	+ Level 16	G18P5	+ Level 24	G18P6	+ Level 52	G18P7	+ Level 80	G18P8	+ Level 108	G18P9	+ Level 147	G18P10	+ Level 175	G18P11	+ Level 203	G18P12	+ Level 231	G18P13	+ Level 239	G18P14	+ Level 247	G18P15	+ Level 251	G18P16	+ Level 255
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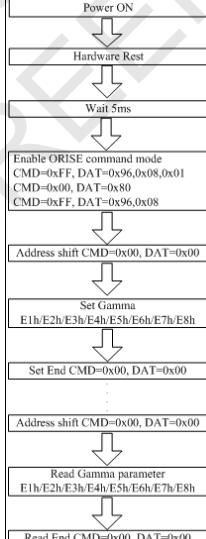
5.3.80. GMCT1.8N (E400h): Gamma Correction Characteristics Setting (1.8 -)

Address	E4h										
Address (SPI/I2C/MDDI)	E400h ~ E40Fh (0x01 st ~0x16 nd Parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	1	0	0	1	0	0	E4h
1 st Parameter	Write/Read		0	0	G18N1	G18N1	G18N1	G18N1	G18N1	G18N1	05h
2 nd Parameter	Write/Read		0	0	G18N2	G18N2	G18N2	G18N2	G18N2	G18N2	0Bh
3 rd Parameter	Write/Read		0	0	G18N3	G18N3	G18N3	G18N3	G18N3	G18N3	1Ah
4 th Parameter	Write/Read		0	0	0	G18N4	G18N4	G18N4	G18N4	G18N4	15h
5 th Parameter	Write/Read		0	0	0	G18N5	G18N5	G18N5	G18N5	G18N5	0Eh
6 th Parameter	Write/Read		0	0	0	G18N6	G18N6	G18N6	G18N6	G18N6	06h
7 th Parameter	Write/Read		0	0	0	0	G18N7	G18N7	G18N7	G18N7	0Eh
8 th Parameter	Write/Read		0	0	0	0	G18N8	G18N8	G18N8	G18N8	0Bh
9 th Parameter	Write/Read		0	0	0	0	G18N9	G18N9	G18N9	G18N9	0Bh
10 th Parameter	Write/Read		0	0	0	0	G18N10	G18N10	G18N10	G18N10	04h
11 st Parameter	Write/Read		0	0	0	G18N11	G18N11	G18N11	G18N11	G18N11	06h
12 nd Parameter	Write/Read		0	0	0	G18N12	G18N12	G18N12	G18N12	G18N12	14h
13 rd Parameter	Write/Read		0	0	0	G18N13	G18N13	G18N13	G18N13	G18N13	0Ah
14 th Parameter	Write/Read		0	0	G18N14	G18N14	G18N14	G18N14	G18N14	G18N14	10h
15 th Parameter	Write/Read		0	0	G18N15	G18N15	G18N15	G18N15	G18N15	G18N15	22h
16 th Parameter	Write/Read		0	0	G18N16	G18N16	G18N16	G18N16	G18N16	G18N16	17h

Description	- Gamma adjustment for 1.8 negative setting. Gamma adjustment for 1.8 negative setting G18N1 - Level 0 G18N2 - Level 4 G18N3 - Level 8 G18N4 - Level 16 G18N5 - Level 24 G18N6 - Level 52 G18N7 - Level 80 G18N8 - Level 108 G18N9 - Level 147 G18N10 - Level 175 G18N11 - Level 203 G18N12 - Level 231 G18N13 - Level 239 G18N14 - Level 247 G18N15 - Level 251 G18N16 - Level 255					
	- Read and Write, Only access when Orise mode enable.					
	- Gamma value is readable only after the register has been written or the OTP has been programmed.					
	<table border="1"> <tr> <td>Status</td> <td>Default Value</td> </tr> <tr> <td>OTP un-programmed</td> <td>Set as default value</td> </tr> <tr> <td>OTP Programmed</td> <td>Set as OTP value</td> </tr> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed
Status	Default Value					
OTP un-programmed	Set as default value					
OTP Programmed	Set as OTP value					

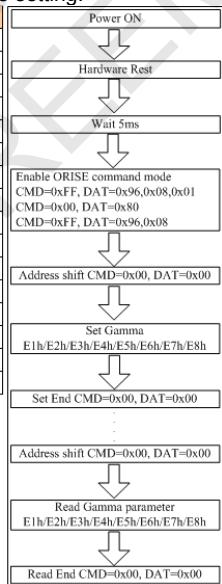
5.3.81. GMCT2.5P (E500h): Gamma Correction Characteristics Setting (2.5 +)

Address	E5h										
Address (SPI/I2C/MDDI)	E500h ~ E50Fh (0x01 st ~0x16 nd Parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	1	0	0	1	0	1	E5h
1 st Parameter	Write/Read		0	0	G25P1	G25P1	G25P1	G25P1	G25P1	G25P1	05h
2 nd Parameter	Write/Read		0	0	G25P2	G25P2	G25P2	G25P2	G25P2	G25P2	0Bh
3 rd Parameter	Write/Read		0	0	G25P3	G25P3	G25P3	G25P3	G25P3	G25P3	1Ah
4 th Parameter	Write/Read		0	0	0	G25P4	G25P4	G25P4	G25P4	G25P4	15h
5 th Parameter	Write/Read		0	0	0	G25P5	G25P5	G25P5	G25P5	G25P5	0Eh
6 th Parameter	Write/Read		0	0	0	G25P6	G25P6	G25P6	G25P6	G25P6	06h
7 th Parameter	Write/Read		0	0	0	0	G25P7	G25P7	G25P7	G25P7	0Eh
8 th Parameter	Write/Read		0	0	0	0	G25P8	G25P8	G25P8	G25P8	0Bh
9 th Parameter	Write/Read		0	0	0	0	G25P9	G25P9	G25P9	G25P9	0Bh
10 th Parameter	Write/Read		0	0	0	0	G25P10	G25P10	G25P10	G25P10	04h
11 st Parameter	Write/Read		0	0	0	G25P11	G25P11	G25P11	G25P11	G25P11	06h
12 nd Parameter	Write/Read		0	0	0	G25P12	G25P12	G25P12	G25P12	G25P12	14h
13 rd Parameter	Write/Read		0	0	0	G25P13	G25P13	G25P13	G25P13	G25P13	0Ah
14 th Parameter	Write/Read		0	0	G25P14	G25P14	G25P14	G25P14	G25P14	G25P14	10h
15 th Parameter	Write/Read		0	0	G25P15	G25P15	G25P15	G25P15	G25P15	G25P15	22h
16 th Parameter	Write/Read		0	0	G25P16	G25P16	G25P16	G25P16	G25P16	G25P16	17h

Description	- Gamma adjustment for 2.5 positive setting. Gamma adjustment for 2.5 positive setting						
	- Read and Write, Only access when Orise mode enable.						
	- Gamma value is readable only after the register has been written or the OTP has been programmed.						
		<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>OTP un-programmed</td><td>Set as default value</td></tr> <tr> <td>OTP Programmed</td><td>Set as OTP value</td></tr> </tbody> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed
Status	Default Value						
OTP un-programmed	Set as default value						
OTP Programmed	Set as OTP value						

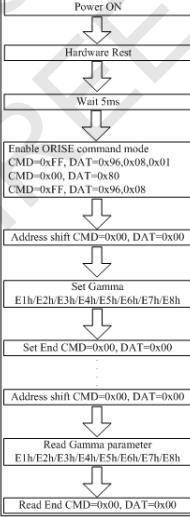
5.3.82. GMCT2.5N (E600h): Gamma Correction Characteristics Setting (2.5 -)

Address	E6h										
Address (SPI/I2C/MDDI)	E600h ~ E60Fh (0x01 st ~0x16 nd Parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	1	0	0	1	1	0	E6h
1 st Parameter	Write/Read		0	0	G25N1	G25N1	G25N1	G25N1	G25N1	G25N1	05h
2 nd Parameter	Write/Read		0	0	G25N2	G25N2	G25N2	G25N2	G25N2	G25N2	0Bh
3 rd Parameter	Write/Read		0	0	G25N3	G25N3	G25N3	G25N3	G25N3	G25N3	1Ah
4 th Parameter	Write/Read		0	0	0	G25N4	G25N4	G25N4	G25N4	G25N4	15h
5 th Parameter	Write/Read		0	0	0	G25N5	G25N5	G25N5	G25N5	G25N5	0Eh
6 th Parameter	Write/Read		0	0	0	G25N6	G25N6	G25N6	G25N6	G25N6	06h
7 th Parameter	Write/Read		0	0	0	0	G25N7	G25N7	G25N7	G25N7	0Eh
8 th Parameter	Write/Read		0	0	0	0	G25N8	G25N8	G25N8	G25N8	0Bh
9 th Parameter	Write/Read		0	0	0	0	G25N9	G25N9	G25N9	G25N9	0Bh
10 th Parameter	Write/Read		0	0	0	0	G25N10	G25N10	G25N10	G25N10	04h
11 st Parameter	Write/Read		0	0	0	G25N11	G25N11	G25N11	G25N11	G25N11	06h
12 nd Parameter	Write/Read		0	0	0	G25N12	G25N12	G25N12	G25N12	G25N12	14h
13 rd Parameter	Write/Read		0	0	0	G25N13	G25N13	G25N13	G25N13	G25N13	0Ah
14 th Parameter	Write/Read		0	0	G25N14	G25N14	G25N14	G25N14	G25N14	G25N14	10h
15 th Parameter	Write/Read		0	0	G25N15	G25N15	G25N15	G25N15	G25N15	G25N15	22h
16 th Parameter	Write/Read		0	0	G25N16	G25N16	G25N16	G25N16	G25N16	G25N16	17h

Description	- Gamma adjustment for 2.5 negative setting. <table border="1"><tr><td>G25N1</td><td>- Level 0</td></tr><tr><td>G25N2</td><td>- Level 4</td></tr><tr><td>G25N3</td><td>- Level 8</td></tr><tr><td>G25N4</td><td>- Level 16</td></tr><tr><td>G25N5</td><td>- Level 24</td></tr><tr><td>G25N6</td><td>- Level 52</td></tr><tr><td>G25N7</td><td>- Level 80</td></tr><tr><td>G25N8</td><td>- Level 108</td></tr><tr><td>G25N9</td><td>- Level 147</td></tr><tr><td>G25N10</td><td>- Level 175</td></tr><tr><td>G25N11</td><td>- Level 203</td></tr><tr><td>G25N12</td><td>- Level 231</td></tr><tr><td>G25N13</td><td>- Level 239</td></tr><tr><td>G25N14</td><td>- Level 247</td></tr><tr><td>G25N15</td><td>- Level 251</td></tr><tr><td>G25N16</td><td>- Level 255</td></tr></table>	G25N1	- Level 0	G25N2	- Level 4	G25N3	- Level 8	G25N4	- Level 16	G25N5	- Level 24	G25N6	- Level 52	G25N7	- Level 80	G25N8	- Level 108	G25N9	- Level 147	G25N10	- Level 175	G25N11	- Level 203	G25N12	- Level 231	G25N13	- Level 239	G25N14	- Level 247	G25N15	- Level 251	G25N16	- Level 255	
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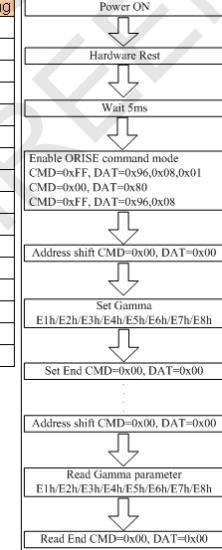
5.3.83. GMCT1.0N (E700h): Gamma Correction Characteristics Setting (1.0 +)

Address	E7h										
Address (SPI/I2C/MDDI)	E700h ~ E70Fh (0x01 st ~0x16 nd Parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	1	0	0	1	1	1	E7h
1 st Parameter	Write/Read		0	0	G10P1	G10P1	G10P1	G10P1	G10P1	G10P1	05h
2 nd Parameter	Write/Read		0	0	G10P2	G10P2	G10P2	G10P2	G10P2	G10P2	0Bh
3 rd Parameter	Write/Read		0	0	G10P3	G10P3	G10P3	G10P3	G10P3	G10P3	1Ah
4 th Parameter	Write/Read		0	0	0	G10P4	G10P4	G10P4	G10P4	G10P4	15h
5 th Parameter	Write/Read		0	0	0	G10P5	G10P5	G10P5	G10P5	G10P5	0Eh
6 th Parameter	Write/Read		0	0	0	G10P6	G10P6	G10P6	G10P6	G10P6	06h
7 th Parameter	Write/Read		0	0	0	0	G10P7	G10P7	G10P7	G10P7	0Eh
8 th Parameter	Write/Read		0	0	0	0	G10P8	G10P8	G10P8	G10P8	0Bh
9 th Parameter	Write/Read		0	0	0	0	G10P9	G10P9	G10P9	G10P9	0Bh
10 th Parameter	Write/Read		0	0	0	0	G10P10	G10P10	G10P10	G10P10	04h
11 st Parameter	Write/Read		0	0	0	G10P11	G10P11	G10P11	G10P11	G10P11	06h
12 nd Parameter	Write/Read		0	0	0	G10P12	G10P12	G10P12	G10P12	G10P12	14h
13 rd Parameter	Write/Read		0	0	0	G10P13	G10P13	G10P13	G10P13	G10P13	0Ah
14 th Parameter	Write/Read		0	0	G10P14	G10P14	G10P14	G10P14	G10P14	G10P14	10h
15 th Parameter	Write/Read		0	0	G10P15	G10P15	G10P15	G10P15	G10P15	G10P15	22h
16 th Parameter	Write/Read		0	0	G10P16	G10P16	G10P16	G10P16	G10P16	G10P16	17h

Description	- Gamma adjustment for 1.0 positive setting. Gamma adjustment for 1.0 positive setting G10P1 + Level 0 G10P2 + Level 4 G10P3 + Level 8 G10P4 + Level 16 G10P5 + Level 24 G10P6 + Level 52 G10P7 + Level 80 G10P8 + Level 108 G10P9 + Level 147 G10P10 + Level 175 G10P11 + Level 203 G10P12 + Level 231 G10P13 + Level 239 G10P14 + Level 247 G10P15 + Level 251 G10P16 + Level 255					
	- Read and Write, Only access when Orise mode enable.					
	- Gamma value is readable only after the register has been written or the OTP has been programmed.					
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Status	Default Value					
OTP un-programmed	Set as default value					
OTP Programmed	Set as OTP value					

5.3.84. GMCT1.0N (E800h): Gamma Correction Characteristics Setting (1.0 -)

Address	E8h										
Address (SPI/I2C/MDDI)	E800h ~ E80Fh (0x01 st ~0x16 nd Parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	1	0	1	0	0	0	E8h
1 st Parameter	Write/Read		0	0	G10N1	G10N1	G10N1	G10N1	G10N1	G10N1	05h
2 nd Parameter	Write/Read		0	0	G10N2	G10N2	G10N2	G10N2	G10N2	G10N2	0Bh
3 rd Parameter	Write/Read		0	0	G10N3	G10N3	G10N3	G10N3	G10N3	G10N3	1Ah
4 th Parameter	Write/Read		0	0	0	G10N4	G10N4	G10N4	G10N4	G10N4	15h
5 th Parameter	Write/Read		0	0	0	G10N5	G10N5	G10N5	G10N5	G10N5	0Eh
6 th Parameter	Write/Read		0	0	0	G10N6	G10N6	G10N6	G10N6	G10N6	06h
7 th Parameter	Write/Read		0	0	0	0	G10N7	G10N7	G10N7	G10N7	0Eh
8 th Parameter	Write/Read		0	0	0	0	G10N8	G10N8	G10N8	G10N8	0Bh
9 th Parameter	Write/Read		0	0	0	0	G10N9	G10N9	G10N9	G10N9	0Bh
10 th Parameter	Write/Read		0	0	0	0	G10N10	G10N10	G10N10	G10N10	04h
11 st Parameter	Write/Read		0	0	0	G10N11	G10N11	G10N11	G10N11	G10N11	06h
12 nd Parameter	Write/Read		0	0	0	G10N12	G10N12	G10N12	G10N12	G10N12	14h
13 rd Parameter	Write/Read		0	0	0	G10N13	G10N13	G10N13	G10N13	G10N13	0Ah
14 th Parameter	Write/Read		0	0	G10N14	G10N14	G10N14	G10N14	G10N14	G10N14	10h
15 th Parameter	Write/Read		0	0	G10N15	G10N15	G10N15	G10N15	G10N15	G10N15	22h
16 th Parameter	Write/Read		0	0	G10N16	G10N16	G10N16	G10N16	G10N16	G10N16	17h

Description	- Gamma adjustment for 1.0 negative setting. Gamma adjustment for 1.0 negative setting G10N1 - Level 0 G10N2 - Level 4 G10N3 - Level 8 G10N4 - Level 16 G10N5 - Level 24 G10N6 - Level 52 G10N7 - Level 80 G10N8 - Level 108 G10N9 - Level 147 G10N10 - Level 175 G10N11 - Level 203 G10N12 - Level 231 G10N13 - Level 239 G10N14 - Level 247 G10N15 - Level 251 G10N16 - Level 255	 <pre> graph TD PowerON[Power ON] --> HardwareRest[Hardware Rest] HardwareRest --> Wait5ms[Wait 5ms] Wait5ms --> EnableMode[Enable ORISE command mode CMD=0xFF, DAT=0x96,0x08,0x01 CMD=0x00, DAT=0x80 CMD=0xFF, DAT=0x96,0x08] EnableMode --> AddressShiftCMD[Address shift CMD=0x00, DAT=0x00] AddressShiftCMD --> SetGamma[Set Gamma E1h/E2h/E3h/E4h/E5h/E6h/E7h/E8h] SetGamma --> SetEndCMD[Set End CMD=0x00, DAT=0x00] SetEndCMD -.-> AddressShiftCMD AddressShiftCMD --> ReadGammaParameter[Read Gamma parameter E1h/E2h/E3h/E4h/E5h/E6h/E7h/E8h] ReadGammaParameter --> ReadEndCMD[Read End CMD=0x00, DAT=0x00] </pre>				
	- Read and Write, Only access when Orise mode enable.					
	- Gamma value is readable only after the register has been written or the OTP has been programmed.					
	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>OTP un-programmed</td> <td>Set as default value</td> </tr> <tr> <td>OTP Programmed</td> <td>Set as OTP value</td> </tr> </tbody> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed
Status	Default Value					
OTP un-programmed	Set as default value					
OTP Programmed	Set as OTP value					

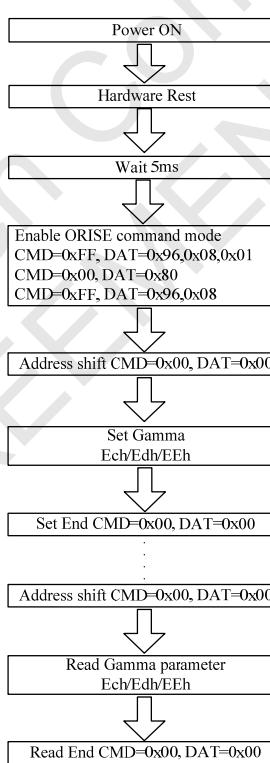
5.3.85. NVMIN (EB00h): NV Memory Write Mode

Address	EBh										
Address (SPI/I2C/MDDI)	EB00h(0x01 st Parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	1	0	1	0	1	1	EBh
Parameter	Write		0	0	0	0	0	0	0	NVM_P GM	00h

Description	-NVM_PGM: NVM programming Function	
	NVM_PGM	NVM programming Function
	0	Disable
	1	Enable
-		
Restriction	Only access when Orise mode enable.	
Default	Status	Default Value
	OTP un-programmed	Set as default value
	OTP Programmed	Set as default value

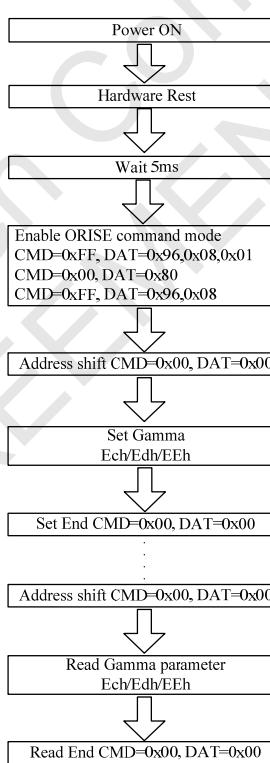
5.3.86. DGAMR (EC00h): Digital Gamma Correction Characteristics Setting (Red):

Address	ECh										
Address (SPI/I2C/MDDI)	EC00h ~ EC21h (0x01 st ~0x22 th Parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	1	0	1	1	0	0	ECh
1 st Parameter	Write/Read		DGR2	DGR2	DGR2	DGR2	DGR1	DGR1	DGR1	DGR1	40h
2 nd Parameter	Write/Read		DGR4	DGR4	DGR4	DGR4	DGR3	DGR3	DGR3	DGR3	44h
3 rd Parameter	Write/Read		DGR6	DGR6	DGR6	DGR6	DGR5	DGR5	DGR5	DGR5	44h
:	Write/Read		:	:							
31 th Parameter	Write/Read		DGR62	DGR62	DGR62	DGR62	DGR61	DGR61	DGR61	DGR61	44h
32 th Parameter	Write/Read		DGR64	DGR64	DGR64	DGR64	DGR63	DGR63	DGR63	DGR63	44h
33 th Parameter	Write/Read		0	0	0	0	DGR65	DGR65	DGR65	DGR65	44h
34 th Parameter	Write/Read		0	0	0	0	0	0	0	0	00h

Description	- Command ECh totally has 34 parameters, these parameters are settings for Digital gamma Red curve - Gamma adjustment for Red setting.						
	 <pre> graph TD A[Power ON] --> B[Hardware Rest] B --> C[Wait 5ms] C --> D["Enable ORISE command mode CMD=0xFF, DAT=0x96,0x08,0x01 CMD=0x00, DAT=0x80 CMD=0xFF, DAT=0x96,0x08"] D --> E["Address shift CMD=0x00, DAT=0x00"] E --> F["Set Gamma Ech/Edh/EEh"] F --> G["Set End CMD=0x00, DAT=0x00"] G -.-> H["Address shift CMD=0x00, DAT=0x00"] H --> I["Read Gamma parameter Ech/Edh/EEh"] I --> J["Read End CMD=0x00, DAT=0x00"] </pre>						
Restriction	<ul style="list-style-type: none"> Read and Write, Only access when Orise mode enable. Gamma value is readable only after the register has been written or the OTP has been programmed. 						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>OTP un-programmed</td> <td>Set as default value</td> </tr> <tr> <td>OTP Programmed</td> <td>Set as OTP value</td> </tr> </tbody> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value
Status	Default Value						
OTP un-programmed	Set as default value						
OTP Programmed	Set as OTP value						

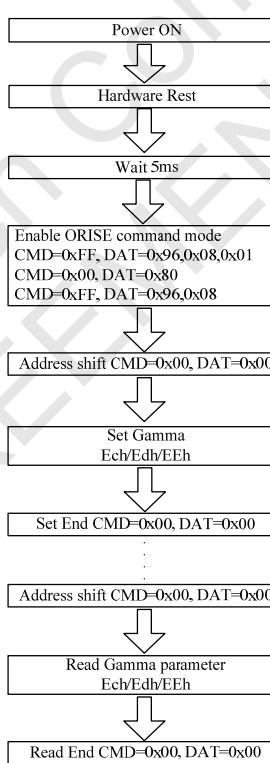
5.3.87. DGAMR (ED00h): Digital Gamma Correction Characteristics Setting (Green):

Address	EDh										
Address (SPI/I2C/MDDI)	ED00h ~ ED21h (0x01 st ~0x22 th Parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	1	0	1	1	0	1	EDh
1 st Parameter	Write/Read		DGG2	DGG2	DGG2	DGG2	DGG1	DGG1	DGG1	DGG1	40h
2 nd Parameter	Write/Read		DGG4	DGG4	DGG4	DGG4	DGG3	DGG3	DGG3	DGG3	44h
3 rd Parameter	Write/Read		DGG6	DGG6	DGG6	DGG6	DGG5	DGG5	DGG5	DGG5	44h
:	Write/Read		:	:							
31 th Parameter	Write/Read		DGG62	DGG62	DGG62	DGG62	DGG29	DGG16	DGG61	DGG61	44h
32 th Parameter	Write/Read		DGG64	DGG64	DGG64	DGG64	DGG63	DGG63	DGG63	DGG63	44h
33 th Parameter	Write/Read		0	0	0	0	DGG65	DGG65	DGG65	DGG65	44h
34 th Parameter	Write/Read		0	0	0	0	0	0	0	0	00h

Description	- Command EDh totally has 34 parameters, these parameters are settings for Digital gamma Green curve - Gamma adjustment for Green setting.						
	 <pre> graph TD A[Power ON] --> B[Hardware Rest] B --> C[Wait 5ms] C --> D["Enable ORISE command mode CMD=0xFF, DAT=0x96,0x08,0x01 CMD=0x00, DAT=0x80 CMD=0xFF, DAT=0x96,0x08"] D --> E["Address shift CMD=0x00, DAT=0x00"] E --> F["Set Gamma Ech/Edh/EEh"] F --> G["Set End CMD=0x00, DAT=0x00"] G -.-> H["Address shift CMD=0x00, DAT=0x00"] H --> I["Read Gamma parameter Ech/Edh/EEh"] I --> J["Read End CMD=0x00, DAT=0x00"] </pre>						
Restriction	<ul style="list-style-type: none"> Read and Write, Only access when Orise mode enable. Gamma value is readable only after the register has been written or the OTP has been programmed. 						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>OTP un-programmed</td> <td>Set as default value</td> </tr> <tr> <td>OTP Programmed</td> <td>Set as OTP value</td> </tr> </tbody> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value
Status	Default Value						
OTP un-programmed	Set as default value						
OTP Programmed	Set as OTP value						

5.3.88. DGAMB (EE00h): Digital Gamma Correction Characteristics Setting (Blue)

Address	EEh										
Address (SPI/I2C/MDDI)	EE00h ~ EE21h (0x01 st ~ 0x22 th Parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	1	0	1	1	1	0	EEh
1 st Parameter	Write/Read		DGB2	DGB2	DGB2	DGB2	DGB1	DGB1	DGB1	DGB1	40h
2 nd Parameter	Write/Read		DGB4	DGB4	DGB4	DGB4	DGB3	DGB3	DGB3	DGB3	44h
3 rd Parameter	Write/Read		DGB6	DGB6	DGB6	DGB6	DGB5	DGB5	DGB5	DGB5	44h
:	Write/Read		:	:							
31 th Parameter	31 st Parameter		DGB62	DGB62	DGB62	DGB62	DGB61	DGB61	DGB61	DGB61	44h
32 th Parameter	32 nd Parameter		DGB64	DGB64	DGB64	DGB64	DGB63	DGB63	DGB63	DGB63	44h
33 th Parameter	33 rd Parameter		0	0	0	0	DGB65	DGB65	DGB65	DGB65	44h
34 th Parameter	Write/Read		0	0	0	0	0	0	0	0	00h

Description	- Command EEh totally has 34 parameters, these parameters are settings for Digital gamma Blue curve						
	- Gamma adjustment for Blue setting.						
							
Restriction	<ul style="list-style-type: none"> - Read and Write, Only access when Orise mode enable. - Gamma value is readable only after the register has been written or the OTP has been programmed. 						
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>OTP un-programmed</td><td>Set as default value</td></tr> <tr> <td>OTP Programmed</td><td>Set as OTP value</td></tr> </tbody> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as OTP value
Status	Default Value						
OTP un-programmed	Set as default value						
OTP Programmed	Set as OTP value						

5.3.89. Command 2 Flag (F101h): Read Program 4 time OTP Flag

Address	F1h										
Address (SPI/I2C/MDDI)	F101h ~ F103h(0x02 nd ~ 0x04 th Parameter)										
Inst. / Para.	Write/Read	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Default
Instruction	Write	00h	1	1	1	1	0	0	0	1	F1h
2 nd Parameter	Read		{rd0_otpena[3:0], rd1_otpena[3:0]}								00h
3 rd parameter	Read		{rd2_otpena[3:0], rd8_otpena[3:0]}								00h
4 th parameter	Read		{rd9_otpena[3:0], 4'b0000}								00h

Description	F1 is read only command, it reads programmed flag by OTP. <ul style="list-style-type: none"> - rd0_otpena[3:0]: Command D0h (ID1) program flag (0:never program, 1:program 1 time, 3:program 2 time, 7:program 3 time, F:program 4 time) - rd1_otpena[3:0]: Command D1h (ID2, ID3) program flag (0:never program, 1:program 1 time, 3:program 2 time, 7:program 3 time, F:program 4 time) - rd2_otpena[3:0]: Command D2h (DDB1, DDB2, DDB3 for A1h/A8h command read ID) program flag (0:never program, 1:program 1 time, 3:program 2 time, 7:program 3 time, F:program 4 time) - rd8_otpena[3:0]: Command D8h (gvdd, ngvdd) program flag (0:never program, 1:program 1 time, 3:program 2 time, 7:program 3 time, F:program 4 time) - rd9_otpena[3:0]: Command D9h (vcomdc) program flag (0:never program, 1:program 1 time, 3:program 2 time, 7:program 3 time, F:program 4 time) 						
Restriction	Only access when Orise mode enable.						
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">OTP un-programmed</td> <td style="text-align: center; padding: 2px;">Set as default value</td> </tr> <tr> <td style="text-align: center; padding: 2px;">OTP Programmed</td> <td style="text-align: center; padding: 2px;">Set as default value</td> </tr> </tbody> </table>	Status	Default Value	OTP un-programmed	Set as default value	OTP Programmed	Set as default value
Status	Default Value						
OTP un-programmed	Set as default value						
OTP Programmed	Set as default value						

6. FUNCTION DESCRIPTIONS

6.1. Interface Type Selection

The MPU interfaces of OTM9608A support high speed serial interfaces, including MIPI, MDDI, and 8/16/24-bit 80-system Interface, RGB 24 bit Interface, which can be set by the IM[2:0] pins. The MPU interface can set instructions and access RAM. Table 6-1 depicts the interface corresponding to IM[2:0] pins .

Table 6-1

External Pad Set				Interface format
IM3	IM2	IM1	IM0	
0	0	0	0	CPU 8bit
0	0	0	1	CPU 16bit
0	0	1	0	CPU 24bit
0	0	1	1	RGB + Serial Interface (SCL rising edge trigger)
1	0	1	1	RGB + Serial Interface (SCL falling edge trigger)
0	1	0	0	MIPI-DSI
0	1	0	1	MDDI + SPI (SCL rising edge trigger)
0	1	1	0	MDDI + SPI (SCL falling edge trigger)
1	1	1	0	MDDI + I2C
0	1	1	1	RGB + I2C

6.2. MIPI-DSI Interface

6.2.1. General description

The communication can be separated 2 different levels between the MCU and the display module:

- Interface Level : Low level communication
- Packet level : High level communication

6.2.2. Interface level communication

6.2.2.1. General

The display module uses data and clock lane differential pairs for DSI . Both clock lane and data lane0 can be driven Low Power (LP) or High Speed (HS) mode. Data lane1 and Data lane2 can be driven High Speed mode only.

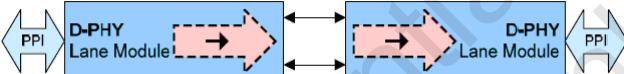
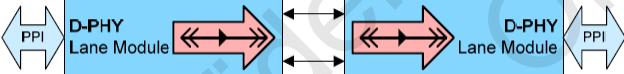
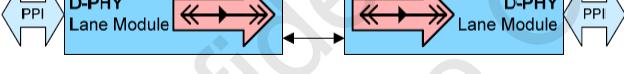
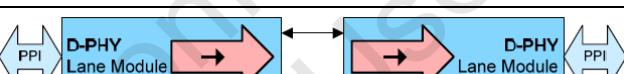
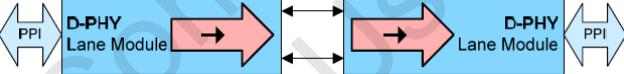
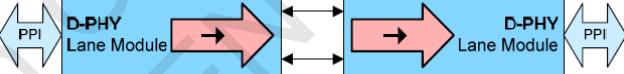
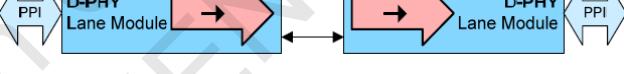
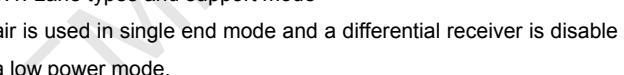
	Lane support mode	MPU(Host)	OTM9608A(Slave)
Clock Lane	Unidirectional lane ★High-Speed Clock only ★Simplified Escape Mode (ULPS Only)		
Data lane0	Bi-directional lane ★Forward high-speed only ★Bi-directional Escape Mode ★Bi-direction LPDT		
Data lane1	Unidirectional lane ★Forward high-speed only ★Simplified Escape Mode (ULPS Only)		
Data lane2	Unidirectional lane ★Forward high-speed only ★Simplified Escape Mode (ULPS Only)		

Table 6.2.2.1.1. Lane types and support mode

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low-Power (LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Table 6.2.2.1.2. High Speed and Low-Power Lane Pair State Descriptions

6.2.2.2. DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM LP-11), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode(LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

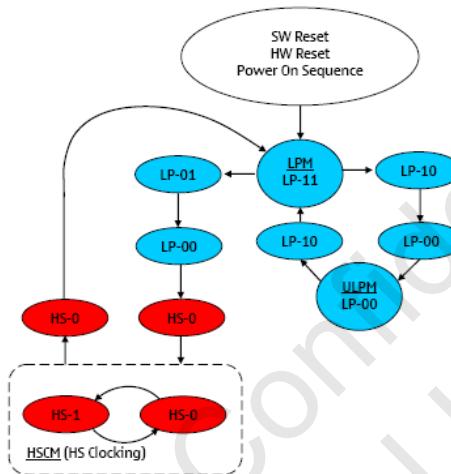


Figure 6.2.2.2.1. Clock Lanes Power Modes

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.
2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

- 1) After SW Reset, HW Reset or Power On Sequence =>LP-11
- 2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.

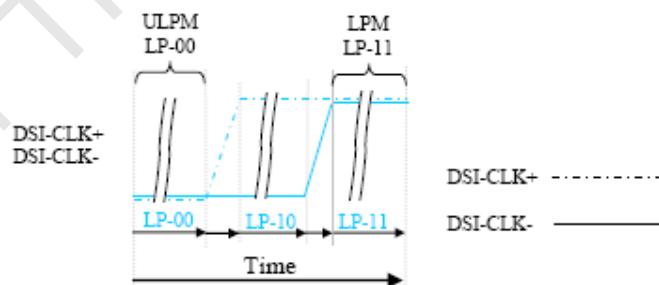


Figure 6.2.2.2.2. From ULPM to LPM

- 3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence is illustrated below.

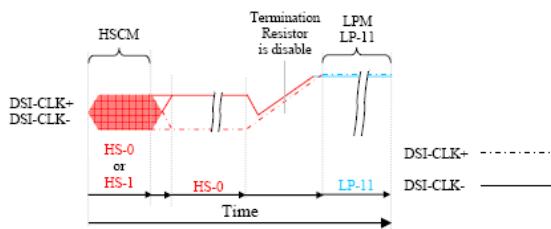


Figure 6.2.2.2.3. From HSCM to LPM

All three mode changes are illustrated a flow chart below.

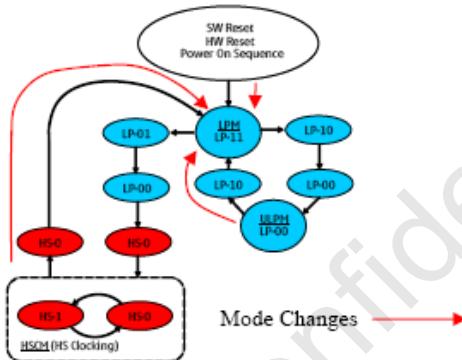


Figure 6.2.2.2.4. All three mode changes to LPM

Ultra Low Power Mode (ULPM)

DSI-CLK+- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

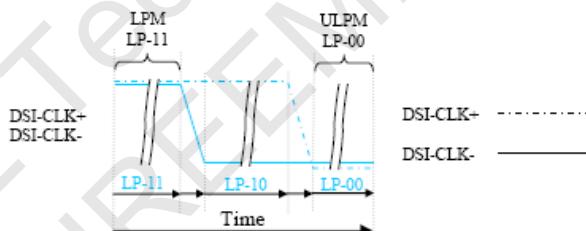


Figure 6.2.2.2.5. From LPM to ULPM

The mode change is also illustrated below:

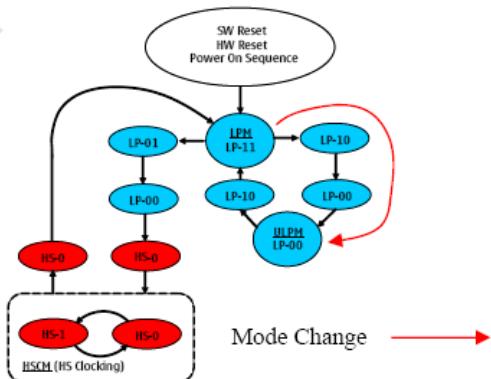


Figure 6.2.2.2.6. The mode change from LPM to ULPM

High-speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

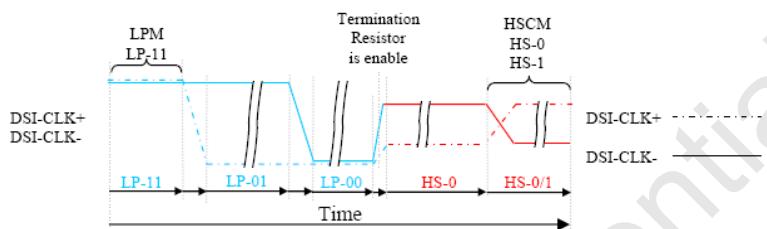


Figure 6.2.2.2.7. From LPM to HSCM

The mode change is also illustrated below:

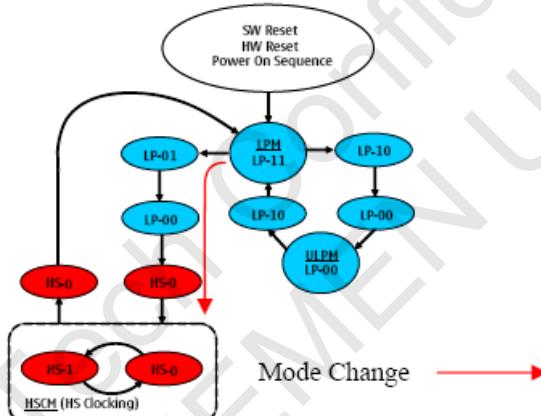


Figure 6.2.2.2.8. Mode change from LPM to HSCM

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0

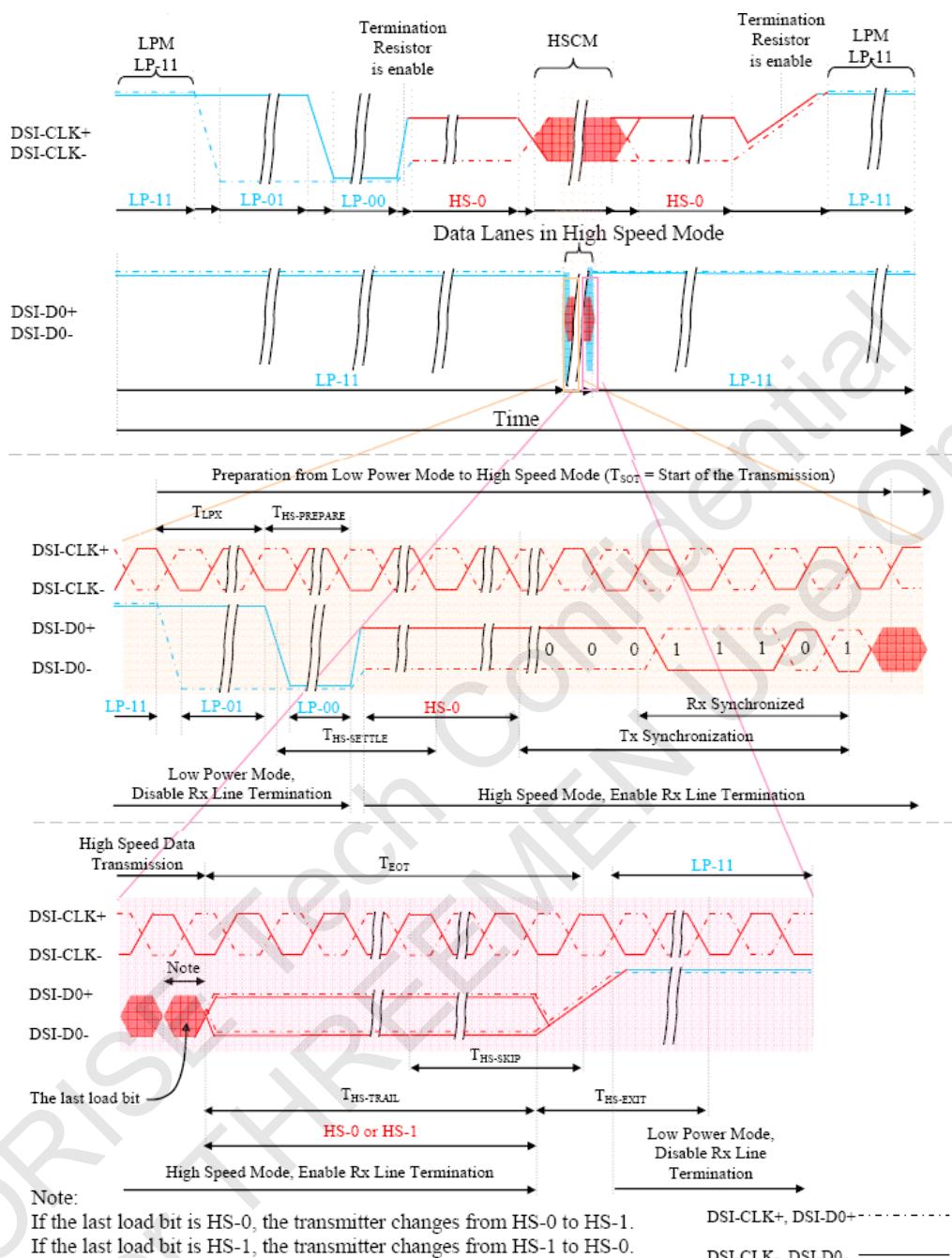


Figure 6.2.2.9. High speed clock burst

6.2.3. DSI Data lanes

6.2.3.1. General

DSI-Dn+/- Data Lanes can be driven in different modes which are:

- Escape Mode (only support DSI_D0 data lane pair)
- High-Speed Data Transmission (support all data lane pairs)
- Bus Turnaround Request (only support DSI_D0 data lane pair)

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00	LP-00 =>LP-10 =>LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 =>LP-01 =>LP-00 =>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11 =>LP-10 =>LP-00 =>LP-10 =>LP-00	High-Z, Note

Table 6.2.3.1.1. Entering and leaving sequences

6.2.3.2. Escape modes

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Escape mode operation shall be supported in the Forward direction and Reverse direction.

The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command , which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit.
- A payload stream if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

For Data Lane0, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action.

All currently available Escape mode commands and actions are list below.

- Send or receive "Low-Power Data Transmission" (LPDT)
- Drive data lanes to "Ultra-Low Power State" (ULPS)
- Indicate "Remote Application Reset" (RAR), which is resetting the display module (same as S/W Reset function)
- Indicate "Tearing Effect" (TEE), which is used for a TE line event from the display module to the MCU,
- Indicate "Acknowledge" (ACK), which is used for a non-error event from the display module to the MCU.

The Stop state shall be used to exit Escape mode and cannot occur during Escape mode operation because of the Spaced-One-Hot encoding. Stop state immediately returns the Lane to Control mode. If the entry command doesn't match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state.

For Data Lane1 and 2, only support ULPS Escape mode commands.

- Drive data lanes to "Ultra-Low Power State" (ULPS)

The basic construction is illustrated below:

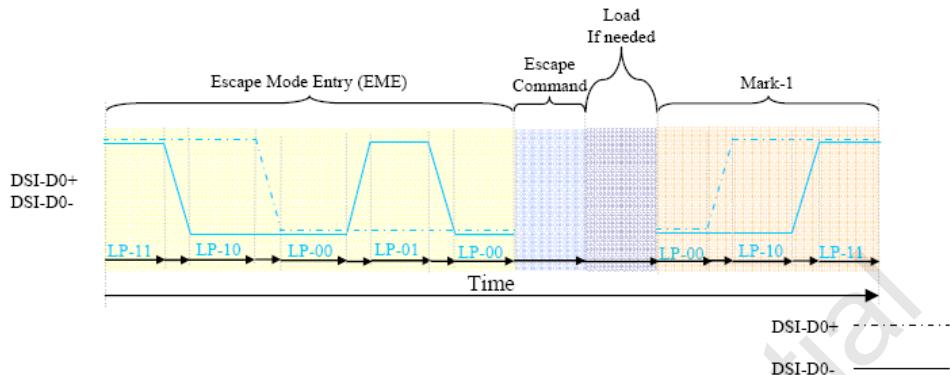


Figure 6.2.3.2.1. General Escape mode sequence

The number of the different Escape Commands is eight. These eight different Escape Commands can be divided 2 different groups: Mode or Trigger.

Escape command groups are defined below.

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit => Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001bin
Ultra-Low Power Mode	Mode	0001 1110bin
Remote Application Reset	Trigger	0110 0010 bin
Tearing Effect	Trigger	0101 1101 bin
Acknowledge	Trigger	0010 0001 bin

Table 6.2.3.2.1 Escape commands

The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode.

The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Payload (Data):
 - One or more bytes
 - Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

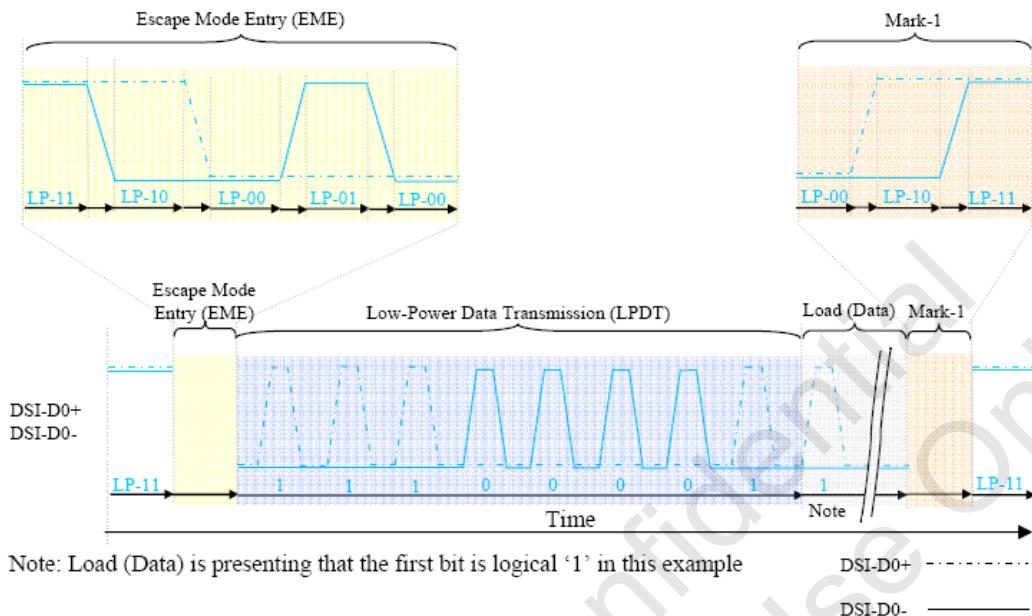


Figure 6.2.3.2.2. Low-power data transmission

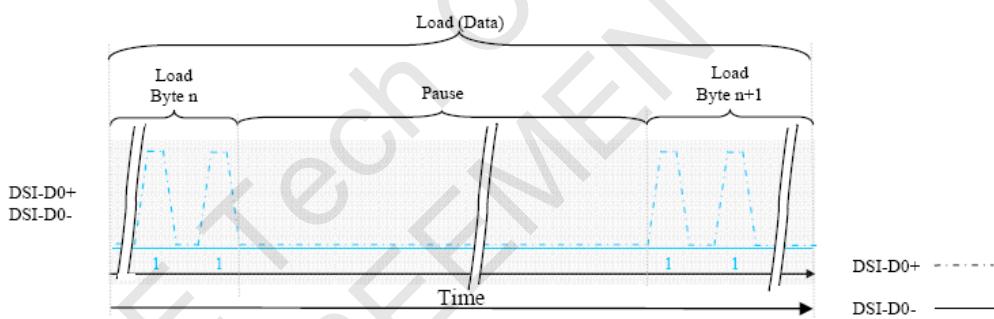


Figure 6.2.3.2.3. Pause (example)

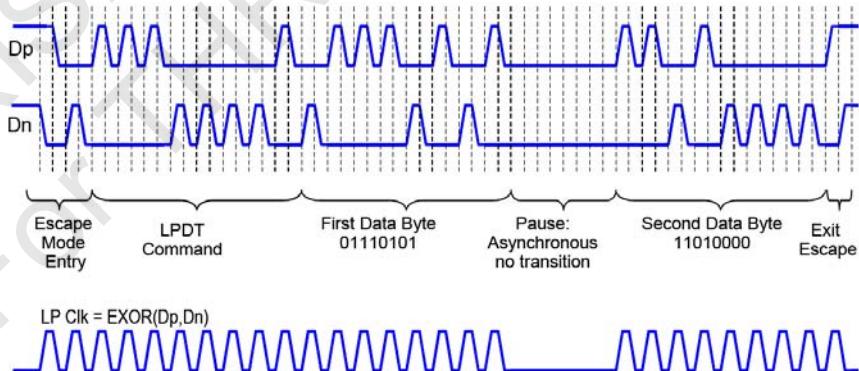


Figure 6.2.3.2.4. Two Data Byte Low-Power Data Transmission Example

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

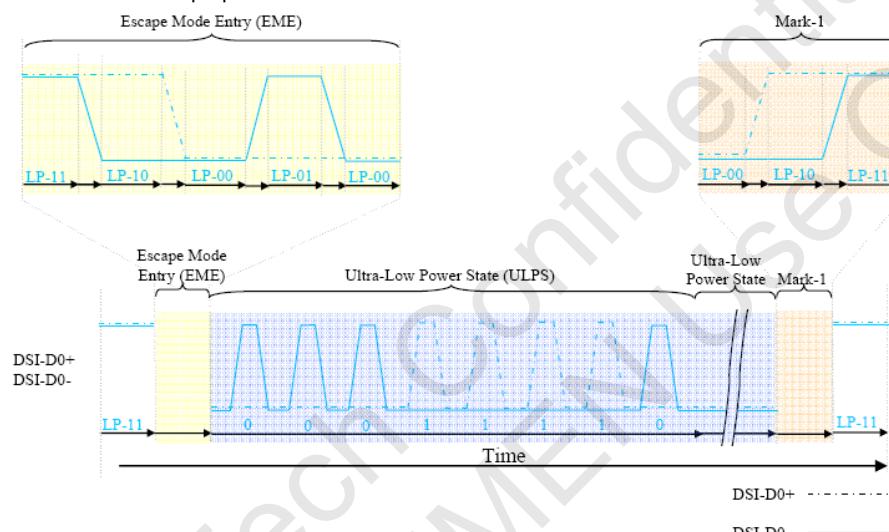


Figure 6.2.3.2.5. Ultra-low power state (ULPS)

Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reseted in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset is using a following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

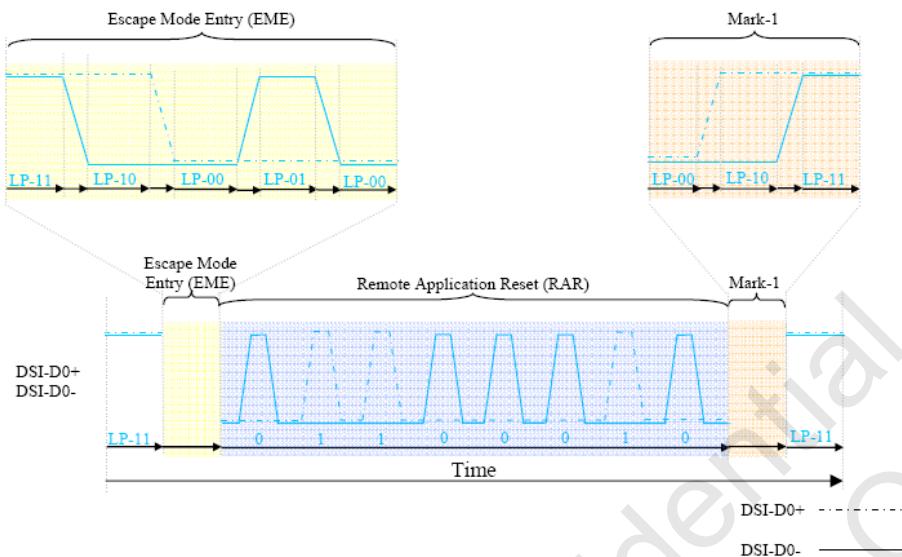


Figure 6.2.3.2.6. Remote Application Reset (RAR)

Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

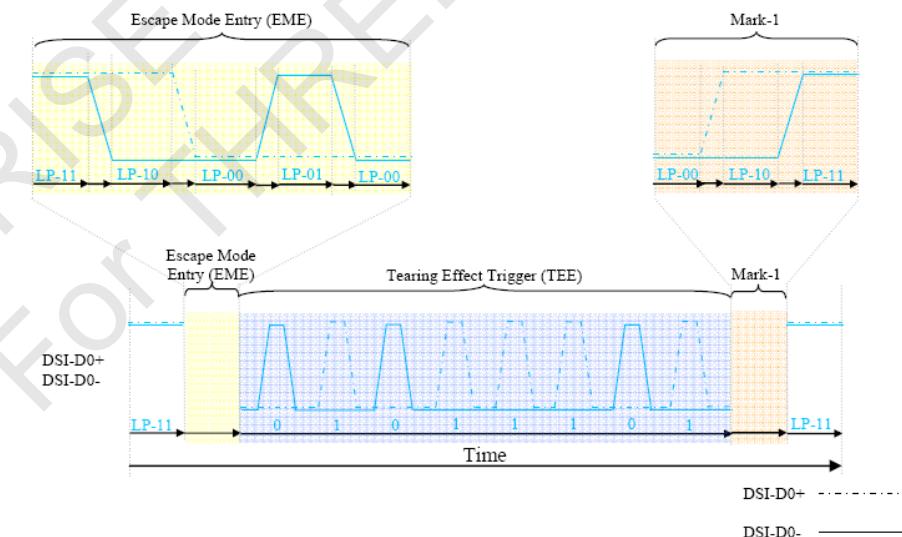


Figure 6.2.3.2.7. Tearing effect (TEE)

Acknowledgement (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

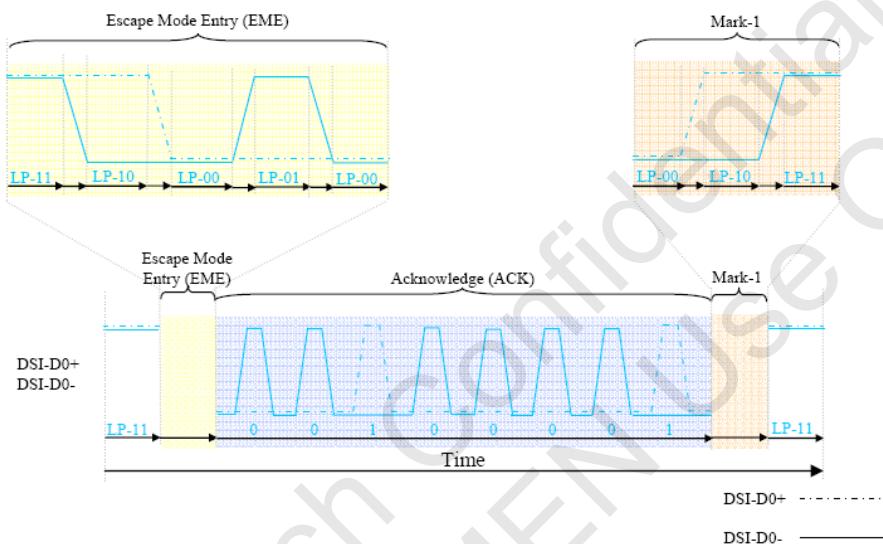


Figure 6.2.3.2.8. Acknowledgement (ACK)

6.2.3.3. High-Speed Data Transmission (HSDT)

Entering High-Speed Data Transmission (T_{SOT} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D0+/- of the display module are entering (T_{SOT}) in the High-Speed Data Transmission(HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below.

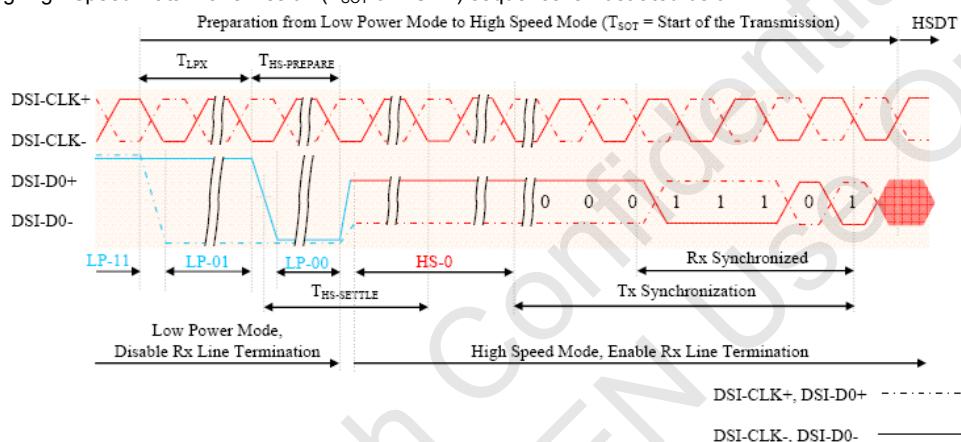


Figure 6.2.3.3.1. T_{SOT} of HSDT

Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

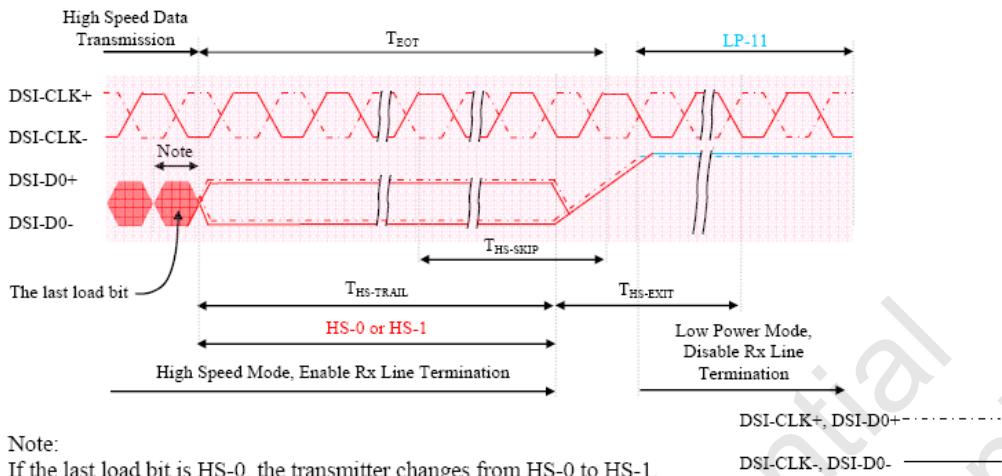
The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSI- CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes

DSI-D0+/- are in LP-11 mode. See more information on chapter “7.2.2 High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
 - MCU changes to HS-1, if the last load bit is HS-0
 - MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below


 Figure 6.2.3.3.2. T_{EOT} of HSDT

Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets.

These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter "Short Packet (SPa) and Long Packet (LPa) Structures".

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

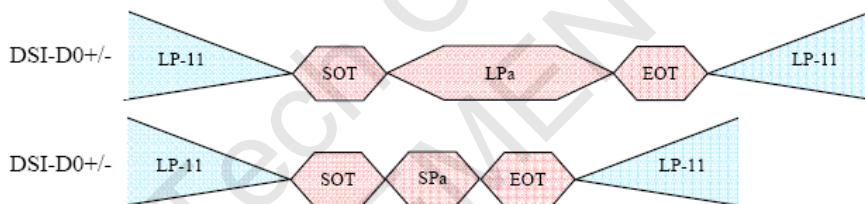


Figure 6.2.3.3.3. Single packet in HSDT

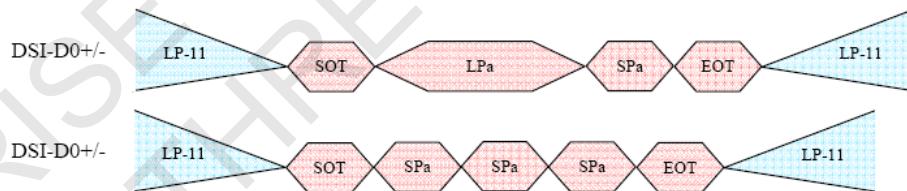


Figure 6.2.3.3.4. Multiple packets in HSDT

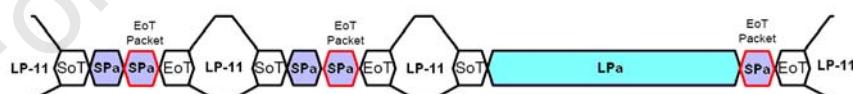


Figure 6.2.3.3.5. Packets with EoT package in HSDT

Abbreviation	Explanation
LP-11	Low Power Mode, Data lanes are '1's (Stop Mode)
SOT	Start of the Transmission
LPa	Long Packet
SPa	Short Packet
EOT	End of the Transmission

Table 6.2.3.3.1. Abbreviations

6.2.3.4. Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU and display module are using the same sequence when this bus turnaround procedure is used.

This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follows.

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 =>LP-10 =>LP-00
- The MCU waits until the display module is starting to control DSI-D0+/- data lanes and the MCU stops to control DSI-D0+/- data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the MCU to the display module) is illustrated below.

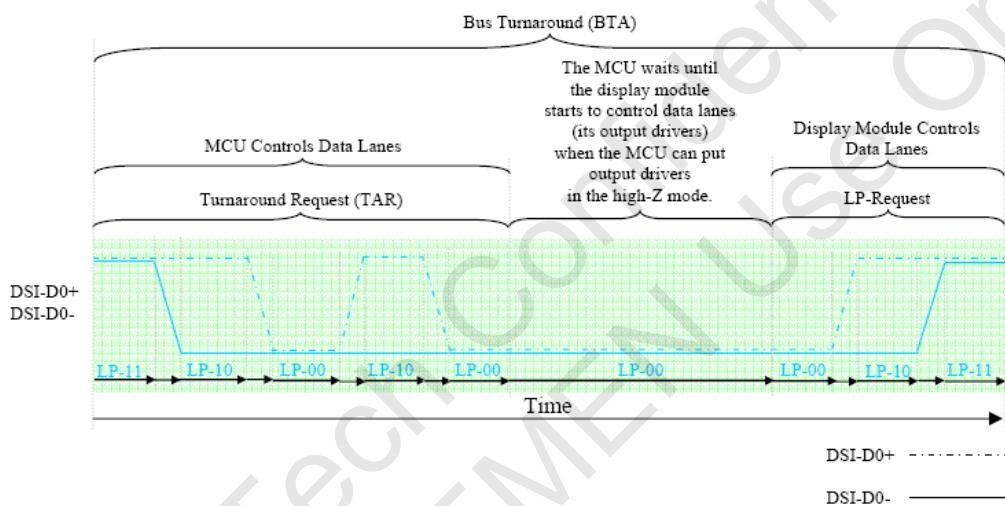


Figure 6.2.3.4.. Bus turnaround procedure

6.2.3.5. Two data-lane high speed transmission

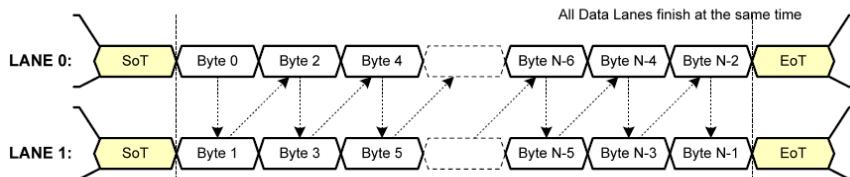
Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of lanes, one lane may run out of data before the other. Therefore, the lane management layer, as it buffers up the final set of less-than-2 bytes, de-asserts its "valid data" signal into all lanes for which there's no further data.

Although all lanes start simultaneously with parallel SoTs, each lane operates independently and may complete the HS transmission before the other lane, sending an EoT one cycle (byte) earlier.

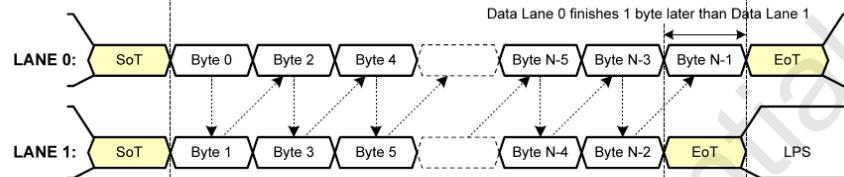
The two PHYs on the receiving end of the link collect bytes in parallel and feed them into the lane management layer. The lane management layer reconstructs the original sequence of bytes in the transmission.

Figure 6.2.3.5. shows the way a HS transmission can terminate for two data-lane HS transmission.

Number of Bytes, N, transmitted is an integer multiple of the number of lanes:



Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes:



KEY:
 LPS – Low Power State SoT – Start of Transmission EoT – End of Transmission

Figure 6.1.3.5.. Two data-lane HS transmission example

6.2.3.6. Three data-lane high speed transmission

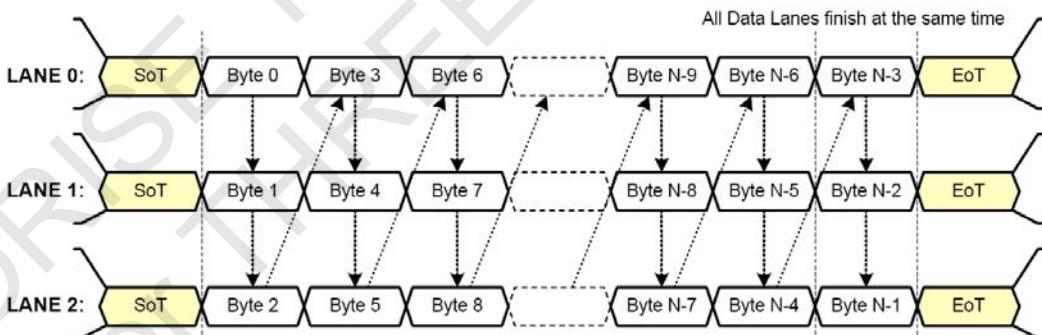
Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of Lanes, some Lanes may run out of data before others. Therefore, the Lane Management layer, as it buffers up the final set of less-than-N bytes, de-asserts its "valid data" signal into all Lanes for which there is no further data.

Although all Lanes start simultaneously with parallel SoTs, each Lane operates independently and may complete the HS transmission before the other Lanes, sending an EoT one cycle (byte) earlier.

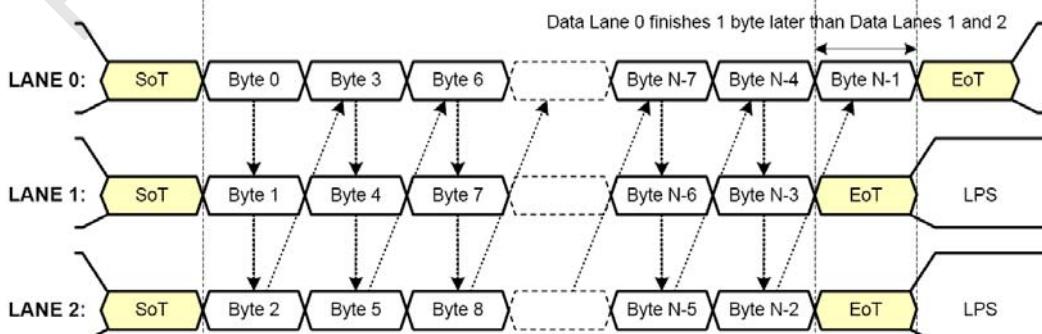
The N PHYs on the receiving end of the Link collect bytes in parallel and feed them into the Lane Management layer. The Lane Management layer reconstructs the original sequence of bytes in the transmission.

Below Figure illustrate a variety of ways a HS transmission can terminate for different number of Lanes and packet lengths.

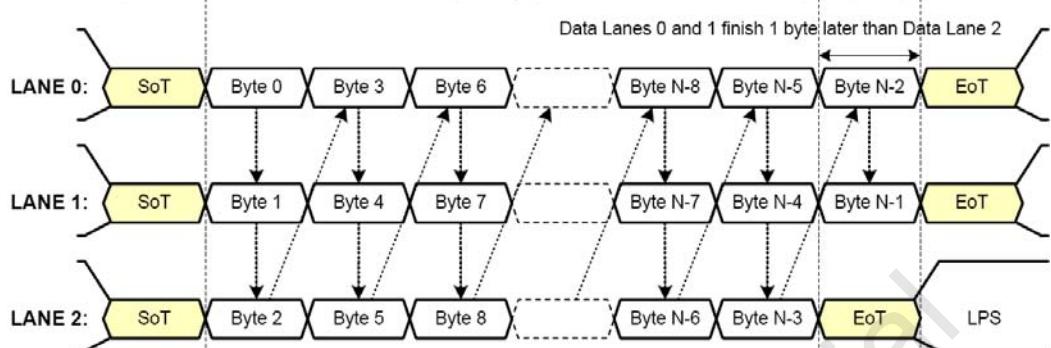
Number of Bytes, N, transmitted is an integer multiple of the number of lanes:



Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 1):



Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 2):



6.2.4. Packet level communication

6.2.4.1. Short Packet (SPa) and Long Packet (LPa) structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

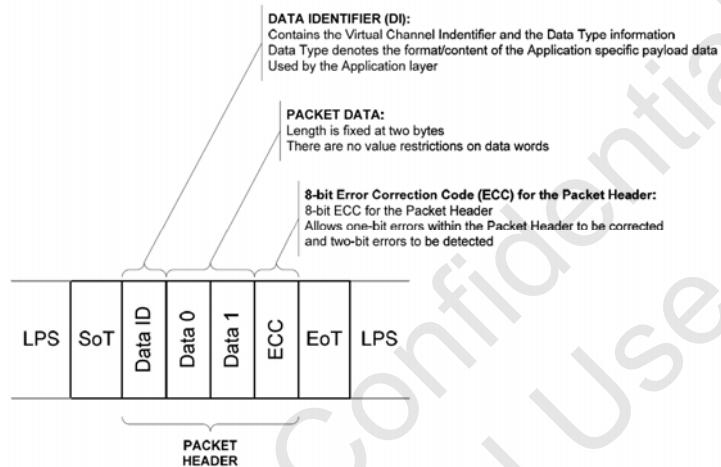


Figure 6.2.4.1.1. Short packet structure

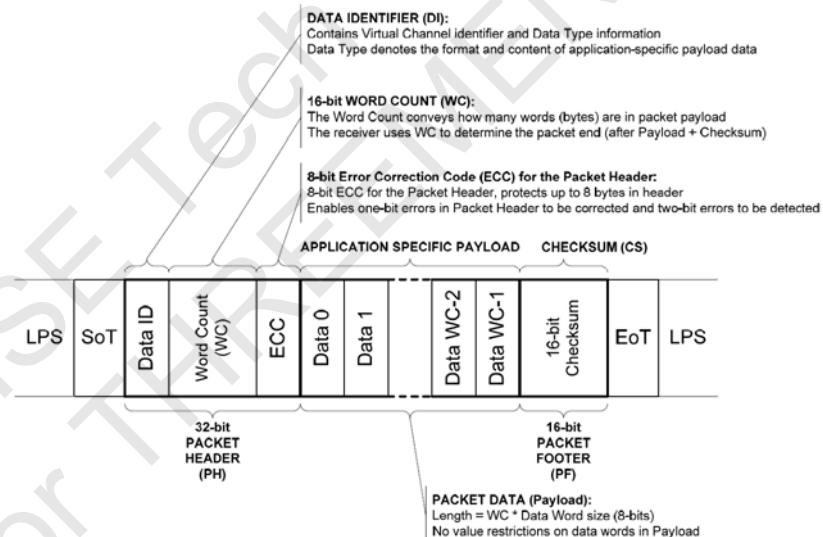


Figure 6.2.4.1.2. Long packet structure

Note:

"Figure 6.2.4.1.1: Short Packet (SPa) Structure" and "Figure 6.2.4.1.2: Long Packet (LPa) Structure" are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format. e.g.:

- LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11
- LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11
- LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11

Bit Order of the Byte on Packets

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified.

Figure 6.2.4.1.3 shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

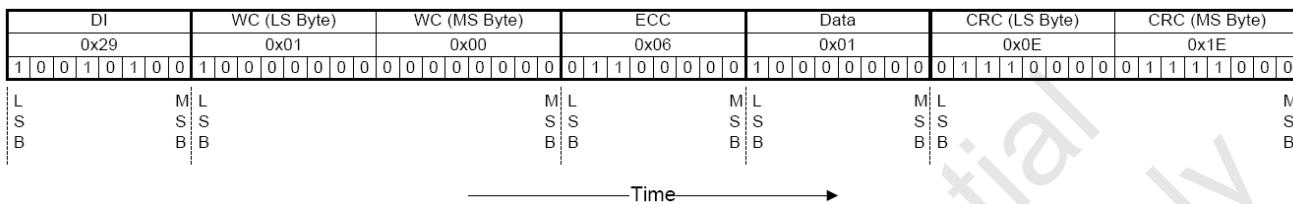


Figure 6.2.4.1.3. Bit order of the byte on packets

Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last.

e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

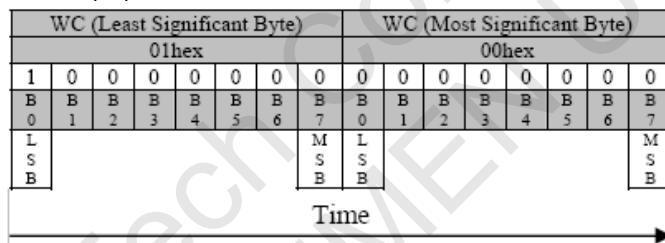


Figure 6.2.4.1.4. Byte order of the multiple byte information on packets

Packet Head (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

- 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

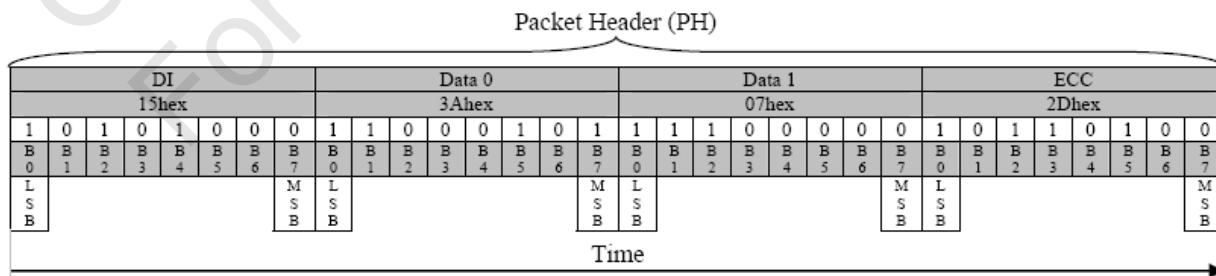


Figure 6.2.4.1.5. Packet head on short packet

Long Packet (LPa):

- 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)

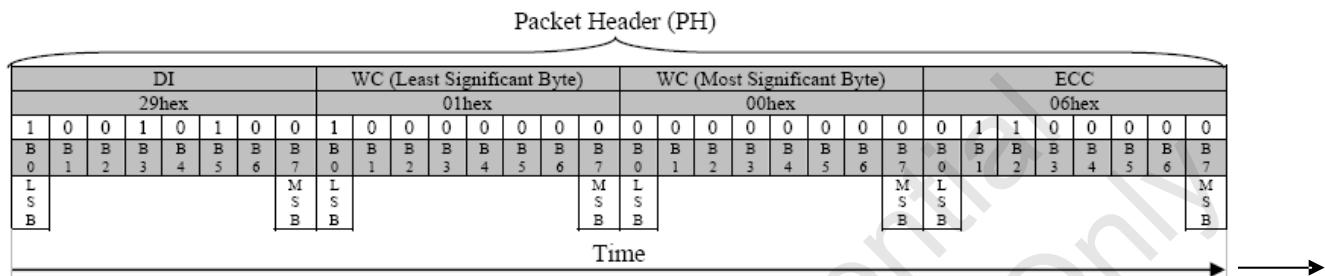


Figure 6.2.4.1.6. Packet head on long packet

Data Identification

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI[7...6]
- Data Type (DT), 6 bits, DI[5...0]

The Data Identification (DI) structure is illustrated on a table below.

B7	B6	B5	B4	B3	B2	B1	B0
VC		DT					
Virtual Channel Identifier (VC)		Data Type (DT)					

Table 6.2.4.1.7. Data identification structure

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

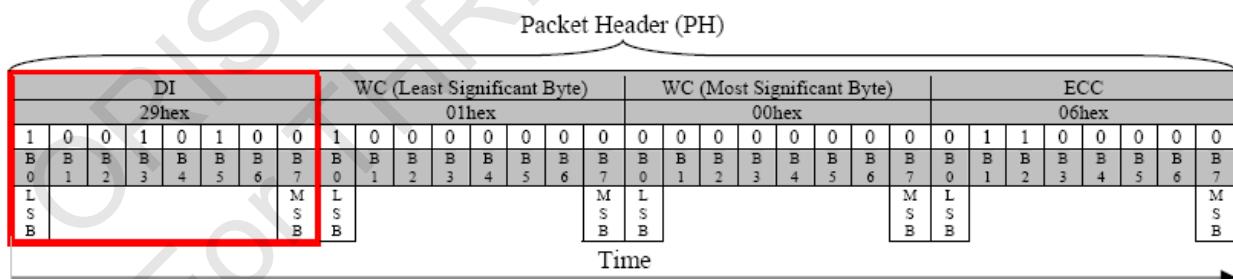


Figure 6.2.4.1.8. Data identification of the packet head

Virtual Channel (VC)

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals.

Virtual Channel (VC) is a part of Data Identification (DI[7...6]) structure and it is used to address where a packet is wanted to send from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

OTM9608A only support VC code=00, package with other VC code(01/10/11) will be filter out.

Packet Header (PH)																	
DI						WC (Least Significant Byte)			WC (Most Significant Byte)			ECC					
29hex						01hex			00hex			06hex					
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0
B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1
L	S	B				M	L		M	L		M	L		M	S	B
						S	S		S	S		S	S		S	S	B
						B	B		B	B		B	B		B	B	B
Time																	

Figure 6.2.4.1.9. Virtual channel on the packet head

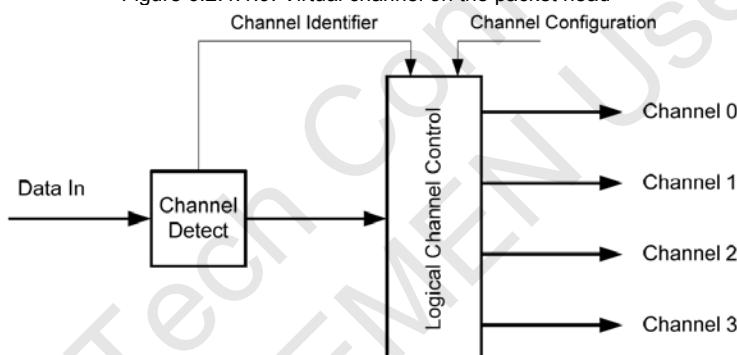


Figure 6.2.4.1.10. Virtual channel Block Diagram (Receiver Case)

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5...0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

Packet Header (PH)																	
DI						WC (Least Significant Byte)			WC (Most Significant Byte)			ECC					
29hex						01hex			00hex			06hex					
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0
B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1
L	S	B				M	L		M	L		M	L		M	S	B
						S	S		S	S		S	S		S	S	B
						B	B		B	B		B	B		B	B	B
Time																	

Figure 6.2.4.1.11. Data Type on the packet head

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Type (DT) are defined on tables below.

From the MCU to the Display module		
Data Type (HEX)	Data Type (Binary)	Description
01h	00 0001	Sync Event, V Sync Start
11h	01 0001	Sync Event, V Sync End
21h	10 0001	Sync Event, H Sync Start
31h	11 0001	Sync Event, H Sync End
08h	00 1000	End of Transmission (EoT) packet
02h	00 0010	Color Mode (CM) Off Command
12h	01 0010	Color Mode (CM) On Command
22h	01 0010	Shut Down Peripheral Command
32h	11 0010	Turn On Peripheral Command
03h	00 0011	Generic Short WRITE, no parameters
13h	01 0011	Generic Short WRITE, 1 parameters
23h	10 0011	Generic Short WRITE, 2 parameters
04h	00 0100	Generic READ, no parameters
14h	01 0100	Generic READ, 1 parameters
24h	10 0100	Generic READ, 2 parameters
05h	00 0101	DCS WRITE, no parameters
15h	01 0101	DCS WRITE, 1 parameters
06h	00 0110	DCS READ, no parameters
37h	11 0111	Set Maximum Return Packet Size
09h	00 1001	Null Packet, no data
19h	01 1001	Blanking Packet, no data
29h	10 1001	Generic Long Write
39h	11 1001	DCS Long Write\write_LUT Command Packet
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format

Table 6.2.4.1.12. Data Type from the MCU to the display module

From the Display Module to the MCU		
Data Type (HEX)	Data Type (Binary)	Description
02h	00 0010	Acknowledge & Error Report
1Ch	01 1100	DCS Long READ Response
21h	10 0001	DCS Short READ Response, 1 byte returned
22h	10 0010	DCS Short READ Response, 2 byte returned

Table 6.2.4.1.13. Data Type from the display module to the MCU

The receiver is ignored other Data Type (DT) if they are not defined on tables above.

Host send "Generic Read" data type, OTM9608A will return DCS Read package to Host.

Packet Data on the Short Packet

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to 00h, if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below.

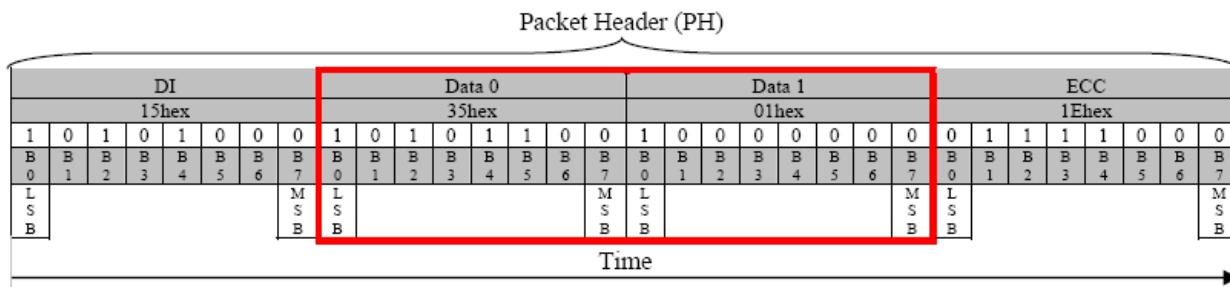


Figure 6.2.4.1.14. Packet data on the short packet, 2 bytes information

Packet Data (PD) information:

- Data 0: 10hex
- Data 1: 00hex (Null)

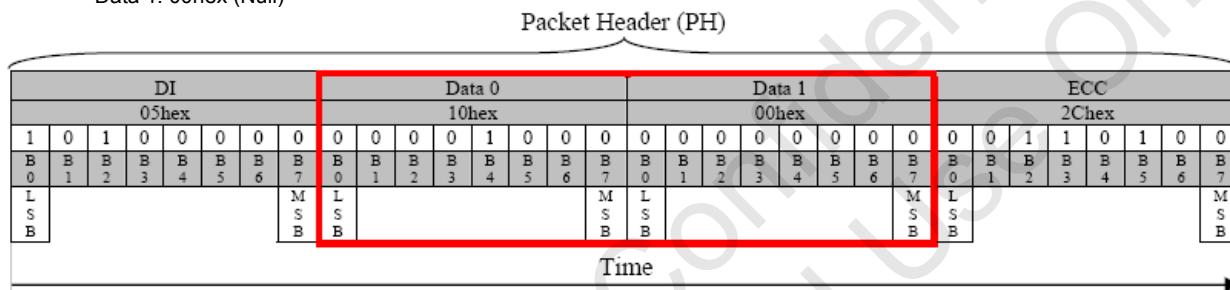


Figure 6.2.4.1.15. Packet data on the short packet, 1 bytes information

Word Count on the Long packet

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

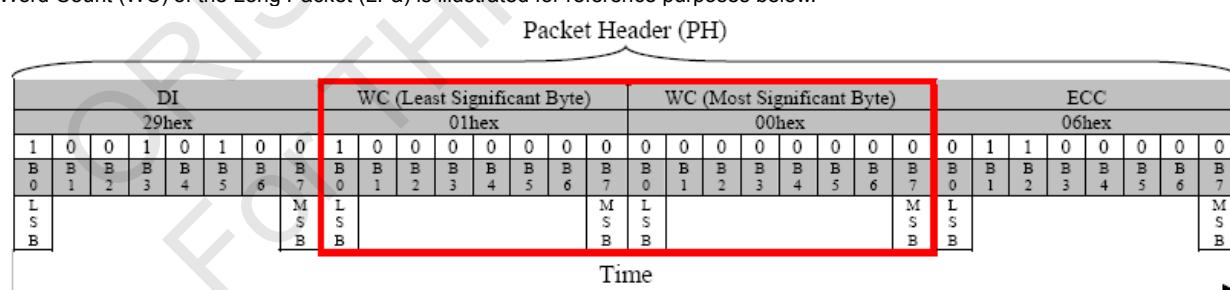


Figure 6.2.4.1.16. Word count on the long packet

Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors:

- Short Packet (SPa): Data Identification (DI) and Packet Data (PD) bytes (24 bits: D[23...0])
- Long Packet (LPa): Data Identification (DI) and Word Count (WC) bytes (24 bits: D[23...0])

D[23...0] is illustrated for reference purposes below.

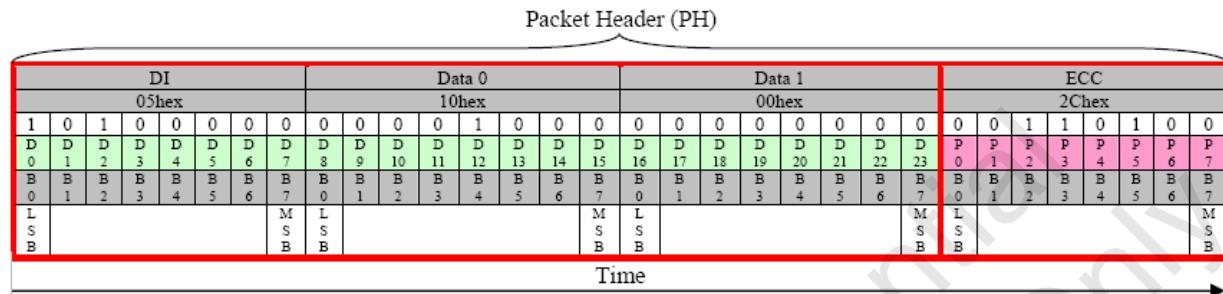


Figure 6.2.4.1.17. D[23:0] and P[7:0] on the short packet

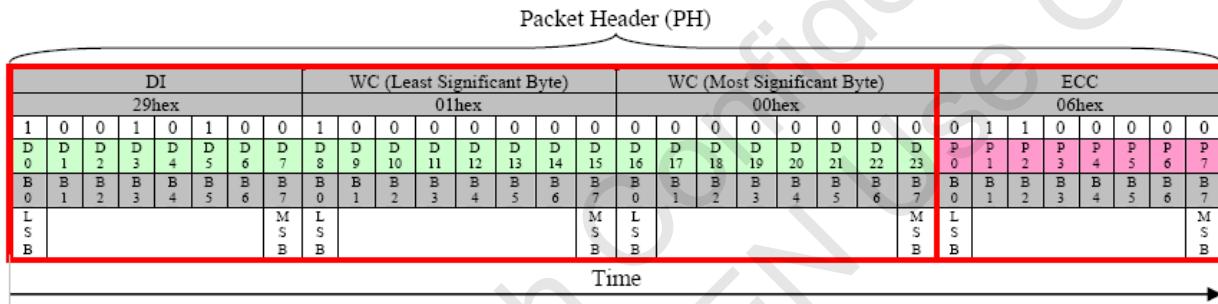


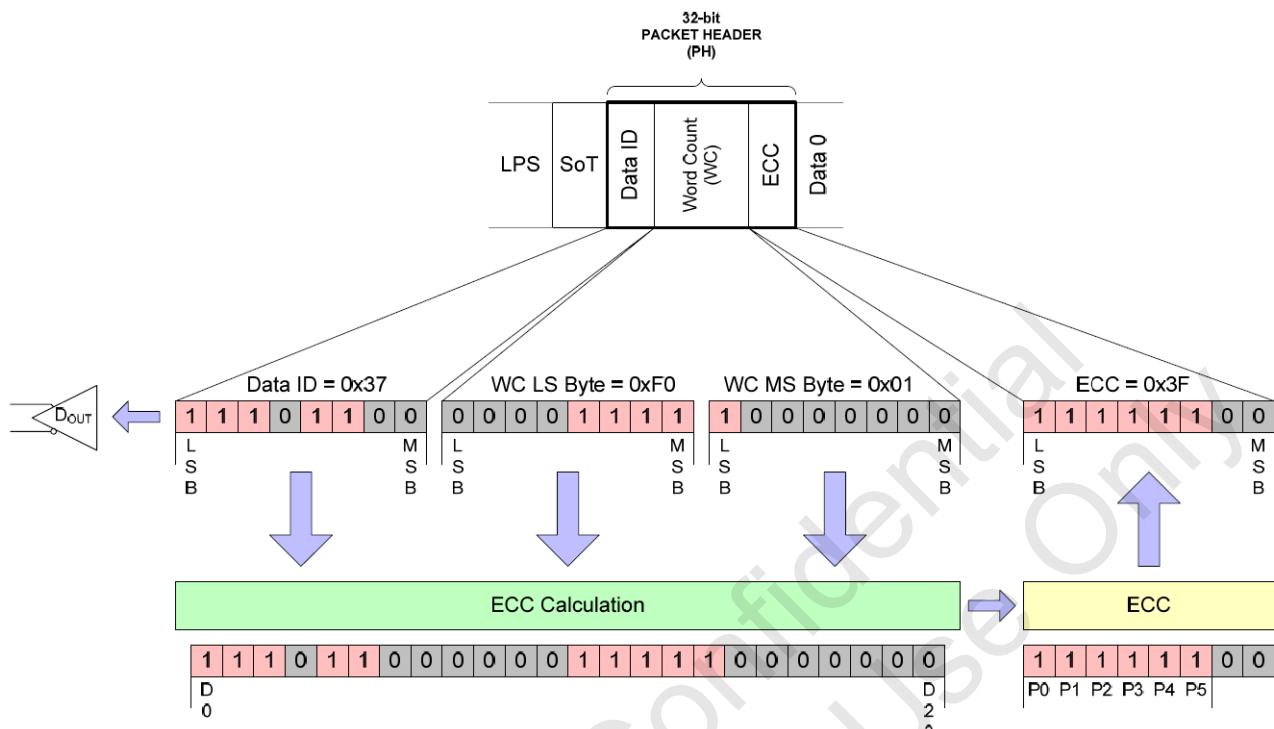
Figure 6.2.4.1.18. D[23:0] and P[7:0] on the long packet

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7...0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

- P7 = 0
- P6 = 0
- P5 = $D10 \wedge D11 \wedge D12 \wedge D13 \wedge D14 \wedge D15 \wedge D16 \wedge D17 \wedge D18 \wedge D19 \wedge D21 \wedge D22 \wedge D23$
- P4 = $D4 \wedge D5 \wedge D6 \wedge D7 \wedge D8 \wedge D9 \wedge D16 \wedge D17 \wedge D18 \wedge D19 \wedge D20 \wedge D22 \wedge D23$
- P3 = $D1 \wedge D2 \wedge D3 \wedge D7 \wedge D8 \wedge D9 \wedge D13 \wedge D14 \wedge D15 \wedge D19 \wedge D20 \wedge D21 \wedge D23$
- P2 = $D0 \wedge D2 \wedge D3 \wedge D5 \wedge D6 \wedge D9 \wedge D11 \wedge D12 \wedge D15 \wedge D18 \wedge D20 \wedge D21 \wedge D22$
- P1 = $D0 \wedge D1 \wedge D3 \wedge D4 \wedge D6 \wedge D8 \wedge D10 \wedge D12 \wedge D14 \wedge D17 \wedge D20 \wedge D21 \wedge D22 \wedge D23$
- P0 = $D0 \wedge D1 \wedge D2 \wedge D4 \wedge D5 \wedge D7 \wedge D10 \wedge D11 \wedge D13 \wedge D16 \wedge D20 \wedge D21 \wedge D22 \wedge D23$

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63...0]), but this implementation is based on 24 bit value (D[23...0]). Therefore, there is only needed 6 bits (P[5...0]) for Error Correction Code (ECC).



Packet Footer on the Long Packet

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial $X^{16}+X^{12}+X^5+X^0$ as it is illustrated below.

$$\text{Polynomial: } x^{16} + x^{12} + x^5 + x^0$$

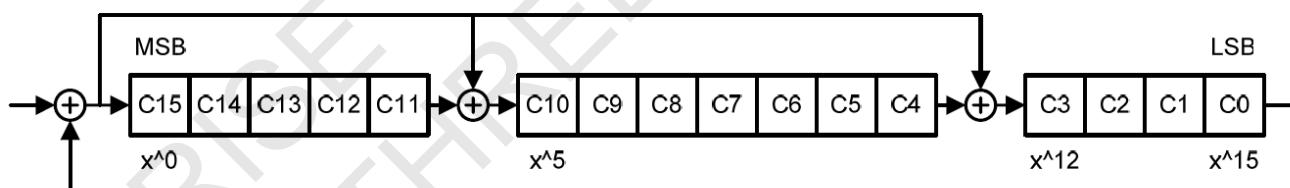


Figure 6.2.4.1.20 16-bit cyclic redundancy check (CRC) calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.

The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

6.2.4.2. Packet transmissions

Packet from the MCU to the Display Module

Display Command Set (DCS), which is defined on chapter “Instructions” is used from the MCU to the display module.

This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.

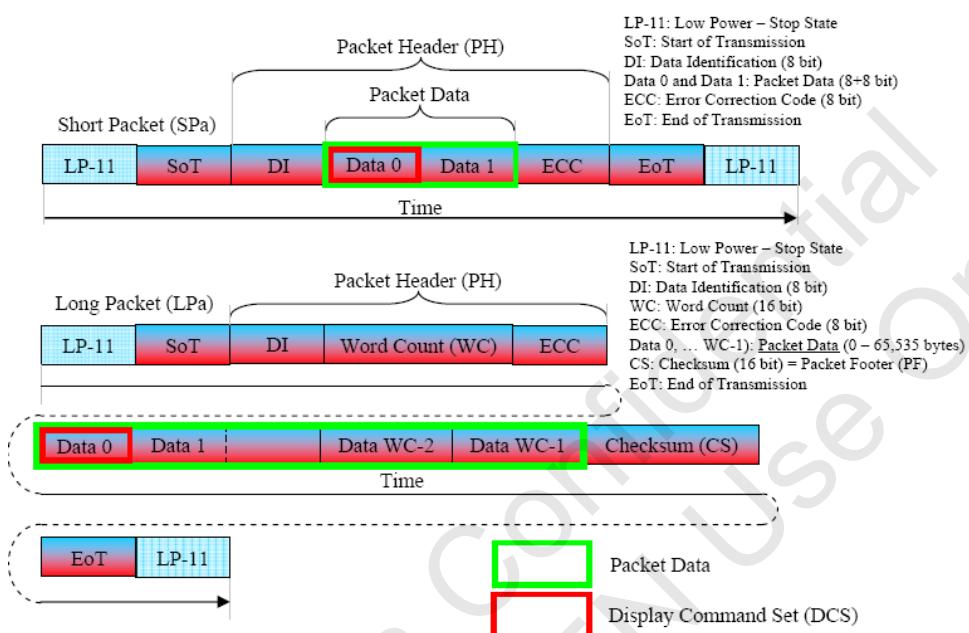


Figure 6.2.4.21. DCS on the short packet and long packet

Packet from the Display Module to the MCU

Used Packet Types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS).

The used packet type is defined on Data Type (DT). See chapter “6.2.4.22. Data Type (DT)”.

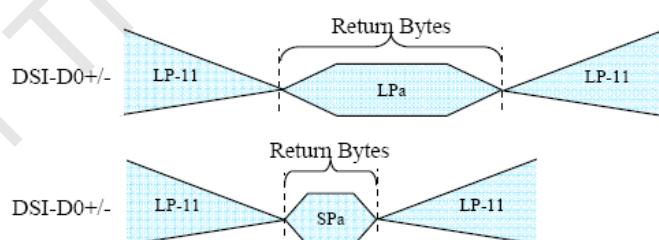


Figure 6.2.4.22. Return bytes on single packet

Acknowledge with Error Report (AwER)

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to 1 , as they are defined on the following table.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	High-Speed Receive Timeout Error Any Protocol Timer Time-Out
6	False Control Error
7	Reserved, Set to '0' internally Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

Figure 6.2.4.23. Acknowledge with error report for long packet response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	High-Speed Receive Timeout Error Any Protocol Timer Time-Out
6	False Control Error
7	Reserved, Set to '0' internally Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Set to '0' internally (Only for Long Packet (LP))
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

Figure 6.2.4.24. Acknowledge with error report for short packet response

These errors are only included on the last packet, which has been received from the MCU to the display module, before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 0010b
- Packet Data (PD)
 - Bit 8: ECC Error, single-bit (detected and corrected)
 - AwER: 0100h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

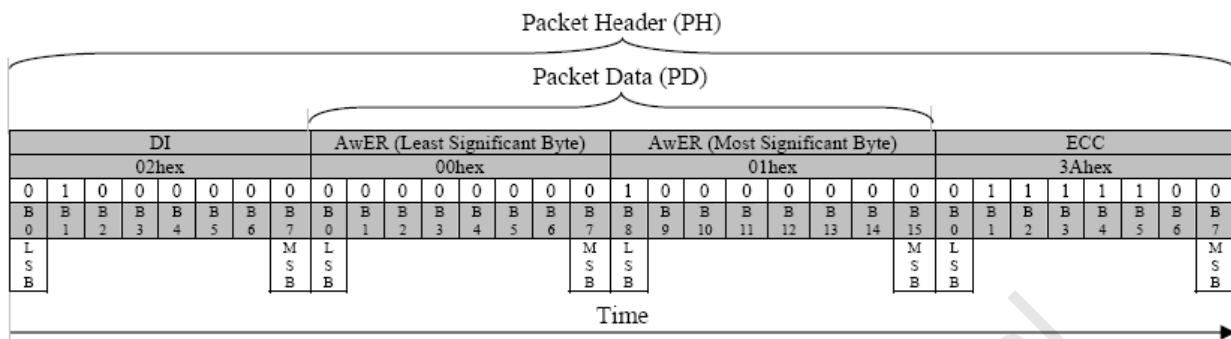


Figure 6.2.4.25. Acknowledge with error report – example

6.2.5. Customer-defined generic read data type Format

The short packet of Data Type 24h (Generic READ, 2 parameters) specifies the register content for read and the Nth parameter that will begin reading. After Data Type 24h is received, BTA is executed. Then, the Nth parameter becomes the first data, and the number of data of WC (word count) value is output.

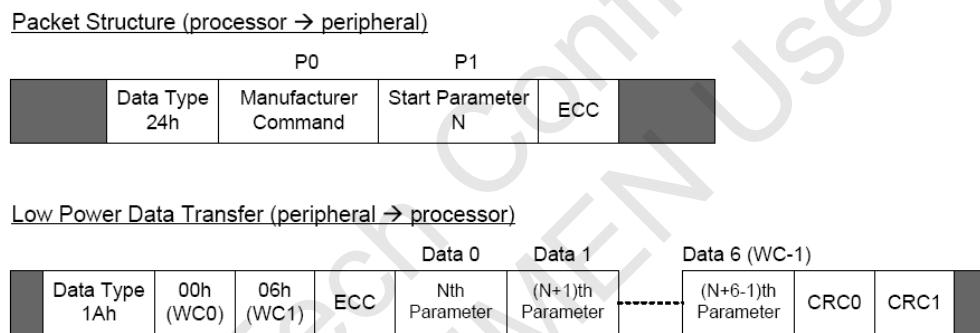
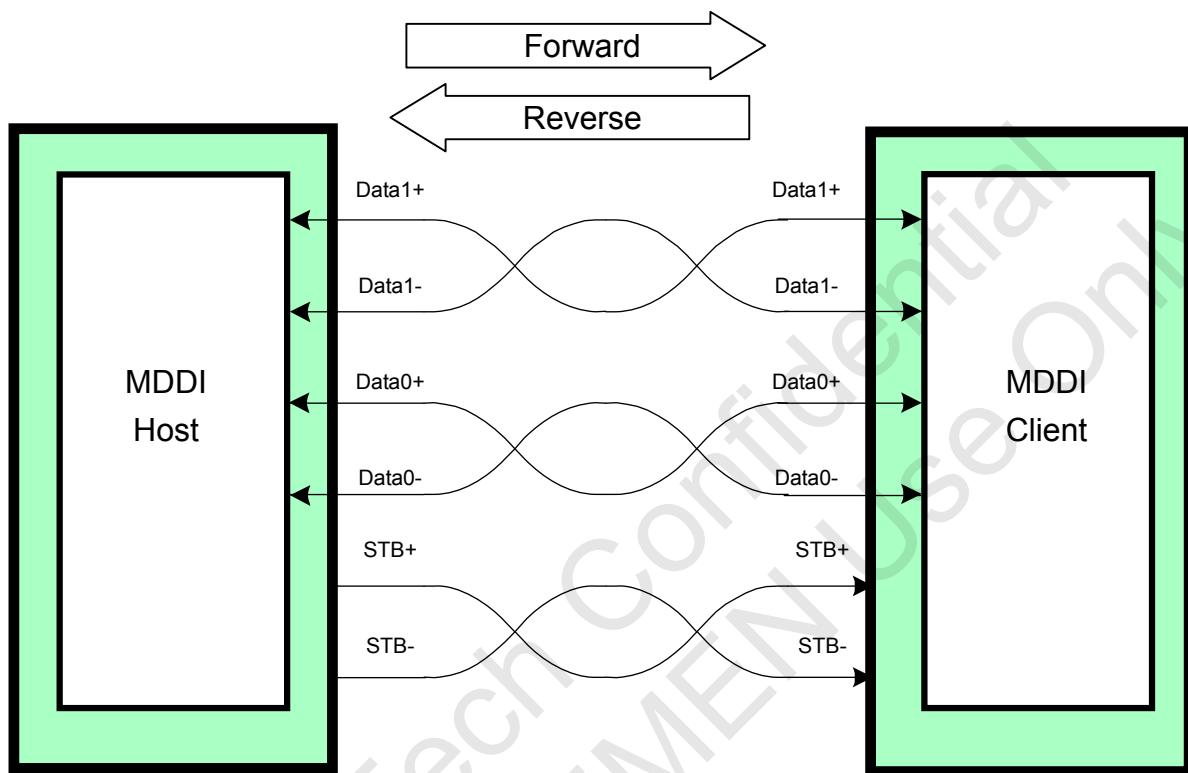


Figure 6.2.5. Generic read data type format

6.3. MDDI interface

6.3.1. General description

The MDDI is a differential and serial interface with high speed. The OTM9608A support the MDDI Type 1 and Type 2.



6.3.2. MDDI Packet summary

The OTM9608A support packet type as shown in table.

Table 6.3.2 The support packet type

	Packet Name	Packet Type (Dec)	Direction
Link Control Packets	Sub-frame header packet	15359	Forward
	Filler packet	0	Forward
	Reverse link encapsulation packet	65	Forward
	Link shutdown packet	69	Forward
	Round-trip delay measurement packet	82	Forward
Basic Media Stream Packets	Video stream packet	16	Forward
Client Status and Control Packets	Client capability packet	66	Reverse
	Client request and status packet	70	Reverse
	Register access packet	146	Forward / Reverse

6.3.3. MDDI Packet format

The structure of the forward link is illustrated in Figure 6.2.3.1. Information transmitted over the MDDI link is grouped into packets. The definition of the types of packets is given later in this section. Multiple packets are grouped together into a sub-frame, and multiple sub-frames make up a media-frame. Every sub-frame begins with a special packet called a Sub-frame Header Packet.

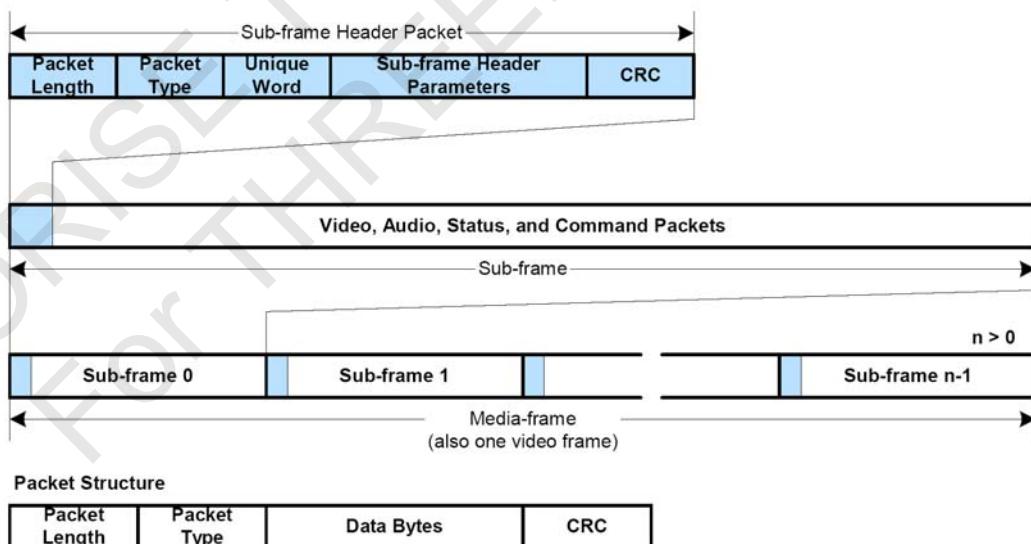


Table 6.3.3. Forward link structure

6.3.3.1. Sub frame header packet

The Sub-Frame Header Packet is the first packet of every sub-frame, and its basic structure is illustrated in Figure 6.2..3.1.1. The Sub-Frame Header Packet is required for host-client synchronization. Every host shall be able to generate this packet, and every client shall be able to receive and interpret this packet.

Sub-frame Header Packet

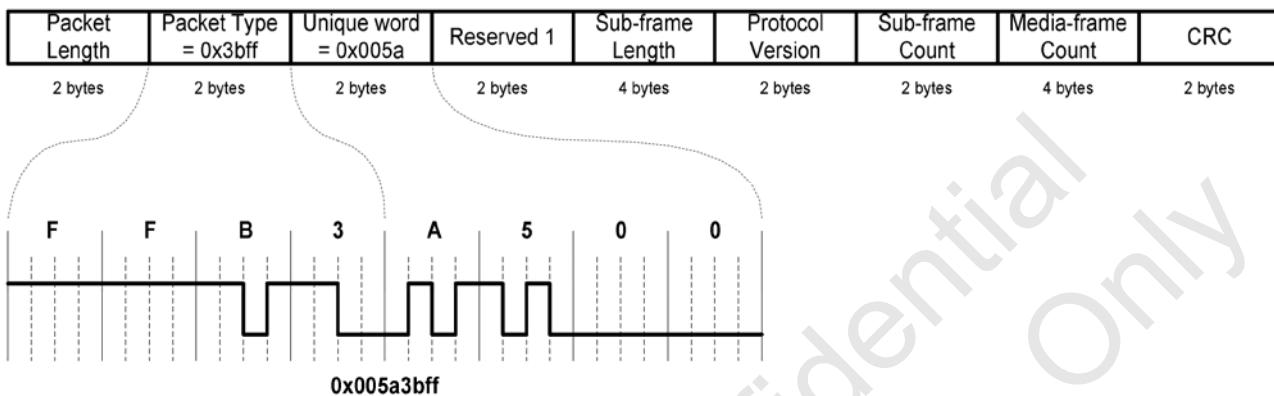


Figure 6.3.3.1 Sub Frame Header Packet format

Packet Contents:

- Packet Length – 2 bytes that contain a 16-bit unsigned integer that specifies the total number of bytes in the packet not including the packet length field. The Packet Length of this packet is always 20.
- Packet Type – 2 bytes that contain a 16-bit unsigned integer. A Packet Type of 15359 (0x3bff hexadecimal) identifies the packet as a Sub-frame Header Packet.
- Unique Word – 2 bytes that contain a 16-bit unsigned integer that contains the 16 most significant bits of the unique word. The 4-byte combination of the Packet Type and Unique Word together form a 32-bit unique word with good autocorrelation. The actual unique word is 0x005a3bff where the lower 16 bits are transmitted first as the Packet Type, and the most significant 16 bits are transmitted immediately afterward.
- Reserved 1 – 2 bytes that contain a 16-bit unsigned integer that is reserved for future use. All bits in this field shall be set to zero. The purpose of this field is to cause all subsequent 2 byte fields to align to a 16-bit word address and cause 4-byte fields to align to a 32-bit word address. The least significant byte is reserved to indicate that the host is capable of addressing multiple client devices. A value of zero is reserved to indicate that the host is capable of operating only with a single client device.
- Sub-frame Length – 4 bytes that contain a 32-bit unsigned integer that specifies the number of bytes per sub-frame. It is valid to change the Sub-frame Length on-the-fly from one sub-frame to the next. This is useful in order to make minor timing adjustments in the sync-pulses for isochronous streams. If the CRC of the Sub-frame Header packet is not valid then the link controller shall use the Sub-frame Length of the previous known-good Sub-frame Header packet to estimate the length of the current sub-frame.
- Protocol Version – 2 bytes that contain a 16-bit unsigned integer that specifies the protocol version used by the host. The Protocol Version field shall be set to 0 to specify the version of the protocol described in this document.
- Sub-frame Count – 2 bytes that contain a 16-bit unsigned integer that specifies a sequence number that indicates the number of sub-frames that have been transmitted since the beginning of the media-frame. The first sub-frame of the media-frame has a Sub-frame Count of zero. The last sub-frame of the media-frame has a value of n-1, where n is the number of sub-frames per media-frame. The value in the Sub-frame Count field shall be equal to the Sub-frame Count sent in the previous Sub-frame Header Packet plus 1, except for the first sub-frame of a media-frame when the Sub-frame Count shall be zero.
- Media-frame Count – 4 bytes that contain a 32-bit unsigned integer that specifies a sequence number that indicates the number of media-frames that have been transmitted since the beginning of the present media item. The first media-frame of the media item has a Media-frame Count of zero. The Media-frame Count increments immediately prior to the first sub-frame of each media-frame and wraps back to zero after the maximum Media-frame Count (media-frame number 232-1 = 4,294,967,295) is used. The Media-frame Count value may be reset at any time by the host to suit the needs of the end application.
- CRC – 2 bytes that contain a 16-bit CRC of all bytes in the packet including the Packet Length.

6.3.3.2. Video stream packet

The Video Stream Packets carry video data to update a rectangular region of the display. The size of this region may be as small as a single pixel or as large as the entire display. There may be an unlimited number of streams displayed simultaneously (limited only by system resources) because all context required to display a stream is contained within the Video Stream Packet. The format of the Video Stream Packet is illustrated in Figure 6.3.3.2.1. The client shall indicate its capability to receive a Video Stream Packet via the RGB Capability, Monochrome Capability, and Y Cr Cb Capability fields of the Client Capability Packet.

Packet Length	Packet Type = 16	bClient ID	Video Data Format Descriptor	Pixel Data Attributes	X Left Edge	Y Top Edge	X Right Edge	Y Bottom Edge
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes
X Start	Y Start	Pixel Count	Parameter CRC	Pixel Data		Pixel Data CRC		
2 bytes	2 bytes	2 bytes	2 bytes	Packet Length - 26 bytes		2 bytes		

Figure 6.3.3.2.1 Video Stream Packet

Packet Contents:

- Packet Length – 2 bytes that contain a 16-bit unsigned integer that specifies the total number of bytes in the packet not including the packet length field.
- Packet Type – 2 bytes that contain a 16-bit unsigned integer. A Packet Type of '0010h' identifies the packet as a Video Stream Packet.
- bClient ID – 2 bytes that contain a 16-bit unsigned integer reserved for the Client ID. This field is reserved for future use and shall be set to '0000h'.
- Video Data Format Descriptor – 2 bytes that contain a 16-bit unsigned integer that specifies the format of each pixel in the Pixel Data in the present stream in the present packet.
 - bits[15:13] = 010 : Value fixed.
 - bits[12] = 1 : Only packed type is available (fixed value)
 - bits[11:0] = 010101100101 (565h) : 16bpp (RGB(565))
= 011001100110 (666h) : 18bpp (RGB(666))
= 100010001000 (888h) : 24bpp (RGB(888))

MDDI Data Type	D7	D6	D5	D4	D3	D2	D1	D0	Color
RGB 5:6:5	Byte n	G2	G1	G0	B4	B3	B2	B1	B0
	Byte n+1	R4	R3	R2	R1	R0	G5	G4	G3
RGB 6:6:6	Byte n	G1	G0	B5	B4	B3	B2	B1	B0
	Byte n+1	R3	R2	R1	R0	G5	G4	G3	G2
RGB 8:8:8	Byte n+2	B5	B4	B3	B2	B1	B0	R5	R4
	Byte n	B7	B6	B5	B4	B3	B2	B1	B0
	Byte n+1	G7	G6	G5	G4	G3	G2	G1	G0
	Byte n+2	R7	R6	R5	R4	R3	R2	R1	R0

Figure 6.3.3.2.2 Packed pixel data format

- Pixel Data Attributes – 2 bytes that contain a 16-bit unsigned integer.
bit[15:0] = 0003h (fixed value)
- X Left Edge – 2 bytes that contain a 16-bit unsigned integer that specifies the X coordinate of the left edge of the screen window filled by the Pixel Data field.
- Y Top Edge – 2 bytes that contain a 16-bit unsigned integer that specifies the Y coordinate of the top edge of the screen window filled by the Pixel Data field.

- X Right Edge – 2 bytes that contain a 16-bit unsigned integer that specifies the X coordinate of the right edge of the window being updated.
- Y Bottom Edge – 2 bytes that contain a 16-bit unsigned integer that specifies the Y coordinate of the bottom edge of the window being updated.
- X Start – 2 bytes that contain a 16-bit unsigned integer that specifies the absolute X coordinate, where the point (X Start, Y Start) is the first pixel in the Pixel Data field below.
- Y Start – 2 bytes that contain a 16-bit unsigned integer that specifies the absolute Y coordinate, where the point (X Start, Y Start) is the first pixel in the Pixel Data field below.
- Pixel Count – 2 bytes that contain a 16-bit unsigned integer that specifies the number of pixels in the Pixel Data field below.
- Parameter CRC – 2 bytes that contain a 16-bit CRC of all bytes from the Packet Length to the Pixel Count. If this CRC fails to check then the entire packet shall be discarded.
- Pixel Data – The raw video information to be displayed. Data is formatted in the manner described by the Video Data Format Descriptor field. If bit 5 of the Pixel Data Attributes field is set to one then the Pixel Data field contains exactly one row of pixels, where the first pixel transmitted corresponds to the leftmost pixel and the last pixel transmitted corresponds to the right-most pixel.
- Pixel Data CRC – 2 bytes that contain a 16-bit CRC of only the Pixel Data. If this CRC fails to check then the Pixel Data may still be used but the CRC error count shall be incremented. Window address and RAM address setting depends on Video Stream Packet setting.

6.3.3.3. Link shut down packet

Packet Length	Packet Type = 69	CRC	All Zeros
2 bytes	2 bytes	2 bytes	(Packet_Length - 4) bytes

Figure 6.3.3.3. Link Shut down Packet Format

The Shutdown Packet is sent from the host to the client to indicate that the MDDI Data and strobe will be shut down and go into a low-power hibernation state. This packet is useful to shut down the link and conserve power after static Image Data are sent from a mobile communication device to the client. Normal operation is resumed when the link is restarted and the host sends packets again. The first packet sent after hibernation is a sub-frame header packet. The Shutdown Packet is required to enable link hibernation. More information about link shutdown and wake-up is provided by some weak up sequence. Every host shall be able to generate this packet, and every client shall be able to receive and interpret this packet.

6.3.3.4. Filler Packet

Packet Length	Packet Type = 0	filler bytes (all zero recommended)	CRC
2 bytes	2 bytes	(Packet_Length - 4) bytes	2 bytes

Figure 6.3.3.4. Filler Packet Format

The Filler Packet is sent when no other information is available to be sent on the forward link. It is recommended to send filler packets with minimum length to allow maximum flexibility to send other packets when required. At the very end of a sub-frame encapsulation packet the MDDI link controller shall set the size of the Filler Packet to exactly fill the remaining space to maintain packet integrity. The Filler Packet is required to maintain timing on the link when the host has no information to send. Every host and client shall be able to send and receive this packet.

6.3.3.5. Reverse Link Encapsulation Packet

Packet Length	Packet Type = 65	hClient ID	Reverse Link flags	Reverse Rate Divisor	Turn-Around 1 Length	Turn-Around 2 Length
2 bytes	2 bytes	2 bytes	1 byte	1 byte	1 byte	1 byte

Parameter CRC	All Zero 1	Turn-Around 1	reverse data packets	Turn-Around 2	All Zero 2
2 bytes	8 bytes	x bytes	(Packet_Length - x - y - 26) bytes	y bytes	8 bytes

Figure 6.3.3.5. Reverse Link Encapsulation Packet Format

Data is transferred in the reverse direction using the Reverse Link Encapsulation Packet. A forward link packet is sent and the MDDI link is turned around in the middle of this packet so that packets can be sent in the reverse direction. The MDDI_Stb signal is always driven by the host. The host behaves as if it were transmitting a zero for each bit of the Turn-Around, Driver Re-enable, and Reverse Data Packets fields of the packet. The result is that the MDDI_Stb toggles at each bit boundary of these portions of the packet. The client shall clock new data on certain rising edges of the MDDI strobe as specified in the packet contents description below, and in more detail in section 7. The format of the Reverse Link Encapsulation Packet is illustrated in Figure 6.2.3.5.1. For External Mode every host shall be able to generate this packet and receive data, and every client shall be able to receive and send data to the host. Implementation of this packet is optional for Internal Mode, but the Reverse Link Encapsulation Packet is necessary for the host to receive data from the client.

Packet Contents:

- **Packet Length** – Specifies the total number of bytes in the packet not including the packet length field.
- **Packet Type** – A Packet Type of 65=0x0041 identifies the packet as a Reverse Link Encapsulation Packet.
- **hClient ID** – This field is reserved for future use and shall be set to zero
- **Reverse Link Flags** – 1 byte that contains an 8-bit unsigned integer that contains a set of flags to request information from the client and specify the reverse link interface type. If a bit is set to one then the host requests the specified information from the client. If the bit is zero then the host does not need the information from the client.
 - Bit 0 – The host needs the Client Capability Packet.
 - Bit 1 – The host needs the Client Request and Status Packet.
 - Bits [7:2] – reserved for future use and shall be set to zero.

- **Reverse Rate Divisor** – 1 byte that contains an 8-bit unsigned integer that specifies the number of MDDI_Stb cycles that occur per reverse link data clock. The reverse link data clock is equal to the forward link data clock divided by two times the Reverse Rate Divisor. The reverse link data rate is related to the reverse link data clock and the Interface Type on the reverse link in the following manner:
 - o Interface Type 1 – reverse data rate = reverse link data clock.
 - o Interface Type 2 – reverse data rate = two times reverse link data clock.
 - o Interface Type 3 – reverse data rate = four times reverse link data clock.
 - o Interface Type 4 – reverse data rate = eight times reverse link data clock.
- **Turn-Around 1 Length** – Specifies the total number of bytes that are allocated for Turn-Around 1.
- **Turn-Around 2 Length** – Specifies the total number of bytes that are allocated for Turn-Around 2.
- **Parameter CRC** – Contain a 16-bit CRC of all bytes from the Packet Length to the Turn-Around Length. If this CRC fails to check then the entire packet shall be discarded
- **All Zero 1** – 8 bytes that each contain an 8-bit unsigned integer equal to zero. This field ensures that all MDDI_Data signals are at a logic-zero level for a sufficient time to allow the client to begin recovering clock using only MDDI_Stb prior to disabling the host's line drivers during the Turn-Around 1 field.
- **Turn-Around 1** – First turn-around period. The number of bytes specified by the Turn-Around 1 Length parameter is allocated to allow the MDDI_Data line drivers in the client to enable before the line drivers in the host are disabled. The client shall enable its MDDI_Data line drivers during bit 0 of Turn-Around 1 and the host shall disable its outputs and be completely disabled prior to the last bit of Turn-Around 1. The MDDI_Stb signal behaves as though MDDI_Data0 were at a logic-zero level during the entire Turn-Around 1 period.
- **Reverse Data Packets** – A series of data packets transferred from the client to host. The client may send filler packets or drive the MDDI_Data lines to a logic-zero level when it has no data to send to the host. If the MDDI_Data lines are driven to zero the host will interpret this as a packet with a zero length (not a valid length) and the host will accept no additional packets from the client for the duration of the current Reverse Link Encapsulation Packet.
- **Turn-Around 2** – The second turn-around period. The number of bytes is specified by the Turn-Around Length parameter. The host shall wait for at least the round trip delay time before it enables its MDDI_Data line drivers during Turn-Around 2. The host shall enable its MDDI_Data line drivers and be completely enabled prior to the last bit of Turn-Around 2 and the client shall disable its outputs and be completely disabled prior to the last bit of Turn-Around 2. The purpose of Turn-Around 2 is to allow the remaining amount of data from the Reverse Data Packets field to be transmitted from the client. Due to variations in different systems and the amount of safety margin allocated it is possible that neither the host nor client will be driving the MDDI_Data signals to a logic-zero level during some parts of the Turn-Around 2 field as seen by the line receivers at the host. The MDDI_Stb signal behaves as though MDDI_Data0 were at a logic-zero level during the entire Turn-Around 2 period.
- **All Zero 2** – 8 bytes that each contains an 8-bit unsigned integer equal to zero. This field ensures that all MDDI_Data signals are at a logic-zero level for a sufficient time to allow the client to begin recovering clock using both MDDI_Data0 and MDDI_Stb after enabling the host's line drivers following the Turn-Around 2 field.

6.3.3.6. Round-Trip Delay Measurement Packet

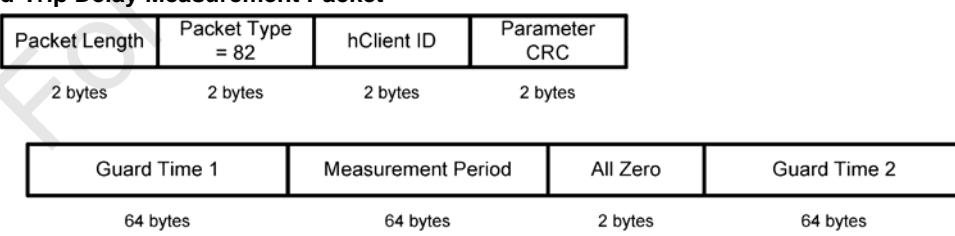


Figure 6.3.3.6.1 Round-Trip Delay Measurement Packet Format

The Round-Trip Delay Measurement Packet is used to measure the propagation delay from the host to the client plus the delay from the client back to the host. This measurement inherently includes all of the delays that exist in the line drivers and receivers and the interconnect subsystem. This measurement is used to set the turn around delay and reverse link rate divisor parameters in the Reverse Link Encapsulation Packet. This packet is most useful when the MDDI link is running at the maximum speed intended for a particular application. The packet may be sent in Type I mode and at a lower data rate to increase the range of the Round-Trip delay measurement.

Packet Contents:

- **Packet Length** – Specifies the total number of bytes in the packet not including the packet length field. The Packet Length is always 200.
- **Packet Type** – A Packet Type of 82=0x0052 identifies the packet as a Round-Trip Delay Measurement Packet.
- **hClient ID** – This field is reserved for future use and shall be set to zero.
- **Parameter CRC** – Contain a 16-bit CRC of all bytes from the Packet Length to the Packet Type. If this CRC fails to check then the entire packet shall be discarded.
- **Guard Time 1** – 64 bytes to allow the MDDI_Data line drivers in the client to enable before the line drivers in the host are disabled. The client shall enable its MDDI_Data line drivers during bit 0 of Guard Time 1 and the host shall disable its line drivers and be completely disabled prior to the last bit of Guard Time 1. The host and client shall both drive a logic zero level during Guard Time 1 when they are not disabled. Another purpose of this field is to ensure that all MDDI_Data signals are at a logic-zero level for a sufficient time to allow the client to begin recovering clock using only MDDI_Stb prior to disabling the host's line drivers.
- **Measurement Period** – a 64 byte window to allow the client to respond with two bytes of 0xff and 30 bytes of 0x00 at half the data rate used on the forward link. This rate corresponds to a Reverse Link Rate Divisor of 1. The client returns this response immediately at the time it perceives as the beginning of the Measurement Period. This response from the client will be received at the host at precisely the round trip delay of the link plus logic delay in the client after the beginning of the first bit of the Measurement Period at the host.
- **All Zero** – 2 bytes that each contains an 8-bit unsigned integer equal to zero. This field allows the MDDI_Data line drivers in the host and client to overlap so that MDDI_Data is always driven. The host shall enable its MDDI_Data line drivers during bit 0 of the All Zero field, and the client shall also continue to drive the signal to a logic-zero level as it did at the end of the Measurement Period.

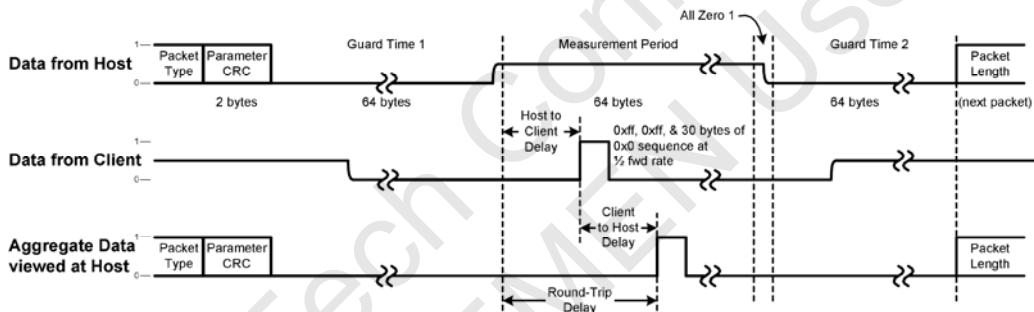


Figure 6.3.3.6.2 Round-Trip Delay Measurement Timing

Figure 6.2.3.6.2 illustrates the timing of events during the Round-Trip Delay Measurement Packet. The host transmits the Round-Trip Delay Measurement Packet and a delay is incurred before the packet reaches the client. As the client receives the packet it transmits the 0xff, 0xff, and 30 bytes of 0x00 pattern precisely at the beginning of the Measurement Period as detected by the client. The actual time the client begins to transmit this sequence is delayed from the beginning of the Measurement Period when viewed at the host. The amount of this delay is precisely the time it takes for the packet to propagate down the cable, through the line receivers and drivers in the client, and back through the cable to the host.

The host shall count the number of forward-link bit times from the start of the Measurement Period to the beginning of the 0xff, 0xff, and 30 bytes of 0x00 sequence. When a Type 2 – 4 reverse link is being used the host shall measure and save the round-trip delay value of all MDDI_Data pairs in case the data rate and round-trip delay skew are large enough to affect the arrival time if each bit differently.

The host and client both drive the line to a logic-zero level during both guard times to keep the MDDI_Data lines in a defined state. The enable and disable times of the host and client during both guard times are such that the MDDI_Data signals are always at a valid low for any valid round-trip delay time.

6.3.3.7. Register Access Packet

Packet Length	Packet Type = 146	bClient ID	Read/Write Info	Register Address	Parameter CRC	Register Data List	Register Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	Packet Length - 14 bytes	2 bytes

Figure 6.3.3.7. Register Access Packet Format

The Register Access Packet provides either the host or client with a means to access configuration and status registers in the opposite end of the MDDI link. The registers are likely to be unique for each display or device controller. These registers already exist in many displays that require setting configurations, modes of operation, and other useful and necessary settings. The Register Access Packet allows the MDDI host or client to both write to a register and request to read a register via the MDDI link. When the host or client requests to read a

register, the opposite end shall respond by sending the register data in the same packet type but indicating that this is the data read from a particular register with the use of the Read/Write Info field. The Register Access Packet may be used to read or write multiple registers by specifying a register count greater than 1. The client shall indicate its ability to support the Register Access Packet via bit 22 of Client Feature Capability Indicators field of the Client Capability Packet.

Packet Contents:

- **Packet Length** – Specifies the total number of bytes in the packet not including the packet length field.
- **Packet Type** – A Packet Type of 146=0x0092 identifies the packet as a Register Access Packet.
- **bClient ID** – This field is reserved for future use and shall be set to zero.
- **Read/Write Info** – Specifies the packet as either a write, or a read, or a response to a read, and provides a count of the data values.
 - o Bits [15:14] – Read/Write Flags
 - o Bits [13:0] – a 14-bit unsigned integer that specifies the number of 32-bit Register Data List items to be transferred in the Register Data List field.
 - o If bits [15:14] equal 00 then bits [13:0] specify the number of 32-bit register data items that are contained in the Register Data List field to be written to registers starting at the register specified by the Register Address field.
 - o If bits [15:14] equal 10 then bits [13:0] specify the number of 32-bit register data items that the receiving device shall send to the device requesting that the registers be read. The Register Data List field in this packet shall contain no items and is of zero length.
 - o If bits [15:14] equal 11 then bits [13:0] specify the number of 32-bit register data items that have been read from registers that are contained in the Register Data List field.
 - o Bits [15:14] shall not be equal to 01. This is not a valid value and is reserved for future use.
 - **Register Address** – Contains the register address that is to be written to or read from. For addressing registers whose addressing is less than 32 bits, the upper bits shall be set to zero.
 - **Parameter CRC** – 2 bytes that contain a 16-bit CRC of all bytes from the Packet Length to the Register Address. If this CRC fails to check then the entire packet shall be discarded.
 - **Register Data List** – a list of 4-byte register data values to be written to client registers or values that were read from client device registers.
 - **Register Data CRC** – 2 bytes that contain a 16-bit CRC of only the Register Data List. If this CRC fails to check then the Register Data may still be used but the CRC error count shall be incremented.

6.3.3.8. Client Request and Status Packet

Packet Length	Packet Type = 70	cClient ID	Reverse Link Request	CRC Error Count	Client Status	Client Busy Flags	CRC
2 bytes	2 bytes	2 bytes	2 bytes	1 byte	1 byte	2 bytes	2 bytes

Figure 6.3.3.8. Client Request and Status Packet Format

The host needs a small amount of information from the client so it can configure the host-to-client link in an optimum manner. It is recommended that the client send one Client Request and Status Packet to the host each sub-frame. It is recommended that the client send this packet as the first packet in the Reverse Link Encapsulation Packet to ensure that it is delivered reliably to the host, and it is required when requested by the host via the Reverse Link Flags in the Reverse Link Encapsulation Packet. The Client Request and Status Packet is required to report errors and status to the host. For external mode every host shall be able to receive this packet, and every client shall be able to send this packet. It is highly recommended that internal mode hosts and clients also support this packet, but it is not required.

Packet Contents:

- **Packet Length** – Specifies the total number of bytes in the packet not including the packet length field. The Packet Length is always 12.
- **Packet Type** – A Packet Type of 70=0x0046 identifies the packet as a Client Request and Status Packet.
- **cClient ID** – This field is reserved for future use and shall be set to zero.
- **Reverse Link Request** – Specifies the number of bytes the client needs in the reverse link in the next sub-frame to send information to the host.
- **CRC Error Count** – Indicates the number of CRC errors that have occurred since the last Client Request and Status Packet was sent by the client. The CRC count is reset each time a Client Request and Status Packet is sent. If the actual number of CRC errors exceeds

255 then this value saturates at 255.

- **Client Status** – Contains a group of flags that indicate the current status of the client device.
 - Bit 0 – Indicates that there has been a change in the capability of the client. This could be due to the user connecting a peripheral device such as a microphone, keyboard, or display, or some other reason.
 - Bit 0 = 1 – capability has changed. Examine the Client Capability Packet to determine the new client characteristics.
 - Bit 0 = 0 – capability has not changed since the last Client Capability Packet was sent.
 - Bit 1 – Indicates that the client device has detected an error in processing a packet since the last Client Capability Packet was sent. Implementation of this bit is optional in the client device. Additional information about the error may be provided via other means, such as the Client Error Report Packet or via a Register Access Packet.
 - Bits [7:2] – reserved for future use and shall be set to zero.
- **Client Busy Flags** – Indicate that the client is performing a specific function and is not ready to accept another packet related to that function. A bit set to one indicates that the particular function is currently being performed by the client and that the related function in the client is busy. If the related function in the client is ready the bit shall be zero. The client shall always return a busy status (bit set to one) for all functions that are not supported in the client.
 - Bit 0 – bitmap block transfer function is busy.
 - Bit 1 – bitmap area fill function is busy.
 - Bit 2 – bitmap pattern fill function is busy.
 - Bit 3 – the graphics subsystem is busy performing an operation that requires use of the frame buffer in the client. Other graphics functions that require use of the frame buffer may not begin until this bit is set to one.
 - Bits [15:4] – reserved for future use and shall be set to one to indicate busy status in case these bits are assigned in a future version of this standard.
- **CRC** – 2 bytes that contain a 16-bit CRC of all bytes in the packet including the Packet Length.

6.3.3.9. Client Capability Packet

Packet Length	Packet Type = 66	cClient ID	Protocol Version	Min Protocol Version	Pre-calibration Data Rate Capability	Interface Type Capability
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	1 byte
Number of Alt Displays	Post-calibration Data Rate Capability	Bitmap Width	Bitmap Height	Display Window Width	Display Window Height	Color Map Size
1 byte	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	4 bytes
Color Map RGB Width	RGB Capability	Monochrome Capability	Reserved 1	Y Cb Cr Capability	Bayer Capability	Reserved 2
2 bytes	2 bytes	1 byte	1 byte	2 bytes	2 bytes	2 bytes
Client Feature Capability	Max Video Frame Rate	Min Video Frame Rate	Min Sub-frame rate	Audio Buffer Depth	Audio Channel Capability	Audio Sample Rate Capability
4 bytes	1 byte	1 byte	2 bytes	2 bytes	2 bytes	2 bytes
Audio Sample Resolution	Mic Sample Resolution	Mic Sample Rate Capability	Keyboard Data Format	Pointing Device Data Format	Content Protection Type	Mfr Name
1 byte	1 byte	2 bytes	1 byte	1 byte	2 bytes	2 bytes
Product Code	Reserved 3	Serial Number	Week of Mfr	Year of Mfr	CRC	
2 bytes	2 bytes	4 bytes	1 byte	1 byte	2 bytes	

Figure 6.3.3.9. Client Capability Packet Format

The host needs to know the capability of the client so it can configure the host-to-client link in an optimum manner. It is recommended that the client send a Client Capability Packet to the host after forward link synchronization is acquired, and it is required when requested by the host via the Reverse Link Flags in the Reverse Link Encapsulation Packet. The Client Capability Packet is required to inform the host of the capabilities of the client. For External Mode every host shall be able to receive this packet, and every client shall be able to send this

packet. Implementation of this packet is optional for Internal Mode.

Packet Contents:

- **Packet Length** – Specifies the total number of bytes in the packet not including the packet length field.
- **Packet Type** – A Packet Type of 66=0x0042 identifies the packet as a Client Capability Packet.
- **cClient ID** – This field is reserved for future use and shall be set to zero.
- **Protocol Version** – Specifies the protocol version used by the client. The present protocol version shall be set to 2.
- **Minimum Protocol Version** – Specifies the minimum protocol version that the client can interpret. Zero is an invalid value.
- **Pre-Calibration Data Rate Capability** – Specifies the maximum data rate the client can receive on each data pair on the forward MDDI link prior to performing forward link skew calibration. The rate is specified as the number of million bits per second (Mbps).
- **Interface Type Capability** – Specifies the interface types that are supported on the forward and reverse links. A bit set to 1 indicates that the specified interface type is supported, and a bit set to 0 indicates that the specified type is not supported. All hosts and clients shall support at least Type 1 on the forward and reverse link. It is not required to support a contiguous range of interface types. For example, it is valid to support only Type 1 and Type 3, and not Type 2 and Type 4. The forward and reverse links are not required to operate with the same interface type except when the link comes out of hibernation where both forward and reverse shall operate in Type 1 mode.
 - Bit 0 – Client can function in Type 2 (2-bit) mode on the forward link.
 - Bit 1 – Client can function in Type 3 (4-bit) mode on the forward link.
 - Bit 2 – Client can function in Type 4 (8-bit) mode on the forward link.
 - Bit 3 – Client can function in Type 2 (2-bit) mode on the reverse link.
 - Bit 4 – Client can function in Type 3 (4-bit) mode on the reverse link.
 - Bit 5 – Client can function in Type 4 (8-bit) mode on the reverse link.
 - Bits [7:6] are reserved and shall be set to zero.
- **Number of Alt Displays** – Specifies the number of alternate displays supported by the MDDI client. This value is zero in OTM9608A.
- **Post-Calibration Data Rate Capability** – Specifies the maximum data rate the client can receive on each data pair on the forward MDDI link after performing forward link skew calibration. The rate is specified as the number of million bits per second (Mbps). If the client device does not support the Forward Link Skew Calibration Packet then this field shall be set to zero.
- **Bitmap Width** – Specifies the width of the bitmap expressed as a number of pixels.
- **Bitmap Height** – Specifies the height of the bitmap expressed as a number of pixels.
- **Display Window Width** – Specifies the width of the display window expressed as a number of pixels. Often this will have the same value as the Bitmap Width.
- **Display Window Height** – Specifies the height of the display window expressed as a number of pixels. Often this will have the same value as the Bitmap Height.
- **Color Map Size** – Specifies the maximum number of table items that exist in the color map table in the client. OTM9608A cannot use the color map format then this value is zero.
- **Color Map RGB Width** – Specifies the number of bits of the red, green, and blue color components that can be displayed in the color map (palette) display mode. OTM9608A cannot use the color map (palette) format then this value is zero.
- **RGB Capability** – Specifies the number of bits of resolution that can be displayed in RGB format. If the client cannot use the RGB format then this value is zero. The RGB Capability word is composed of three separate unsigned values:
 - Bits [3:0] define the maximum number of bits of blue (the blue intensity) in each pixel.
 - Bits [7:4] define the maximum number of bits of green (the green intensity) in each pixel.
 - Bits [11:8] define the maximum number of bits of red (the red intensity) in each pixel.
 - Bits [13:12] are reserved for future use and shall be set to zero.
 - Bit 14 is equal to zero this indicates that the client cannot accept RGB pixel data in unpacked format.
 - Bit 15 when set to one indicates that the client can accept RGB pixel data in packed format. If bit 15 is equal to zero this indicates that the client cannot accept RGB pixel data in packed format.
- **Monochrome Capability** – Specifies the parameter of monochrome format. OTM9608A cannot use this format then the value is zero.
- **Reserved 1** – 1 byte that contains an 8-bit unsigned integer that is reserved for future use. All bits in this field shall be set to zero.
- **YCbCr Capability** – Specifies the parameter of YCbCr format. OTM9608A cannot use the YCbCr format then this value is zero.
- **Bayer Capability** – Specifies the parameter of Bayer format. OTM9608A cannot use the Bayer format then this value is zero.
- **Reserved 2** – 2 bytes that contain a 16-bit unsigned integer that is reserved for future use. All bits in this field shall be set to zero.

- **Client Feature Capability Indicators** – Contains a set of flags that indicate the whether specific features in the client are supported. A bit set to one indicates the capability is supported, and a bit set to zero indicates the capability is not supported.
 - Bit 0 – the Bitmap Block Transfer Packet (packet type 71) is supported
 - Bit 1 – the Bitmap Area Fill Packet (packet type 72) is supported.
 - Bit 2 – the Bitmap Pattern Fill Packet (packet type 73) is supported.
 - Bit 3 – the Read Frame Buffer Packet (packet type 74) is supported.
 - Bit 4 – the client has the capability to support the Transparent Color and Mask Setup Packet.
 - Bit 5 – the client can accept audio data in unpacked format.
 - Bit 6 – the client can accept audio data in packed format.
 - Bit 7 – the client can send a reverse-link video stream from a camera.
 - Bit 8 – the client has the ability to receive a full line of pixel data.
 - Bit 9 – the client has the ability to respond to the Display Power State Packet.
 - Bit 10 – the client has the ability to support display power state 01.
 - Bit 11 – the client is communicating with a pointing device and can send and receive Pointing Device Data Packets.
 - Bit 12 – the client is communicating with a keyboard and can send and receive Keyboard Data Packets.
 - Bit 13 – the client has the ability to set one or more audio or video parameters by supporting the VCP Feature packets.
 - Bit 14 – the client has the ability to write pixel data into the offline display frame buffer.
 - Bit 15 – the client has the ability to write pixel data into only the display frame buffer currently being used to refresh the display image.
 - Bit 16 – the client has the ability to write pixel data from a single Video Stream Packet into all display frame buffers.
 - Bit 17 – the client has the ability to respond to the Request Specific Status Packet.
 - Bit 18 – the client has the ability to respond to the Round-Trip Delay Measurement Packet.
 - Bit 19 – the client has the ability to respond to the Forward Link Skew Calibration Packet.
 - Bit 20 – the client has the ability to interpret the Request Specific Status Packet and respond with the Valid Status Reply List Packet.
 - Bit 21 – the client has the ability to use the Raster Operation field of the Bitmap Block Transfer Packet (packet type 71).
 - Bit 22 – the client has the ability to respond to the Register Access Packet
 - Bits [31:23] – reserved for future use, shall be set to zero.
- **Maximum Video Frame Rate Capability** – Specifies the maximum video frame update capability of the client in frames per second. The host may choose to update the image at a rate less than or equal to the value specified in this field.
- **Minimum Video Frame Rate Capability** – Specifies the minimum video frame update capability of the client in frames per second.
- **Minimum Sub-frame Rate** – Specifies the minimum sub-frame rate in frames per second.
- **Audio Buffer Depth** – OTM9608A can not support Audio function then this value is zero.
- **Audio Channel Capability** – OTM9608A can not support Audio function then this value is zero.
- **Audio Sample Rate Capability (forward link)** – OTM9608A can not support Audio function then this value is zero.
- **Audio Sample Resolution (forward link)** – OTM9608A can not support Audio function then this value is zero.
- **Mic Audio Sample Resolution (reverse link)** – OTM9608A can not support Audio function then this value is zero.
- **Mic Sample Rate Capability (reverse link)** – OTM9608A can not support Audio function then this value is zero.
- **Keyboard Data Format** – OTM9608A can not support Audio function then this value is zero.
- **Pointing Device Data Format** – OTM9608A can not support Audio function then this value is zero.
- **Content Protection Type** – OTM9608A can not support Audio function then this value is zero.
- **Mfr Name** – 2 bytes that form a 16-bit value that contains the EISA 3-character ID of the manufacturer, packed into three 5-bit characters in the same manner as in the VESA EDID specification. The character 'A' is represented as 00001 binary, the character 'Z' is represented as 11010 binary, and all letters between 'A' and 'Z' are represented as sequential binary values that correspond to the alphabetic sequence between 'A' and 'Z'. The most significant bit of the Mfr Name field is unused and shall always be zero. Example: a manufacturer represented by the string "XYZ" would have a Mfr Name value of 0x633a. If this field is not supported by the client it shall be set to zero.
- **Product Code** – 2 bytes that contain a 16-bit unsigned integer that contains a product code assigned by the display manufacturer. If this field is not supported by the client it shall be set to zero.
- **Reserved 3** – 2 bytes that contain a 16-bit unsigned integer that is reserved for future use.
- **Serial Number** – 4 bytes that contain a 32-bit unsigned integer that specifies the serial number of the display in numeric form. If this field is not supported by the client it shall be set to zero.

- Week of Manufacture – 1 byte that contains an 8-bit unsigned integer that defines the week of manufacture of the display. This value shall be in the range of 1 to 53 if it is supported by the client. If this field is not supported by the client it shall be set to zero.
- Year of Manufacture – 1 byte that contains an 8-bit unsigned integer that defines the year of manufacture of the display. This value is an offset from the year 1990. Years in the range of 1991 to 2245 can be expressed by this field. Example: the year 2003 corresponds to a Year of Manufacture value of 13. If this field is not supported by the client it shall be set to zero.
- CRC – 2 bytes that contain a 16-bit CRC of all bytes in the packet including the Packet Length.

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6.3.4. Hibernation / Wake-up

6.3.4.1. Hibernation state

This IC support hibernation mode to save interface power consumption. MDDI link can enter the hibernation state quickly and wake up from hibernation quickly. This allows the system to force MDDI link into hibernation frequently to save power consumption.

During hibernation mode, the hi-speed transmitters and receivers are disabled and the low-speed & low-power receivers are enabled in order to detect wake-up sequence.

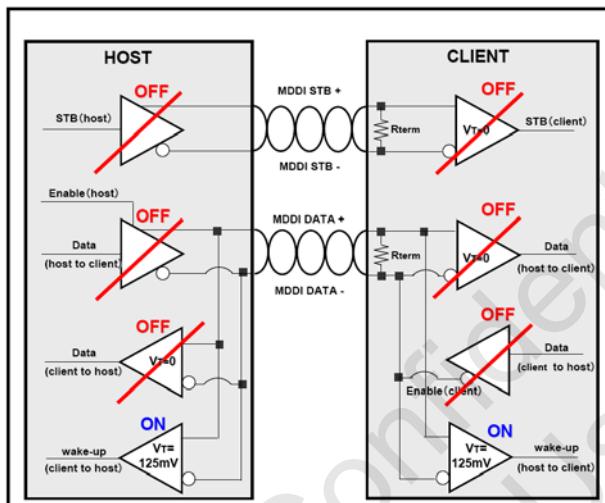


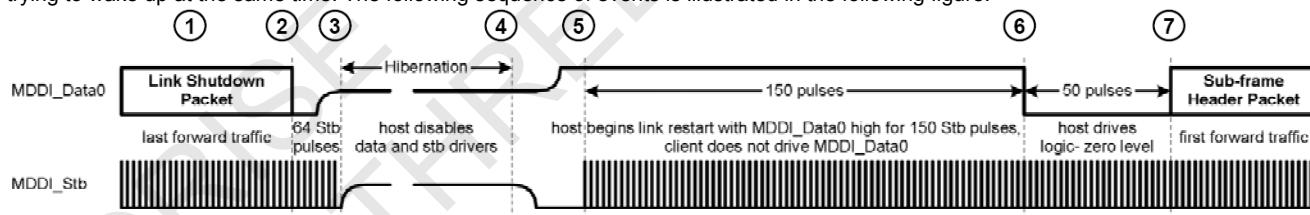
Figure 6.3.4.1. MDDI transceiver / receiver state in hibernation

When the link wakes up from hibernation, the host and client exchange a sequence of pulses. These pulses can be detected using low-speed, low-power receivers that consume only a fraction of the current of the differential receivers required to receive the signals at the maximum link operating speed.

Either the client or the host can wake up the link; Host-initiated link wakeup and Client-initiated link wakeup.

6.3.4.2. Host-Initiated Wake-up from Hibernation

A. Host-initiated Link Wake-up Procedure The simple case of a host-initiated wake-up is described below without contention from the client trying to wake up at the same time. The following sequence of events is illustrated in the following figure.



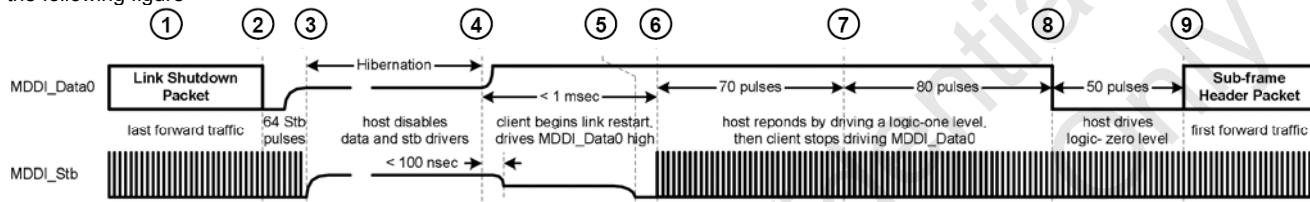
The Detailed descriptions for labeled events are as follows:

- ①. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low- power hibernation state.
- ②. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_Data to a logic-zero level, and then disables the MDDI_Data output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point 3.
- ③. The host enters the low-power hibernation state by disabling the MDDI_Data and MDDI_Stb drivers and by placing the host controller into a low-power hibernation state. It is also allowable for MDDI_Stb to be driven to logic-zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.
- ④. After a while, the host begins the link restart sequence by enabling the MDDI_Data and MDDI_Stb driver outputs. The host drives MDDI_Data to a logic-one level and MDDI_Stb to logic- zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200n sec after MDDI_Data reaches a valid logic-one level and MDDI_Stb reaches a valid logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb. The client first detects the wake-up pulse using a low-power differential receiver having a +125mV input offset voltage.

- ⑤. The host drivers are fully enabled and MDDI_Data is being driven to a logic-one level. The host begins to toggle MDDI_Stb in a manner consistent with having logic-zero level on MDDI_Data for duration of 150 MDDI_Stb cycles.
- ⑥. The host drives MDDI_Data to logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data is at logic-zero level for 40 MDDI_Stb cycles.
- ⑦. The host begins to transmit data on the forward link by sending a Sub-frame Header Packet. Beginning at point 7. The MDDI host generates MDDI_Stb based on the logic level on MDDI_Data so that proper data-strobe encoding commences from point 7.

6.3.4.3. Client-Initiated Wake-up from Hibernation

B. Client-initiated Link Wake-up Procedure An example of a typical client-initiated service request event with no contention is illustrated in the following figure



The Detailed descriptions for labeled events are as follows:

- ①. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.
- ②. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_Data to a logic-zero level, and then disables the MDDI_Data output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point 3.
- ③. The host enters the low-power hibernation state by disabling its MDDI_Data and MDDI_Stb driver outputs. It is also allowable for MDDI_Stb to be driven to logic-zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.
- ④. After a while, the client begins the link restart sequence by enabling the MDDI_Stb receiver and also enabling an offset in its MDDI_Stb receiver to guarantee the state of the received version of MDDI_Stb is a logical-zero level in the client before the host enables its MDDI_Stb driver. The client will need to enable the offset in MDDI_Stb immediately before enabling its MDDI_Stb receiver to ensure that the MDDI_Stb receiver in the client is always receiving a valid differential signal and to prevent erroneous received signals from propagating into the client. After that, the client enables its MDDI_Data driver while driving MDDI_Data to a logic-one level. It is allowed for MDDI_Data and MDDI_Stb to be enabled simultaneously if the time to enable the offset and enable the standard MDDI_Stb differential receiver is less than 200n sec.
- ⑤. Within 1m sec the host recognizes the service request pulse (TE), and the host begins the link restart sequence by enabling the MDDI_Data and MDDI_Stb driver outputs. The host drives MDDI_Data to a logic-one level and MDDI_Stb to a logical-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200n sec after MDDI_Data reaches a valid logic-one level and MDDI_Stb reaches a valid fully-driven logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb.
- ⑥. The host begins outputting pulses on MDDI_Stb and shall keep MDDI_Data at a logic-one level for a total duration of 150 MDDI_Stb pulses through point 8. The host generates MDDI_Stb in a manner consistent with sending a logical-zero level on MDDI_Data. When the client recognizes the first pulse on MDDI_Stb it shall disable the offset in its MDDI_Stb receiver.
- ⑦. The client continues to drive MDDI_Data to a logic-one level for 70 MDDI_Stb pulses, and the client disables its MDDI_Data driver at point 7. The host continues to drive MDDI_Data to a logic-one level for duration of 80 additional MDDI_Stb pulses, and at point 8 drives MDDI_Data to logic-zero level.
- ⑧. The host drives MDDI_Data to logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data is at logic-zero level for 40 MDDI_Stb cycles.
- ⑨. After asserting MDDI_Data to logic-zero level and driving MDDI_Stb for duration of 50 MDDI_Stb pulses the host begins to transmit data on the forward link at point 9 by sending a Sub-frame Header Packet. The client begins to look for the Sub-frame Header Packet after MDDI_Data is at logic-zero level for 40 MDDI_Stb cycles.

6.4. RGB Interface

The OTM9608A support RGB interface Mode 1 and Mode 2. The interface signals as shown in table 6.3.1.

The Mode 1 and Mode 2 function is select by setting in the Command 2, please reference application note.

In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D[23:0]), when DE is high state. The external clocks (PCLK, VS and HS) are used for internal displaying clock. So, controller must always transfer PCLK, VS and HS signal to OTM9608A.

In RGB Mode 2, back porch of Vsync is defined by VBP[5:0] of RGBPRCTR command. And back porch of Hsync is defined by HBP[5:0] of RGBPRCTR command. Front porch of Vsync is defined by VFP[5:0] of RGBPRCTR command. And front porch of Hsync is defined by HFP[5:0] of RGBPRCTR command.

RGB I/F Mode	PCLK	DE	VS	HS	DB[23:0]	SHUT	Register for Blanking Porch setting (Register 0x3Bh, 2 nd ~5 th Parameters)
RGB Mode 1	Used	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used	Used

Symbol	name	Description
PCLK	Pixel clock	Pixel clock for capturing pixels at display interface
HS	Horizontal sync	Horizontal synchronization timing signal
VS	Vertical sync	Vertical synchronization timing signal
DE	Data enable	Data enable signal (assertion indicates valid pixels)
D[23:0],	Pixel data	Pixel data in 16-bit, 18-bit and 24-bit format
SHUT	Shutdown	Control pin to shut down display ("1"=Shutdown)

Table 6.4. The interface signals of RGB interface

6.4.1. RGB interface color mapping format

The OTM9608A implement a 16-bit, 18-bit and 24 bit pixel-data bus width. The selection of this pixel-data bus width is VIPF [3:0] in the command (3Ah). The interface color mapping of RGB interface are given in Table 6.4.1.

Table 6.4.1. The interface color mapping of DPI interface

Pad name	24 bits configuration VIPF[3:0] = 0111	18 bits configuration VIPF[3:0] = 0110	16 bits configuration VIPF[3:0] = 0101
D23	R7	Not used	Not used
D22	R6	Not used	Not used
D21	R5	R5	Not used
D20	R4	R4	R4
D19	R3	R3	R3
D18	R2	R2	R2
D17	R1	R1	R1
D16	R0	R0	R0
D15	G7	Not used	Not used
D14	G6	Not used	Not used
D13	G5	G5	G5
D12	G4	G4	G4
D11	G3	G3	G3
D10	G2	G2	G2
D9	G1	G1	G1
D8	G0	G0	G0
D7	B7	Not used	Not used
D6	B6	Not used	Not used

D5	B5	B5	Not used
D4	B4	B4	B4
D3	B3	B3	B3
D2	B2	B2	B2
D1	B1	B1	B1
D0	B0	B0	B0

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6.4.2. RGB Timing parameter

In the RGB interface, the frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

Vsync (VS) indicates the beginning of each frame of the displayed image.

Hsync (HS) signals the beginning of each horizontal line of pixels.

Each pixel value (16-, 18-, or 24-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data.

Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.

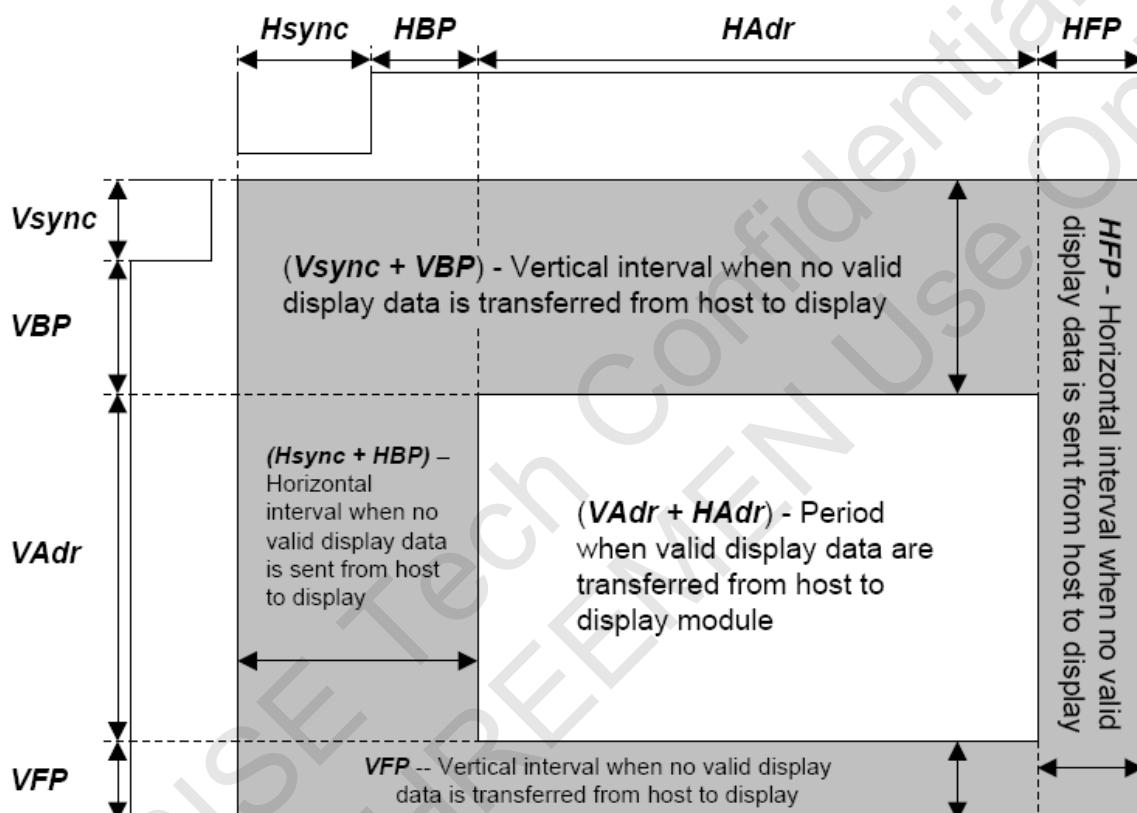


Figure 6.4.2.1 define timing parameter for RGB operation.

Table 6.4.2.2 provide the timing parameter for support display resolution.

Table 6.4.2.2 540horizontal x 960 vertical display timing parameter

Parameters	Symbols	Min.	Typ	Max.	Unit
PCLK Frequency	F_{PCLK}	-	35.5	-	MHz
Horizontal Synchronization	Hsync	4	10	63	PCLK
Horizontal Back Porch	HBP	4	20	63	PCLK
Horizontal Address (Display area)	HAdr	-	540	-	PCLK
Horizontal Front Porch	HFP	32	40	63	PCLK
Horizontal cycle	---	-	610	729	PCLK
Vertical Synchronization	Vsync	1	2	63	Line
Vertical Back Porch	VBP	4	4	63	Line
Vertical Address (Display area)	VAdr	-	960	-	Line
Vertical Front Porch	VFP	4	4	63	Line
Vertical cycle	---	-	970	1023	Line

6.4.3. RGB interface power on/off sequence

The RGB interface control the normal/shutdown mode by the SHUT pin, the on/off sequence as shown in figure.

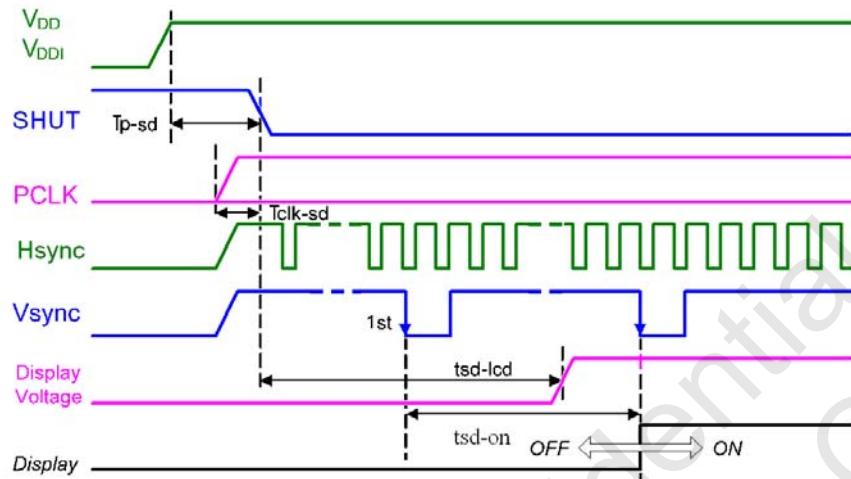


Figure 6.4.3.1 Power on and shutdown recovery sequence.

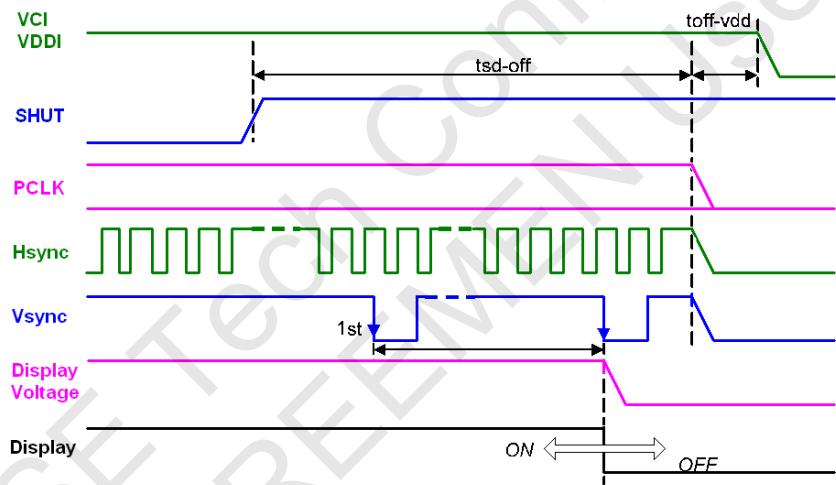


Figure 6.4.3.2 Power off and shutdown sequence.

Table 6.4.3 540 horizontal x 960 vertical display timing parameter

Parameters	Symbols	Min.	Typ	Max.	Unit
V _{DD} /V _{DDI} -on to falling edge of SHUT	Tp-sd	5	10	-	ms
PCLK input to the falling edge of SHUT	Tclk-sd	1	-	-	PCLK
Falling edge of SHUT to display voltage ready	Tsd-lcd	-	3	-	Frame
Falling edge of SHUT to display on	Tsd-on	-	2	-	Frame
Rising edge of SHUT to display off	tsd-off	-	5	-	Frame
Input-signal-off- to V _{DD} /V _{DDI} -off	toff-vdd	0	1	-	us

6.5. MPU-Series Parallel Interface

The MCU uses a 28-wires 24-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write, RDX is the parallel data read and D[23:0] is parallel data.

The Graphics Controller Chip reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[23:0] bits are display RAM data or command parameters. When D/CX='0', D[23:0] bits are commands.

The 8080-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. The selection of this interface is done when IM[3:0] = 0b0000.

6.5.1. Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (DCX, RDX, WRX) and data signals (DB[23:0]). DCX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low ('=0') and vice versa it is data ('=1').

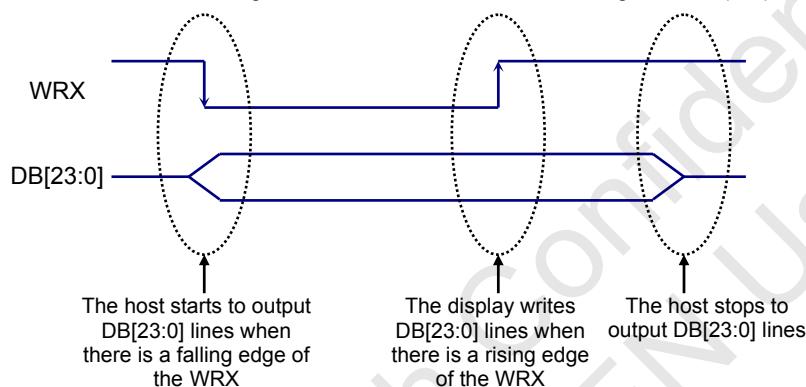


Fig. 6.5.1.1 8080-Series WRX Protocol

Note: WRX is an unsynchronized signal (It can be stopped)

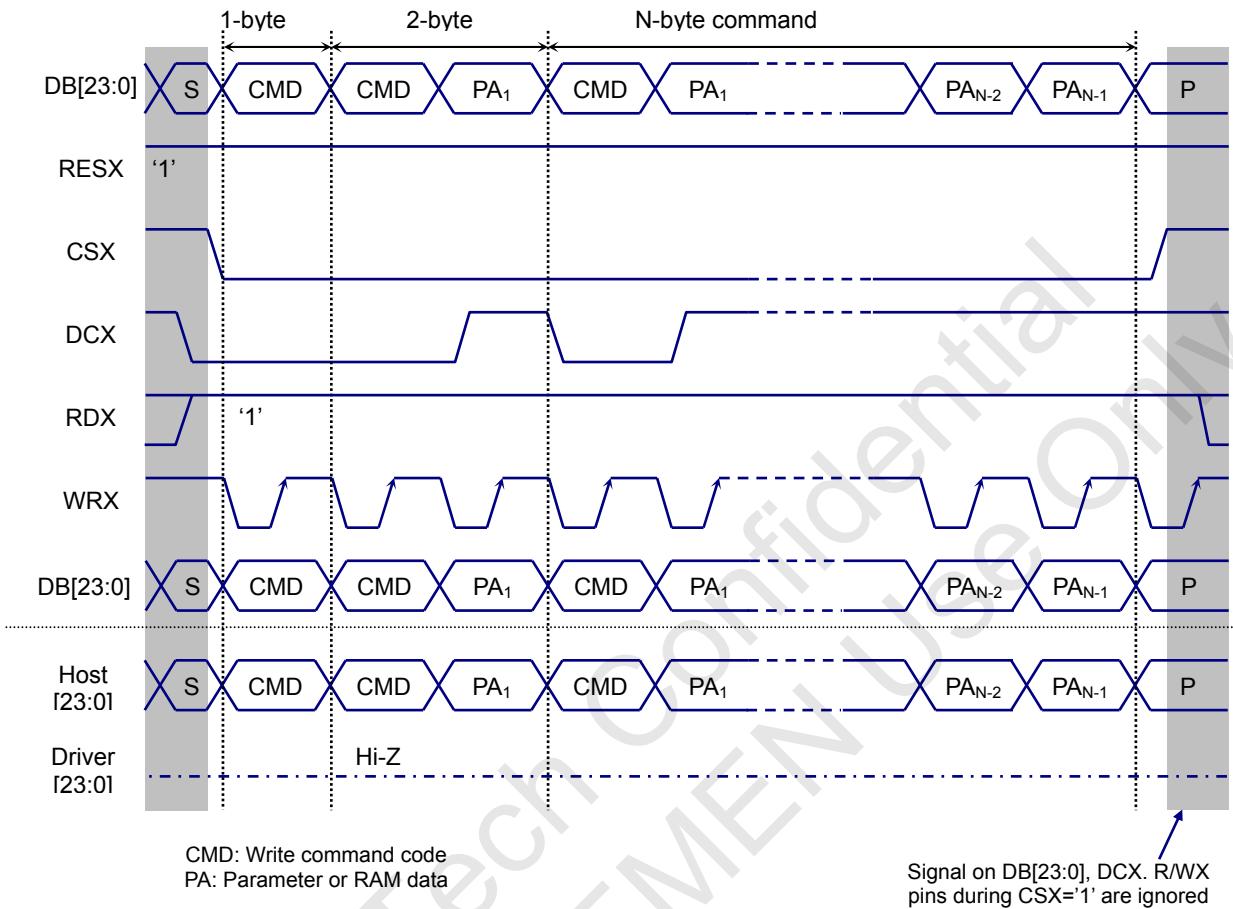


Fig. 6.4.1.2 8080-Series parallel bus protocol, Write to register or display RAM

6.5.2. Read cycle sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The display sends data (DB[23:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

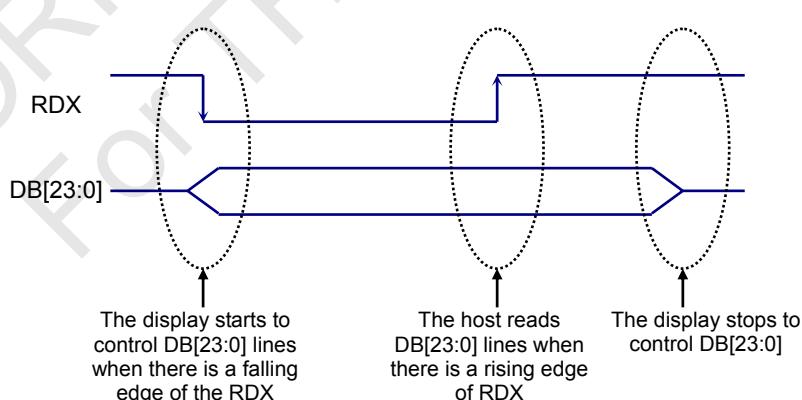


Fig. 6.5.2.1 8080-Series RDX Protocol

Note: RDX is an unsynchronized signal (It can be stopped)

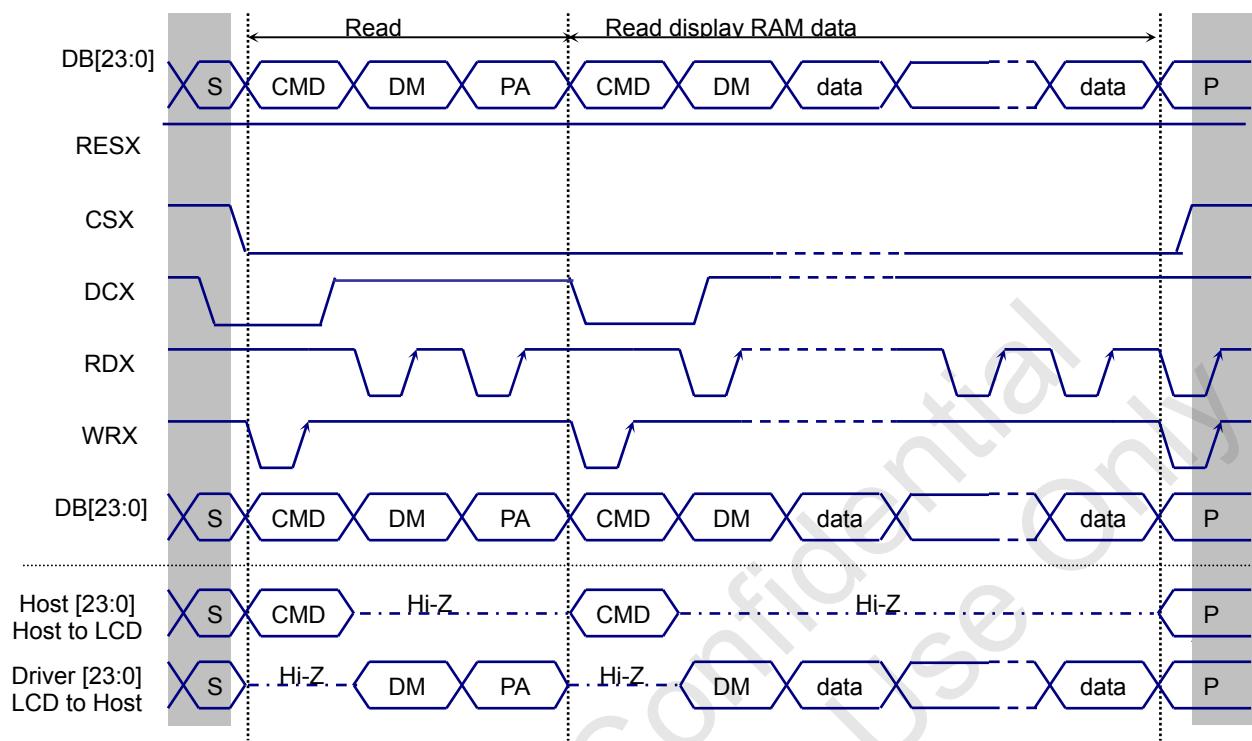


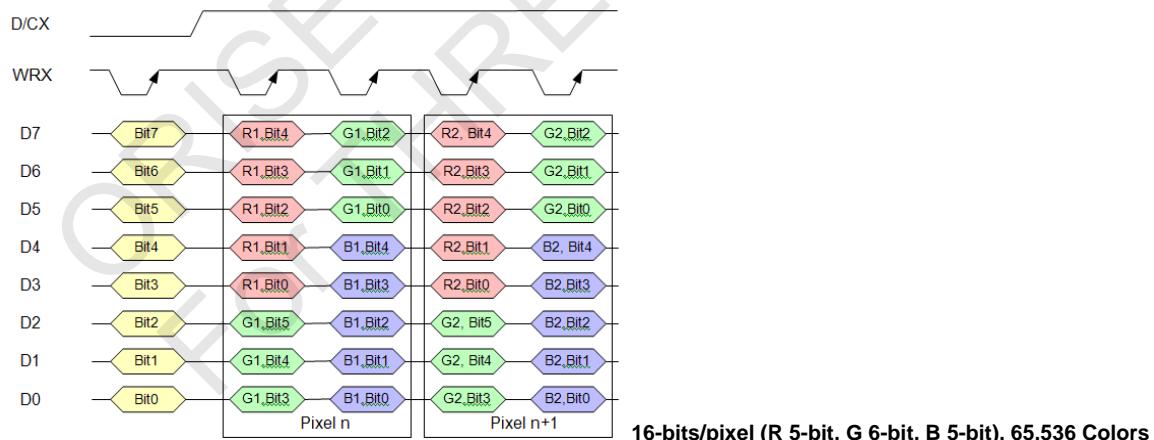
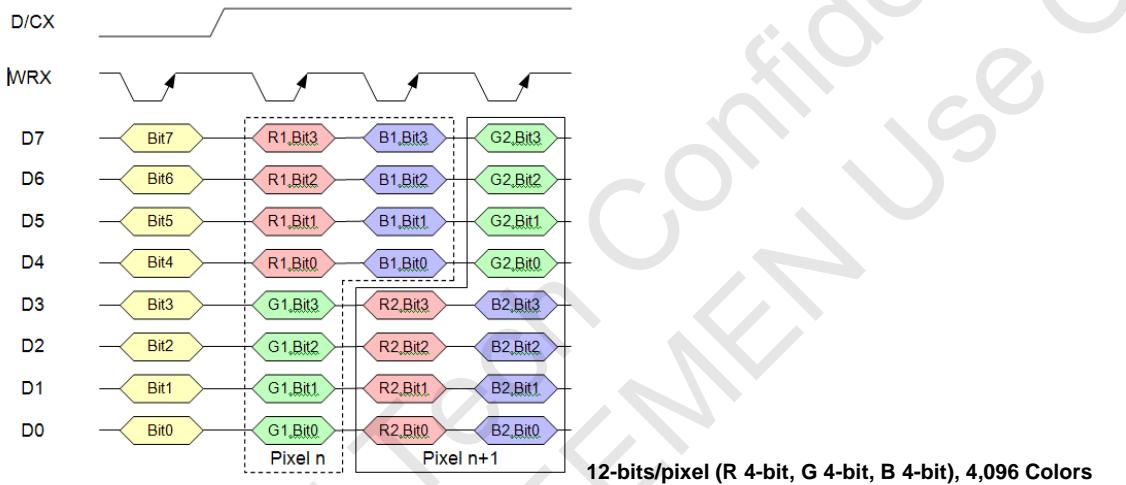
Fig. 6.5.2.2 8080-Series parallel bus protocol, Read data from register or display RAM

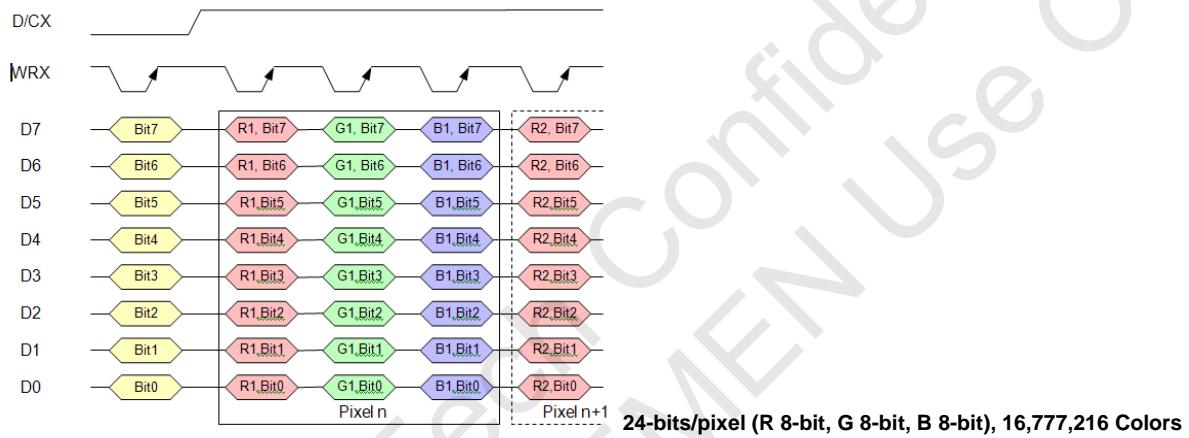
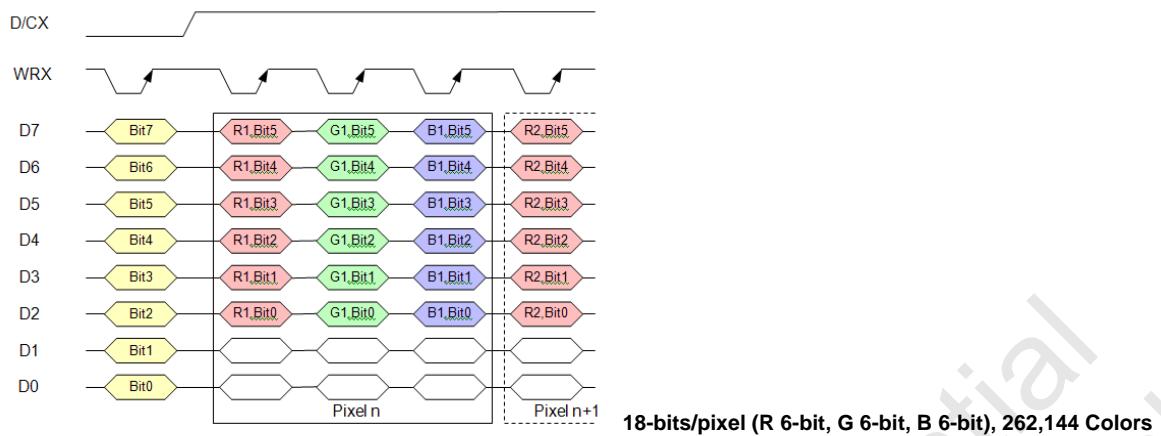
6.5.3. MPU mode color coding

Color coding uses a red [R], green [G] and blue [B] additive color mixing method. R, G and B are used for each color data index in the following sections.

6.5.3.1. 8-bit Interface color coding

BUS	COLOR	D7	D6	D5	D4	D3	D2	D1	D0
8	444	R1[3]	R1[2]	R1[1]	R1[0]	G1[3]	G1[2]	G1[1]	G1[0]
		B1[3]	B1[2]	B1[1]	B1[0]	R2[3]	R2[2]	R2[1]	R2[0]
		G2[3]	G2[2]	G2[1]	G2[0]	B2[3]	B2[2]	B2[1]	B2[0]
	565	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[5]	G1[4]	G1[3]
		G1[2]	G1[1]	G1[0]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]
	666	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	X	X
		G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	X	X
		B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	X	X
	888	R1[7]	R1[6]	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]
		G1[7]	G1[6]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]
		B1[7]	B1[6]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]





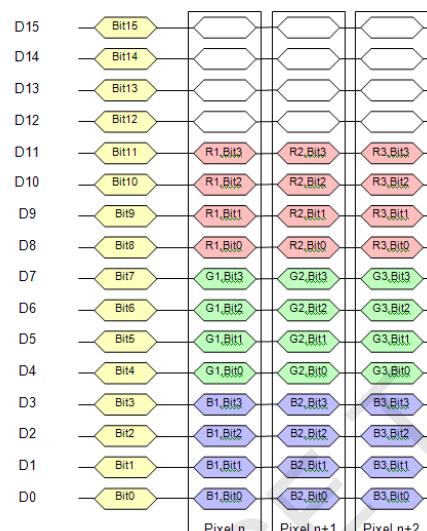
6.5.3.2. 16-bit Interface color coding

444	X	X	X	X	R1[3]	R1[2]	R1[1]	R1[0]	G1[3]	G1[2]	G1[1]	G1[0]	B1[3]	B1[2]	B1[1]	B1[0]
565	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]
666 OPT1	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	X	X	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	X	X
666 OPT1	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	X	X	R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]	X	X
666 OPT2	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]	X	X	B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]	X	X
888 OPT1	X	X	X	X	X	X	X	X	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	X	X
888 OPT1	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	X	X	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	X	X
888 OPT1	R1[7]	R1[6]	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[7]	G1[6]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]
888 OPT1	B1[7]	B1[6]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	R2[7]	R2[6]	R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]
888 OPT2	G2[7]	G2[6]	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]	B2[7]	B2[6]	B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]
888 OPT2	X	X	X	X	X	X	X	X	R1[7]	R1[6]	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]
888 OPT2	G1[7]	G1[6]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	B1[7]	B1[6]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]

D/CX



WRX

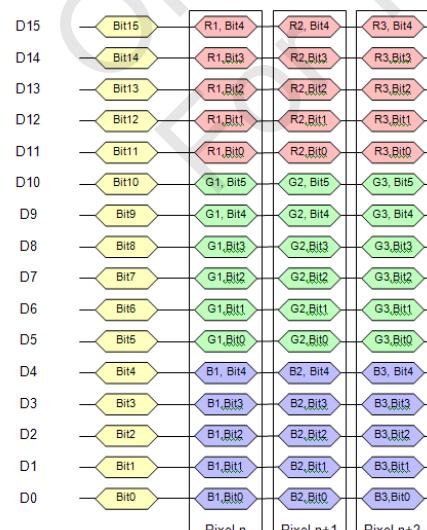



12-bits/pixel (R 4-bit, G 4-bit, B 4-bit), 4,096 Colors

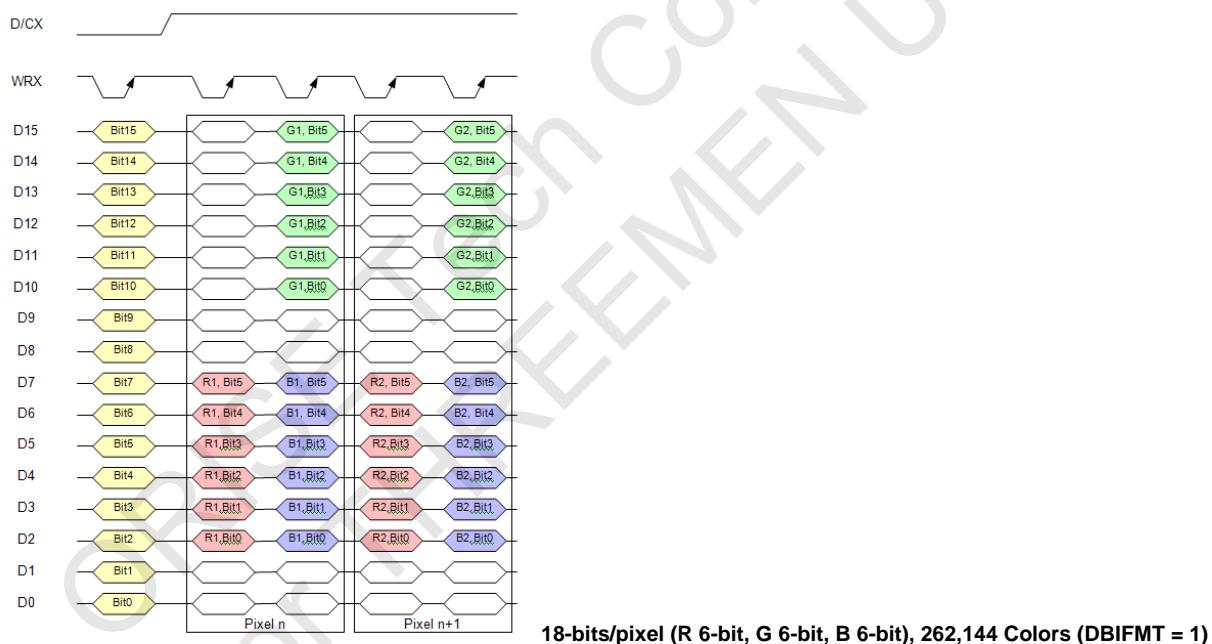
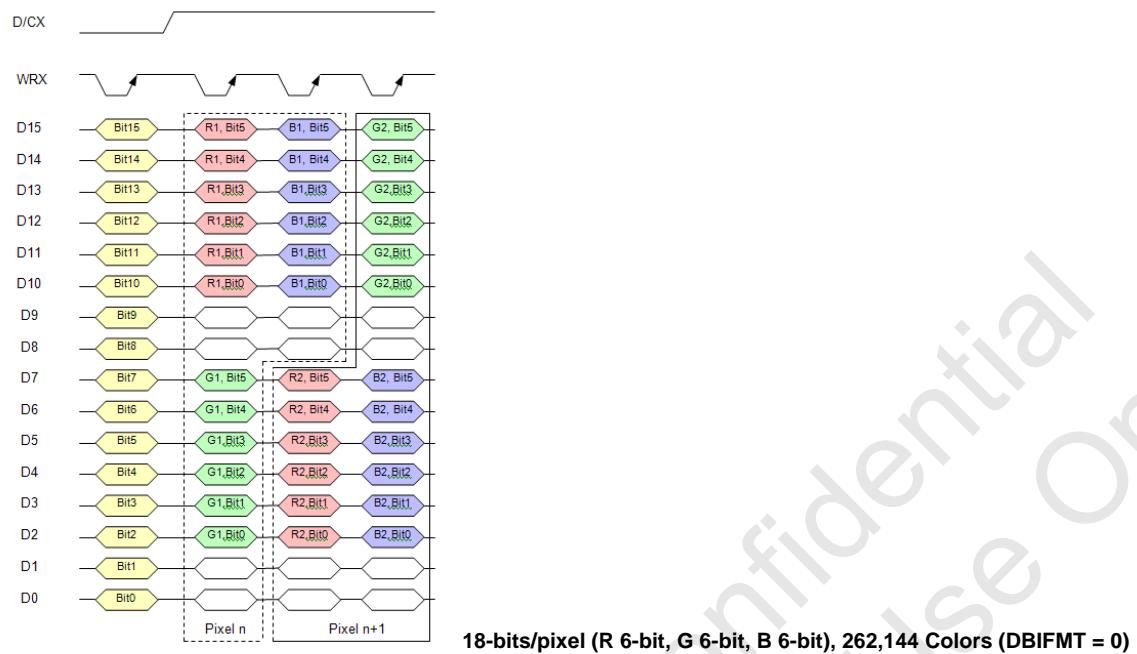
D/CX

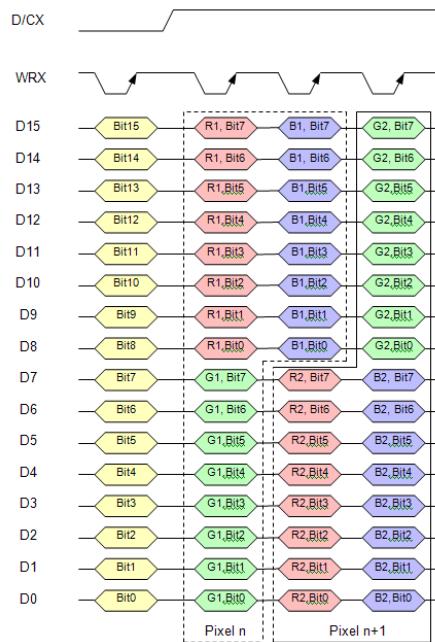


WRX

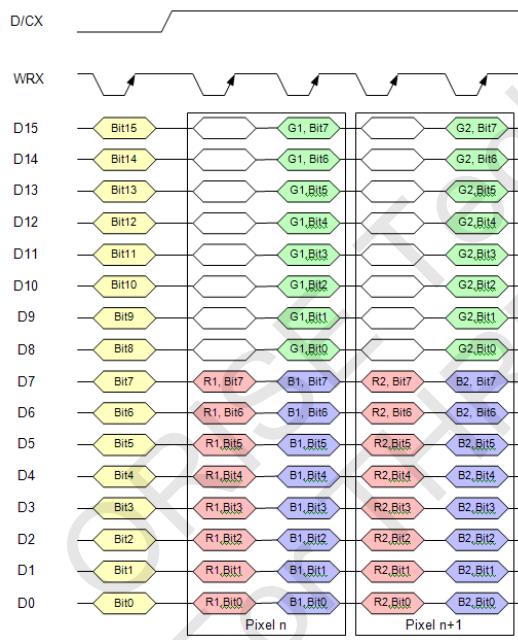



16-bits/pixel (R 5-bit, G 6-bit, B 5-bit), 65,536 Colors





24-bits/pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 Colors (DBIFMT = 0)



24-bits/pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 Colors (DBIFMT = 1)

6.5.3.3. 9-bit Interface color coding

BUS	COLOR	D8	D7	D6	D5	D4	D3	D2	D1	D0
9	666	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[5]	G1[4]	G1[3]

G1[2] G1[1] G1[0] B1[5] B1[4] B1[3] B1[2] B1[1] B1[0]

9-bits interface only support 262144 color mode.

6.5.3.4. 18-bit Interface color coding

BUS	COLOR	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18	444	X	X	X	X	X	X	R1[3]	R1[2]	R1[1]	R1[0]	G1[3]	G1[2]	G1[1]	G1[0]	B1[3]	B1[2]	B1[1]	B1[0]
	565	X	X	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]
	666	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]

No support 16.7M(888) color format in 18-bits interface.

6.5.3.5. 24-bit Interface color coding

BUS	COLOR	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		
24	444	X	X	X	X	X	X	X	X	R1[3]	R1[2]	R1[1]	R1[0]	G1[3]	G1[2]	G1[1]	G1[0]	B1[3]	B1[2]	B1[1]	B1[0]						
	565	X	X	X	X	X	X	X	X	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]		
	666	X	X	X	X	X	X	X	X	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]
	888	R1[7]	R1[6]	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[7]	G1[6]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	B1[7]	B1[6]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]		

6.6. I²C-Bus Interface

6.6.1. Characteristics of I²C-bus

The I²C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines compose of a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

6.6.1.1. System configuration (See Figure 6.6.1.1.)

- (1) Transmitter: the device which sends the data to the bus
- (2) Receiver: the device which receives the data from the bus
- (3) Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- (4) Slave: the device addressed by a master
- (5) Multi-Master: more than one master attempts to control the bus at the same time without corrupting the message
- (6) Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- (7) Synchronization: procedure to synchronize the clock signals of two or more devices.

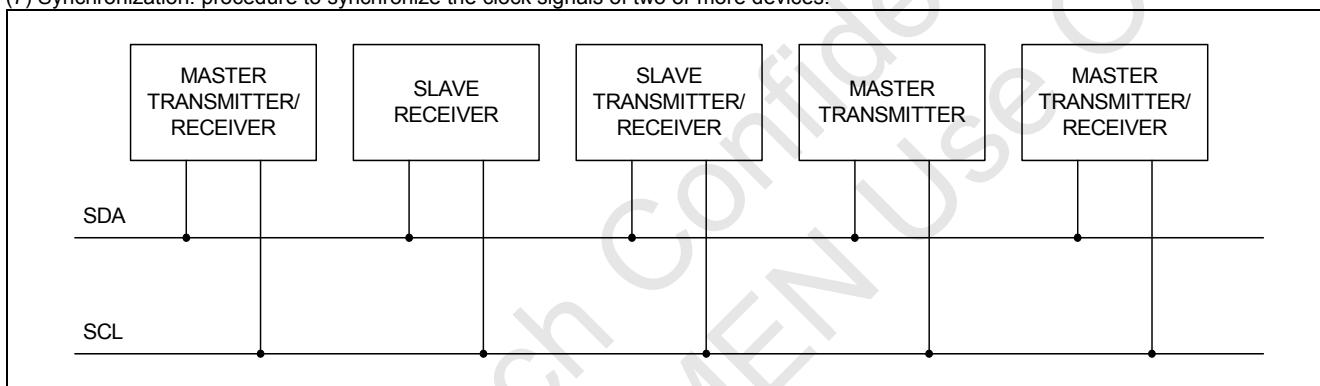


Figure 6.6.1.1 System configuration

6.6.1.2. Bit transfer (See Figure 6.6.1.2)

One data bit is transferred during each clock pulse. The data on SDA line must remain stabilized during the HIGH period of the clock pulse. As changes in the data line at this time will be interpreted as a control signal.

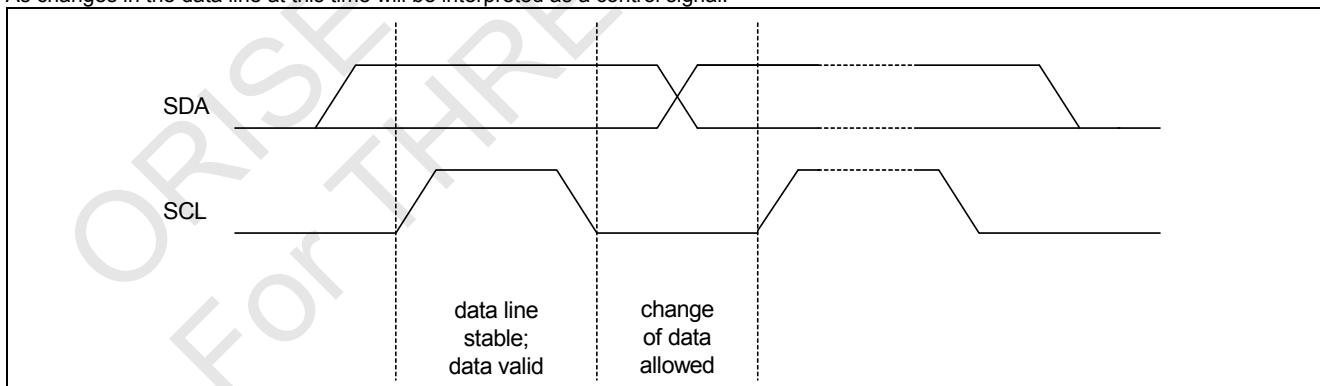


Figure 6.6.1.2 Bit transfer.

6.6.1.3. START and STOP conditions (See Figure 6.6.1.3)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition on the data line is defined as the STOP condition (P) while the clock is HIGH.

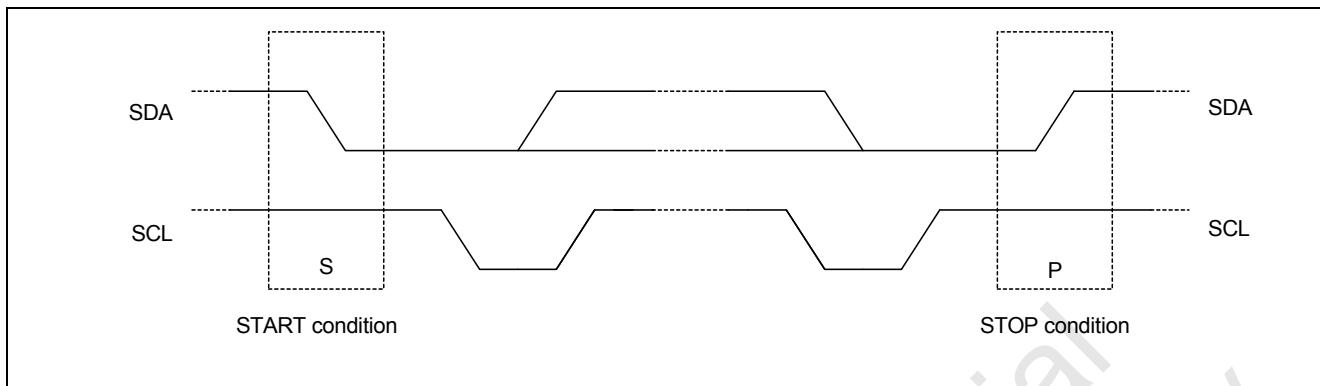


Figure 6.1.5.3 Definition of START and STOP conditions.

6.6.1.4. Acknowledgment (See Figure 6.6.1.4)

Each bit in a byte (8 bits) is followed by an acknowledgment bit. The acknowledgment bit is a HIGH signal placed on the bus by the transmitter during the master generating an extra acknowledgment related clock pulse.

An addressed slave receiver must generate an acknowledgment after the reception of each byte. Also a master receiver must generate an acknowledgment after the reception of each byte that has been clocked out of the slave transmitter.

The acknowledged device must pull-down the SDA line during the acknowledgment clock pulse, so that the SDA line remains LOW during the HIGH period of the acknowledgment related clock pulse (setup and hold times must be considered).

A master receiver must signal an end of data to the transmitter by not generating an acknowledgment on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

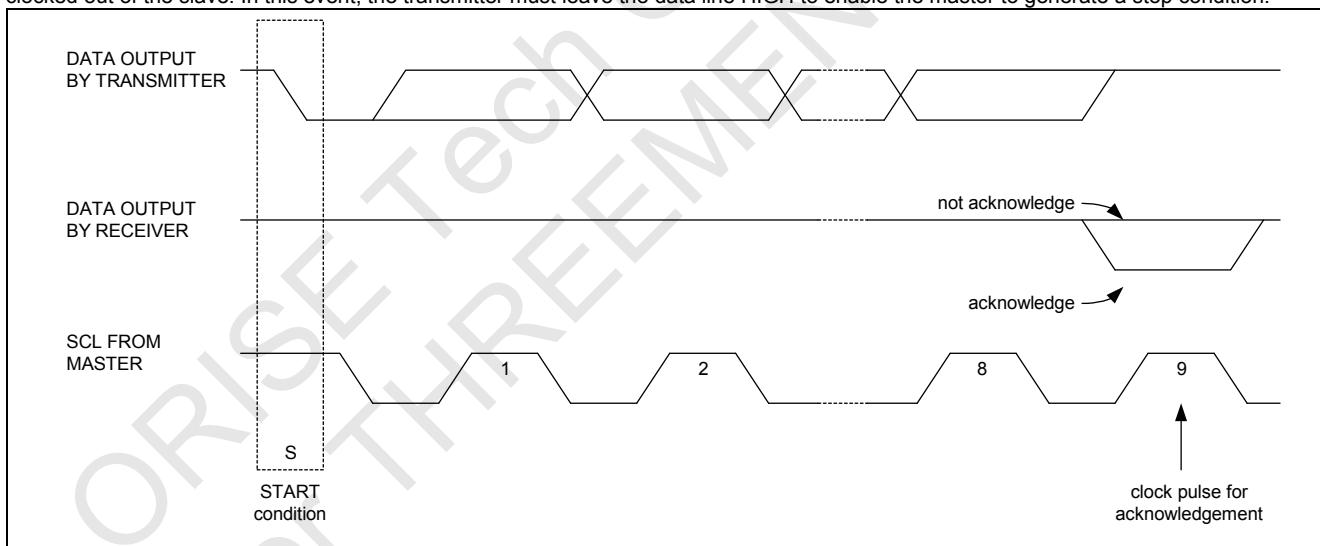


Figure 6.6.1.4 Acknowledgement on the I²C-bus.

6.6.2. I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device to respond is addressed first. Two 7-bit slave addresses (10011xx) are reserved for the OTM9608A. The least significant bit of the slave address is set by connecting the input I²C_SA[1:0].

I ² C_SA1	I ² C_SA0	Slave address	Notes
0	0	1001100	Other slave address are reversed for other IC.
0	1	1001101	
1	0	1001110	
1	1	1001111	

Table 6.6.2.1 Reserve address for OTM9608A.

6.6.2.1. I²C-bus Write Instruction and parameter

OTM9608A supports register write sequence via I²C-bus transfer. The detail transference sequences are illustrated and described as below.

- (1) Data transfers for register writing follow the format is shown in Figure 6.5.2.1.
- (2) After the START condition (Str), a slave address is sent. R/W bit is setting to "zero" for WRITE.
- (3) The slave issues an ACK to master.
- (4) 16 bits register high byte address transfer first. Then transfer the register low byte address.
- (5) 16 bits register high byte data of parameter transfer first. Then transfer the register low byte data parameter .
- (6) A data transfer is always terminated by a STOP condition.

Write Instruction (No parameter)	Str	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	End
		ID(6:0)=10011xx	R/W	Instruction Address[15:8]		Instruction Address[7:0]		

Write Instruction +1 Parameter	Str	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	End
		ID(6:0)=10011xx	R/W	Instruction Address[15:8]		Instruction Address[7:0]		Parameter[11:8]		Parameter[7:0]		

Figure 6.6.2.1 I²C write stream for write command

6.6.2.2. I²C-bus Write GRAM

Write GRAM 4096 Color	Str	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	End
		ID(6:0)=10011xx	R/W	Instruction Address[2:0] = 2Ch or 3Ch		Instruction Address[7:0]=00h		Instruction Address[7:0]=00h		Instruction Address[7:0]=00h		
Write GRAM 65536 Color	Str	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	End
		ID(6:0)=10011xx	R/W	Instruction Address[2:0] = 2Ch or 3Ch		Instruction Address[7:0]=00h		Instruction Address[7:0]=00h		Instruction Address[7:0]=00h		
Write GRAM 262K Color	Str	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	End
		ID(6:0)=10011xx	R/W	Instruction Address[2:0] = 2Ch or 3Ch		Instruction Address[7:0]=00h		Instruction Address[7:0]=00h		Instruction Address[7:0]=00h		
Write GRAM 16.7M Color	Str	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	End
		ID(6:0)=10011xx	R/W	Instruction Address[2:0] = 2Ch or 3Ch		Instruction Address[7:0]=00h		Instruction Address[7:0]=00h		Instruction Address[7:0]=00h		
Write GRAM 8 Color mode 1	Str	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	End
		ID(6:0)=10011xx	R/W	Instruction Address[2:0] = 2Ch or 3Ch		Instruction Address[7:0]=00h		Instruction Address[7:0]=00h		Instruction Address[7:0]=00h		
Write GRAM 8 Color mode 2	Str	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	End
		ID(6:0)=10011xx	R/W	Instruction Address[2:0] = 2Ch or 3Ch		Instruction Address[7:0]=00h		Instruction Address[7:0]=00h		Instruction Address[7:0]=00h		

Figure 6.5.2.2 Color format and I²C write stream

Note :

- (1) 4096 color : 3 bytes = 2 pixels
- (2) 65536 color: 2 bytes = 1 pixel
- (3) 262K color: 3bytes = 1 pixel
- (4) 16.7M color: 3bytes = 1 pixel
- (5) 8 color(idle mode): 1 byte = 2 pixel

6.6.2.3. I²C-bus Read

Read Instruction +1 Parameter	Str	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	End
		ID(6:0)=10011xx	R/W	Instruction Address[7:0]		Instruction Address[7:0]		Parameter[15:8]		Parameter[7:0]		
Read GRAM	Str	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	D7 D6 D5 D4 D3 D2 D1 D0	Ack	End
		ID(6:0)=10011xx	R/W	Instruction Address[7:0]=00h		Instruction Address[7:0]=00h		Parameter[15:8]		Parameter[7:0]		

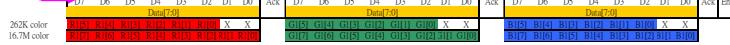


Figure 6.6.2.3 Color format and I²C Read stream

Note : OTM9608A only support 16.7M / 262K color for GRAM read back.

6.7. Serial Interface (SPI)

The selection of this interface is done by set IM2 / IM1 / IM0 = 011. And select IM3 = 0 or 1 to decide the trigger edge of serial clock (SCL) is rising edge or falling edge. The serial interface is used to communication between the micro controller and the LCD driver chip. It contains CSX (chip select), SCL (serial clock), SDI (serial data input) and SDO (serial data output). Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary. If the host places the SDI line into high-impedance state during the read intervals, then the SDI and SDO can be tied together.

6.7.1. SPI Write mode

The write mode of the interface means the micro controller writes commands and data to the OTM9608A. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling CSX edge, SCL can be high or low (See Figure 6.7.1.1). SDI / SDO is sampled at the rising edge of SCL. R/W indicates, whether the byte is read command (R/W = '1') or write command (R/W = '0'). It is sampled when first rising SCL edge. If CSX stays low after the last bit of command/data byte, the serial interface expects the R/W bit of the next byte at the next rising edge of SCL.

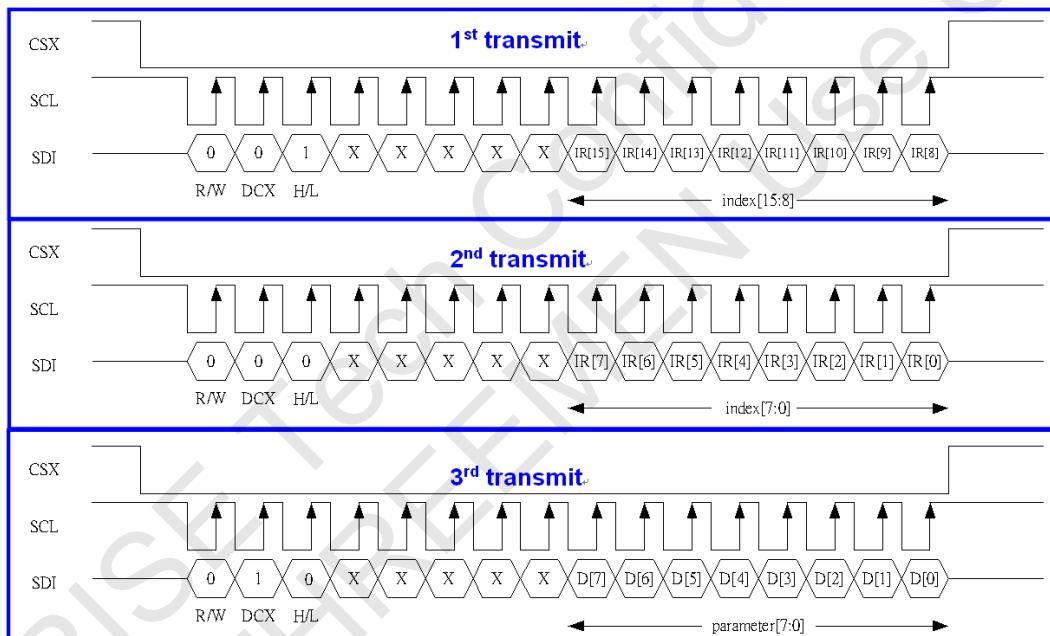


Figure 6.7.1.1 SPI Protocol for Register Write Mode

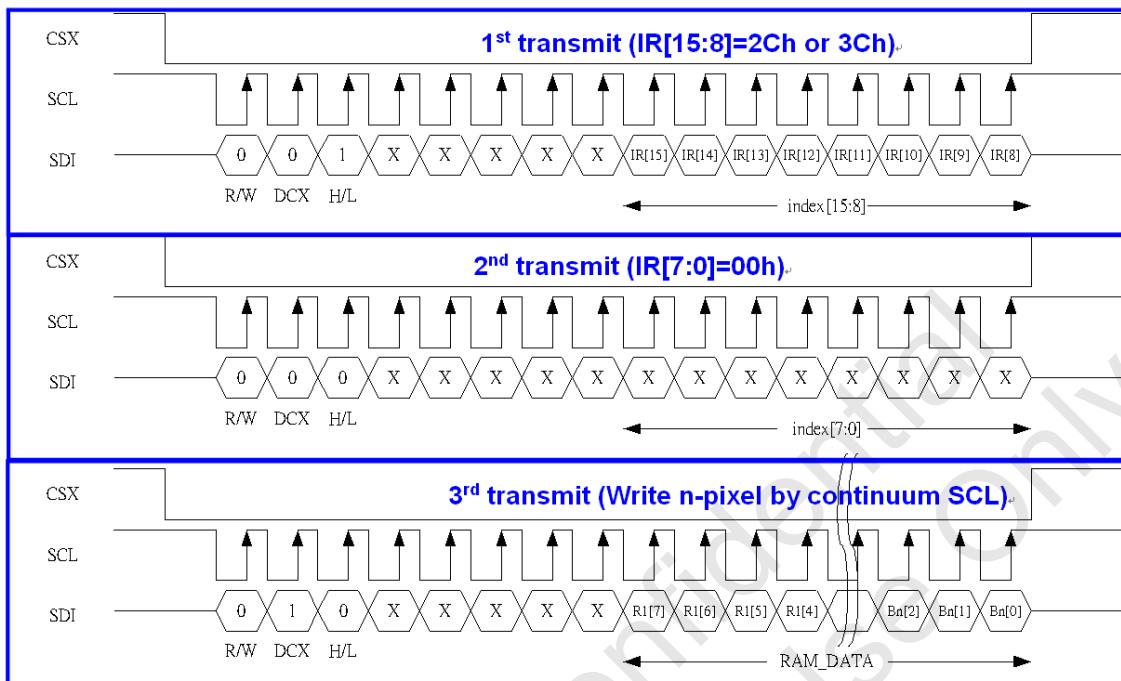


Figure 6.6.1.2 SPI Protocol for GRAM Write (continuum SCL Mode)

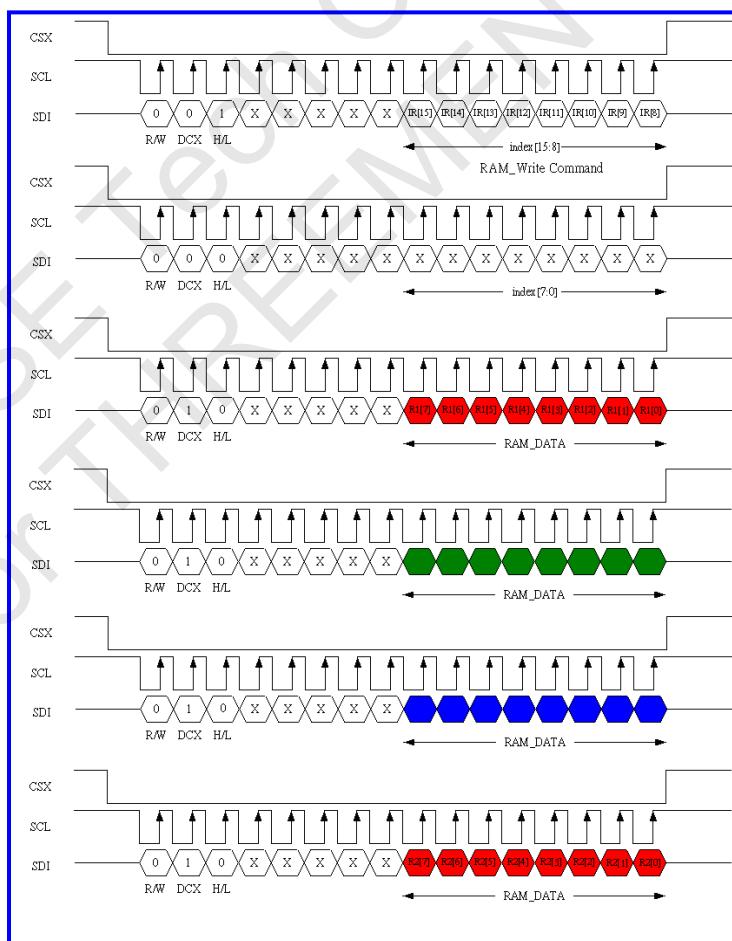


Figure 6.6.1.3 SPI Protocol for GRAM Write (Separate Byte Mode)

RAM Write	SPI interface		7	6	5	4	3	2	1	0
			D7	D6	D5	D4	D3	D2	D1	D0
444	3T2P	RJ[3]	RJ[2]	RJ[1]	RJ[0]	G1[3]	G1[2]	G1[1]	G1[0]	
		B1[3]	B1[2]	B1[1]	B1[0]	R2[3]	R2[2]	R2[1]	R2[0]	
565	2T1P	RJ[4]	RJ[3]	RJ[2]	RJ[1]	RJ[0]	G1[5]	G1[4]	G1[3]	
		G1[2]	G1[1]	G1[0]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	
666	3T1P	RJ[5]	RJ[4]	RJ[3]	RJ[2]	RJ[1]	RJ[0]	X	X	
		G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	X	X	
888	3T1P	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	X	X	
		RJ[7]	RJ[6]	RJ[5]	RJ[4]	RJ[3]	RJ[2]	RJ[1]	RJ[0]	
8 color OPT-1	1T2P	X	X	RJ[0]	G1[0]	B1[0]	R2[0]	G2[0]	B2[0]	
	1T2P	X	RJ[0]	G1[0]	B1[0]	X	R2[0]	G2[0]	B2[0]	

1'st transmit
 2'nd transmit
 3'rd transmit
 1'st transmit
 2'nd transmit
 1'st transmit
 2'nd transmit
 3'rd transmit
 1'st transmit
 2'nd transmit
 3'rd transmit
 1'st transmit
 1'st transmit

Table 6.6.1.1 Available color format for SPI interface

6.7.2. SPI Read mode

The read mode of the interface means that the micro controller reads register value from the OTM9608A. To do so the micro controller first has to send a command and then the following byte is transmitted in the opposite direction. After that CSX is required to go high before a new command is send (see Figure. 6.6.2.1). The OTM9608A samples the SDI (input data) at the rising edges, but shifts SDO (output data) at the falling SCL edges. Thus the micro controller is supported to read data at the rising SCL edges. After the read status command has been sent, the SDI line must be set to tri-state no later than at the falling SCL edge of the last bit. For the memory data read, a dummy clock cycle is needed (16 SCL clocks) to wait the memory data send out in SPI interface. But it doesn't need any dummy clock when execute the command data read.

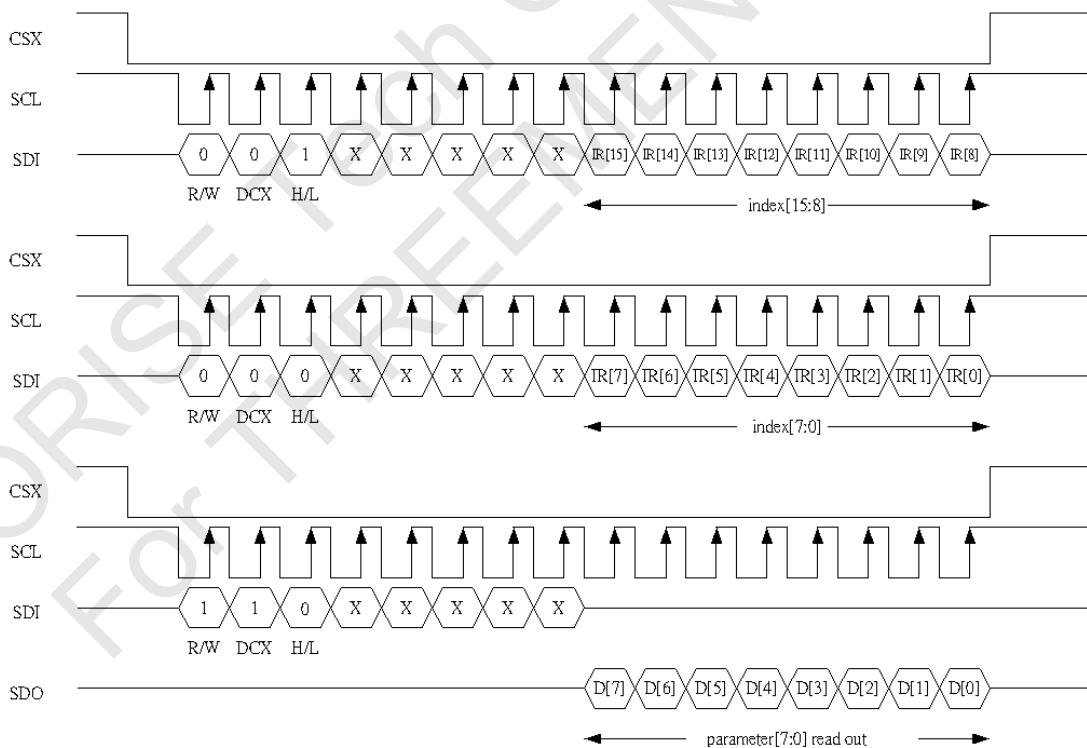


Figure 6.7.2.1 SPI Protocol for Register Read Mode

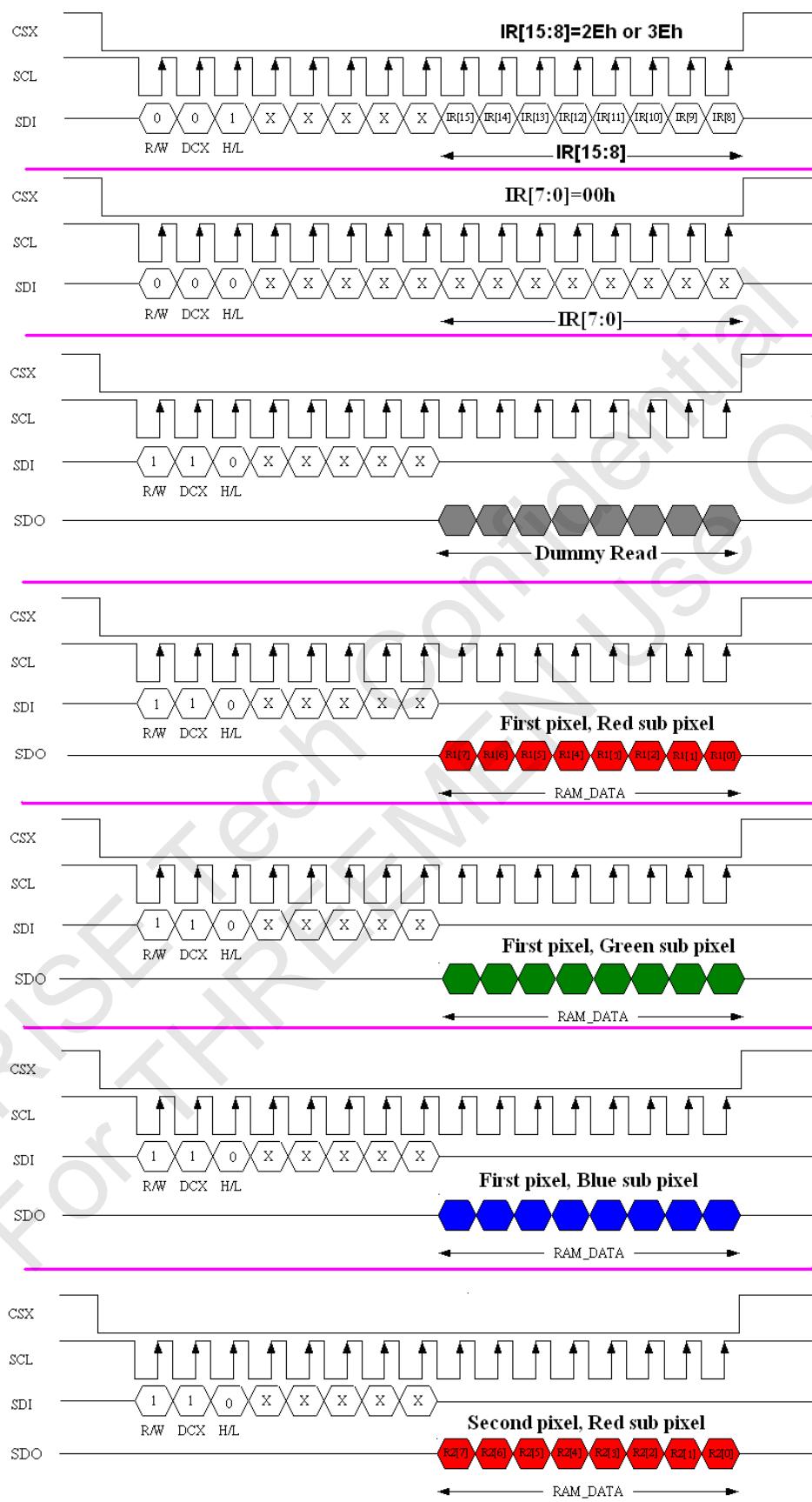


Figure 6.7.2.2 SPI Protocol for GRAM Read

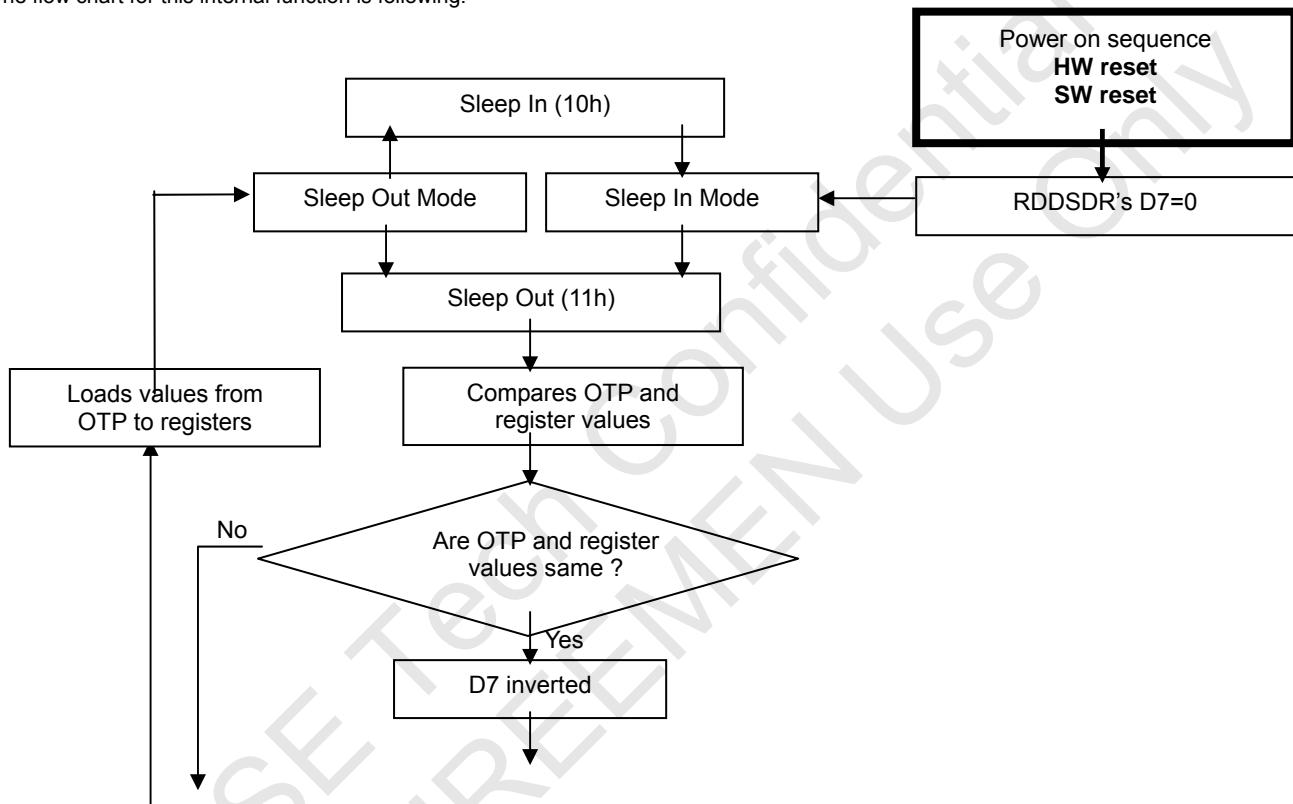
6.8. Sleep Out-Command and Self-Diagnostic Functions of the Display Module

6.8.1. Register loading detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (one-time programming memory) to registers of the display controller is working properly.

There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit in "Read Display Self-Diagnostic Result (0Fh)" (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= increased by 1).

The flow chart for this internal function is following:



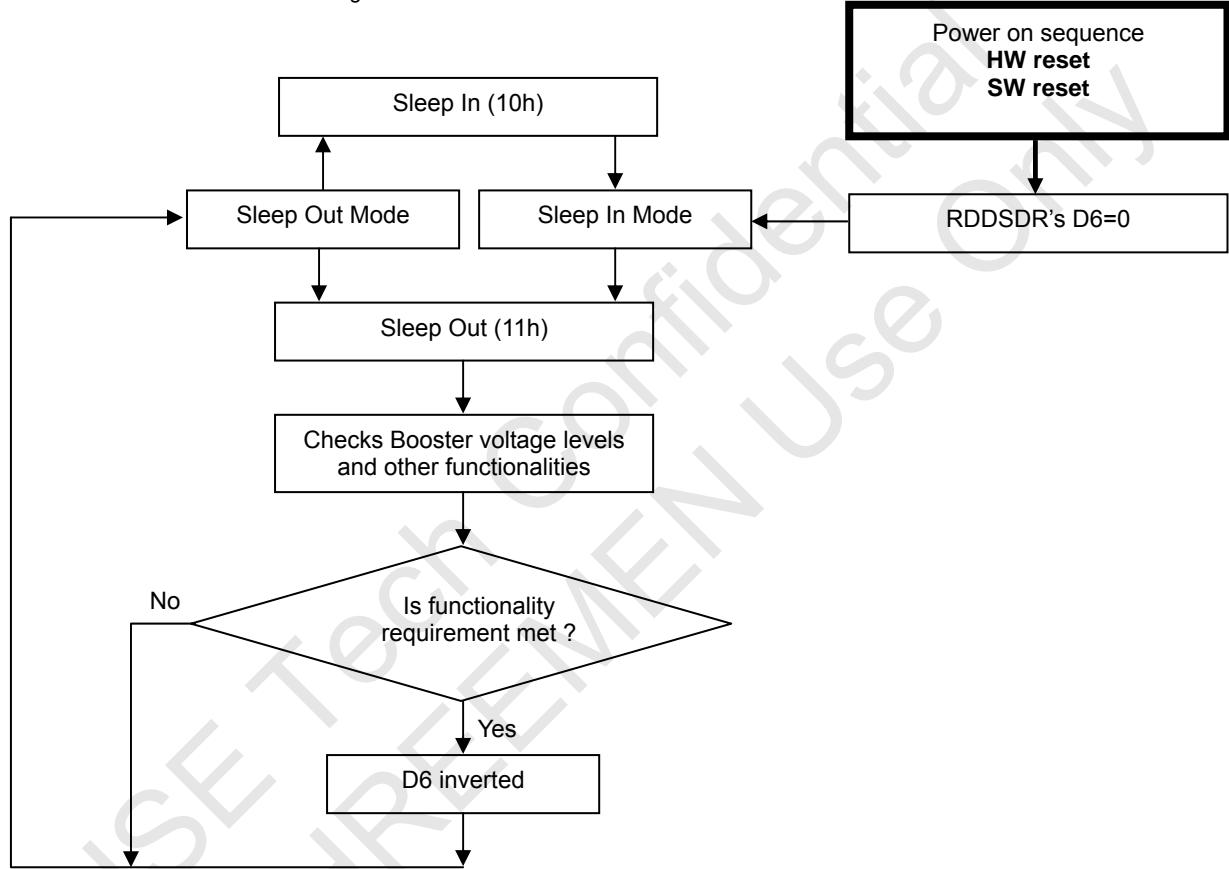
Note: There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DDh), by the display module.

6.8.2. Functionality detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (only Booster voltage level). If functionality requirement is met, there is inverted (= increased by 1) a bit in “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1).

The flow chart for this internal function is following:



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In -mode to Sleep Out -mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out -command is sent in Sleep Out -mode.

6.9. POWER ON/OFF SEQUENCE

VDDIO and VDD can be applied in any order.

VDDIO and VDD can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDIO must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDIO or VDD can be powered down minimum 0msec after RESX has been released. CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

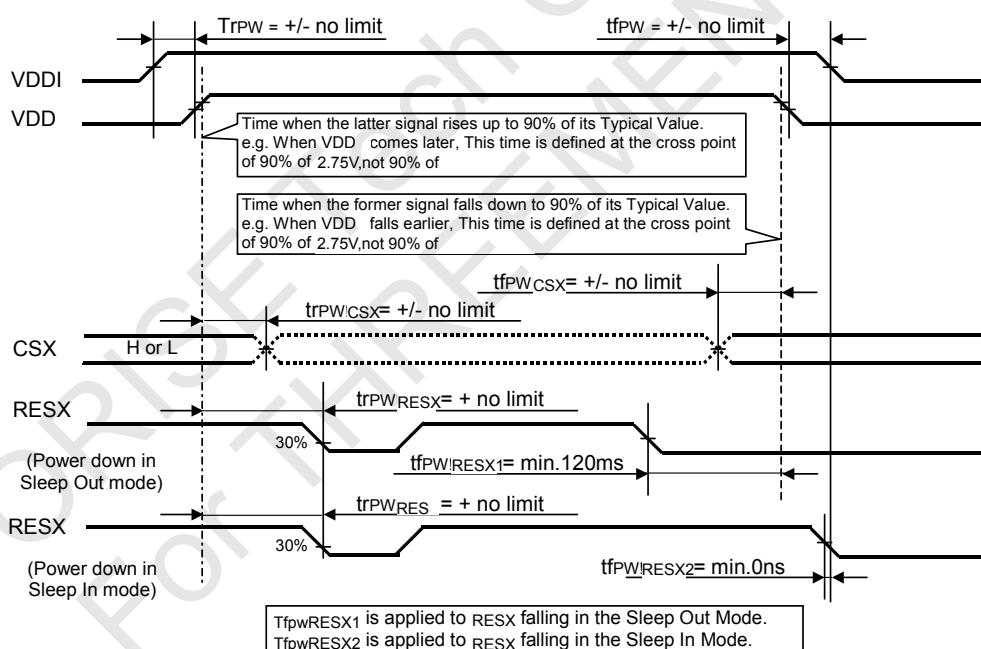
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

If RESX line is not held stable by host during Power On Sequence, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

6.9.1. Case 1 – RESX line is held high or unstable by host at power on

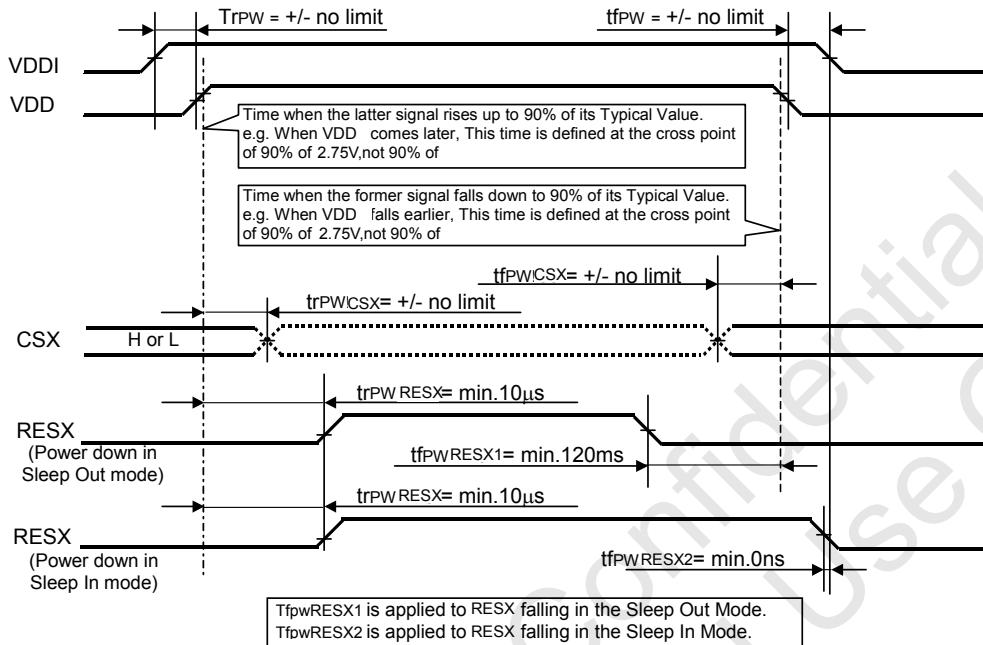
If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD and VDDIO have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

6.9.2. Case 1 – RESX line is held high or unstable by host at power on

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10 μ sec after both VDD and VDDIO have been applied.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

6.9.3. Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface.

At an uncontrolled power off the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until "Power On Sequence" powers it up.

6.10. Power level Definition

6.10.1. Power level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode

In this mode, the DC: DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDIO power supply. Contents of the memory are safe.

6. Power Off Mode

In this mode, both VDD and VDDIO are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

6.10.2. Power flow chart

Normal display mode on = NORON

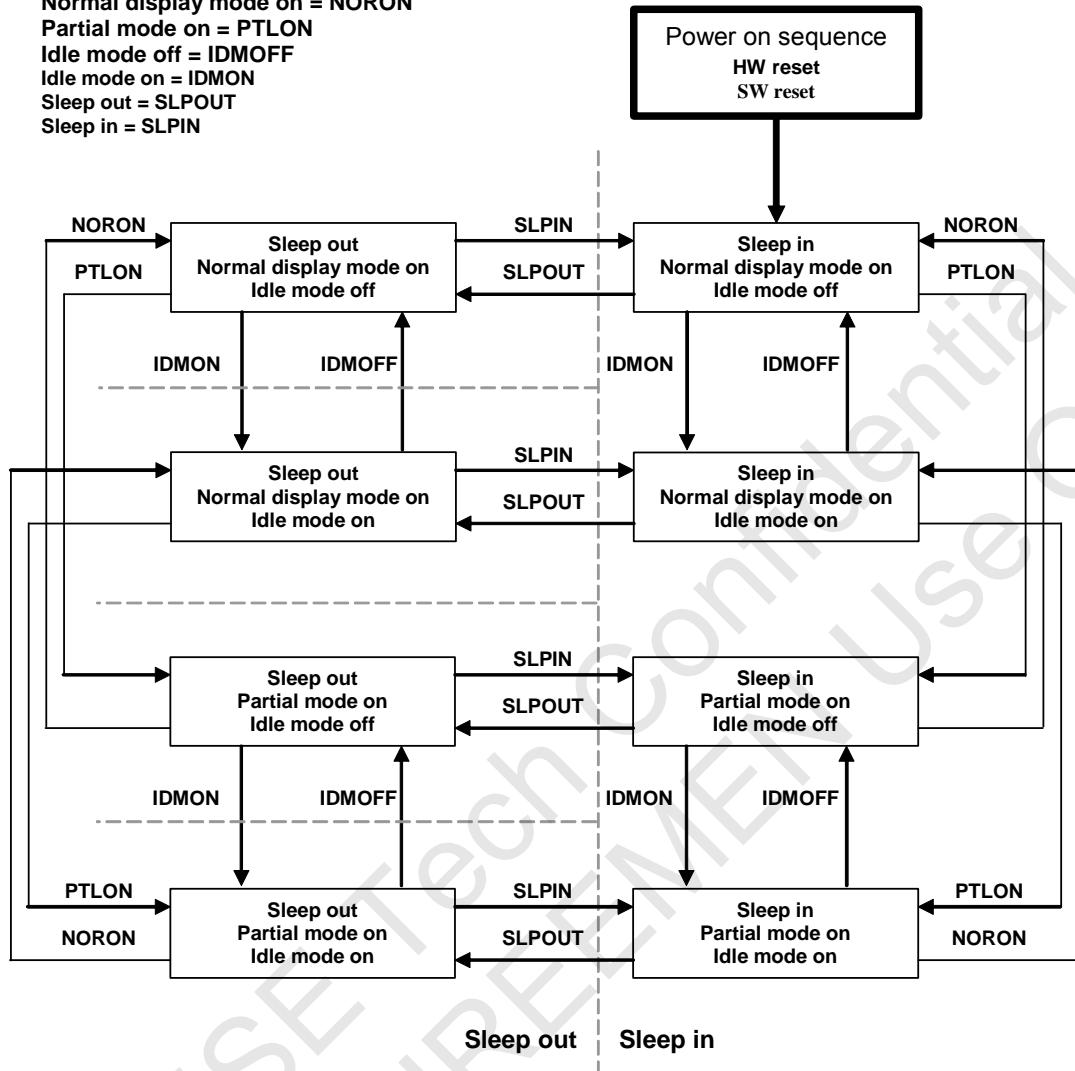
Partial mode on = PTLON

Idle mode off = IDMOFF

Idle mode on = IDMON

Sleep out = SLPOUT

Sleep in = SLPIN



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode.

6.11. Tear Effect Information

6.11.1. General

The MCU is updating the frame memory of the display module via its interface (DSI).

The display module is refreshing the display panel from the frame memory independently and it does not know what is happening on the interface of the display module (The MCU is sending image information to the display module). It is possible that this asynchronous updating is causing an abnormal visual effect on the display panel of the display module.

Therefore, the display module is sending a synchronous information (= Tearing Effect Information), which is telling the position of the refreshing on the display panel, to the MCU which can decide when it can send image information to the display module (Mainly used for a moving image e.g. video clips) that there can avoid the abnormal visual effect on the display panel of the display module.

This Tearing Effect information can be sent in two different ways:

- Separated Line, which is so-called Tearing Effect (TE) line
- Bus, which is so-called Tearing Effect (TEE) Bus Trigger, when the display module is sending a trigger to the MCU

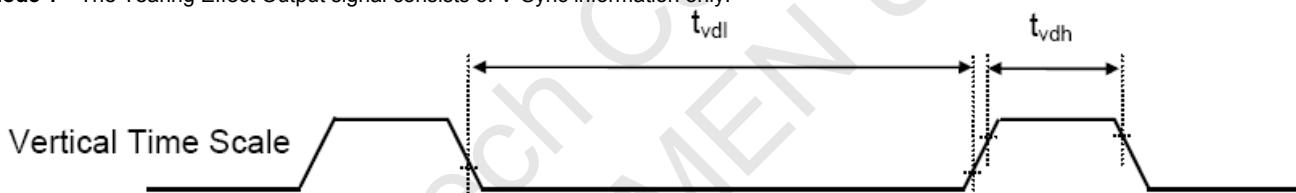
The TE line can be used in DSI case if the Tearing Effect (TEE) bus trigger is not possible to use and the Tearing Effect (TEE) Bus Trigger is only used in DSI case.

6.11.1.1. Tearing effect line models

The Tearing Effect line supplies to the MCU a Panel synchronisation signal and this signal can be enabled or disabled by the Tearing Effect Line Off & On commands.

The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command.

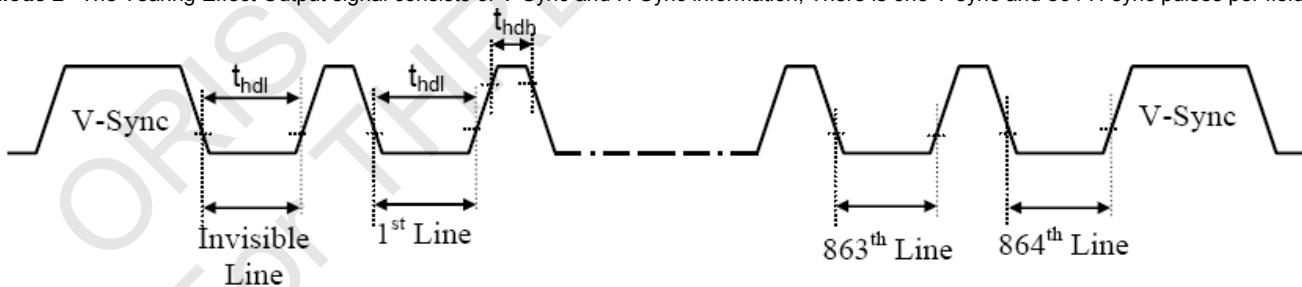
Mode 1 : The Tearing Effect Output signal consists of V-Sync information only:



t_{vdh} = The display panel is not updated from the Frame Memory.

t_{vdl} = The display panel is updated from the Frame Memory (except Invisible Line – see below).

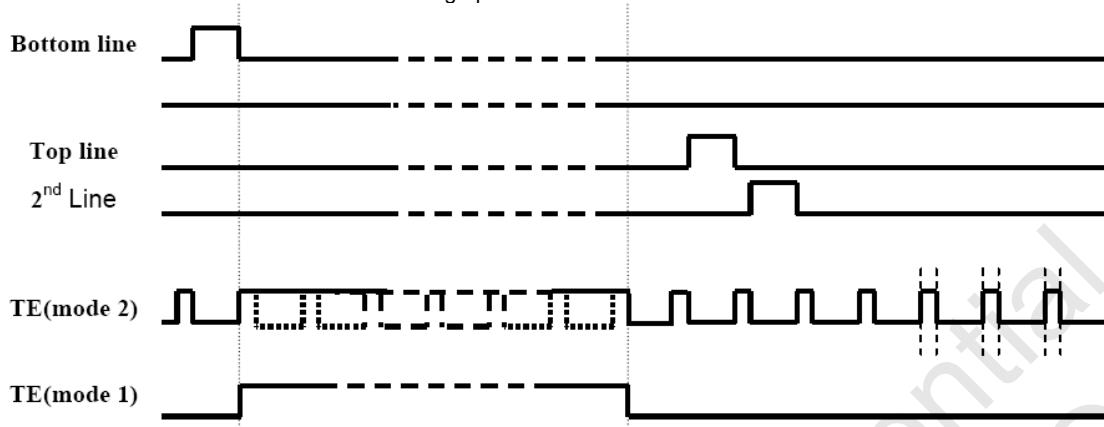
Mode 2 : The Tearing Effect Output signal consists of V-Sync and H-Sync information; There is one V-sync and 864 H-sync pulses per field:



t_{vdh} = The display panel is not updated from the Frame Memory.

t_{vdl} = The display panel is updated from the Frame Memory (except Invisible Line – see below).

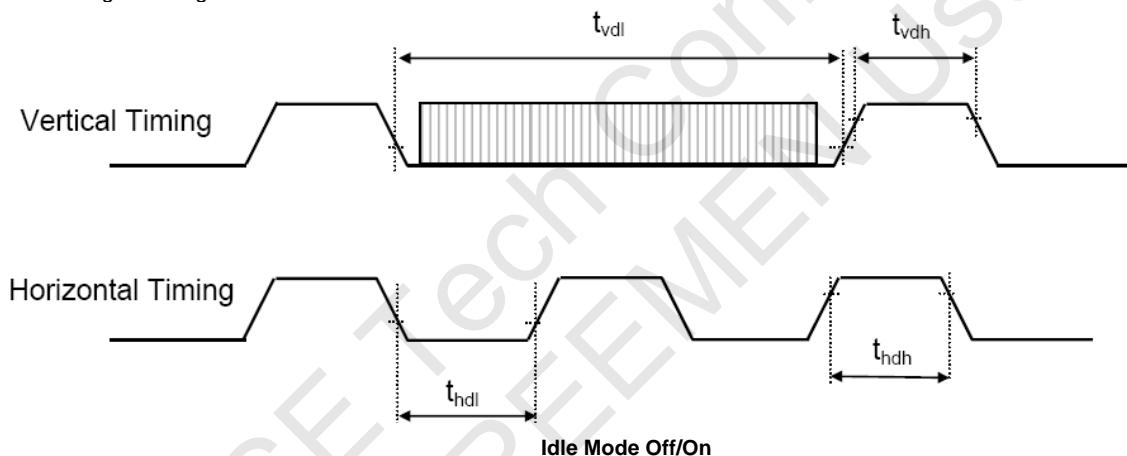
TE Line mode1 and Mode2 is shown as below graph:



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

6.11.1.2. Tearing effect line timing

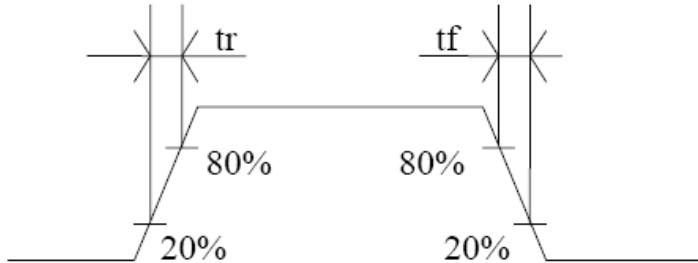
The Tearing Effect signal is described below:



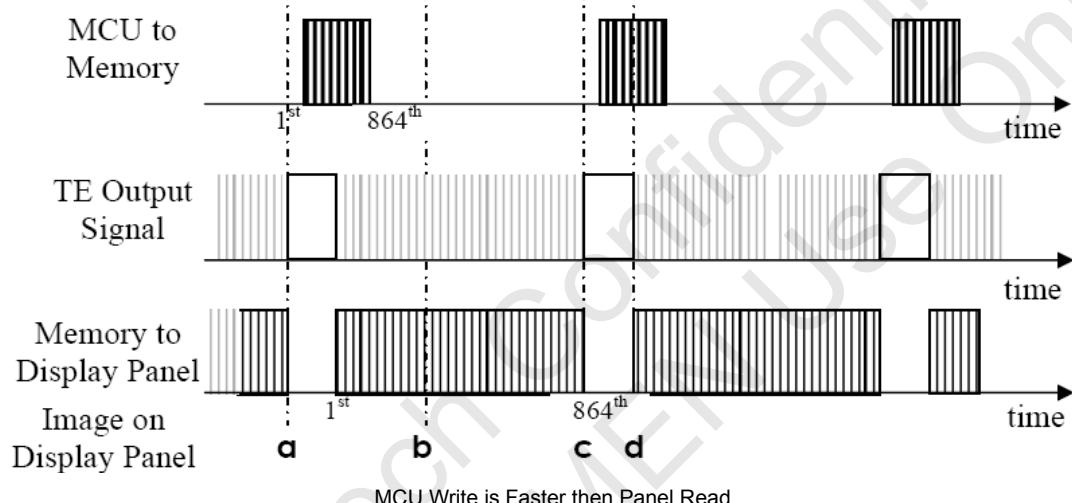
Symbol	Parameter	Min.	Max.	Unit
t_vdl	Vertical Timing Low Duration			ms
t_vdh	Vertical Timing High Duration	1000		μs
t_hdl	Horizontal Timing Low Duration		-	μs
t_hdh	Horizontal Timing High Duration		500	μs

1. Minimum frequency of the TE-line cannot be less than 25Hz, when the TE-line is active, on Mode 1.
2. The signal's rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns when the maximum load is TBD Ω .

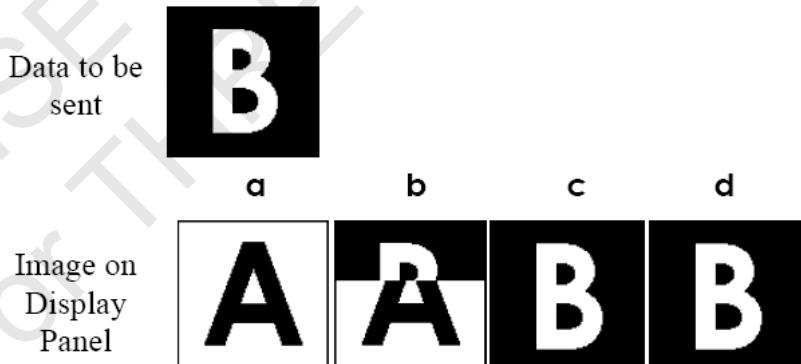
The TE signal rising and falling timing is described below:



6.11.1.3. Example 1 MCU write is faster than panel read

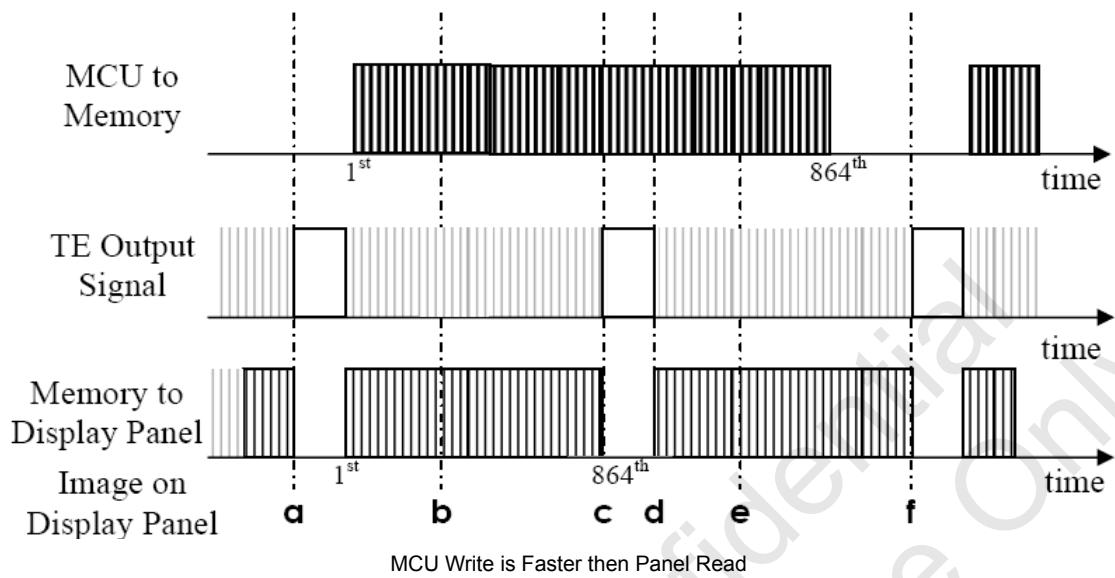


Data write to Frame Memory is now synchronised to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

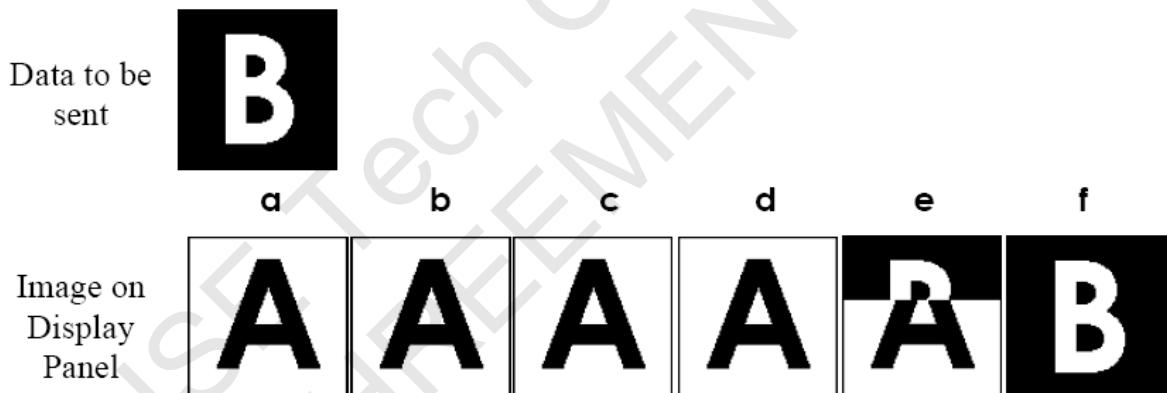


Example 1 – Image on the Display Panel

6.11.1.4. Example 1 MCU write is slower than panel read



The MCU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent frame before the Read Pointer “catches” the MCU to frame memory write position.

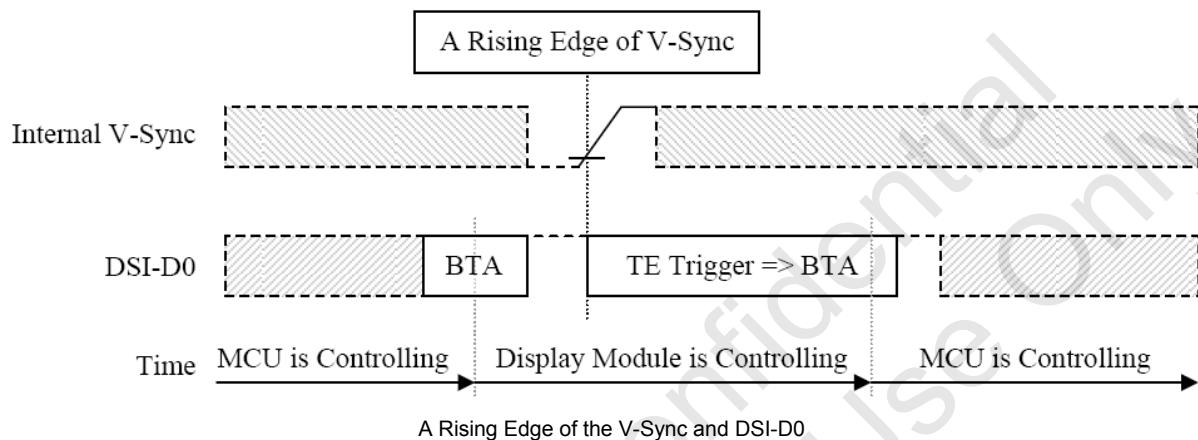


Example 2 – Image on the Display Panel

6.11.2. Tearing effect bus trigger

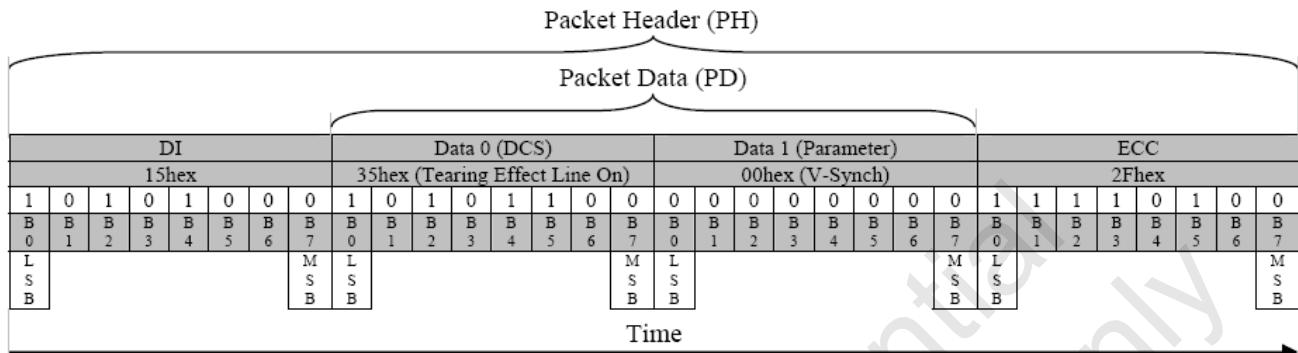
A Tearing Effect Bus Trigger information supplies to the MCU a Panel synchronisation trigger and this Tearing Effect Bus Trigger information can be enabled or disabled by commands “Tearing Effect Line Off (34h)” and “Tearing Effect Line On (35h)” when the only mode of the Tearing Effect Signal is VSync. information.

The display module is sending this trigger information in Escape Mode after the Bus Turnaround (BTA). The Tearing Effect Bus Trigger can only use in DSI case without the TE line.

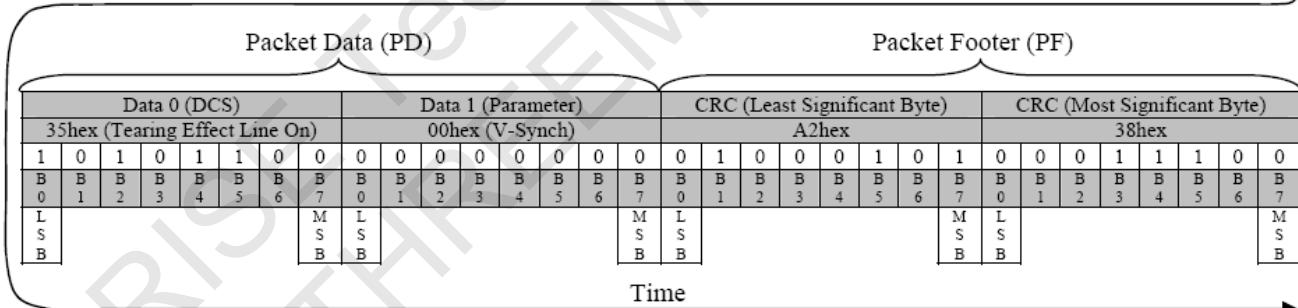
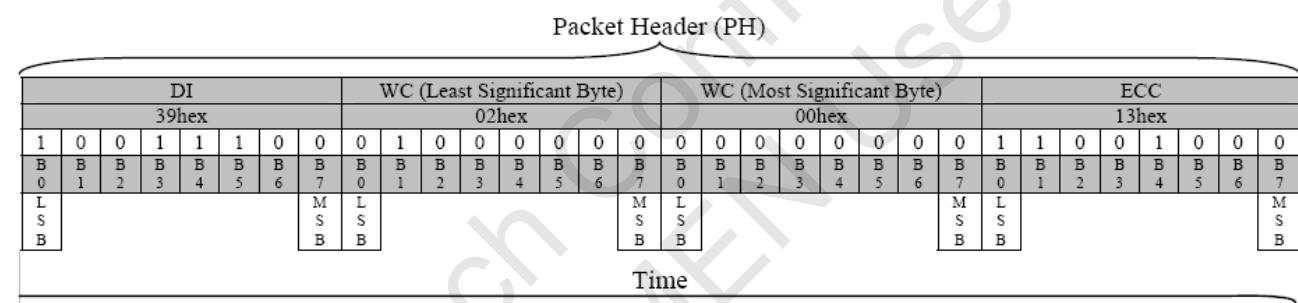


6.11.2.1. Tearing effect bus trigger enable

The MCU can enable the Tearing Effect Bus Trigger on the display module in 2 different ways when a Short Packet (SPa) or Long Packet (LPa) is used. These cases are illustrated below.



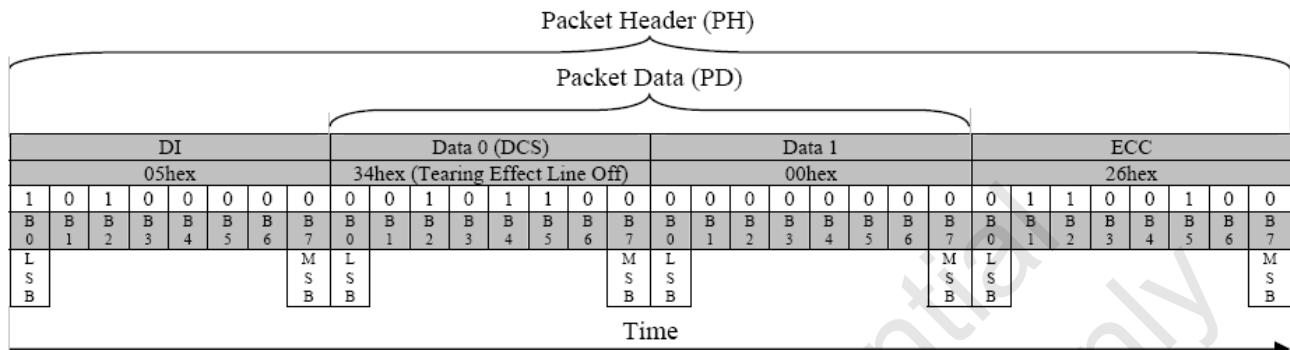
Tearing Effect Bus Trigger Enable (DCSW1-S) – Short Packet (SPa)



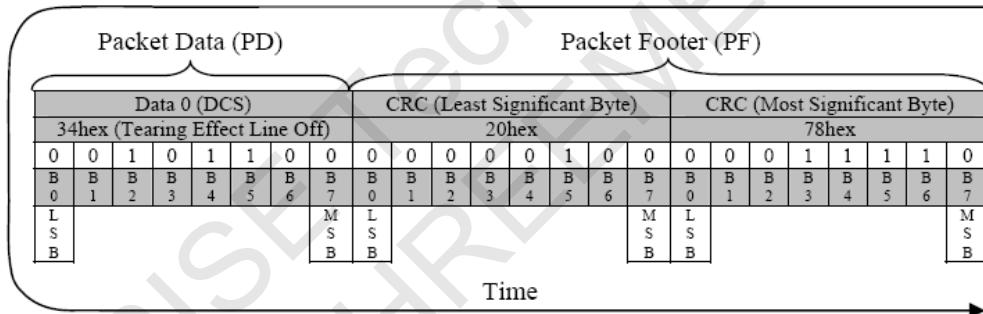
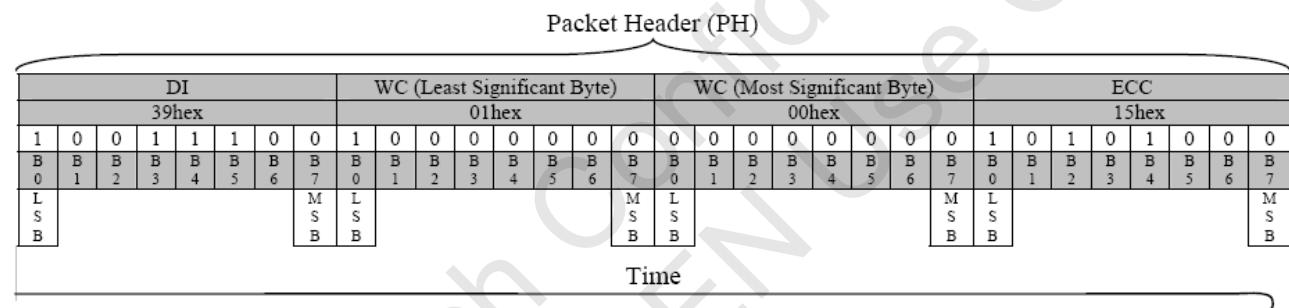
Tearing Effect Bus Trigger Enable (DCSW-L) – Long Packet (LPa)

6.11.2.2. Tearing effect bus trigger disable

The MCU can enable the Tearing Effect Bus Trigger on the display module in 2 different ways when a Short Packet (SPa) or Long Packet (LPa) is used. These both possibilities are illustrated below.



Tearing Effect Bus Trigger Disable (DCSWN-S) – Short Packet (SPa)



Tearing Effect Bus Trigger Disable (DCSW-L) – Long Packet (LPa)

6.11.2.3. Tearing effect bus trigger sequences
6.11.2.4. Tearing effect bus trigger enable sequence – DCSW-L and HSDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
6	-	-	<=	LP-11	-	If No Error => Goto Line 8 If Error is Corrected by ECC => Goto Line 19 If Error => Goto Line 30
7						
8	-	-	<=	ACK	-	No Error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
11	-	LP-11	=>	-	-	
12	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
13	-	-	<=	LP-11	-	
14	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Synch.
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
17	-	LP-11	=>	-	-	End
18						
19	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
20	-	-	<=	LP-11	-	
21	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
22	-	LP-11	=>	-	-	
23	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
24	-	-	<=	LP-11	-	
25	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Synch.
26	-	-	<=	LP-11	-	
27	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
28	-	LP-11	=>	-	-	End
29						
30	-	-	<=	LPDT	AwER	Error Report
31	-	-	<=	LP-11	-	
32	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
33	-	LP-11	=>	-	-	If the MCU is not forcing BTA => Goto Line 34 If the MCU is forcing BTA => Goto Line 36
34	-	LP-11	=>	-	-	End
35						
36	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
37	-	-	<=	LP-11	-	Dead-Lock (No TE information) See Note 2
38	-	LP-11	=>	-	-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
39	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
40	-	-	<=	LP-11	-	
41	-	-	<=	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported) See Note 2
42	-	-	<=	LP-11	-	
43	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
44	-	LP-11	=>	-	-	End

Notes:

1. Lines 1 – 17 are needed for every frame..
2. Bits 5 and 7 of the AwER are applied.

6.11.2.5. Tearing effect bus trigger Enable Sequence – DCSW-L and LPDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	LPDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	-	LP-11	=>	-	-	
4	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
5	-	-	<=	LP-11	-	If No Error => Goto Line 7 If Error is Corrected by ECC => Goto Line 18 If Error => Goto Line 29
6						
7	-	-	<=	ACK	-	No Error
8	-	-	<=	LP-11	-	
9	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
10	-	LP-11	=>	-	-	
11	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
12	-	-	<=	LP-11	-	
13	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Synch.
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
16	-	LP-11	=>	-	-	End
17						
18	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
19	-	-	<=	LP-11	-	
20	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
21	-	LP-11	=>	-	-	
22	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
23	-	-	<=	LP-11	-	
24	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Synch.
25	-	-	<=	LP-11	-	
26	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
27	-	LP-11	=>	-	-	End
28						
29	-	-	<=	LPDT	AwER	Error Report
30	-	-	<=	LP-11	-	
31	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
32	-	LP-11	=>	-	-	If the MCU is not forcing BTA => Goto Line 33 If the MCU is forcing BTA => Goto Line 35
33	-	LP-11	=>	-	-	End
34						
35	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
36	-	-	<=	LP-11	-	Dead-Lock (No TE information) See Note 2
37	-	LP-11	=>	-	-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
38	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
39	-	-	<=	LP-11	-	
40	-	-	<=	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported) See Note 2
41	-	-	<=	LP-11	-	
42	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
43	-	LP-11	=>	-	-	End

Notes:

1. Lines 1 – 16 are needed for every frame.
2. Bits 5 and 7 of the AwER are applied.

6.11.2.6. Tearing effect bus trigger enable sequence – DCSW1-S and HPDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module If No Error => Goto Line 8 If Error is Corrected by ECC => Goto Line 19 If Error => Goto Line 30
6	-	-	=<	LP-11	-	
7						
8	-	-	=<	ACK	-	No Error
9	-	-	=<	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
11	-	LP-11	=>	-	-	
12	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
13	-	-	=<	LP-11	-	
14	-	-	=<	TEE	-	TE (Escape Trigger) on the next V-Synch.
15	-	-	=<	LP-11	-	
16	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
17	-	LP-11	=>	-	-	End
18						
19	-	-	=<	LPDT	AwER	Error Report (Error is Corrected by ECC)
20	-	-	=<	LP-11	-	
21	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
22	-	LP-11	=>	-	-	
23	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
24	-	-	=<	LP-11	-	
25	-	-	=<	TEE	-	TE (Escape Trigger) on the next V-Synch.
26	-	-	=<	LP-11	-	
27	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
28	-	LP-11	=>	-	-	End
29						
30	-	-	=<	LPDT	AwER	Error Report
31	-	-	=<	LP-11	-	
32	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
33	-	LP-11	=>	-	-	If the MCU is not forcing BTA => Goto Line 34 If the MCU is forcing BTA => Goto Line 36
34	-	LP-11	=>	-	-	End
35						
36	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
37	-	-	=<	LP-11	-	Dead-Lock (No TE information) See Note 2
38	-	LP-11	=>	-	-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
39	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
40	-	-	=<	LP-11	-	
41	-	-	=<	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported) See Note 2
42	-	-	=<	LP-11	-	
43	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
44	-	LP-11	=>	-	-	End

Notes:

1. Lines 1 – 17 are needed for every frame.
2. Bits 5 and 7 of the AwER are applied.

6.11.2.7. Tearing effect bus trigger enable sequence – DCSW1-S and LPDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	Tearing Effect Bus Trigger Enable
3	-	LP-11	=>	-	-	
4	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module If No Error => Goto Line 7 If Error is Corrected by ECC => Goto Line 18 If Error => Goto Line 29
5	-	-	<=	LP-11	-	
6						
7	-	-	<=	ACK	-	No Error
8	-	-	<=	LP-11	-	
9	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
10	-	LP-11	=>	-	-	
11	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
12	-	-	<=	LP-11	-	
13	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Synch.
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
16	-	LP-11	=>	-	-	End
17						
18	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
19	-	-	<=	LP-11	-	
20	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
21	-	LP-11	=>	-	-	
22	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
23	-	-	<=	LP-11	-	
24	-	-	<=	TEE	-	TE (Escape Trigger) on the next V-Synch.
25	-	-	<=	LP-11	-	
26	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
27	-	LP-11	=>	-	-	End
28						
29	-	-	<=	LPDT	AwER	Error Report
30	-	-	<=	LP-11	-	
31	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
32	-	LP-11	=>	-	-	If the MCU is not forcing BTA => Goto Line 33 If the MCU is forcing BTA => Goto Line 35
33	-	LP-11	=>	-	-	End
34						
35	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
36	-	-	<=	LP-11	-	Dead-Lock (No TE information) See Note 2
37	-	LP-11	=>	-	-	The MCU is forced to start to control the interface. The display module detects Bus Connection Error (BCE)
38	-	BTA	<=>	BTA	-	Interface Control Change from the MCU to the display module
39	-	-	<=	LP-11	-	
40	-	-	<=	LPDT	AwER	Error Report (Bus Connection Error (BCE) is reported) See Note 2
41	-	-	<=	LP-11	-	
42	-	BTA	<=>	BTA	-	Interface Control Change from the display module to the MCU
43	-	LP-11	=>	-	-	End

Notes:

1. Lines 1 – 16 are needed for every frame.
2. Bits 5 and 7 of the AwER are applied.

6.11.2.8. Tearing effect bus trigger enable sequence – DCSWN-S and HPDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	Tearing Effect Bus Trigger Disable
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

6.11.2.9. Tearing effect bus trigger enable sequence – DCSWN-S and LPDT

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	LPDT	=>	-	-	Tearing Effect Bus Trigger Disable
3	-	LP-11	=>	-	-	End

6.12. Checksum

The display module consists of two 8-bit checksum registers, which are used checksum calculations for area registers (includes the frame memory), on the display module. Area registers are registers which values can change a command directly. One of the checksum registers is "First Checksum" (FCS) and another is "Continue Checksum" (CCS). These register values are set to 00h as an initial value when there is started to calculate a new checksum. The display module is starting to calculate the new checksum after there is a write access on area registers. This means that read commands are not used as a calculation starting trigger in this case. The checksum calculation is always interrupted, when there is a new write access on area registers. The checksum calculation is also started from the beginning. The result of the first finished checksum calculation is stored on the FCS register, which value is kept until there is the new write access on area registers and the new checksum value is calculated in the first time again.

The maximum time, when the FCS is readable, is 150ms after there is the last write access on area registers.

The checksum calculation is continuing after the finished first checksum calculation where the FCS has gotten the checksum value. These new checksum values are always stored on CCS register (Old value is replaced a new one) after the last area register has been calculated to the checksum.

The maximum time, when the CCS is readable in the first time, is 300ms after there is the last write access on area registers.

There is always updated a checksum comparison bit (See command "Read Display Self-Diagnostic Result (0FH)" and bit D0) when there is compared FCS and CCS checksums after a new checksum value is stored on CCS.

The maximum time, when the comparison has been done between FCS and CCS in the first time, is 300ms then the comparison has been done in every 150ms (this is maximum time). Area can read FCS, CCS and Comparison bit D0 values. See command: "Read First Checksum (AAH)", "Read Continue Checksum (AFH)" and "Read Display Self-Diagnostic Result (0FH)".

There can be an overflow during a checksum calculation. These overflow bits are not needed to store anywhere. This means that these overflow bits can be ignored by the display module.

An example of the checksum calculation:

- Register Values: A1h, 12h, 81h, DEh, F2h
- Calculated Value: 304h (= A1h + 12h + 81h + DEh + F2h)
- Ignored Bits: 3h
- Stored Checksum: 04h

This checksum calculation function is only running in "Sleep Out" mode and it is stopped in "Sleep In" mode.

Checksum Sequence

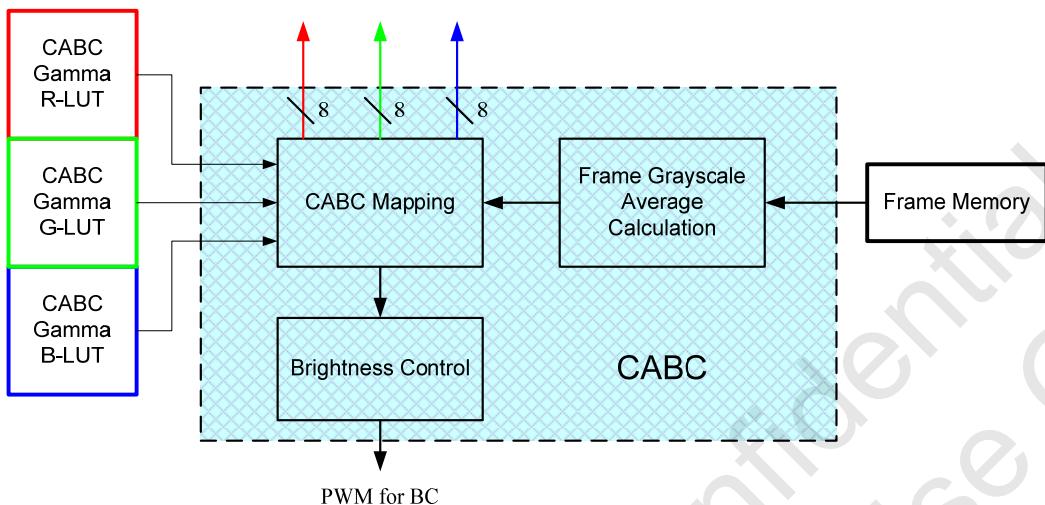
Step Note 1	Time Note 2	Action	Temporary Register	First Checksum Register (FCS)	Continue Checksum Register (CCS)	Comment
1	0	Initialization	Set to 00h	Set to 00h	Set to 00h	The last write action on Nokia area registers => FCS and CCS registers are initialized.
2	0 – 150ms	Counting Sum of Nokia Area Registers	Counting	-	-	The first register counting is running
3	150ms	Stores Sum of Registers on FCS Register	Set to 00h after Value is Moved to FCS Register	Stores Sum of Nokia Area Registers on FCS Register	-	The result of the first register counting is stored on the FCS register. The result of the FCS is available to the MCU.
4	150 – 300ms	Counting Sum of Nokia Area Registers	Counting	-	-	The second register counting is running
5	300ms	1) Stores Sum of Registers on CCS Register 2) Compares Stored FCS and CCS Values	Set to 00h after Value is Moved to CCS Register	-	Stores Sum of Nokia Area Registers on CCS Register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MCU.
6	300 – 450ms	Counting Sum of Nokia Area Registers	Counting	-	-	The third register counting is running
7	450ms	1) Stores Sum of Registers on CCS Register 2) Compares Stored FCS and CCS Values	Set to 00h after Value is Moved to CCS Register	-	Stores Sum of Nokia Area Registers on CCS Register	The result of the comparison is stored on separated registers, which can read separated read commands. The latest result of the CCS and comparison result are available to the MCU.
8	450 – 600ms	Counting Sum of Nokia Area Registers	Counting	-	-	The fourth register counting is running
9	600ms	1) Stores Sum of Registers on CCS Register 2) Compares Stored FCS and CCS Values	Set to 00h after Value is Moved to CCS Register	-	Stores Sum of Nokia Area Registers on CCS Register	The result of the comparison is stored on separated registers, which can read separated read commands. The latest result of the CCS and comparison result are available to the MCU.
10	etc	-	-	-	-	Same Sequence Continue e.g. steps 4 and 5

Notes:

1. This function is restarted at Step 1 if there is any write action on area registers.
2. These time can be shorter on the display module.

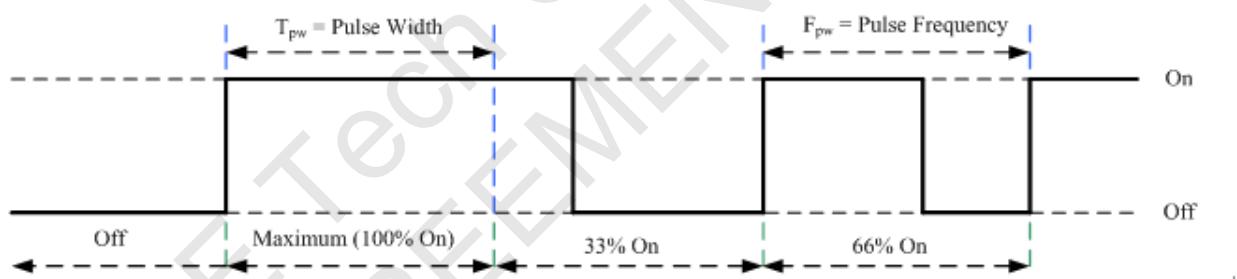
6.13. Content Adaptive Brightness Control (CABC)

Content adaptation means that content grey level scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. CABC block diagram is shown as below:



6.13.1. Backlight(BC) Brightness Control

Use the PWM output to control backlight. BC timing is described as below graph:



Symbol	Definition	MIN		Max.	Unit
t _{pw}	Pulse Width	0.0073		15.15	ms
F _{pw}	PWM Frequency	66		136.7k	Hz

6.14. Duty Ratio Mapping Table For Backlight PWM Pulse

The duty calculation rule: if (DBV = 0) Duty = 0 else Duty = (DBV[7:0]+1)/256

DBV[7:0]	Brightness Level	PWM High Duty(%)	Remark
0000_0000	0	0.00	
0000_0001	1	0.78	
0000_0010	2	1.17	
0000_0011	3	1.56	
0000_0100	4	1.95	
0000_0101	5	2.34	
0000_0110	6	2.73	
0000_0111	7	3.13	
0000_1000	8	3.52	
0000_1001	9	3.91	
0000_1010	10	4.30	
0000_1011	11	4.69	
0000_1100	12	5.08	
0000_1101	13	5.47	
0000_1110	14	5.86	
0000_1111	15	6.25	
0001_0000	16	6.64	
0001_0001	17	7.03	
0001_0010	18	7.42	
0001_0011	19	7.81	
0001_0100	20	8.20	
0001_0101	21	8.59	
0001_0110	22	8.98	
0001_0111	23	9.38	
0001_1000	24	9.77	
0001_1001	25	10.16	
0001_1010	26	10.55	
0001_1011	27	10.94	
0001_1100	28	11.33	
0001_1101	29	11.72	
0001_1110	30	12.11	
0001_1111	31	12.50	
0010_0000	32	12.89	
0010_0001	33	13.28	
0010_0010	34	13.67	
0010_0011	35	14.06	
0010_0100	36	14.45	
0010_0101	37	14.84	
0010_0110	38	15.23	
0010_0111	39	15.63	
0010_1000	40	16.02	
0010_1001	41	16.41	
0010_1010	42	16.80	
0010_1011	43	17.19	
0010_1100	44	17.58	
0010_1101	45	17.97	
0010_1110	46	18.36	
0010_1111	47	18.75	
0011_0000	48	19.14	
0011_0001	49	19.53	
0011_0010	50	19.92	
0011_0011	51	20.31	
0011_0100	52	20.70	
0011_0101	53	21.09	

DBV[7:0]	Brightness Level	PWM High Duty(%)	Remark
0011_0110	54	21.48	
0011_0111	55	21.88	
0011_1000	56	22.27	
0011_1001	57	22.66	
0011_1010	58	23.05	
0011_1011	59	23.44	
0011_1100	60	23.83	
0011_1101	61	24.22	
0011_1110	62	24.61	
0011_1111	63	25.00	
0100_0000	64	25.39	
0100_0001	65	25.78	
0100_0010	66	26.17	
0100_0011	67	26.56	
0100_0100	68	26.95	
0100_0101	69	27.34	
0100_0110	70	27.73	
0100_0111	71	28.13	
0100_1000	72	28.52	
0100_1001	73	28.91	
0100_1010	74	29.30	
0100_1011	75	29.69	
0100_1100	76	30.08	
0100_1101	77	30.47	
0100_1110	78	30.86	
0100_1111	79	31.25	
0101_0000	80	31.64	
0101_0001	81	32.03	
0101_0010	82	32.42	
0101_0011	83	32.81	
0101_0100	84	33.20	
0101_0101	85	33.59	
0101_0110	86	33.98	
0101_0111	87	34.38	
0101_1000	88	34.77	
0101_1001	89	35.16	
0101_1010	90	35.55	
0101_1011	91	35.94	
0101_1100	92	36.33	
0101_1101	93	36.72	
0101_1110	94	37.11	
0101_1111	95	37.50	
0110_0000	96	37.89	
0110_0001	97	38.28	
0110_0010	98	38.67	
0110_0011	99	39.06	
0110_0100	100	39.45	
0110_0101	101	39.84	
0110_0110	102	40.23	
0110_0111	103	40.63	
0110_1000	104	41.02	
0110_1001	105	41.41	
0110_1010	106	41.80	
0110_1011	107	42.19	

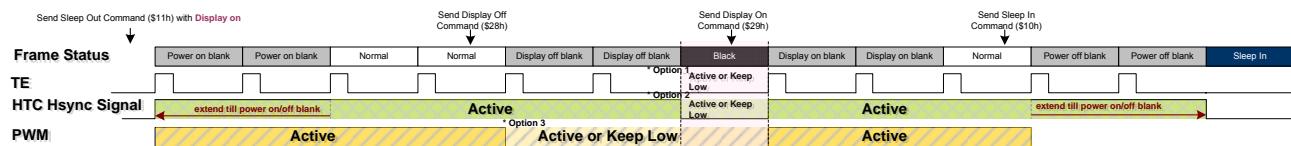
DBV[7:0]	Brightness Level	PWM High Duty(%)	Remark
0110_1100	108	42.58	
0110_1101	109	42.97	
0110_1110	110	43.36	
0110_1111	111	43.75	
0111_0000	112	44.14	
0111_0001	113	44.53	
0111_0010	114	44.92	
0111_0011	115	45.31	
0111_0100	116	45.70	
0111_0101	117	46.09	
0111_0110	118	46.48	
0111_0111	119	46.88	
0111_1000	120	47.27	
0111_1001	121	47.66	
0111_1010	122	48.05	
0111_1011	123	48.44	
0111_1100	124	48.83	
0111_1101	125	49.22	
0111_1110	126	49.61	
0111_1111	127	50.00	
1000_0000	128	50.39	
1000_0001	129	50.78	
1000_0010	130	51.17	
1000_0011	131	51.56	
1000_0100	132	51.95	
1000_0101	133	52.34	
1000_0110	134	52.73	
1000_0111	135	53.13	
1000_1000	136	53.52	
1000_1001	137	53.91	
1000_1010	138	54.30	
1000_1011	139	54.69	
1000_1100	140	55.08	
1000_1101	141	55.47	
1000_1110	142	55.86	
1000_1111	143	56.25	
1001_0000	144	56.64	
1001_0001	145	57.03	
1001_0010	146	57.42	
1001_0011	147	57.81	
1001_0100	148	58.20	
1001_0101	149	58.59	
1001_0110	150	58.98	
1001_0111	151	59.38	
1001_1000	152	59.77	
1001_1001	153	60.16	
1001_1010	154	60.55	
1001_1011	155	60.94	
1001_1100	156	61.33	
1001_1101	157	61.72	
1001_1110	158	62.11	
1001_1111	159	62.50	
1010_0000	160	62.89	
1010_0001	161	63.28	
1010_0010	162	63.67	
1010_0011	163	64.06	
1010_0100	164	64.45	

DBV[7:0]	Brightness Level	PWM High Duty(%)	Remark
1010_0101	165	64.84	
1010_0110	166	65.23	
1010_0111	167	65.63	
1010_1000	168	66.02	
1010_1001	169	66.41	
1010_1010	170	66.80	
1010_1011	171	67.19	
1010_1100	172	67.58	
1010_1101	173	67.97	
1010_1110	174	68.36	
1010_1111	175	68.75	
1011_0000	176	69.14	
1011_0001	177	69.53	
1011_0010	178	69.92	
1011_0011	179	70.31	
1011_0100	180	70.70	
1011_0101	181	71.09	
1011_0110	182	71.48	
1011_0111	183	71.88	
1011_1000	184	72.27	
1011_1001	185	72.66	
1011_1010	186	73.05	
1011_1011	187	73.44	
1011_1100	188	73.83	
1011_1101	189	74.22	
1011_1110	190	74.61	
1011_1111	191	75.00	
1100_0000	192	75.39	
1100_0001	193	75.78	
1100_0010	194	76.17	
1100_0011	195	76.56	
1100_0100	196	76.95	
1100_0101	197	77.34	
1100_0110	198	77.73	
1100_0111	199	78.13	
1100_1000	200	78.52	
1100_1001	201	78.91	
1100_1010	202	79.30	
1100_1011	203	79.69	
1100_1100	204	80.08	
1100_1101	205	80.47	
1100_1110	206	80.86	
1100_1111	207	81.25	
1101_0000	208	81.64	
1101_0001	209	82.03	
1101_0010	210	82.42	
1101_0011	211	82.81	
1101_0100	212	83.20	
1101_0101	213	83.59	
1101_0110	214	83.98	
1101_0111	215	84.38	
1101_1000	216	84.77	
1101_1001	217	85.16	
1101_1010	218	85.55	
1101_1011	219	85.94	
1101_1100	220	86.33	
1101_1101	221	86.72	

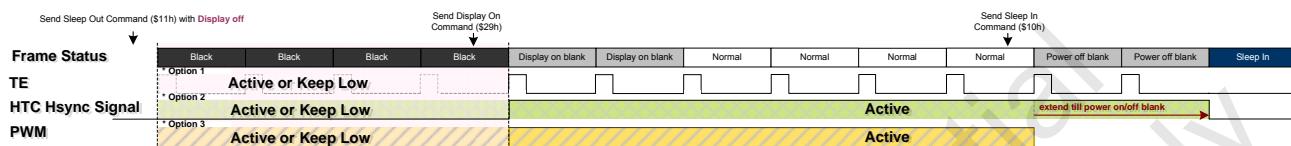
DBV[7:0]	Brightness Level	PWM High Duty(%)	Remark
1101_1110	222	87.11	
1101_1111	223	87.50	
1110_0000	224	87.89	
1110_0001	225	88.28	
1110_0010	226	88.67	
1110_0011	227	89.06	
1110_0100	228	89.45	
1110_0101	229	89.84	
1110_0110	230	90.23	
1110_0111	231	90.63	
1110_1000	232	91.02	
1110_1001	233	91.41	
1110_1010	234	91.80	
1110_1011	235	92.19	
1110_1100	236	92.58	
1110_1101	237	92.97	
1110_1110	238	93.36	
1110_1111	239	93.75	
1111_0000	240	94.14	
1111_0001	241	94.53	
1111_0010	242	94.92	
1111_0011	243	95.31	
1111_0100	244	95.70	
1111_0101	245	96.09	
1111_0110	246	96.48	
1111_0111	247	96.88	
1111_1000	248	97.27	
1111_1001	249	97.66	
1111_1010	250	98.05	
1111_1011	251	98.44	
1111_1100	252	98.83	
1111_1101	253	99.22	
1111_1110	254	99.61	
1111_1111	255	100.00	

6.15. PWM/TE/HSYNC output Control

Case-1



Case-2



* Option 1

Control by `reg_te_dispoff_act ($C0B2h, D0)`

1 : TE keep low during display off area

0 : TE keep toggle during display off area

* Option 2

Control by `reg_stb_dispoff_act ($C0E1h, D4)`

1 : htc hsync keep low during display off area

0 : htc hsync keep toggle during display off area

* Option 3

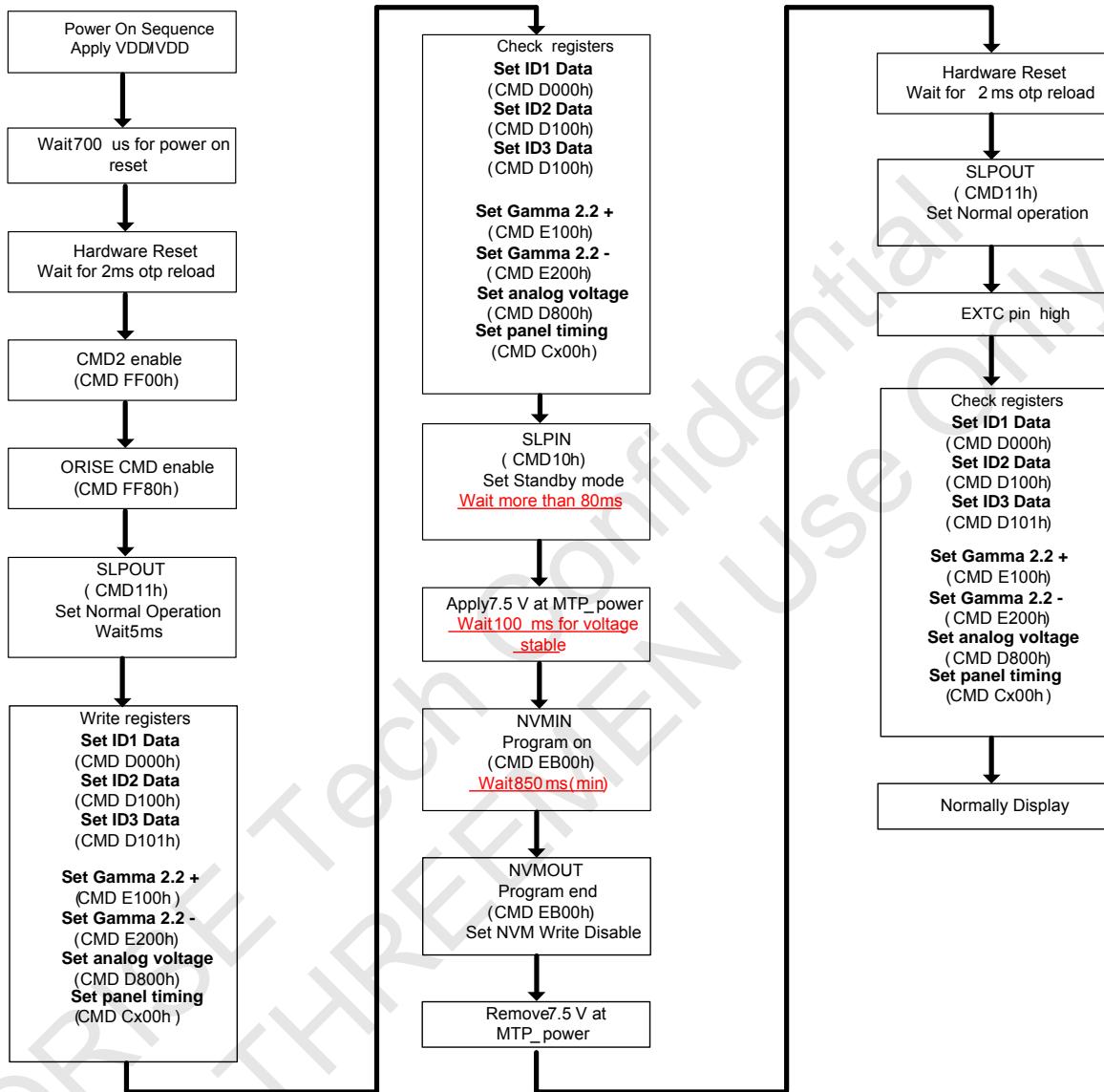
Control by `reg_pwm_dispoff_act ($CAA3h, D0)`

1 : PWM keep low during display off area

0 : PWM keep toggle during display off area

6.16. NVM Programming Procedure

6.16.1. NVM program flow chart



6.16.2. Analog Gamma programming and checking flow

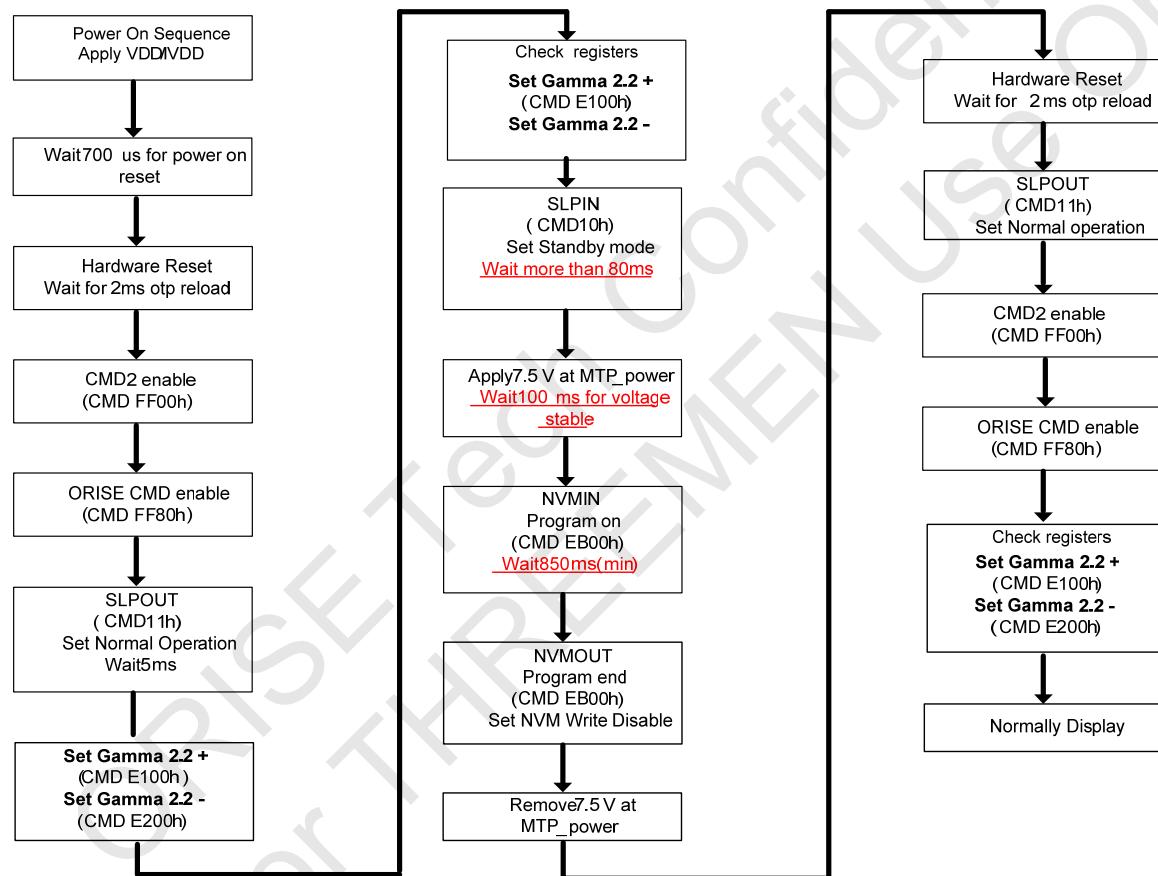
Method-A

Analog Gamma	OTP_SEL	Programming status
0	x	No
1	0	1st
1	1	2nd

Register bit for Analog Gamma : AE8Fh D5

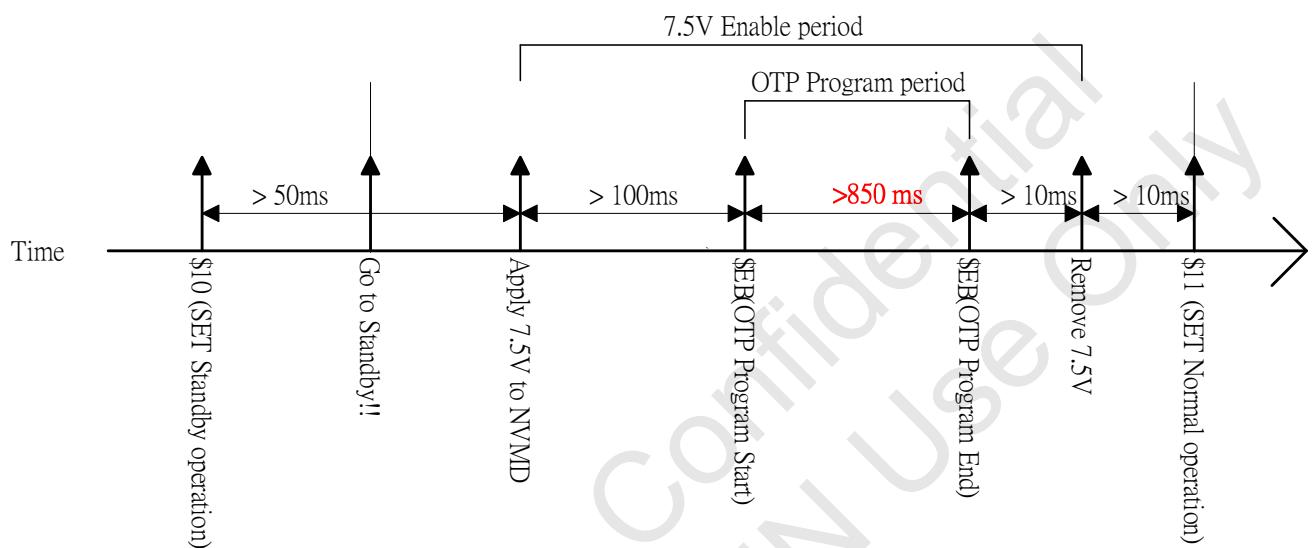
OTP_SEL bit : A000h D0

Method-B : Check E1h/E2h registers



6.16.3. Programming sequence

Figure 6.9.1 shows the sequence about NVM. The first step to program NVM is “write Standby operation command”. After this command, over than 50ms must be hold to make sure that the dirver IC is in Standby mode. Another 100ms is necessary to make sure NVMD is stable to 7.5V. NVM program command can be written after stable 7.5V voltage existed. Then, NVM Program End command is written after **850ms**. 7.5V voltage is removed after Program End command, and then Normal operation command is written to verify the NVM memory.



7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply for I/O	VDDIO-VSS	-0.3~+4.5	V
Power Supply for HSSI Interface	VDDAM-AVSS	-0.3~+6.0	V
Power Supply for logic power regulator	VCC-VSS	-0.3~+6.0	V
Power Supply for Analog circuit	VDD-AVSS	-0.3~+6.0	V
Power Supply for OTP	MTP_PWR-AVSS	-0.3~+7.8	V
I/O input Voltage	Vt	-0.3~VDDIO+0.3	V
Driver output voltage	VGH-VGL	-0.3~+32	V
Differential Input Voltage	HSSI_CLK_P/N HSSI_D0_P/N HSSI_D1_P/N HSSI_D2_P/N	-0.3~1.8	V
Operating Temperature	Topr	-30~+70	°C
Storage Temperature	Tstg	-30~+85	°C

Note1. The maximum applicable voltage on any pin with respect to 0V.

Note2. Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

7.2. DC Characteristic

7.2.1. Basic DC characteristic

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VDD	Operating Voltage	2.3	2.8/3.7	4.8	V	Note3
Logic Operating voltage	VDDIO	I/O supply voltage	1.65	1.8	3.3	V	
	VDDIOL		1.1	1.2	1.3	V	
Digital Operating voltage	VCC	Digital supply voltage	2.3	2.8/3.7	4.8	V	
Hissi interface Operating voltage	VDDAM	MIPPI/MDDI supply voltage	2.3	2.8/3.7	4.8	V	
Input / Output							
Logic High level input voltage	VIH		0.7VDDIO	-	VDDIO	V	
Logic Low level input voltage	VIL	-	VSS	-	0.3VDDIO	V	
Logic High level output voltage	VOH	IOH = -1.0mA	0.8VDDIO	-	VDDIO	V	
Logic Low level output voltage	VOL	IOL = +1.0mA	VSS	-	0.2VDDIO	V	
Logic High level input current	IIH	Vin = VDDIO or VDDAM			1	μA	
Logic Low level input current	IIL	Vin = VDDIO or VDDAM	-1			μA	
VCOM Operation							
VCOMDC output voltage	VCOM		-3.475	-1.0	0	V	
Source Driver							
Gamma positive reference voltage	VGMP	VGMP<VDDA-0.3V	3.1125		6.3	V	
Gamma negative reference voltage	VGMN	VGMN>NVDDA-0.3V	-6.3		-3.1125	V	
Source output voltage	VSD		VGMN		VGMP		
Output deviation voltage (Source positive output channel)	V,dev	Sout >=+4.2V, Sout<=+0.8V		20	30	mV	
		+4.2V>Sout>+0.8V		15	20	mV	
Output deviation voltage (Source negative output channel)	V,dev	Sout <=-4.2V, Sout>=-0.8V		20	30	mV	
		-4.2V<Sout<-0.8V		15	20	mV	
Output offset voltage	V _{OFFSET}				35	mv	
Reference Voltage							
Internal reference voltage	V _{REF}		1.96	2	2.04	V	
Booster operation							
1 st booster output voltage	VDDA	Range =1xVDD~3xVDD			6.75	V	
	NVDDA	Range = -1xVDDA			-6.75	V	
2 nd booster output voltage	VGH	Range=(2xVDDA-NVDD A) ~ (3xVDDA-NVDDA)	11.5		19	V	
	VGL	Range=(NVDDA-VDDA) ~(2xNVDDA-VDDA)	-7		-16	V	
3 rd booster output voltage	VCL	Range= -1xVDD	-2.3		-3.5	V	
OSC Frequency							
Oscillator Frequency(MCK) with 540x960 Mode	fosc11	Frame rate =70Hz	4.816	5.069	5.323	MHz	
	fosc12	Frame rate =60Hz	4.128	4.345	4.562	MHz	
	fosc13	Frame rate =50Hz	3.440	3.621	3.802	MHz	
	fosc14	Frame rate =40Hz	2.752	2.897	3.041	MHz	

Oscillator Frequency for PWM pulse generation	Fosc2		16.625	17.5	18.375	MHz	
Current consumption							
Sleep-IN mode (LP-11) (RAM power is ON)	IVDDIO	RESX=High		5	10	uA	Note4
	IVDD			140	200	uA	
Sleep-IN mode (ULPS) (RAM power is OFF)	IVDDIO	RESX=HIGH		5	10	uA	
	IVDD			30	70	uA	
Sleep-IN mode (MDDI, Hibernation) (RAM power is OFF)	IVDDIO	RESX=High		5	10	uA	
	IVDD			70	120	uA	

Note1. Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

Note2. Test condition is at 25°C and without panel loading.

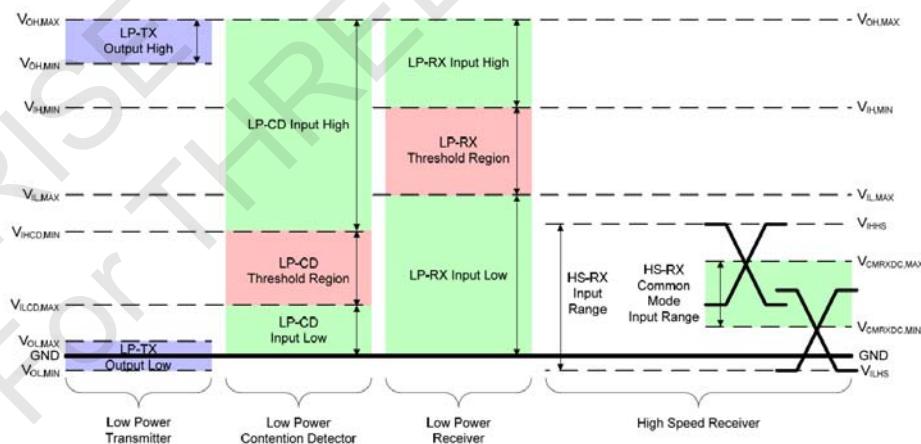
Note3. The case of (VDD,VDDAM, VCC) < VDDIO is not supported in this IC.

Note4. For Display RAM power=ON case, the temperature condition is at 25°C . It's including RAM with 00h/FFh data

7.2.2. MIPI DC character

Table 7.2.2.1: DC Characteristics for MIPI-DSI

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Power supply voltage for MIPI Interface						
Power supply voltage for MIPI interface	VDDAM	-	1.65	2.8	4.8	V
	VLPH	For LPDT	1.1	1.2	1.3	V
	VP_HISSI	-	1.5	1.55	1.6	V
LPDT Input Characteristics						
Pad signal voltage range	VI	-	-50	-	1350	mV
Ground Shift	VGNDH	-	-50	-	50	mV
Logic 0 input threshold	VIL	-	0	-	550	mV
Logic 1 input threshold	VIH	-	880	-	VDDAM	mV
Input hysteresis	VHYST	-	25	-	-	mV
LPDT Output Characteristics						
Output low level	VOL	-	-50	-	50	mV
Output high level	VOH	-	1.1	1.2	1.3	V
Logic 1 contention threshold	VILCD,MIN	-	450	-	VDDAM	mV
Logic 0 contention threshold	VIHCD,MAX	-	0	-	200	mV
Output impedance of LPDT	ZOLP	-	80	100	125	ohm
Hi-speed Input/Output Characteristics						
Single-end input low voltage	VILHS	-	-40	-	-	mV
Single-end input high voltage	VIHHS	-	-	-	460	mV
Common mode voltage	VCMRXDC	-	70	-	330	mV
Hi-speed transmit voltage	VOD	-	140	200	250	mV
Differential input impedance	ZID	-	80	100	125	ohm



7.2.3. MDDI DC character

Table 7.2.3.: DC Characteristics for MDDI

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Power supply voltage for MDDI interface	VDDAM	-	1.65	2.8	4.8	V
Data input high level voltage	VIT+off		-	100	125	mV
Data input low level voltage	VIT-off		75	100	-	mV
Data/Strobe input high level voltage	VIT+	VT=0V	-	0	50	mV
Data/Strobe input low level voltage	VIT-	VT=0V	-50	0	-	mV
Current consumption in Hibernation	Ihib	VDDAM=2.8V ; 550Mbps	-	40	-	uA
Current consumption in Data transfer	Itrans	VDDAM=2.8V ; 550Mbps	-	4	-	mA
Differential input impedance	Zt	-	80	100	125	Ohm

7.3. AC timing Characteristics

7.3.1. MIPI-DSI characteristics

Table 7.3.1.: AC Characteristics for MIPI-DSI

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Hi-Speed mode						
DSI CLK Frequency (HS)	fDSICLK_HS	DDR mode	40		275	MHz
DSI CLK Cycle Time (HS)	tCLKP_HS	DDR mode	1.82		25	ns
DSI Data0/1/2 Transfer Rate (HS)	tDSIR_HS	DDR mode	80		550	Mbps
DSI Data0/1/2 Cycle Time (HS)	tDATAP_HS	DDR mode	1.82		25	ns
UI instantaneous	Ulinst		1.82		25	ns
Data lane to Clock lane Skew	TSKEW[TX]		-0.15		0.15	Ulinst
Data lane to Clock lane Setup Time	TSETUP[RX]		0.15			Ulinst
Data lane to Clock lane Hold Time	THOLD[RX]		0.15			Ulinst
Low Power Data Transfer (LPDT)						
DSI CLK Frequency (LPDT)	fDSICLK_LP		0.5		10	MHz
DSI CLK Cycle Time (LPDT)	tCLKP_LP		2		0.1	us
DSI Data0 Transfer Rate (LPDT)	tDSIR_LP		1		10	Mbps

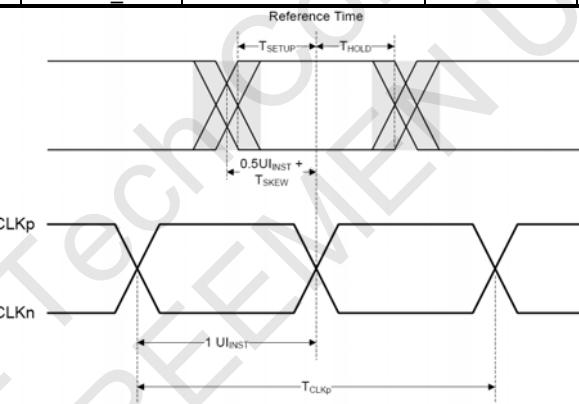
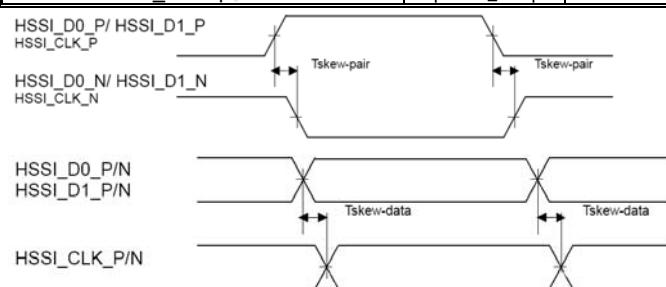


Fig. 7.3.1.: AC Characteristics for MIPI-DSI

7.3.2. MDDI AC timing Characteristics

Table 7.3.2.: AC Characteristics for MDDI

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Data Transfer Speed	1/tBIT	VCI=2.3V~5.5V VDDIO=1.65~3.6V TA=-30~+70°C	-	384	550	Mbps
Transfer input skew	Tskew_Pair		-	-	50	ps
Data_Stb input skew	Tskew_Data		-	-	300	ps



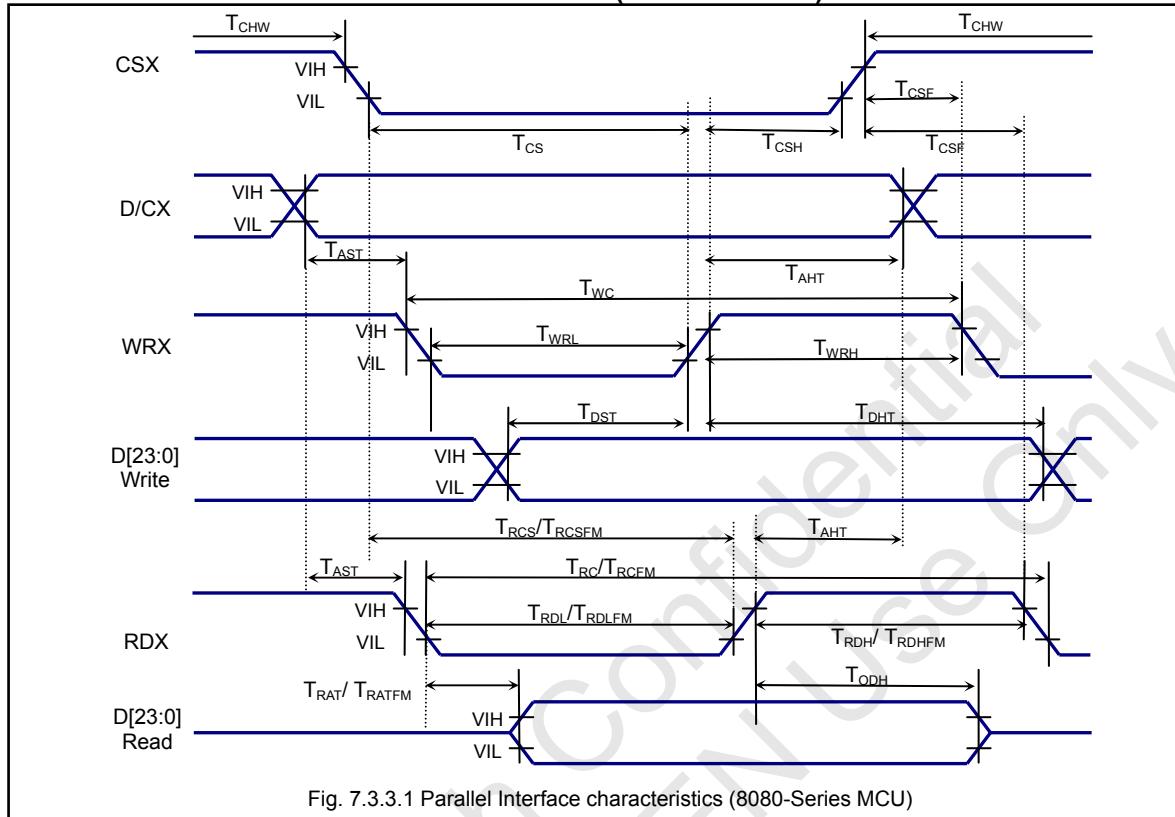
7.3.3. Allel Interface Characteristics 24/18/16/9/8-bits bus (8080-series MCU)


Table 7.3.3.1: AC Characteristics for Parallel Interface 24/18/16/8-bits bus (8080-series MCU)

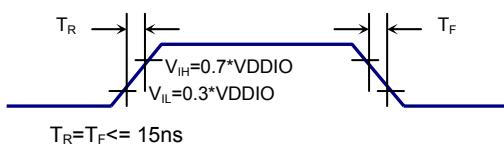
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
D/CX	T _{AST}	Address setup time	0		ns	-
	T _{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T _{CHW}	Chip select "H" pulse width	0		ns	-(3-transfer for one pixel) -(1-transfer for one pixel)
	T _{CS}	Chip select setup time (Write)	15		ns	
	T _{RCS}	Chip select setup time (Read ID)	45		ns	
	T _{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T _{CSF}	Chip select wait time (Write/Read)	10		ns	
	T _{CSH}	Chip select hold time	10		ns	
WRX	T _{WC}	Write cycle	66		ns	
	T _{WRH}	Control pulse "H" duration	15		ns	
	T _{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T _{RC}	Read cycle (ID)	160		ns	When read ID1~ID3 data
	T _{RDH}	Control pulse "H" duration (ID)	90		ns	
	T _{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T _{RCFM}	Read cycle (FM = Frame Memory)	450		ns	When read from frame memory
	T _{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T _{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[23:0]	T _{DST}	Data setup time	10		ns	For maximum C _L =30pF For minimum C _L =8pF
	T _{DHT}	Data hold time	10		ns	
	T _{RAT}	Read access time (ID)		40	ns	
	T _{RATFM}	Read access time (FM)		340	ns	
	T _{ODH}	Output disable time	20	80	ns	

Note 1: VDDIO=1.65 to 3.6V, VCI=2.3 to 5.5V, VSSA=VSS=0V, Ta=-30 to 70°C

Note 2: The input signal rise time and fall time (Tr, Tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDDIO for Input signals.

Input Signal Slope



Output Signal Slope

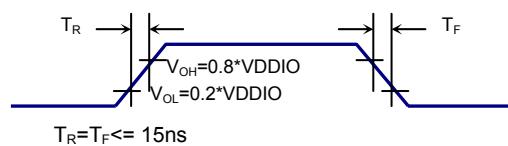


Fig. 7.3.3.2 Rising and Falling timing for Input and Output signal

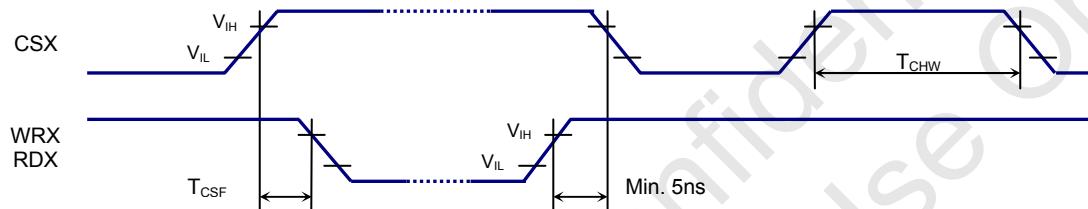


Fig. 7.3.3.3 Chip selection (CSX) timing

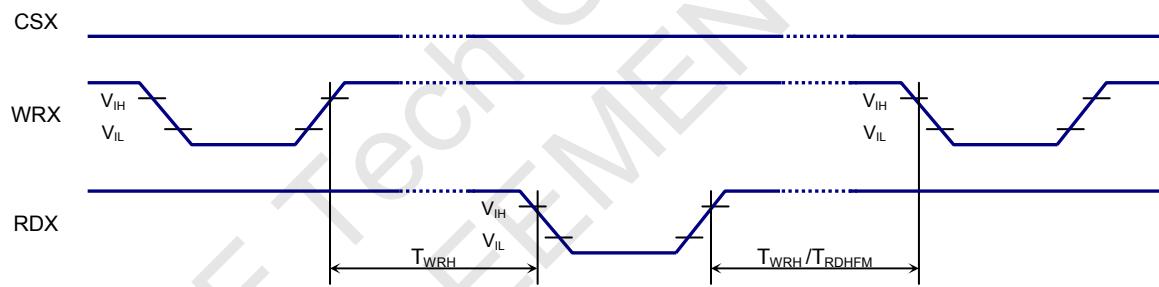


Fig. 7.3.3.4 Write to read and Read to write timing

7.3.4. Parallel Interface Characteristics 24/18/16/9/8-bits bus (6800-series MCU)

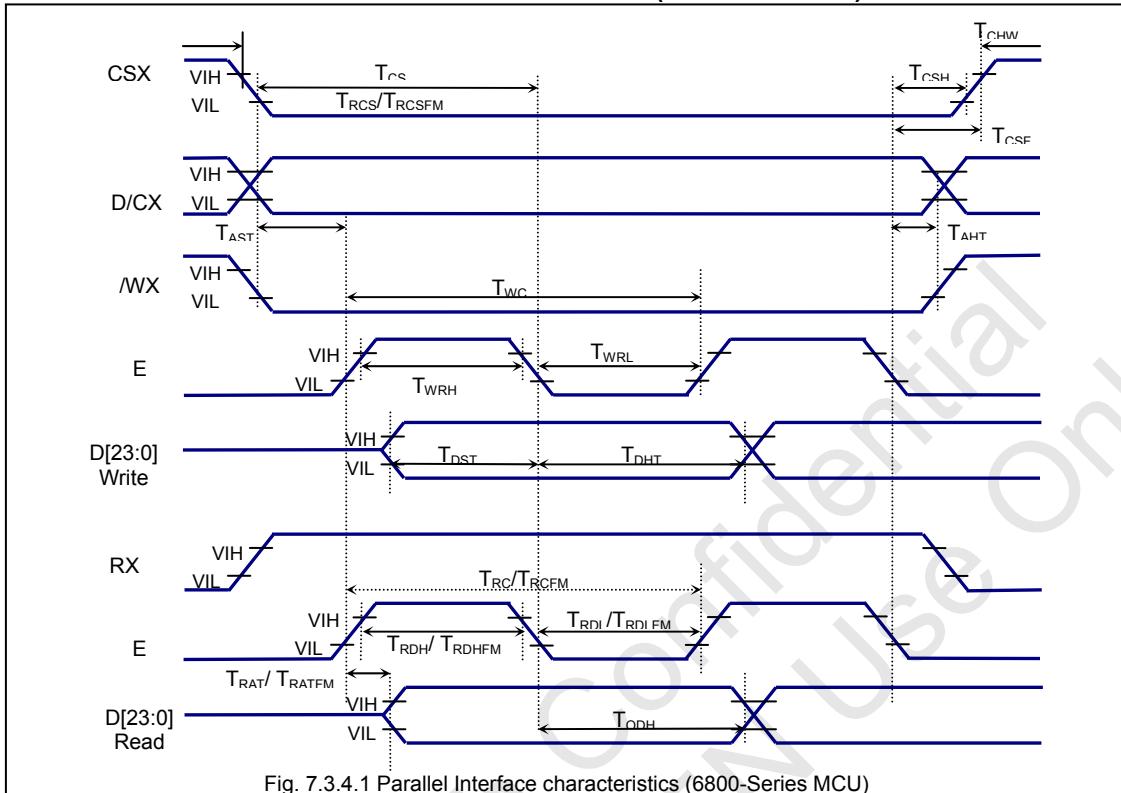


Table 7.3.4.1: AC Characteristics for Parallel Interface 24/18/16/9/8-bits bus (6800-series MCU)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
D/CX	T _{AST}	Address setup time	0		ns	-
	T _{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T _{CHW}	Chip select "H" pulse width	0		ns	-
	T _{CS}	Chip select setup time (Write)	15		ns	
	T _{RCS}	Chip select setup time (Read ID)	45		ns	
	T _{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T _{CSF}	Chip select wait time (Write/Read)	10		ns	
	T _{CSH}	Chip select hold time	10		ns	
E	T _{WC}	Write cycle	66		ns	-
	T _{WRH}	Control pulse "H" duration	15		ns	
	T _{WRL}	Control pulse "L" duration	15		ns	
E (ID)	T _{RC}	Read cycle (ID)	160		ns	When read ID data
	T _{RDH}	Control pulse "H" duration (ID)	90		ns	
	T _{RDL}	Control pulse "L" duration (ID)	45		ns	
E (FM)	T _{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T _{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T _{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[23:0]	T _{DST}	Data setup time	10		ns	For maximum C _L =30pF For minimum C _L =8pF
	T _{DHT}	Data hold time	10		ns	
	T _{RAT}	Read access time (ID)		40	ns	
	T _{RATFM}	Read access time (FM)		340	ns	
	T _{ODH}	Output disable time	20	80	ns	

Note 1: VDDIO=1.65 to 3.6V, VCI=2.3 to 5.5V, VSSA=VSS=0V, Ta=-30 to 70°C

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDDIO for Input signals.

7.3.5. Serial Interface Characteristics (SPI)

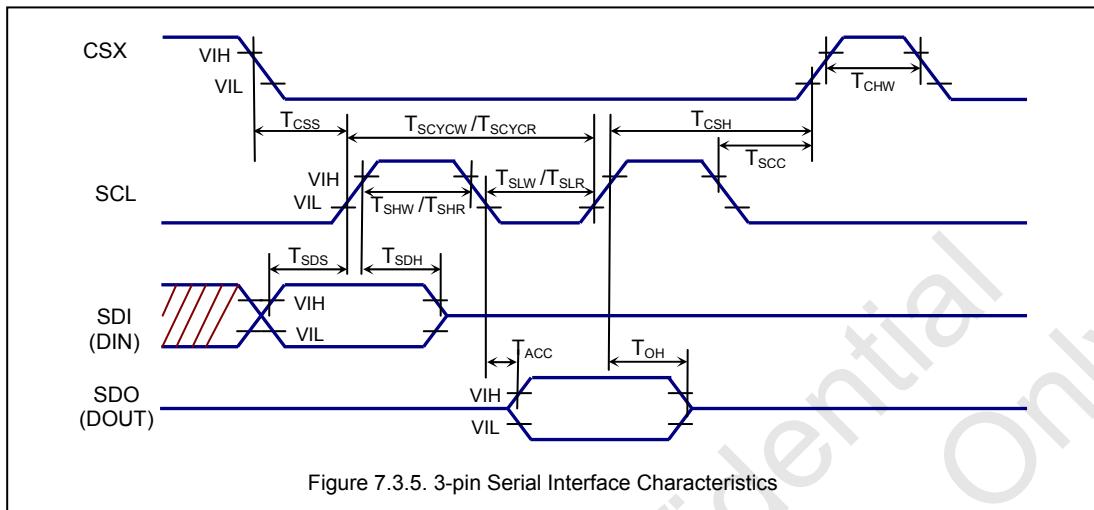


Table 7.3.5. SPI Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T _{CSS}	Chip select setup time	15	-	ns	
	T _{CSH}	Chip select hold time	15	-	ns	
	T _{SCC}	Chip select setup time	20	-	ns	
	T _{CHW}	Chip select setup time	40	-	ns	
SCL	T _{SCYCW}	Serial clock cycle (Write)	66	-	ns	
	T _{SHW}	SCL "H" pulse width (Write)	10	-	ns	
	T _{SLW}	SCL "L" pulse width (Write)	10	-	ns	
	T _{SCYCR}	Serial clock cycle (Read)	150	-	ns	
	T _{SHR}	SCL "H" pulse width (Read)	60	-	ns	
	T _{SLR}	SCL "L" pulse width (Read)	60	-	ns	
SDA (DIN) (DOUT)	T _{SDS}	Data setup time	10	-	ns	
	T _{SDH}	Data hold time	10	-	ns	
	T _{ACC}	Access time	10	50	ns	For maximum C _L =30pF
	T _{OH}	Output disable time	15	50	ns	For minimum C _L =8pF

Note 1: VDDIO=1.65 to 3.6V, VCI=2.3 to 5.5V, VSSA=VSS=0V, Ta=-30 to 70°C

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDDIO for Input signals.

7.3.6. RGB Interface Characteristics

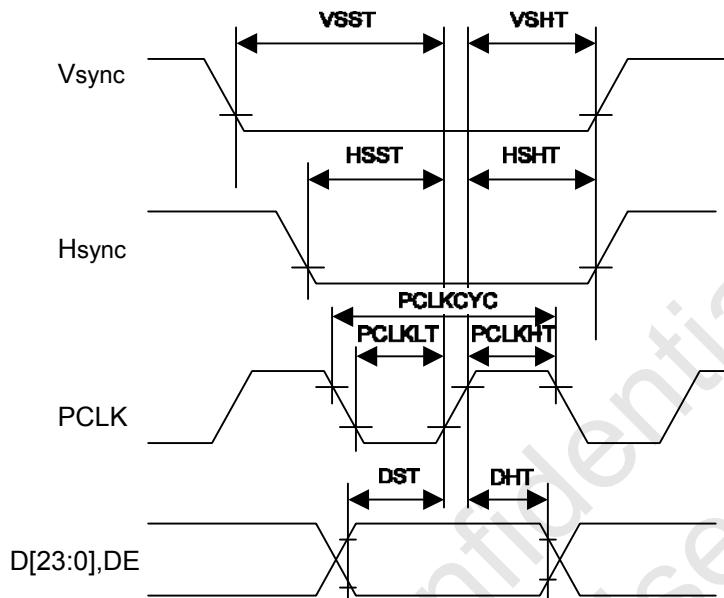


Figure 7.3.6. AC Timing Characteristics, RGB Interface

Table 7.3.6. RGB Interface Characteristics

(VCI=2.3V~5.5V, VDDIO = 1.65V~3.6V, Ta = -40°C ~ 85°C)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Vsync	VSST	VS setup time	5	-	ns	
	VSHT	VS hold time	5	-	ns	
Hsync	HSST	HS setup time	5	-	ns	
	HSHT	HS hold time	5	-	ns	
PCLK		Pixel clock duty cycle	33	67	%	
	PCLKLT	Pixel clock low duration	14	-	ns	
	PCLKHT	Pixel clock high duration	14	-	ns	
D [23:0], DE	DST	Data setup time	5	-	ns	
	DHT	Date hold time	5	-	ns	

7.3.7. I²C Interface characteristics

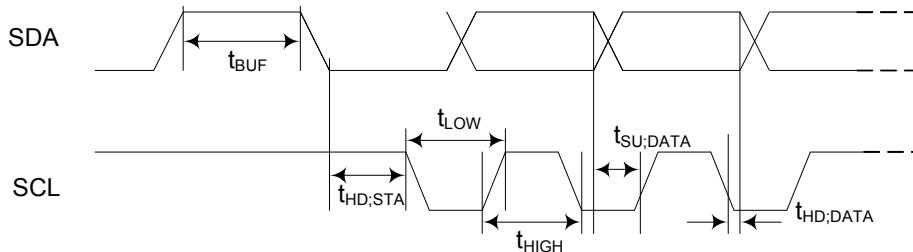


Table 7.3.7.1 I²C Interface Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCLK}	SCL clock frequency		DC	-	400	KHz
t_{LOW}	SCL clock LOW period		1.3	-	-	μ s
t_{HIGH}	SCL clock HIGH period		0.6	-	-	μ s
$t_{SU:DATA}$	data set-up time		100	-	-	ns
$t_{HD:DATA}$	data hold time		0	-	0.9	μ s
t_R	SCL and SDA rise time	Note 2	$20+0.1C_b$	-	300	ns
t_F	SCL and SDA fall time	Note 2	$20+0.1C_b$	-	300	ns
t_F	SDA fall time for read out		$20+0.1C_b$	-	1000	ns
C_b	Capacitive load represented by each bus line		-	-	400	pF
$t_{SU:STA}$	Setup time for a repeated START condition		0.6	-	-	μ s
$t_{HD:STA}$	START condition hold time		0.6	-	-	μ s
$t_{SU:STOP}$	Setup time for STOP condition		0.6	-	-	μ s
t_{SW}	Tolerable spike width on bus	Note 1	-	-	50	ns
t_{BUFS}	BUS free time between a STOP and START condition		1.3	-	-	μ s

Note1: The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of width $< t_{SW(max)}$.

Note2: The rise and fall times specified here refer to the driver device and are part of the general fast I²C-bus specification. C_b = capacitive load per bus line.

Note3: All timing values are valid within the operating supply voltage and ambient temperature ranges and are referenced to V_{IL} and V_{IH} with an input voltage swing of VSS to VDDIO.

7.3.8. Reset timing characteristics

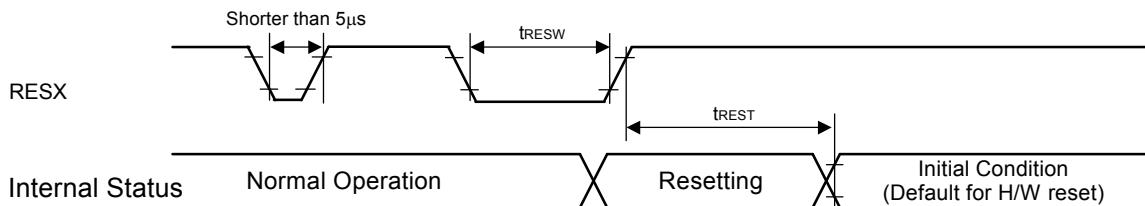


Table 7.3.8.1 Reset input timing

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

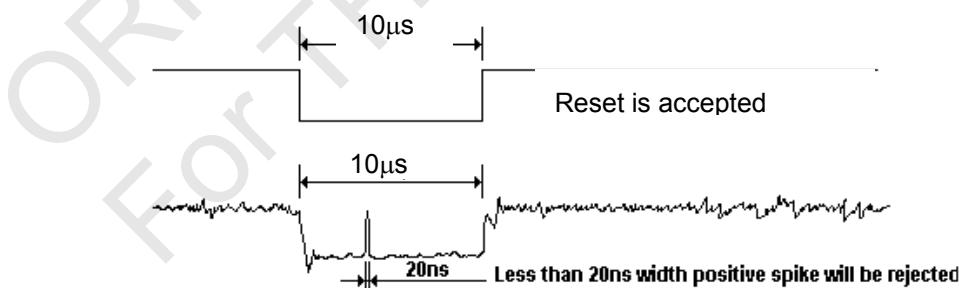
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, ID1/ID2/ID3/ID4 and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

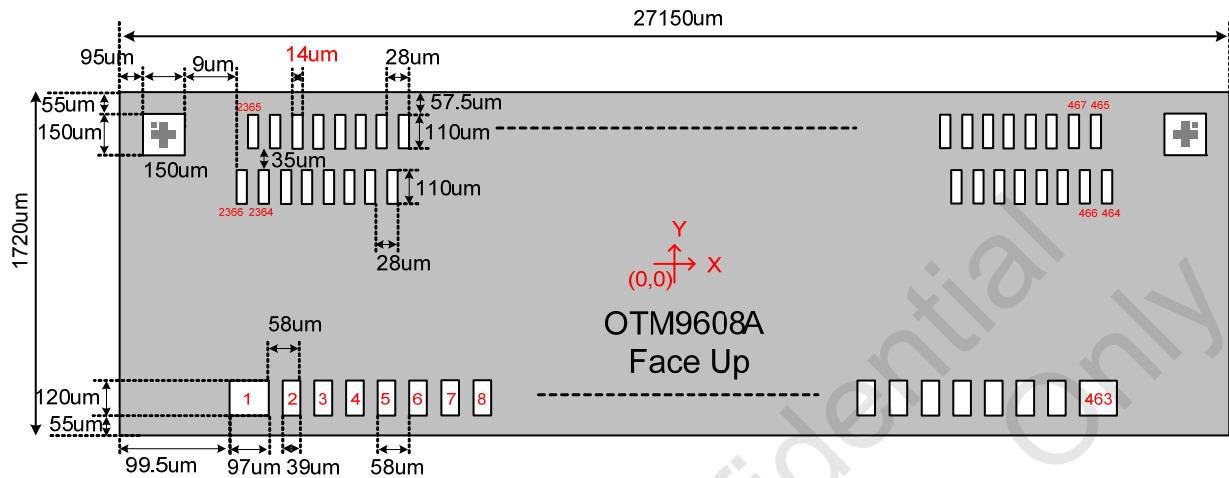
Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. CHIP INFORMATION

8.1. PAD Assignment



Chip size included scribe line.

8.2. PAD Dimension

Item	PAD No.	Size		Unit
		X	Y	
Chip Size	-	27150	1720	um
Chip thickness	-	250 ± 10		
Pad pitch	1 ~ 463	58	--	um
	464 ~ 2366	28	--	
Pad size	2 ~ 462	39	120	um
	464 ~ 2366	14	110	
	1, 463	97	120	

Note1: Chip size included scribe line.

8.3. Pad Location

NO.	PAD NAME	X-axis	Y-axis
1	VSSIDUM0	-13427.00	-745.00
2	PADA1	-13340.00	-745.00
3	PADA2	-13282.00	-745.00
4	PADA5	-13224.00	-745.00
5	PADA6	-13166.00	-745.00
6	PADA7	-13108.00	-745.00
7	VCOM	-13050.00	-745.00
8	VCOM	-12992.00	-745.00
9	VCOM	-12934.00	-745.00
10	VCOM	-12876.00	-745.00
11	3D_CLK_0	-12818.00	-745.00
12	3D_CLK_0	-12760.00	-745.00
13	3D_CLK_0	-12702.00	-745.00
14	3D_CLK_0	-12644.00	-745.00
15	3D_CLK_0	-12586.00	-745.00
16	3D_CLK_1	-12528.00	-745.00
17	3D_CLK_1	-12470.00	-745.00
18	3D_CLK_1	-12412.00	-745.00
19	3D_CLK_1	-12354.00	-745.00
20	3D_CLK_1	-12296.00	-745.00
21	3D_CLK_2	-12238.00	-745.00
22	3D_CLK_2	-12180.00	-745.00
23	3D_CLK_2	-12122.00	-745.00
24	3D_CLK_2	-12064.00	-745.00
25	3D_CLK_2	-12006.00	-745.00
26	3D_CLK_3	-11948.00	-745.00
27	3D_CLK_3	-11890.00	-745.00
28	3D_CLK_3	-11832.00	-745.00
29	3D_CLK_3	-11774.00	-745.00
30	3D_CLK_3	-11716.00	-745.00
31	BVP3D	-11658.00	-745.00
32	BVP3D	-11600.00	-745.00
33	BVN3D	-11542.00	-745.00
34	BVN3D	-11484.00	-745.00
35	MTP_PWR	-11426.00	-745.00
36	MTP_PWR	-11368.00	-745.00
37	VGL	-11310.00	-745.00
38	VGL	-11252.00	-745.00
39	VGL	-11194.00	-745.00
40	VGL_REG	-11136.00	-745.00
41	VGL_REG	-11078.00	-745.00
42	VGL_REG	-11020.00	-745.00
43	VRGH	-10962.00	-745.00
44	VRGH	-10904.00	-745.00
45	VCL	-10846.00	-745.00
46	VCL	-10788.00	-745.00
47	VCL	-10730.00	-745.00
48	VCL	-10672.00	-745.00
49	VCL	-10614.00	-745.00
50	VCL	-10556.00	-745.00
51	VREF	-10498.00	-745.00
52	VREF	-10440.00	-745.00
53	VSSA	-10382.00	-745.00
54	VSSA	-10324.00	-745.00
55	VSSA	-10266.00	-745.00

NO.	PAD NAME	X-axis	Y-axis
56	VSSA	-10208.00	-745.00
57	VDD	-10150.00	-745.00
58	VDD	-10092.00	-745.00
59	VDD	-10034.00	-745.00
60	VDD	-9976.00	-745.00
61	VDD	-9918.00	-745.00
62	VDD	-9860.00	-745.00
63	VSS	-9802.00	-745.00
64	VSS	-9744.00	-745.00
65	VDD	-9686.00	-745.00
66	DIOPWR	-9628.00	-745.00
67	DIOPWR	-9570.00	-745.00
68	VGSN	-9512.00	-745.00
69	VGSP	-9454.00	-745.00
70	VGMN	-9396.00	-745.00
71	VGMP	-9338.00	-745.00
72	VSS	-9280.00	-745.00
73	VSS	-9222.00	-745.00
74	VSS	-9164.00	-745.00
75	VSS	-9106.00	-745.00
76	VDD_18V	-9048.00	-745.00
77	VDD_18V	-8990.00	-745.00
78	VDD_18V	-8932.00	-745.00
79	VDD_18V	-8874.00	-745.00
80	VSSA	-8816.00	-745.00
81	VSSA	-8758.00	-745.00
82	VSSA	-8700.00	-745.00
83	VSSA	-8642.00	-745.00
84	VDDIO	-8584.00	-745.00
85	LANSEL	-8526.00	-745.00
86	DSWAP0	-8468.00	-745.00
87	DSWAP1	-8410.00	-745.00
88	PSWAP	-8352.00	-745.00
89	DSTB_SEL	-8294.00	-745.00
90	RGBBP	-8236.00	-745.00
91	I2C_SA0	-8178.00	-745.00
92	IM3	-8120.00	-745.00
93	IM2	-8062.00	-745.00
94	IM1	-8004.00	-745.00
95	IM0	-7946.00	-745.00
96	GPO3	-7888.00	-745.00
97	GPO2	-7830.00	-745.00
98	GPO1	-7772.00	-745.00
99	GPO0	-7714.00	-745.00
100	EXB1T	-7656.00	-745.00
101	TE_L	-7598.00	-745.00
102	VSEL	-7540.00	-745.00
103	SDO	-7482.00	-745.00
104	SDI	-7424.00	-745.00
105	DCX	-7366.00	-745.00
106	WRX	-7308.00	-745.00
107	RDX	-7250.00	-745.00
108	CSX	-7192.00	-745.00
109	RESX	-7134.00	-745.00
110	VSS	-7076.00	-745.00

NO.	PAD NAME	X-axis	Y-axis
111	VSS	-7018.00	-745.00
112	VSS	-6960.00	-745.00
113	VDDIO	-6902.00	-745.00
114	VDDIO	-6844.00	-745.00
115	VDDIO	-6786.00	-745.00
116	TEST0	-6728.00	-745.00
117	TEST1	-6670.00	-745.00
118	TEST2	-6612.00	-745.00
119	TEST3	-6554.00	-745.00
120	VSS	-6496.00	-745.00
121	NBWSEL	-6438.00	-745.00
122	VGSW3	-6380.00	-745.00
123	VGSW2	-6322.00	-745.00
124	VGSW1	-6264.00	-745.00
125	VGSW0	-6206.00	-745.00
126	VDDIO	-6148.00	-745.00
127	D23	-6090.00	-745.00
128	D22	-6032.00	-745.00
129	D21	-5974.00	-745.00
130	D20	-5916.00	-745.00
131	D19	-5858.00	-745.00
132	D18	-5800.00	-745.00
133	D17	-5742.00	-745.00
134	D16	-5684.00	-745.00
135	D15	-5626.00	-745.00
136	D14	-5568.00	-745.00
137	D13	-5510.00	-745.00
138	D12	-5452.00	-745.00
139	D11	-5394.00	-745.00
140	D10	-5336.00	-745.00
141	D9	-5278.00	-745.00
142	D8	-5220.00	-745.00
143	D7	-5162.00	-745.00
144	D6	-5104.00	-745.00
145	D5	-5046.00	-745.00
146	D4	-4988.00	-745.00
147	D3	-4930.00	-745.00
148	D2	-4872.00	-745.00
149	D1	-4814.00	-745.00
150	D0	-4756.00	-745.00
151	DE	-4698.00	-745.00
152	PCLK	-4640.00	-745.00
153	HS	-4582.00	-745.00
154	VS	-4524.00	-745.00
155	LEDPWM	-4466.00	-745.00
156	LEDON	-4408.00	-745.00
157	ERR	-4350.00	-745.00
158	VDDIO	-4292.00	-745.00
159	VDDIO	-4234.00	-745.00
160	VDDIO	-4176.00	-745.00
161	VSS	-4118.00	-745.00
162	VSS	-4060.00	-745.00
163	VSS	-4002.00	-745.00
164	VCC	-3944.00	-745.00
165	VCC	-3886.00	-745.00

NO.	PAD NAME	X-axis	Y-axis
166	VCC	-3828.00	-745.00
167	VCC	-3770.00	-745.00
168	VCC	-3712.00	-745.00
169	VCC	-3654.00	-745.00
170	VDDA	-3596.00	-745.00
171	VDDA	-3538.00	-745.00
172	VDDA	-3480.00	-745.00
173	VDDA	-3422.00	-745.00
174	NVDDA	-3364.00	-745.00
175	NVDDA	-3306.00	-745.00
176	NVDDA	-3248.00	-745.00
177	NVDDA	-3190.00	-745.00
178	VSS	-3132.00	-745.00
179	VSS	-3074.00	-745.00
180	VSS	-3016.00	-745.00
181	VSS	-2958.00	-745.00
182	VDD_18V	-2900.00	-745.00
183	VDD_18V	-2842.00	-745.00
184	VDD_18V	-2784.00	-745.00
185	VDD_18V	-2726.00	-745.00
186	LVDSVDD	-2668.00	-745.00
187	LVDSVDD	-2610.00	-745.00
188	LVDSVDD	-2552.00	-745.00
189	VDDAM	-2494.00	-745.00
190	VDDAM	-2436.00	-745.00
191	VDDAM	-2378.00	-745.00
192	VDDP	-2320.00	-745.00
193	VDDP	-2262.00	-745.00
194	VDDP	-2204.00	-745.00
195	LVDSVSS	-2146.00	-745.00
196	LVDSVSS	-2088.00	-745.00
197	LVDSVSS	-2030.00	-745.00
198	LVDSVSS	-1972.00	-745.00
199	LVDSVSS	-1914.00	-745.00
200	D22P	-1856.00	-745.00
201	D22P	-1798.00	-745.00
202	D22P	-1740.00	-745.00
203	D22P	-1682.00	-745.00
204	D22N	-1624.00	-745.00
205	D22N	-1566.00	-745.00
206	D22N	-1508.00	-745.00
207	D22N	-1450.00	-745.00
208	LVDSVSS	-1392.00	-745.00
209	LVDSVSS	-1334.00	-745.00
210	D1P	-1276.00	-745.00
211	D1P	-1218.00	-745.00
212	D1P	-1160.00	-745.00
213	D1P	-1102.00	-745.00
214	D1N	-1044.00	-745.00
215	D1N	-986.00	-745.00
216	D1N	-928.00	-745.00
217	D1N	-870.00	-745.00
218	LVDSVSS	-812.00	-745.00
219	LVDSVSS	-754.00	-745.00
220	CLKP	-696.00	-745.00
221	CLKP	-638.00	-745.00
222	CLKP	-580.00	-745.00

NO.	PAD NAME	X-axis	Y-axis
223	CLKP	-522.00	-745.00
224	CLKN	-464.00	-745.00
225	CLKN	-406.00	-745.00
226	CLKN	-348.00	-745.00
227	CLKN	-290.00	-745.00
228	LVDSVSS	-232.00	-745.00
229	LVDSVSS	-174.00	-745.00
230	D0P	-116.00	-745.00
231	D0P	-58.00	-745.00
232	D0P	0.00	-745.00
233	D0P	58.00	-745.00
234	D0N	116.00	-745.00
235	D0N	174.00	-745.00
236	D0N	232.00	-745.00
237	D0N	290.00	-745.00
238	LVDSVSS	348.00	-745.00
239	LVDSVSS	406.00	-745.00
240	D2P	464.00	-745.00
241	D2P	522.00	-745.00
242	D2P	580.00	-745.00
243	D2P	638.00	-745.00
244	D2N	696.00	-745.00
245	D2N	754.00	-745.00
246	D2N	812.00	-745.00
247	D2N	870.00	-745.00
248	LVDSVSS	928.00	-745.00
249	LVDSVSS	986.00	-745.00
250	TEST4	1044.00	-745.00
251	TEST5	1102.00	-745.00
252	VDD	1160.00	-745.00
253	VDD	1218.00	-745.00
254	VDD	1276.00	-745.00
255	OSC_TEST	1334.00	-745.00
256	TE_R	1392.00	-745.00
257	VSS	1450.00	-745.00
258	VSS	1508.00	-745.00
259	VSS	1566.00	-745.00
260	VREFCP	1624.00	-745.00
261	VREFCP	1682.00	-745.00
262	VRGH	1740.00	-745.00
263	VRGH	1798.00	-745.00
264	EXTP	1856.00	-745.00
265	EXTP	1914.00	-745.00
266	CSP	1972.00	-745.00
267	CSP	2030.00	-745.00
268	EXTN	2088.00	-745.00
269	EXTN	2146.00	-745.00
270	CSN	2204.00	-745.00
271	CSN	2262.00	-745.00
272	VSSA	2320.00	-745.00
273	VSSA	2378.00	-745.00
274	VSSA	2436.00	-745.00
275	VSSA	2494.00	-745.00
276	VSSA	2552.00	-745.00
277	VSSA	2610.00	-745.00
278	C11P	2668.00	-745.00
279	C11P	2726.00	-745.00

NO.	PAD NAME	X-axis	Y-axis
280	C11P	2784.00	-745.00
281	C11P	2842.00	-745.00
282	C11P	2900.00	-745.00
283	C11P	2958.00	-745.00
284	C11N	3016.00	-745.00
285	C11N	3074.00	-745.00
286	C11N	3132.00	-745.00
287	C11N	3190.00	-745.00
288	C11N	3248.00	-745.00
289	C11N	3306.00	-745.00
290	C12P	3364.00	-745.00
291	C12P	3422.00	-745.00
292	C12P	3480.00	-745.00
293	C12P	3538.00	-745.00
294	C12P	3596.00	-745.00
295	C12P	3654.00	-745.00
296	C12N	3712.00	-745.00
297	C12N	3770.00	-745.00
298	C12N	3828.00	-745.00
299	C12N	3886.00	-745.00
300	C12N	3944.00	-745.00
301	C12N	4002.00	-745.00
302	C13N	4060.00	-745.00
303	C13N	4118.00	-745.00
304	C13N	4176.00	-745.00
305	C13N	4234.00	-745.00
306	C13N	4292.00	-745.00
307	C13P	4350.00	-745.00
308	C13P	4408.00	-745.00
309	C13P	4466.00	-745.00
310	C13P	4524.00	-745.00
311	C13P	4582.00	-745.00
312	VDDA	4640.00	-745.00
313	VDDA	4698.00	-745.00
314	VDDA	4756.00	-745.00
315	VDDA	4814.00	-745.00
316	VDDA	4872.00	-745.00
317	VDD	4930.00	-745.00
318	VDD	4988.00	-745.00
319	VDD	5046.00	-745.00
320	VDD	5104.00	-745.00
321	VDD	5162.00	-745.00
322	VDD	5220.00	-745.00
323	VDD	5278.00	-745.00
324	VDD	5336.00	-745.00
325	VDD	5394.00	-745.00
326	VDD	5452.00	-745.00
327	VSS	5510.00	-745.00
328	VSS	5568.00	-745.00
329	VSS	5626.00	-745.00
330	VSS	5684.00	-745.00
331	VSS	5742.00	-745.00
332	VSS	5800.00	-745.00
333	VSS	5858.00	-745.00
334	VSS	5916.00	-745.00
335	VSS	5974.00	-745.00
336	VSS	6032.00	-745.00

NO.	PAD NAME	X-axis	Y-axis
337	C31P	6090.00	-745.00
338	C31P	6148.00	-745.00
339	C31P	6206.00	-745.00
340	C31P	6264.00	-745.00
341	C31P	6322.00	-745.00
342	C31P	6380.00	-745.00
343	C31N	6438.00	-745.00
344	C31N	6496.00	-745.00
345	C31N	6554.00	-745.00
346	C31N	6612.00	-745.00
347	C31N	6670.00	-745.00
348	C31N	6728.00	-745.00
349	C32P	6786.00	-745.00
350	C32P	6844.00	-745.00
351	C32P	6902.00	-745.00
352	C32P	6960.00	-745.00
353	C32P	7018.00	-745.00
354	C32P	7076.00	-745.00
355	C32N	7134.00	-745.00
356	C32N	7192.00	-745.00
357	C32N	7250.00	-745.00
358	C32N	7308.00	-745.00
359	C32N	7366.00	-745.00
360	C32N	7424.00	-745.00
361	VCL	7482.00	-745.00
362	VCL	7540.00	-745.00
363	VCL	7598.00	-745.00
364	VCL	7656.00	-745.00
365	VCL	7714.00	-745.00
366	C21P	7772.00	-745.00
367	C21P	7830.00	-745.00
368	C21P	7888.00	-745.00
369	C21P	7946.00	-745.00
370	C21P	8004.00	-745.00
371	C21N	8062.00	-745.00
372	C21N	8120.00	-745.00
373	C21N	8178.00	-745.00
374	C21N	8236.00	-745.00
375	C21N	8294.00	-745.00
376	C22P	8352.00	-745.00
377	C22P	8410.00	-745.00
378	C22P	8468.00	-745.00
379	C22P	8526.00	-745.00
380	C22P	8584.00	-745.00
381	C22N	8642.00	-745.00
382	C22N	8700.00	-745.00
383	C22N	8758.00	-745.00
384	C22N	8816.00	-745.00
385	C22N	8874.00	-745.00
386	C23N	8932.00	-745.00
387	C23N	8990.00	-745.00
388	C23N	9048.00	-745.00
389	C23N	9106.00	-745.00
390	C23N	9164.00	-745.00
391	C23P	9222.00	-745.00
392	C23P	9280.00	-745.00
393	C23P	9338.00	-745.00

NO.	PAD NAME	X-axis	Y-axis
394	C23P	9396.00	-745.00
395	C23P	9454.00	-745.00
396	NVDDA	9512.00	-745.00
397	NVDDA	9570.00	-745.00
398	NVDDA	9628.00	-745.00
399	NVDDA	9686.00	-745.00
400	NVDDA	9744.00	-745.00
401	VDD	9802.00	-745.00
402	VDD	9860.00	-745.00
403	VDD	9918.00	-745.00
404	VDD	9976.00	-745.00
405	VDD	10034.00	-745.00
406	VDD	10092.00	-745.00
407	VSS	10150.00	-745.00
408	VSS	10208.00	-745.00
409	VSS	10266.00	-745.00
410	VSS	10324.00	-745.00
411	VSS	10382.00	-745.00
412	VSS	10440.00	-745.00
413	TEST6	10498.00	-745.00
414	TEST7	10556.00	-745.00
415	C41P	10614.00	-745.00
416	C41P	10672.00	-745.00
417	C41P	10730.00	-745.00
418	C41N	10788.00	-745.00
419	C41N	10846.00	-745.00
420	C41N	10904.00	-745.00
421	C51N	10962.00	-745.00
422	C51N	11020.00	-745.00
423	C51N	11078.00	-745.00
424	C51P	11136.00	-745.00
425	C51P	11194.00	-745.00
426	C51P	11252.00	-745.00
427	VGH	11310.00	-745.00
428	VGH	11368.00	-745.00
429	VGH	11426.00	-745.00
430	VRGH	11484.00	-745.00
431	VRGH	11542.00	-745.00
432	VGL_REG	11600.00	-745.00
433	VGL_REG	11658.00	-745.00
434	VGL_REG	11716.00	-745.00
435	VGL	11774.00	-745.00
436	VGL	11832.00	-745.00
437	VGL	11890.00	-745.00
438	VSSA	11948.00	-745.00
439	VSSA	12006.00	-745.00
440	VSSA	12064.00	-745.00
441	VSSA	12122.00	-745.00
442	VDD	12180.00	-745.00
443	VDD	12238.00	-745.00
444	VDD	12296.00	-745.00
445	VDD	12354.00	-745.00
446	VDD_18V	12412.00	-745.00
447	VDD_18V	12470.00	-745.00
448	VDD_18V	12528.00	-745.00
449	VDD_18V	12586.00	-745.00
450	VSS	12644.00	-745.00

NO.	PAD NAME	X-axis	Y-axis
451	VSS	12702.00	-745.00
452	VSS	12760.00	-745.00
453	VSS	12818.00	-745.00
454	VCOM	12876.00	-745.00
455	VCOM	12934.00	-745.00
456	VCOM	12992.00	-745.00
457	VCOM	13050.00	-745.00
458	PADB7	13108.00	-745.00
459	PADB6	13166.00	-745.00
460	PADB5	13224.00	-745.00
461	PADB2	13282.00	-745.00
462	PADB1	13340.00	-745.00
463	VSSIDUM1	13427.00	-745.00
464	AVSSDUM0	13314.00	602.50
465	AVSSDUM0	13300.00	747.50
466	AVSSDUM1	13286.00	602.50
467	PADB3	13272.00	747.50
468	PADB4	13258.00	602.50
469	VGHO	13244.00	747.50
470	VGHO	13230.00	602.50
471	VGHO	13216.00	747.50
472	VGHO	13202.00	602.50
473	GOUT1	13188.00	747.50
474	GOUT1	13174.00	602.50
475	GOUT2	13160.00	747.50
476	GOUT2	13146.00	602.50
477	GDUM1	13132.00	747.50
478	GDUM1	13118.00	602.50
479	LVGL	13104.00	747.50
480	LVGL	13090.00	602.50
481	LVGL	13076.00	747.50
482	LVGL	13062.00	602.50
483	VRGH	13048.00	747.50
484	VRGH	13034.00	602.50
485	VRGH	13020.00	747.50
486	VRGH	13006.00	602.50
487	VGLO	12992.00	747.50
488	VGLO	12978.00	602.50
489	VGLO	12964.00	747.50
490	VGLO	12950.00	602.50
491	GOUT3	12936.00	747.50
492	GOUT3	12922.00	602.50
493	GOUT4	12908.00	747.50
494	GOUT4	12894.00	602.50
495	GOUT5	12880.00	747.50
496	GOUT5	12866.00	602.50
497	GOUT6	12852.00	747.50
498	GOUT6	12838.00	602.50
499	GOUT7	12824.00	747.50
500	GOUT7	12810.00	602.50
501	GOUT8	12796.00	747.50
502	GOUT8	12782.00	602.50
503	GOUT9	12768.00	747.50
504	GOUT9	12754.00	602.50
505	GOUT10	12740.00	747.50
506	GOUT10	12726.00	602.50
507	GOUT11	12712.00	747.50

NO.	PAD NAME	X-axis	Y-axis
508	GOUT11	12698.00	602.50
509	GOUT12	12684.00	747.50
510	GOUT12	12670.00	602.50
511	GOUT13	12656.00	747.50
512	GOUT13	12642.00	602.50
513	GOUT14	12628.00	747.50
514	GOUT14	12614.00	602.50
515	GOUT15	12600.00	747.50
516	GOUT15	12586.00	602.50
517	GOUT16	12572.00	747.50
518	GOUT16	12558.00	602.50
519	GOUT17	12544.00	747.50
520	GOUT17	12530.00	602.50
521	GOUT18	12516.00	747.50
522	GOUT18	12502.00	602.50
523	GOUT19	12488.00	747.50
524	GOUT19	12474.00	602.50
525	GOUT20	12460.00	747.50
526	GOUT20	12446.00	602.50
527	GOUT21	12432.00	747.50
528	GOUT21	12418.00	602.50
529	GOUT22	12404.00	747.50
530	GOUT22	12390.00	602.50
531	GOUT23	12376.00	747.50
532	GOUT23	12362.00	602.50
533	GOUT24	12348.00	747.50
534	GOUT24	12334.00	602.50
535	GOUT25	12320.00	747.50
536	GOUT25	12306.00	602.50
537	GOUT26	12292.00	747.50
538	GOUT26	12278.00	602.50
539	GOUT27	12264.00	747.50
540	GOUT27	12250.00	602.50
541	GOUT28	12236.00	747.50
542	GOUT28	12222.00	602.50
543	GOUT29	12208.00	747.50
544	GOUT29	12194.00	602.50
545	GOUT30	12180.00	747.50
546	GOUT30	12166.00	602.50
547	GOUT31	12152.00	747.50
548	GOUT31	12138.00	602.50
549	GOUT32	12124.00	747.50
550	GOUT32	12110.00	602.50
551	GOUT33	12096.00	747.50
552	GOUT33	12082.00	602.50
553	GOUT34	12068.00	747.50
554	GOUT34	12054.00	602.50
555	LVGL	12040.00	747.50
556	LVGL	12026.00	602.50
557	LVGL	12012.00	747.50
558	LVGL	11998.00	602.50
559	VGLO	11984.00	747.50
560	VGLO	11970.00	602.50
561	VGLO	11956.00	747.50
562	VGLO	11942.00	602.50
563	GDUM2	11928.00	747.50
564	GDUM2	11914.00	602.50

NO.	PAD NAME	X-axis	Y-axis
565	GDUM3	11900.00	747.50
566	GDUM3	11886.00	602.50
567	VGHO	11872.00	747.50
568	VGHO	11858.00	602.50
569	VGHO	11844.00	747.50
570	VGHO	11830.00	602.50
571	GDUM4	11816.00	747.50
572	GDUM4	11802.00	602.50
573	VCOM	11788.00	747.50
574	VCOM	11774.00	602.50
575	VCOM	11760.00	747.50
576	VCOM	11746.00	602.50
577	VCOM	11732.00	747.50
578	VCOM	11718.00	602.50
579	GDUM5	11704.00	747.50
580	GDUM5	11690.00	602.50
581	GOUT35	11676.00	747.50
582	GOUT35	11662.00	602.50
583	GDUM6	11648.00	747.50
584	GDUM6	11634.00	602.50
585	VSSA	11620.00	747.50
586	VSSA	11606.00	602.50
587	SDUM0	11592.00	747.50
588	SDUM1	11578.00	602.50
589	S1	11564.00	747.50
590	S2	11550.00	602.50
591	S3	11536.00	747.50
592	S4	11522.00	602.50
593	S5	11508.00	747.50
594	S6	11494.00	602.50
595	S7	11480.00	747.50
596	S8	11466.00	602.50
597	S9	11452.00	747.50
598	S10	11438.00	602.50
599	S11	11424.00	747.50
600	S12	11410.00	602.50
601	S13	11396.00	747.50
602	S14	11382.00	602.50
603	S15	11368.00	747.50
604	S16	11354.00	602.50
605	S17	11340.00	747.50
606	S18	11326.00	602.50
607	S19	11312.00	747.50
608	S20	11298.00	602.50
609	S21	11284.00	747.50
610	S22	11270.00	602.50
611	S23	11256.00	747.50
612	S24	11242.00	602.50
613	S25	11228.00	747.50
614	S26	11214.00	602.50
615	S27	11200.00	747.50
616	S28	11186.00	602.50
617	S29	11172.00	747.50
618	S30	11158.00	602.50
619	S31	11144.00	747.50
620	S32	11130.00	602.50
621	S33	11116.00	747.50

NO.	PAD NAME	X-axis	Y-axis
622	S34	11102.00	602.50
623	S35	11088.00	747.50
624	S36	11074.00	602.50
625	S37	11060.00	747.50
626	S38	11046.00	602.50
627	S39	11032.00	747.50
628	S40	11018.00	602.50
629	S41	11004.00	747.50
630	S42	10990.00	602.50
631	S43	10976.00	747.50
632	S44	10962.00	602.50
633	S45	10948.00	747.50
634	S46	10934.00	602.50
635	S47	10920.00	747.50
636	S48	10906.00	602.50
637	S49	10892.00	747.50
638	S50	10878.00	602.50
639	S51	10864.00	747.50
640	S52	10850.00	602.50
641	S53	10836.00	747.50
642	S54	10822.00	602.50
643	S55	10808.00	747.50
644	S56	10794.00	602.50
645	S57	10780.00	747.50
646	S58	10766.00	602.50
647	S59	10752.00	747.50
648	S60	10738.00	602.50
649	S61	10724.00	747.50
650	S62	10710.00	602.50
651	S63	10696.00	747.50
652	S64	10682.00	602.50
653	S65	10668.00	747.50
654	S66	10654.00	602.50
655	S67	10640.00	747.50
656	S68	10626.00	602.50
657	S69	10612.00	747.50
658	S70	10598.00	602.50
659	S71	10584.00	747.50
660	S72	10570.00	602.50
661	S73	10556.00	747.50
662	S74	10542.00	602.50
663	S75	10528.00	747.50
664	S76	10514.00	602.50
665	S77	10500.00	747.50
666	S78	10486.00	602.50
667	S79	10472.00	747.50
668	S80	10458.00	602.50
669	S81	10444.00	747.50
670	S82	10430.00	602.50
671	S83	10416.00	747.50
672	S84	10402.00	602.50
673	S85	10388.00	747.50
674	S86	10374.00	602.50
675	S87	10360.00	747.50
676	S88	10346.00	602.50
677	S89	10332.00	747.50
678	S90	10318.00	602.50

NO.	PAD NAME	X-axis	Y-axis
679	S91	10304.00	747.50
680	S92	10290.00	602.50
681	S93	10276.00	747.50
682	S94	10262.00	602.50
683	S95	10248.00	747.50
684	S96	10234.00	602.50
685	S97	10220.00	747.50
686	S98	10206.00	602.50
687	S99	10192.00	747.50
688	S100	10178.00	602.50
689	S101	10164.00	747.50
690	S102	10150.00	602.50
691	S103	10136.00	747.50
692	S104	10122.00	602.50
693	S105	10108.00	747.50
694	S106	10094.00	602.50
695	S107	10080.00	747.50
696	S108	10066.00	602.50
697	S109	10052.00	747.50
698	S110	10038.00	602.50
699	S111	10024.00	747.50
700	S112	10010.00	602.50
701	S113	9996.00	747.50
702	S114	9982.00	602.50
703	S115	9968.00	747.50
704	S116	9954.00	602.50
705	S117	9940.00	747.50
706	S118	9926.00	602.50
707	S119	9912.00	747.50
708	S120	9898.00	602.50
709	S121	9884.00	747.50
710	S122	9870.00	602.50
711	S123	9856.00	747.50
712	S124	9842.00	602.50
713	S125	9828.00	747.50
714	S126	9814.00	602.50
715	S127	9800.00	747.50
716	S128	9786.00	602.50
717	S129	9772.00	747.50
718	S130	9758.00	602.50
719	S131	9744.00	747.50
720	S132	9730.00	602.50
721	S133	9716.00	747.50
722	S134	9702.00	602.50
723	S135	9688.00	747.50
724	S136	9674.00	602.50
725	S137	9660.00	747.50
726	S138	9646.00	602.50
727	S139	9632.00	747.50
728	S140	9618.00	602.50
729	S141	9604.00	747.50
730	S142	9590.00	602.50
731	S143	9576.00	747.50
732	S144	9562.00	602.50
733	S145	9548.00	747.50
734	S146	9534.00	602.50
735	S147	9520.00	747.50

NO.	PAD NAME	X-axis	Y-axis
736	S148	9506.00	602.50
737	S149	9492.00	747.50
738	S150	9478.00	602.50
739	S151	9464.00	747.50
740	S152	9450.00	602.50
741	S153	9436.00	747.50
742	S154	9422.00	602.50
743	S155	9408.00	747.50
744	S156	9394.00	602.50
745	S157	9380.00	747.50
746	S158	9366.00	602.50
747	S159	9352.00	747.50
748	S160	9338.00	602.50
749	S161	9324.00	747.50
750	S162	9310.00	602.50
751	S163	9296.00	747.50
752	S164	9282.00	602.50
753	S165	9268.00	747.50
754	S166	9254.00	602.50
755	S167	9240.00	747.50
756	S168	9226.00	602.50
757	S169	9212.00	747.50
758	S170	9198.00	602.50
759	S171	9184.00	747.50
760	S172	9170.00	602.50
761	S173	9156.00	747.50
762	S174	9142.00	602.50
763	S175	9128.00	747.50
764	S176	9114.00	602.50
765	S177	9100.00	747.50
766	S178	9086.00	602.50
767	S179	9072.00	747.50
768	S180	9058.00	602.50
769	S181	9044.00	747.50
770	S182	9030.00	602.50
771	S183	9016.00	747.50
772	S184	9002.00	602.50
773	S185	8988.00	747.50
774	S186	8974.00	602.50
775	S187	8960.00	747.50
776	S188	8946.00	602.50
777	S189	8932.00	747.50
778	S190	8918.00	602.50
779	S191	8904.00	747.50
780	S192	8890.00	602.50
781	S193	8876.00	747.50
782	S194	8862.00	602.50
783	S195	8848.00	747.50
784	S196	8834.00	602.50
785	S197	8820.00	747.50
786	S198	8806.00	602.50
787	S199	8792.00	747.50
788	S200	8778.00	602.50
789	S201	8764.00	747.50
790	S202	8750.00	602.50
791	S203	8736.00	747.50
792	S204	8722.00	602.50

NO.	PAD NAME	X-axis	Y-axis
793	S205	8708.00	747.50
794	S206	8694.00	602.50
795	S207	8680.00	747.50
796	S208	8666.00	602.50
797	S209	8652.00	747.50
798	S210	8638.00	602.50
799	S211	8624.00	747.50
800	S212	8610.00	602.50
801	S213	8596.00	747.50
802	S214	8582.00	602.50
803	S215	8568.00	747.50
804	S216	8554.00	602.50
805	S217	8540.00	747.50
806	S218	8526.00	602.50
807	S219	8512.00	747.50
808	S220	8498.00	602.50
809	S221	8484.00	747.50
810	S222	8470.00	602.50
811	S223	8456.00	747.50
812	S224	8442.00	602.50
813	S225	8428.00	747.50
814	S226	8414.00	602.50
815	S227	8400.00	747.50
816	S228	8386.00	602.50
817	S229	8372.00	747.50
818	S230	8358.00	602.50
819	S231	8344.00	747.50
820	S232	8330.00	602.50
821	S233	8316.00	747.50
822	S234	8302.00	602.50
823	S235	8288.00	747.50
824	S236	8274.00	602.50
825	S237	8260.00	747.50
826	S238	8246.00	602.50
827	S239	8232.00	747.50
828	S240	8218.00	602.50
829	S241	8204.00	747.50
830	S242	8190.00	602.50
831	S243	8176.00	747.50
832	S244	8162.00	602.50
833	S245	8148.00	747.50
834	S246	8134.00	602.50
835	S247	8120.00	747.50
836	S248	8106.00	602.50
837	S249	8092.00	747.50
838	S250	8078.00	602.50
839	S251	8064.00	747.50
840	S252	8050.00	602.50
841	S253	8036.00	747.50
842	S254	8022.00	602.50
843	S255	8008.00	747.50
844	S256	7994.00	602.50
845	S257	7980.00	747.50
846	S258	7966.00	602.50
847	S259	7952.00	747.50
848	S260	7938.00	602.50
849	S261	7924.00	747.50

NO.	PAD NAME	X-axis	Y-axis
850	S262	7910.00	602.50
851	S263	7896.00	747.50
852	S264	7882.00	602.50
853	S265	7868.00	747.50
854	S266	7854.00	602.50
855	S267	7840.00	747.50
856	S268	7826.00	602.50
857	S269	7812.00	747.50
858	S270	7798.00	602.50
859	S271	7784.00	747.50
860	S272	7770.00	602.50
861	S273	7756.00	747.50
862	S274	7742.00	602.50
863	S275	7728.00	747.50
864	S276	7714.00	602.50
865	S277	7700.00	747.50
866	S278	7686.00	602.50
867	S279	7672.00	747.50
868	S280	7658.00	602.50
869	S281	7644.00	747.50
870	S282	7630.00	602.50
871	S283	7616.00	747.50
872	S284	7602.00	602.50
873	S285	7588.00	747.50
874	S286	7574.00	602.50
875	S287	7560.00	747.50
876	S288	7546.00	602.50
877	S289	7532.00	747.50
878	S290	7518.00	602.50
879	S291	7504.00	747.50
880	S292	7490.00	602.50
881	S293	7476.00	747.50
882	S294	7462.00	602.50
883	S295	7448.00	747.50
884	S296	7434.00	602.50
885	S297	7420.00	747.50
886	S298	7406.00	602.50
887	S299	7392.00	747.50
888	S300	7378.00	602.50
889	S301	7364.00	747.50
890	S302	7350.00	602.50
891	S303	7336.00	747.50
892	S304	7322.00	602.50
893	S305	7308.00	747.50
894	S306	7294.00	602.50
895	S307	7280.00	747.50
896	S308	7266.00	602.50
897	S309	7252.00	747.50
898	S310	7238.00	602.50
899	S311	7224.00	747.50
900	S312	7210.00	602.50
901	S313	7196.00	747.50
902	S314	7182.00	602.50
903	S315	7168.00	747.50
904	S316	7154.00	602.50
905	S317	7140.00	747.50
906	S318	7126.00	602.50

NO.	PAD NAME	X-axis	Y-axis
907	S319	7112.00	747.50
908	S320	7098.00	602.50
909	S321	7084.00	747.50
910	S322	7070.00	602.50
911	S323	7056.00	747.50
912	S324	7042.00	602.50
913	S325	7028.00	747.50
914	S326	7014.00	602.50
915	S327	7000.00	747.50
916	S328	6986.00	602.50
917	S329	6972.00	747.50
918	S330	6958.00	602.50
919	S331	6944.00	747.50
920	S332	6930.00	602.50
921	S333	6916.00	747.50
922	S334	6902.00	602.50
923	S335	6888.00	747.50
924	S336	6874.00	602.50
925	S337	6860.00	747.50
926	S338	6846.00	602.50
927	S339	6832.00	747.50
928	S340	6818.00	602.50
929	S341	6804.00	747.50
930	S342	6790.00	602.50
931	S343	6776.00	747.50
932	S344	6762.00	602.50
933	S345	6748.00	747.50
934	S346	6734.00	602.50
935	S347	6720.00	747.50
936	S348	6706.00	602.50
937	S349	6692.00	747.50
938	S350	6678.00	602.50
939	S351	6664.00	747.50
940	S352	6650.00	602.50
941	S353	6636.00	747.50
942	S354	6622.00	602.50
943	S355	6608.00	747.50
944	S356	6594.00	602.50
945	S357	6580.00	747.50
946	S358	6566.00	602.50
947	S359	6552.00	747.50
948	S360	6538.00	602.50
949	S361	6524.00	747.50
950	S362	6510.00	602.50
951	S363	6496.00	747.50
952	S364	6482.00	602.50
953	S365	6468.00	747.50
954	S366	6454.00	602.50
955	S367	6440.00	747.50
956	S368	6426.00	602.50
957	S369	6412.00	747.50
958	S370	6398.00	602.50
959	S371	6384.00	747.50
960	S372	6370.00	602.50
961	S373	6356.00	747.50
962	S374	6342.00	602.50
963	S375	6328.00	747.50

NO.	PAD NAME	X-axis	Y-axis
964	S376	6314.00	602.50
965	S377	6300.00	747.50
966	S378	6286.00	602.50
967	S379	6272.00	747.50
968	S380	6258.00	602.50
969	S381	6244.00	747.50
970	S382	6230.00	602.50
971	S383	6216.00	747.50
972	S384	6202.00	602.50
973	S385	6188.00	747.50
974	S386	6174.00	602.50
975	S387	6160.00	747.50
976	S388	6146.00	602.50
977	S389	6132.00	747.50
978	S390	6118.00	602.50
979	S391	6104.00	747.50
980	S392	6090.00	602.50
981	S393	6076.00	747.50
982	S394	6062.00	602.50
983	S395	6048.00	747.50
984	S396	6034.00	602.50
985	S397	6020.00	747.50
986	S398	6006.00	602.50
987	S399	5992.00	747.50
988	S400	5978.00	602.50
989	S401	5964.00	747.50
990	S402	5950.00	602.50
991	S403	5936.00	747.50
992	S404	5922.00	602.50
993	S405	5908.00	747.50
994	S406	5894.00	602.50
995	S407	5880.00	747.50
996	S408	5866.00	602.50
997	S409	5852.00	747.50
998	S410	5838.00	602.50
999	S411	5824.00	747.50
1000	S412	5810.00	602.50
1001	S413	5796.00	747.50
1002	S414	5782.00	602.50
1003	S415	5768.00	747.50
1004	S416	5754.00	602.50
1005	S417	5740.00	747.50
1006	S418	5726.00	602.50
1007	S419	5712.00	747.50
1008	S420	5698.00	602.50
1009	S421	5684.00	747.50
1010	S422	5670.00	602.50
1011	S423	5656.00	747.50
1012	S424	5642.00	602.50
1013	S425	5628.00	747.50
1014	S426	5614.00	602.50
1015	S427	5600.00	747.50
1016	S428	5586.00	602.50
1017	S429	5572.00	747.50
1018	S430	5558.00	602.50
1019	S431	5544.00	747.50
1020	S432	5530.00	602.50

NO.	PAD NAME	X-axis	Y-axis
1021	S433	5516.00	747.50
1022	S434	5502.00	602.50
1023	S435	5488.00	747.50
1024	S436	5474.00	602.50
1025	S437	5460.00	747.50
1026	S438	5446.00	602.50
1027	S439	5432.00	747.50
1028	S440	5418.00	602.50
1029	S441	5404.00	747.50
1030	S442	5390.00	602.50
1031	S443	5376.00	747.50
1032	S444	5362.00	602.50
1033	S445	5348.00	747.50
1034	S446	5334.00	602.50
1035	S447	5320.00	747.50
1036	S448	5306.00	602.50
1037	S449	5292.00	747.50
1038	S450	5278.00	602.50
1039	S451	5264.00	747.50
1040	S452	5250.00	602.50
1041	S453	5236.00	747.50
1042	S454	5222.00	602.50
1043	S455	5208.00	747.50
1044	S456	5194.00	602.50
1045	S457	5180.00	747.50
1046	S458	5166.00	602.50
1047	S459	5152.00	747.50
1048	S460	5138.00	602.50
1049	S461	5124.00	747.50
1050	S462	5110.00	602.50
1051	S463	5096.00	747.50
1052	S464	5082.00	602.50
1053	S465	5068.00	747.50
1054	S466	5054.00	602.50
1055	S467	5040.00	747.50
1056	S468	5026.00	602.50
1057	S469	5012.00	747.50
1058	S470	4998.00	602.50
1059	S471	4984.00	747.50
1060	S472	4970.00	602.50
1061	S473	4956.00	747.50
1062	S474	4942.00	602.50
1063	S475	4928.00	747.50
1064	S476	4914.00	602.50
1065	S477	4900.00	747.50
1066	S478	4886.00	602.50
1067	S479	4872.00	747.50
1068	S480	4858.00	602.50
1069	S481	4844.00	747.50
1070	S482	4830.00	602.50
1071	S483	4816.00	747.50
1072	S484	4802.00	602.50
1073	S485	4788.00	747.50
1074	S486	4774.00	602.50
1075	S487	4760.00	747.50
1076	S488	4746.00	602.50
1077	S489	4732.00	747.50

NO.	PAD NAME	X-axis	Y-axis
1078	S490	4718.00	602.50
1079	S491	4704.00	747.50
1080	S492	4690.00	602.50
1081	S493	4676.00	747.50
1082	S494	4662.00	602.50
1083	S495	4648.00	747.50
1084	S496	4634.00	602.50
1085	S497	4620.00	747.50
1086	S498	4606.00	602.50
1087	S499	4592.00	747.50
1088	S500	4578.00	602.50
1089	S501	4564.00	747.50
1090	S502	4550.00	602.50
1091	S503	4536.00	747.50
1092	S504	4522.00	602.50
1093	S505	4508.00	747.50
1094	S506	4494.00	602.50
1095	S507	4480.00	747.50
1096	S508	4466.00	602.50
1097	S509	4452.00	747.50
1098	S510	4438.00	602.50
1099	S511	4424.00	747.50
1100	S512	4410.00	602.50
1101	S513	4396.00	747.50
1102	S514	4382.00	602.50
1103	S515	4368.00	747.50
1104	S516	4354.00	602.50
1105	S517	4340.00	747.50
1106	S518	4326.00	602.50
1107	S519	4312.00	747.50
1108	S520	4298.00	602.50
1109	S521	4284.00	747.50
1110	S522	4270.00	602.50
1111	S523	4256.00	747.50
1112	S524	4242.00	602.50
1113	S525	4228.00	747.50
1114	S526	4214.00	602.50
1115	S527	4200.00	747.50
1116	S528	4186.00	602.50
1117	S529	4172.00	747.50
1118	S530	4158.00	602.50
1119	S531	4144.00	747.50
1120	S532	4130.00	602.50
1121	S533	4116.00	747.50
1122	S534	4102.00	602.50
1123	S535	4088.00	747.50
1124	S536	4074.00	602.50
1125	S537	4060.00	747.50
1126	S538	4046.00	602.50
1127	S539	4032.00	747.50
1128	S540	4018.00	602.50
1129	S541	4004.00	747.50
1130	S542	3990.00	602.50
1131	S543	3976.00	747.50
1132	S544	3962.00	602.50
1133	S545	3948.00	747.50
1134	S546	3934.00	602.50

NO.	PAD NAME	X-axis	Y-axis
1135	S547	3920.00	747.50
1136	S548	3906.00	602.50
1137	S549	3892.00	747.50
1138	S550	3878.00	602.50
1139	S551	3864.00	747.50
1140	S552	3850.00	602.50
1141	S553	3836.00	747.50
1142	S554	3822.00	602.50
1143	S555	3808.00	747.50
1144	S556	3794.00	602.50
1145	S557	3780.00	747.50
1146	S558	3766.00	602.50
1147	S559	3752.00	747.50
1148	S560	3738.00	602.50
1149	S561	3724.00	747.50
1150	S562	3710.00	602.50
1151	S563	3696.00	747.50
1152	S564	3682.00	602.50
1153	S565	3668.00	747.50
1154	S566	3654.00	602.50
1155	S567	3640.00	747.50
1156	S568	3626.00	602.50
1157	S569	3612.00	747.50
1158	S570	3598.00	602.50
1159	S571	3584.00	747.50
1160	S572	3570.00	602.50
1161	S573	3556.00	747.50
1162	S574	3542.00	602.50
1163	S575	3528.00	747.50
1164	S576	3514.00	602.50
1165	S577	3500.00	747.50
1166	S578	3486.00	602.50
1167	S579	3472.00	747.50
1168	S580	3458.00	602.50
1169	S581	3444.00	747.50
1170	S582	3430.00	602.50
1171	S583	3416.00	747.50
1172	S584	3402.00	602.50
1173	S585	3388.00	747.50
1174	S586	3374.00	602.50
1175	S587	3360.00	747.50
1176	S588	3346.00	602.50
1177	S589	3332.00	747.50
1178	S590	3318.00	602.50
1179	S591	3304.00	747.50
1180	S592	3290.00	602.50
1181	S593	3276.00	747.50
1182	S594	3262.00	602.50
1183	S595	3248.00	747.50
1184	S596	3234.00	602.50
1185	S597	3220.00	747.50
1186	S598	3206.00	602.50
1187	S599	3192.00	747.50
1188	S600	3178.00	602.50
1189	S601	3164.00	747.50
1190	S602	3150.00	602.50
1191	S603	3136.00	747.50

NO.	PAD NAME	X-axis	Y-axis
1192	S604	3122.00	602.50
1193	S605	3108.00	747.50
1194	S606	3094.00	602.50
1195	S607	3080.00	747.50
1196	S608	3066.00	602.50
1197	S609	3052.00	747.50
1198	S610	3038.00	602.50
1199	S611	3024.00	747.50
1200	S612	3010.00	602.50
1201	S613	2996.00	747.50
1202	S614	2982.00	602.50
1203	S615	2968.00	747.50
1204	S616	2954.00	602.50
1205	S617	2940.00	747.50
1206	S618	2926.00	602.50
1207	S619	2912.00	747.50
1208	S620	2898.00	602.50
1209	S621	2884.00	747.50
1210	S622	2870.00	602.50
1211	S623	2856.00	747.50
1212	S624	2842.00	602.50
1213	S625	2828.00	747.50
1214	S626	2814.00	602.50
1215	S627	2800.00	747.50
1216	S628	2786.00	602.50
1217	S629	2772.00	747.50
1218	S630	2758.00	602.50
1219	S631	2744.00	747.50
1220	S632	2730.00	602.50
1221	S633	2716.00	747.50
1222	S634	2702.00	602.50
1223	S635	2688.00	747.50
1224	S636	2674.00	602.50
1225	S637	2660.00	747.50
1226	S638	2646.00	602.50
1227	S639	2632.00	747.50
1228	S640	2618.00	602.50
1229	S641	2604.00	747.50
1230	S642	2590.00	602.50
1231	S643	2576.00	747.50
1232	S644	2562.00	602.50
1233	S645	2548.00	747.50
1234	S646	2534.00	602.50
1235	S647	2520.00	747.50
1236	S648	2506.00	602.50
1237	S649	2492.00	747.50
1238	S650	2478.00	602.50
1239	S651	2464.00	747.50
1240	S652	2450.00	602.50
1241	S653	2436.00	747.50
1242	S654	2422.00	602.50
1243	S655	2408.00	747.50
1244	S656	2394.00	602.50
1245	S657	2380.00	747.50
1246	S658	2366.00	602.50
1247	S659	2352.00	747.50
1248	S660	2338.00	602.50

NO.	PAD NAME	X-axis	Y-axis
1249	S661	2324.00	747.50
1250	S662	2310.00	602.50
1251	S663	2296.00	747.50
1252	S664	2282.00	602.50
1253	S665	2268.00	747.50
1254	S666	2254.00	602.50
1255	S667	2240.00	747.50
1256	S668	2226.00	602.50
1257	S669	2212.00	747.50
1258	S670	2198.00	602.50
1259	S671	2184.00	747.50
1260	S672	2170.00	602.50
1261	S673	2156.00	747.50
1262	S674	2142.00	602.50
1263	S675	2128.00	747.50
1264	S676	2114.00	602.50
1265	S677	2100.00	747.50
1266	S678	2086.00	602.50
1267	S679	2072.00	747.50
1268	S680	2058.00	602.50
1269	S681	2044.00	747.50
1270	S682	2030.00	602.50
1271	S683	2016.00	747.50
1272	S684	2002.00	602.50
1273	S685	1988.00	747.50
1274	S686	1974.00	602.50
1275	S687	1960.00	747.50
1276	S688	1946.00	602.50
1277	S689	1932.00	747.50
1278	S690	1918.00	602.50
1279	S691	1904.00	747.50
1280	S692	1890.00	602.50
1281	S693	1876.00	747.50
1282	S694	1862.00	602.50
1283	S695	1848.00	747.50
1284	S696	1834.00	602.50
1285	S697	1820.00	747.50
1286	S698	1806.00	602.50
1287	S699	1792.00	747.50
1288	S700	1778.00	602.50
1289	S701	1764.00	747.50
1290	S702	1750.00	602.50
1291	S703	1736.00	747.50
1292	S704	1722.00	602.50
1293	S705	1708.00	747.50
1294	S706	1694.00	602.50
1295	S707	1680.00	747.50
1296	S708	1666.00	602.50
1297	S709	1652.00	747.50
1298	S710	1638.00	602.50
1299	S711	1624.00	747.50
1300	S712	1610.00	602.50
1301	S713	1596.00	747.50
1302	S714	1582.00	602.50
1303	S715	1568.00	747.50
1304	S716	1554.00	602.50
1305	S717	1540.00	747.50

NO.	PAD NAME	X-axis	Y-axis
1306	S718	1526.00	602.50
1307	S719	1512.00	747.50
1308	S720	1498.00	602.50
1309	S721	1484.00	747.50
1310	S722	1470.00	602.50
1311	S723	1456.00	747.50
1312	S724	1442.00	602.50
1313	S725	1428.00	747.50
1314	S726	1414.00	602.50
1315	S727	1400.00	747.50
1316	S728	1386.00	602.50
1317	S729	1372.00	747.50
1318	S730	1358.00	602.50
1319	S731	1344.00	747.50
1320	S732	1330.00	602.50
1321	S733	1316.00	747.50
1322	S734	1302.00	602.50
1323	S735	1288.00	747.50
1324	S736	1274.00	602.50
1325	S737	1260.00	747.50
1326	S738	1246.00	602.50
1327	S739	1232.00	747.50
1328	S740	1218.00	602.50
1329	S741	1204.00	747.50
1330	S742	1190.00	602.50
1331	S743	1176.00	747.50
1332	S744	1162.00	602.50
1333	S745	1148.00	747.50
1334	S746	1134.00	602.50
1335	S747	1120.00	747.50
1336	S748	1106.00	602.50
1337	S749	1092.00	747.50
1338	S750	1078.00	602.50
1339	S751	1064.00	747.50
1340	S752	1050.00	602.50
1341	S753	1036.00	747.50
1342	S754	1022.00	602.50
1343	S755	1008.00	747.50
1344	S756	994.00	602.50
1345	S757	980.00	747.50
1346	S758	966.00	602.50
1347	S759	952.00	747.50
1348	S760	938.00	602.50
1349	S761	924.00	747.50
1350	S762	910.00	602.50
1351	S763	896.00	747.50
1352	S764	882.00	602.50
1353	S765	868.00	747.50
1354	S766	854.00	602.50
1355	S767	840.00	747.50
1356	S768	826.00	602.50
1357	S769	812.00	747.50
1358	S770	798.00	602.50
1359	S771	784.00	747.50
1360	S772	770.00	602.50
1361	S773	756.00	747.50
1362	S774	742.00	602.50

NO.	PAD NAME	X-axis	Y-axis
1363	S775	728.00	747.50
1364	S776	714.00	602.50
1365	S777	700.00	747.50
1366	S778	686.00	602.50
1367	S779	672.00	747.50
1368	S780	658.00	602.50
1369	S781	644.00	747.50
1370	S782	630.00	602.50
1371	S783	616.00	747.50
1372	S784	602.00	602.50
1373	S785	588.00	747.50
1374	S786	574.00	602.50
1375	S787	560.00	747.50
1376	S788	546.00	602.50
1377	S789	532.00	747.50
1378	S790	518.00	602.50
1379	S791	504.00	747.50
1380	S792	490.00	602.50
1381	S793	476.00	747.50
1382	S794	462.00	602.50
1383	S795	448.00	747.50
1384	S796	434.00	602.50
1385	S797	420.00	747.50
1386	S798	406.00	602.50
1387	S799	392.00	747.50
1388	S800	378.00	602.50
1389	S801	364.00	747.50
1390	S802	350.00	602.50
1391	S803	336.00	747.50
1392	S804	322.00	602.50
1393	S805	308.00	747.50
1394	S806	294.00	602.50
1395	S807	280.00	747.50
1396	S808	266.00	602.50
1397	S809	252.00	747.50
1398	S810	238.00	602.50
1399	AVSSDUM2	224.00	747.50
1400	AVSSDUM3	210.00	602.50
1401	AVSSDUM4	196.00	747.50
1402	AVSSDUM5	182.00	602.50
1403	AVSSDUM6	168.00	747.50
1404	AVSSDUM7	154.00	602.50
1405	AVSSDUM8	140.00	747.50
1406	AVSSDUM9	126.00	602.50
1407	AVSSDUM10	112.00	747.50
1408	AVSSDUM11	98.00	602.50
1409	AVSSDUM12	84.00	747.50
1410	AVSSDUM13	70.00	602.50
1411	AVSSDUM14	56.00	747.50
1412	AVSSDUM15	42.00	602.50
1413	AVSSDUM16	28.00	747.50
1414	AVSSDUM17	14.00	602.50
1415	AVSSDUM18	0.00	747.50
1416	AVSSDUM19	-14.00	602.50
1417	AVSSDUM20	-28.00	747.50
1418	AVSSDUM21	-42.00	602.50
1419	AVSSDUM22	-56.00	747.50

NO.	PAD NAME	X-axis	Y-axis
1420	AVSSDUM23	-70.00	602.50
1421	AVSSDUM24	-84.00	747.50
1422	AVSSDUM25	-98.00	602.50
1423	AVSSDUM26	-112.00	747.50
1424	AVSSDUM27	-126.00	602.50
1425	AVSSDUM28	-140.00	747.50
1426	AVSSDUM29	-154.00	602.50
1427	AVSSDUM30	-168.00	747.50
1428	AVSSDUM31	-182.00	602.50
1429	AVSSDUM32	-196.00	747.50
1430	AVSSDUM33	-210.00	602.50
1431	AVSSDUM34	-224.00	747.50
1432	S811	-238.00	602.50
1433	S812	-252.00	747.50
1434	S813	-266.00	602.50
1435	S814	-280.00	747.50
1436	S815	-294.00	602.50
1437	S816	-308.00	747.50
1438	S817	-322.00	602.50
1439	S818	-336.00	747.50
1440	S819	-350.00	602.50
1441	S820	-364.00	747.50
1442	S821	-378.00	602.50
1443	S822	-392.00	747.50
1444	S823	-406.00	602.50
1445	S824	-420.00	747.50
1446	S825	-434.00	602.50
1447	S826	-448.00	747.50
1448	S827	-462.00	602.50
1449	S828	-476.00	747.50
1450	S829	-490.00	602.50
1451	S830	-504.00	747.50
1452	S831	-518.00	602.50
1453	S832	-532.00	747.50
1454	S833	-546.00	602.50
1455	S834	-560.00	747.50
1456	S835	-574.00	602.50
1457	S836	-588.00	747.50
1458	S837	-602.00	602.50
1459	S838	-616.00	747.50
1460	S839	-630.00	602.50
1461	S840	-644.00	747.50
1462	S841	-658.00	602.50
1463	S842	-672.00	747.50
1464	S843	-686.00	602.50
1465	S844	-700.00	747.50
1466	S845	-714.00	602.50
1467	S846	-728.00	747.50
1468	S847	-742.00	602.50
1469	S848	-756.00	747.50
1470	S849	-770.00	602.50
1471	S850	-784.00	747.50
1472	S851	-798.00	602.50
1473	S852	-812.00	747.50
1474	S853	-826.00	602.50
1475	S854	-840.00	747.50
1476	S855	-854.00	602.50

NO.	PAD NAME	X-axis	Y-axis
1477	S856	-868.00	747.50
1478	S857	-882.00	602.50
1479	S858	-896.00	747.50
1480	S859	-910.00	602.50
1481	S860	-924.00	747.50
1482	S861	-938.00	602.50
1483	S862	-952.00	747.50
1484	S863	-966.00	602.50
1485	S864	-980.00	747.50
1486	S865	-994.00	602.50
1487	S866	-1008.00	747.50
1488	S867	-1022.00	602.50
1489	S868	-1036.00	747.50
1490	S869	-1050.00	602.50
1491	S870	-1064.00	747.50
1492	S871	-1078.00	602.50
1493	S872	-1092.00	747.50
1494	S873	-1106.00	602.50
1495	S874	-1120.00	747.50
1496	S875	-1134.00	602.50
1497	S876	-1148.00	747.50
1498	S877	-1162.00	602.50
1499	S878	-1176.00	747.50
1500	S879	-1190.00	602.50
1501	S880	-1204.00	747.50
1502	S881	-1218.00	602.50
1503	S882	-1232.00	747.50
1504	S883	-1246.00	602.50
1505	S884	-1260.00	747.50
1506	S885	-1274.00	602.50
1507	S886	-1288.00	747.50
1508	S887	-1302.00	602.50
1509	S888	-1316.00	747.50
1510	S889	-1330.00	602.50
1511	S890	-1344.00	747.50
1512	S891	-1358.00	602.50
1513	S892	-1372.00	747.50
1514	S893	-1386.00	602.50
1515	S894	-1400.00	747.50
1516	S895	-1414.00	602.50
1517	S896	-1428.00	747.50
1518	S897	-1442.00	602.50
1519	S898	-1456.00	747.50
1520	S899	-1470.00	602.50
1521	S900	-1484.00	747.50
1522	S901	-1498.00	602.50
1523	S902	-1512.00	747.50
1524	S903	-1526.00	602.50
1525	S904	-1540.00	747.50
1526	S905	-1554.00	602.50
1527	S906	-1568.00	747.50
1528	S907	-1582.00	602.50
1529	S908	-1596.00	747.50
1530	S909	-1610.00	602.50
1531	S910	-1624.00	747.50
1532	S911	-1638.00	602.50
1533	S912	-1652.00	747.50

NO.	PAD NAME	X-axis	Y-axis
1534	S913	-1666.00	602.50
1535	S914	-1680.00	747.50
1536	S915	-1694.00	602.50
1537	S916	-1708.00	747.50
1538	S917	-1722.00	602.50
1539	S918	-1736.00	747.50
1540	S919	-1750.00	602.50
1541	S920	-1764.00	747.50
1542	S921	-1778.00	602.50
1543	S922	-1792.00	747.50
1544	S923	-1806.00	602.50
1545	S924	-1820.00	747.50
1546	S925	-1834.00	602.50
1547	S926	-1848.00	747.50
1548	S927	-1862.00	602.50
1549	S928	-1876.00	747.50
1550	S929	-1890.00	602.50
1551	S930	-1904.00	747.50
1552	S931	-1918.00	602.50
1553	S932	-1932.00	747.50
1554	S933	-1946.00	602.50
1555	S934	-1960.00	747.50
1556	S935	-1974.00	602.50
1557	S936	-1988.00	747.50
1558	S937	-2002.00	602.50
1559	S938	-2016.00	747.50
1560	S939	-2030.00	602.50
1561	S940	-2044.00	747.50
1562	S941	-2058.00	602.50
1563	S942	-2072.00	747.50
1564	S943	-2086.00	602.50
1565	S944	-2100.00	747.50
1566	S945	-2114.00	602.50
1567	S946	-2128.00	747.50
1568	S947	-2142.00	602.50
1569	S948	-2156.00	747.50
1570	S949	-2170.00	602.50
1571	S950	-2184.00	747.50
1572	S951	-2198.00	602.50
1573	S952	-2212.00	747.50
1574	S953	-2226.00	602.50
1575	S954	-2240.00	747.50
1576	S955	-2254.00	602.50
1577	S956	-2268.00	747.50
1578	S957	-2282.00	602.50
1579	S958	-2296.00	747.50
1580	S959	-2310.00	602.50
1581	S960	-2324.00	747.50
1582	S961	-2338.00	602.50
1583	S962	-2352.00	747.50
1584	S963	-2366.00	602.50
1585	S964	-2380.00	747.50
1586	S965	-2394.00	602.50
1587	S966	-2408.00	747.50
1588	S967	-2422.00	602.50
1589	S968	-2436.00	747.50
1590	S969	-2450.00	602.50

NO.	PAD NAME	X-axis	Y-axis
1591	S970	-2464.00	747.50
1592	S971	-2478.00	602.50
1593	S972	-2492.00	747.50
1594	S973	-2506.00	602.50
1595	S974	-2520.00	747.50
1596	S975	-2534.00	602.50
1597	S976	-2548.00	747.50
1598	S977	-2562.00	602.50
1599	S978	-2576.00	747.50
1600	S979	-2590.00	602.50
1601	S980	-2604.00	747.50
1602	S981	-2618.00	602.50
1603	S982	-2632.00	747.50
1604	S983	-2646.00	602.50
1605	S984	-2660.00	747.50
1606	S985	-2674.00	602.50
1607	S986	-2688.00	747.50
1608	S987	-2702.00	602.50
1609	S988	-2716.00	747.50
1610	S989	-2730.00	602.50
1611	S990	-2744.00	747.50
1612	S991	-2758.00	602.50
1613	S992	-2772.00	747.50
1614	S993	-2786.00	602.50
1615	S994	-2800.00	747.50
1616	S995	-2814.00	602.50
1617	S996	-2828.00	747.50
1618	S997	-2842.00	602.50
1619	S998	-2856.00	747.50
1620	S999	-2870.00	602.50
1621	S1000	-2884.00	747.50
1622	S1001	-2898.00	602.50
1623	S1002	-2912.00	747.50
1624	S1003	-2926.00	602.50
1625	S1004	-2940.00	747.50
1626	S1005	-2954.00	602.50
1627	S1006	-2968.00	747.50
1628	S1007	-2982.00	602.50
1629	S1008	-2996.00	747.50
1630	S1009	-3010.00	602.50
1631	S1010	-3024.00	747.50
1632	S1011	-3038.00	602.50
1633	S1012	-3052.00	747.50
1634	S1013	-3066.00	602.50
1635	S1014	-3080.00	747.50
1636	S1015	-3094.00	602.50
1637	S1016	-3108.00	747.50
1638	S1017	-3122.00	602.50
1639	S1018	-3136.00	747.50
1640	S1019	-3150.00	602.50
1641	S1020	-3164.00	747.50
1642	S1021	-3178.00	602.50
1643	S1022	-3192.00	747.50
1644	S1023	-3206.00	602.50
1645	S1024	-3220.00	747.50
1646	S1025	-3234.00	602.50
1647	S1026	-3248.00	747.50

NO.	PAD NAME	X-axis	Y-axis
1648	S1027	-3262.00	602.50
1649	S1028	-3276.00	747.50
1650	S1029	-3290.00	602.50
1651	S1030	-3304.00	747.50
1652	S1031	-3318.00	602.50
1653	S1032	-3332.00	747.50
1654	S1033	-3346.00	602.50
1655	S1034	-3360.00	747.50
1656	S1035	-3374.00	602.50
1657	S1036	-3388.00	747.50
1658	S1037	-3402.00	602.50
1659	S1038	-3416.00	747.50
1660	S1039	-3430.00	602.50
1661	S1040	-3444.00	747.50
1662	S1041	-3458.00	602.50
1663	S1042	-3472.00	747.50
1664	S1043	-3486.00	602.50
1665	S1044	-3500.00	747.50
1666	S1045	-3514.00	602.50
1667	S1046	-3528.00	747.50
1668	S1047	-3542.00	602.50
1669	S1048	-3556.00	747.50
1670	S1049	-3570.00	602.50
1671	S1050	-3584.00	747.50
1672	S1051	-3598.00	602.50
1673	S1052	-3612.00	747.50
1674	S1053	-3626.00	602.50
1675	S1054	-3640.00	747.50
1676	S1055	-3654.00	602.50
1677	S1056	-3668.00	747.50
1678	S1057	-3682.00	602.50
1679	S1058	-3696.00	747.50
1680	S1059	-3710.00	602.50
1681	S1060	-3724.00	747.50
1682	S1061	-3738.00	602.50
1683	S1062	-3752.00	747.50
1684	S1063	-3766.00	602.50
1685	S1064	-3780.00	747.50
1686	S1065	-3794.00	602.50
1687	S1066	-3808.00	747.50
1688	S1067	-3822.00	602.50
1689	S1068	-3836.00	747.50
1690	S1069	-3850.00	602.50
1691	S1070	-3864.00	747.50
1692	S1071	-3878.00	602.50
1693	S1072	-3892.00	747.50
1694	S1073	-3906.00	602.50
1695	S1074	-3920.00	747.50
1696	S1075	-3934.00	602.50
1697	S1076	-3948.00	747.50
1698	S1077	-3962.00	602.50
1699	S1078	-3976.00	747.50
1700	S1079	-3990.00	602.50
1701	S1080	-4004.00	747.50
1702	S1081	-4018.00	602.50
1703	S1082	-4032.00	747.50
1704	S1083	-4046.00	602.50

NO.	PAD NAME	X-axis	Y-axis
1705	S1084	-4060.00	747.50
1706	S1085	-4074.00	602.50
1707	S1086	-4088.00	747.50
1708	S1087	-4102.00	602.50
1709	S1088	-4116.00	747.50
1710	S1089	-4130.00	602.50
1711	S1090	-4144.00	747.50
1712	S1091	-4158.00	602.50
1713	S1092	-4172.00	747.50
1714	S1093	-4186.00	602.50
1715	S1094	-4200.00	747.50
1716	S1095	-4214.00	602.50
1717	S1096	-4228.00	747.50
1718	S1097	-4242.00	602.50
1719	S1098	-4256.00	747.50
1720	S1099	-4270.00	602.50
1721	S1100	-4284.00	747.50
1722	S1101	-4298.00	602.50
1723	S1102	-4312.00	747.50
1724	S1103	-4326.00	602.50
1725	S1104	-4340.00	747.50
1726	S1105	-4354.00	602.50
1727	S1106	-4368.00	747.50
1728	S1107	-4382.00	602.50
1729	S1108	-4396.00	747.50
1730	S1109	-4410.00	602.50
1731	S1110	-4424.00	747.50
1732	S1111	-4438.00	602.50
1733	S1112	-4452.00	747.50
1734	S1113	-4466.00	602.50
1735	S1114	-4480.00	747.50
1736	S1115	-4494.00	602.50
1737	S1116	-4508.00	747.50
1738	S1117	-4522.00	602.50
1739	S1118	-4536.00	747.50
1740	S1119	-4550.00	602.50
1741	S1120	-4564.00	747.50
1742	S1121	-4578.00	602.50
1743	S1122	-4592.00	747.50
1744	S1123	-4606.00	602.50
1745	S1124	-4620.00	747.50
1746	S1125	-4634.00	602.50
1747	S1126	-4648.00	747.50
1748	S1127	-4662.00	602.50
1749	S1128	-4676.00	747.50
1750	S1129	-4690.00	602.50
1751	S1130	-4704.00	747.50
1752	S1131	-4718.00	602.50
1753	S1132	-4732.00	747.50
1754	S1133	-4746.00	602.50
1755	S1134	-4760.00	747.50
1756	S1135	-4774.00	602.50
1757	S1136	-4788.00	747.50
1758	S1137	-4802.00	602.50
1759	S1138	-4816.00	747.50
1760	S1139	-4830.00	602.50
1761	S1140	-4844.00	747.50

NO.	PAD NAME	X-axis	Y-axis
1762	S1141	-4858.00	602.50
1763	S1142	-4872.00	747.50
1764	S1143	-4886.00	602.50
1765	S1144	-4900.00	747.50
1766	S1145	-4914.00	602.50
1767	S1146	-4928.00	747.50
1768	S1147	-4942.00	602.50
1769	S1148	-4956.00	747.50
1770	S1149	-4970.00	602.50
1771	S1150	-4984.00	747.50
1772	S1151	-4998.00	602.50
1773	S1152	-5012.00	747.50
1774	S1153	-5026.00	602.50
1775	S1154	-5040.00	747.50
1776	S1155	-5054.00	602.50
1777	S1156	-5068.00	747.50
1778	S1157	-5082.00	602.50
1779	S1158	-5096.00	747.50
1780	S1159	-5110.00	602.50
1781	S1160	-5124.00	747.50
1782	S1161	-5138.00	602.50
1783	S1162	-5152.00	747.50
1784	S1163	-5166.00	602.50
1785	S1164	-5180.00	747.50
1786	S1165	-5194.00	602.50
1787	S1166	-5208.00	747.50
1788	S1167	-5222.00	602.50
1789	S1168	-5236.00	747.50
1790	S1169	-5250.00	602.50
1791	S1170	-5264.00	747.50
1792	S1171	-5278.00	602.50
1793	S1172	-5292.00	747.50
1794	S1173	-5306.00	602.50
1795	S1174	-5320.00	747.50
1796	S1175	-5334.00	602.50
1797	S1176	-5348.00	747.50
1798	S1177	-5362.00	602.50
1799	S1178	-5376.00	747.50
1800	S1179	-5390.00	602.50
1801	S1180	-5404.00	747.50
1802	S1181	-5418.00	602.50
1803	S1182	-5432.00	747.50
1804	S1183	-5446.00	602.50
1805	S1184	-5460.00	747.50
1806	S1185	-5474.00	602.50
1807	S1186	-5488.00	747.50
1808	S1187	-5502.00	602.50
1809	S1188	-5516.00	747.50
1810	S1189	-5530.00	602.50
1811	S1190	-5544.00	747.50
1812	S1191	-5558.00	602.50
1813	S1192	-5572.00	747.50
1814	S1193	-5586.00	602.50
1815	S1194	-5600.00	747.50
1816	S1195	-5614.00	602.50
1817	S1196	-5628.00	747.50
1818	S1197	-5642.00	602.50

NO.	PAD NAME	X-axis	Y-axis
1819	S1198	-5656.00	747.50
1820	S1199	-5670.00	602.50
1821	S1200	-5684.00	747.50
1822	S1201	-5698.00	602.50
1823	S1202	-5712.00	747.50
1824	S1203	-5726.00	602.50
1825	S1204	-5740.00	747.50
1826	S1205	-5754.00	602.50
1827	S1206	-5768.00	747.50
1828	S1207	-5782.00	602.50
1829	S1208	-5796.00	747.50
1830	S1209	-5810.00	602.50
1831	S1210	-5824.00	747.50
1832	S1211	-5838.00	602.50
1833	S1212	-5852.00	747.50
1834	S1213	-5866.00	602.50
1835	S1214	-5880.00	747.50
1836	S1215	-5894.00	602.50
1837	S1216	-5908.00	747.50
1838	S1217	-5922.00	602.50
1839	S1218	-5936.00	747.50
1840	S1219	-5950.00	602.50
1841	S1220	-5964.00	747.50
1842	S1221	-5978.00	602.50
1843	S1222	-5992.00	747.50
1844	S1223	-6006.00	602.50
1845	S1224	-6020.00	747.50
1846	S1225	-6034.00	602.50
1847	S1226	-6048.00	747.50
1848	S1227	-6062.00	602.50
1849	S1228	-6076.00	747.50
1850	S1229	-6090.00	602.50
1851	S1230	-6104.00	747.50
1852	S1231	-6118.00	602.50
1853	S1232	-6132.00	747.50
1854	S1233	-6146.00	602.50
1855	S1234	-6160.00	747.50
1856	S1235	-6174.00	602.50
1857	S1236	-6188.00	747.50
1858	S1237	-6202.00	602.50
1859	S1238	-6216.00	747.50
1860	S1239	-6230.00	602.50
1861	S1240	-6244.00	747.50
1862	S1241	-6258.00	602.50
1863	S1242	-6272.00	747.50
1864	S1243	-6286.00	602.50
1865	S1244	-6300.00	747.50
1866	S1245	-6314.00	602.50
1867	S1246	-6328.00	747.50
1868	S1247	-6342.00	602.50
1869	S1248	-6356.00	747.50
1870	S1249	-6370.00	602.50
1871	S1250	-6384.00	747.50
1872	S1251	-6398.00	602.50
1873	S1252	-6412.00	747.50
1874	S1253	-6426.00	602.50
1875	S1254	-6440.00	747.50

NO.	PAD NAME	X-axis	Y-axis
1876	S1255	-6454.00	602.50
1877	S1256	-6468.00	747.50
1878	S1257	-6482.00	602.50
1879	S1258	-6496.00	747.50
1880	S1259	-6510.00	602.50
1881	S1260	-6524.00	747.50
1882	S1261	-6538.00	602.50
1883	S1262	-6552.00	747.50
1884	S1263	-6566.00	602.50
1885	S1264	-6580.00	747.50
1886	S1265	-6594.00	602.50
1887	S1266	-6608.00	747.50
1888	S1267	-6622.00	602.50
1889	S1268	-6636.00	747.50
1890	S1269	-6650.00	602.50
1891	S1270	-6664.00	747.50
1892	S1271	-6678.00	602.50
1893	S1272	-6692.00	747.50
1894	S1273	-6706.00	602.50
1895	S1274	-6720.00	747.50
1896	S1275	-6734.00	602.50
1897	S1276	-6748.00	747.50
1898	S1277	-6762.00	602.50
1899	S1278	-6776.00	747.50
1900	S1279	-6790.00	602.50
1901	S1280	-6804.00	747.50
1902	S1281	-6818.00	602.50
1903	S1282	-6832.00	747.50
1904	S1283	-6846.00	602.50
1905	S1284	-6860.00	747.50
1906	S1285	-6874.00	602.50
1907	S1286	-6888.00	747.50
1908	S1287	-6902.00	602.50
1909	S1288	-6916.00	747.50
1910	S1289	-6930.00	602.50
1911	S1290	-6944.00	747.50
1912	S1291	-6958.00	602.50
1913	S1292	-6972.00	747.50
1914	S1293	-6986.00	602.50
1915	S1294	-7000.00	747.50
1916	S1295	-7014.00	602.50
1917	S1296	-7028.00	747.50
1918	S1297	-7042.00	602.50
1919	S1298	-7056.00	747.50
1920	S1299	-7070.00	602.50
1921	S1300	-7084.00	747.50
1922	S1301	-7098.00	602.50
1923	S1302	-7112.00	747.50
1924	S1303	-7126.00	602.50
1925	S1304	-7140.00	747.50
1926	S1305	-7154.00	602.50
1927	S1306	-7168.00	747.50
1928	S1307	-7182.00	602.50
1929	S1308	-7196.00	747.50
1930	S1309	-7210.00	602.50
1931	S1310	-7224.00	747.50
1932	S1311	-7238.00	602.50

NO.	PAD NAME	X-axis	Y-axis
1933	S1312	-7252.00	747.50
1934	S1313	-7266.00	602.50
1935	S1314	-7280.00	747.50
1936	S1315	-7294.00	602.50
1937	S1316	-7308.00	747.50
1938	S1317	-7322.00	602.50
1939	S1318	-7336.00	747.50
1940	S1319	-7350.00	602.50
1941	S1320	-7364.00	747.50
1942	S1321	-7378.00	602.50
1943	S1322	-7392.00	747.50
1944	S1323	-7406.00	602.50
1945	S1324	-7420.00	747.50
1946	S1325	-7434.00	602.50
1947	S1326	-7448.00	747.50
1948	S1327	-7462.00	602.50
1949	S1328	-7476.00	747.50
1950	S1329	-7490.00	602.50
1951	S1330	-7504.00	747.50
1952	S1331	-7518.00	602.50
1953	S1332	-7532.00	747.50
1954	S1333	-7546.00	602.50
1955	S1334	-7560.00	747.50
1956	S1335	-7574.00	602.50
1957	S1336	-7588.00	747.50
1958	S1337	-7602.00	602.50
1959	S1338	-7616.00	747.50
1960	S1339	-7630.00	602.50
1961	S1340	-7644.00	747.50
1962	S1341	-7658.00	602.50
1963	S1342	-7672.00	747.50
1964	S1343	-7686.00	602.50
1965	S1344	-7700.00	747.50
1966	S1345	-7714.00	602.50
1967	S1346	-7728.00	747.50
1968	S1347	-7742.00	602.50
1969	S1348	-7756.00	747.50
1970	S1349	-7770.00	602.50
1971	S1350	-7784.00	747.50
1972	S1351	-7798.00	602.50
1973	S1352	-7812.00	747.50
1974	S1353	-7826.00	602.50
1975	S1354	-7840.00	747.50
1976	S1355	-7854.00	602.50
1977	S1356	-7868.00	747.50
1978	S1357	-7882.00	602.50
1979	S1358	-7896.00	747.50
1980	S1359	-7910.00	602.50
1981	S1360	-7924.00	747.50
1982	S1361	-7938.00	602.50
1983	S1362	-7952.00	747.50
1984	S1363	-7966.00	602.50
1985	S1364	-7980.00	747.50
1986	S1365	-7994.00	602.50
1987	S1366	-8008.00	747.50
1988	S1367	-8022.00	602.50
1989	S1368	-8036.00	747.50

NO.	PAD NAME	X-axis	Y-axis
1990	S1369	-8050.00	602.50
1991	S1370	-8064.00	747.50
1992	S1371	-8078.00	602.50
1993	S1372	-8092.00	747.50
1994	S1373	-8106.00	602.50
1995	S1374	-8120.00	747.50
1996	S1375	-8134.00	602.50
1997	S1376	-8148.00	747.50
1998	S1377	-8162.00	602.50
1999	S1378	-8176.00	747.50
2000	S1379	-8190.00	602.50
2001	S1380	-8204.00	747.50
2002	S1381	-8218.00	602.50
2003	S1382	-8232.00	747.50
2004	S1383	-8246.00	602.50
2005	S1384	-8260.00	747.50
2006	S1385	-8274.00	602.50
2007	S1386	-8288.00	747.50
2008	S1387	-8302.00	602.50
2009	S1388	-8316.00	747.50
2010	S1389	-8330.00	602.50
2011	S1390	-8344.00	747.50
2012	S1391	-8358.00	602.50
2013	S1392	-8372.00	747.50
2014	S1393	-8386.00	602.50
2015	S1394	-8400.00	747.50
2016	S1395	-8414.00	602.50
2017	S1396	-8428.00	747.50
2018	S1397	-8442.00	602.50
2019	S1398	-8456.00	747.50
2020	S1399	-8470.00	602.50
2021	S1400	-8484.00	747.50
2022	S1401	-8498.00	602.50
2023	S1402	-8512.00	747.50
2024	S1403	-8526.00	602.50
2025	S1404	-8540.00	747.50
2026	S1405	-8554.00	602.50
2027	S1406	-8568.00	747.50
2028	S1407	-8582.00	602.50
2029	S1408	-8596.00	747.50
2030	S1409	-8610.00	602.50
2031	S1410	-8624.00	747.50
2032	S1411	-8638.00	602.50
2033	S1412	-8652.00	747.50
2034	S1413	-8666.00	602.50
2035	S1414	-8680.00	747.50
2036	S1415	-8694.00	602.50
2037	S1416	-8708.00	747.50
2038	S1417	-8722.00	602.50
2039	S1418	-8736.00	747.50
2040	S1419	-8750.00	602.50
2041	S1420	-8764.00	747.50
2042	S1421	-8778.00	602.50
2043	S1422	-8792.00	747.50
2044	S1423	-8806.00	602.50
2045	S1424	-8820.00	747.50
2046	S1425	-8834.00	602.50

NO.	PAD NAME	X-axis	Y-axis
2047	S1426	-8848.00	747.50
2048	S1427	-8862.00	602.50
2049	S1428	-8876.00	747.50
2050	S1429	-8890.00	602.50
2051	S1430	-8904.00	747.50
2052	S1431	-8918.00	602.50
2053	S1432	-8932.00	747.50
2054	S1433	-8946.00	602.50
2055	S1434	-8960.00	747.50
2056	S1435	-8974.00	602.50
2057	S1436	-8988.00	747.50
2058	S1437	-9002.00	602.50
2059	S1438	-9016.00	747.50
2060	S1439	-9030.00	602.50
2061	S1440	-9044.00	747.50
2062	S1441	-9058.00	602.50
2063	S1442	-9072.00	747.50
2064	S1443	-9086.00	602.50
2065	S1444	-9100.00	747.50
2066	S1445	-9114.00	602.50
2067	S1446	-9128.00	747.50
2068	S1447	-9142.00	602.50
2069	S1448	-9156.00	747.50
2070	S1449	-9170.00	602.50
2071	S1450	-9184.00	747.50
2072	S1451	-9198.00	602.50
2073	S1452	-9212.00	747.50
2074	S1453	-9226.00	602.50
2075	S1454	-9240.00	747.50
2076	S1455	-9254.00	602.50
2077	S1456	-9268.00	747.50
2078	S1457	-9282.00	602.50
2079	S1458	-9296.00	747.50
2080	S1459	-9310.00	602.50
2081	S1460	-9324.00	747.50
2082	S1461	-9338.00	602.50
2083	S1462	-9352.00	747.50
2084	S1463	-9366.00	602.50
2085	S1464	-9380.00	747.50
2086	S1465	-9394.00	602.50
2087	S1466	-9408.00	747.50
2088	S1467	-9422.00	602.50
2089	S1468	-9436.00	747.50
2090	S1469	-9450.00	602.50
2091	S1470	-9464.00	747.50
2092	S1471	-9478.00	602.50
2093	S1472	-9492.00	747.50
2094	S1473	-9506.00	602.50
2095	S1474	-9520.00	747.50
2096	S1475	-9534.00	602.50
2097	S1476	-9548.00	747.50
2098	S1477	-9562.00	602.50
2099	S1478	-9576.00	747.50
2100	S1479	-9590.00	602.50
2101	S1480	-9604.00	747.50
2102	S1481	-9618.00	602.50
2103	S1482	-9632.00	747.50

NO.	PAD NAME	X-axis	Y-axis
2104	S1483	-9646.00	602.50
2105	S1484	-9660.00	747.50
2106	S1485	-9674.00	602.50
2107	S1486	-9688.00	747.50
2108	S1487	-9702.00	602.50
2109	S1488	-9716.00	747.50
2110	S1489	-9730.00	602.50
2111	S1490	-9744.00	747.50
2112	S1491	-9758.00	602.50
2113	S1492	-9772.00	747.50
2114	S1493	-9786.00	602.50
2115	S1494	-9800.00	747.50
2116	S1495	-9814.00	602.50
2117	S1496	-9828.00	747.50
2118	S1497	-9842.00	602.50
2119	S1498	-9856.00	747.50
2120	S1499	-9870.00	602.50
2121	S1500	-9884.00	747.50
2122	S1501	-9898.00	602.50
2123	S1502	-9912.00	747.50
2124	S1503	-9926.00	602.50
2125	S1504	-9940.00	747.50
2126	S1505	-9954.00	602.50
2127	S1506	-9968.00	747.50
2128	S1507	-9982.00	602.50
2129	S1508	-9996.00	747.50
2130	S1509	-10010.00	602.50
2131	S1510	-10024.00	747.50
2132	S1511	-10038.00	602.50
2133	S1512	-10052.00	747.50
2134	S1513	-10066.00	602.50
2135	S1514	-10080.00	747.50
2136	S1515	-10094.00	602.50
2137	S1516	-10108.00	747.50
2138	S1517	-10122.00	602.50
2139	S1518	-10136.00	747.50
2140	S1519	-10150.00	602.50
2141	S1520	-10164.00	747.50
2142	S1521	-10178.00	602.50
2143	S1522	-10192.00	747.50
2144	S1523	-10206.00	602.50
2145	S1524	-10220.00	747.50
2146	S1525	-10234.00	602.50
2147	S1526	-10248.00	747.50
2148	S1527	-10262.00	602.50
2149	S1528	-10276.00	747.50
2150	S1529	-10290.00	602.50
2151	S1530	-10304.00	747.50
2152	S1531	-10318.00	602.50
2153	S1532	-10332.00	747.50
2154	S1533	-10346.00	602.50
2155	S1534	-10360.00	747.50
2156	S1535	-10374.00	602.50
2157	S1536	-10388.00	747.50
2158	S1537	-10402.00	602.50
2159	S1538	-10416.00	747.50
2160	S1539	-10430.00	602.50

NO.	PAD NAME	X-axis	Y-axis
2161	S1540	-10444.00	747.50
2162	S1541	-10458.00	602.50
2163	S1542	-10472.00	747.50
2164	S1543	-10486.00	602.50
2165	S1544	-10500.00	747.50
2166	S1545	-10514.00	602.50
2167	S1546	-10528.00	747.50
2168	S1547	-10542.00	602.50
2169	S1548	-10556.00	747.50
2170	S1549	-10570.00	602.50
2171	S1550	-10584.00	747.50
2172	S1551	-10598.00	602.50
2173	S1552	-10612.00	747.50
2174	S1553	-10626.00	602.50
2175	S1554	-10640.00	747.50
2176	S1555	-10654.00	602.50
2177	S1556	-10668.00	747.50
2178	S1557	-10682.00	602.50
2179	S1558	-10696.00	747.50
2180	S1559	-10710.00	602.50
2181	S1560	-10724.00	747.50
2182	S1561	-10738.00	602.50
2183	S1562	-10752.00	747.50
2184	S1563	-10766.00	602.50
2185	S1564	-10780.00	747.50
2186	S1565	-10794.00	602.50
2187	S1566	-10808.00	747.50
2188	S1567	-10822.00	602.50
2189	S1568	-10836.00	747.50
2190	S1569	-10850.00	602.50
2191	S1570	-10864.00	747.50
2192	S1571	-10878.00	602.50
2193	S1572	-10892.00	747.50
2194	S1573	-10906.00	602.50
2195	S1574	-10920.00	747.50
2196	S1575	-10934.00	602.50
2197	S1576	-10948.00	747.50
2198	S1577	-10962.00	602.50
2199	S1578	-10976.00	747.50
2200	S1579	-10990.00	602.50
2201	S1580	-11004.00	747.50
2202	S1581	-11018.00	602.50
2203	S1582	-11032.00	747.50
2204	S1583	-11046.00	602.50
2205	S1584	-11060.00	747.50
2206	S1585	-11074.00	602.50
2207	S1586	-11088.00	747.50
2208	S1587	-11102.00	602.50
2209	S1588	-11116.00	747.50
2210	S1589	-11130.00	602.50
2211	S1590	-11144.00	747.50
2212	S1591	-11158.00	602.50
2213	S1592	-11172.00	747.50
2214	S1593	-11186.00	602.50
2215	S1594	-11200.00	747.50
2216	S1595	-11214.00	602.50
2217	S1596	-11228.00	747.50

NO.	PAD NAME	X-axis	Y-axis
2218	S1597	-11242.00	602.50
2219	S1598	-11256.00	747.50
2220	S1599	-11270.00	602.50
2221	S1600	-11284.00	747.50
2222	S1601	-11298.00	602.50
2223	S1602	-11312.00	747.50
2224	S1603	-11326.00	602.50
2225	S1604	-11340.00	747.50
2226	S1605	-11354.00	602.50
2227	S1606	-11368.00	747.50
2228	S1607	-11382.00	602.50
2229	S1608	-11396.00	747.50
2230	S1609	-11410.00	602.50
2231	S1610	-11424.00	747.50
2232	S1611	-11438.00	602.50
2233	S1612	-11452.00	747.50
2234	S1613	-11466.00	602.50
2235	S1614	-11480.00	747.50
2236	S1615	-11494.00	602.50
2237	S1616	-11508.00	747.50
2238	S1617	-11522.00	602.50
2239	S1618	-11536.00	747.50
2240	S1619	-11550.00	602.50
2241	S1620	-11564.00	747.50
2242	SDUM2	-11578.00	602.50
2243	SDUM3	-11592.00	747.50
2244	VSSA	-11606.00	602.50
2245	VSSA	-11620.00	747.50
2246	GDUM7	-11634.00	602.50
2247	GDUM7	-11648.00	747.50
2248	GOUT36	-11662.00	602.50
2249	GOUT36	-11676.00	747.50
2250	GDUM8	-11690.00	602.50
2251	GDUM8	-11704.00	747.50
2252	VCOM	-11718.00	602.50
2253	VCOM	-11732.00	747.50
2254	VCOM	-11746.00	602.50
2255	VCOM	-11760.00	747.50
2256	VCOM	-11774.00	602.50
2257	VCOM	-11788.00	747.50
2258	GDUM9	-11802.00	602.50
2259	GDUM9	-11816.00	747.50
2260	VGHO	-11830.00	602.50
2261	VGHO	-11844.00	747.50
2262	VGHO	-11858.00	602.50
2263	VGHO	-11872.00	747.50
2264	GDUM10	-11886.00	602.50
2265	GDUM10	-11900.00	747.50
2266	GDUM11	-11914.00	602.50
2267	GDUM11	-11928.00	747.50
2268	VGLO	-11942.00	602.50
2269	VGLO	-11956.00	747.50
2270	VGLO	-11970.00	602.50
2271	VGLO	-11984.00	747.50
2272	LVGL	-11998.00	602.50
2273	LVGL	-12012.00	747.50

NO.	PAD NAME	X-axis	Y-axis
2274	LVGL	-12026.00	602.50
2275	LVGL	-12040.00	747.50
2276	GOUT37	-12054.00	602.50
2277	GOUT37	-12068.00	747.50
2278	GOUT38	-12082.00	602.50
2279	GOUT38	-12096.00	747.50
2280	GOUT39	-12110.00	602.50
2281	GOUT39	-12124.00	747.50
2282	GOUT40	-12138.00	602.50
2283	GOUT40	-12152.00	747.50
2284	GOUT41	-12166.00	602.50
2285	GOUT41	-12180.00	747.50
2286	GOUT42	-12194.00	602.50
2287	GOUT42	-12208.00	747.50
2288	GOUT43	-12222.00	602.50
2289	GOUT43	-12236.00	747.50
2290	GOUT44	-12250.00	602.50
2291	GOUT44	-12264.00	747.50
2292	GOUT45	-12278.00	602.50
2293	GOUT45	-12292.00	747.50
2294	GOUT46	-12306.00	602.50
2295	GOUT46	-12320.00	747.50
2296	GOUT47	-12334.00	602.50
2297	GOUT47	-12348.00	747.50
2298	GOUT48	-12362.00	602.50
2299	GOUT48	-12376.00	747.50
2300	GOUT49	-12390.00	602.50
2301	GOUT49	-12404.00	747.50
2302	GOUT50	-12418.00	602.50
2303	GOUT50	-12432.00	747.50
2304	GOUT51	-12446.00	602.50
2305	GOUT51	-12460.00	747.50
2306	GOUT52	-12474.00	602.50
2307	GOUT52	-12488.00	747.50
2308	GOUT53	-12502.00	602.50
2309	GOUT53	-12516.00	747.50
2310	GOUT54	-12530.00	602.50
2311	GOUT54	-12544.00	747.50
2312	GOUT55	-12558.00	602.50
2313	GOUT55	-12572.00	747.50
2314	GOUT56	-12586.00	602.50
2315	GOUT56	-12600.00	747.50
2316	GOUT57	-12614.00	602.50
2317	GOUT57	-12628.00	747.50
2318	GOUT58	-12642.00	602.50
2319	GOUT58	-12656.00	747.50
2320	GOUT59	-12670.00	602.50
2321	GOUT59	-12684.00	747.50
2322	GOUT60	-12698.00	602.50
2323	GOUT60	-12712.00	747.50
2324	GOUT61	-12726.00	602.50
2325	GOUT61	-12740.00	747.50
2326	GOUT62	-12754.00	602.50
2327	GOUT62	-12768.00	747.50
2328	GOUT63	-12782.00	602.50
2329	GOUT63	-12796.00	747.50

NO.	PAD NAME	X-axis	Y-axis
2330	GOUT64	-12810.00	602.50
2331	GOUT64	-12824.00	747.50
2332	GOUT65	-12838.00	602.50
2333	GOUT65	-12852.00	747.50
2334	GOUT66	-12866.00	602.50
2335	GOUT66	-12880.00	747.50
2336	GOUT67	-12894.00	602.50
2337	GOUT67	-12908.00	747.50
2338	GOUT68	-12922.00	602.50
2339	GOUT68	-12936.00	747.50
2340	VGLO	-12950.00	602.50
2341	VGLO	-12964.00	747.50
2342	VGLO	-12978.00	602.50
2343	VGLO	-12992.00	747.50
2344	VRGH	-13006.00	602.50
2345	VRGH	-13020.00	747.50
2346	VRGH	-13034.00	602.50
2347	VRGH	-13048.00	747.50
2348	LVGL	-13062.00	602.50
2349	LVGL	-13076.00	747.50
2350	LVGL	-13090.00	602.50
2351	LVGL	-13104.00	747.50
2352	GDUM12	-13118.00	602.50
2353	GDUM12	-13132.00	747.50
2354	GOUT69	-13146.00	602.50
2355	GOUT69	-13160.00	747.50
2356	GOUT70	-13174.00	602.50
2357	GOUT70	-13188.00	747.50
2358	VGHO	-13202.00	602.50
2359	VGHO	-13216.00	747.50
2360	VGHO	-13230.00	602.50
2361	VGHO	-13244.00	747.50
2362	PADA4	-13258.00	602.50
2363	PADA3	-13272.00	747.50
2364	AVSSDUM35	-13286.00	602.50
2365	AVSSDUM36	-13300.00	747.50
2366	AVSSDUM36	-13314.00	602.50

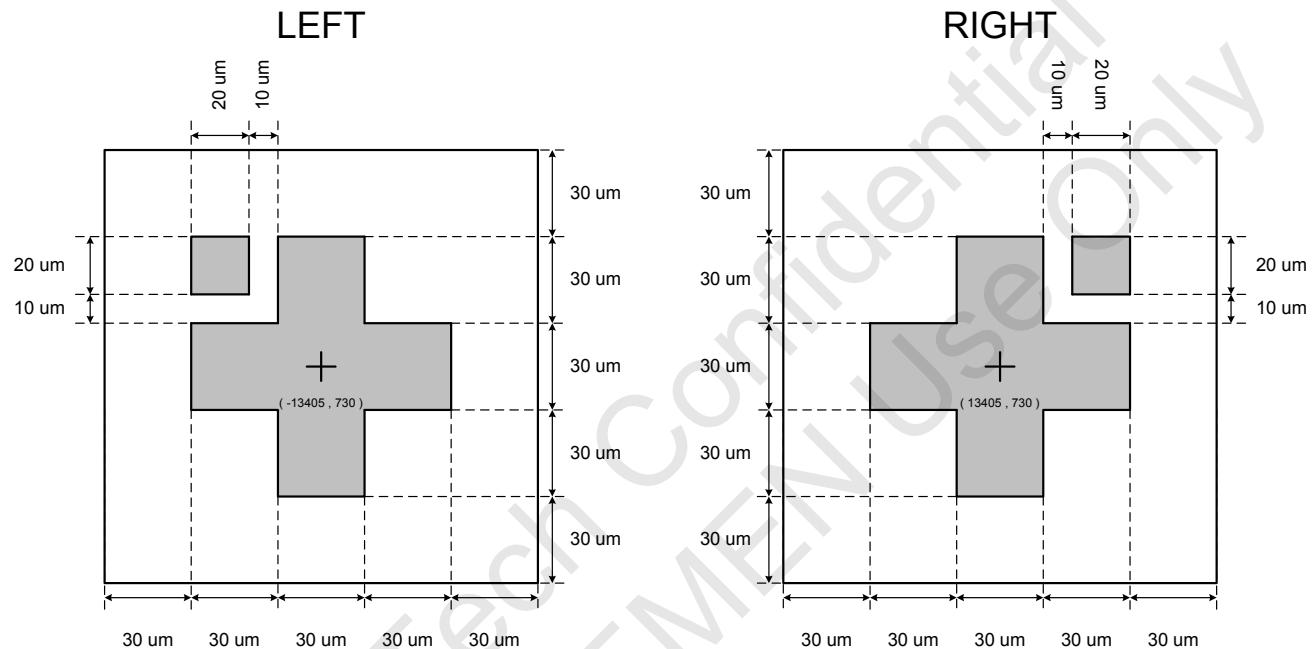
8.4. Alignment Mark

--Alignment Mark coordinate

Left (-13405, 730)

Right (13405, 730)

--Alignment Mark size



9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page	Auditor
NOV. 02, 2011	1.0	1. TE control 2. Add TE state setting 3. Modify HSYNC output control 4. Modify pump1_clamp[1 :0] table 5. Add CABC_AIE PWM dummy Setting 6. Add diagram for PWM/TE/HSYNC control 7. Add OSC freq for PWM generation 8. Modify Power consumption table 9. Add note for VDD < VDDIO case is not supported	120 123 126-128 133-134 157 299 304 304 305	Daniel.Chang
SEP. 22, 2011	0.5	1. Add D2(MH) bit, but don't care 2. Add D2(MH) bit, but keep '0' 3. Add C2 bit (Reserved) for 55h 4. Add descriptions for error report read control (0Eh D0) 5. Add C0B0h(TE_WIDTH) register 6. Modify the diagram for BC_SEL(C6B4h) 7. Remove C6B5h Register 8. Modify E1h/E2h mapping table(with don't care bit) 9. Add duty ratio mapping table for BC PWM pulse 10. Analog Gamma programming and checking flow	33 64-66 78 113 131-133 165 166 215,217 317 321	Daniel.Chang
AUG. 26, 2011	0.4	1. Modify command2 list 2. Add AE8Fh for OTP programming status check 3. Add HSYNC output control 4. Modify the TYPO 5. VDD_18V, LVDSVDD, DIOPWR table update 6. Add C6B2h (Reserved) 7. Change the default value of C5B1h 8. Add gnd_option bit 9. Add CFC9h register 10. Add ID1/2/3, DDB Write 11. Modify ECh ~ EEh registers	24-25 91 111-112 125-128 129 134 168 170 171 172-174 195-197	Daniel.Chang
AUG. 04, 2011	0.3	VDD_18V and LVDSVDD voltage table update	127	Tz Shyan Yang
JUL. 21, 2011	0.2	1. Revise General description 2. Revise the pin description 3. Add DC/AC characteristics	16	Max.lin
JUN. 14, 2011	0.1	Original.		Max.lin