

瑞鼎科技股份有限公司
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RM69032 Data Sheet

Single Chip Driver with 16.7M color

for 540RGBx960 LTPS AMOLED

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Revision History

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0.0	2012/06/05		New version
0.1	2013/09/02	229	osc clock characteristics update

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1. General Description

RM69032 is a 16.7 million-color single-chip SoC driver for LTPS AMOLED driver IC that supply resolution of 480RGBx800, 480RGBx854, 480RGBx864, 540x960 with internal GRAM and 540RGB x 1024 by pass internal GRAM. RM69032 comprise a 1620-channel source driver, gate control timing by level shift, 1,555,200 bytes GRAM for graphic data of 540RGBx960 dots, and power supply circuit.

The RM69032 supports 24-/16-/8-bit data bus interface, I2C interface and serial peripheral interfaces (SPI). It also supplies 24bit, 18-bit or 16-bit RGB interface, MDDI interface and MIPI interface for driving video signal directly from application controller. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

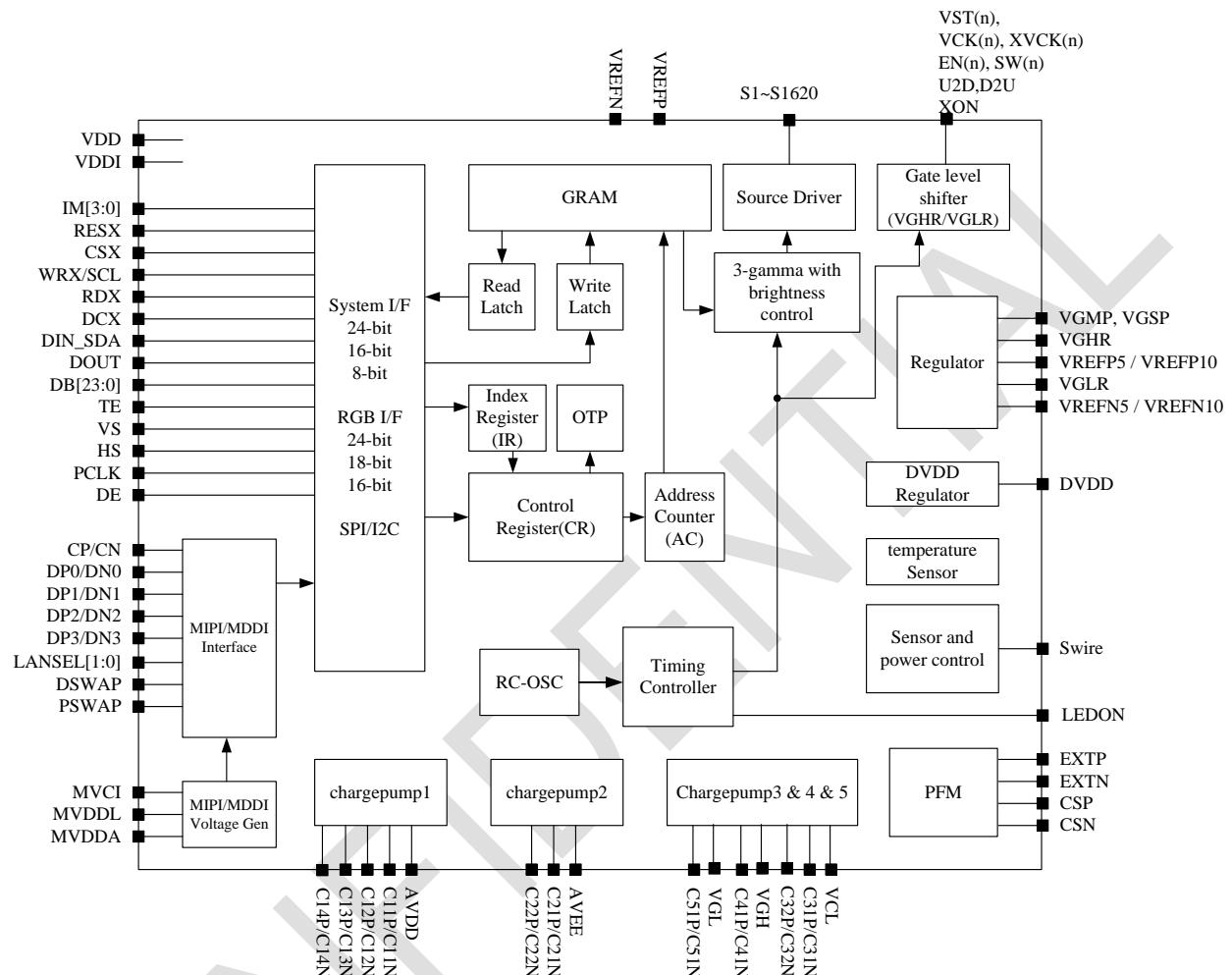
RM69032 can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving a LTPS AMOLED panel. The RM69032 also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the RM69032 an ideal driver for portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- A single-chip controller driver for a QHD panel type LTPS AMOLED display
- Display resolution option
 - (1). With GRAM:
 1. 540RGB x 960
 2. 480RGB x 854
 3. 480RGB x 854
 4. 480RGB x 864
 - (2). By pass GRAM:
 1. 480RGB x 1024
 2. 540RGB x 1024
- RAM size: $540 \times 3 \times 960 = 1,555,200$ bytes
- System interface
 - (1). 8-, 16-, 24-bits 80-series MPU interface
 - (2). 16-bits serial peripheral interface
 - (3). I2C interface
- Moving picture display interface
 - (1). 16-, 18-, 24-bit RGB interface (SYNC and DE mode)
- High speed interface
 - (1). Mobile Display Digital Interface (MDDI V1.2, 1 clock and 1 or 2 data lane pairs)
 - (2). MIPI Display Serial Interface (DSI V1.01 r11 and D-PHY V1.0, 1 clock and 2 to 4 data lane pairs)
- Display color mode
 - (1). Full color mode: 16.7M colors
 - (2). Reduce color mode:
 1. 262k colors
 2. 65k colors
 3. 8 colors (Idle mode)

- Window address function to specify a rectangular area writing data in the internal RAM
- Abundant color display and drawing functions
 - (1). Programmable γ-correction function for 16.7 million color display
 - (2). Individual gamma correction setting for RGB dots
 - (3). Partial display function
- Low power consumption architecture
 - (1). Deep standby mode
 - (2). Sleep mode
 - (3). 8-color display function
- Power supply startup sequencer
- Four GPO pins for external control
- On chip checksums check
- Operating temperate: -30°C ~ 70°C
- On module DC/DC converter
 - (1). DDVDH=4.5V to 6.5V
 - (2). DDVDL=-4.5V to -6.5V
 - (3). VCL=-2.5V to -4.0V
 - (4). Positive gamma high voltage level: VGMP=4.5V to 6.5V
 - (5). Positive gamma low voltage level: VGSP=0.0V, 0.3V to 3.7V
 - (6). Positive gate driver output voltage level: VGH=+7V to +18V
 - (7). Negative gate driver output voltage level: VGL=-8V to -18V
- Input power supply voltages:
 - (1). IOVCC (VDDI) = 1.65V~3.3V
 - (2). VDDIL = 1.1V~1.3V
 - (3). VCI = 2.3V~4.8V
 - (4). MIPI/MDDI regulator supply voltage range: 2.3V ~ 4.8V

3. Block Diagram



4. Pin Description

Power Supply Pins

Signal	I/O	Function
VDBB	P	Power supply for DC/DC converter VDBB, VDDA and VDDR should be the same input voltage level
VDDA	P	Power supply for analog system VDBB, VDDA and VDDR should be the same input voltage level
VDDR	P	Power supply for regulator system VDBB, VDDA and VDDR should be the same input voltage level
VDD_DET	P	Connect to VDBB/VDDA/VDDR for detection
VDDAM	P	Power supply for MIPI/MDDI analog regulator system
VDDI	P	Power supply for interface system except MIPI/MDDI interface
VSSB	P	System ground for DC/DC converter
VSSA	P	System ground for analog system
VSSR	P	System ground for regulator system
VSSAM	P	System ground for internal MIPI/MDDI analog system
VSSI	P	System ground for interface system except MIPI/MDDI interface
VSS3D	P	System ground for 3D control PAD
DVSS	P	System ground for internal digital system
AVSS	P	System ground for source OP system.
MTP_PWR	P	MTP programming power supply pin (7.5V typical) Must be left open or connected to DVSS in normal condition.

Interface Pins

Signal	I/O	Function
CSX	I	Chip select input pin ("Low" enable) in 80-series MPU I/F and SPI I/F. This pin is not used for I2C, MIPI or MDDI I/F, please connect to VSSI.
WRX (SCL / I2C_SCL)	I	WRX: Writes strobe signal to write data when WRX is "Low" in 80-series MPU I/F. SCL: A synchronous clock signal in SPI I/F. I2C_SCL: Serial input clock in I2C I/F. This pin is not used for MIPI or MDDI I/F, please connect to VSSI.
RDX	I	Reads strobe signal to write data when RDX is "Low" in 80-series MPU interface. This pin is not used for 16-bit SPI, I2C, MIPI or MDDI I/F, please connect to VSSI.
D/CX	I	Display data / command selection in 80-series MPU I/F. D/CX = "0" : Command D/CX = "1" : Display data or Parameter This pin is not used for 9-bit/16-bit SPI, I2C, MIPI or MDDI I/F, please connect to VSSI.
D[23:0]	I/O	24-bit bi-directional data bus for 80-series MPU I/F and 24-bit input data bus for RGB I/F. For 8080-series MPU I/F: 8-bit interface: D[7:0] are used, D[23:8] should be connected to VSSI 16-bit interface: D[15:0] are used, D[23:16] should be connected to VSSI 24-bit interface: D[23:0] are used For RGB I/F: 16-bit/pixel: D[20:16]=R[4:0], D[13:8]=G[5:0] and D[4:0]=B[4:0], connect unused pins to VSSI 18-bit/pixel: D[21:16]=R[5:0], D[13:8]=G[5:0] and D[5:0]=B[5:0], connect unused pins to VSSI 24-bit/pixel: D[23:16]=R[7:0], D[15:8]=G[7:0] and D[7:0]=B[7:0]

		These pins are not used for SPI, I2C, MIPI or MDDI I/F, please connect to VSSI.
SDI (I2C_SDA)	I/O	SDI: Serial input signal in SPI I/F. The data is input on the rising/falling edge of the SCL signal. I2C_SDA: Serial input/output signal in I2C I/F. The data is input/output on the rising edge of the I2C_SCL signal. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI.
SDO	O	Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal. If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together. This pin is not used for 80-series MPU, I2C, MIPI or MDDI I/F, please open this pin.
PCLK	I	Pixel clock signal in RGB I/F. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI.
VS	I	Vertical sync. Signal in RGB I/F. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI.
HS	I	Horizontal sync. Signal in RGB I/F. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI.
DE	I	Data enable signal in RGB I/F mode 1. This pin is not used for RGB mode 2, 80-series MPU, MIPI or MDDI I/F, please connect to VSSI.

MIPI/MDDI Interface Pins

Signal	I/O	Function															
HSSI_CLK_P HSSI_CLK_N	I	-These pins are DSI-CLK+/- differential clock signals if MIPI interface is used. -These pins are MDDI_STB_P/M differential strobe signals if MDDI interface is used. -HSSI_CLK_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. -If not used, please connect these pins to VSSAM.															
HSSI_D0_P HSSI_D0_N	I/O	-These pins are DSI-D0+/- differential data signals if MIPI interface is used. -These pins are MDDI_DATA0_P/M differential strobe signals if MDDI interface is used. -HSSI_D0_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. -If not used, please connect these pins to VSSAM.															
HSSI_D1_P HSSI_D1_N	I	-These pins are DSI-D1+/- differential data signals if MIPI interface is used. -These pins are MDDI_DATA1_P/M differential strobe signals if MDDI interface is used. -HSSI_D1_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. -If not used, please connect these pins to VSSAM.															
HSSI_D21_P HSSI_D21_N	I	-These pins are differential data signals if MIPI interface is used. -HSSI_D21_P/N or HSSI_D22_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. -If not used, please connect these pins to VSSAM.															
HSSI_D22_P HSSI_D22_N	I	-These pins are differential data signals if MIPI interface is used. -HSSI_D21_P/N or HSSI_D22_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. -If not used, please connect these pins to VSSAM.															
ERR	O	CRC and ECC error output pin for MIPI interface. This pin is output low when it is not activated. When this pin is activated, it output high if CRC/ECC error found. If not used, please open this pin.															
LANSEL[1:0]	I	Input pin to select number of data lanes in MIPI interface. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>LANSEL[1]</th> <th>LANSEL[0]</th> <th>DATA LANE of MIPI</th> </tr> <tr> <td>0</td> <td>0</td> <td>2 data lane</td> </tr> <tr> <td>0</td> <td>1</td> <td>3 data lane</td> </tr> <tr> <td>1</td> <td>0</td> <td>4 data lane</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reserved</td> </tr> </table> If not used, please connect to VSSI.	LANSEL[1]	LANSEL[0]	DATA LANE of MIPI	0	0	2 data lane	0	1	3 data lane	1	0	4 data lane	1	1	Reserved
LANSEL[1]	LANSEL[0]	DATA LANE of MIPI															
0	0	2 data lane															
0	1	3 data lane															
1	0	4 data lane															
1	1	Reserved															

DSWAP[1:0] PSWAP	I	Input pin to select HSSI_D0/D1 data lane sequence and polarity in high speed interface only. For MIPI interface, both DSWAP and PSWAP function are available. For MDDI interface, only PSWAP function is available. Please connect DSWAP[1:0] pins to VSSI (i.e. only DSWAP[1:0]=00 in below table is valid for MDDI interface).										
		Pin Name	HSSI_D21_P	HSSI_D21_N	HSSI_D0_P	HSSI_D0_N	HSSI_CLK_P	HSSI_CLK_N	HSSI_D1_P	HSSI_D1_N	HSSI_D22_P	HSSI_D22_N
		DSWAP=00 PSWAP=0	DSI D2+	DSI D2-	DSI D0+	DSI D0-	DSI CLK+	DSI CLK-	DSI D1+	DSI D1-	DSI ID3+	DSI D3-
		DSWAP=00 PSWAP=1	DSI D2-	DSI D2+	DSI D0-	DSI D0+	DSI CLK-	DSI CLK+	DSI D1-	DSI D1+	DSI D3-	DSI D3+
		DSWAP=01 PSWAP=0	DSI D2+	DSI D2-	DSI D1+	DSI D1-	DSI CLK+	DSI CLK-	DSI D0+	DSI D0-	DSI D3+	DSI D3-
		DSWAP=01 PSWAP=1	DSI D2-	DSI D2+	DSI D1-	DSI D1+	DSI CLK+	DSI CLK-	DSI D0-	DSI D0+	DSI D3-	DSI D3+
		DSWAP=10 PSWAP=0	DSI D3+	DSI D3-	DSI D0+	DSI D0-	DSI CLK+	DSI CLK-	DSI D1+	DSI D1-	DSI D2+	DSI D2-
		DSWAP=10 PSWAP=1	DSI D3-	DSI D3+	DSI D0-	DSI D0+	DSI CLK-	DSI CLK+	DSI D1-	DSI D1+	DSI D2-	DSI D2+
If not used, please connect to VSSI.												

NOTE: "1" = VDDI level, "0" = VSSI level.

Interface Logic Pins

Signal	I/O	Function																																																												
RESX	I	<p>This signal will reset the device and must be applied to properly initialize the chip. Signal is active low. The input voltage range for RESX pin is related to DSTB_SEL and VSEL pins.</p> <table border="1"> <thead> <tr> <th colspan="2">Input Voltage Level (DSTB_SEL="0")</th> <th>Min.</th> <th>Max.</th> <th>Unit</th> </tr> </thead> <tbody> <tr> <td rowspan="2">VDDI=1.65~3.3V</td> <td>Logic High level input voltage</td> <td>0.7xVDDI</td> <td>VDDI</td> <td>V</td> </tr> <tr> <td>Logic Low level input voltage</td> <td>VSSI</td> <td>0.3xVDDI</td> <td>V</td> </tr> <tr> <td rowspan="2">VDDI=1.1~1.3V</td> <td>Logic High level input voltage</td> <td>0.88</td> <td>1.35</td> <td>V</td> </tr> <tr> <td>Logic Low level input voltage</td> <td>VSSI</td> <td>0.55</td> <td>V</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th colspan="2">Input Voltage Level (DSTB_SEL="1")</th> <th>VDDI=1.65~3.3V</th> <th>VDDIL=1.1~1.3V</th> <th rowspan="2">Unit</th> </tr> <tr> <th></th> <th></th> <th>Min.</th> <th>Max.</th> </tr> </thead> <tbody> <tr> <td rowspan="2">VSEL =High</td> <td>Logic High level input voltage</td> <td>0.7xVDDI</td> <td>VDDI</td> <td>1.155</td> <td>V</td> </tr> <tr> <td>Logic Low level input voltage</td> <td>VSSI</td> <td>0.3xVDDI</td> <td>VSSI</td> <td>0.585</td> <td>V</td> </tr> <tr> <td rowspan="2">VSEL =Low</td> <td>Logic High level input voltage</td> <td>0.88</td> <td>1.35</td> <td>0.88</td> <td>V</td> </tr> <tr> <td>Logic Low level input voltage</td> <td>VSSI</td> <td>0.55</td> <td>VSSI</td> <td>0.55</td> <td>V</td> </tr> </tbody> </table>					Input Voltage Level (DSTB_SEL="0")		Min.	Max.	Unit	VDDI=1.65~3.3V	Logic High level input voltage	0.7xVDDI	VDDI	V	Logic Low level input voltage	VSSI	0.3xVDDI	V	VDDI=1.1~1.3V	Logic High level input voltage	0.88	1.35	V	Logic Low level input voltage	VSSI	0.55	V	Input Voltage Level (DSTB_SEL="1")		VDDI=1.65~3.3V	VDDIL=1.1~1.3V	Unit			Min.	Max.	VSEL =High	Logic High level input voltage	0.7xVDDI	VDDI	1.155	V	Logic Low level input voltage	VSSI	0.3xVDDI	VSSI	0.585	V	VSEL =Low	Logic High level input voltage	0.88	1.35	0.88	V	Logic Low level input voltage	VSSI	0.55	VSSI	0.55	V
		Input Voltage Level (DSTB_SEL="0")		Min.	Max.	Unit																																																								
		VDDI=1.65~3.3V	Logic High level input voltage	0.7xVDDI	VDDI	V																																																								
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			Logic Low level input voltage	VSSI	0.3xVDDI	VSSI	0.585	V																																																						
VSEL =Low	Logic High level input voltage	0.88	1.35	0.88	V																																																									
	Logic Low level input voltage	VSSI	0.55	VSSI	0.55	V																																																								
<p>Interface type selection. The connections of IM[3:0] which not shown in table are invalid.</p> <table border="1"> <thead> <tr> <th>IM[3:0]</th> <th>Display Data</th> <th>Command</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>80-series 8-bit MPU I/F, D[7:0]</td> <td>80-series 8-bit MPU I/F, D[7:0]</td> </tr> <tr> <td>0001</td> <td>80-series 16-bit MPU I/F, D[15:0]</td> <td>80-series 16-bit MPU I/F, D[15:0]</td> </tr> <tr> <td>0010</td> <td>80-series 24-bit MPU I/F, D[23:0]</td> <td>80-series 24-bit MPU I/F, D[23:0]</td> </tr> <tr> <td>0011</td> <td>RGB I/F, D[23:0]</td> <td>16-bit SPI (SCL rising edge trigger), SDI/SDO</td> </tr> <tr> <td>1011</td> <td>RGB I/F, D[23:0]</td> <td>16-bit SPI (SCL falling edge trigger), SDI/SDO</td> </tr> <tr> <td>0100</td> <td>MIPI DSI,</td> <td>MIPI DSI</td> </tr> <tr> <td>0101</td> <td>MDDI,</td> <td>MDDI, 16-bit SPI (SCL rising edge trigger), SDI/SDO</td> </tr> <tr> <td>0110</td> <td>MDDI,</td> <td>MDDI, 16-bit SPI (SCL falling edge trigger), SDI/SDO</td> </tr> <tr> <td>1110</td> <td>MDDI,</td> <td>MDDI, I2C I/F, I2C_SDA serial data</td> </tr> <tr> <td>0111</td> <td>RGB I/F, D[23:0]</td> <td>I2C I/F, I2C_SDA</td> </tr> </tbody> </table>					IM[3:0]	Display Data	Command	0000	80-series 8-bit MPU I/F, D[7:0]	80-series 8-bit MPU I/F, D[7:0]	0001	80-series 16-bit MPU I/F, D[15:0]	80-series 16-bit MPU I/F, D[15:0]	0010	80-series 24-bit MPU I/F, D[23:0]	80-series 24-bit MPU I/F, D[23:0]	0011	RGB I/F, D[23:0]	16-bit SPI (SCL rising edge trigger), SDI/SDO	1011	RGB I/F, D[23:0]	16-bit SPI (SCL falling edge trigger), SDI/SDO	0100	MIPI DSI,	MIPI DSI	0101	MDDI,	MDDI, 16-bit SPI (SCL rising edge trigger), SDI/SDO	0110	MDDI,	MDDI, 16-bit SPI (SCL falling edge trigger), SDI/SDO	1110	MDDI,	MDDI, I2C I/F, I2C_SDA serial data	0111	RGB I/F, D[23:0]	I2C I/F, I2C_SDA																									
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CGM[2:0]	I	Resolution selection																																												
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CGM[2:0]	Resolution																																													
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101	480RGBx864																																													
110	480RGBx854																																													
111	480RGBx800																																													
I2C_SA0	I	Select the I2C interface address from MPU. If not used, please connect to VSSI.																																												
		<table border="1"> <thead> <tr> <th>I2C_SA0</th><th>Slave Address</th></tr> </thead> <tbody> <tr><td>0</td><td>1001100</td></tr> <tr><td>1</td><td>1001101</td></tr> </tbody> </table>	I2C_SA0	Slave Address	0	1001100	1	1001101																																						
I2C_SA0	Slave Address																																													
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DSTB_SEL	I	<p>Input pin to control DIOPWR regulator on/off.</p> <table border="1"> <thead> <tr> <th>DSTB_SEL</th><th>DIOPWR Regulator</th><th>VSEL Function</th></tr> </thead> <tbody> <tr><td>0</td><td>DIOPWR Off</td><td>Invalid</td></tr> <tr><td>1</td><td>DIOPWR On</td><td>Valid</td></tr> </tbody> </table>	DSTB_SEL	DIOPWR Regulator	VSEL Function	0	DIOPWR Off	Invalid	1	DIOPWR On	Valid																																			
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<p>Input pin to switch the I/O voltage. This VSEL function only apply for RESX, TE, LEDPWM, LEDON pins. The VSEL dual IO function is valid when DSTB_SEL="1".</p> <table border="1"> <thead> <tr> <th rowspan="2">DSTB_SEL</th><th rowspan="2">VDDI</th><th rowspan="2">VSEL</th><th rowspan="2">DIOPWR</th><th colspan="2">TE Output Voltage Level</th></tr> <tr> <th>VOH</th><th>VOL</th></tr> </thead> <tbody> <tr><td>0</td><td>1.65~3.3V or 1.1~1.3V</td><td>X</td><td>Off</td><td>VDDI</td><td>VSSI</td></tr> <tr> <td rowspan="2">1</td><td rowspan="2">1.65~3.3V</td><td>0</td><td>1.2V</td><td>1.2V</td><td>VSSI</td></tr> <tr> <td>1</td><td>1.8V</td><td>VDDI or DIOPWR</td><td>VSSI</td></tr> <tr> <td rowspan="2">1</td><td rowspan="2">1.1~1.3V</td><td>0</td><td>1.2V</td><td>1.2V</td><td>VSSI</td></tr> <tr> <td>1</td><td>1.8V</td><td>1.8V</td><td>VSSI</td></tr> </tbody> </table> <p>The input voltage range for VSEL pin:</p> <table border="1"> <thead> <tr> <th>Input Voltage Level</th><th>Min.</th><th>Max.</th><th>Unit</th></tr> </thead> <tbody> <tr><td>Logic High level input voltage</td><td>0.88</td><td>VDDI</td><td>V</td></tr> <tr><td>Logic Low level input voltage</td><td>VSSI</td><td>0.55</td><td>V</td></tr> </tbody> </table> <p>If not used, please connect to VSSI.</p>	DSTB_SEL	VDDI	VSEL	DIOPWR	TE Output Voltage Level		VOH	VOL	0	1.65~3.3V or 1.1~1.3V	X	Off	VDDI	VSSI	1	1.65~3.3V	0	1.2V	1.2V	VSSI	1	1.8V	VDDI or DIOPWR	VSSI	1	1.1~1.3V	0	1.2V	1.2V	VSSI	1	1.8V	1.8V	VSSI	Input Voltage Level	Min.	Max.	Unit	Logic High level input voltage	0.88	VDDI	V	Logic Low level input voltage	VSSI	0.55	V
DSTB_SEL					VDDI	VSEL	DIOPWR	TE Output Voltage Level																																						
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0	1.65~3.3V or 1.1~1.3V	X	Off	VDDI	VSSI																																									
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1	1.1~1.3V	0	1.2V	1.2V	VSSI																																									
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Logic Low level input voltage	VSSI	0.55	V																																											

EXB1T	I	Input pin to select the external AVDD DC/DC voltage. <table border="1"> <tr> <td>EXB1T</td><td>AVDD Voltage</td></tr> <tr> <td>0</td><td>Use internal DC/DC for AVDD</td></tr> <tr> <td>1</td><td>Use PFM for AVDD</td></tr> </table>	EXB1T	AVDD Voltage	0	Use internal DC/DC for AVDD	1	Use PFM for AVDD
EXB1T	AVDD Voltage							
0	Use internal DC/DC for AVDD							
1	Use PFM for AVDD							
GPO[1:0]	O	Output pins to control the external circuit. The output voltage swing is VDDI to VSSI. If not used, please open these pins.						
TE_L	O	Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is output low.						
TE_R	O	If not used, please open this pin.						
MUX13	I	SD output MUX selection. MUX13 = 0, SD output mux 1:1. MUX13 = 1, SD output mux 1:3.						
PMOS [1:0]	I	LTPS process type selection. PMOS[1:0] = 00 : CMOS type PMOS[1:0] = 01 : PMOS type PMOS[1:0] = 10 : NMOS 2phase type PMOS[1:0] = 11 : NMOS 4phase type						
SWIRE	O	Swire protocol setting pin of Power IC, If not used, please open this pin.						
OLED_EN	O	Power IC enable control pin, If not used, please open this pin.						
SCL_M	O	Serial output clock in I2C I/F for temperature sensor IC. If not used, please open this pin.						
SDA_M	I/O	Serial input/output clock in I2C I/F for temperature sensor IC. If not used, please open this pin.						

NOTE: "1" = VDDI level, "0" = VSSI level.

Driver Output Pins (Pins for Panel)

Signal	I/O	Function
S1 ~ S1620	O	Pixel electrode driving output.
SDUM0 ~ SDUM3	O	Dummy Source, leave it Open.
U2D_R,D2U_R, U2D_L,D2U_L	O	VSR control signals, Level shift output, (VGHR-VGLR)
VST1-8_R VST1-8_L	O	VSR control signals, Level shift output, (VGHR-VGLR)
VCK1-2_R XVCK1-2_R VCK1-2_L XVCK1-2_L	O	VSR control signals, Level shift output, (VGHR-VGLR)
EN1-3_R EN1-3_L	O	VSR control signals, Level shift output, (VGHR-VGLR)
SW1-3_R SW1-3_L	O	VSR control signals, Level shift output, (VGHR-VGLR)
XON_R, XON_L	O	VSR control signals, Level shift output, (VGHR-VGLR)
D3_P1 D3_P2	O	Control signals for 3D panel(BVP3D-VSS3D).

DC/DC Convert Pins

Signal	I/O	Function
AVDD	O	Output voltage from step-up circuit 1, generated from VDDB. Connect a capacitor for stabilization.
AVEE	O	Output voltage from step-up circuit 2, generated from VDDB. Connect a capacitor for stabilization.
VCL	O	Output voltage from step-up circuit 3, generated from VDDB. Connect a capacitor for stabilization.
VGH	O	Output voltage from step-up circuit 4. Connect a capacitor for stabilization.
VGL	O	Output voltage from step-up circuit 5. Connect a capacitor for stabilization.
C11P, C11N C12P, C12N C13P, C13N C14P, C14N	IO	Capacitor connection pins for the step-up circuit which generate AVDD. Connect capacitor as requirement. When not in used, please open these pins.
C21P, C21N C22P, C22N	IO	Capacitor connection pins for the step-up circuit which generate AVEE. Connect capacitor as requirement. When not in used, please open these pins.
C31P, C31N C32P, C32N	IO	Capacitor connection pins for the step-up circuit which generate VCL. Connect capacitor as requirement.
C41P, C41N	IO	Capacitor connection pins for the step-up circuit which generate VGH. Connect capacitor as requirement.
C51P, C51N	IO	Capacitor connection pins for the step-up circuit which generate VGLX. Connect capacitor as requirement.
VGHR	O	Output voltage generated from VGH. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
VGLR	O	Output voltage generated from VGL. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
BVP3D	O	Positive voltage level for 3D control signals. Connect a capacitor for stabilization. When not in use, please open this pin.
BVN3D	O	Negative voltage level for 3D control signals. Connect a capacitor for stabilization. When not in use, please open this pin.
VGMP	O	Output voltage generated from AVDD. LDO output for positive gamma high voltage generator.
VGSP	O	Output voltage generated from AVDD. LDO output for positive gamma low voltage generator.
VREF	O	Regulator output for internal reference voltage. Connect capacitor for stabilization.
VREFCP	O	Reference voltage for internal voltage generating circuit. Connect capacitor for stabilization
EXTP	O	PFM1 control output for DC/DC converter to generate AVDD. Connect to gate of external NMOS device.
EXTN	O	PFM2 control output for DC/DC converter to generate AVEE. Connect to gate of external PMOS device.
CSP	O	TEST pin, When not in use, please open this pin

CSN	O	TEST pin, When not in use, please open this pin
DVDD	O	Regulator output for logic system power. Connect a capacitor for stabilization.
DIOPWR	O	Regulator output for dual I/O voltage system Connect a capacitor for stabilization if dual I/O application is used. When not in use, please open this pin.
MVDDA	O	Regulator output for internal MIPI/MDDI analog system (1.5V typical) Connect a capacitor for stabilization. If not use MIPI or MDDI interface, please open this pin.
MVDDL	O	Regulator output for internal MIPI low power system (1.2V typical) Connect a capacitor for stabilization. If not use MIPI interface, please open this pin.
VREFP	O	Positive reference voltage for the panel voltage. Connect to VREFP10 or VREFP5. Connect to a stabilizing capacitor.
VREFP10	O	Regulator output for VREFP(3~15V)
VREFP5	O	Regulator output for VREFP(1~5V)
VREFN	O	Positive reference voltage for the panel voltage. Connect to VREFN10 or VREFN5. Connect to a stabilizing capacitor.
VREFN10	O	Regulator output for VREFP(-3~-15V)
VREFN5	O	Regulator output for VREFP(-1~-5V)

Test Pins

Signal	I/O	Function
PADA1~PADA7 PADB1~PADB7	I/O	These test pins for bonding resistance measurement. These pins are Hi-Z in driver IC. PADA1 and PADA2 are short in driver IC. PADA3, PADA5 and PADA6 are short in driver IC. PADA4 and PADA7 are short in driver IC. PADB1 and PADB2 are short in driver IC. PADB3, PADB5 and PADB6 are short in driver IC. PADB4 and PADB7 are short in driver IC.
ANALOG_TEST	IO	Test pin, not accessible to user. Must be left open.
VDDI_OPT1~2	O	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave it open.
VSSI_OPT1	O	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave it open.
GDUM1~12 GOUTDUM* DUMY0~7	-	Dummy PAD, leave it open.
VSSIDUM0~1	O	These pins are dummy with VSSI potential
AVSSDUM0~36	O	-These pins are dummy with AVSS potential
TEST1~2	I	Test pins

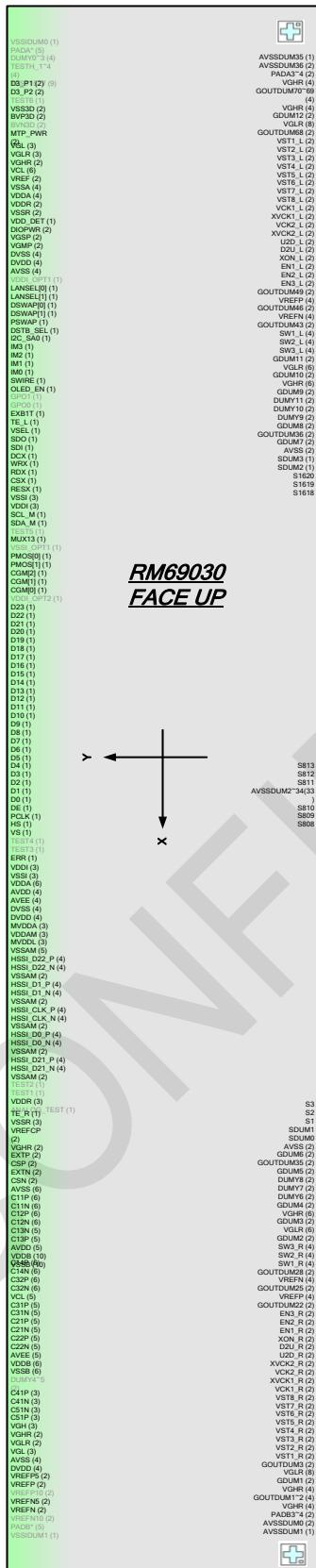
TEST3~15	I/O	Test pins, not accessible to user. Must be left open.
TESTH_1~4		

CONFIDENTIAL

LTPS AMOLED Drive Power Supply Specifications Table

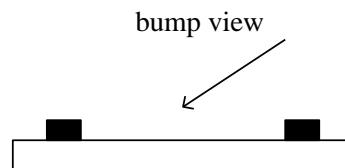
No.	Item		Description
1	LTPS AMOLED source driver		1620 pins (S1 ~ S1620)
3	LTPS AMOLED drive output	S1~S1620	V0~V255 grayscales
4	Input voltage	IOVCC	1.65V~3.30V
		VCI	2.30V~4.80V
5	LTPS AMOLED drive voltages	DDVDH(AVDD)	4.5V ~ 6.5V
		DDVDL (AVEE)	-4.5V ~ -6.5V
		VGH	7.0V ~ 18V
		VGL	-8V ~ -18V
		VGH-VGL	Avoid exceed 32v
6	Internal step-up circuits	DDVDH(AVDD)	VClx1.5, VClx1.66, VClx2, VClx2.5, VClx3
		DDVDL(AVEE)	VClx-2,VClx-3
		VCL	VClx-0.5, VClx-1.0, VClx-2.0
		VGH	VClx3, VClx4, VClx5, VClx6
		VGL	VClx-3, VClx-4, VClx-5, VClx-6

5. Pad Diagram and Coordination

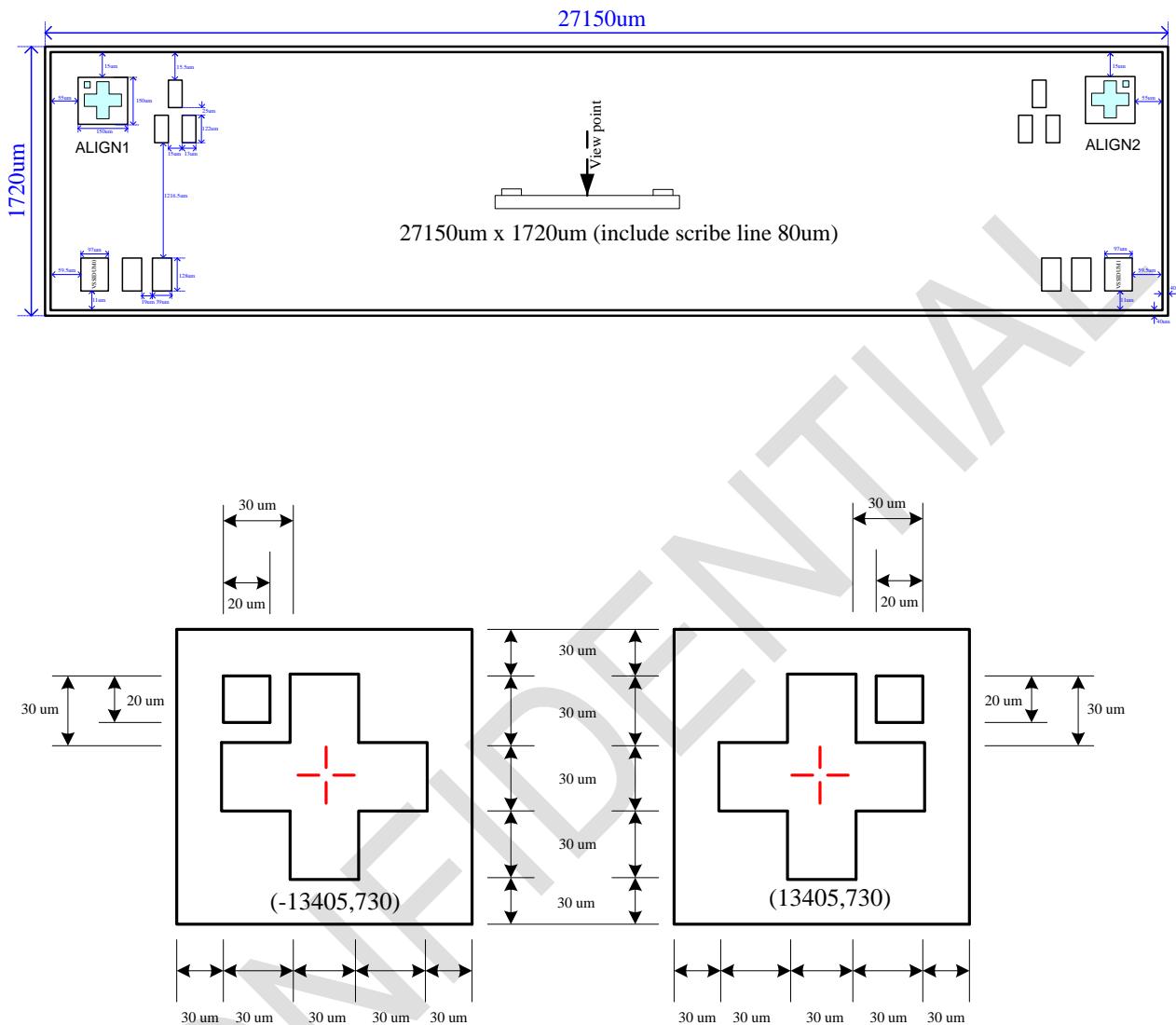


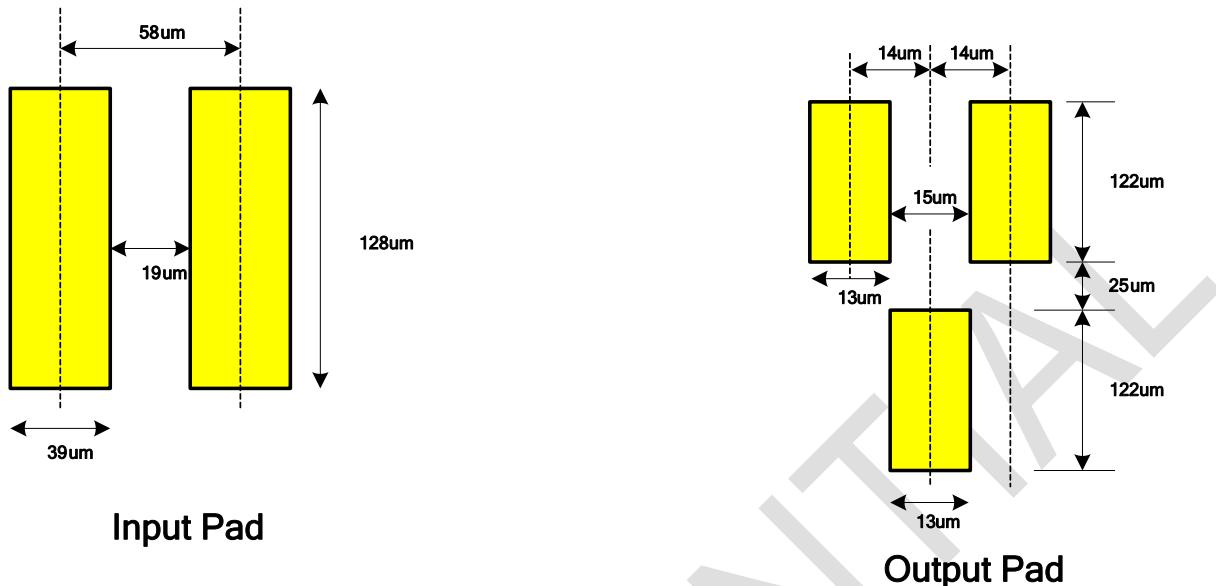
**RM69030
FACE UP**

Chip size: 27150um x 1720um
Chip thickness: 400um
Au bump height: 15um
Au bump input size: 39um x 128um
Au buamo output size: 13um x 122um



Alignment Mark:



Bump Arrangement:

Coordinate:

BUMP location	X-axis	Y-axis
VSSIDUM0	-13427	-745
PADA1	-13340	-745
PADA2	-13282	-745
PADA5	-13224	-745
PADA6	-13166	-745
PADA7	-13108	-745
DUMY0	-13050	-745
DUMY1	-12992	-745
DUMY2	-12934	-745
DUMY3	-12876	-745
TESTH_1	-12818	-745
TESTH_2	-12760	-745
TESTH_3	-12702	-745
TESTH_4	-12644	-745
TEST15	-12586	-745
TEST14	-12528	-745
TEST13	-12470	-745
TEST12	-12412	-745
TEST11	-12354	-745
TEST10	-12296	-745
TEST9	-12238	-745
TEST8	-12180	-745
TEST7	-12122	-745
D3_P1	-12064	-745
D3_P1	-12006	-745
D3_P2	-11948	-745
D3_P2	-11890	-745
TEST6	-11832	-745
VSS3D	-11774	-745
VSS3D	-11716	-745
BVP3D	-11658	-745
BVP3D	-11600	-745
BVN3D	-11542	-745
BVN3D	-11484	-745
MTP_PWR	-11426	-745
MTP_PWR	-11368	-745
VGL	-11310	-745
VGL	-11252	-745

VGL	-11194	-745
VGLR	-11136	-745
VGLR	-11078	-745
VGLR	-11020	-745
VGHR	-10962	-745
VGHR	-10904	-745
VCL	-10846	-745
VCL	-10788	-745
VCL	-10730	-745
VCL	-10672	-745
VCL	-10614	-745
VCL	-10556	-745
VREF	-10498	-745
VREF	-10440	-745
VSSA	-10382	-745
VSSA	-10324	-745
VSSA	-10266	-745
VSSA	-10208	-745
VDDA	-10150	-745
VDDA	-10092	-745
VDDA	-10034	-745
VDDA	-9976	-745
VDDR	-9918	-745
VDDR	-9860	-745
VSSR	-9802	-745
VSSR	-9744	-745
VDD_DET	-9686	-745
DIOPWR	-9628	-745
DIOPWR	-9570	-745
VGSP	-9512	-745
VGSP	-9454	-745
VGMP	-9396	-745
VGMP	-9338	-745
DVSS	-9280	-745
DVSS	-9222	-745
DVSS	-9164	-745
DVSS	-9106	-745
DVDD	-9048	-745
DVDD	-8990	-745
DVDD	-8932	-745
DVDD	-8874	-745

AVSS	-8816	-745
AVSS	-8758	-745
AVSS	-8700	-745
AVSS	-8642	-745
VDDI_OPT1	-8584	-745
LANSEL0	-8526	-745
LANSEL1	-8468	-745
DSWAP0	-8410	-745
DSWAP1	-8352	-745
PSWAP	-8294	-745
DSTB_SEL	-8236	-745
I2C_SA0	-8178	-745
IM3	-8120	-745
IM2	-8062	-745
IM1	-8004	-745
IM0	-7946	-745
SWIRE	-7888	-745
OLED_EN	-7830	-745
GPO1	-7772	-745
GPO0	-7714	-745
EXB1T	-7656	-745
TE_L	-7598	-745
VSEL	-7540	-745
SDO	-7482	-745
SDI	-7424	-745
DCX	-7366	-745
WRX	-7308	-745
RDX	-7250	-745
CSX	-7192	-745
RESX	-7134	-745
VSSI	-7076	-745
VSSI	-7018	-745
VSSI	-6960	-745
VDDI	-6902	-745
VDDI	-6844	-745
VDDI	-6786	-745
SCL_M	-6728	-745
SDA_M	-6670	-745
TEST5	-6612	-745
MUX13	-6554	-745
VSSI_OPT1	-6496	-745

PMOS0	-6438	-745
PMOS1	-6380	-745
CGM2	-6322	-745
CGM1	-6264	-745
CGM0	-6206	-745
VDDI_OPT2	-6148	-745
D23	-6090	-745
D22	-6032	-745
D21	-5974	-745
D20	-5916	-745
D19	-5858	-745
D18	-5800	-745
D17	-5742	-745
D16	-5684	-745
D15	-5626	-745
D14	-5568	-745
D13	-5510	-745
D12	-5452	-745
D11	-5394	-745
D10	-5336	-745
D9	-5278	-745
D8	-5220	-745
D7	-5162	-745
D6	-5104	-745
D5	-5046	-745
D4	-4988	-745
D3	-4930	-745
D2	-4872	-745
D1	-4814	-745
D0	-4756	-745
DE	-4698	-745
PCLK	-4640	-745
HS	-4582	-745
VS	-4524	-745
TEST4	-4466	-745
TEST3	-4408	-745
ERR	-4350	-745
VDDI	-4292	-745
VDDI	-4234	-745
VDDI	-4176	-745
VSSI	-4118	-745

VSSI	-4060	-745
VSSI	-4002	-745
VDDA	-3944	-745
VDDA	-3886	-745
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S1523	-10206	596.5	S1564	-10780	743.5
S1524	-10220	743.5	S1565	-10794	596.5
S1525	-10234	596.5	S1566	-10808	743.5
S1526	-10248	743.5	S1567	-10822	596.5
S1527	-10262	596.5	S1568	-10836	743.5
S1528	-10276	743.5	S1569	-10850	596.5
S1529	-10290	596.5	S1570	-10864	743.5
S1530	-10304	743.5	S1571	-10878	596.5
S1531	-10318	596.5	S1572	-10892	743.5
S1532	-10332	743.5	S1573	-10906	596.5
S1533	-10346	596.5	S1574	-10920	743.5
S1534	-10360	743.5	S1575	-10934	596.5
S1535	-10374	596.5	S1576	-10948	743.5
S1536	-10388	743.5	S1577	-10962	596.5
S1537	-10402	596.5	S1578	-10976	743.5
S1538	-10416	743.5	S1579	-10990	596.5
S1539	-10430	596.5	S1580	-11004	743.5
S1540	-10444	743.5	S1581	-11018	596.5
S1541	-10458	596.5	S1582	-11032	743.5
S1542	-10472	743.5	S1583	-11046	596.5
S1543	-10486	596.5	S1584	-11060	743.5
S1544	-10500	743.5	S1585	-11074	596.5
S1545	-10514	596.5	S1586	-11088	743.5
S1546	-10528	743.5	S1587	-11102	596.5
S1547	-10542	596.5	S1588	-11116	743.5
S1548	-10556	743.5	S1589	-11130	596.5
S1549	-10570	596.5	S1590	-11144	743.5

S1591	-11158	596.5
S1592	-11172	743.5
S1593	-11186	596.5
S1594	-11200	743.5
S1595	-11214	596.5
S1596	-11228	743.5
S1597	-11242	596.5
S1598	-11256	743.5
S1599	-11270	596.5
S1600	-11284	743.5
S1601	-11298	596.5
S1602	-11312	743.5
S1603	-11326	596.5
S1604	-11340	743.5
S1605	-11354	596.5
S1606	-11368	743.5
S1607	-11382	596.5
S1608	-11396	743.5
S1609	-11410	596.5
S1610	-11424	743.5
S1611	-11438	596.5
S1612	-11452	743.5
S1613	-11466	596.5
S1614	-11480	743.5
S1615	-11494	596.5
S1616	-11508	743.5
S1617	-11522	596.5
S1618	-11536	743.5
S1619	-11550	596.5
S1620	-11564	743.5
SDUM2	-11578	596.5
SDUM3	-11592	743.5
AVSS	-11606	596.5
AVSS	-11620	743.5
GDUM7	-11634	596.5
GDUM7	-11648	743.5
GOUTDUM36	-11662	596.5
GOUTDUM36	-11676	743.5
GDUM8	-11690	596.5
GDUM8	-11704	743.5
DUMY9	-11718	596.5

DUMY9	-11732	743.5
DUMY10	-11746	596.5
DUMY10	-11760	743.5
DUMY11	-11774	596.5
DUMY11	-11788	743.5
GDUM9	-11802	596.5
GDUM9	-11816	743.5
VGHR	-11830	596.5
VGHR	-11844	743.5
VGHR	-11858	596.5
VGHR	-11872	743.5
VGHR	-11886	596.5
VGHR	-11900	743.5
GDUM10	-11914	596.5
GDUM10	-11928	743.5
VGLR	-11942	596.5
VGLR	-11956	743.5
VGLR	-11970	596.5
VGLR	-11984	743.5
VGLR	-11998	596.5
VGLR	-12012	743.5
GDUM11	-12026	596.5
GDUM11	-12040	743.5
SW3_L	-12054	596.5
SW3_L	-12068	743.5
SW3_L	-12082	596.5
SW3_L	-12096	743.5
SW2_L	-12110	596.5
SW2_L	-12124	743.5
SW2_L	-12138	596.5
SW2_L	-12152	743.5
SW1_L	-12166	596.5
SW1_L	-12180	743.5
SW1_L	-12194	596.5
SW1_L	-12208	743.5
GOUTDUM43	-12222	596.5
GOUTDUM43	-12236	743.5
VREFN	-12250	596.5
VREFN	-12264	743.5
VREFN	-12278	596.5
VREFN	-12292	743.5

GOUTDUM46	-12306	596.5
GOUTDUM46	-12320	743.5
VREFP	-12334	596.5
VREFP	-12348	743.5
VREFP	-12362	596.5
VREFP	-12376	743.5
GOUTDUM49	-12390	596.5
GOUTDUM49	-12404	743.5
EN3_L	-12418	596.5
EN3_L	-12432	743.5
EN2_L	-12446	596.5
EN2_L	-12460	743.5
EN1_L	-12474	596.5
EN1_L	-12488	743.5
XON_L	-12502	596.5
XON_L	-12516	743.5
D2U_L	-12530	596.5
D2U_L	-12544	743.5
U2D_L	-12558	596.5
U2D_L	-12572	743.5
XVCK2_L	-12586	596.5
XVCK2_L	-12600	743.5
VCK2_L	-12614	596.5
VCK2_L	-12628	743.5
XVCK1_L	-12642	596.5
XVCK1_L	-12656	743.5
VCK1_L	-12670	596.5
VCK1_L	-12684	743.5
VST8_L	-12698	596.5
VST8_L	-12712	743.5
VST7_L	-12726	596.5
VST7_L	-12740	743.5
VST6_L	-12754	596.5
VST6_L	-12768	743.5
VST5_L	-12782	596.5
VST5_L	-12796	743.5
VST4_L	-12810	596.5
VST4_L	-12824	743.5
VST3_L	-12838	596.5
VST3_L	-12852	743.5
VST2_L	-12866	596.5

VST2_L	-12880	743.5
VST1_L	-12894	596.5
VST1_L	-12908	743.5
GOUTDUM68	-12922	596.5
GOUTDUM68	-12936	743.5
VGLR	-12950	596.5
VGLR	-12964	743.5
VGLR	-12978	596.5
VGLR	-12992	743.5
VGLR	-13006	596.5
VGLR	-13020	743.5
VGLR	-13034	596.5
VGLR	-13048	743.5
GDUM12	-13062	596.5
GDUM12	-13076	743.5
VGHR	-13090	596.5
VGHR	-13104	743.5
VGHR	-13118	596.5
VGHR	-13132	743.5
GOUTDUM69	-13146	596.5
GOUTDUM69	-13160	743.5
GOUTDUM70	-13174	596.5
GOUTDUM70	-13188	743.5
VGHR	-13202	596.5
VGHR	-13216	743.5
VGHR	-13230	596.5
VGHR	-13244	743.5
PADA4	-13258	596.5
PADA3	-13272	743.5
AVSSDUM36	-13300	743.5
AVSSDUM36	-13314	596.5
AVSSDUM35	-13286	596.5
ALIGN1	-13405	730
ALIGN2	13405	730

6. Block Function Description

Interface

The RM69032 incorporates command method 24-/16-/8-bits bus display command interface. WDR stores data to be written into GRAM or parameters temporarily while RDR stores data read out from GRAM temporarily. When data is written from microcomputer to GRAM, the RM69032 writes firstly to WDR, and then the data is written to GRAM automatically by internal operation. Because read out operation from GRAM is conducted through RDR, first read out data is invalid. Normal data is read out from 2nd read out data.

Address Counter (AC)

Address counter (AC) gives address to GRAM. When command setting address is written to CR, the data is transferred from CR to AC.

When data is written to GRAM, address counter (AC) increments by +1 or -1 automatically. AC after data is read out increments by +1 or -1 likewise. The RM69032 writes data to only rectangular area that was specified by GRAM.

Graphic RAM (GRAM)

The graphic RAM (GRAM) stores 1,555,200 bytes pattern data using 24 bits for one pixel, enabling maximum 540RGB x 960 dot graphic display.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a drive voltage, which corresponds to grayscale level set in the y correction register. The RM69032 displays 16.7M colors at the maximum.

Power Supply Circuit

The power supply circuit generates supply voltages to LTPS AMOLED panel, VREG1OUT, VGH,VGL.

Timing Generating

The timing generator generates timing signals for internal circuits such as the internal GRAM. The timing for display operation such as RAM read operation and the timing for internal operation such as RAM access by MPU is outputted separately so that they do not interfere with each other.

Oscillator

The RM69032 incorporates RC oscillator circuit. The frame frequency is changeable by command settings.

Panel Driver Circuit

The LTPS AMOLED display driver circuit consists of 1620 source drivers (S1~S1620). Display pattern data is latched when 1620 data is input. This latched data controls source drivers and outputs drive waveform. The shift direction of 1620-dot output from the source driver can be changed by setting commands. The gate signal is controlled by VSR timing .

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7. Function Description

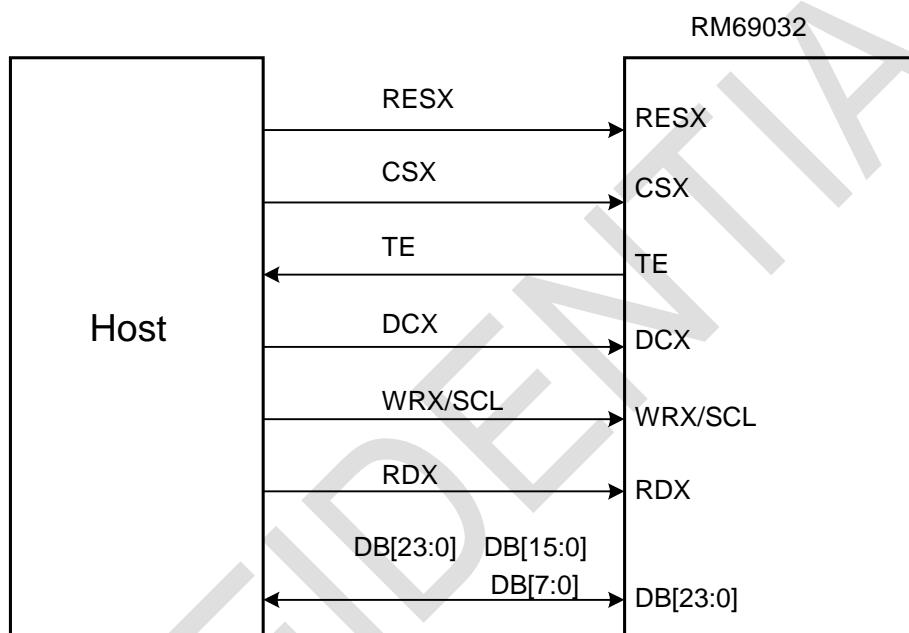
7.1 Interface Type Selection

The selection of a given interfaces are done by setting IM3, IM2, IM1 and IM0 pins as show below.

IM[3:0]	Display Data	Command
0000	80-series 8-bit MPU I/F, D[7:0]	80-series 8-bit MPU I/F, D[7:0]
0001	80-series 16-bit MPU I/F, D[15:0]	80-series 16-bit MPU I/F, D[15:0]
0010	80-series 24-bit MPU I/F, D[23:0]	80-series 24-bit MPU I/F, D[23:0]
0011	RGB I/F, D[23:0]	16-bit SPI (SCL rising edge trigger), SDI/SDO
1011	RGB I/F, D[23:0]	16-bit SPI (SCL falling edge trigger), SDI/SDO
0100	MIPI DSI,	MIPI DSI
0101	MDDI,	MDDI, 16-bit SPI (SCL rising edge trigger), SDI/SDO
0110	MDDI,	MDDI, 16-bit SPI (SCL falling edge trigger), SDI/SDO
1110	MDDI,	MDDI, I2C I/F, I2C_SDA serial data
0111	RGB I/F, D[23:0]	I2C I/F, I2C_SDA

7.2 Display Bus Interface (DBI)

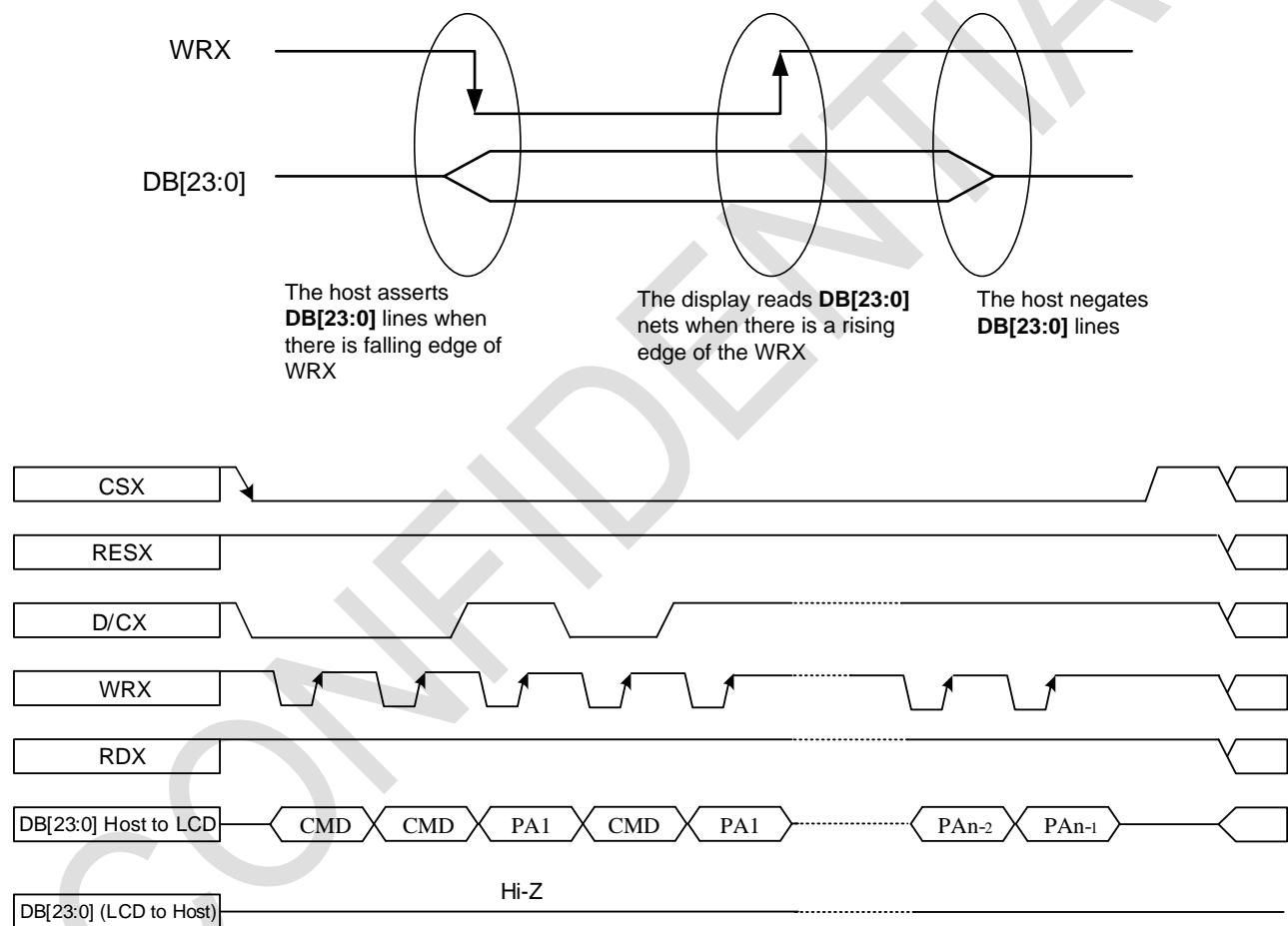
The RM69032 uses a 28-wires 24-bit parallel interface. The chip-select CSX (active low) enables and disables the DBI interface. RESX (active low) is an external reset signal. WRX is the data write, RDX is the data read and DB[23:0] is parallel DBI data. There are three 24/16/8-bit types interface supported for the display data transfer. The graphics controller chip reads the data at the rising edge of RDX signal. The DCX is data/command flag. When DCX = "1", D23 to D0 bits are display RAM data or command parameters. When DCX = "0", D7 to D0 bits are commands.



7.2.1 Write Cycle

During a write cycle the host processor sends data to the display module via the interface. The Type B interface utilizes DCX, RDX and WRX signals as well as all information signals (DB[23:0]). WRX is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of WRX. DCX is driven low while command information is on the interface and is pulled high when data is present.

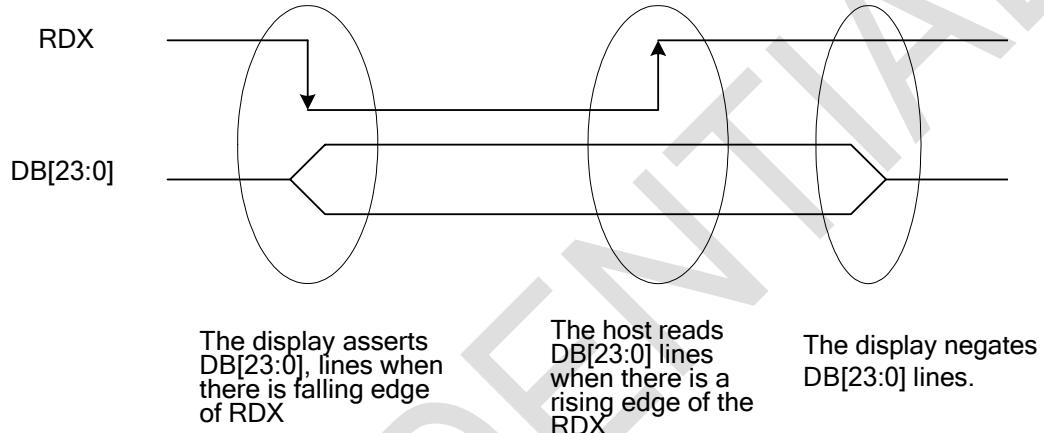
The following figure shows a write cycle for the type B interface.



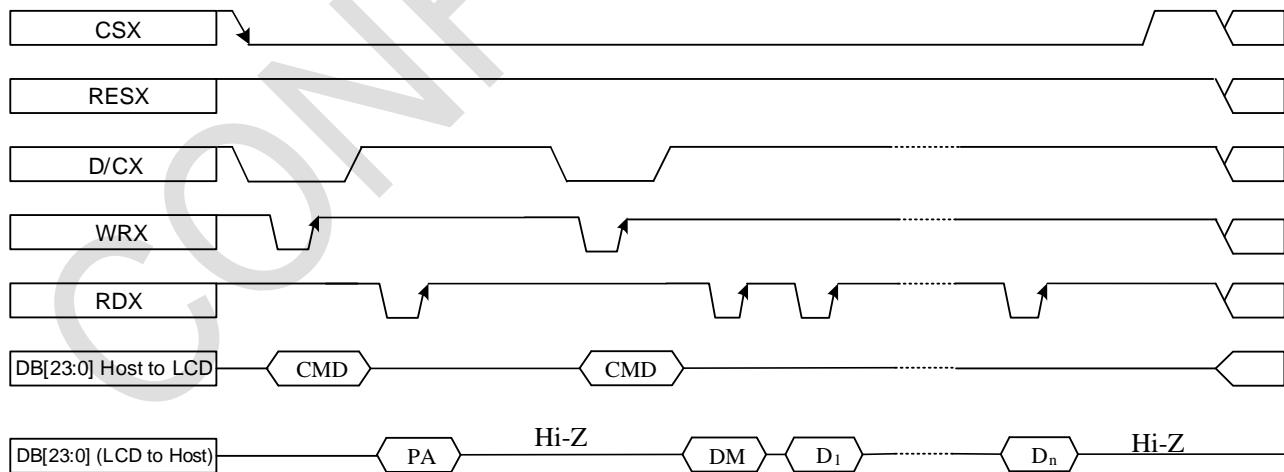
7.2.2 Read Cycle

During a read cycle the host processor reads data from the display module via the interface. The Type B interface utilizes DCX, RDX and WRX signals as well as all information signals (D[23:0]). RDX is driven from high to low then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX. DCX is driven high during the read cycle.

The following figure shows the read cycle for the type B interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read Data is only valid when the DCX input is pulled high. If DCX is driven low during read then the display information outputs will be High-Z.

DBI Type B Interface

24-bit data bus DB[23:0] interface, IM[3:0] = 0010
IFPF[3:0]: command_3A[3:0]

	IFPF	DB 23	DB 22	DB 21	DB 20	DB 19	DB 18	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Command Write	*	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command Read	*	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	IFPF	DB 23	DB 22	DB 21	DB 20	DB 19	DB 18	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	color	
Memory Write	5	/	/	/	/	/	/	/	/	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	65K	
	6	/	/	/	/	/	/	/	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	262K
	7	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	16.7M	

The read data for RGB is 24 bit output as below.

	DB 23	DB 22	DB 21	DB 20	DB 19	DB 18	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	color
Memory Read	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	16.7M

16-bit data bus DB[15:0] interface, IM[3:0] = 0001

	IFPF	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Command Write	*	/	/	/	/	/	/	/	/	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command Read	*	/	/	/	/	/	/	/	/	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	IFPF	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	color
Memory Write	5	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	65K
	6	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	X	X	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	X	X	262K
		B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	X	X	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	X	X	
		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	X	X	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	X	X	
7		R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	16.7M
		B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	
		G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	

The read data for RGB is 16 bit output as below.

	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	color
Memory Read	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	16.7M
	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	/	/	/	/	/	/	/	/	

8-bit data bus DB[7:0] interface, IM[3:0] = 0000

	IFPF	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Command Write	*	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command Read	*	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	IFPF	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	color
Memory Write	5	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	65K
		G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	
	6	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	X	X	262K
		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	X	X	
		B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	X	X	
	7	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	16.7M
		G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	
		B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	

The read data for RGB is 8 bit output as below.

	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	color
Memory Read	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	16.7M
	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	
	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	

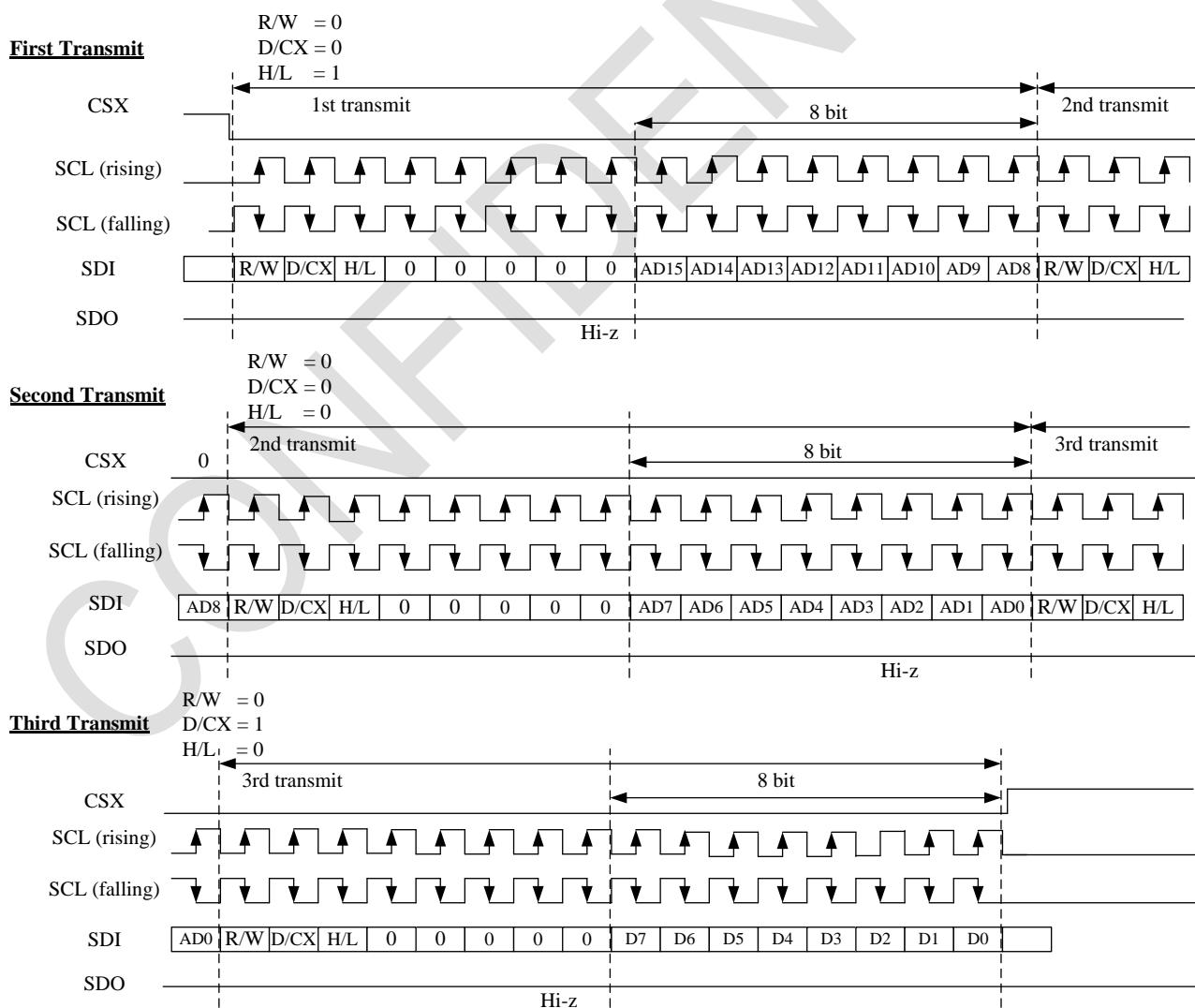
7.3 Serial Interface

7.3.1 Write Cycle and Sequence

During a write cycle the host processor sends a single bit of data to the display module via the interface. The SPI interface utilizes CSX, SCL and SDI and SDO signals. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

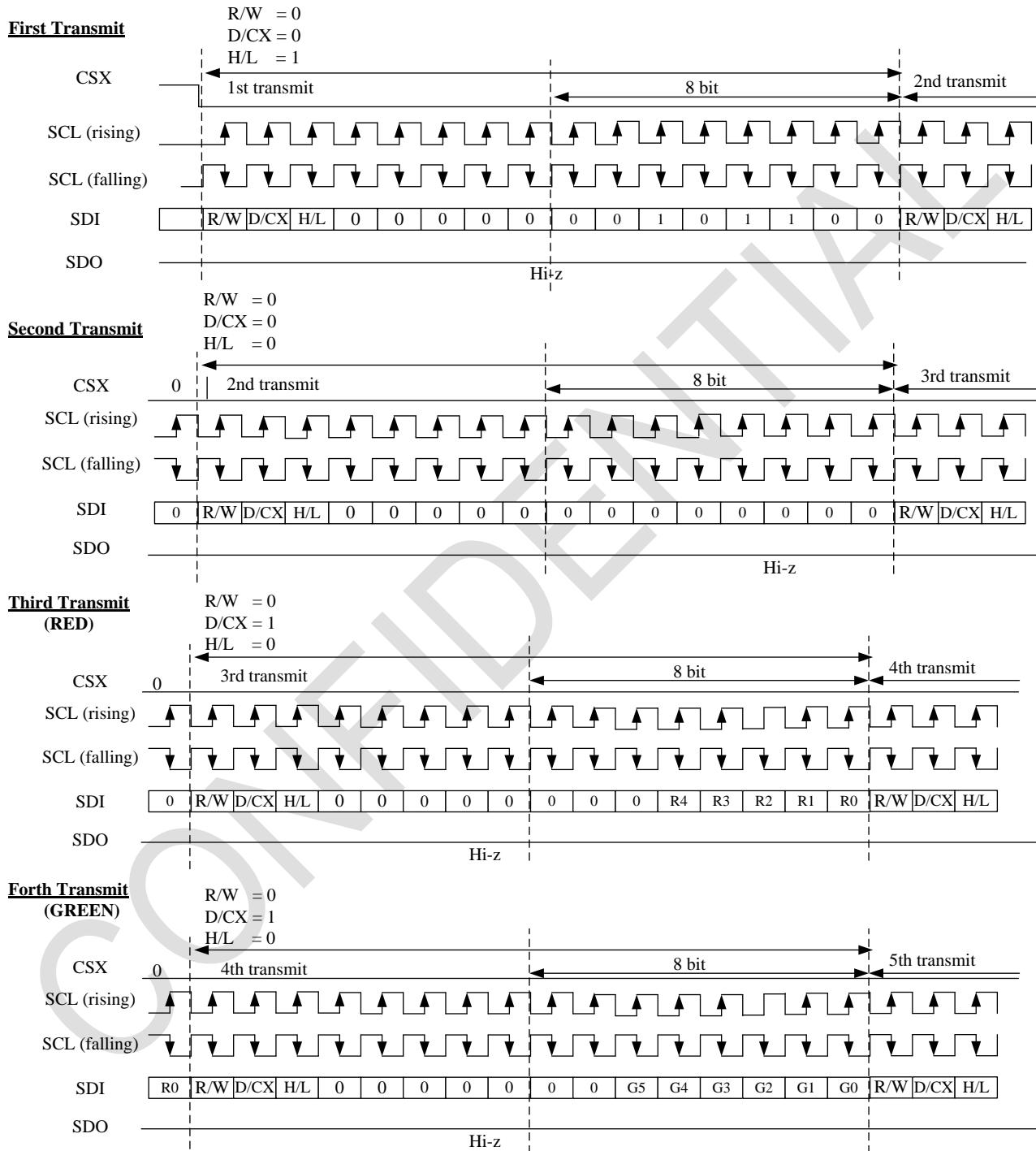
During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional DCX signal is used a byte is eight write cycles long. DCX is driven low while command information is on the interface and is pulled high when data is present.

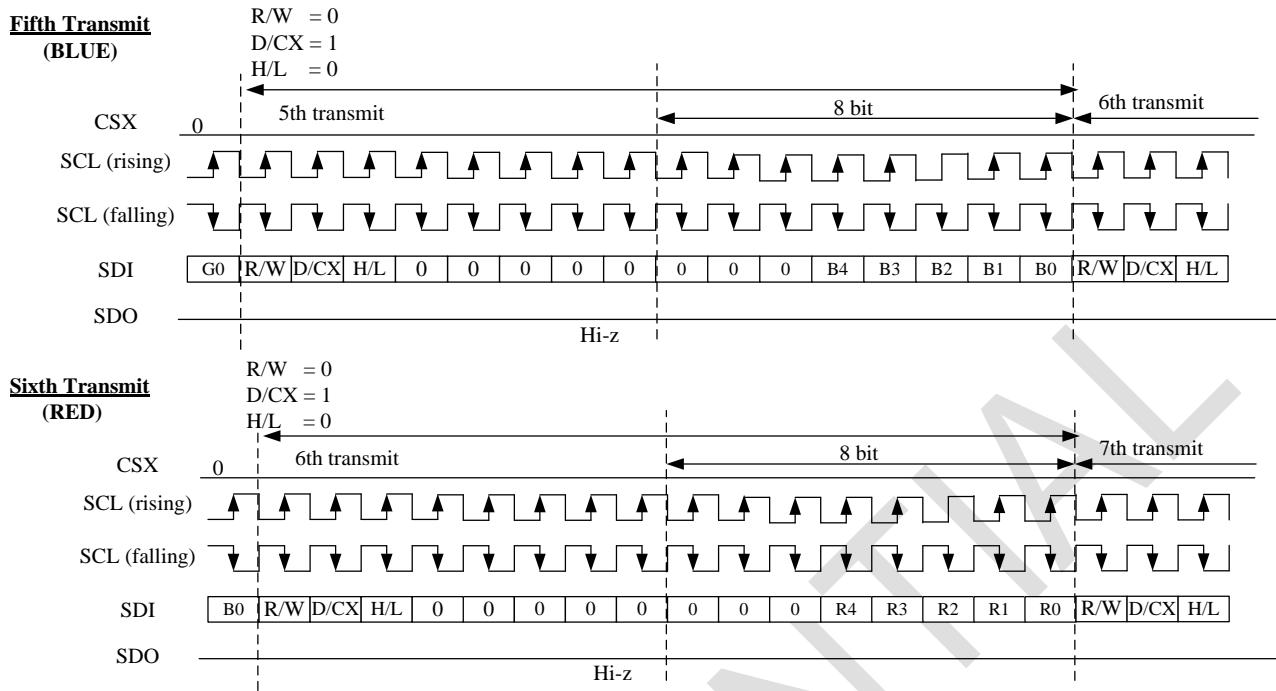
The SPI interface write command sequences are described in the following figure.



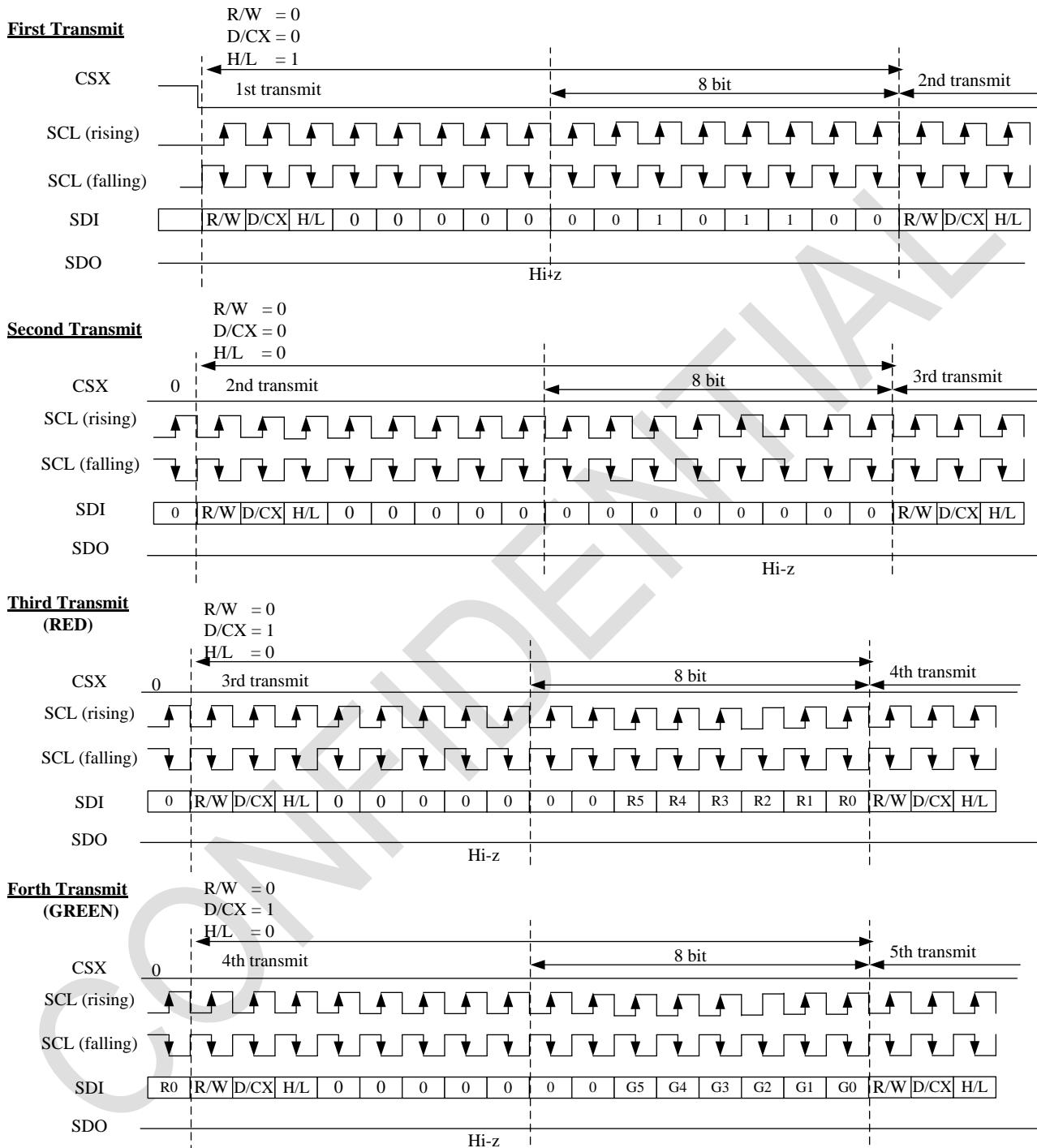
The SPI interface write data sequences are described in the following figure.

SRAM write: 65K colors, RGB 5-6-5 pixel data input (parameter of command 3A00h is 0x0005)

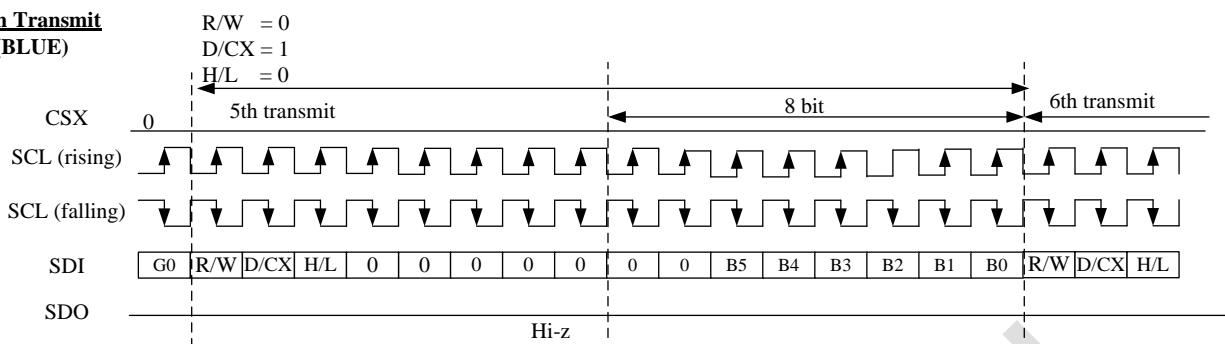




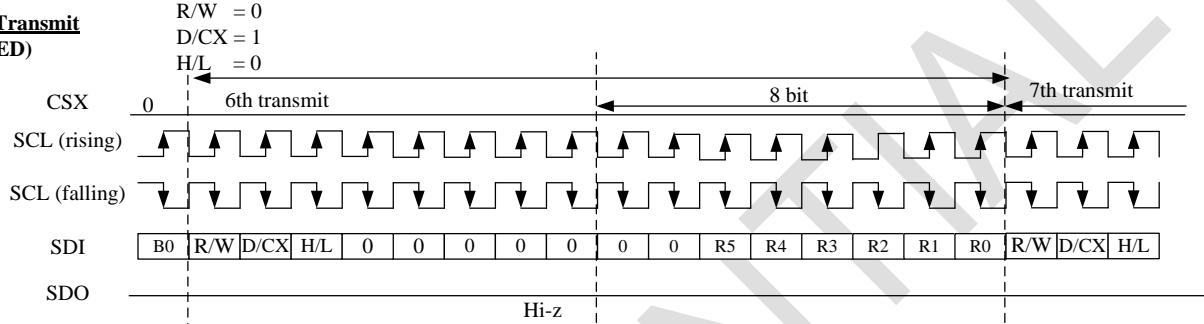
SRAM write: 262K colors, RGB 6-6-6 pixel data input (parameter of command 3A00h is 0x0006)



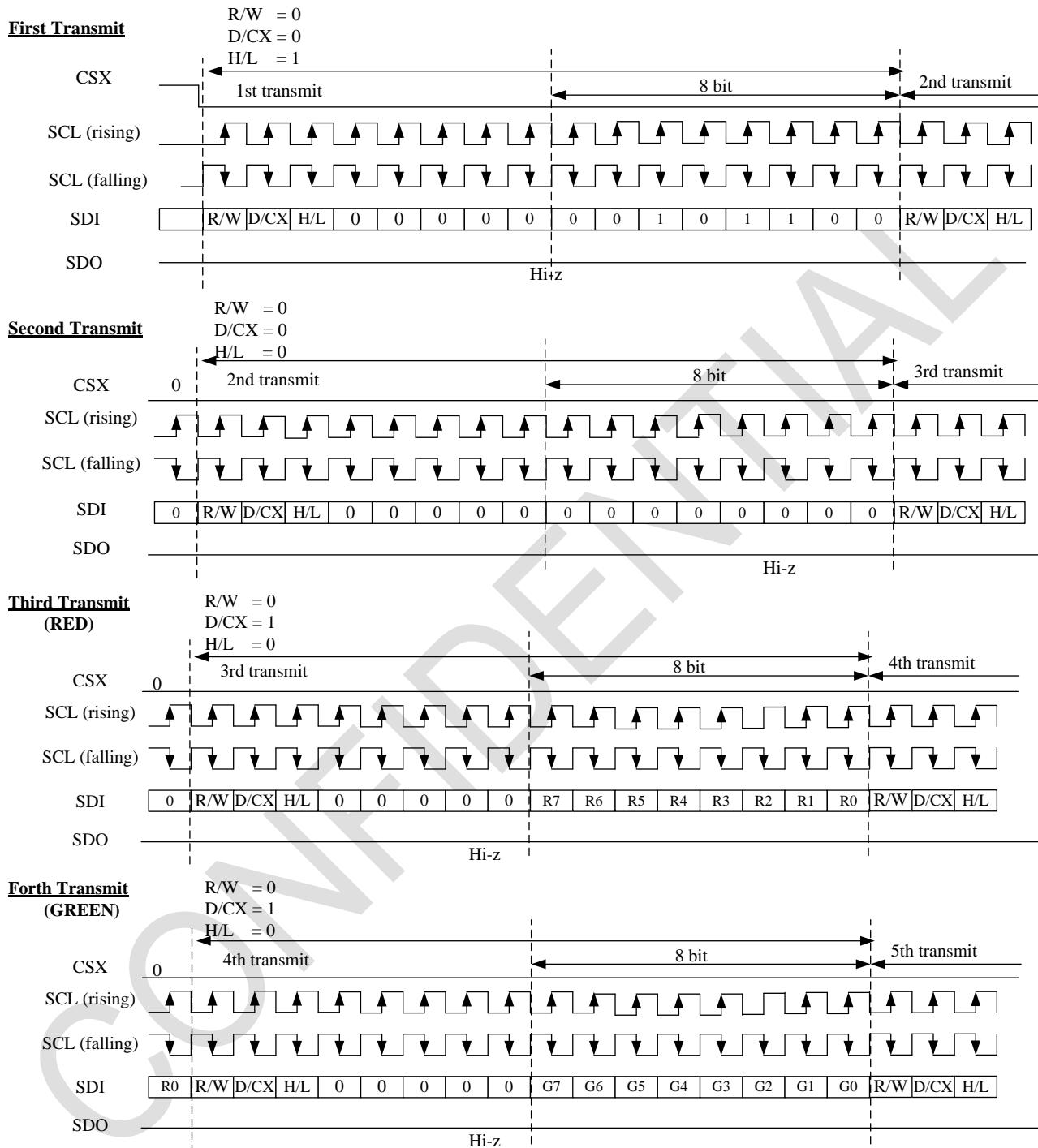
**Fifth Transmit
(BLUE)**

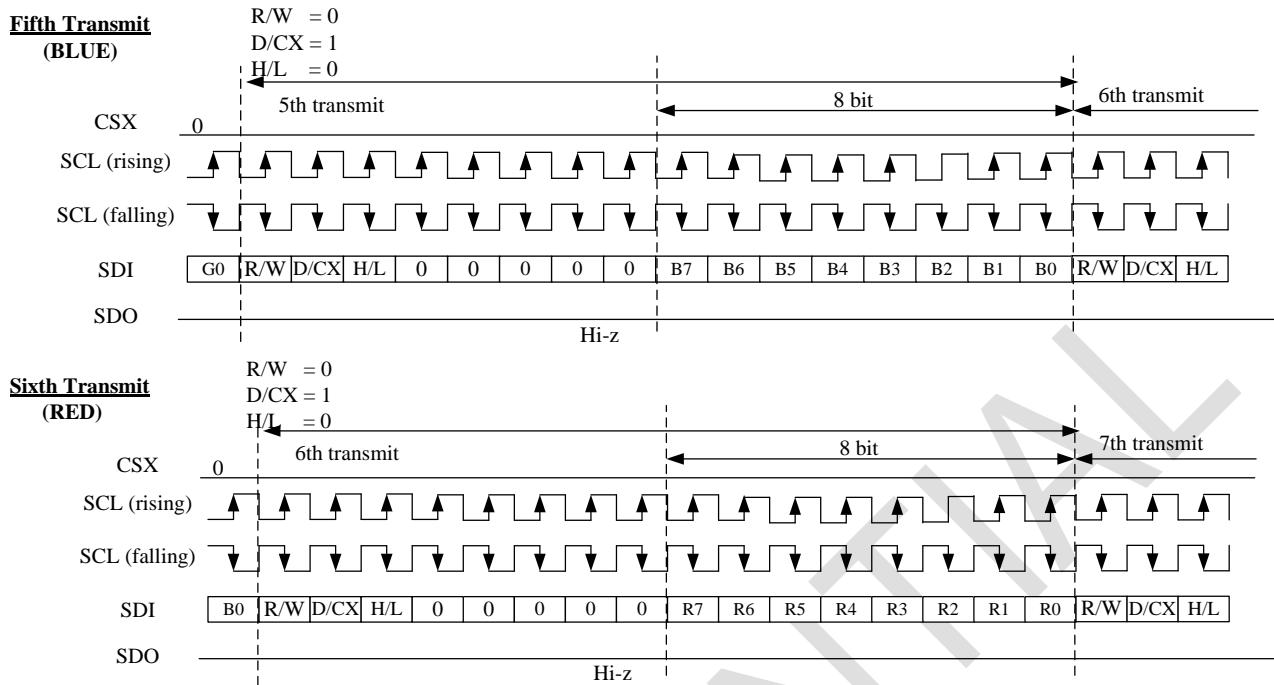


**Sixth Transmit
(RED)**



SRAM write: 16.7K colors, RGB 8-8-8 pixel data input (parameter of command 3A00h is 0x0007)



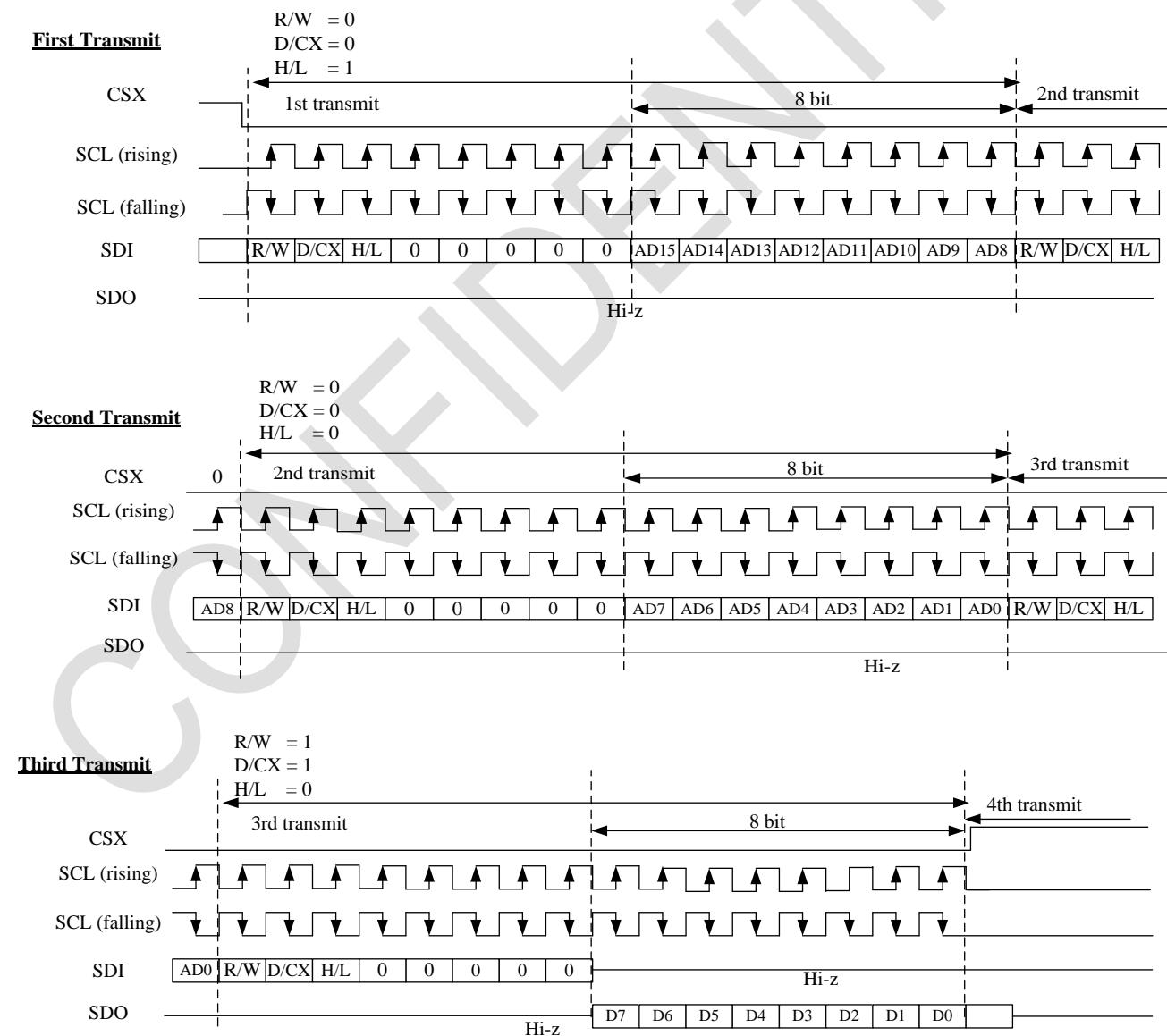


7.3.2 Read Cycle and Sequence

During a read cycle the host processor reads a single bit of data from the display module via the interface. The SPI interface utilizes CSX, SCL and DIN signals. SCL is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCL.

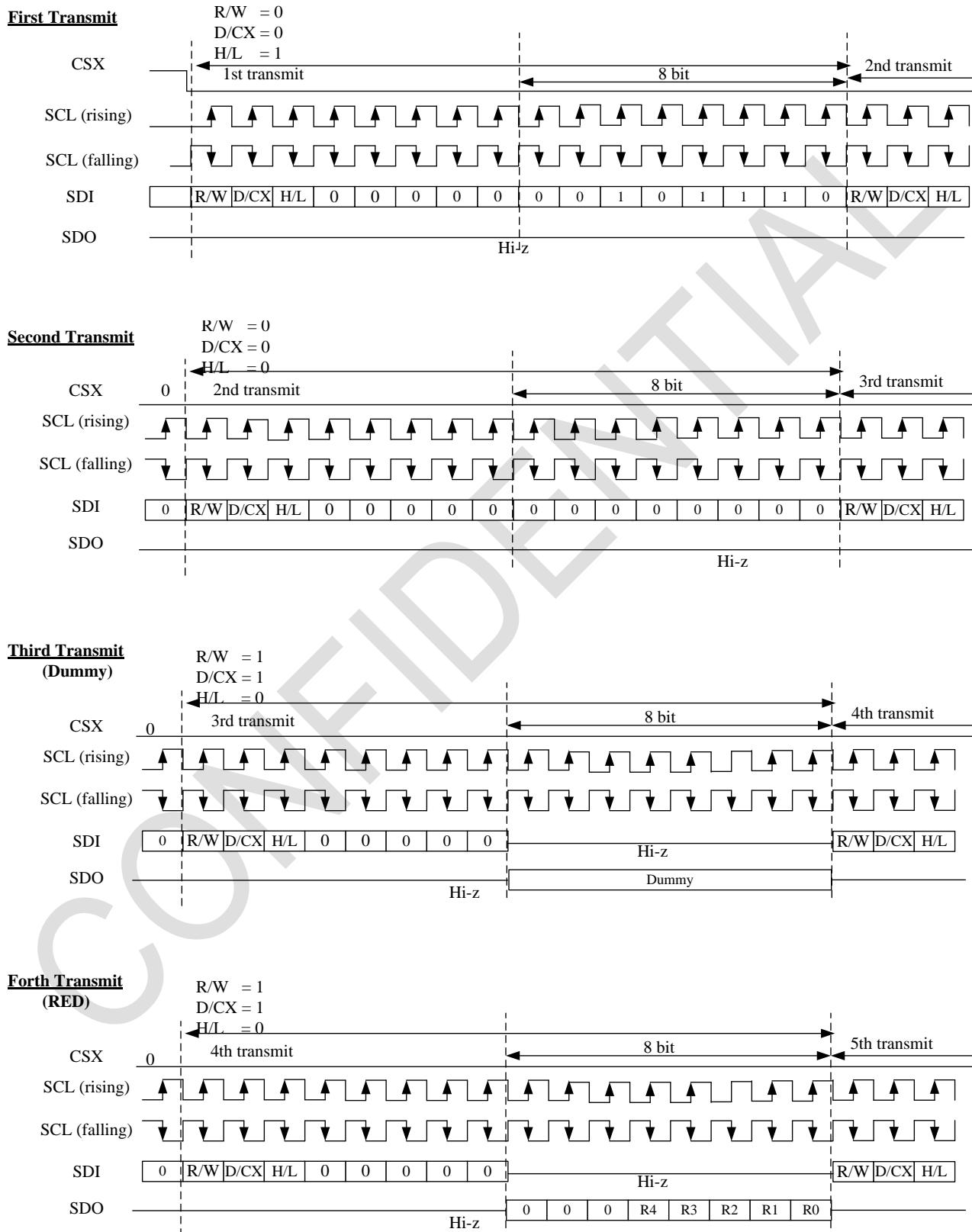
During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional DCX signal is used a byte is eight read cycles long. DCX is driven low while command information is on the interface and is pulled high when data is present.

The SPI interface read command sequences are described in the following figure.

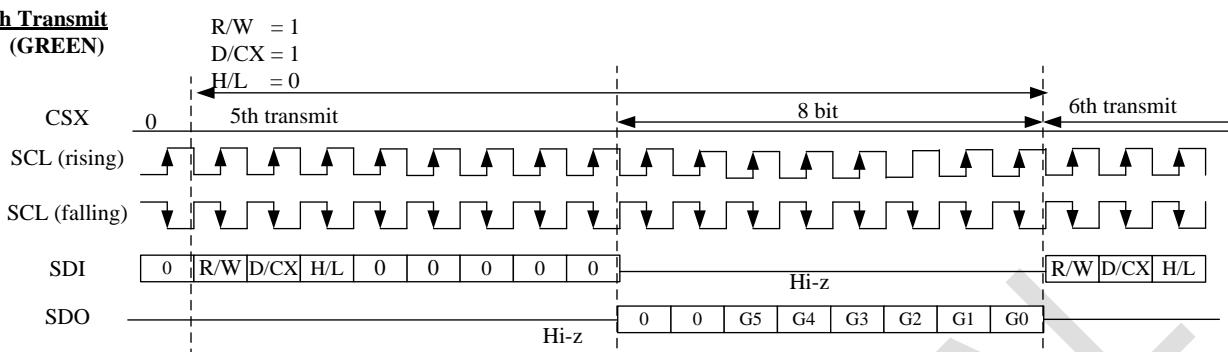


The SPI interface read data sequences are described in the following figure.

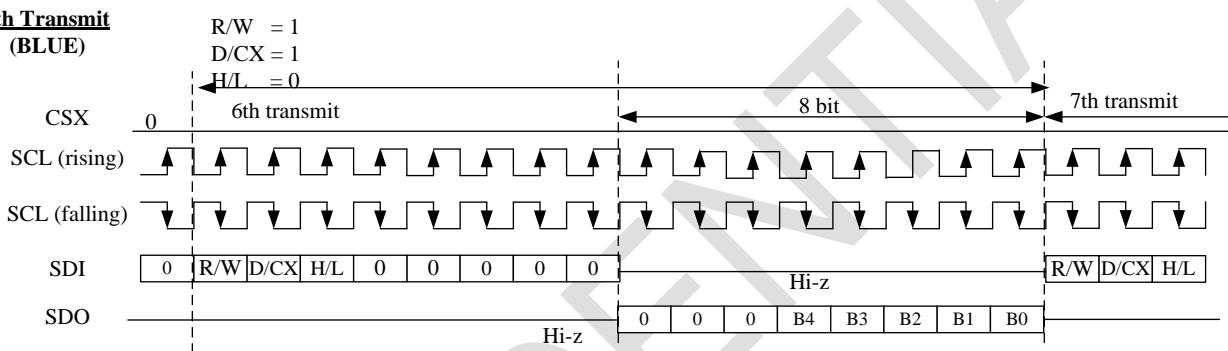
SRAM read: 65K colors, RGB 5-6-5 pixel data input (parameter of command 3A00h is 0x0005)



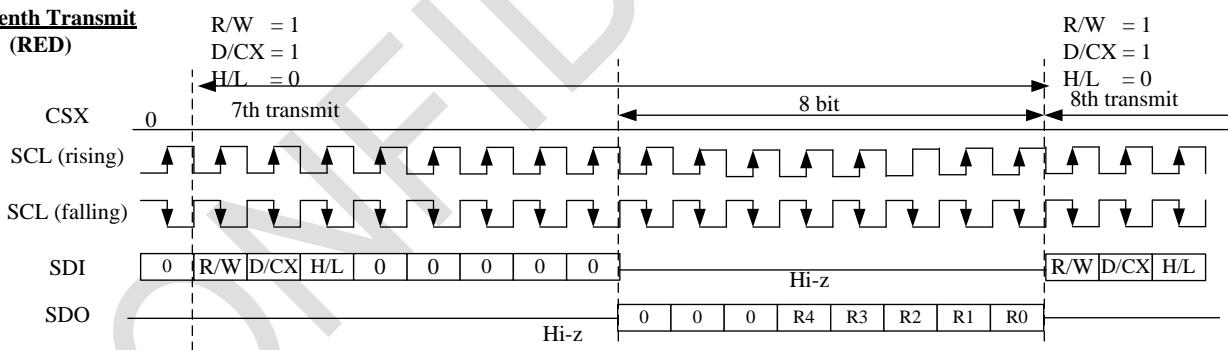
**Fifth Transmit
(GREEN)**



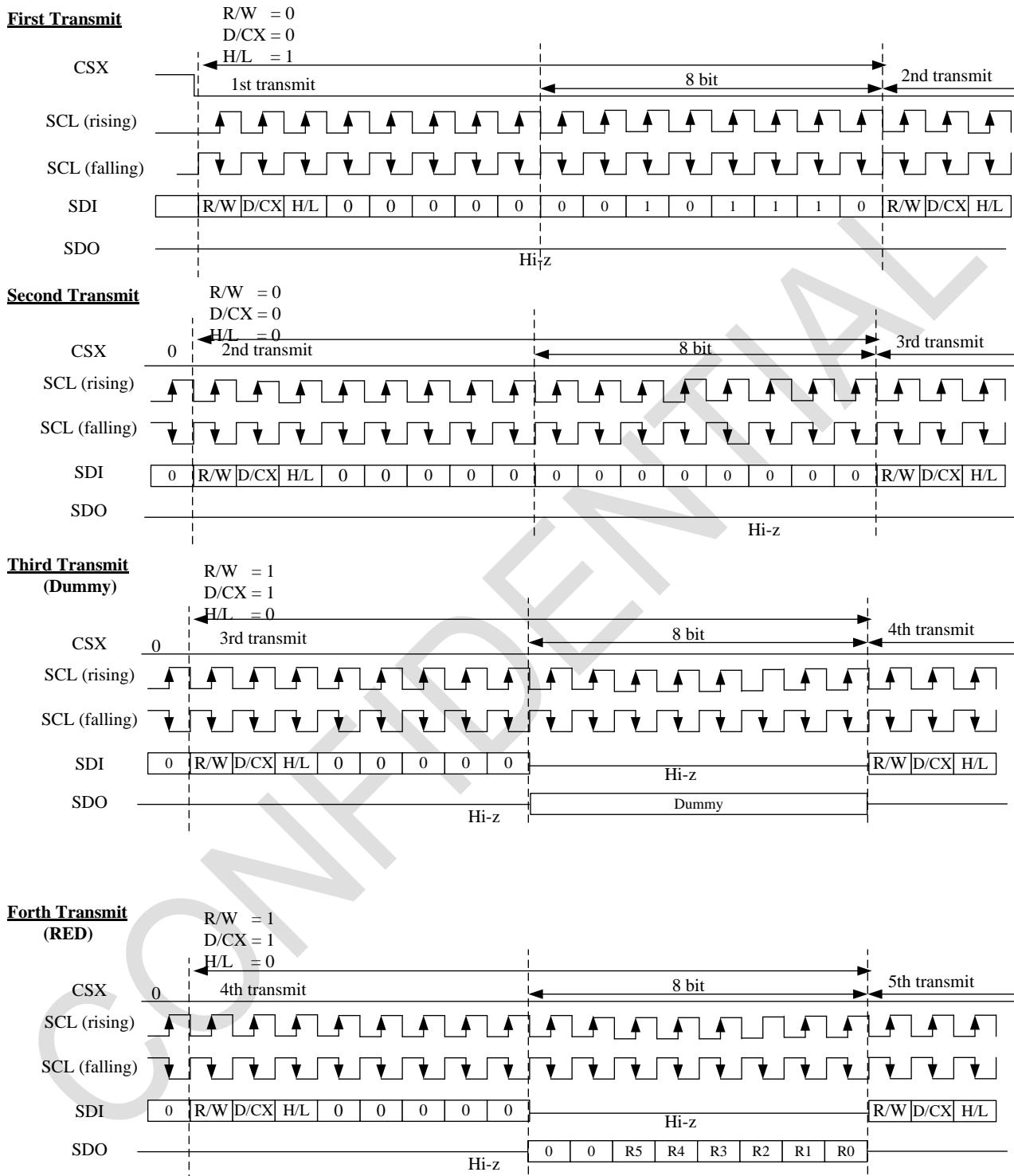
**Sixth Transmit
(BLUE)**

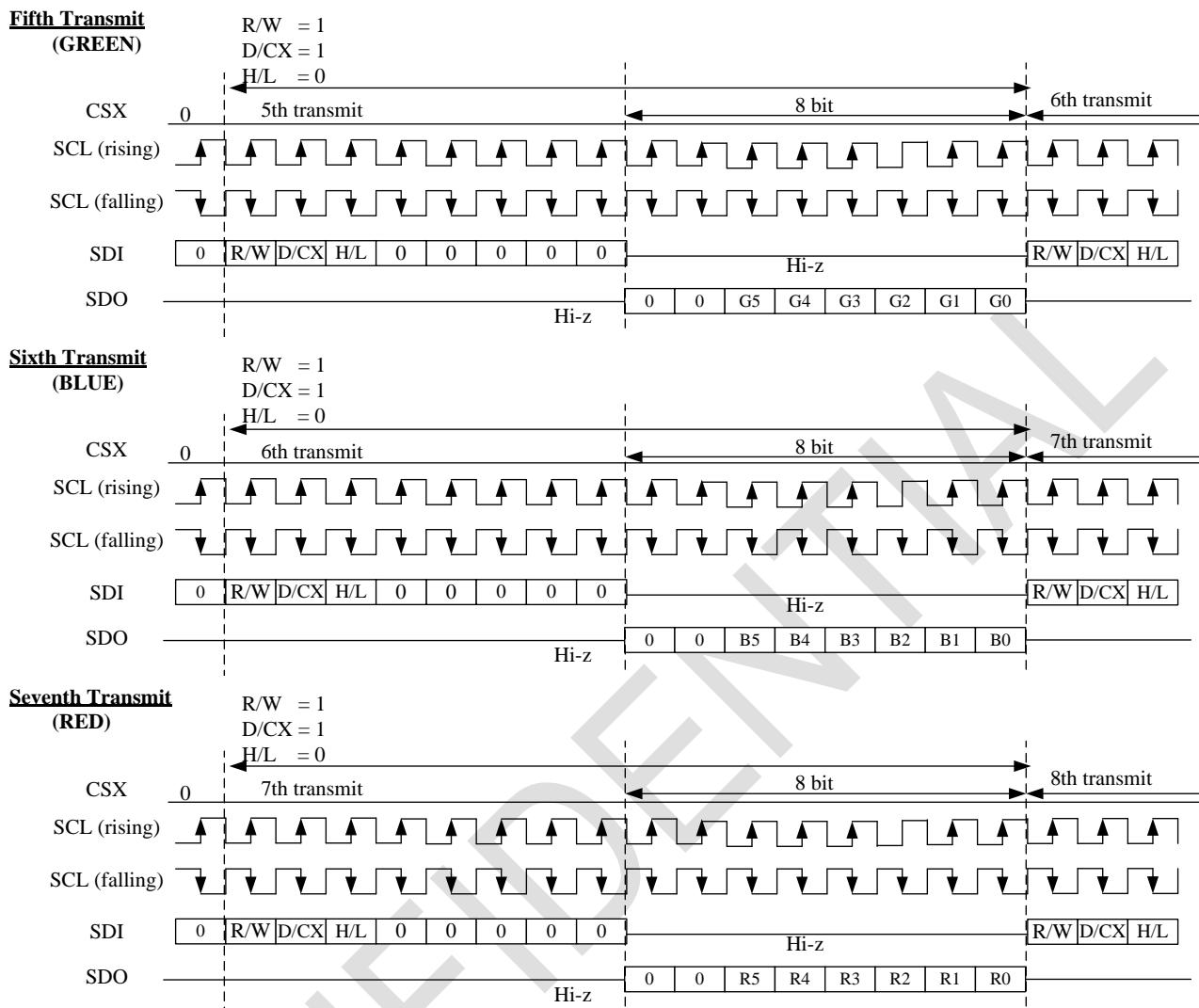


**Seventh Transmit
(RED)**

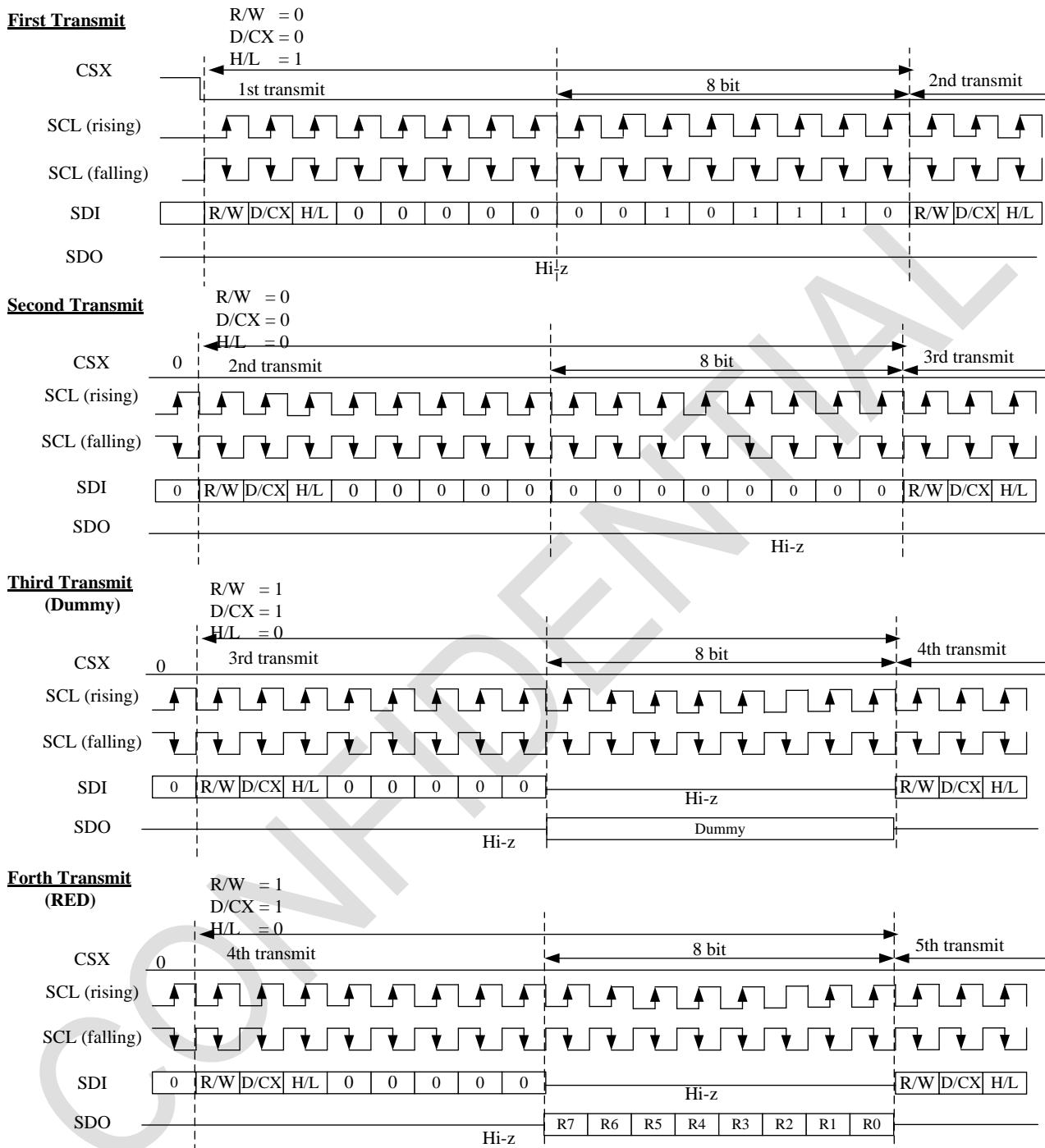


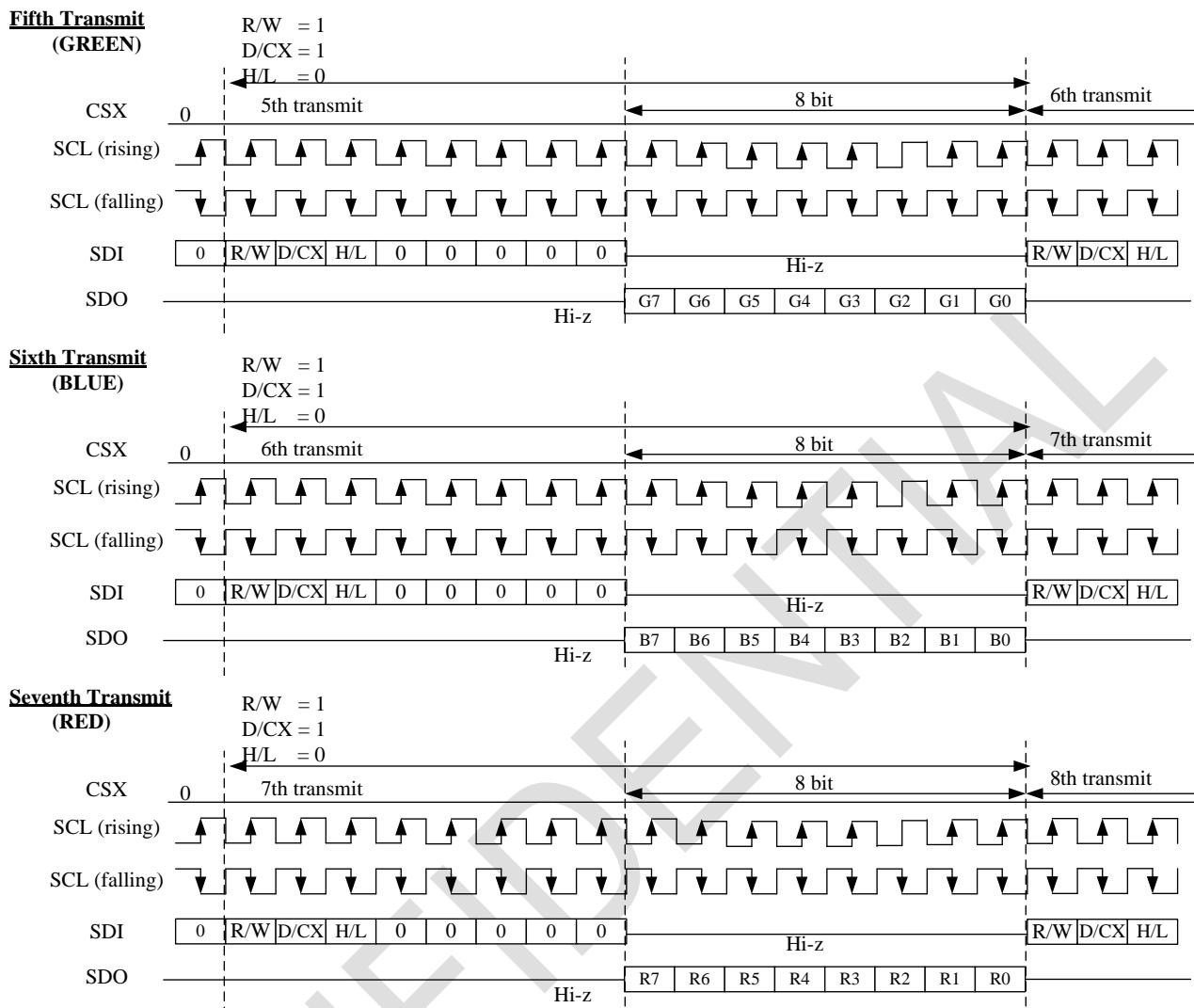
SRAM read: 262K colors, RGB 6-6-6 pixel data input (parameter of command 3A00h is 0x0006)





SRAM read: 16.7M colors, RGB 8-8-8 pixel data input (parameter of command 3A00h is 0x0007)



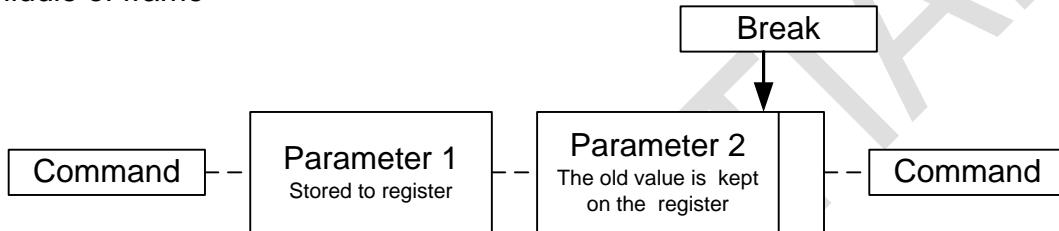


7.3.3 Break and Pause Sequences

The host processor can break a read or write sequence by pulling the CSX signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

The host processor can pause a read or write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.

1. Middle of frame

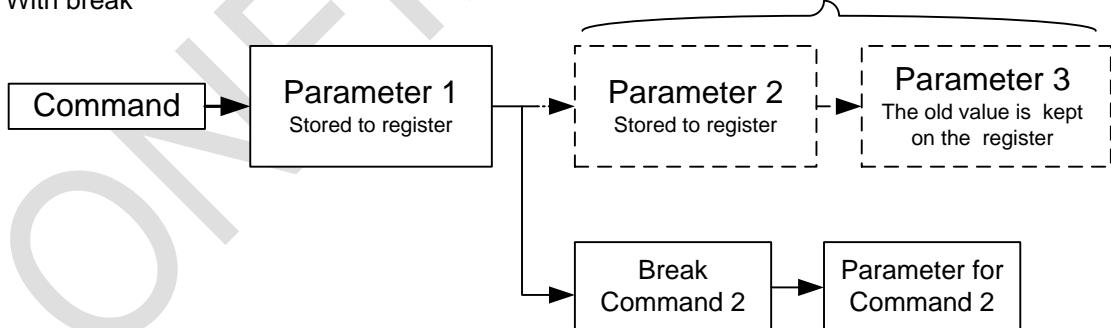


2. Between frames

Without break



With break



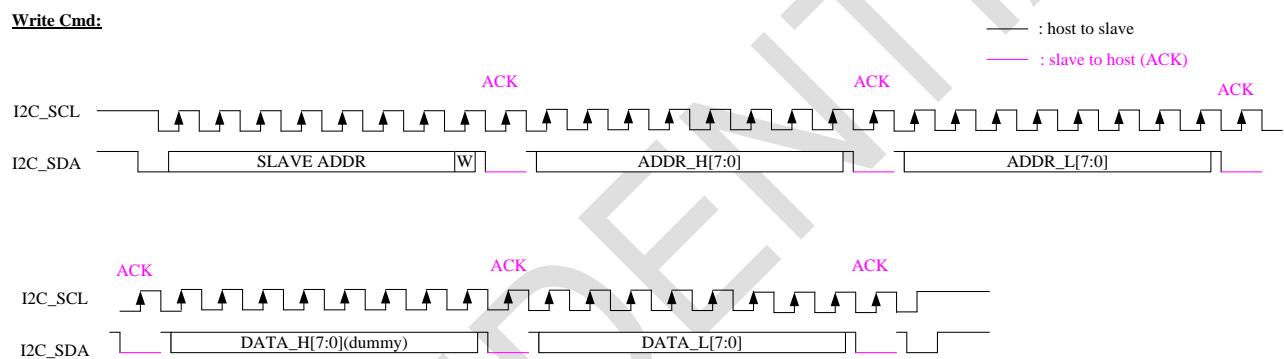
Break can be e.g. another command or noise pulse.

7.4 I2C Interface

The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data line (I2C_SDA) and the Serial Clock Line (I2C_SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledgement related clock pulse. A slave receiver which is addressed must generate an acknowledgement after the reception of each byte. Also a master receiver must generate an acknowledgement after the reception of each byte that has been clocked out of the slave transmitter.

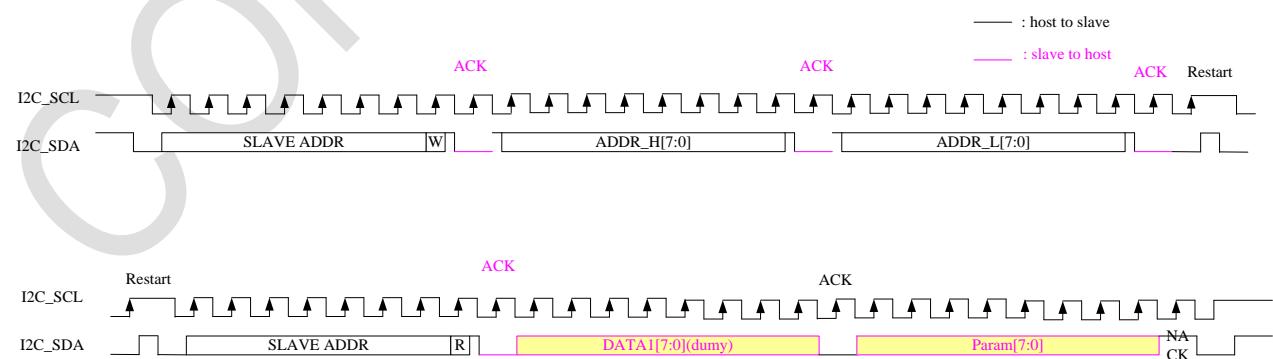
The I2C interface write command sequences are described in the following figure.

Write Cmd:



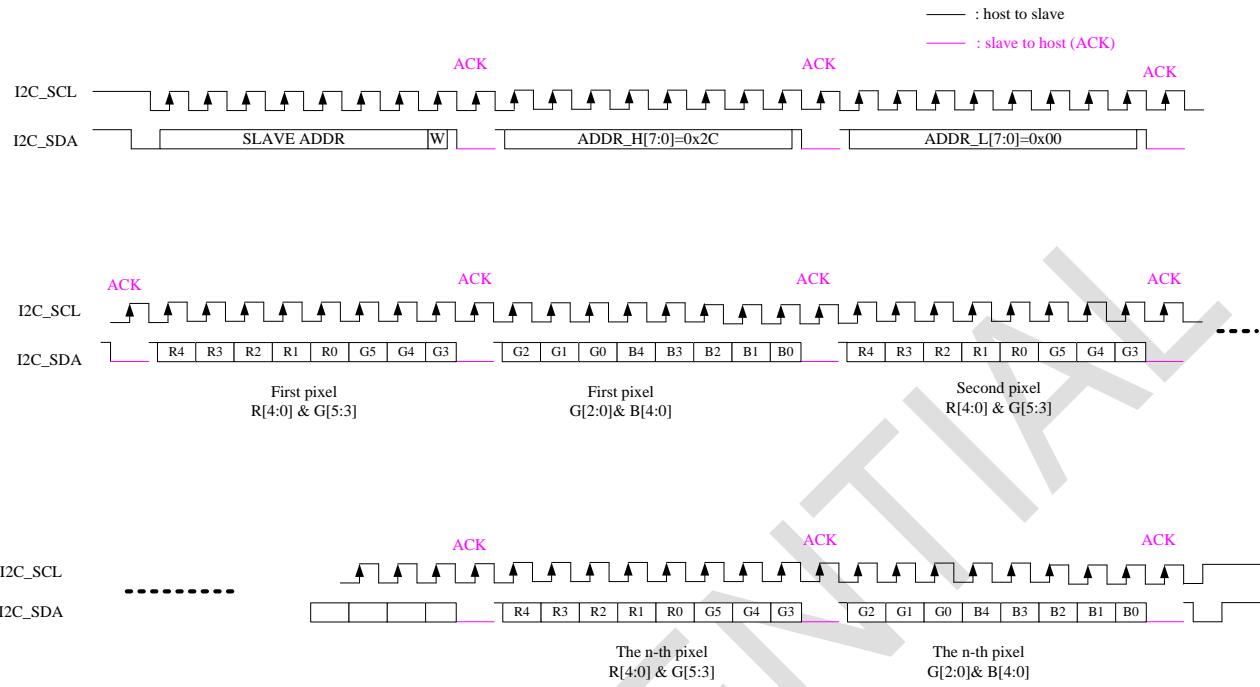
The I2C interface read command sequences are described in the following figure.

Read Cmd :

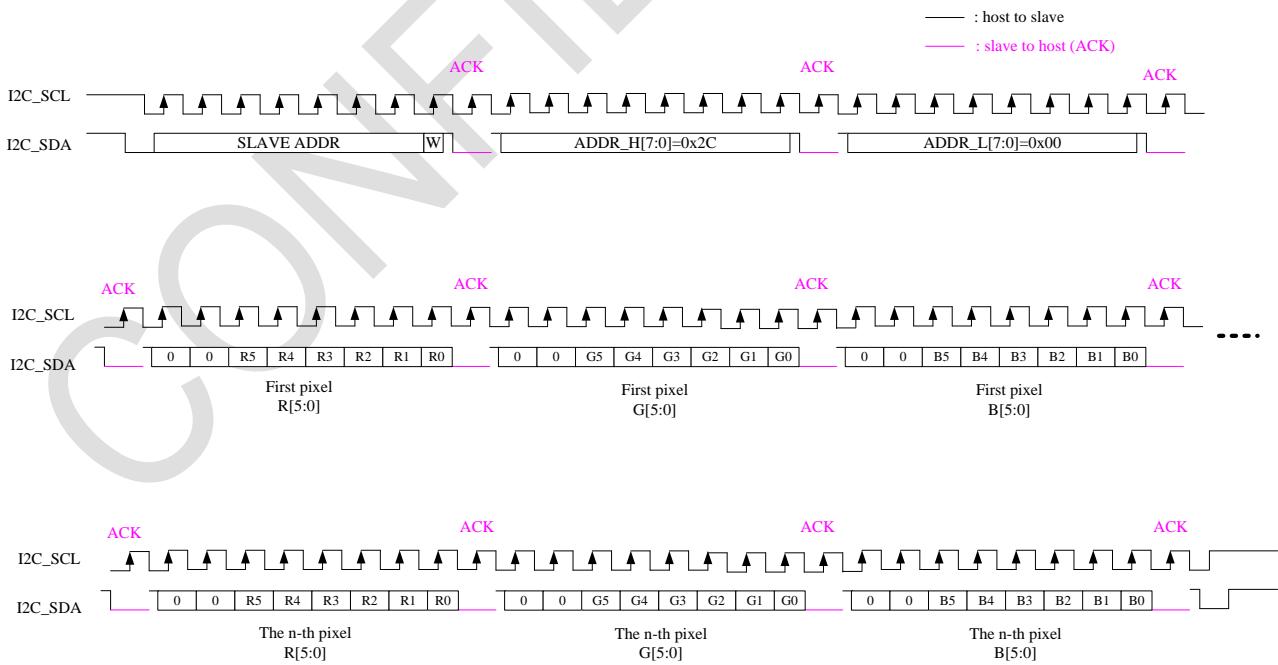


The I2C interface write data sequences are described in the following figure.

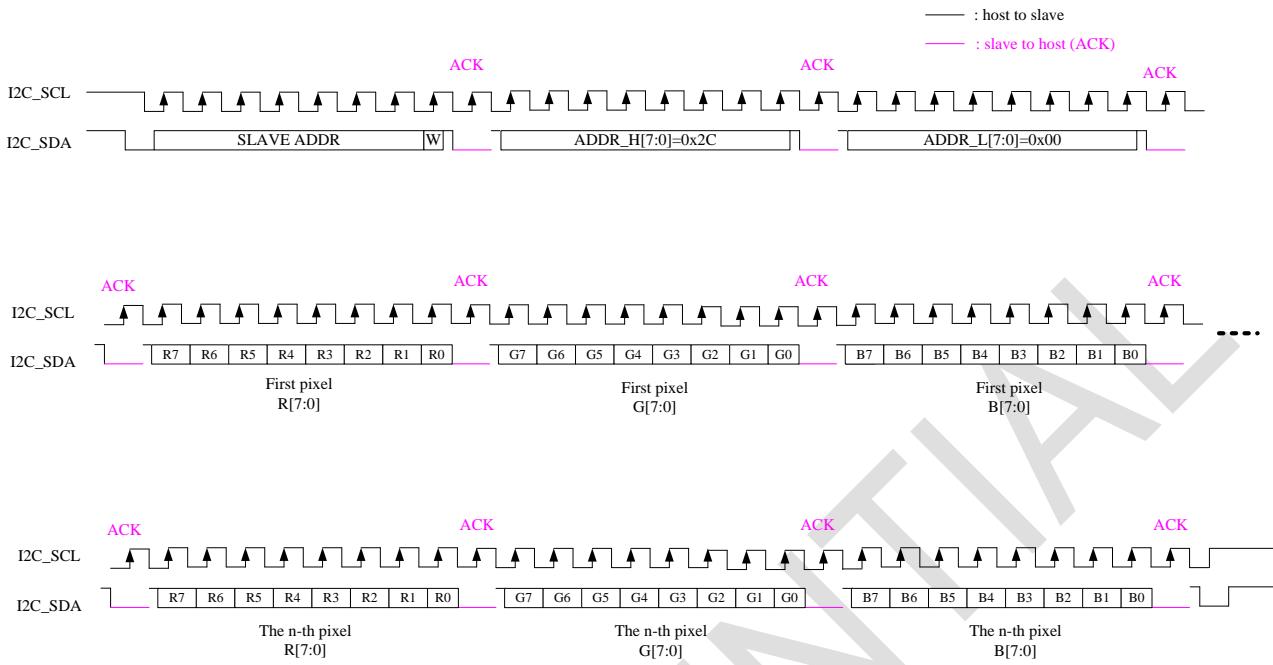
SRAM write: 65k colors, RGB 5-6-5 pixel data input (parameter of command 3A00h is 0x0005)



SRAM write: 262k colors, RGB 6-6-6 pixel data input (parameter of command 3A00h is 0x0006)

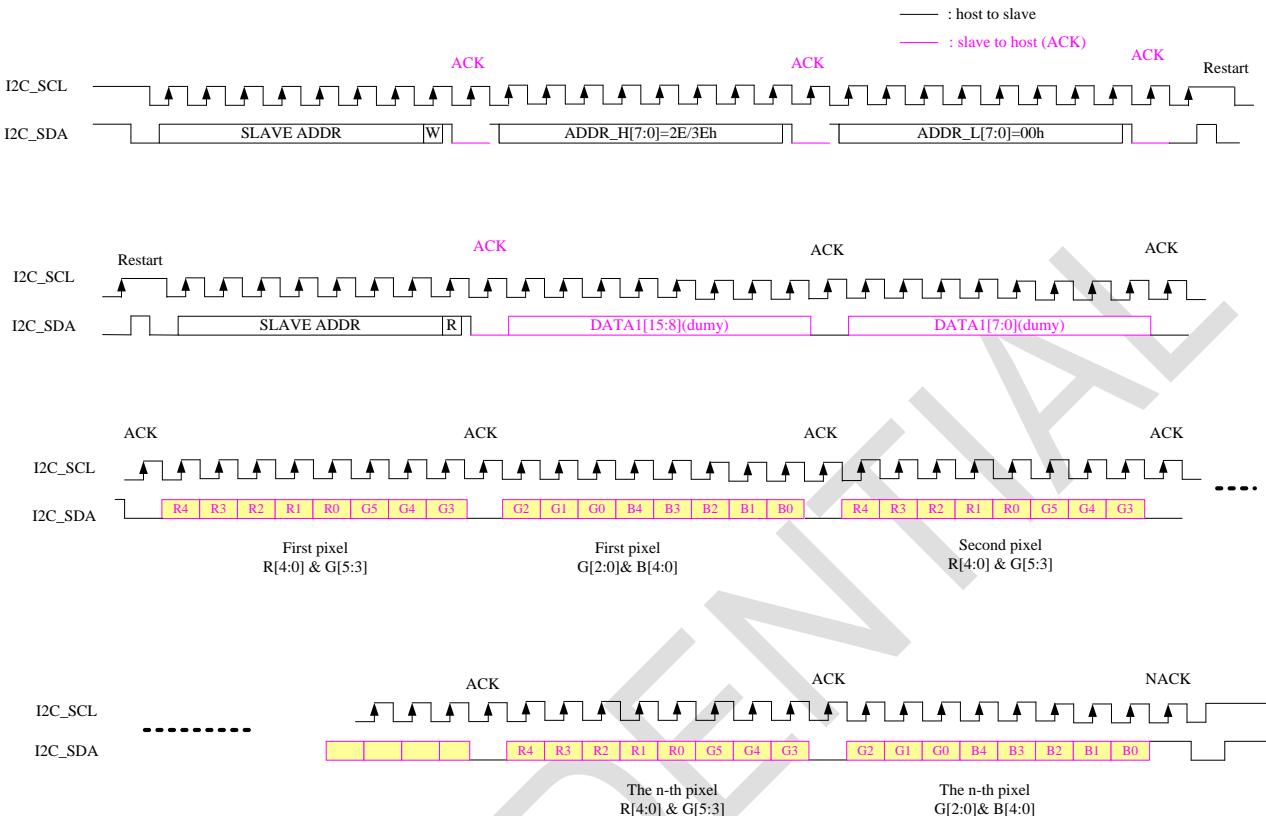


SRAM write: 16.7M colors, RGB 8-8-8 pixel data input (parameter of command 3A00h is 0x0007)

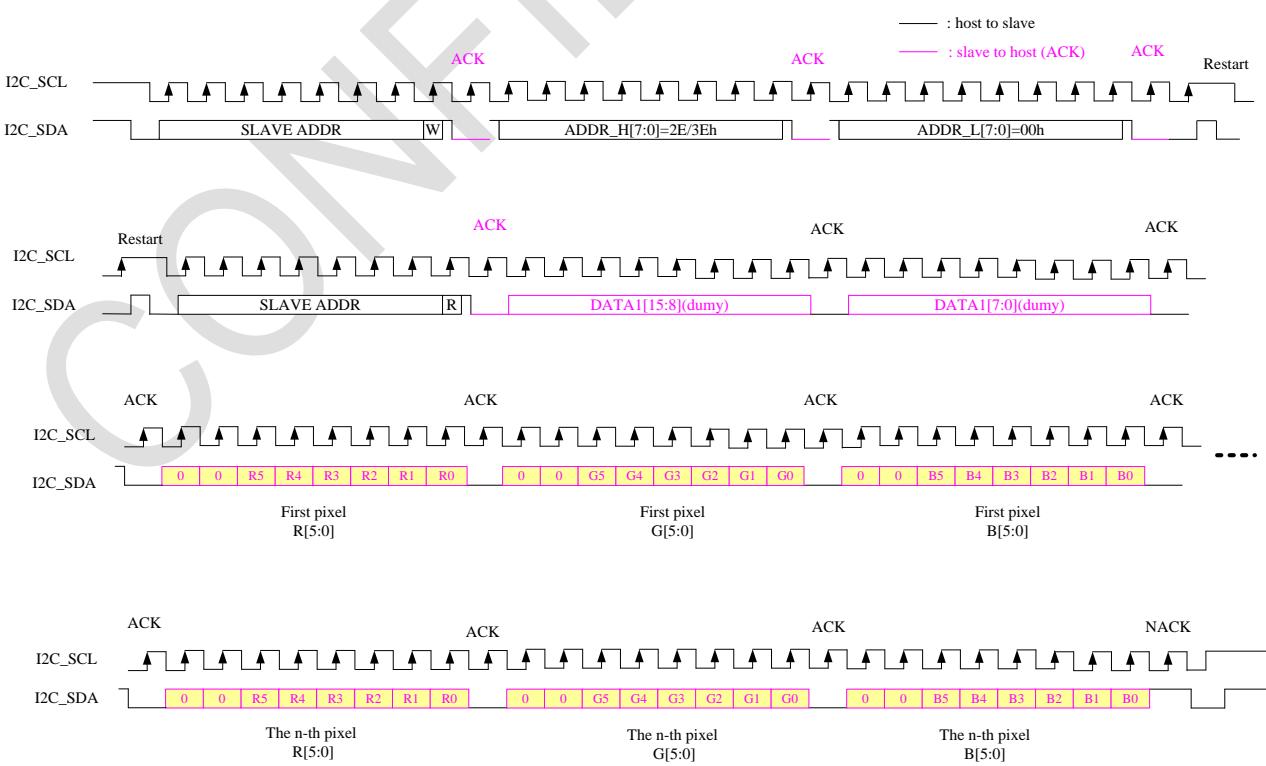


The I2C interface read data sequences are described in the following figure.

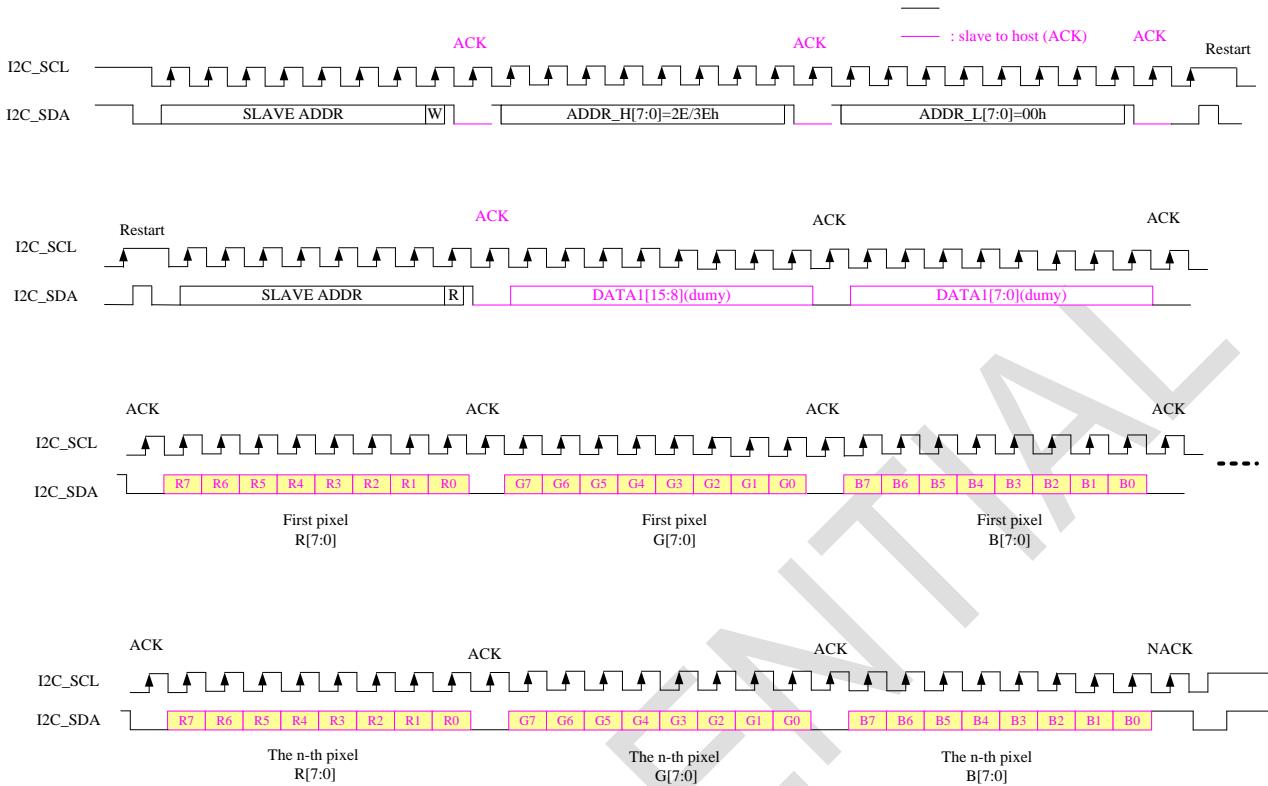
SRAM read: 65k colors, RGB 5-6-5 pixel data input (parameter of command 3A00h is 0x0005)



SRAM read: 262k colors, RGB 6-6-6 pixel data input (parameter of command 3A00h is 0x0006)



SRAM read: 16.7M colors, RGB 8-8-8 pixel data input (parameter of command 3A00h is 0x0007)



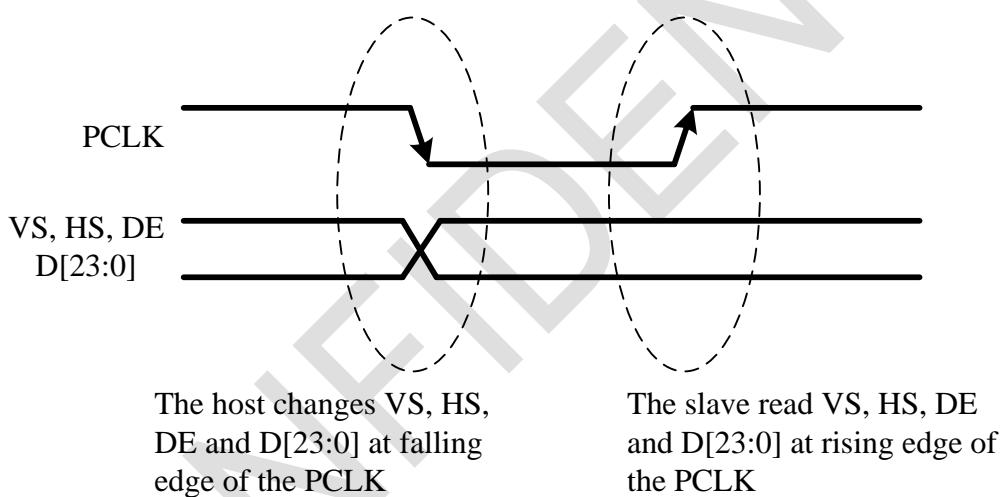
7.5 Display Pixel Interface (DPI)

In normal operation, systems based on DPI architecture rely on the host processor to continuously provide complete frames of image data at a sufficient frame rate to avoid flicker or other visible artifacts. The displayed image, or frame, is comprised of a rectangular array of pixels. The frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

Vsync indicates the beginning of each frame of the displayed image. Hsync signals the beginning of each horizontal line of pixels.

Each pixel value (16, 18 or 24-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data. Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.

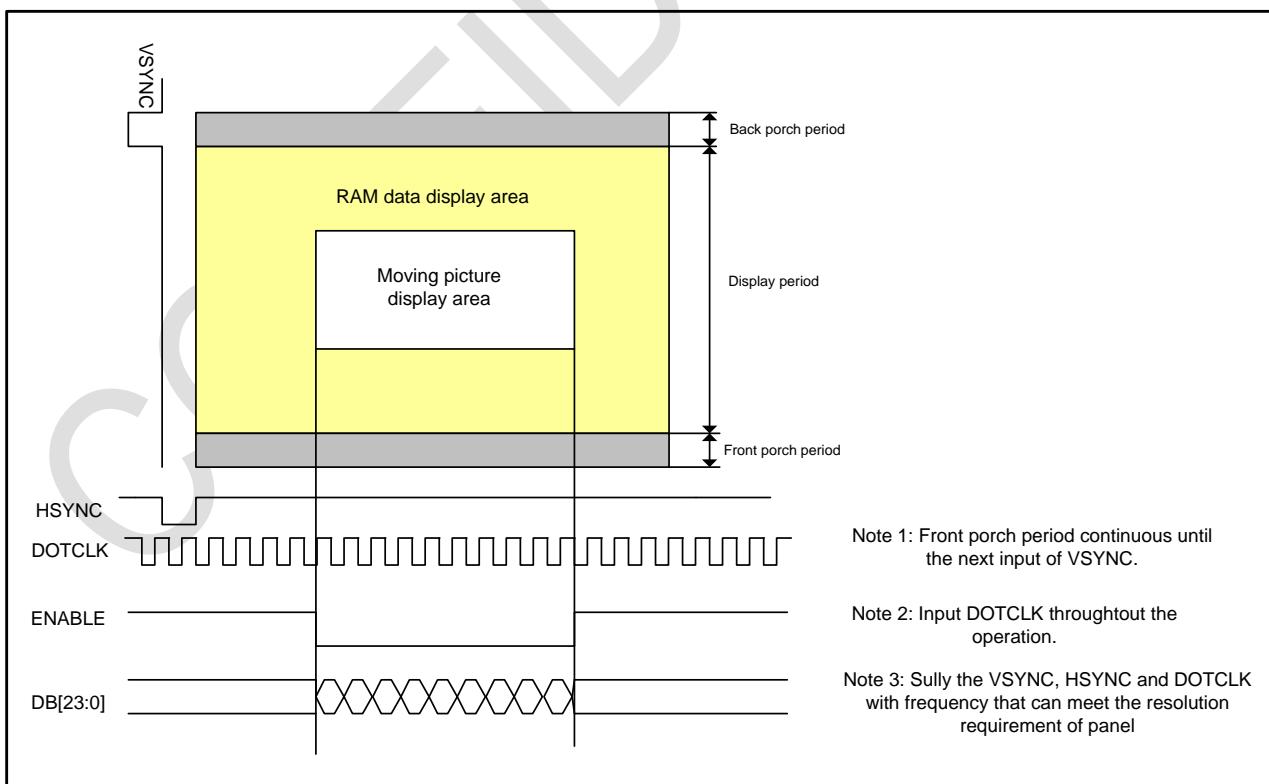
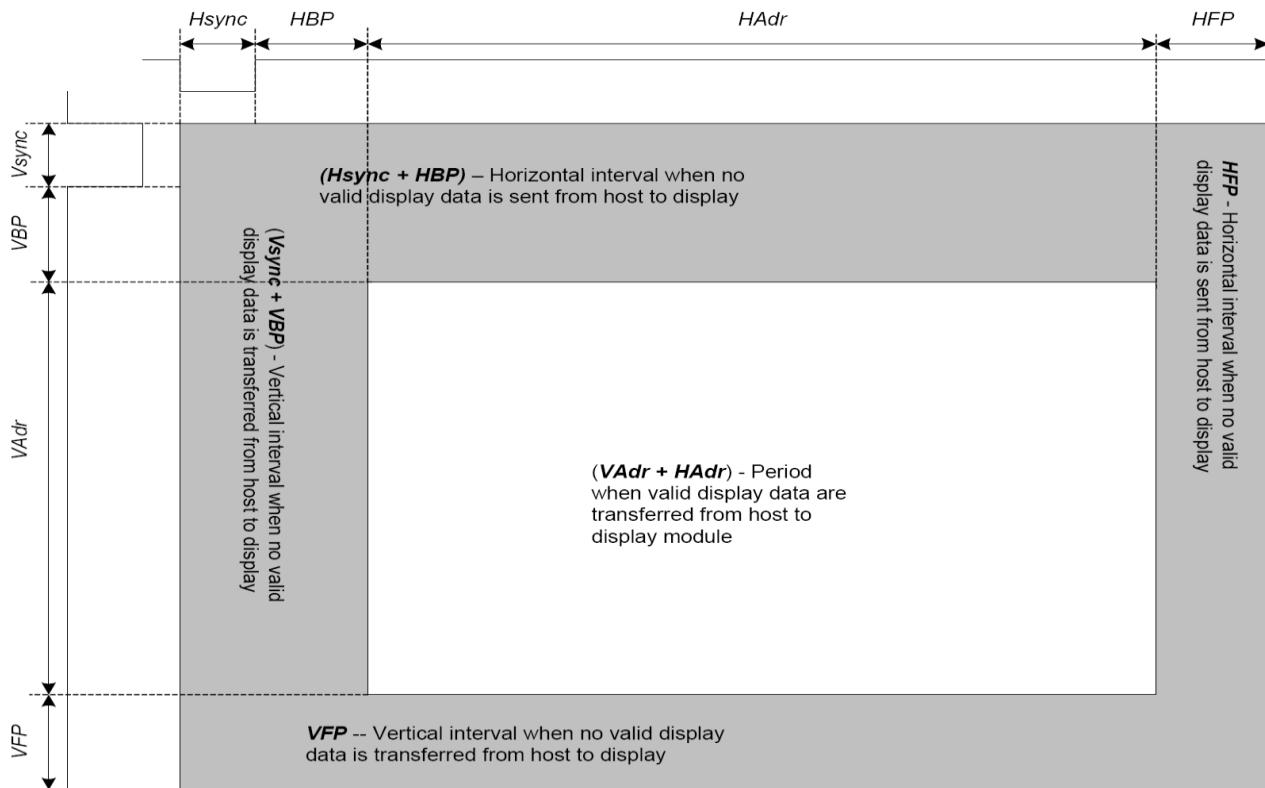
DPI signals are described in the follow figure.



DPI Interface data bus format: (Selected by VIPF[3:0])

VIPF	DB ₂₃	DB ₂₂	DB ₂₁	DB ₂₀	DB ₁₉	DB ₁₈	DB ₁₇	DB ₁₆	DB ₁₅	DB ₁₄	DB ₁₃	DB ₁₂	DB ₁₁	DB ₁₀	DB ₉	DB ₈	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀	color
5				R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[4]	B[3]	B[2]	B[1]	B[0]	65K	
6				R[5]	R[4]	R[3]	R[2]	R[1]	R[0]		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	262K
7	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	16.7M

DPI Interface Timing Chart.



7.6 Display Serial Interface (DSI)

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

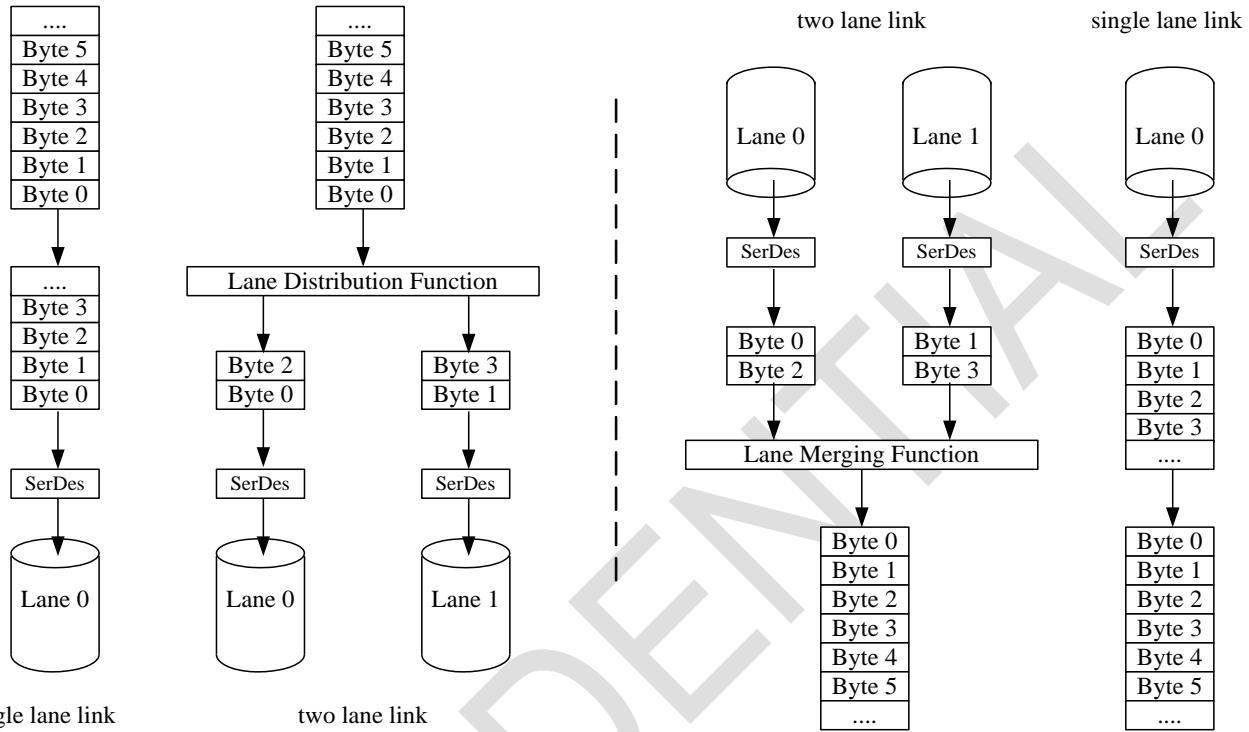
RM69032 is capable of both Command Mode operation and Video Mode operation. Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a display module that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface. Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. RM69032 Video Mode architectures also include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to reduce power consumption.

RM69032 Configuration:

Lane Pair	MCU(Master) RM69032(Slave)
Clock Lane	Unidirectional Lane Clock only
Data Lane 0	Bi-directional Lane ➤ Forward High-speed ➤ Bi-directional Escape Mode ➤ Bi-directional LPDT
Data Lane 1	Unidirectional Lane ➤ Forward High-Speed ➤ Escape Mode ➤ No LPDT
Data Lane 2	Bi-directional Lane ➤ Forward High-speed ➤ Escape Mode ➤ No LPDT
Data Lane 3	Bi-directional Lane ➤ Forward High-speed ➤ Escape Mode ➤ No LPDT

7.6.1 DSI Protocol

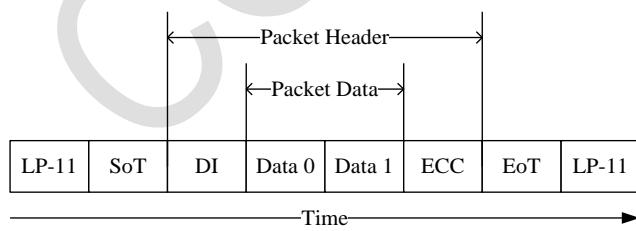
On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted to packets. These packets are sent across the serial Link. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands.



There are two kinds of packets, **short packet and long packet**.

- Short packet structure:

LP-11: low power mode
 SoT: start of transmission
 DI: data identification
 Data 0, Data1: packet data
 ECC: error correction code
 EoT: End of Transmission



DI structure:

Virtual Channel: these two bits identify the data as directed to one of four virtual channels

Data Type: It specifies the packet structure and packet format

Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

➤ Long packet structure:

LP-11: low power mode

SoT: start of transmission

DI: data identification

Word Count: the number of data bytes of packet data

ECC: error correction code

Checksum: The 16-bit CRC generator to check packet data. If the calculated checksum of receiver are equal to the packet data, the packet data is correct. If the calculated checksum of receiver are not equal, the packet data are not correct.

EoT: end of transmission



7.6.2 Processor to Peripheral Transactions

Processor to Peripheral Direction Packet Data Types

Data Type	Data Type binary	Description	Packet Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	reserved	Short
32h	11 0010	reserved	Short
03h	00 0011	reserved	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	reserved	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS Short WRITE, no parameters	Short
15h	01 0101	DCS Short WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
29h	10 1001	Generic Long Write	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long

➤ Sync Event, Data Type = xx 0001

Sync Events are all short packets and time-accurately. They can perform like the start and end of sync pulses. To represent timing information as accurately as possible, a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Hence, a V Sync End event implies an H Sync Start event for the last line of the VSA. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode.

➤ EoT packet

This short packet is used to indicate the end of a high speed (HS) transmission. This packet will enhance overall system reliability. Although the main objective of the EoTp is to enhance robustness during HS transmission mode, RM69032 can detect and interpret arriving EoTps regardless of transmission mode (HS or LP modes)

➤ Color Mode Off / On Command

They are short packet commands to switch video display module between normal display mode and low-color mode for power saving.

➤ Generic short write / read packet

Generic Short WRITE command is a Short packet type for sending generic data to the peripheral. Generic READ request is a Short packet requesting data from the peripheral.

➤ DCS commands

■ DCS short write command

DCS short write command is used to write a single data byte command to display module. If there is a valid parameter byte, data type bit 4 shall be set to 1. If there is no valid parameter byte, data type bit 4 shall be set to 0 and the parameter byte shall be 00h.

■ DCS read commands

The commands are used to request data from a display module.

■ DCS Long Write / write_LUT command

The commands are used to send larger blocks of data to a display module.

■ Maximum return packet size

This command specifies the maximum size of the payload in a long packet transmission from a display module to host processor.

■ Null Packet

This is a mechanism for keeping the data lane(s) in high speed mode while sending dummy data.

■ Blanking Packet

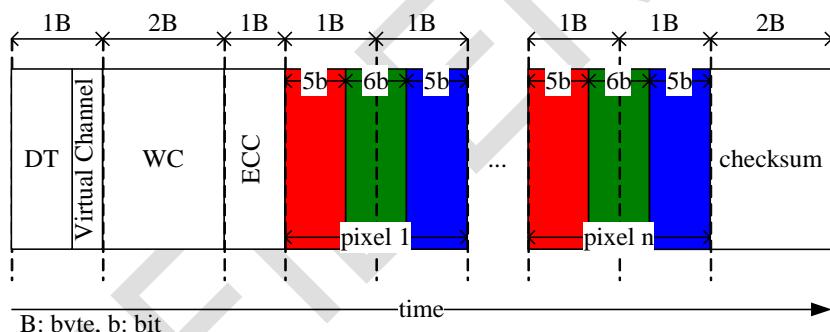
A Blanking packet is used to convey blanking timing information in a Long packet. The packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Blanking packets may contain arbitrary data as payload.

■ Generic Long Write

This is used to transmit arbitrary blocks of data from a host processor to a peripheral.

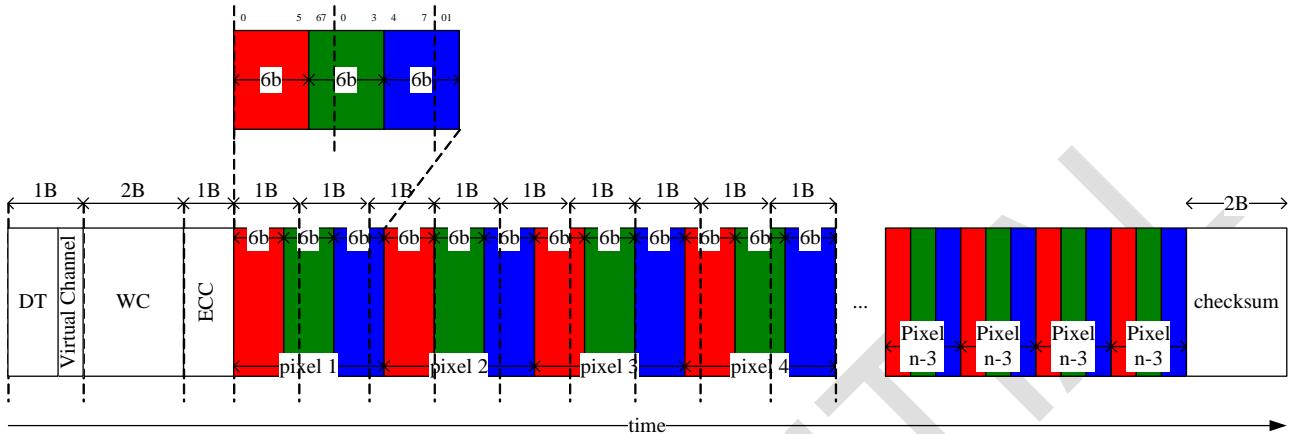
■ Packed Pixel Stream, 16-bit Format, Data Type: 00 1110

The pixel format is five bits red, six bits green and five bits blue. The green component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.



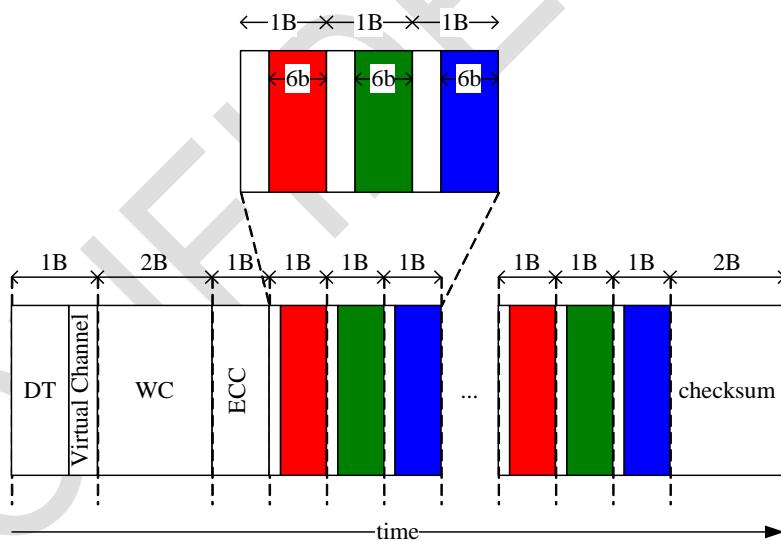
- Packet pixel stream, 18-bit format, Data Type: 01 1110

The pixel format is six bits red, six bits green and six bits blue. Within a color component, the LSB is sent first, the MSB last.



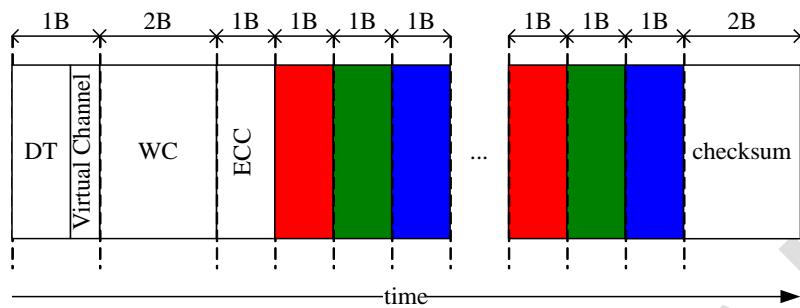
- Packet pixel stream, 18-bit format in three bytes, Data Type: 10 1110

This is 18-bit pixel losslessly packed format, each R, G or B color component is six bits but shifted to the upper bits of byte.



- Packet pixel stream, 24-bit format, Data Type: 11 1110

The pixel format is eight bits red, eight bits green and eight bits blue.



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7.6.3 Peripheral-to-Processor LP Transmission

All Command Mode systems require bidirectional capability for returning READ data, acknowledge, or error information to the host processor. Multi-Lane systems shall use Lane 0 for all peripheral-to-processor transmissions. Reverse-direction signaling shall only use low power mode transmission. Packet structure for peripheral-to-processor transaction is the same as for the processor-to-peripheral direction. For the processor-to-peripheral direction, two basic packet formats are the same as the peripheral-to-processor direction: Short and Long packet structure. BTA shall take place after every peripheral-to-processor transaction. This returns bus control to the host processor following the completion of the LP transmission from the peripheral.

There are four basic types of peripheral-to-processor transactions.

- Tearing Effect: It is a Trigger message sent to convey display timing information to the host processor.
- Acknowledge: It is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.
- Acknowledge and Error Report: It is a Short packet sent if any errors were detected in preceding transmissions from the host processor.
- Response to Read Request: It may be a Short or Long packet that returns data requested by the preceding READ command from the processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

- Following a non-Read command: If no errors were detected, the peripheral shall respond with Acknowledge.
- Following a Read request: The peripheral shall send the requested READ data if no errors were detected and stored since the last peripheral to host communication.
- Following a Read request: If only a single-bit ECC error was detected and corrected, the peripheral shall send the requested READ data in a Long or Short packet and a 4-byte Acknowledge and Error Report packet in the same LP transmission.
- Following a non-Read command: If only a single-bit ECC error was detected and corrected, the peripheral shall respond to BTA by sending a 4-byte Acknowledge and Error Report packet.
- Following a Read request: If multi-bit ECC errors were detected and not corrected, the peripheral shall send a 4-byte Acknowledge and Error Report packet without sending Read data.
- Following a non-Read command: If multi-bit ECC errors were detected and not corrected, the peripheral shall not execute the command, and shall send a 4-byte Acknowledge and Error Report packet.
- Following any command: If SoT Error, SoT Sync Error, the VC of DSI or the ID of DSI Invalid or DSI protocol violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge and Error Report response.
- Following any command: If EoT Sync Error or LP Transmit Sync Error is detected, or a checksum error

is detected in the payload, the peripheral shall send a 4-byte Acknowledge and Error Report packet.

Error Report Format

The following table shows the bit assignment for all error report.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	False Control Error
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	reserved
14	reserved
15	reserved

Peripheral-to-Processor Transaction – Detail Format Description

The following list is the complete set of peripheral-to-processor data types.

Data type, hex	Data type binary	Description	Packet size
02h	00 0010	Acknowledge and error report	short
08h	00 1000	reserved	short
11h	01 0001	GEN short read reponse, 1byte returned	short
12h	01 0010	GEN short read reponse, 2bytes returned	short
1Ah	01 1010	Generic long read reponse	long
1Ch	01 1100	DCS long read reponse	long
21h	10 0001	DCS short read reponse, 1byte returned	short
22h	10 0010	DCS short read reponse, 2bytes returned	short

- Acknowledge and error report: It is sent with BTA asserted when a reportable error is detected in the preceding, or earlier, transmission from the host processor.
- Generic Short Read Response: This is the short-packet response to Generic READ Request. Packet composition is the Data Identifier (DI) byte, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.
- Generic long read reponse: This is the long-packet response to Generic READ Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.
- DCS long read reponse: This is a Long packet response to DCS Read Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the DCS command itself is possibly corrupt, due to uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.
- DCS short read reponse: This is the short-packet response to DCS Read Request. Packet composition is DI, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

7.6.4 Error Correction Code (ECC)

ECC shall always be generated and appended in the Packet Header from the host processor. Peripherals with Bidirectional Links shall also generate and send ECC.

The number of parity or error check bits required is given by the Hamming rule, which uses parity to correct a single-bit error or detect a two-bit error, but are not capable of doing both simultaneously. DSI uses Hamming-modified codes where an extra parity bit is used to support both single error correction as well as two-bit error detection.

Since Packet Headers are fixed at four bytes (twenty-four data bits and eight ECC bits), P6 and P7 of the ECC byte are unused and shall be set to zero by the transmitter. The receiver shall ignore P6 and P7 and set both bits to zero before processing ECC.

- The parity bits of ECC are defined as below:

P7 = 0
P6 = 0
P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

The table below shows a compact way to specify the encoding of parity and decoding of syndromes.

- ECC Parity Generation Rules:

Data Bit	P7	P6	P5	P4	P3	P2	P1	P0	Hex
0	0	0	0	0	0	1	1	1	0x07
1	0	0	0	0	1	0	1	1	0x0B
2	0	0	0	0	1	1	0	1	0x0D
3	0	0	0	0	1	1	1	0	0x0E
4	0	0	0	1	0	0	1	1	0x13
5	0	0	0	1	0	1	0	1	0x15
6	0	0	0	1	0	1	1	0	0x16
7	0	0	0	1	1	0	0	1	0x19
8	0	0	0	1	1	0	1	0	0x1A
9	0	0	0	1	1	1	0	0	0x1C
10	0	0	1	0	0	0	1	1	0x23
11	0	0	1	0	0	1	0	1	0x25
12	0	0	1	0	0	1	1	0	0x26
13	0	0	1	0	1	0	0	1	0x29
14	0	0	1	0	1	0	1	0	0x2A
15	0	0	1	0	1	1	0	0	0x2C
16	0	0	1	1	0	0	0	1	0x31
17	0	0	1	1	0	0	1	0	0x32
18	0	0	1	1	0	1	0	0	0x34
19	0	0	1	1	1	0	0	0	0x38
20	0	0	0	1	1	1	1	1	0x1F
21	0	0	1	0	1	1	1	1	0x2F

22	0	0	1	1	0	1	1	1	0x37
23	0	0	1	1	1	0	1	1	0x3B

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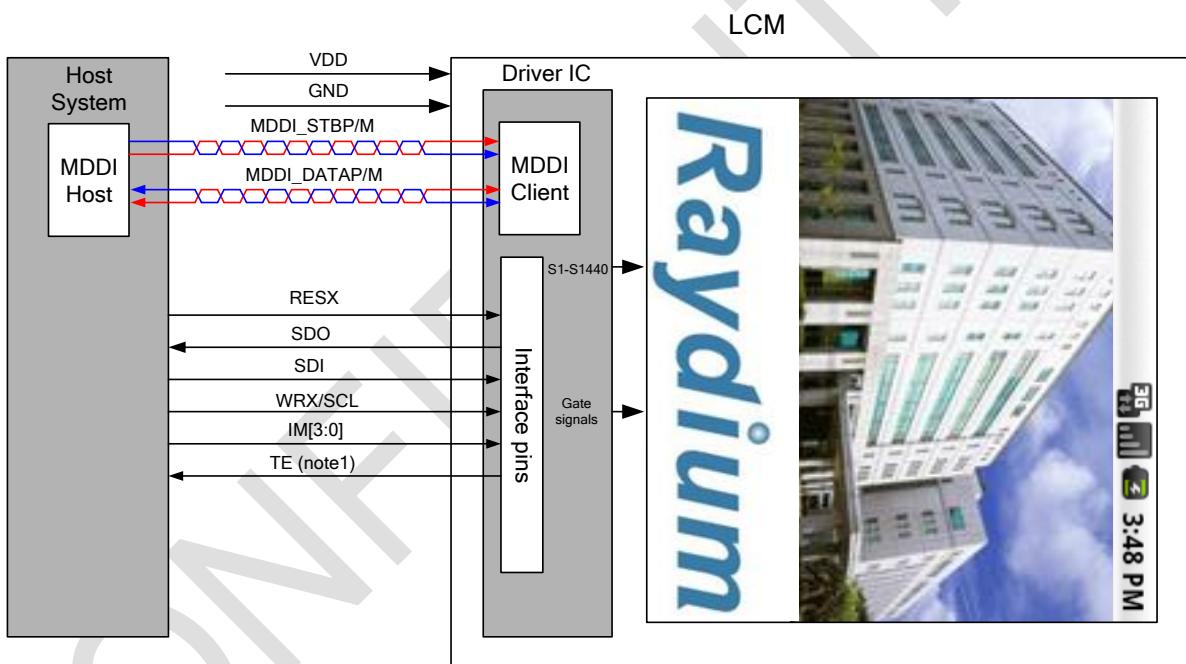
7.7 MDDI Interface

The RM69032 supports the Mobile Display Digital Interface (MDDI) is a differential small amplitude serial interface for high-speed data transfer through the following lines: DATA0_P/M, DATA1_P/M and STB_P/M. The specifications of MDDI supported by the RM69032 meet the MDDI specifications Version 1.2 as published by the Video Electronics Standards Association (VESA).

The RM69032 offers the bi-direction link to use for the register and display data read / write.

For power saving, the RM69032 offers both hibernation mode (Send shutdown packet), and enter deep standby mode to reduce power consumption.

The RM69032 supports the MDDI Type-I and Type-II of the MDDI specifications Version 1.2 and the application diagram is illustrated as follow.



Notes:

1. Based on the system configuration, use TE signal as the reference signal for moving picture display to avoid the tearing effect.
2. When enter to the MDDI interface from other interface, the Host needs to wait 100ms and can start to send any packet. For example wake up packet.
3. After shutting down the MDDI interface the Host needs to wait 500ns and can start to send wake up packet to wake up the MDDI link.
4. The terminal resistors are embedded between MDDI_DATA0_P/M, MDDI_DATA1_P/M and MDDI_STB_P/M.

7.7.1 MDDI Link Protocol

The RM69032's MDDI Link Protocol is in accordance with the MDDI specifications as published by VESA; refer to these specifications for more information on the MDDI Link Protocol.

DO NOT send any packets that are not supported by the RM69032 into a system containing the RM69032.

Supported MDDI packets are as follows:

RM69032 MDDI packets	Packet Name	Packet Type	Direction	Supported Type
Link Control Packet	Sub-frame header packet	15359 (0x3BFF)	Forward	Type I/Type II
	Filler packet	0	Forward/Reverse	Type I/ Type II (Forward) Type I Only (Reverse)
	Link Shutdown packet	69 (0x45)	Forward	Type I/Type II
	Reverse link encapsulation packet	65 (0x41)	Forward	Type I Only
	Round-trip delay measurement packet	82 (0x52)	Forward	Type I/Type II
	Forward link skew calibration packet	82 (0x52)	Forward	Type I/Type II
Client Status and Control Packet	Client capability packet	66 (0x42)	Reverse	Type I Only
	Client request and status packet	70 (0x46)	Reverse	Type I Only
	Register access packet	146 (0x92)	Forward/Reverse	Type I/ Type II (Forward) Type I Only (Reverse)
Basic Media Stream Packet	Video stream packet	16 (0x10)	Forward	Type I/Type II
	Flexible video stream packet	20 (0x14)	Forward	Type I/Type II
	Windowless video stream packet	22 (0x16)	Forward	Type I/Type II

7.7.2 MDDI Link Packet Descriptions

Sub-frame Header Packet

The Sub-Frame Header Packet is the first packet of every sub-frame.

Sub-frame Header Packet

Packet Length	Packet Type =0x3bff	Unique word =0x005a	Reversed 1	Sub-frame Length	Protocol Version	Sub-frame Count	Media-frame Count	CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	2 bytes	4 bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 0x3bff

Unique Word: unique word is 0x005a

Reserved 1: not used (set to zero)

Sub-frame Length: specify the number of bytes per sub-frame

Protocol version: set to zero

- Bit [15:2] – Reserved for future expansion. These should be set to all zero.
- Bits[1:0] – Sub-frame operational mode

“00” – Sub-frame lengths strictly followed.

“01” – Sub-frame lengths are flexible. Sub-frame packets should be sent at the first opportunity after the sub-frame length has been transmitted.

“10” – Sub-frame lengths are unlimited. No more sub-frame packets are required to be transmitted after the first sub-frame packet at startup.

Sub-frame Count: specify the number of sub-frame header packet

Media-frame Count: specify the number of media-frames

CRC: error check

Filler Packet

The Filler Packet is sent when no other information is available to be sent on the forward or reverse link.

Filler Packet

Packet Length	Packet Type=0	Filler Bytes (all zero recommended)	CRC
2 bytes	2 bytes	(Packet Length – 4) bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 0

Filler Bytes: set to zero

CRC: error check

Link Shutdown Packet

The Link Shutdown Packet is sent from the host to the client to indicate that the MDDI data and strobe will be shut down and go into a low-power hibernation state.

Link Shutdown Packet

Packet Length	Packet Type=69	CRC	All Zero
2 bytes	2 bytes	2 bytes	(Packet Length – 4) bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 69

CRC: error check

All Zero: set to zero (Type I: size is 16 bytes, Type II: size is 32 bytes)

Reverse Link Encapsulation Packet

Data is transferred in the reverse direction using the Reverse Link Encapsulation Packet.

Reverse Link Encapsulation Packet

Packet Length	Packet Type=65	hClient ID	Reversed Link Flags	Reverse Rate Divisor	Turn-Around 1 Length	Turn-Around 2 Length
2 bytes	2 bytes	2 bytes	1 byte	1 byte	1 byte	1 byte

Parameter CRC	All Zero 1	Turn-Around 1	Reversed Data Packets	Turn-Around 2	All Zero 2
2 bytes	8 bytes	x bytes	(Packet Length – x – y -26) bytes	y bytes	8 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 65

hClient ID: set to zero

Reverse Link Flags:

- Bit 0 – 0: No packet request
 - 1: Host needs the Client Capability Packet
- Bit 1 – 0: No packet request
 - 1: Host needs the Client Request and Status Packet
- Bit [7:2] – set to zero

Reverse Rate Divisor: reverse data rate = reverse link data clock

Turn-Around 1 Length: the length of Turn-Around 1 is the forward link data rate

Turn-Around 2 Length: the length of Turn-Around 2 is determined by Round-trip delay of the link

Parameter CRC: error check

All zero: set to zero

Turn-Around 1: First turn-around period

Reverse Data Packets: A series of data packets transferred from the client to host

Turn-Around 2: The second turn-around period

Round-Trip Delay Measurement Packet

The Round-Trip Delay Measurement Packet is used to measure the propagation delay from the host to the client plus the delay from the client back to the host. This packet is most useful when the MDDI link is running at the maximum speed intended for a particular application. The packet may be sent in Type I mode and at a lower data rate to increase the range of the Round-Trip delay measurement.

Round Trip Measurement Packet

Packet Length	Packet Type=82	hClient ID	Parameter CRC
2 bytes	2 bytes	2 bytes	2 byte
64 bytes	64 bytes	2 bytes	64 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 82

hClient ID: set to zero

Parameter CRC: error check

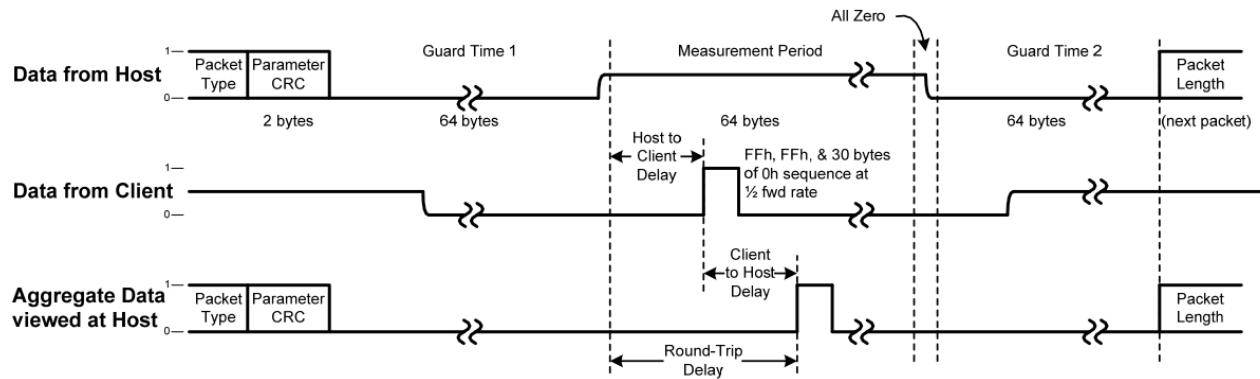
Guard Time 1: allow overlap of the host and client

Measurement Period: a 64 bytes window to allow the client to respond

All Zero: set to zero

Guard Time 2: allow overlap of the measurement period by the client

The timing of events during the Round-Trip Delay Measurement Packet illustrates as follow.



Forward Link Skew Calibration Packet

This packet allows the client to calibrate itself for differences in the propagation delay of the MDDI_DATA signals with respect to the MDDI_STB signal. Without delay skew compensation the maximum data rate must be limited to account for the worst-case variation in these delays. It is recommended that this packet only be sent when the forward link data rate is configured to 50 Mbps or lower. After sending this packet to calibrate the client the data rate may be stepped up above 50 Mbps. With the data rate set too high during the skew calibration process the client might synchronize to an alias of the bit period which would cause the delay skew compensation setting to be off by more than one bit time, resulting in erroneous data clocking. The greatest possible Interface Type must be selected prior to sending the Forward Link Skew Calibration Packet so that all existing data bits are calibrated. The client must indicate its ability to support the Forward Link Skew Calibration Packet via bit 19 of Client Feature Capability Indicators field of the Client Capability Packet.

Prior to performing skew calibration the host must not send data faster than the rate specified by the Pre-calibration Data Rate Capability field of the Client Capability Packet. However, after calibration is performed, the host may send data up to the rate defined by the Post-calibration Data Rate Capability field. It is recommended that the host send the Forward Link Skew Calibration Packet at regular intervals to correct

changes in the relative delay between the different signal pairs due to changes in temperature.

Forward Link Skew Calibration Packet

Packet Length	Packet Type=83	hClient ID	Parameter CRC	All Zero 1	Calibration Data Sequence	All Zero 2
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	Pacet Length – 22 bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 83

hCilent ID: set to zero

Parameter CRC: error check from packet length to the hClient ID.

All Zero 1:

8 bytes that contain eight 8-bit unsigned integers equal to zero. This field ensures that there will be a transition on MDDI_STB at the beginning of the Calibration Data Sequence field. It also provides sufficient time for the client core logic to change the mode of the clock recovery circuit from using the XOR of MDDI_Data0 and MDDI_STB to simply using MDDI_STB as the recovered clock.

Calibration Data Sequence:

a data sequence that causes the MDDI_Data signals to toggle at every data period. The length of the Calibration Data Sequence field is determined by the interface type being used on the forward link. During the Calibration Data Sequence the MDDI host controller sets all MDDI_Data signals equal to the strobe signal. The client clock recovery circuit must use only MDDI_STB rather than MDDI_STB XOR MDDI_Data0 to recover the data clock while the Calibration Data Sequence field is being received by the client.

Depending on the exact phase of MDDI_STB at the beginning of the Calibration Data Sequence field the Calibration Data Sequence will be one of the following based on the interface Type being used when this packet is sent:

- Type 1 – (64 byte data sequence) AAh, AAh … or 55h, 55h…
- Type 2 – (128 byte data sequence) CCh, CCh … or 33h, 33h…

All Zero 2:

8 bytes that contain eight 8-bit unsigned integers equal to zero. This field provides sufficient time for the client core logic to change the mode of the clock recovery circuit back to the original state, from using MDDI_STB as the recovered clock to using the XOR of MDDI_Data0 and MDDI_STB.

Client Capability Packet

It is recommended that the client send a Client Capability Packet to the host after forward link

synchronization is acquired, and it is required when requested by the host via the Reverse Link Flags in the Reverse Link Encapsulation Packet.

Client Capability Packet

Packet Length	Packet Type=66	cClient ID	Protocol Version	Min Protocol Version	Pre-calibration Data Rate Capability	Interface Type Capability
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	1 byte
Number of Alt Display	Post-calibration Data Rate Capability	Bitmap Width	Bitmap Height	Display Window Width	Display Window Height	Color Map Size
1 byte	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	4 bytes
Color Map RGB Width	RGB Capability	Monochrome Capability	Reversed 1	Y Cb Cr Capability	Bayer Capability	Reversed 2
2 bytes	2 bytes	1 byte	1 byte	2 bytes	2 bytes	2 bytes
Client Feature Capability	Max Video Frame Rate	Min Video Frame Rate	Min Sub-frame Rate	Audio Buffer Depth	Audio Channel Capability	Audio Sample Rate Capability
4 bytes	1 byte	1 byte	2 bytes	2 bytes	2 bytes	2 bytes
Audio Sample Resolution	Mic Sample Resolution	Mic Sample Rate Capability	Keyboard Data Format	Pointing Device Data Format	Content Protection Type	Mfr Name
1 byte	1 byte	2 bytes	1 byte	1 byte	2 bytes	2 bytes
Product Code	Reversed 3	Serial Number	Week of Mfr	Year of Mfr	CRC	
2 bytes	2 bytes	4 bytes	1 byte	1 byte	2 bytes	

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 66

cClient ID: set to zero

Protocol Version: set to 0002h

Min Protocol Version: specify the minimum protocol version (0001h)

Pre-Calibration Data Rate Capability: specify the maximum data rate the client can receive (190h)

Interface Type Capability: Client can function in Type 2 (2-bit) mode on the forward link (01h)

Number of Alt Displays: set to zero

Post-Calibration Data Rate Capability: specify the maximum data rate the client can receive (190h)

Bitmap Width: specify the width of the bitmap (1E0h)
Bitmap Height: specify the height of the bitmap (320h)
Display Window Width: specify the width of the display window (1E0h)
Display Window Height: specify the height of the display window (320h)
Color Map Size: set to zero
Color Map RGB Width: set to zero
RGB Capability: specify the resolution of RGB format (0888h)
Monochrome Capability: set to zero
Reserved 1: set to zero
Y Cb Cr Capability: set to zero
Bayer Capability: set to zero
Reserved 2: set to zero
Client Feature Capability Indicators: 00CC8000h
Maximum Video Frame Rate Capability: specify the maximum video frame (3Ch)
Minimum Video Frame Rate Capability: specify the minimum video frame (3Ch)
Minimum Sub-frame Rate: specify the minimum sub-frame rate (00h)
Audio Buffer Depth: set to zero
Audio Channel Capability: set to zero
Audio Sample Rate Capability: Set to zero
Audio Sample Resolution: set to zero
Mic Audio Sample Resolution: set to zero
Mic Sample Rate Capability: set to zero
Keyboard Data Format: set to zero
Pointing Device Data Format: set to zero
Content Protection Type: set to zero
Mfr Name: set to 0000h
Product Code: set to 6812h
Reserved 3: set to zero
Serial Number: set to zero
Week of Manufacture: set to zero
Year of Manufacture: 00h
CRC: error check

Client Request and Status Packet

The host needs a small amount of information from the client so it can configure the host-to-client link in an optimum manner. The Client Request and Status Packet is required to report errors and status to the host.

Client Request and Status Packet

Packet Length	Packet Type=70	cClient ID	Reverse Link Request	CRC Error Count	Client Status	Client Busy Flags	CRC
2 bytes	2 bytes	2 bytes	2 bytes	1 byte	1 byte	2 bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 70

cClient ID: set to zero

Reverse Link Request: specify the number of bytes the client needs in the reverse link in the next sub-frame to send information to the host.

CRC Error Count: count the number of CRC errors occurred

Client Status:

- Bit 0 – 1: capability has changed
0: capability has not changed
- Bit 1 – indicates the client has detected an error
- Bit [7:2] – set to zero

Client Busy Flags:

- Bit 0 – bitmap block transfer function is busy
- Bit 1 – bitmap area fill function is busy
- Bit 2 – bitmap pattern fill function is busy
- Bit 3 – the graphics subsystem is busy
- Bit [15:4] – set to zero

CRC: error check

Register Access Packet

Register Access Packet is utilized when setting instruction to the RM69032. This packet cannot be used for RAM access.

Register Access Packet

Packet Length	Packet Type=146	bClient ID	Read/Write Info	Register Address	Parameter CRC	Register Data List	Register Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	(Packet Length -14) bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 146

bClient ID: set to zero

Read/Write Info:

Bits[15:14]	Read/Write Flags
00	Write
01	Reserved
10	Read
11	Response to read

Bit [13:0] – specifies the number of 32-bit register data list items to be transferred in the Register Data List Filed.

Register Address: upper bits shall set to zero

Parameter CRC: error check from packet length to the register address

Register Data List: written (or read) registers to (from) client

Register Data CRC: error check of the register data list

Video Stream Packet

The RM69032 supports the Video Stream Packet to transfer display data including RGB data to RAM.

Video Stream Packet

Packet Length	Packet Type=16	bClient ID	Video Data Format Descriptor	Pixel Data Attributes	X Left Edge	Y Top Edge
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes

X Right Edge	Y Bottom Edge	X Start	Y Start	Pixel Count	Parameter CRC	Pixel Data	Pixel Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	(Packet Length -26) bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 16

bClient ID: set to zero

Video Data Format Descriptor

[15:12]	[11:18]	[7:4]	[3:0]	Transfer pixel format
0101	0x8	0x8	0x8	Packed 24 bits pixel RGB format (R:G:B=8:8:8)
0101	0x6	0x6	0x6	Packed 18 bits pixel RGB format (R:G:B=6:6:6)
0101	0x5	0x6	0x5	Packed 16 bits pixel RGB format (R:G:B=5:6:5)
Others setting disabled				

Pixel Data Attributes: The pixel data is written to RAM buffer of RM69032 (00C3h)

X Left Edge: Specify the X coordinate of the left edge of the screen window filled by the Pixel Data field.

Y Top Edge: Specify the Y coordinate of the top edge of the screen window filled by the Pixel Data field

X Right Edge: Specify the X coordinate of the right edge of the window being updated.

Y Bottom Edge: Specify the Y coordinate of the bottom edge of the window being updated.

X Start: Specify X start address for the first pixel in the Pixel Data field below.

Y Start: Specify Y start address for the first pixel in the Pixel Data field below.

Pixel Count: specify the number of pixels

Parameter CRC: error check from packet length to the pixel count

Pixel Data: the raw video data

Pixel Data CRC: error check of the pixel data

Pixel Data Format

MDDI data byte	D7	D6	D5	D4	D3	D2	D1	D0	Color
RGB 5:6:5	G2	G1	G0	B4	B3	B2	B1	B0	65-Color (1 pixel/ 16 bits RGB format)
	R4	R3	R2	R1	R0	G5	G4	G3	
RGB 6:6:6	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color (1 pixel/ 18 bits RGB format)
	R3	R2	R1	R0	G5	G4	G3	G2	
	B5	B4	B3	B2	B1	B0	R5	R4	
RGB 8:8:8	B7	B6	B5	B4	B3	B2	B1	B0	16.7M-Color (1 pixel/ 24 bits RGB format)
	G7	G6	G5	G4	G3	G2	G1	G0	
	R7	R6	R5	R4	R3	R2	R1	R0	

Flexible Video Stream Packet

The RM69032 supports the Flexible Video Stream Packet to transfer display data including RGB data to RAM. This allows for a reduction in the number of fields sent in an environment where one or more fields are not changing values.

Flexible Video Stream Packet

Packet Length	Packet Type=20	bClient ID	Field Present Flags	Video Data Format Description	Pixel Data Attributes	X Left Edge	Y Top Edge
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes
X Right Edge	Y Bottom Edge	X Start	Y Start	Pixel Count	Parameter CRC	Pixel Data	Pixel Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	Packet Length – present header bytes	2 bytes

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 20

bClient ID: set to zero

Field Present Flags: indicates the field in the packet is present (value "1") or not present (value "0").

- Bit 0: indicates the presence of the Video Data Format Description Field.
- Bit 1: indicates the presence of the Pixel Data Attributes Field.
- Bit 2: indicates the presence of the X Left Edge Field.
- Bit 3: indicates the presence of the Y Top Edge Field.
- Bit 4: indicates the presence of the X Right Edge Field.
- Bit 5: indicates the presence of the Y Bottom Edge Field.
- Bit 6: indicates the presence of the X Start Field.
- Bit 7: indicates the presence of the Y Start Field.
- Bit 8: indicates the presence of the Pixel Count Field.
- Bits [15:9] are all "0".

Video Data Format Descriptor

[15:12]	[11:18]	[7:4]	[3:0]	Transfer pixel format
0101	0x8	0x8	0x8	Packed 24 bits pixel RGB format (R:G:B=8:8:8)
0101	0x6	0x6	0x6	Packed 18 bits pixel RGB format (R:G:B=6:6:6)
0101	0x5	0x6	0x5	Packed 16 bits pixel RGB format (R:G:B=5:6:5)
Others setting disabled				

X Left Edge: Specify the X coordinate of the left edge of the screen window filled by the Pixel Data field.

Y Top Edge: Specify the Y coordinate of the top edge of the screen window filled by the Pixel Data field

X Right Edge: Specify the X coordinate of the right edge of the window being updated.

Y Bottom Edge: Specify the Y coordinate of the bottom edge of the window being updated.

X Start: Specify X start address for the first pixel in the Pixel Data field below.

Y Start: Specify Y start address for the first pixel in the Pixel Data field below.

Pixel Data Attributes: The pixel data is written to RAM buffer of RM69032 (00C3h)

Pixel Count: specify the number of pixels

Parameter CRC: error check from packet length to the pixel count

Pixel Data: the raw video data

Pixel Data CRC: error check of the pixel data

Windowless Video Stream Packet

The RM69032 supports the Windowless Video Stream Packet to transfer display data including RGB data to RAM. This packet type assumes that full screen updates are always occurring and therefore there is no need for the window information.

Windowless Video Stream Packet

Packet Length	Packet Type=22	bClient ID	Video Data Format Description	Pixel Data Attributes	Pixel Count	Parameter CRC
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes
Pixel Data				Pixel Data CRC		
Packet Length – 14 bytes				2 bytes		

Packet Contents:

Packet Length: packet length not including the packet length field

Packet Type: packet type is 22

bClient ID: set to zero

Video Data Format Descriptor

[15:12]	[11:18]	[7:4]	[3:0]	Transfer pixel format
0101	0x8	0x8	0x8	Packed 24 bits pixel RGB format (R:G:B=8:8:8)
0101	0x6	0x6	0x6	Packed 18 bits pixel RGB format (R:G:B=6:6:6)
0101	0x5	0x6	0x5	Packed 16 bits pixel RGB format (R:G:B=5:6:5)
Others setting disabled				

Pixel Data Attributes: The pixel data is written to RAM buffer of RM69032 (00C3h)

Pixel Count: specify the number of pixels

Parameter CRC: error check from packet length to the pixel count

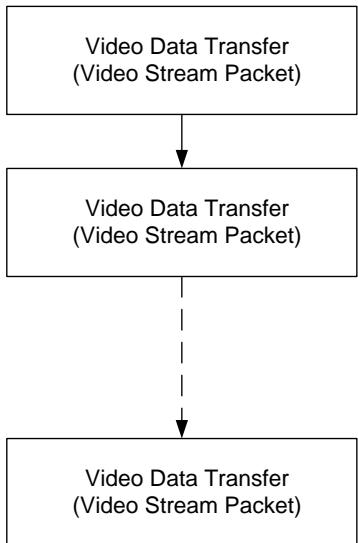
Pixel Data: the raw video data

Pixel Data CRC: error check of the pixel data

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7.7.3 Writing Video Data to Memory Sequence

In order to write video data to memory, the following sequence should be programmed. This packet should be followed by video stream packets.

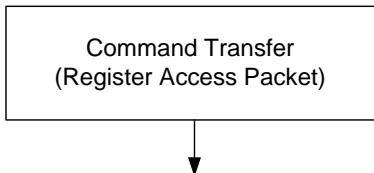


Writing Video Data to Memory Sequence

7.7.4 Writing Register Sequence

In order to write registers, register access packet should be used. Register access packet is used to write data to register.

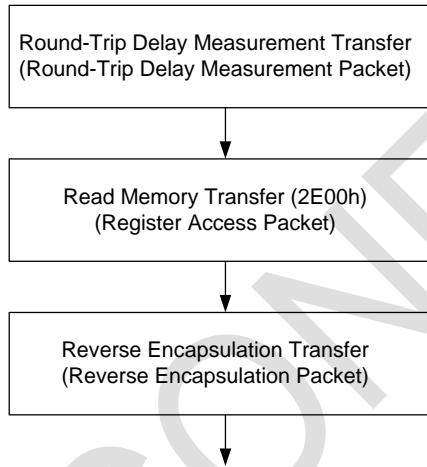
Writing Register Sequence:



7.7.5 Reading Video Data from Memory Sequence

In order to read a pixel data from memory (readable one pixel only), the following sequence should be programmed. Memory read command (2E00h) is followed by reverse encapsulation packet. DDI transmits video pixel data through encapsulation packet. Please refer to VESA spec for detailed description.

Reading Video Data from Memory Sequence:



Notes:

1. X addresses for memory data read is set by 2A00h and 2A01h (XS[15:0]).

The parameters of 2A00h and 2A01h are stored on relative registers while command 2A00h~2A03h are executed completely. See also section “6.1 User Command Set” and Note 2.

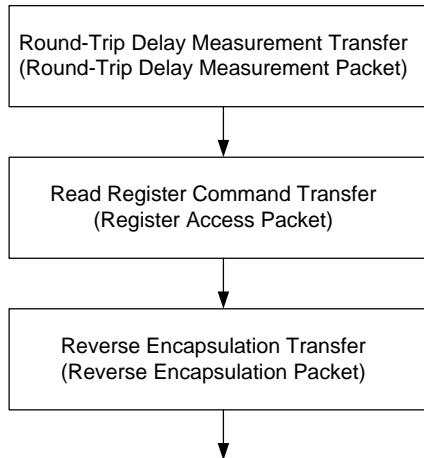
2. Y addresses for memory data read is set by 2B00h and 2B01h (YS[15:0]).

The parameters of 2B00h and 2B01h are stored on relative registers while command 2B00h~2B03h are executed completely. See also section “6.1 User Command Set” and Note 2.

7.7.6 Reading Register Sequence

In order to read registers, the following sequence should be programmed. Next, register read command is followed by reverse encapsulation packet. DDI transmits register data through encapsulation packet. Please refer to VESA spec for detailed description.

Reading Register Sequence:



7.7.7 Hibernation Setting

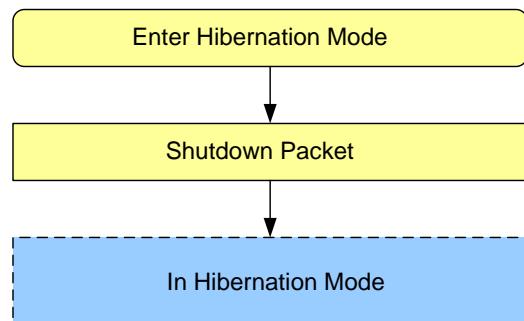
The Client MDDI of the RM69032 provides a hibernation setting. The methods for waking up the hibernation mode can be determined based on actual usage.

Wake-up	Condition
Host-Initiated Wake-up	Wake up the MDDI link by MDDI Host

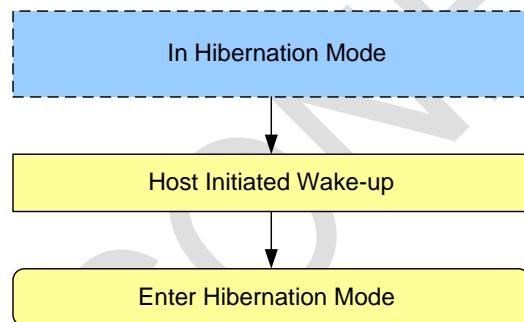
Note: In the Hibernation state, the data is retained in RAM and the display operation is maintained.

Hibernation setting and wake-up sequence must in accordance with VESA-MDDI specifications.

Hibernation setting sequence



Hibernation Wake-up sequence



7.7.8 MDDI Deep Standby Mode Setting

The Client MDDI of the RM69032 includes a MDDI deep standby mode setting so it can enter a off state and reduce power consumption during Hibernation mode.

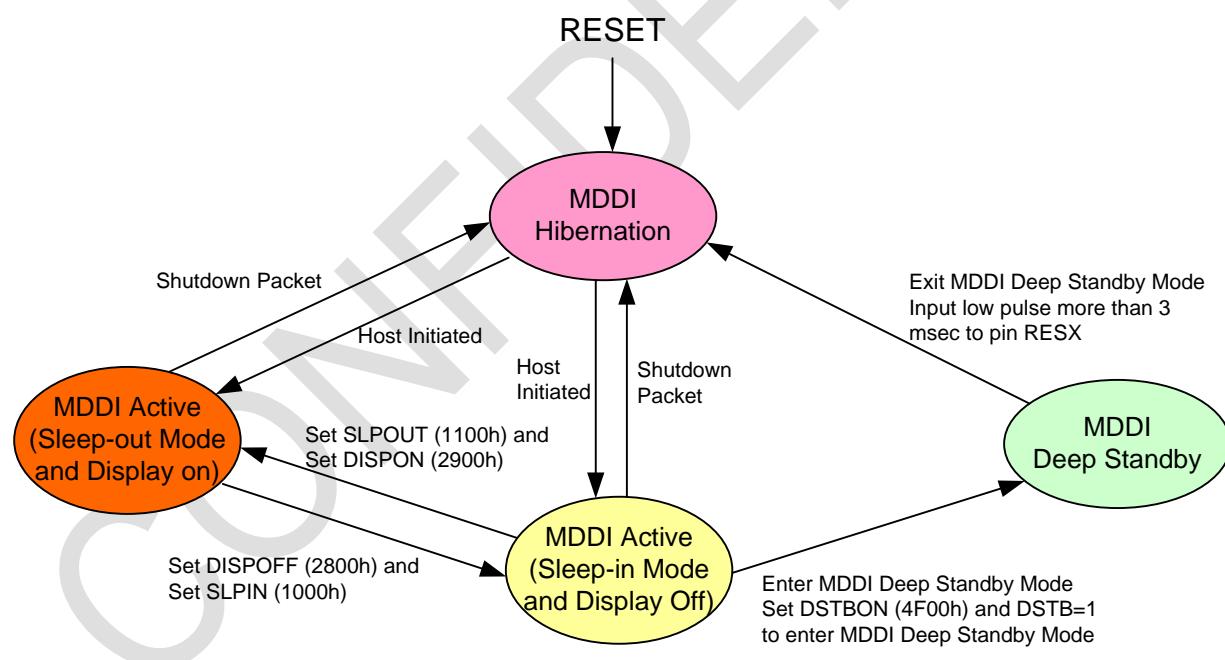
The MDDI enters Hibernation mode when a Shutdown Packet is sent. The standby power needs of the Client MDDI can be reduced, even while the MDDI Link is maintained in Hibernation mode.

When entering MDDI deep standby mode, the RM69032 stops operation rather than maintaining Hibernation mode. Input low pulse 3 msec from RESX pin to cancel deep standby mode, after which a Host-Initiated Wake-up should cancel the Hibernation mode.

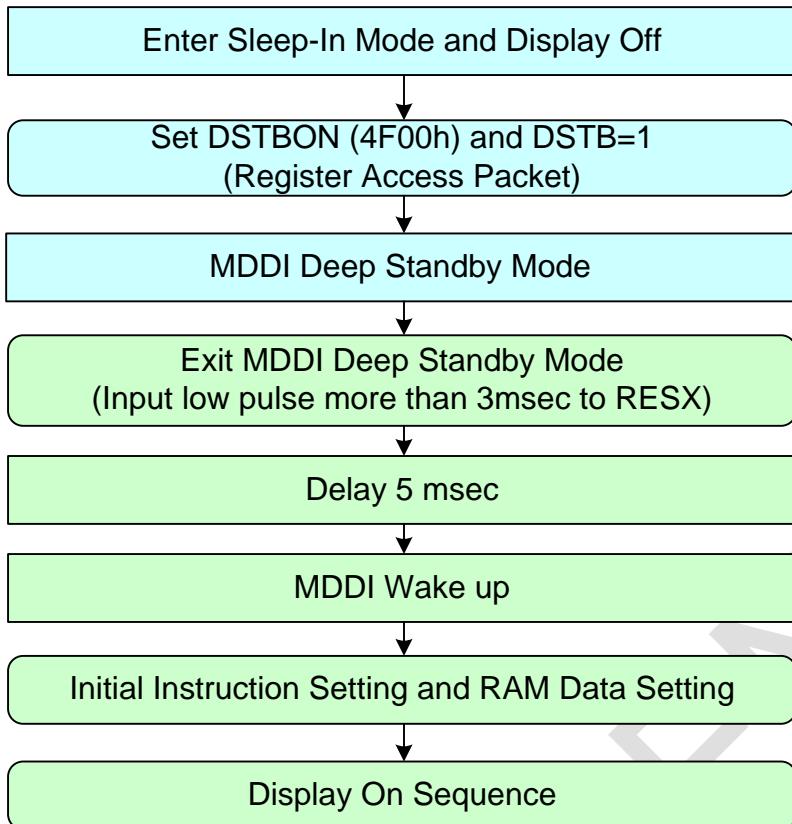
When in deep standby mode, instruction settings and RAM data are not stored, so they must be reset after Hibernation mode is cancelled.

Follow the sequence indicated in the VESA MDDI specifications when initiating or canceling the Hibernation mode.

State Transitions in MDDI Deep Standby Mode:



Note: When the RM69032 is in the MDDI Hibernation mode or MDDI deep standby mode, both links are in the link hibernation states.

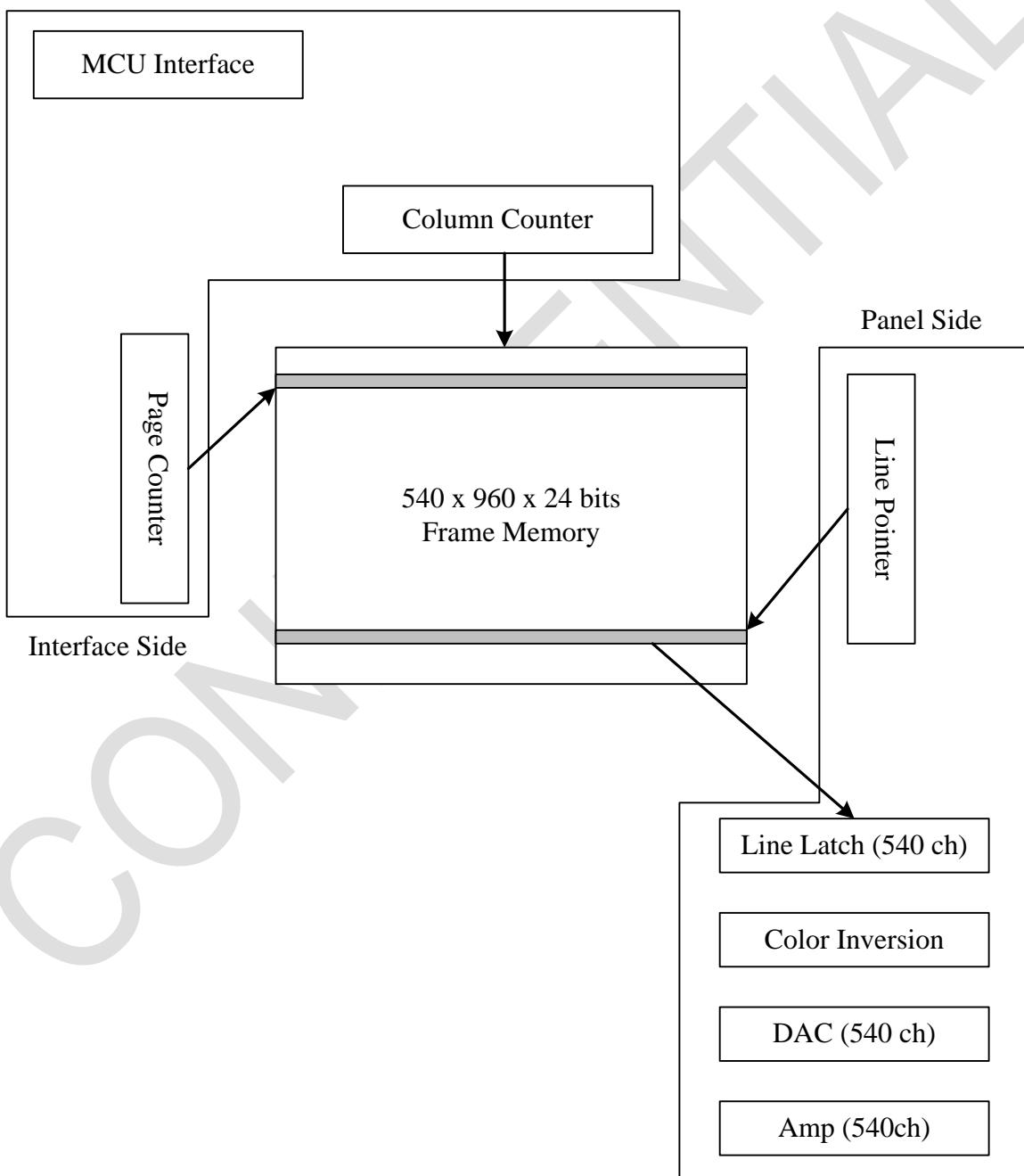
MDDI Deep Standby Mode Sequence

Note: When in MDDI Deep Standby mode, instruction settings and RAM data are not stored, so they must be reset after Hibernation mode is cancelled.

7.8 Display Data RAM

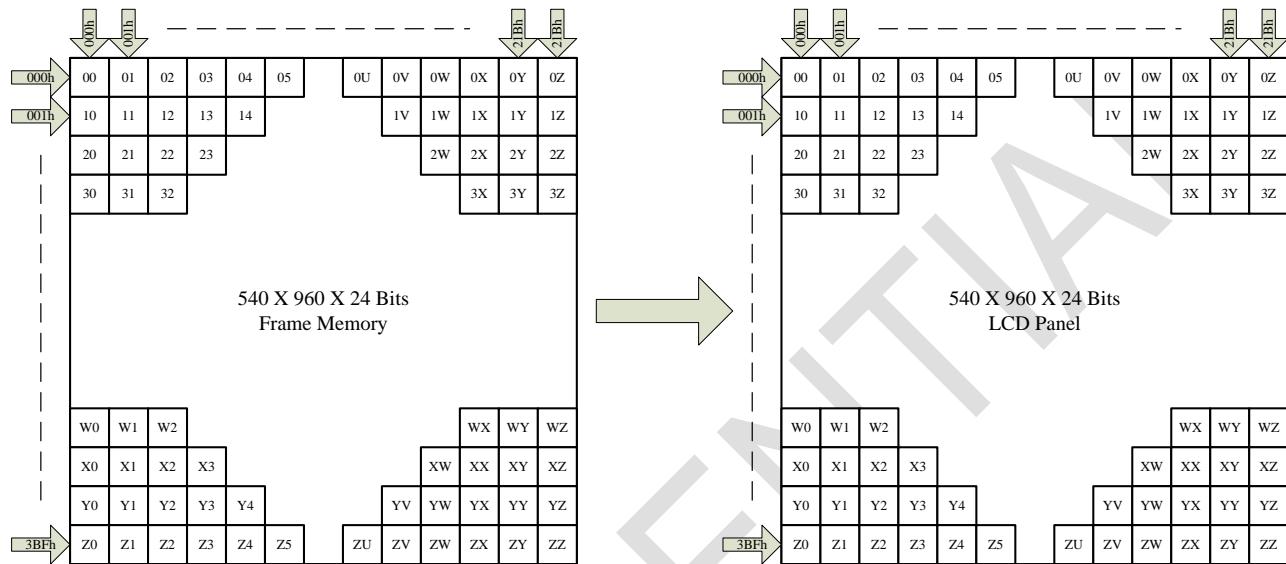
7.8.1 Configuration

The display data RAM stores display dots and consists of 12,441,600bits (540 x 24 x 960 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the frame memory.



7.8.2 Memory to Display Address Mapping

In this mode, content of the frame memory within an area where column pointer is 0000h to 021Bh and page pointer 0000h to 03BFh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0).

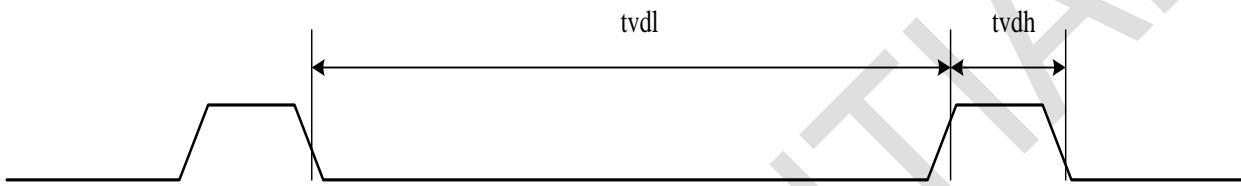


7.9 Tearing Effect Output

The tearing effect output line supplies to the MCU a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off (34h) and set_tear_on (35h) commands. The mode of the tearing effect signal is defined by the parameter of the set_tear_on (35h) and set_tear_scanline(44h) commands. The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

7.9.1 Tearing Effect Line Mode

Mode 1, the tearing effect output signal consist of V-sync information only:



tvdh = The LCD display is not updated from the frame memory.

tvdl = The LCD display is updated from the frame memory.

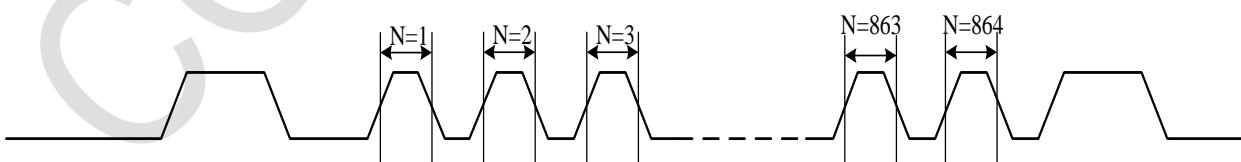
Mode 2, the tearing effect output signal consist of V-sync and H-sync information:



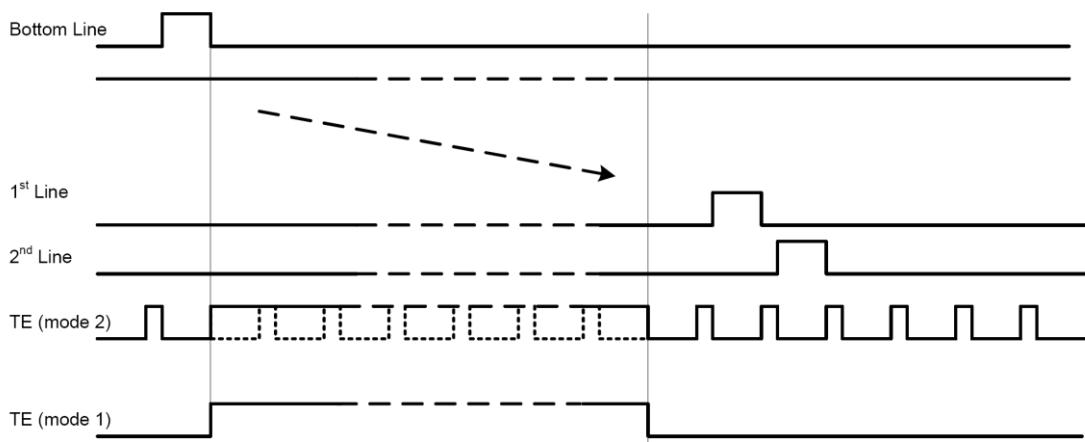
thdh = The LCD display is not updated from the frame memory.

thdl = The LCD display is updated from the frame memory.

Mode 3, this mode turn on the tearing effect output signal when vertical scanning reaches line N.



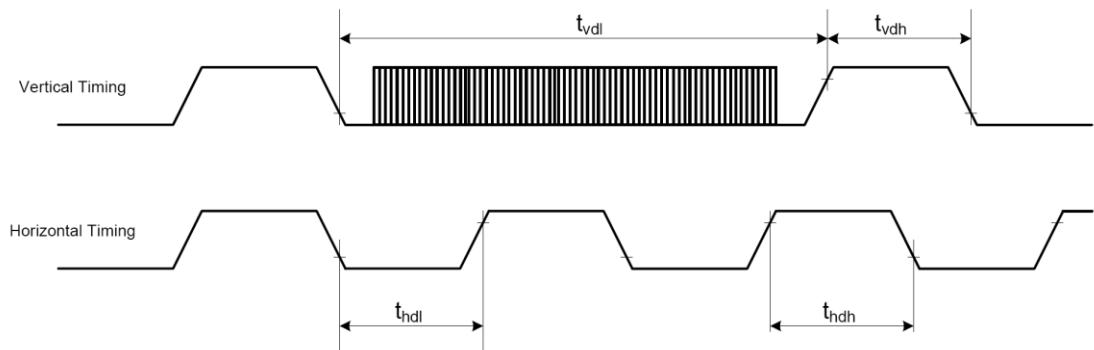
N = The N-th scanning line which set by register N[15:0] of command STESL(44h).



Note. During Sleep In mode, the tearing effect output signal is active low.

7.9.2 Tearing Effect Line Timing

The tearing effect signal is described as below:

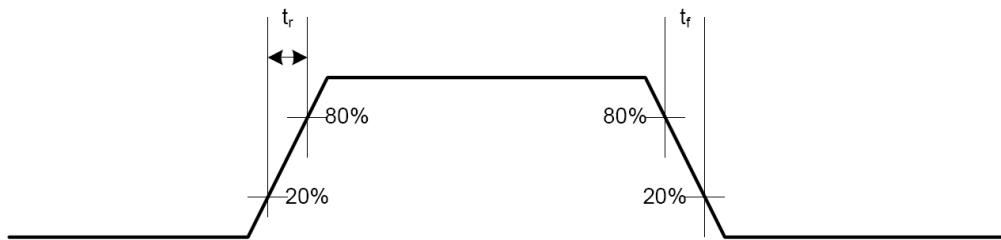


AC characteristics of Tearing Effect Signal (Frame Rate = 60.5Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
t_{vdL}	Vertical timing low duration	TBD		ms	
t_{vdH}	Vertical timing high duration	TBD		us	
t_{hdL}	Horizontal timing low duration	TBD		us	
t_{hdH}	Horizontal timing high duration	TBD		us	

Notes:

1. The timings apply when MADCTL B4=0 and B4=1
2. The signal's rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used as shown below to avoid tearing effect:

The Tearing Effect output line supplies to the MCU a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off(34h), set_tear_on(35h) commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command. The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

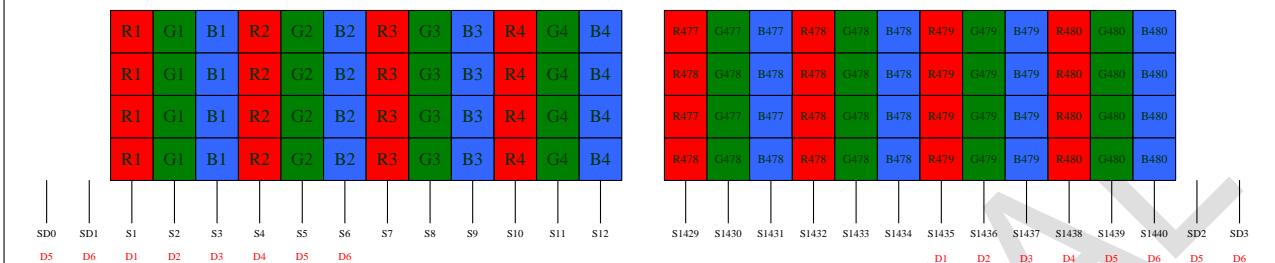
TEON (35h)	TELOM (35h, 1 st bit)	TE signal Output
0	*	GND
1	0	TE (Mode 1)
1	1	TE (Mode 2)

7.10 Panel Type

7.10.1 Normal Type

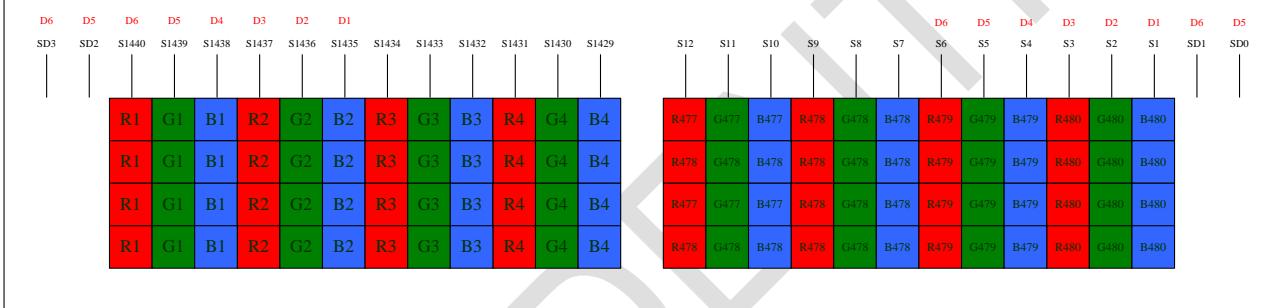
Bottom Side

normal (CTB=0, CRL=0, CRGB=0)

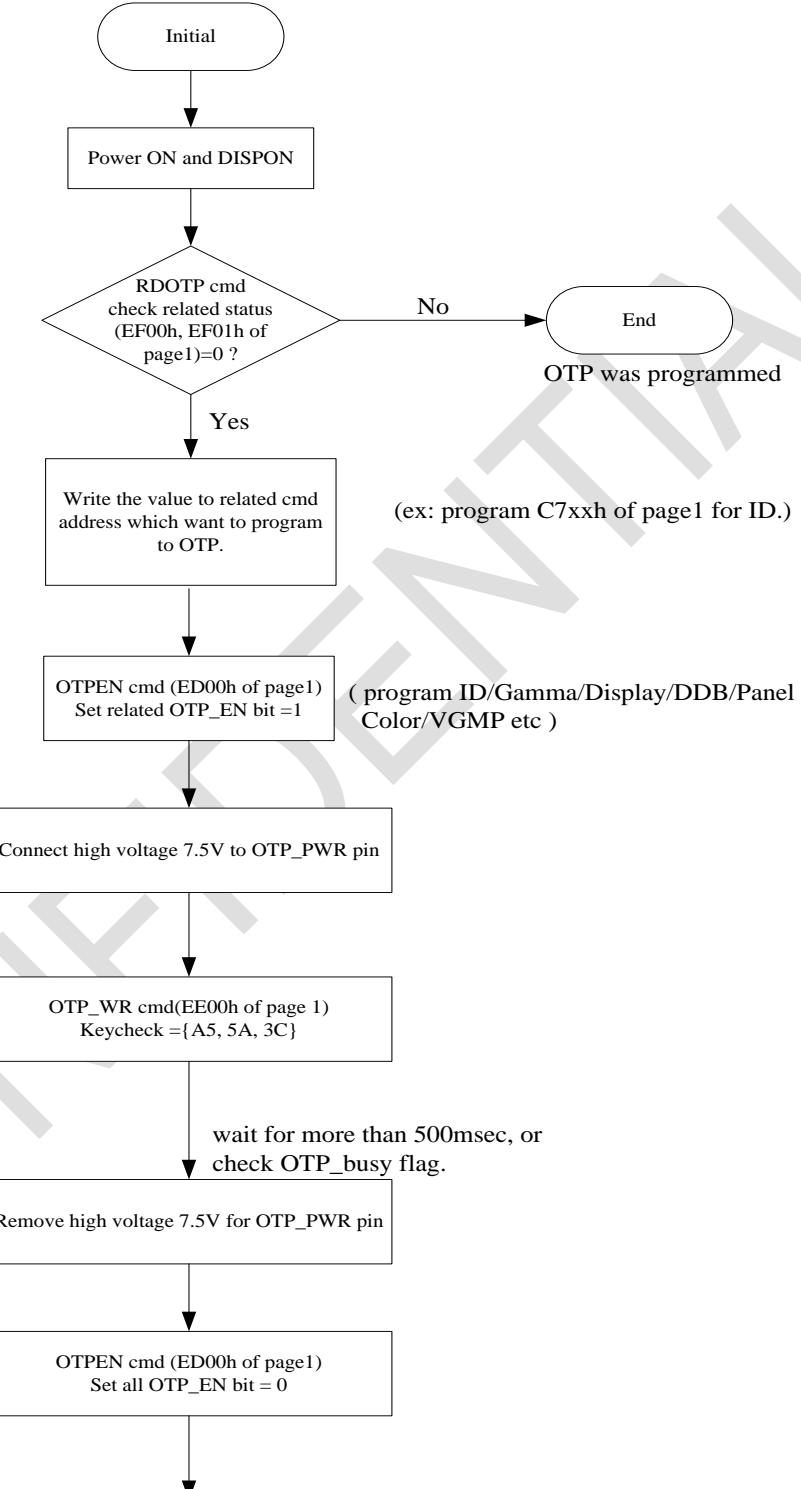


Upper Side

normal (CTB=0, CRL=1, CRGB=1)



7.11 OTP Program Sequence



OTP Programming Flow

8. Command

8.1. Command List

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number Of Parameter
00h	nop	C	0
01h	soft_reset	C	0
04h	get_display_ID	R	3
05h	get_DSI_err	R	1
0Ah	get_power_mode	R	1
0Bh	get_address_mode	R	1
0Ch	get_pixel_format	R	1
0Dh	get_display_mode	R	1
0Eh	get_signal_mode	R	1
0Fh	get_diagnostic_result	R	1
10h	enter_sleep_mode	C	0
11h	exit_sleep_mode	C	0
12h	enter_partial_mode	C	0
13h	enter_normal_mode	C	0
20h	exit_invert_mode	C	0
21h	enter_invert_mode	C	0
22h	set_all_pixel_off	C	0
23h	set_all_pixel_on	C	0
26h	Gamma_curve_setlect	W	1
28h	set_display_off	C	0
29h	set_display_on	C	0
2Ah	set_column_address	W	4
2Bh	set_page_address	W	4
2Ch	write_memory_start	W	Variable
2Eh	read_memory_start	R	Variable
30h	set_partial_area	W	4
34h	set_tear_off	C	0
35h	set_tear_on	W	1
36h	set_address_mode	W	1
38h	exit_idle_mode	C	0
39h	enter_idle_mode	C	0
3Ah	set_pixel_format	W	1
3Ch	write_memory_continue	W	Variable
3Eh	read_memory_continue	R	Variable
44h	set_tear_scanline	W	2
45h	get_scanline	R	2
4Fh	set_deep_standby_mode	W	1
50h	set_profile_value_for_display	W	16

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number Of Parameter
51h	set_display_brightness	W	1
52h	get_display_brightness	R	1
53h	set_control_display	W	1
54h	get_control_display	R	1
55h	set_cabc_mode	W	1
56h	get_cabc_mode	R	1
57h	set_hysteresis	W	32
58h	set_gamma_setting	W	8
5Ah	get_FS_value_MSBs	R	1
5Bh	get_FS_value_LSBs	R	1
5Ch	get_median_filter_FS_value_MSBs	R	1
5Dh	get_median_filter_FS_value_LSBs	R	1
5Eh	set_cabc_min_brightness	W	1
5Fh	get_cabc_min_brightness	R	1
65h	set_light_sensor_compensation_coefficient	W	2
66h	get_LSCC_MSBs	R	1
67h	get_LSCC_LSBs	R	1
70h	get_black/white low bit	R	1
71h	get_Bkx	R	1
72h	get_Bky	R	1
73h	get_Wx	R	1
74h	get_Wy	R	1
75h	get_red/green low bit	R	1
76h	get_Rx	R	1
77h	get_Ry	R	1
78h	get_Gx	R	1
79h	get_Gy	R	1
7Ah	get_blue/Acolor low bit	R	1
7Bh	get_Bx	R	1
7Ch	get_By	R	1
7Dh	get_Ax	R	1
7Eh	get_Ay	R	1
A1h	read_DDB_start	R	5
A8h	read_DDB_continue	R	5
AAh	read_first_checksum	R	1
AFh	read_continue_checksum	R	1
DAh	read_ID1	R	1
DBh	read_ID2	R	1
DCh	read_ID3	R	1

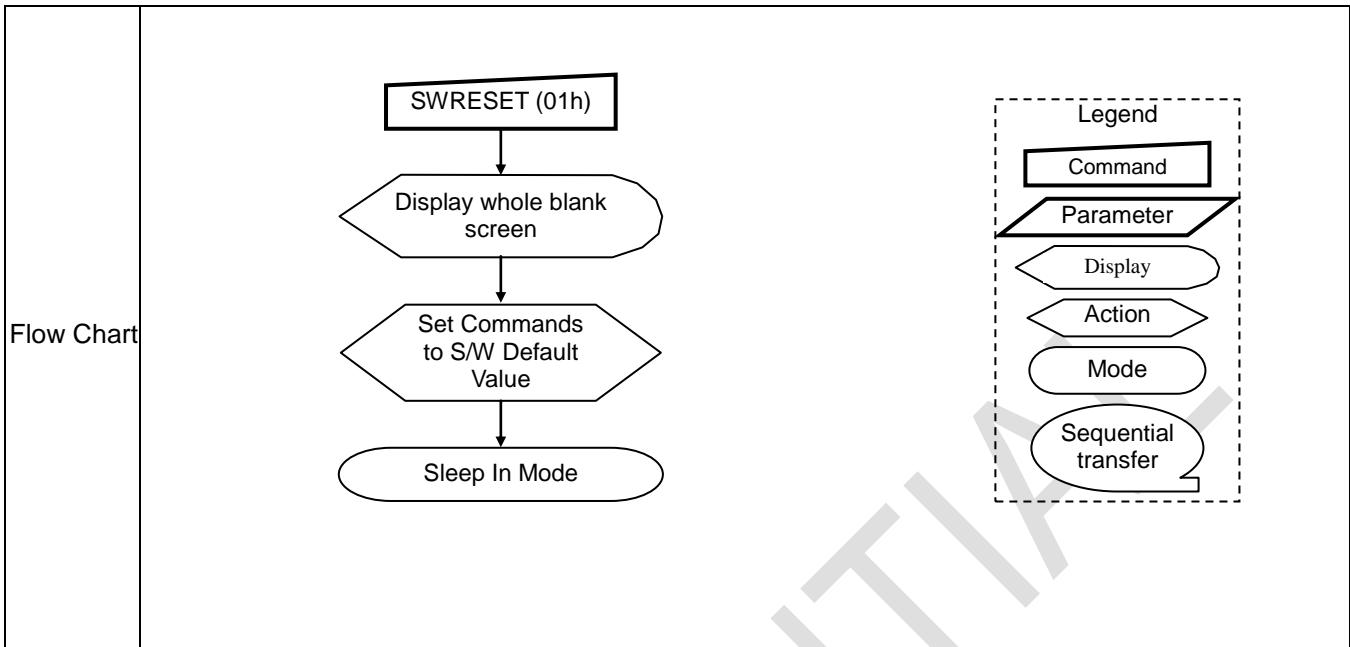
8.2. Command Description

NOP (0000h)

NOP (No Operation)																											
Inst/Para	R/W	Addresss		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
		MIP	Other																								
NOP	W	00h	0000h	No Argument																							
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X = Don't care.																										
Restriction	None																										
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes			
Status	Availability																										
Normal Mode On, Idle Mode Off, Sleep Out	Yes																										
Normal Mode On, Idle Mode On, Sleep Out	Yes																										
Partial Mode On, Idle Mode Off, Sleep Out	Yes																										
Partial Mode On, Idle Mode On, Sleep Out	Yes																										
Sleep In	Yes																										
Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></tbody></table>												Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A							
Status	Default Value																										
Power On Sequence	N/A																										
SW Reset	N/A																										
HW Reset	N/A																										
Flow Chart	None																										

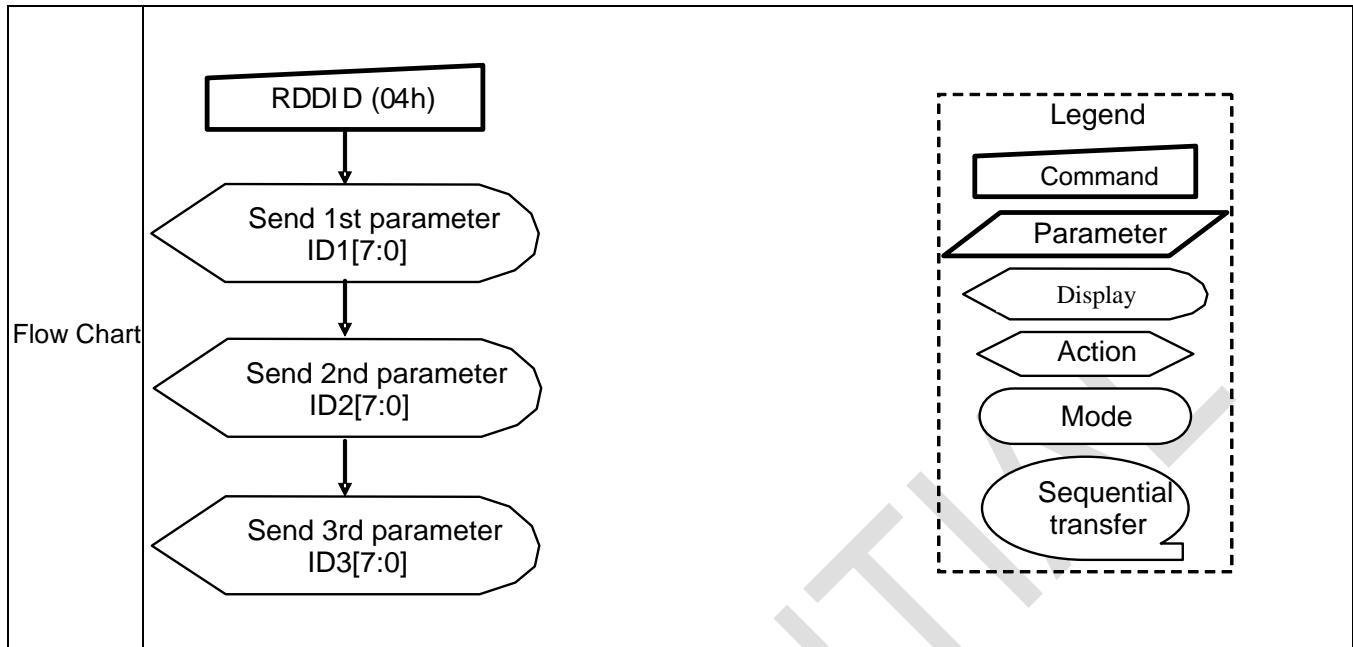
SWRESET(0100h) : Software Reset

0100H		SWRESET(Software Reset)																					
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX										
		MIPI	Other																				
SWRESET	W	01h	0100h	No Argument																			
Description	<p>When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)</p> <p>Note: The Frame Memory contents are affected by this command.</p> <p>X = Don't care</p>																						
Restriction	<p>Software Reset Command cannot be sent during Sleep Out sequence.</p> <p>Any new command is cannot be sent for 10-frame period until the RM69032 enters Sleep-In mode.</p> <p>Do not send any command.</p>																						
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
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Status	Default Value																						
Power On Sequence	N/A																						
SW Reset	N/A																						
HW Reset	N/A																						



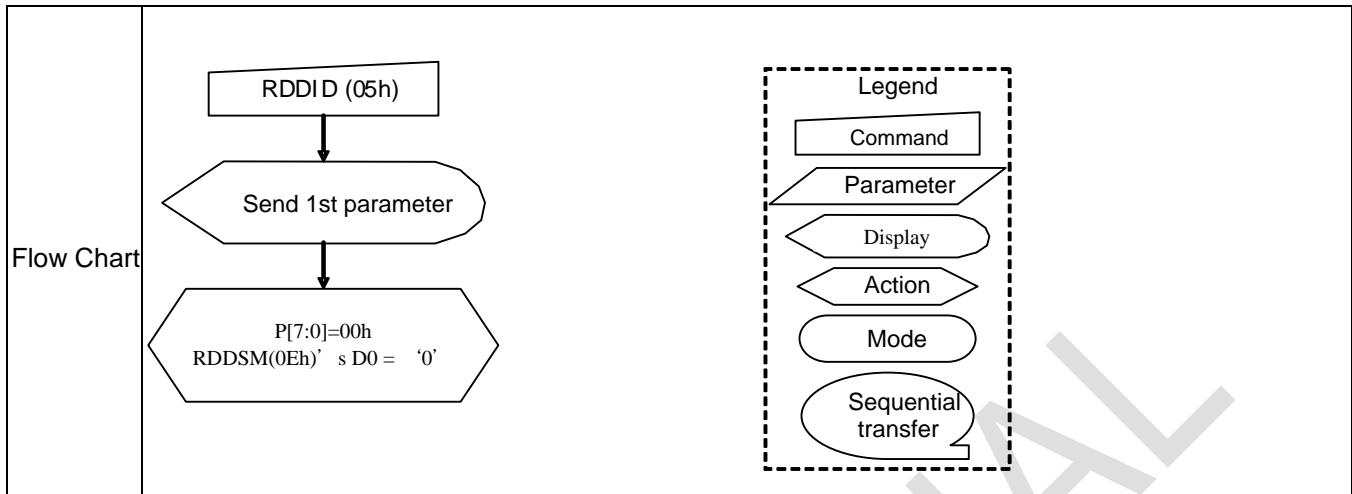
RDDID(0400h~0402h) : Read Display ID

Inst/Para	R/W	RDDID																													
		Adderss		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
		MIPI	Other																												
RDDID	R	04h	0400h	x	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	00																		
			0401h	x	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80																		
			0402h	x	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	00																		
Description	The 1 st parameter (ID1): the module's manufacture ID The 2 nd parameter (ID2): the module/driver version ID The 3 rd parameter (ID3): the module/driver ID Note: Commands RDID1/2/3 (DAh/DBh/DCh) read data correspond to the parameter 1, 2, 3 of command 04h, respectively.																														
Restriction	-																														
Register Availability	<table border="1"> <thead> <tr> <th colspan="2">Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td colspan="2">Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td colspan="2">Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td colspan="2">Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td colspan="2">Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td colspan="2">Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status		Availability	Normal Mode On, Idle Mode Off, Sleep Out		Yes	Normal Mode On, Idle Mode On, Sleep Out		Yes	Partial Mode On, Idle Mode Off, Sleep Out		Yes	Partial Mode On, Idle Mode On, Sleep Out		Yes	Sleep In		Yes
Status		Availability																													
Normal Mode On, Idle Mode Off, Sleep Out		Yes																													
Normal Mode On, Idle Mode On, Sleep Out		Yes																													
Partial Mode On, Idle Mode Off, Sleep Out		Yes																													
Partial Mode On, Idle Mode On, Sleep Out		Yes																													
Sleep In		Yes																													
<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th colspan="2">After MTP</th> <th>Before MTP</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td colspan="2">MTP value</td> <td>ID1=00h / ID2=80h / ID3=00h</td> </tr> <tr> <td>SW Reset</td> <td colspan="2">MTP value</td> <td>ID1=00h / ID2=80h / ID3=00h</td> </tr> <tr> <td>HW Reset</td> <td colspan="2">MTP value</td> <td>ID1=00h / ID2=80h / ID3=00h</td> </tr> </tbody> </table>													Status	Default Value			After MTP		Before MTP	Power On Sequence	MTP value		ID1=00h / ID2=80h / ID3=00h	SW Reset	MTP value		ID1=00h / ID2=80h / ID3=00h	HW Reset	MTP value		ID1=00h / ID2=80h / ID3=00h
Status	Default Value																														
	After MTP		Before MTP																												
Power On Sequence	MTP value		ID1=00h / ID2=80h / ID3=00h																												
SW Reset	MTP value		ID1=00h / ID2=80h / ID3=00h																												
HW Reset	MTP value		ID1=00h / ID2=80h / ID3=00h																												



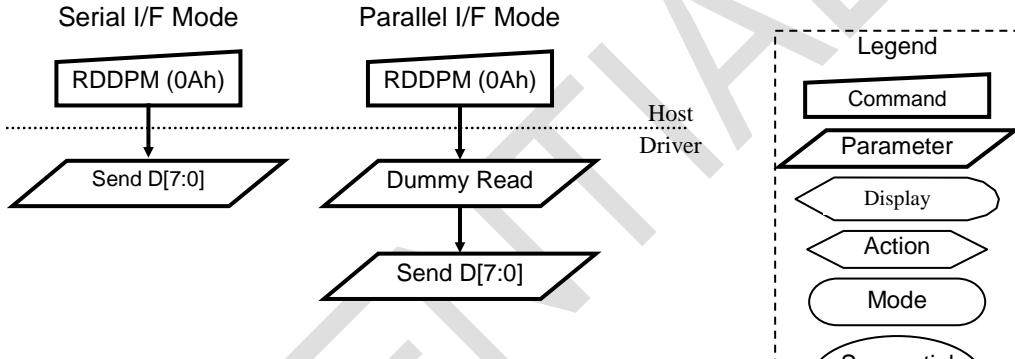
RDNUMED(0500h) : Read Number of Errors on DSI

		RDNUMED																						
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
		MIPI	Other																					
RDNUMED	R	05h	0500h	x	P7	P6	P5	P4	P3	P2	P1	P0	00											
Description	<p>The first parameter is telling a number of the parity errors on DSI. The more detailed description of the bits is below.</p> <p>P[6..0] bits are telling a number of the parity errors.</p> <p>P[7] is set to “1” if there is overflow with P[6..0] bits.</p> <p>P[7..0] bits are set to “0”’s (as well as RDDSM(0Eh)’s D0 are set “0” at the same time) after there is sent the first parameter information (= The read function is completed).</p> <p>This command is used for MIPI DSI only. It is no function for others interface operation.</p>																							
Restriction	-																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
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Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>SW Reset</td> <td>00h</td> </tr> <tr> <td>HW Reset</td> <td>00h</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	00h	SW Reset	00h	HW Reset	00h				
Status	Default Value																							
Power On Sequence	00h																							
SW Reset	00h																							
HW Reset	00h																							



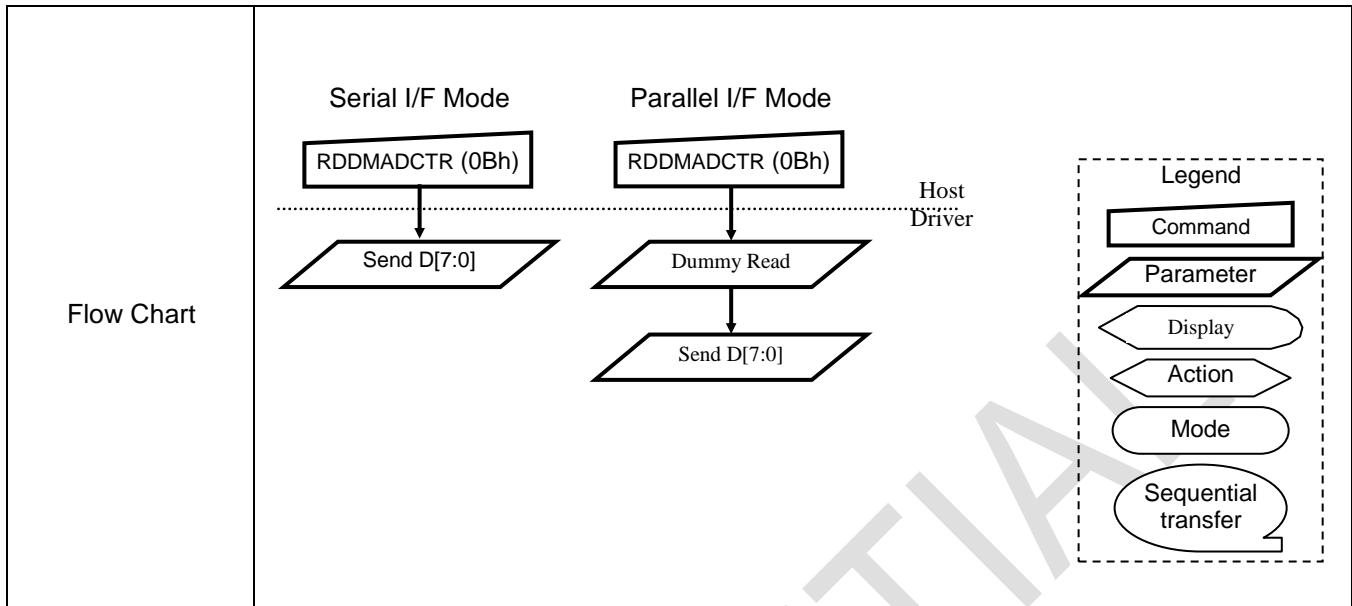
RDDPM (0A00h) : Read Display Power Mode

		RDDPM (Read Display Power Mode)																																														
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																			
		MIPI	Other																																													
RDDPM	R	0Ah	0A00h	x	D7	D6	D5	D4	D3	D2	D1	D0	08																																			
		This command indicates the current status of the display as described in the table below:																																														
Description	<table border="1"> <thead> <tr> <th>Bit</th> <th>Symbol</th> <th>Description</th> <th>Comment</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>BSTON</td> <td>Booster Voltage Status</td> <td>'1'=Booster on, '0'=Booster off</td> </tr> <tr> <td>D6</td> <td>IDMON</td> <td>Idle Mode On/Off</td> <td>'1' = Idle Mode On, '0' = Idle Mode Off</td> </tr> <tr> <td>D5</td> <td>PTLON</td> <td>Partial Mode On/Off</td> <td>'1' = Partial Mode On, '0' = Partial Mode Off</td> </tr> <tr> <td>D4</td> <td>SLPON</td> <td>Sleep In/Out</td> <td>'1' = Sleep Out, '0' = Sleep In</td> </tr> <tr> <td>D3</td> <td>NORON</td> <td>Display Normal Mode On/Off</td> <td>'1' = Normal Display, '0' = Partial Display</td> </tr> <tr> <td>D2</td> <td>DISON</td> <td>Display On/Off</td> <td>'1' = Display On, '0' = Display Off</td> </tr> <tr> <td>D1</td> <td>Reserved</td> <td></td> <td>0</td> </tr> <tr> <td>D0</td> <td>Reserved</td> <td></td> <td>0</td> </tr> </tbody> </table>												Bit	Symbol	Description	Comment	D7	BSTON	Booster Voltage Status	'1'=Booster on, '0'=Booster off	D6	IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off	D5	PTLON	Partial Mode On/Off	'1' = Partial Mode On, '0' = Partial Mode Off	D4	SLPON	Sleep In/Out	'1' = Sleep Out, '0' = Sleep In	D3	NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display	D2	DISON	Display On/Off	'1' = Display On, '0' = Display Off	D1	Reserved		0	D0	Reserved		0
Bit	Symbol	Description	Comment																																													
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Status	Default Value								
Power On Sequence	08h								
SW Reset	08h								
HW Reset	08h								
Default									
Flow Chart	<p style="text-align: center;">Host Driver</p> <p>Serial I/F Mode Parallel I/F Mode</p>  <pre>graph TD; RDDPM[RDDPM (0Ah)] --> SendD[Send D[7:0]]; RDDPM --> DummyRead[Dummy Read]; DummyRead --> SendD2[Send D[7:0]];</pre> <p>Legend</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer								

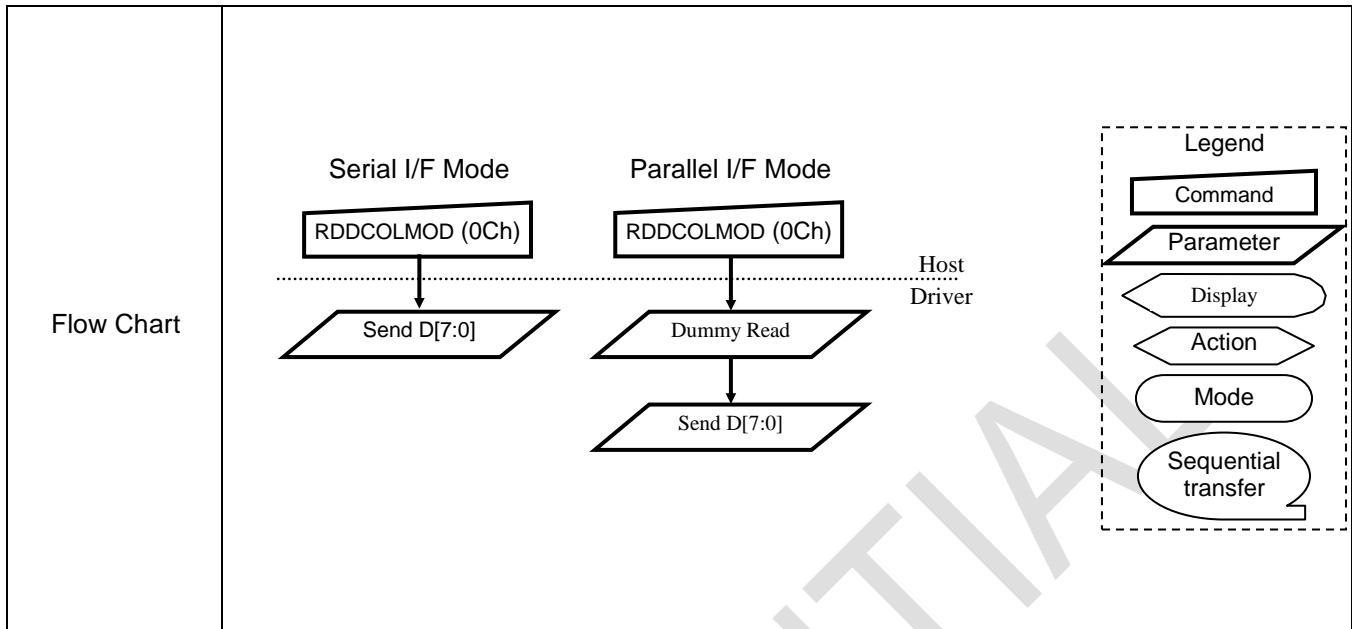
RDDMADCTR (0B00h): Read Display MADCTR

		RDDMADCTR (Read Display MADCTR)											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDMADCTR	R	0Bh	0B00h	x	D7	D6	D5	D4	D3	D2	D1	D0	00
		This command indicates the current status of the display as described in the table below:											
Description	Bit	Symbol	Description			Comment							
	D7	MY	Row Address Order			'1' = Bottom to Top (36H-D7='1') '0' = Top to Bottom (36H- D7='0')							
	D6	MX	Column Address Order			'1' = Right to Left (MADCTL D6='1') '0' = Left to Right (MADCTL D6='0')							
	D5	MV	Row/Column Order (MV)			'1' = Row/column exchange(36H-D5='1') '0' = Normal (36H-D5='1')							
	D4	ML	Vertical Refresh Order			'1' =LCD Refresh Top to Bottom '0' =LCD Refresh Bottom to Top							
	D3	RGB	RGB/BGR Order			'1' =BGR, "0"=RGB							
	D2	MH	Horizontal Refresh Order			'0' = LCD Refresh Left to Right '1' = LCD Refresh Right to Left							
	D1	RSMX	Horizontal Flip			'0' = Normal display(36H-D1='1') '1' = Flipped display(36H-D1='1')							
	D0	RSMY	Vertical Flip			'0' = Normal display(36H-D0='1') '1' = Flipped display(36H-D0='1')							
Register Availability													
			Status						Availability				
			Normal Mode On, Idle Mode Off, Sleep Out						Yes				
			Normal Mode On, Idle Mode On, Sleep Out						Yes				
			Partial Mode On, Idle Mode Off, Sleep Out						Yes				
			Partial Mode On, Idle Mode On, Sleep Out						Yes				
Default													
			Status						Default Value				
			Power On Sequence						00h				
			SW Reset						No Change				
		HW Reset						00h					



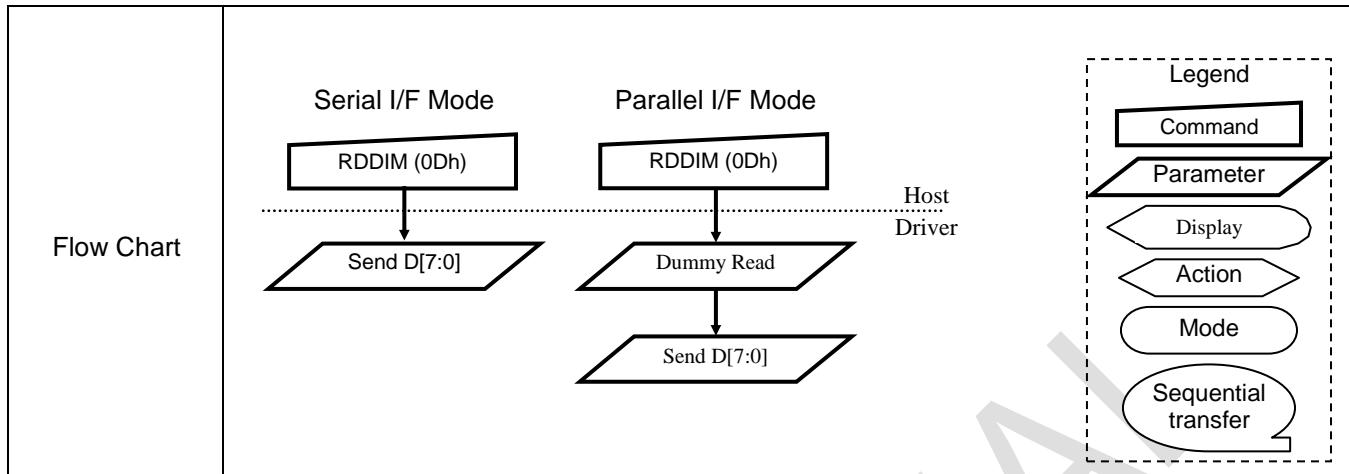
RDDCOLMOD (0C00h): Read Display Pixel Format

		RDDCOLMOD (Read Display Pixel Format)													
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
		MIPI	Other												
RDDCOLMOD	R	0Ch	0C00h	x	D7	D6	D5	D4	D3	D2	D1	D0	77		
Description	This command indicates the current status of the display as described in the table below:														
	Bit	Symbol	Description			Comment									
	D7	Reserved				'0'									
	D6	VIPF[2]	DPI Pixel Format(RGB Interface Color Format)			'101' = 16-bits / pixel, '110' = 18-bits / pixel, '111' = 24-bits / pixel, others are no define									
	D5	VIPF[1]													
	D4	VIPF[0]													
	D3	Reserved													
	D2	IFPF[2]	DBI Pixel Format(Control Interface Color Format)			'101' = 16-bits / pixel, '110' = 18-bits / pixel, '111' = 24-bits / pixel, others are no define									
	D1	IFPF[1]													
	D0	IFPF[0]													
Register Availability															
	Status						Availability								
	Normal Mode On, Idle Mode Off, Sleep Out						Yes								
	Normal Mode On, Idle Mode On, Sleep Out						Yes								
	Partial Mode On, Idle Mode Off, Sleep Out						Yes								
	Partial Mode On, Idle Mode On, Sleep Out						Yes								
Default															
	Status						Default Value								
	Power On Sequence						66h								
	SW Reset						No Change								
	HW Reset						66h								



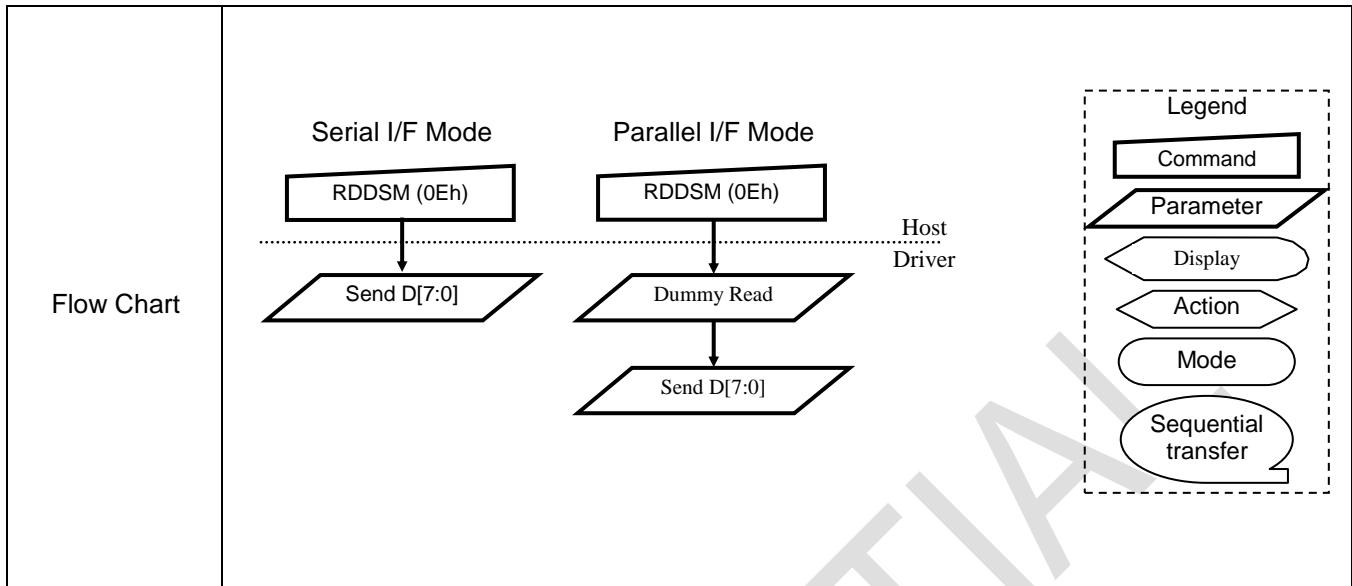
RDDIM (0D00h): Read Display Image Mode

		RDDIM (Read Display Image Mode)													
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
		MIPI	Other												
RDDIM	R	0Dh	0D00h	x	D7	D6	D5	D4	D3	D2	D1	D0	00		
Description	The display module returns the display image mode status.														
	Bit	Symbol	Description			Comment									
	D7	Reserved				'0'									
	D6	Reserved				'0'									
	D5	INVON	Inversion On/Off			'1' = Inversion is On, '0' = Inversion is Off									
	D4	ALLON	All Pixel On			'0' = Normal display '1' = White display									
	D3	ALLOFF	All Pixel Off			'0' = Normal display '1' = Black display									
Register Availability	D2~D0	GAMSET	Gamma Curve Selection			'000' = GC0, '001' = GC1 '010' = GC2, '011' = GC3									
	Status						Availability								
	Normal Mode On, Idle Mode Off, Sleep Out						Yes								
	Normal Mode On, Idle Mode On, Sleep Out						Yes								
	Partial Mode On, Idle Mode Off, Sleep Out						Yes								
	Partial Mode On, Idle Mode On, Sleep Out						Yes								
Default	Sleep In						Yes								
	Status						Default Value								
	Power On Sequence						00h								
	SW Reset						00h								
						HW Reset						00h			



RDDSM (0E00h): Read Display Signal Mode

		RDDSM (Read Display Signal Mode)																						
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
		MIPI	Other																					
RDDSM	R	0Eh	0E00h	x	D7	D6	D5	D4	D3	D2	D1	D0	00											
Description	The display module returns the Display Signal Mode.																							
	Bit	Symbol	Description			Comment																		
	D7	TEON	Tearing Effect Line On/Off			'1' = On, '0' = Off																		
	D6	TELOM	Tearing effect line mode			'0' = mode1, '1' = mode2																		
	D5	HS	Horizontal Sync On/Off			'0' = HS bit is 0 '1' = HS bit is 1																		
	D4	VS	Vertical Sync On/Off			'0' = VS bit is 0 '1' = VS bit is 1																		
	D3	PCLK	Pixel Clock On/Off			'0' = PCLK is Off '1' = PCLK is On																		
	D2	DE	Data Enable On/Off			'0' = DE is 0 '1' = DE is 1																		
	D1	Reserved				'0'																		
	D0	Error on DSI	Error on DSI			'0' = No Error '1' = Error																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
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Status	Default Value																							
Power On Sequence	00h																							
SW Reset	00h																							
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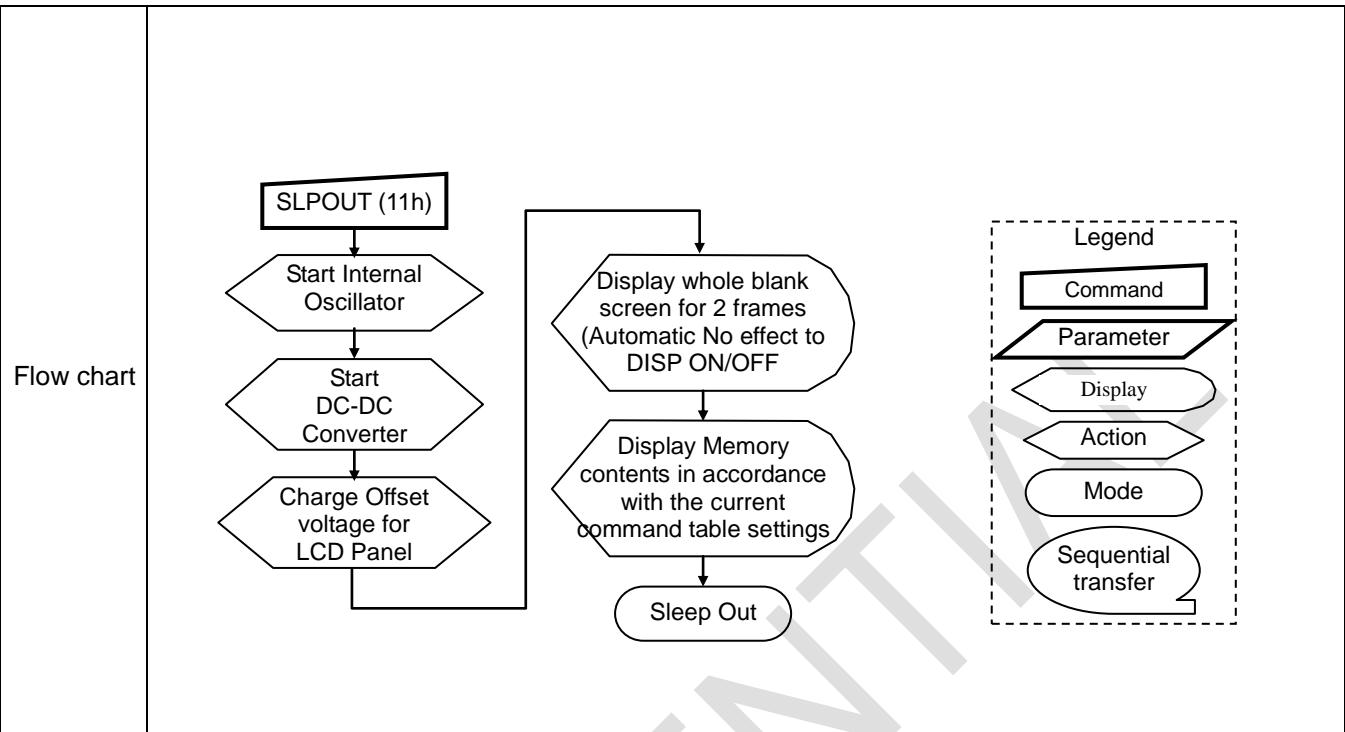
SLPIN (1000h): Sleep In

1000H		SLPIN (Sleep In)																						
Inst/Para	R/W	Adderss		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
		MIPi	Other																					
SLPIN	W	10h	1000h	No Argument																				
Description	<p>This command causes the display module to enter the minimum power consumption mode.</p> <p>In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.</p> <p>The control Interface such as memory and registers are still working and the memory keeps (RAMKP="1") or loses (RAMKP="0") its contents.</p> <p>After Sleep in command, user can send PCLK, HS and VS information on RGB I/F for blank display and this information is valid during 2 frames if there is used Normal Mode On in Sleep Out-mode.</p> <p>There is used an internal oscillator for blank display.</p>																							
Restriction	<p>This command has no effect when the display module is already in Sleep mode.</p> <p>Sleep In Mode can only be exit by the Sleep Out Command (11h).</p> <p>It must wait 5msec before sending next command for the supply voltages and clock circuits to stabilize.</p> <p>It must wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p>																							
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
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Sleep In	Yes																							

Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>SW Reset</td><td>Sleep In Mode</td></tr><tr><td>HW Reset</td><td>Sleep In Mode</td></tr></tbody></table>	Status	Default Value	Power On Sequence	Sleep In Mode	SW Reset	Sleep In Mode	HW Reset	Sleep In Mode
Status	Default Value								
Power On Sequence	Sleep In Mode								
SW Reset	Sleep In Mode								
HW Reset	Sleep In Mode								
<p>Flow Chart</p> <pre>graph TD; A[SPLIN (10h)] --> B{Display whole blank screen Automatic No effect to DISP ON/OFF Command}; B --> C{Drain charge from panel}; C --> D{Stop DC/DC Converter}; D --> E{Stop Internal Oscillator}; E --> F{Sleep In Mode}</pre> <p>Legend:</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer									

SLPOUT (1100h): Sleep Out

SLPOUT (Sleep Out)																																
Inst/Para	R/W	Adderss		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
		MIPI	Other																													
SLPOUT	W	11h	1100h	No Argument																												
Description	This command causes the display module to exit Sleep mode. All blocks inside the display module are enabled. The host processor sends PCLK, HS and VS information to display modules two frames before this command is sent when the display module is in Normal Mode.																															
Restriction	<p>This command shall not cause any visible effect on the display device when the display module is not in Sleep mode. The host processor must wait five milliseconds after sending this command before sending another command. This delay allows the supply voltages and clock circuits to stabilize.</p> <p>The host processor must wait 120 milliseconds after sending a Sleep Out command before sending a Sleep-In command. The display module loads the display module's default values to the registers when exiting the Sleep mode. There shall not be any abnormal visual effect on the display device when loading the registers if the factory default and register values are the same or when the display module is not in Sleep mode. The display module runs the self-diagnostic functions after this command is received.</p>																															
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																															
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Normal Mode On, Idle Mode On, Sleep Out	Yes																															
Partial Mode On, Idle Mode Off, Sleep Out	Yes																															
Partial Mode On, Idle Mode On, Sleep Out	Yes																															
Sleep In	Yes																															
Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>SW Reset</td><td>Sleep In Mode</td></tr><tr><td>HW Reset</td><td>Sleep In Mode</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Sleep In Mode	SW Reset	Sleep In Mode	HW Reset	Sleep In Mode											
Status	Default Value																															
Power On Sequence	Sleep In Mode																															
SW Reset	Sleep In Mode																															
HW Reset	Sleep In Mode																															



PTLON (1200h): Partial Display Mode On

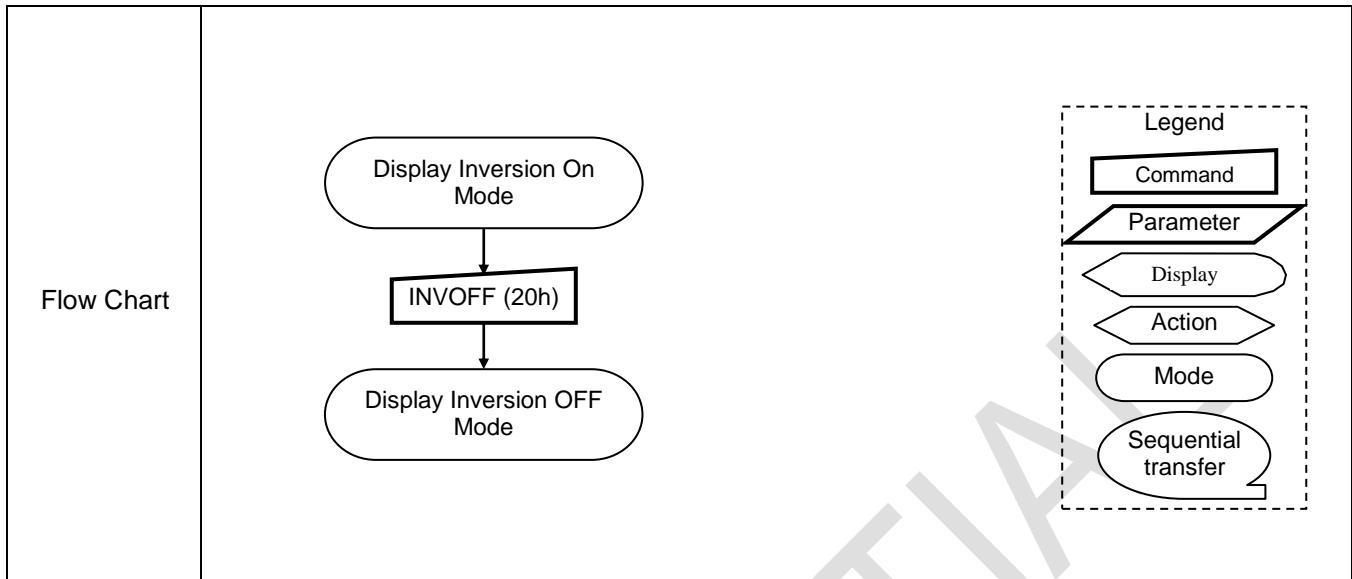
1200H		PTLON (Partial Display Mode On)																						
Inst/Para	R/W	Addresss		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
		MIPI	Other																					
PTLON	W	12h	1200h	No Argument																				
Description	<p>This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the Partial Area (30h) command.</p> <p>To leave Partial Display Mode, the Normal Display Mode On (13h) command should be written. The host processor continues to send PCLK, HS and VS information to display modules for two frames after this command is sent when the display module is in Normal Display Mode.</p>																							
Restriction	This command has no effect when Partial Display Mode is already active.																							
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Normal display mode On</td></tr><tr><td>SW Reset</td><td>Normal display mode On</td></tr><tr><td>HW Reset</td><td>Normal display mode On</td></tr></tbody></table>												Status	Default Value	Power On Sequence	Normal display mode On	SW Reset	Normal display mode On	HW Reset	Normal display mode On				
Status	Default Value																							
Power On Sequence	Normal display mode On																							
SW Reset	Normal display mode On																							
HW Reset	Normal display mode On																							
Flow Chart	Refer to Partial Area (30h)																							

NORON (1300h): Normal Display Mode On

1300H		NORON (Normal Display Mode On)																							
Inst/Para	R/W	Adderss		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
		MIPI	Other																						
NORON	W	13h	1300h	No Argument																					
Description	<p>This command causes the display module to enter the Normal mode. Normal Mode is defined as Partial Display mode .</p> <p>The host processor sends PCLK, HS and VS information to Type 2 display modules two frames before this command is sent when the display module is in Partial Display Mode.</p>																								
Restriction	This command has no effect when Normal Display mode is already active.																								
Register Availability		<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>SW Reset</td><td>Normal Display Mode On</td></tr><tr><td>HW Reset</td><td>Normal Display Mode On</td></tr></tbody></table>												Status	Default Value	Power On Sequence	Normal Display Mode On	SW Reset	Normal Display Mode On	HW Reset	Normal Display Mode On					
Status	Default Value																								
Power On Sequence	Normal Display Mode On																								
SW Reset	Normal Display Mode On																								
HW Reset	Normal Display Mode On																								
Flow Chart	Refer to the description of Partial Area (3000h)																								

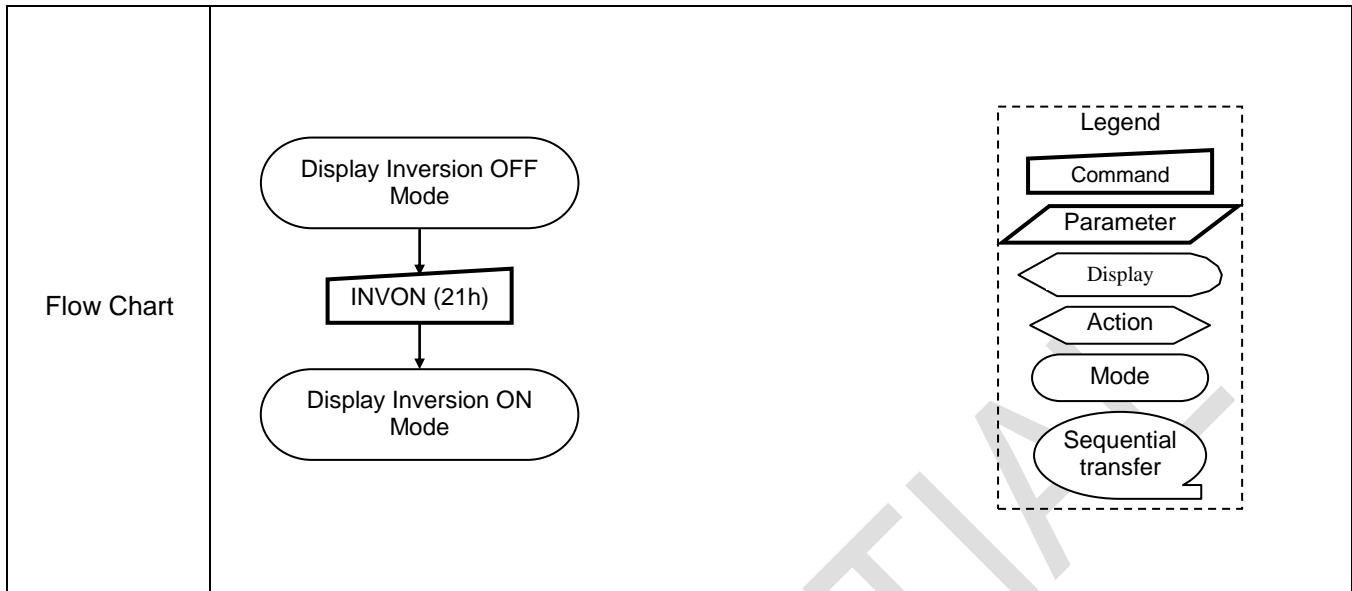
INVOFF (2000H): Display Inversion Off

2000H		INVOFF (Display Inversion Off)																						
Inst/Para	R/W	Adders		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
		MIPI	Other																					
INVOFF	W	20h	2000h	No Argument																				
Description	This command causes the display module to stop inverting the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.																							
Restriction	This command has no effect when the display module is not inverting the display image.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
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Status	Default Value																							
Power On Sequence	Display Inversion off																							
SW Reset	Display Inversion off																							
HW Reset	Display Inversion off																							

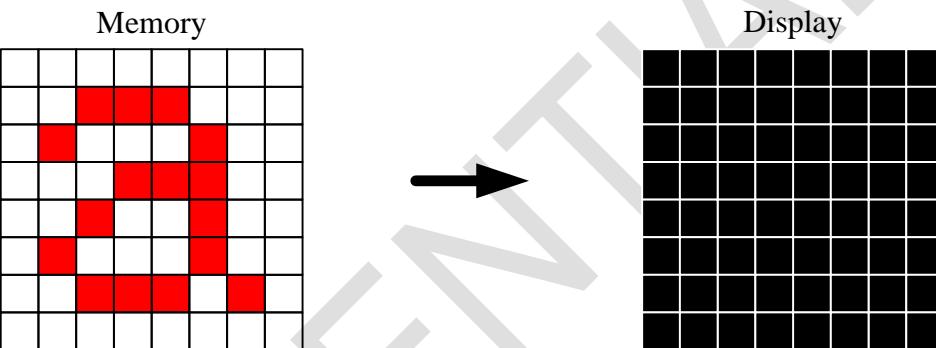


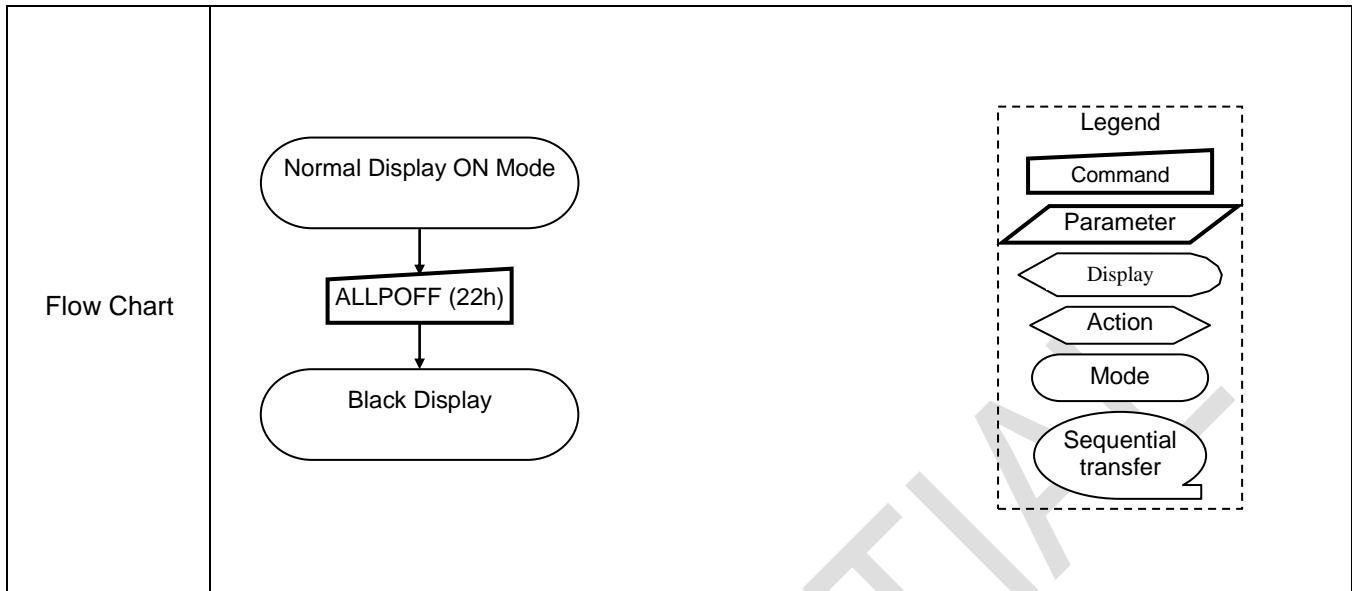
INVON (2100H): Display Inversion On

2100H		INVON (Display Inversion On)																							
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
		MIPI	Other																						
INVON	W	21h	2100h	No Argument																					
Description	This command causes the display module to invert the image data only on the display device. The frame memory contents remain unchanged. No status bits are changed.																								
Restriction	This command has no effect when module is already in inversion on mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
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Status	Default Value																								
Power On Sequence	Display Inversion off																								
SW Reset	Display Inversion off																								
HW Reset	Display Inversion off																								

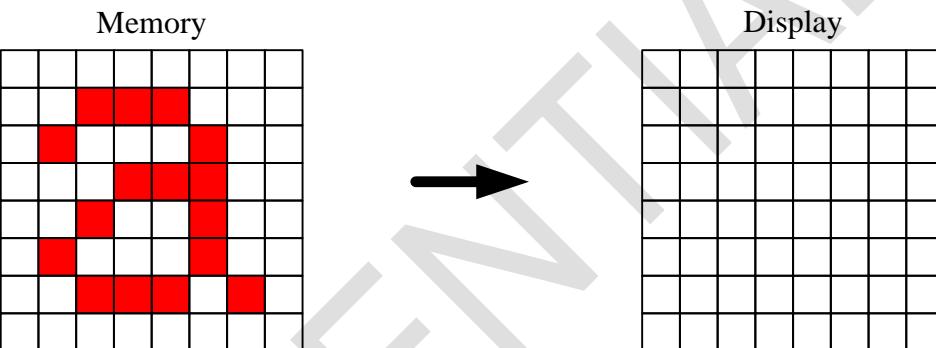


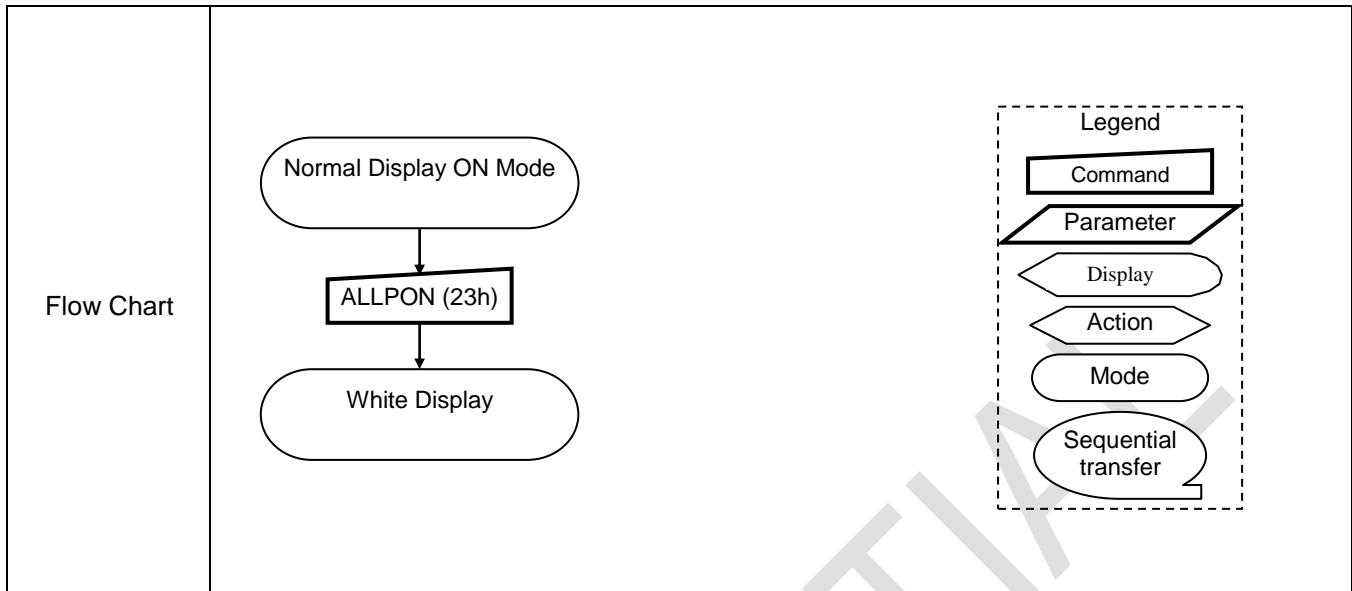
ALLPOFF (2200H): All Pixel Off

2200H		ALLPOFF																							
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
		MIPI	Other																						
ALLPOFF	W	22h	2200h	No Argument																					
Description	This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off. This command makes no change of contents of frame memory. This command does not change any other status.  "All Pixels On", "Normal Display Mode On" or "Partial Mode On" commands are used to leave this mode. The display panel is showing the content of the frame memory after "Normal Display On" and "Partial Mode On" commands.																								
Restriction	-																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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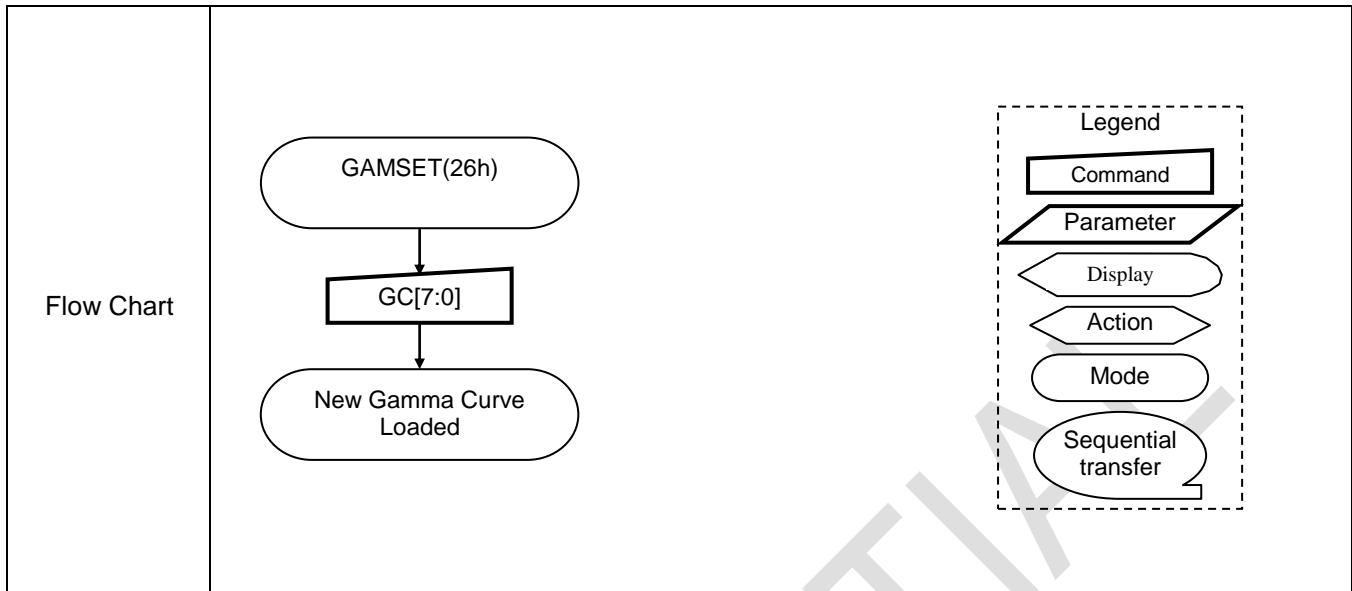
ALLPON (2300H): All Pixel On

2300H		ALLPON																						
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
		MIPI	Other																					
ALLPON	W	23h	2300h	No Argument																				
Description		<p>This command turns the display panel white in Sleep Out mode and a status of the Display On/Off register can be on or off.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p> 																						
		<p>"All Pixels Off", "Normal Display Mode On" or "Partial Mode On" commands are used to leave this mode. The display panel is showing the content of the frame memory after "Normal Display On" and "Partial Mode On" commands.</p>																						
		Restriction																						
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Status	Default Value																							
Power On Sequence	Display Inversion off																							
SW Reset	Display Inversion off																							
HW Reset	Display Inversion off																							

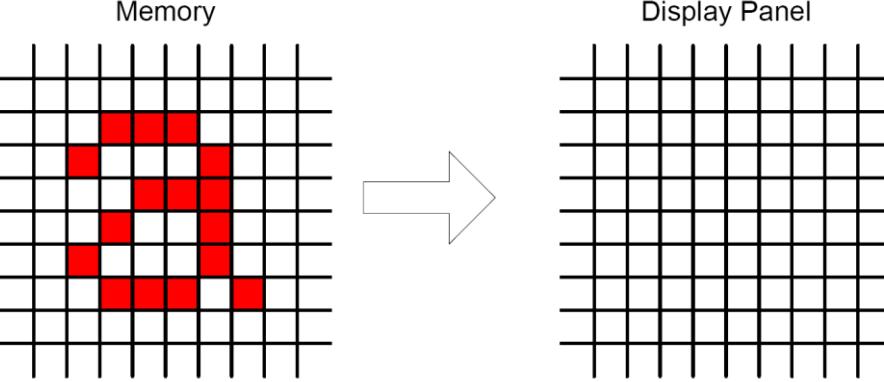


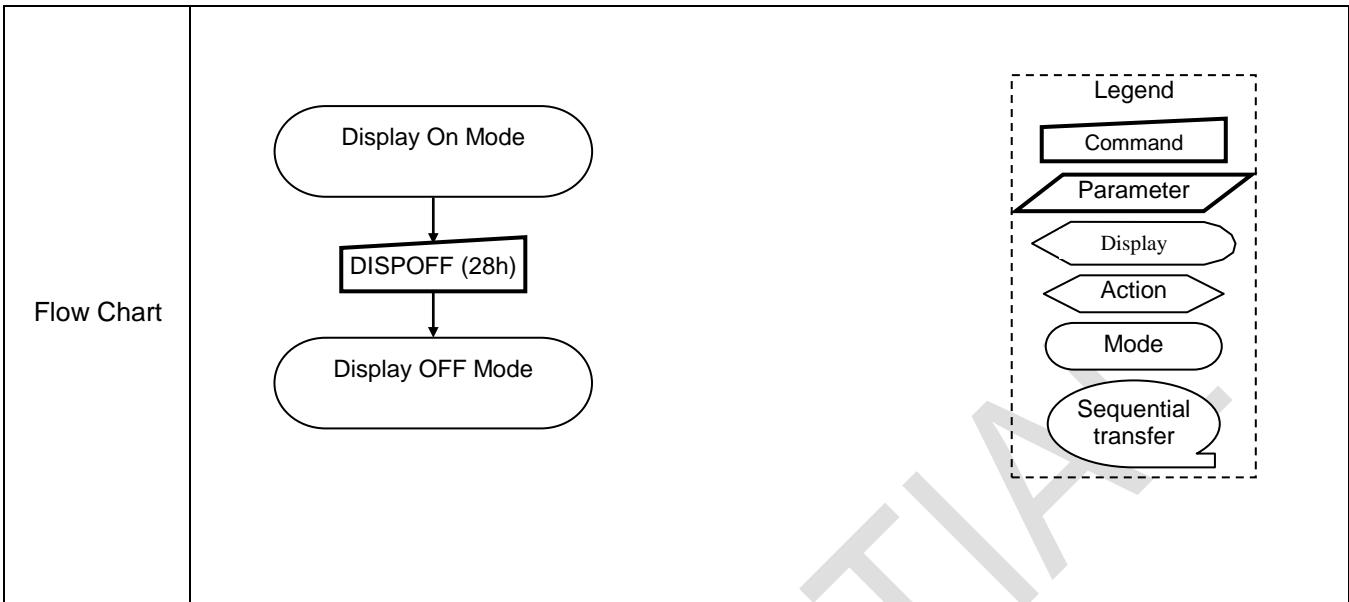
GAMSET (2600H): Gamma Set

GAMSET																																
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
		MIPI	Other																													
GAMSET	W	26h	2600h	X	GC[7:0]					01																						
Description	This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.																															
	<table border="1"><thead><tr><th>GC[7:0]</th><th>Parameter</th><th>Curve</th></tr></thead><tbody><tr><td>01h</td><td>GC0</td><td>Gamma Curve (G2.2)</td></tr><tr><td>02h</td><td>GC1</td><td>Reserved</td></tr><tr><td>04h</td><td>GC2</td><td>Reserved</td></tr><tr><td>08h</td><td>GC3</td><td>Reserved</td></tr></tbody></table>												GC[7:0]	Parameter	Curve	01h	GC0	Gamma Curve (G2.2)	02h	GC1	Reserved	04h	GC2	Reserved	08h	GC3	Reserved					
GC[7:0]	Parameter	Curve																														
01h	GC0	Gamma Curve (G2.2)																														
02h	GC1	Reserved																														
04h	GC2	Reserved																														
08h	GC3	Reserved																														
Note: All other values are undefined.																																
Restriction Values of GC [7:0] not shown in table above are invalid and will not change the current selected gamma																																
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr><tr><td> </td><td> </td></tr><tr><td> </td><td> </td></tr><tr><td> </td><td> </td></tr><tr><td> </td><td> </td></tr></tbody></table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes								
Status	Availability																															
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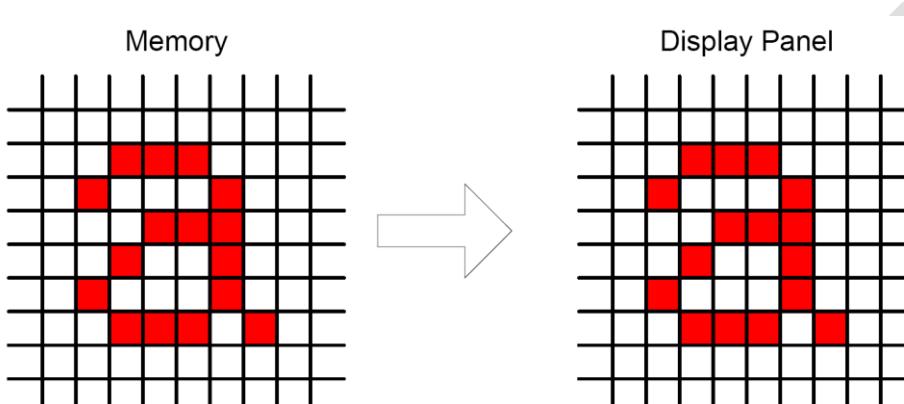


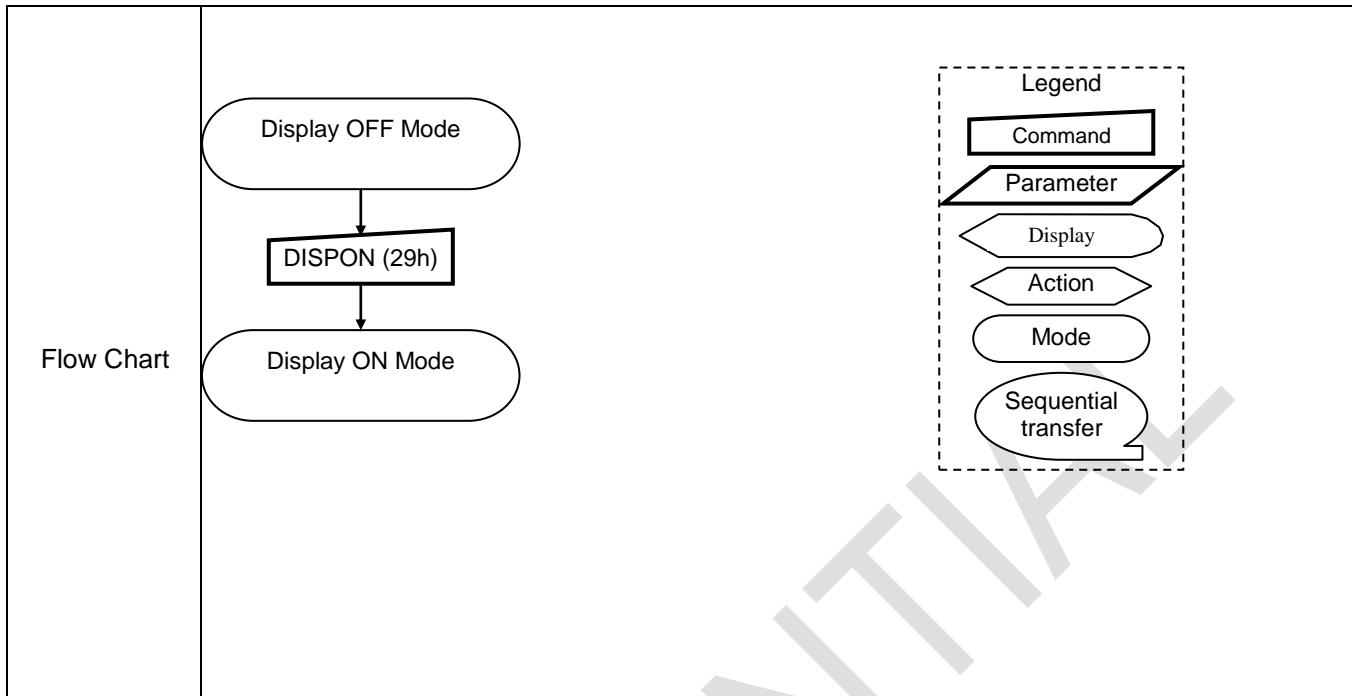
DISPOFF (2800h): Display Off

2800H		DISPOFF (Display Off)																							
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
		MIPI	Other																						
DISPOFF	W	28h	2800h	No Argument																					
Description	<p>This command causes the display module to stop displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.</p> 																								
Restriction	This command has no effect when module is already in display off mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	Display Off																								
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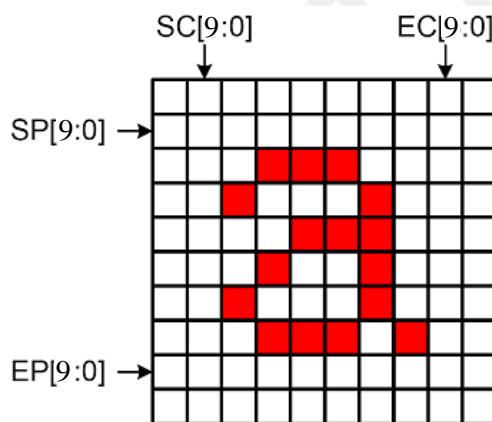
DISPON (2900h): Display On

2900H		DISPON (Display On)																							
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
		MIPI	Other																						
DISPON	W	29h	2900h	No Argument																					
Description	This command causes the display module to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.																								
																									
Restriction	This command has no effect when module is already in display on mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Power On Sequence	Display Off																								
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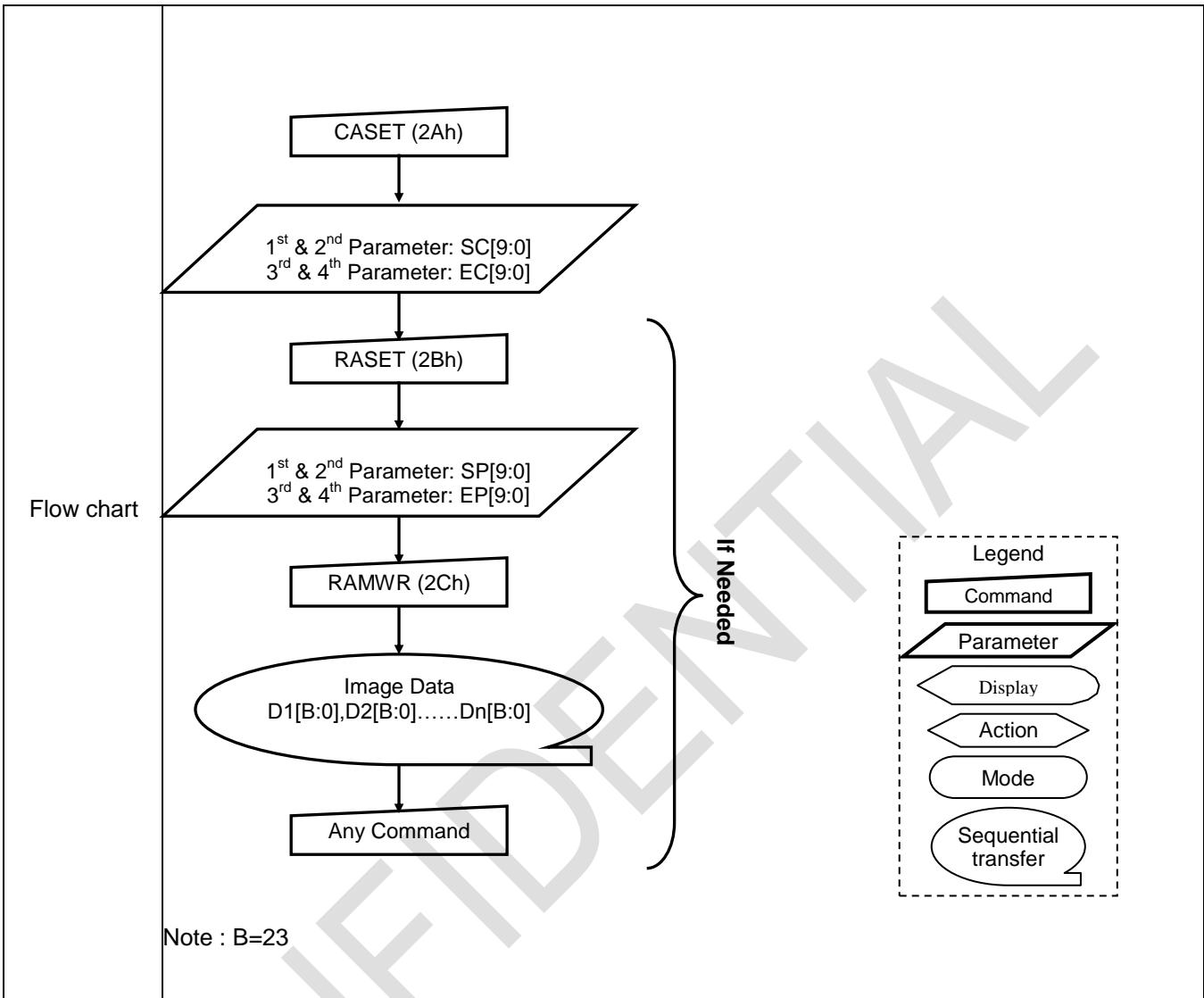


CASET (2A00h~2A03h): Column Address Set

Inst/Para	R/W	CASET (Column Address Set)											
		Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CASET	W	2Ah	2A00h	x	0	0	0	0	0	SC9	SC8	00	
			2A01h	x	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00
			2A02h	x	0	0	0	0	0	EC9	EC8	-	-
			2A03h	x	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	-
Description	This command defines the column extent of the frame memory accessed by the host processor with the read_memory_continue and write_memory_continue commands.												

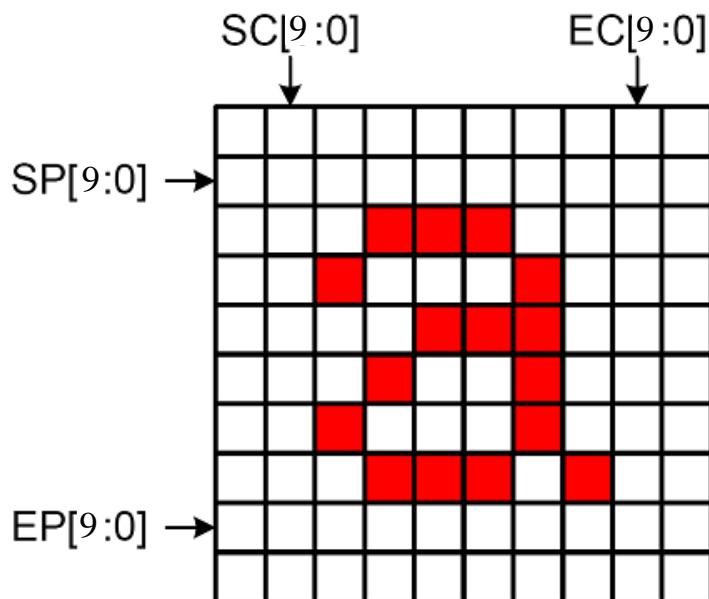


Restriction	<p>SC[9:0] always must be equal to or less than EC[9:0]</p> <p>When SC[9:0] or EC[9:0] is greater than maximum address like below, data of out of range will be ignored.</p> <p>For CGM[2:0] = "000" (540 x 960 resolution)</p> <p>MV = "0": Parameter range $0 \leq SC[9:0] \leq EC[9:0] \leq 539$ (021Bh)</p> <p>MV = "1": Parameter range $0 \leq SC[9:0] \leq EC[9:0] \leq 959$ (03BFh)</p> <p>For CGM[2:0] = "100" (480 x 960 resolution)</p> <p>MV = "0": Parameter range $0 \leq SC[9:0] \leq EC[9:0] \leq 479$ (01DFh)</p> <p>MV = "1": Parameter range $0 \leq SC[9:0] \leq EC[9:0] \leq 959$ (03BFh)</p> <p>For CGM[2:0] = "101" (480 x 864 resolution)</p> <p>MV = "0": Parameter range $0 \leq SC[9:0] \leq EC[9:0] \leq 479$ (01DFh)</p> <p>MV = "1": Parameter range $0 \leq SC[9:0] \leq EC[9:0] \leq 863$ (035Fh)</p> <p>For CGM[2:0] = "110" (480 x 854 resolution)</p> <p>MV = "0": Parameter range $0 \leq SC[9:0] \leq EC[9:0] \leq 479$ (01DFh)</p> <p>MV = "1": Parameter range $0 \leq SC[9:0] \leq EC[9:0] \leq 853$ (0355h)</p> <p>For CGM[2:0] = "111" (480 x 800 resolution)</p> <p>MV = "0": Parameter range $0 \leq SC[9:0] \leq EC[9:0] \leq 479$ (01DFh)</p> <p>MV = "1": Parameter range $0 \leq SC[9:0] \leq EC[9:0] \leq 799$ (031Fh)</p>														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes		
Status	Availability														
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Partial Mode On, Idle Mode Off, Sleep Out	Yes														
Partial Mode On, Idle Mode On, Sleep Out	Yes														
Sleep In	Yes														
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th><th colspan="2">Default Value</th></tr> <tr> <th>SC[8:0]</th><th>EC[8:0](36h-B5=0)</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>0000h</td><td>01DFh</td></tr> <tr> <td>SW Reset</td><td>0000h</td><td>01DFh</td></tr> <tr> <td>HW Reset</td><td>0000h</td><td>01DFh</td></tr> </tbody> </table>	Status	Default Value		SC[8:0]	EC[8:0](36h-B5=0)	Power On Sequence	0000h	01DFh	SW Reset	0000h	01DFh	HW Reset	0000h	01DFh
Status	Default Value														
	SC[8:0]	EC[8:0](36h-B5=0)													
Power On Sequence	0000h	01DFh													
SW Reset	0000h	01DFh													
HW Reset	0000h	01DFh													

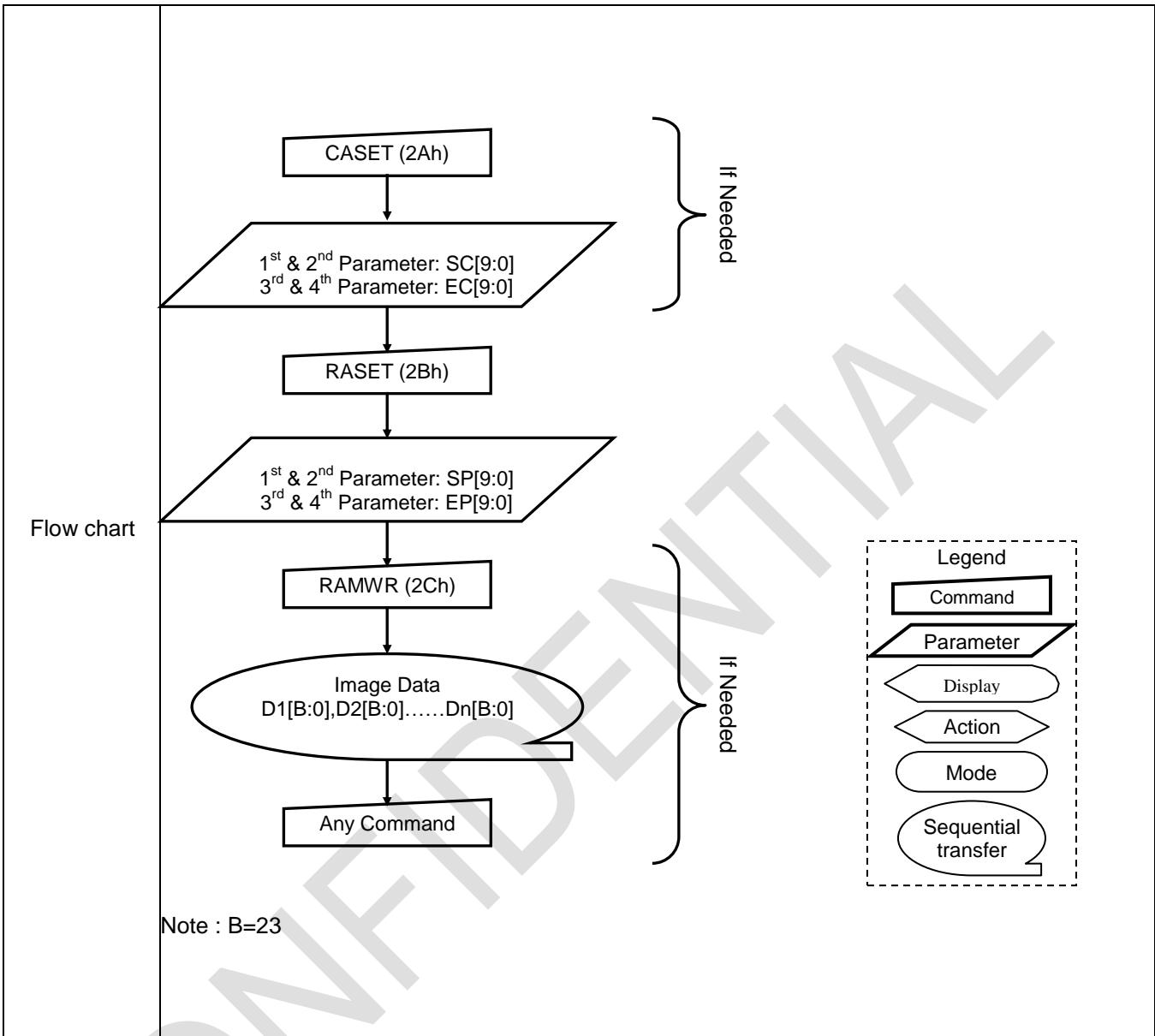


RASET (2B00h): Row Address Set

Inst/Para	R/W	RASET (Row Address Set)											
		Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RASET	W	MIPI	Other	2B00h	x	0	0	0	0	0	SP9	SP8	00
		2B01h	x	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	00	
		2B02h	x	0	0	0	0	0	0	0	EP9	EP8	-
		2B03h	x	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0		-
Description	This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command.												



Restriction	<p>SP[9:0] always must be equal to or less than EP[9:0]</p> <p>When SP[9:0] or EP[9:0] is greater than maximum address like below, data of out of range will be ignored.</p> <p>For CGM[2:0] = "000" (540 x 960 resolution)</p> <p>MV = "0": Parameter range $0 \leq SP[9:0] \leq EP[9:0] \leq 959$ (03BFh)</p> <p>MV = "1": Parameter range $0 \leq SP[9:0] \leq EP[9:0] \leq 539$ (021Bh)</p> <p>For CGM[2:0] = "100" (480 x 960 resolution)</p> <p>MV = "0": Parameter range $0 \leq SP[9:0] \leq EP[9:0] \leq 959$ (03BFh)</p> <p>MV = "1": Parameter range $0 \leq SP[9:0] \leq EP[9:0] \leq 479$ (01DFh)</p> <p>For CGM[2:0] = "101" (480 x 864 resolution)</p> <p>MV = "0": Parameter range $0 \leq SP[9:0] \leq EP[9:0] \leq 863$ (035Fh)</p> <p>MV = "1": Parameter range $0 \leq SP[9:0] \leq EP[9:0] \leq 479$ (01DFh)</p> <p>For CGM[2:0] = "110" (480 x 854 resolution)</p> <p>MV = "0": Parameter range $0 \leq SP[9:0] \leq EP[9:0] \leq 853$ (0355h)</p> <p>MV = "1": Parameter range $0 \leq SP[9:0] \leq EP[9:0] \leq 479$ (01DFh)</p> <p>For CGM[2:0] = "111" (480 x 800 resolution)</p> <p>MV = "0": Parameter range $0 \leq SP[9:0] \leq EP[9:0] \leq 799$ (031Fh)</p> <p>MV = "1": Parameter range $0 \leq SP[9:0] \leq EP[9:0] \leq 479$ (01DFh)</p>														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes		
Status	Availability														
Normal Mode On, Idle Mode Off, Sleep Out	Yes														
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Sleep In	Yes														
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th><th colspan="2">Default Value</th></tr> <tr> <th>SC[8:0]</th><th>EC[8:0](36h-B5=0)</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>0000h</td><td>031Fh</td></tr> <tr> <td>SW Reset</td><td>0000h</td><td>031Fh</td></tr> <tr> <td>HW Reset</td><td>0000h</td><td>031Fh</td></tr> </tbody> </table>	Status	Default Value		SC[8:0]	EC[8:0](36h-B5=0)	Power On Sequence	0000h	031Fh	SW Reset	0000h	031Fh	HW Reset	0000h	031Fh
Status	Default Value														
	SC[8:0]	EC[8:0](36h-B5=0)													
Power On Sequence	0000h	031Fh													
SW Reset	0000h	031Fh													
HW Reset	0000h	031Fh													



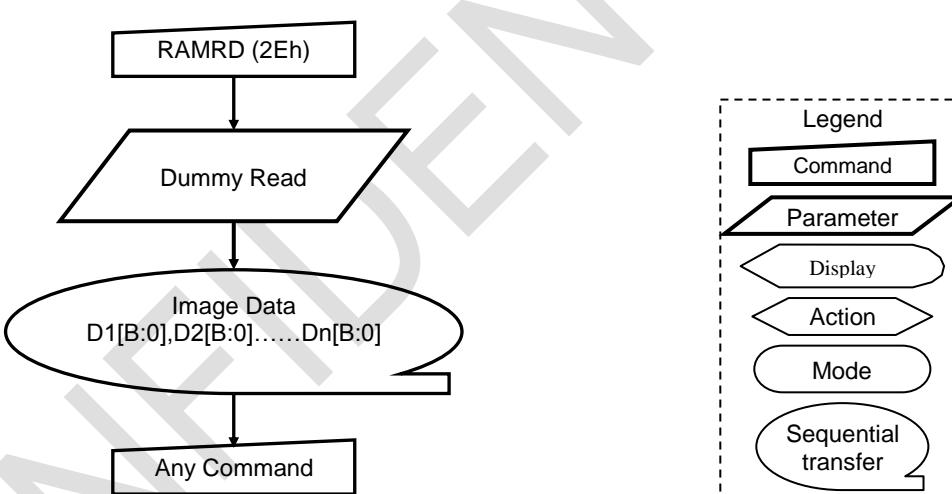
RAMWR (2C00h): Memory Write

2C00H		RAMWR (Memory Write)													
Inst/Para	R/W	Address		D24-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
		MIPi	Other	D1[24..8]	D17	D16	D15	D14	D13	D12	D11	D10	-		
RAMWR	W	2Ch	2C00h	:	:	:	:	:	:	:	:	:	:		
				Dn[24..8]	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	-		
Description	<p>This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands.</p> <p>If MV(36h-B5) = 0:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.</p> <p>If MV(36h-B5) = 1:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.</p>														
Restriction	<p>A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.</p>														

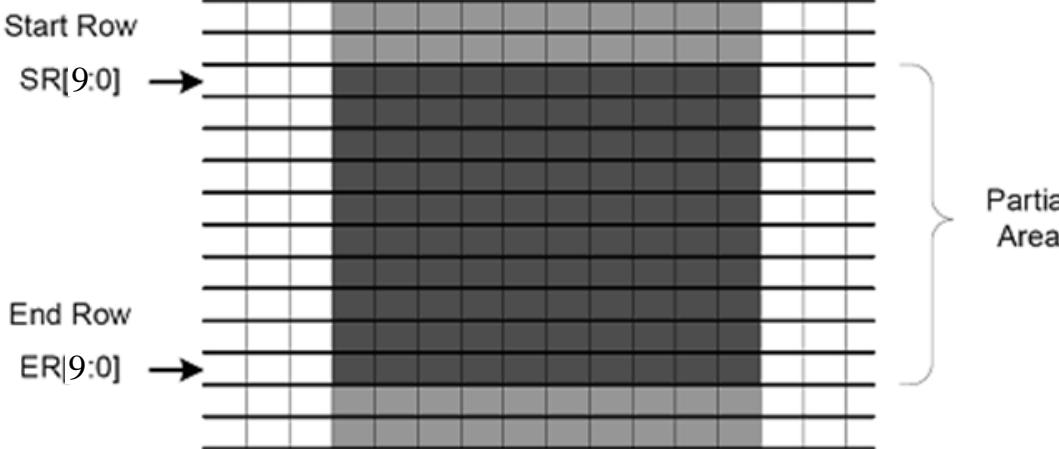
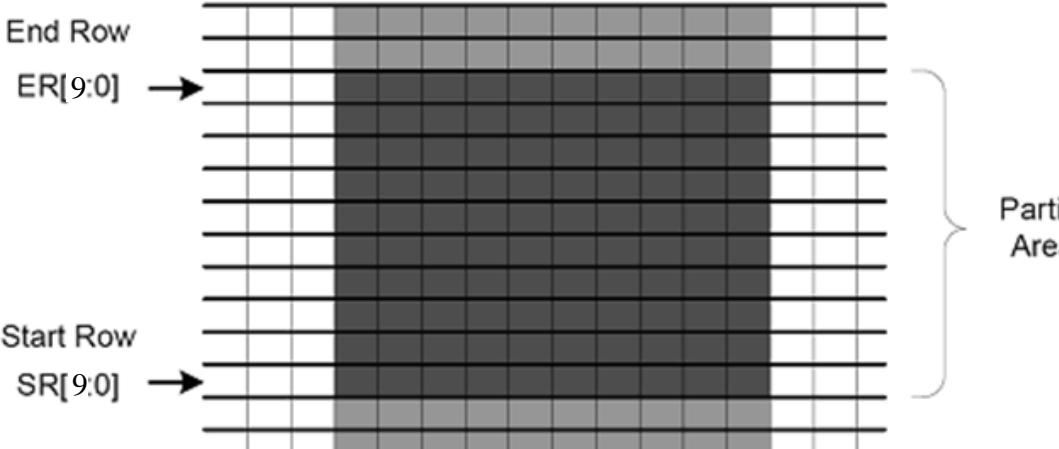
Register Availability		<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
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Status	Default Value												
Power On Sequence	Contents of memory is set randomly												
SW Reset	Contents of memory is not cleared												
HW Reset	Contents of memory is not cleared												
<p>Flow chart</p> <pre> graph TD RAMWR[RAMWR (2Ch)] --> ImageData((Image Data D1[B:0], D2[B:0], ..., Dn[B:0])) ImageData --> AnyCommand[Any Command] Note["Note : B=23"] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

RAMRD (2E00h): Memory Read

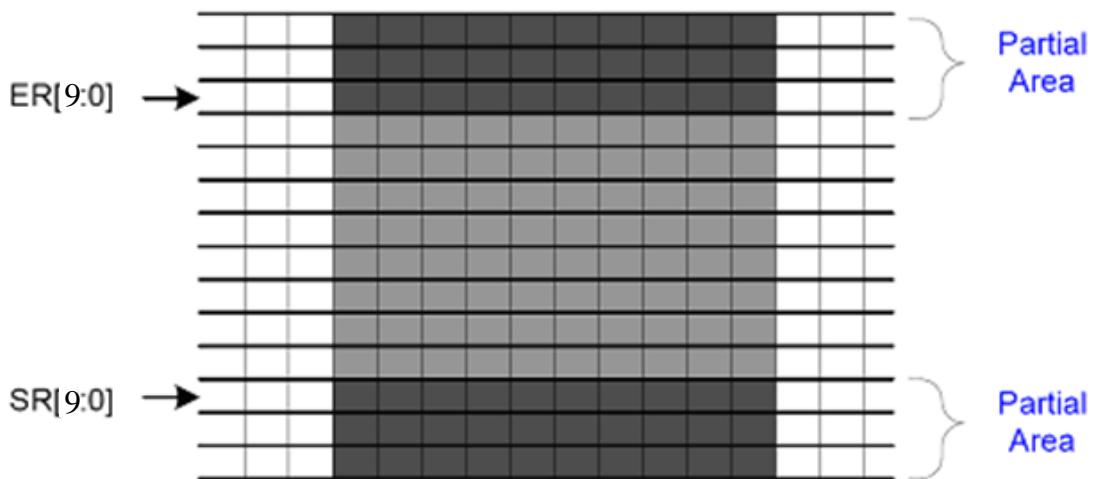
2E00H		RAMRD (Memory Read)													
Inst/Para	R/W	Address		D24-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
		MIPI	Other	D1[24..8]	D17	D16	D15	D14	D13	D12	D11	D10	-		
RAMRD	R	2Eh	2E00h	:	:	:	:	:	:	:	:	:	-		
				Dn[24..8]	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	-		
Description	<p>This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding CASET (2Ah) and RASET (2Bh) commands.</p> <p>If MV(36h-B5) = 0:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.</p> <p>If MV(36h-B5) = 1:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.</p>														
Restriction															

Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
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Status	Default Value												
Power On Sequence	Contents of memory is set randomly												
SW Reset	Contents of memory is not cleared												
Flow chart	 <pre> graph TD RAMRD[RAMRD (2Eh)] --> DR{Dummy Read} DR --> ID((Image Data D1[B:0], D2[B:0], ..., Dn[B:0])) ID --> AC[Any Command] </pre> <p>Note : B=23</p>												

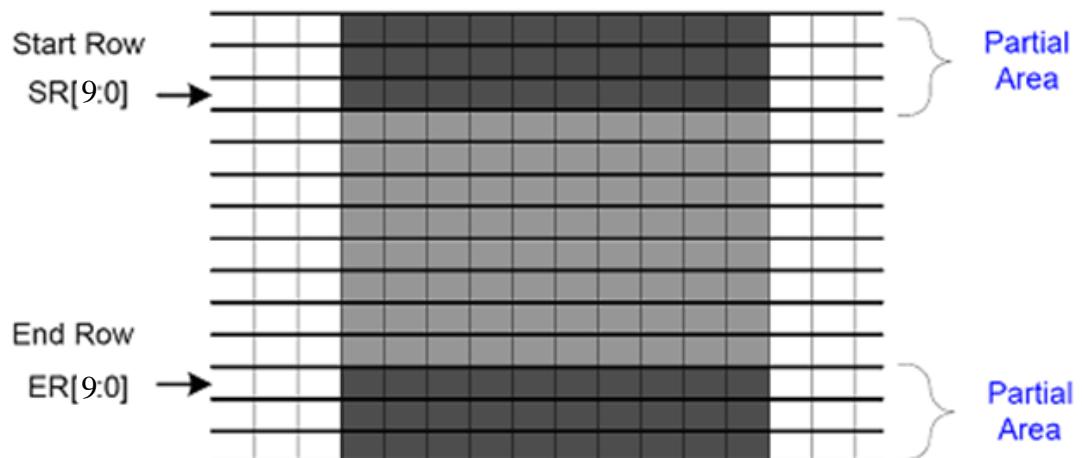
PTLAR (3000h): Partial Area

3000H		PTLAR (Partial Area)												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
		MIPI	Other											
PTLAR	R/W	30h	3000h	x	0	0	0	0	0	0	SR9	SR8	00	
			3001h	x	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00	
			3002h	x	0	0	0	0	0	0	ER9	ER8	-	
			3003h	x	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	-	
Description	<p>This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. SR and ER refer to the Frame Memory.</p> <p>-If End Row > Start Row, when ML(36h-B4) = '0'</p> 													
	<p>-If End Row > Start Row, when ML(36h-B4) = '1'</p> 													

-If End Row < Start Row, when ML(36h-B4) ='0'

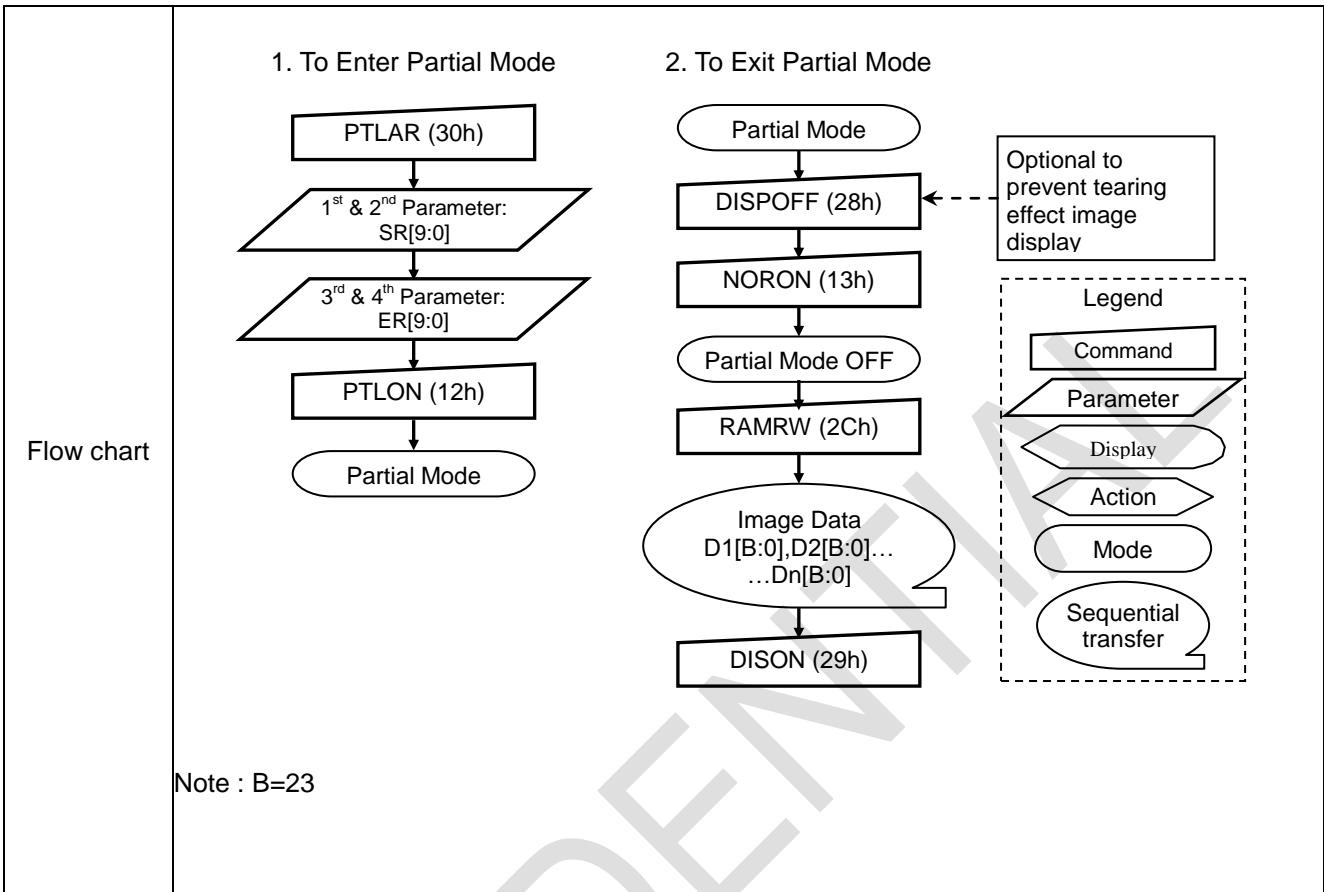


-If End Row < Start Row, when ML(36h-B4) ='1'



-If End Row = Start Row then the Partial Area will be one row deep.

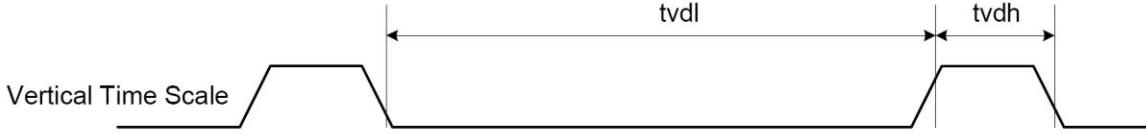
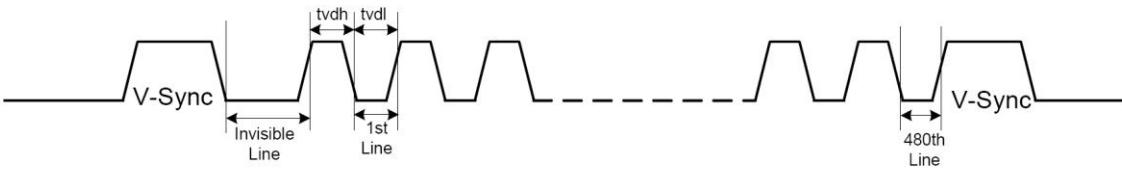
Restriction	SR[15:0] and ER[15:0] should have below range. CGM[2:0] = "000" (540 x 960): $0 \leq SR[15:0]$, $ER[15:0] \leq 959$ (03BFh), $ ER-SR \leq 959$ (03BFh) CGM[2:0] = "100" (480 x 960): $0 \leq SR[15:0]$, $ER[15:0] \leq 959$ (03BFh), $ ER-SR \leq 959$ (03BFh) CGM[2:0] = "101" (480 x 864): $0 \leq SR[15:0]$, $ER[15:0] \leq 863$ (035Fh), $ ER-SR \leq 863$ (035Fh) CGM[2:0] = "110" (480 x 854): $0 \leq SR[15:0]$, $ER[15:0] \leq 853$ (0355h), $ ER-SR \leq 853$ (0355h) CGM[2:0] = "111" (480 x 800): $0 \leq SR[15:0]$, $ER[15:0] \leq 799$ (031Fh), $ ER-SR \leq 799$ (031Fh)														
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes		
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Default	<table border="1"><thead><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>SR[8:0]</th><th>ER[8:0]</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>0000h</td><td>031Fh</td></tr><tr><td>SW Reset</td><td>0000h</td><td>031Fh</td></tr><tr><td>HW Reset</td><td>0000h</td><td>031Fh</td></tr></tbody></table>	Status	Default Value		SR[8:0]	ER[8:0]	Power On Sequence	0000h	031Fh	SW Reset	0000h	031Fh	HW Reset	0000h	031Fh
Status	Default Value														
	SR[8:0]	ER[8:0]													
Power On Sequence	0000h	031Fh													
SW Reset	0000h	031Fh													
HW Reset	0000h	031Fh													



TEOFF (3400h): Tearing Effect Line OFF

3400H		TEOFF (Tearing Effect Line OFF)																								
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
		MIPI	Other																							
TEOFF	W	34h	3400h	No Argument																						
Description	This command turns off the display module's Tearing Effect output signal on the TE signal line.																									
Restriction	This command has no effect when the Tearing Effect output is already off.																									
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OFF</td> </tr> <tr> <td>SW Reset</td> <td>OFF</td> </tr> <tr> <td>HW Reset</td> <td>OFF</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	OFF	SW Reset	OFF	HW Reset	OFF						
Status	Default Value																									
Power On Sequence	OFF																									
SW Reset	OFF																									
HW Reset	OFF																									
<pre> graph TD A([TE Line Output ON]) --> B[TEOFF (34h)] B --> C([TE Line Output OFF]) </pre>																										
<table border="1"> <thead> <tr> <th>Legend</th> </tr> </thead> <tbody> <tr> <td>Command</td> </tr> <tr> <td>Parameter</td> </tr> <tr> <td>Display</td> </tr> <tr> <td>Action</td> </tr> <tr> <td>Mode</td> </tr> <tr> <td>Sequential transfer</td> </tr> </tbody> </table>													Legend	Command	Parameter	Display	Action	Mode	Sequential transfer							
Legend																										
Command																										
Parameter																										
Display																										
Action																										
Mode																										
Sequential transfer																										

TEON (3500h): Tearing Effect Line ON

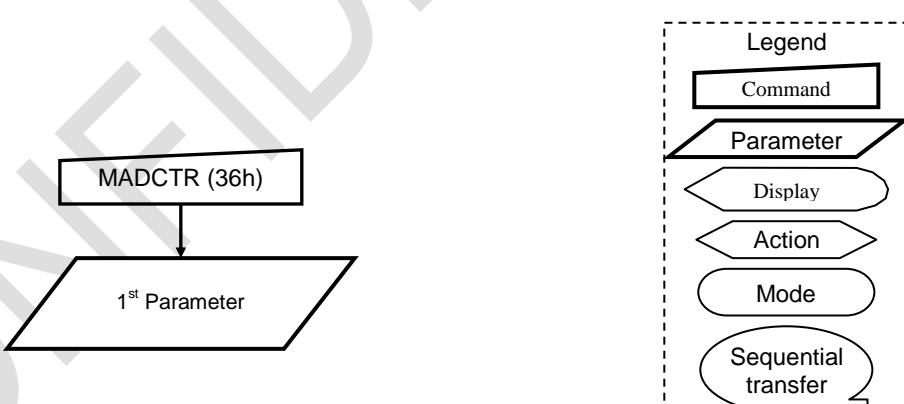
3500H		TEON (Tearing Effect Line ON)																						
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
		MIPI	Other																					
TEON	R/W	35h	3500h	x	0	0	0	0	0	0	0	TELOM	00											
Description	<p>This command turns on the tearing Effect output signal on the TE signal line. The TE signal is not affected by changing MADCTR (36h) B4 (Line Address Order).</p> <p>The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.</p> <p>If TELOM = 0:</p> <p>The Tearing Effect Output line consists of V-Blanking information only.</p>  <p>If TELOM = 1:</p> <p>The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.</p>  <p><i>The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</i></p>																							
Restriction	This command has no effect when Tearing Effect output is already ON.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes																							

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Status	Default Value								
Power On Sequence	OFF								
SW Reset	OFF								
HW Reset	OFF								
Flow Chart	<pre>graph TD; A([TE Line Output OFF]) --> B[TEON (35h)]; B --> C[/1st Parameter: TELOM/]; C --> D([TE Line Output ON]);</pre> <p>The flowchart illustrates a sequence of events. It begins with an oval labeled "TE Line Output OFF". An arrow points down to a rectangular box labeled "TEON (35h)". Another arrow points down to a trapezoidal box labeled "1st Parameter: TELOM". A final arrow points down to an oval labeled "TE Line Output ON".</p> <p>Legend:</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer								

MADCTR (3600h): Memory Data Access Control

3600H		MADCTR (Memory Data Access Control)											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
MADCTR	W	36h	3600h	x	B7	B6	B5	B4	B3	0	B1	B0	00
Description	This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status.												
	Bit	Symbol	Description			Comment							
	B7	MY	Row Address Order			'1' = Bottom to Top '0' = Top to Bottom							
	B6	MX	Column Address Order			'1' = Right to Left '0' = Left to Right							
	B5	MV	Row/Column Order (MV)			'1' = Row/column exchange '0' = Normal							
	B4	ML	Vertical Refresh Order			'0' =LCD Refresh Top to Bottom '1' =LCD Refresh Bottom to Top							
	B3	RGB	RGB/BGR Order			'1' =BGR, "0"=RGB							
	B2		reserved										
	B1	H_FLIP	Horizontal Flip			'0' = Normal display '1' = Flipped display							
	B0	V_FLIP	Vertical Flip			'0' = Normal display '1' = Flipped display							

			Image in Frame Memory		
B5	B6	B7	B5	B6	B7
0	0	0			
0	0	1			
0	1	0			
0	1	1			
			B3 = 0		
			Memory	Sent RGB	
			Display Panel		
			B3 = 1		
			Memory	Sent BGR	
			Display Panel		
Restriction					

Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
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Sleep In	Yes													
<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr><td>Power On Sequence</td><td>00h</td></tr> <tr><td>SW Reset</td><td>No Change</td></tr> <tr><td>HW Reset</td><td>00h</td></tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	SW Reset	No Change	HW Reset	00h					
Status	Default Value													
Power On Sequence	00h													
SW Reset	No Change													
HW Reset	00h													
 <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 														

IDMOFF (3800h): Idle Mode Off

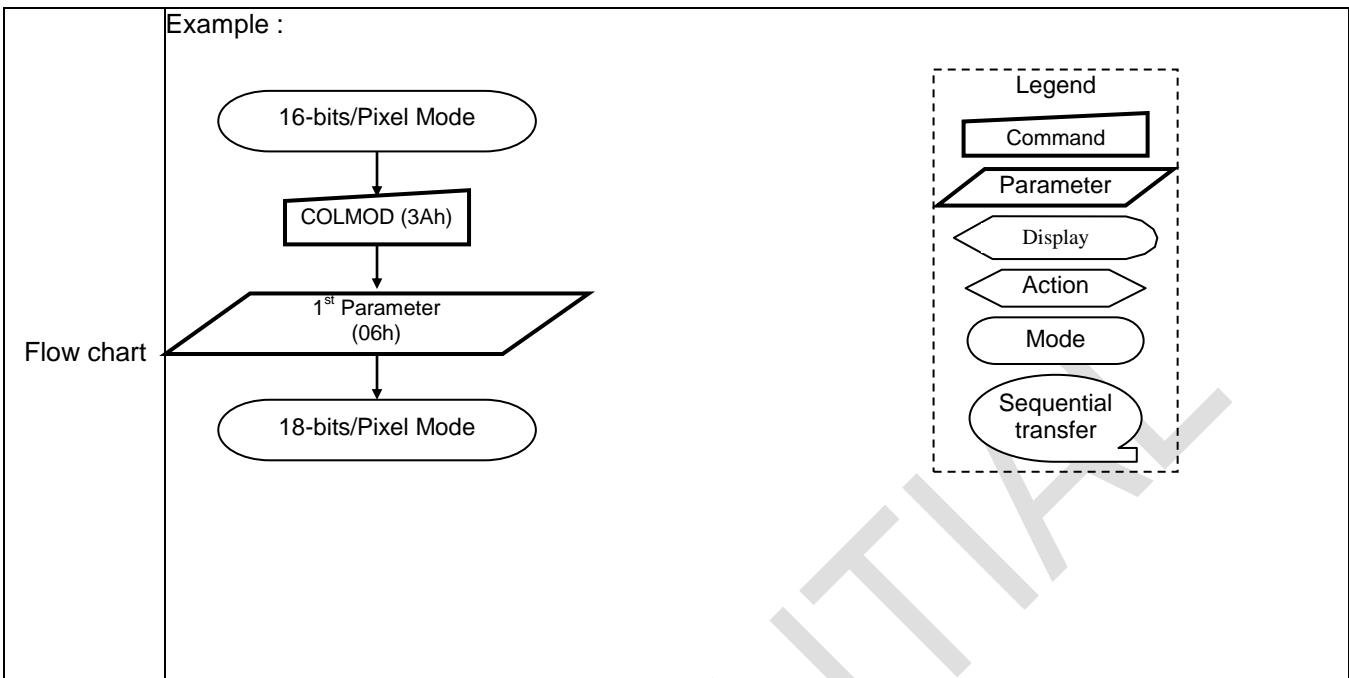
3800H		IDMOFF (Idle Mode Off)																													
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
		MIPI	Other																												
IDMOFF	W	38h	3800h	No Argument																											
Description	This command causes the display module to exit Idle mode.																														
Restriction	This command has no effect when the display module is not in Idle mode.																														
Register Availability	<table border="1"> <thead> <tr> <th colspan="2">Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td></td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td></td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td></td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td></td><td>Yes</td></tr> <tr> <td colspan="2">Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status		Availability	Normal Mode On, Idle Mode Off, Sleep Out		Yes	Normal Mode On, Idle Mode On, Sleep Out		Yes	Partial Mode On, Idle Mode Off, Sleep Out		Yes	Partial Mode On, Idle Mode On, Sleep Out		Yes	Sleep In		Yes
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Status		Default Value																													
Power On Sequence		Idle Mode Off																													
SW Reset		Idle Mode Off																													
HW Reset		Idle Mode Off																													
Flow Chart	<pre> graph TD A([Idle mode ON]) --> B[IDMOFF (38h)] B --> C([Idle mode OFF]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																														

IDMON (3900h): Enter_idle_mode

Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr><tr><td>SW Reset</td><td>Idle Mode Off</td></tr><tr><td>HW Reset</td><td>Idle Mode Off</td></tr></tbody></table>	Status	Default Value	Power On Sequence	Idle Mode Off	SW Reset	Idle Mode Off	HW Reset	Idle Mode Off
Status	Default Value								
Power On Sequence	Idle Mode Off								
SW Reset	Idle Mode Off								
HW Reset	Idle Mode Off								
Flow Chart	<pre>graph TD; A([Idle mode OFF]) --> B[IDMON (39h)]; B --> C([Idle mode ON]);</pre> <p>The flowchart illustrates a sequence of events. It begins with an oval labeled "Idle mode OFF". An arrow points down to a rectangular box labeled "IDMON (39h)". From "IDMON (39h)", another arrow points down to an oval labeled "Idle mode ON".</p> <p>Legend:</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer								

COLMOD (3A00h): Interface Pixel Format

COLMOD (Interface Pixel Format)																																																
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																			
		MIPI	Other																																													
COLMOD	W	3Ah	3A00h	x	0	D6	D5	D4	0	D2	D1	D0	77																																			
<p>This command sets the pixel format for the RGB image data used by the interface.</p> <p>Bits D[6:4] – DPI Pixel Format Definition Bits D[2:0] – DBI Pixel Format Definition Bits D7 and D3 are not used.</p> <p>If a particular interface, either DBI or DPI, is not used then the corresponding bits in the parameter are ignored.</p>																																																
Description	<table border="1"> <thead> <tr> <th>Control Interface Color Format</th><th>D6/D2</th><th>D5/D1</th><th>D4/D0</th></tr> </thead> <tbody> <tr><td>Not defined</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>Not defined</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>Not defined</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>Not defined</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>Not defined</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>16bit/pixel (65,536 colors)</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>18bit/pixel (262,144 colors)</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>24bit/pixel (16.7M colors)</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>												Control Interface Color Format	D6/D2	D5/D1	D4/D0	Not defined	0	0	0	Not defined	0	0	1	Not defined	0	1	0	Not defined	0	1	1	Not defined	1	0	0	16bit/pixel (65,536 colors)	1	0	1	18bit/pixel (262,144 colors)	1	1	0	24bit/pixel (16.7M colors)	1	1	1
Control Interface Color Format	D6/D2	D5/D1	D4/D0																																													
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Status	Default Value																																															
Power On Sequence	66h																																															
SW Reset	No Change																																															
HW Reset	66h																																															



RAMWRC(3C00h) : Write_Memory_Continue

3C00H		Write_Memory_Continue													
Inst/Para	R/W	Address		D24-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
		MIPi	Other	D1[24..8]	D17	D16	D15	D14	D13	D12	D11	D10	-		
RAMWRC	W	3Ch	3C00h	:	:	:	:	:	:	:	:	:	:		
				Dn[24..8]	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	-		
Description	<p>This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.</p> <p>If MV(36h-B5) = 0:</p> <p>Data is written continuing from the pixel location after the write range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds $(EC - SC + 1) * (EP - SP + 1)$ the extra pixels are ignored.</p> <p>If MV(36h-B5) = 1:</p> <p>Data is written continuing from the pixel location after the write range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds $(EC - SC + 1) * (EP - SP + 1)$ the extra pixels are ignored.</p> <p>Frame Memory Access and Interface setting (B3h), WEMODE=0</p> <p>When the transfer number of data exceeds $(EC-SC+1)*(EP-SP+1)$, the exceeding data will be ignored.</p>														
	<p>Frame Memory Access and Interface setting (B3h), WEMODE=1</p> <p>When the transfer number of data exceeds $(EC-SC+1)*(EP-SP+1)$, the column and page number will be reset, and the exceeding data will be written into the following column and page.</p>														

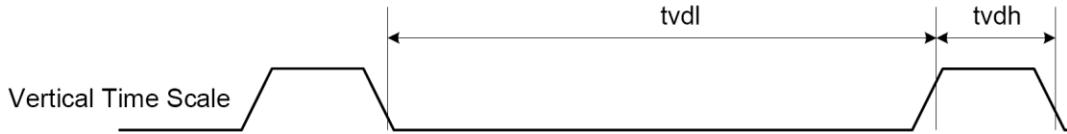
Restriction	A Memory Write should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMWR(2Ch) and any following RAMWRC(3Ch) commands is written to undefined locations.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value												
Power On Sequence	Contents of memory is set randomly												
SW Reset	Contents of memory is not cleared												
HW Reset	Contents of memory is not cleared												
Flow chart	<pre> graph TD RAMWRC[RAMWRC (3Ch)] --> ImageData((Image Data D1[B:0], D2[B:0].....Dn[B:0])) ImageData --> AnyCommand[Any Command] </pre> <p>Note : B = 23</p> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

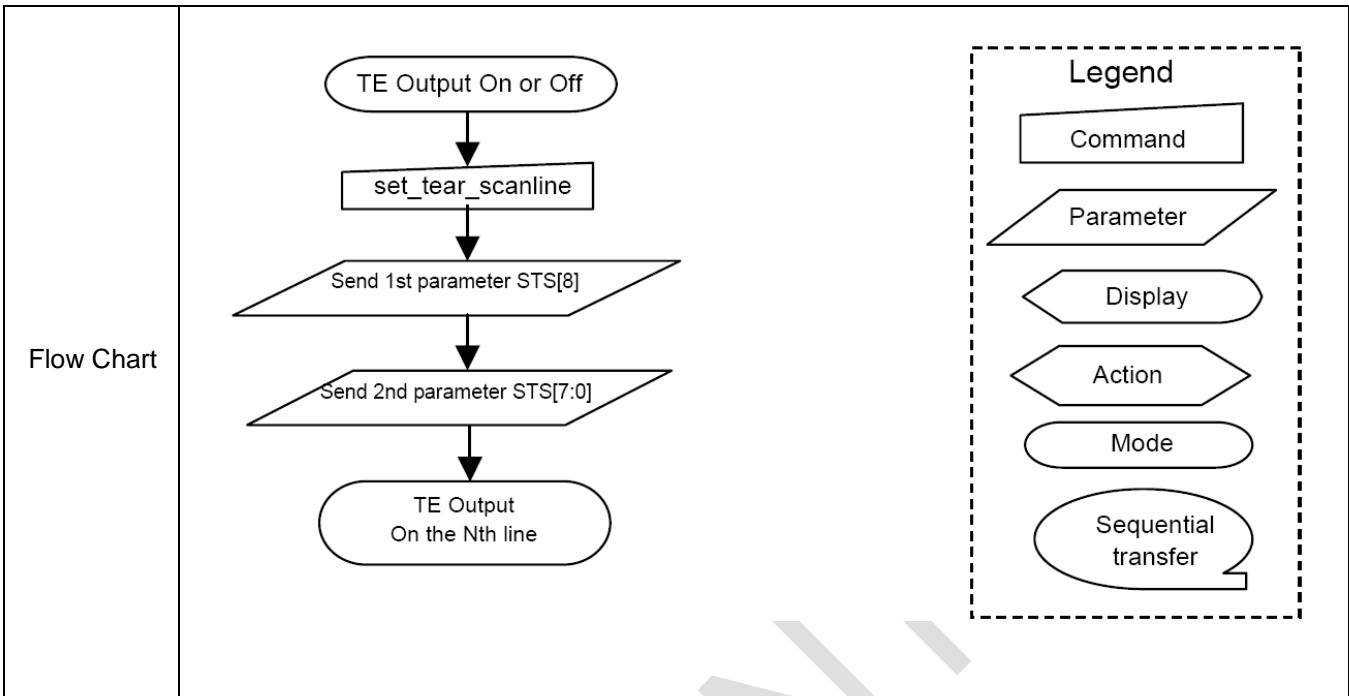
RAMRDC(3E00h) : Read_Memory_Continue

3E00H		Read_Memory_Continue											
Inst/Para	R/W	Address		D24-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPi	Other										
RAMRDC	R	3Eh	3E00h	D1[24..8]	D17	D16	D15	D14	D13	D12	D11	D10	-
				:	:	:	:	:	:	:	:	:	-
				Dn[24..8]	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	-
Description	<p>This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command.</p> <p>If MV(36h-B5) = 0: Pixels are read continuing from the pixel location after the read range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.</p> <p>If MV(36h-B5) B5 = 1: Pixels are read continuing from the pixel location after the read range of the previous RAMWR(2Ch) or RAMWRC(3Ch). The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.</p>												
	<p>A Memory Read should follow a CASET(2Ah), RASET(2Bh) or MADCTR(36h) to define the write location. Otherwise, data written with RAMRD(2Eh) and any following RAMRDC(3Eh) commands is written to undefined locations.</p>												

	Status	Availability								
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes								
	Normal Mode On, Idle Mode On, Sleep Out	Yes								
	Partial Mode On, Idle Mode Off, Sleep Out	Yes								
	Partial Mode On, Idle Mode On, Sleep Out	Yes								
	Sleep In	Yes								
	Status	Default Value								
Default	Power On Sequence	Contents of memory is set randomly								
	SW Reset	Contents of memory is not cleared								
	HW Reset	Contents of memory is not cleared								
Flow chart	<pre> graph TD A[RAMRDC (3Eh)] --> B{Dummy Read} B --> C([Image Data D1[B:0], D2[B:0], ..., Dn[B:0]]) C --> D[Any Command] </pre>	<p>Note : B=23</p> <table border="1"> <thead> <tr> <th colspan="2">Legend</th> </tr> </thead> <tbody> <tr> <td>Command</td> <td>Parameter</td> </tr> <tr> <td>Display</td> <td>Action</td> </tr> <tr> <td>Mode</td> <td>Sequential transfer</td> </tr> </tbody> </table>	Legend		Command	Parameter	Display	Action	Mode	Sequential transfer
Legend										
Command	Parameter									
Display	Action									
Mode	Sequential transfer									

STESL(4400h) : Set_Tear_Scanline

STESL(Set_Tear_Scanline)																								
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
		MIPi	Other																					
STESL	W	44h	4400h	x	STS[15]	STS[14]	STS[13]	STS[12]	STS[11]	STS[10]	STS[9]	STS[8]	00											
STESL			4401h	x	STS[7]	STS[6]	STS[5]	STS[4]	STS[3]	STS[2]	STS[1]	STS[0]	00											
Description	<p>This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.</p>  <p>The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</p>																							
Restriction																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
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Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>STS[15:0]=16'h0000</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>STS[15:0]=16'h0000</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	STS[15:0]=16'h0000	SW Reset	No change	HW Reset	STS[15:0]=16'h0000				
Status	Default Value																							
Power On Sequence	STS[15:0]=16'h0000																							
SW Reset	No change																							
HW Reset	STS[15:0]=16'h0000																							



CONFIDENTIAL

GSL (4500h) : Get_Scanline

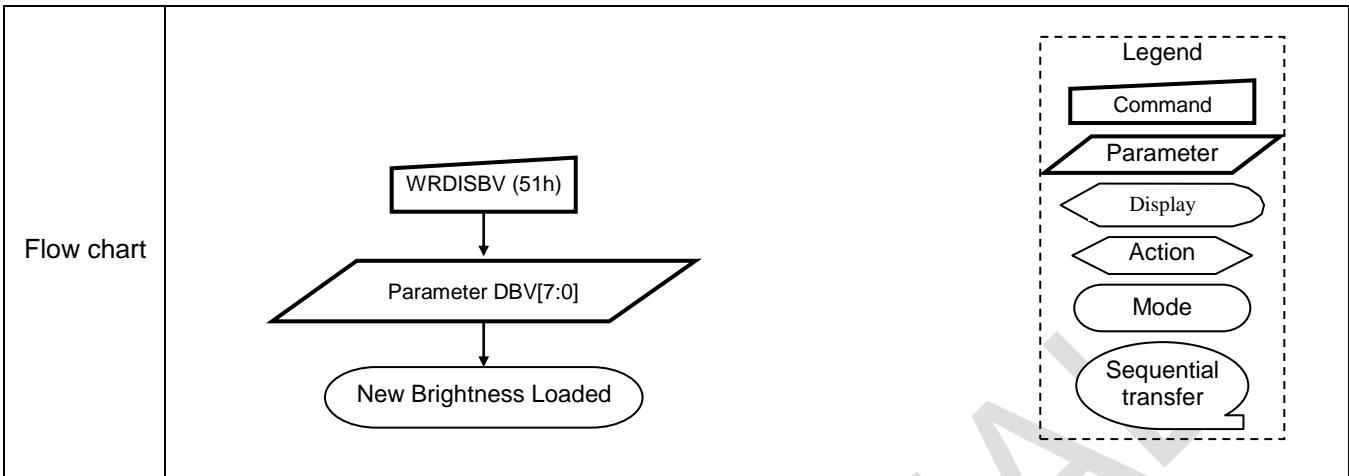
GSL(Get_Scanline)																									
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
		MIPI	Other																						
GSL	R	45h	4500h	x	GTS[15]	GTS[14]	GTS[13]	GTS[12]	GTS[11]	GTS[10]	GTS[9]	GTS[8]	0x												
			4501h	x	GTS[7]	GTS[6]	GTS[5]	GTS[4]	GTS[3]	GTS[2]	GTS[1]	GTS[0]	xx												
Description	The display returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get_scanline is undefined.																								
Restriction	-																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes																								
<pre> graph TD A[get_scanline] --> B{Wait 3us} B --> C[Dummy Read] C --> D[/Send 1st parameter GTS[9:8]/] D --> E[/Send 2nd parameter GTS[7:0]/] </pre>																									
<table border="1"> <thead> <tr> <th>Legend</th> </tr> </thead> <tbody> <tr> <td>Command</td> </tr> <tr> <td>Parameter</td> </tr> <tr> <td>Display</td> </tr> <tr> <td>Action</td> </tr> <tr> <td>Mode</td> </tr> <tr> <td>Sequential transfer</td> </tr> </tbody> </table>													Legend	Command	Parameter	Display	Action	Mode	Sequential transfer						
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Command																									
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Sequential transfer																									

DSTBON (4F00h): Deep Standby Mode On

		DSTBON(Deep Standby Mode On)																						
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
		MIPi	Other																					
DSTBON	W	4Fh	4F00h	x	0	0	0	0	0	0	0	DSTB	00											
Description	<p>This command is used to enter deep standby mode.</p> <p>DSTB="1", enter deep standby mode.</p> <p>Notes:</p> <ol style="list-style-type: none"> To exit Deep Standby Mode, input low pulse more than 3 msec to pin RESX. 																							
Restriction	There is no visible effect until the Frame Memory is written to.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>SW Reset</td> <td>00h</td> </tr> <tr> <td>HW Reset</td> <td>00h</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	00h	SW Reset	00h	HW Reset	00h				
Status	Default Value																							
Power On Sequence	00h																							
SW Reset	00h																							
HW Reset	00h																							
Flow chart	<pre> graph TD A[DSTBON (4Fh)] --> B[Parameter DSTB=1] B --> C([Deep Standby Mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																							

WRDISBV (5100h): Write Display Brightness

WRDISBV																												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
		MIPI	Other																									
WRDISBV	W	51h	5100h	x	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	FF															
This command is used to adjust brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.																												
Description	<table border="1"> <thead> <tr> <th>DBV[7:0] Brightness (cd/m²)</th> <th>DBV[7:0] Brightness (cd/m²)</th> </tr> </thead> <tbody> <tr><td>F9h</td><td>30</td></tr> <tr><td>FAh</td><td>50</td></tr> <tr><td>FBh</td><td>80</td></tr> <tr><td>FCh</td><td>100</td></tr> <tr><td>FDh</td><td>150</td></tr> <tr><td>FEh</td><td>200</td></tr> <tr><td>FFh</td><td>300</td></tr> </tbody> </table>												DBV[7:0] Brightness (cd/m ²)	DBV[7:0] Brightness (cd/m ²)	F9h	30	FAh	50	FBh	80	FCh	100	FDh	150	FEh	200	FFh	300
DBV[7:0] Brightness (cd/m ²)	DBV[7:0] Brightness (cd/m ²)																											
F9h	30																											
FAh	50																											
FBh	80																											
FCh	100																											
FDh	150																											
FEh	200																											
FFh	300																											
Restriction	The display supplier cannot use this command for tuning																											
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes				
Status	Availability																											
Normal Mode On, Idle Mode Off, Sleep Out	Yes																											
Normal Mode On, Idle Mode On, Sleep Out	Yes																											
Partial Mode On, Idle Mode Off, Sleep Out	Yes																											
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Status	Default Value																											
Power On Sequence	00h																											
SW Reset	00h																											
HW Reset	00h																											



RDDISBV (5200h): Read Display Brightness

		RDDISBV																						
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
		MIPi	Other																					
RDDISBV	R	52h	5200h	x	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	FF											
Description	<p>This command returns brightness value.</p> <p>In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p>																							
Restriction	-																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
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Sleep In	Yes																							
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Status	Default Value																							
Power On Sequence	00h																							
SW Reset	00h																							
HW Reset	00h																							
Flow Chart	<pre> graph TD RD[RDIDSBV (52hH)] --> SD[/Send parameter DBV[7:0]/] SD --> D[Display] style RD fill:#fff,stroke:#000 style SD fill:#fff,stroke:#000 style D fill:#fff,stroke:#000 style L fill:#fff,stroke:#000 L --- C[Command] L --- P[Parameter] L --- Dp[Display] L --- A[Action] L --- M[Mode] L --- ST[Sequential transfer] </pre> <p>The flowchart illustrates the communication sequence. It starts with the command RDIDSBV (52hH) from the Host Driver, which triggers the action "Send parameter DBV[7:0]" to the Display. A legend on the right side defines the symbols used in the flowchart:</p> <ul style="list-style-type: none"> Command: Represented by a rectangle. Parameter: Represented by a parallelogram. Display: Represented by a diamond. Action: Represented by a triangle. Mode: Represented by an oval. Sequential transfer: Represented by an oval with an arrow indicating a sequence. 																							

RDBWLB (7000h): Read Black/White Low Bits

		RDBWLB																																																																																									
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																														
		MIPI	Other																																																																																								
RDBWLB	R	70h	7000h	x	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0	00																																																																														
Description	This command returns the lowest bits of black and white color characteristic. Black: Bkx and Bky White: Wx and Wy																																																																																										
Restriction	-																																																																																										
Register Availability	<table border="1"> <thead> <tr> <th colspan="6">Status</th><th colspan="7">Availability</th></tr> </thead> <tbody> <tr> <td colspan="6">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="7">Yes</td></tr> <tr> <td colspan="6">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="7">Yes</td></tr> <tr> <td colspan="6">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="7">Yes</td></tr> <tr> <td colspan="6">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="7">Yes</td></tr> <tr> <td colspan="6">Sleep In</td><td colspan="7" rowspan="2">Yes</td></tr> </tbody> </table>													Status						Availability							Normal Mode On, Idle Mode Off, Sleep Out						Yes							Normal Mode On, Idle Mode On, Sleep Out						Yes							Partial Mode On, Idle Mode Off, Sleep Out						Yes							Partial Mode On, Idle Mode On, Sleep Out						Yes							Sleep In						Yes						
Status						Availability																																																																																					
Normal Mode On, Idle Mode Off, Sleep Out						Yes																																																																																					
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Sleep In						Yes																																																																																					
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Status						Default Value																																																																																					
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Power On Sequence						MTP Value		00h																																																																																			
SW Reset						MTP Value		00h																																																																																			
HW Reset						MTP Value		00h																																																																																			
Flow Chart	<pre> graph TD A[RDBWLB(70h)] --> B{Send Parameter Bkx[1:0], Bky[1:0], Wx[1:0], Wy[1:0]} </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																																																																																										

RDBkx (7100h): Read Bkx

7100H		RDBkx															
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX				
		MIPI	Other														
RDBkx	R	71h	7100h	x	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2	00				
Description	This command returns the Bkx bit (Bkx[9:2]) of black color characteristic.																
Restriction	-																
Register Availability	Status							Availability									
	Normal Mode On, Idle Mode Off, Sleep Out							Yes									
	Normal Mode On, Idle Mode On, Sleep Out							Yes									
	Partial Mode On, Idle Mode Off, Sleep Out							Yes									
	Partial Mode On, Idle Mode On, Sleep Out							Yes									
	Sleep In							Yes									
Default	Status							Default Value									
	Power On Sequence							After MTP		Before MTP							
	SW Reset							MTP Value		00h							
	HW Reset							MTP Value		00h							
Flow Chart	<pre> graph TD A[RDBkx(71h)] --> B[/Send Parameter Bkx[9:2]/] style A fill:#fff,stroke:#000,stroke-width:1px style B fill:#fff,stroke:#000,stroke-width:1px </pre>																
	<table border="1"> <tr> <td>Command</td> </tr> <tr> <td>Parameter</td> </tr> <tr> <td>Display</td> </tr> <tr> <td>Action</td> </tr> <tr> <td>Mode</td> </tr> <tr> <td>Sequential transfer</td> </tr> </table>												Command	Parameter	Display	Action	Mode
Command																	
Parameter																	
Display																	
Action																	
Mode																	
Sequential transfer																	

RDBky (7200h): Read Bky

7200H		RDBky																
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX					
		MIPI	Other															
RDBky	R	72h	7200h	x	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2	00					
Description	This command returns the Bky bit (Bky[9:2]) of black color characteristic.																	
Restriction	-																	
Register Availability	Status							Availability										
	Normal Mode On, Idle Mode Off, Sleep Out							Yes										
	Normal Mode On, Idle Mode On, Sleep Out							Yes										
	Partial Mode On, Idle Mode Off, Sleep Out							Yes										
	Partial Mode On, Idle Mode On, Sleep Out							Yes										
	Sleep In							Yes										
Default	Status							Default Value										
	Power On Sequence							After MTP		Before MTP								
	SW Reset							MTP Value		00h								
	HW Reset							MTP Value		00h								
Flow Chart	<pre> graph TD A[RDBky(72h)] --> B[/Send Parameter Bky[9:2]/] </pre>																	
	<table border="1"> <tr> <td>Legend</td> </tr> <tr> <td>Command</td> </tr> <tr> <td>Parameter</td> </tr> <tr> <td>Display</td> </tr> <tr> <td>Action</td> </tr> <tr> <td>Mode</td> </tr> <tr> <td>Sequential transfer</td> </tr> </table>												Legend	Command	Parameter	Display	Action	Mode
Legend																		
Command																		
Parameter																		
Display																		
Action																		
Mode																		
Sequential transfer																		

RDWx (7300h): Read Wx

		RDWx																	
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX						
		MIPI	Other																
RDWx	R	73h	7300h	x	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2	00						
Description	This command returns the Wx bit (Wx[9:2]) of black color characteristic.																		
Restriction	-																		
Register Availability	Status							Availability											
	Normal Mode On, Idle Mode Off, Sleep Out							Yes											
	Normal Mode On, Idle Mode On, Sleep Out							Yes											
	Partial Mode On, Idle Mode Off, Sleep Out							Yes											
	Partial Mode On, Idle Mode On, Sleep Out							Yes											
	Sleep In							Yes											
Default	Status							Default Value											
	Power On Sequence							After MTP		Before MTP									
	SW Reset							MTP Value		00h									
	HW Reset							MTP Value		00h									
Flow Chart	<pre> graph TD RDWx[RDWx(73h)] --> Param[/Send Parameter
Wx[9:2]] style RDWx fill:#fff,stroke:#000,stroke-width:1px style Param fill:#fff,stroke:#000,stroke-width:1px </pre>																		
	<table border="1"> <tr> <td>Command</td> </tr> <tr> <td>Parameter</td> </tr> <tr> <td>Display</td> </tr> <tr> <td>Action</td> </tr> <tr> <td>Mode</td> </tr> <tr> <td>Sequential transfer</td> </tr> </table>													Command	Parameter	Display	Action	Mode	Sequential transfer
Command																			
Parameter																			
Display																			
Action																			
Mode																			
Sequential transfer																			

RDWy (7400h): Read Wy

		RDWy																		
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX							
		MIPI	Other																	
RDWy	R	74h	7400h	x	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2	00							
Description	This command returns the Bky bit (Bky[9:2]) of black color characteristic.																			
Restriction	-																			
Register Availability	Status							Availability												
	Normal Mode On, Idle Mode Off, Sleep Out							Yes												
	Normal Mode On, Idle Mode On, Sleep Out							Yes												
	Partial Mode On, Idle Mode Off, Sleep Out							Yes												
	Partial Mode On, Idle Mode On, Sleep Out							Yes												
	Sleep In							Yes												
Default	Status							Default Value												
								After MTP		Before MTP										
	Power On Sequence							MTP Value		00h										
	SW Reset							MTP Value		00h										
Flow Chart	HW Reset							MTP Value		00h										
	<pre> graph TD RDWy[RDWy(74h)] --> Send[Send Parameter Wy[9:2]] </pre>							<table border="1"> <tr> <td>Legend</td> </tr> <tr> <td>Command</td> </tr> <tr> <td>Parameter</td> </tr> <tr> <td>Display</td> </tr> <tr> <td>Action</td> </tr> <tr> <td>Mode</td> </tr> <tr> <td>Sequential transfer</td> </tr> </table>							Legend	Command	Parameter	Display	Action	Mode
Legend																				
Command																				
Parameter																				
Display																				
Action																				
Mode																				
Sequential transfer																				

RDRGLB (7500h): Read Red/Green Low Bits

		RDRGLB																							
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
		MIPI	Other																						
RDRGLB	R	75h	7500h	x	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0	00												
Description	This command returns the lowest bits of red and green color characteristic. Red: Rx and Ry Green: Gx and Gy																								
Restriction	-																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>						Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
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Status	Default Value																								
	After MTP	Before MTP																							
Power On Sequence	MTP Value	00h																							
SW Reset	MTP Value	00h																							
HW Reset	MTP Value	00h																							
Flow Chart	<pre> graph TD A[RDRGLB(75h)] --> B[/Send Parameter Rx[1:0], Ry[1:0], Gx[1:0], Gy[1:0]/] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

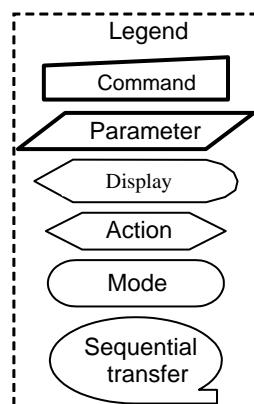
RDRx (7600h): Read Rx

7600H		RDRx											
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDRx	R	76h	7600h	x	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	00
Description	This command returns the Rx bit (Rx[9:2]) of red color characteristic.												
Restriction	-												
Register Availability	Status							Availability					
	Normal Mode On, Idle Mode Off, Sleep Out							Yes					
	Normal Mode On, Idle Mode On, Sleep Out							Yes					
	Partial Mode On, Idle Mode Off, Sleep Out							Yes					
	Partial Mode On, Idle Mode On, Sleep Out							Yes					
	Sleep In							Yes					
Default	Status							Default Value					
								After MTP		Before MTP			
	Power On Sequence							MTP Value		00h			
	SW Reset							MTP Value		00h			
Flow Chart	HW Reset							MTP Value		00h			
	<pre> graph TD A[RDRx(76h)] --> B[/Send Parameter Rx[9:2]/] </pre>							Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 					

RDRy (7700h): Read Ry

		RDRy																																																																							
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																												
		MIPI	Other																																																																						
RDRy	R	77h	7700h	x	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2	00																																																												
Description	This command returns the Ry bit (Ry[9:2]) of red color characteristic.																																																																								
Restriction	-																																																																								
Register Availability	<table border="1"> <thead> <tr> <th colspan="5">Status</th><th colspan="5">Availability</th></tr> </thead> <tbody> <tr> <td colspan="5">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="5">Yes</td></tr> <tr> <td colspan="5">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="5">Yes</td></tr> <tr> <td colspan="5">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="5">Yes</td></tr> <tr> <td colspan="5">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="5">Yes</td></tr> <tr> <td colspan="5">Sleep In</td><td colspan="5" rowspan="2">Yes</td></tr> </tbody> </table>													Status					Availability					Normal Mode On, Idle Mode Off, Sleep Out					Yes					Normal Mode On, Idle Mode On, Sleep Out					Yes					Partial Mode On, Idle Mode Off, Sleep Out					Yes					Partial Mode On, Idle Mode On, Sleep Out					Yes					Sleep In					Yes				
Status					Availability																																																																				
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Partial Mode On, Idle Mode On, Sleep Out					Yes																																																																				
Sleep In					Yes																																																																				
Default	<table border="1"> <thead> <tr> <th colspan="5">Status</th><th colspan="5">Default Value</th></tr> <tr> <th colspan="5"></th><th colspan="2">After MTP</th><th colspan="3">Before MTP</th></tr> </thead> <tbody> <tr> <td colspan="5">Power On Sequence</td><td colspan="2">MTP Value</td><td colspan="3">00h</td></tr> <tr> <td colspan="5">SW Reset</td><td colspan="2">MTP Value</td><td colspan="3">00h</td></tr> <tr> <td colspan="5">HW Reset</td><td colspan="2" rowspan="3">MTP Value</td><td colspan="3" rowspan="3">00h</td></tr> </tbody> </table>													Status					Default Value										After MTP		Before MTP			Power On Sequence					MTP Value		00h			SW Reset					MTP Value		00h			HW Reset					MTP Value		00h												
Status					Default Value																																																																				
					After MTP		Before MTP																																																																		
Power On Sequence					MTP Value		00h																																																																		
SW Reset					MTP Value		00h																																																																		
HW Reset					MTP Value		00h																																																																		
Flow Chart	<pre> graph TD A[RDRy(77h)] --> B[/Send Parameter Ry[9:2]/] </pre>																																																																								
	<p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																																																																								

RDGx (7800h): Read Gx

Inst/Para	R/W	RDGx																	
		Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX						
		MIPI	Other																
RDGx	R	78h	7800h	x	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2	00						
Description	This command returns the Gx bit (Gx[9:2]) of green color characteristic.																		
Restriction	-																		
Register Availability	Status								Availability										
	Normal Mode On, Idle Mode Off, Sleep Out								Yes										
	Normal Mode On, Idle Mode On, Sleep Out								Yes										
	Partial Mode On, Idle Mode Off, Sleep Out								Yes										
	Partial Mode On, Idle Mode On, Sleep Out								Yes										
	Sleep In								Yes										
Default	Status								Default Value										
	Power On Sequence								After MTP		Before MTP								
	SW Reset								MTP Value		00h								
	HW Reset								MTP Value		00h								
Flow Chart	<pre> graph TD RDGx[RDGx(78h)] --> Send[/Send Parameter Gx[9:2]/] </pre>																		
	 <table border="1"> <tr> <td>Legend</td> </tr> <tr> <td>Command</td> </tr> <tr> <td>Parameter</td> </tr> <tr> <td>Display</td> </tr> <tr> <td>Action</td> </tr> <tr> <td>Mode</td> </tr> <tr> <td>Sequential transfer</td> </tr> </table>													Legend	Command	Parameter	Display	Action	Mode
Legend																			
Command																			
Parameter																			
Display																			
Action																			
Mode																			
Sequential transfer																			

RDGy (7900h): Read Gy

Inst/Para	R/W	RDGy																	
		Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX						
		MIPI	Other																
RDGy	R	79h	7900h	x	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2	00						
Description	This command returns the Gy bit (Gy[9:2]) of green color characteristic.																		
Restriction	-																		
Register Availability	Status							Availability											
	Normal Mode On, Idle Mode Off, Sleep Out							Yes											
	Normal Mode On, Idle Mode On, Sleep Out							Yes											
	Partial Mode On, Idle Mode Off, Sleep Out							Yes											
	Partial Mode On, Idle Mode On, Sleep Out							Yes											
	Sleep In							Yes											
Default	Status							Default Value											
	Power On Sequence							After MTP		Before MTP									
	SW Reset							MTP Value		00h									
	HW Reset							MTP Value		00h									
Flow Chart	<pre> graph TD RDGy[RDGy(79h)] --> Send[Send Parameter Gy[9:2]] </pre>																		
	<table border="1"> <tr> <td>Legend</td> </tr> <tr> <td>Command</td> </tr> <tr> <td>Parameter</td> </tr> <tr> <td>Display</td> </tr> <tr> <td>Action</td> </tr> <tr> <td>Mode</td> </tr> <tr> <td>Sequential transfer</td> </tr> </table>													Legend	Command	Parameter	Display	Action	Mode
Legend																			
Command																			
Parameter																			
Display																			
Action																			
Mode																			
Sequential transfer																			

RDBALB (7A00h): Read Red/Green Low Bits

		RDBALB																						
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
		MIPI	Other																					
RDBALB	R	7Ah	7A00h	x	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0	00											
Description	This command returns the lowest bits of blue and A color characteristic. Blue: Bx and By A: Ax and Ay																							
Restriction	-																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>						Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes						
Status	Availability																							
Normal Mode On, Idle Mode Off, Sleep Out	Yes																							
Normal Mode On, Idle Mode On, Sleep Out	Yes																							
Partial Mode On, Idle Mode Off, Sleep Out	Yes																							
Partial Mode On, Idle Mode On, Sleep Out	Yes																							
Sleep In	Yes																							
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Status	Default Value																							
After MTP	Before MTP																							
Power On Sequence	MTP Value	00h																						
SW Reset	MTP Value	00h																						
HW Reset	MTP Value	00h																						
Flow Chart	<pre> graph TD RDBALB[RDBALB(7Ah)] --> Send[Send Parameter Bx[1:0], By[1:0], Ax[1:0], Ay[1:0]] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																							

RDBx (7B00h): Read Rx

Inst/Para	R/W	RDBx											
		Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDBx	R	7Bh	7B00h	x	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2	00
Description	This command returns the Bx bit (Bx[9:2]) of blue color characteristic.												
Restriction	-												
Register Availability	Status							Availability					
	Normal Mode On, Idle Mode Off, Sleep Out							Yes					
	Normal Mode On, Idle Mode On, Sleep Out							Yes					
	Partial Mode On, Idle Mode Off, Sleep Out							Yes					
	Partial Mode On, Idle Mode On, Sleep Out							Yes					
	Sleep In							Yes					
Default	Status							Default Value					
	Power On Sequence							After MTP		Before MTP			
	SW Reset							MTP Value		00h			
	HW Reset							MTP Value		00h			
Flow Chart	<pre> graph TD A[RDBx(7Bh)] --> B[/ Send Parameter Bx[9:2] /] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

RDBy (7C00h): Read By

Inst/Para	R/W	RDBy																							
		Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
		MIPI	Other																						
RDBy	R	7Ch	7C00h	x	By9	By8	By7	By6	By5	By4	By3	By2	00												
Description	This command returns the By bit (By[9:2]) of blue color characteristic.																								
Restriction	-																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
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Sleep In	Yes																								
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Status	Default Value																								
After MTP	Before MTP																								
Power On Sequence	MTP Value	00h																							
SW Reset	MTP Value	00h																							
HW Reset	MTP Value	00h																							
<pre> graph TD A[RDBy(7Ch)] --> B[/ Send Parameter By[9:2] /] </pre>																									
<table border="1"> <thead> <tr> <th>Legend</th> </tr> </thead> <tbody> <tr> <td>Command</td> </tr> <tr> <td>Parameter</td> </tr> <tr> <td>Display</td> </tr> <tr> <td>Action</td> </tr> <tr> <td>Mode</td> </tr> <tr> <td>Sequential transfer</td> </tr> </tbody> </table>													Legend	Command	Parameter	Display	Action	Mode	Sequential transfer						
Legend																									
Command																									
Parameter																									
Display																									
Action																									
Mode																									
Sequential transfer																									
Flow Chart																									

RDAx (7D00h): Read Ax

		RDAx																																																																							
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																												
		MIPI	Other																																																																						
RDAx	R	7Dh	7D00h	x	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2	00																																																												
Description	This command returns the Ax bit (Ax[9:2]) of A color characteristic.																																																																								
Restriction	-																																																																								
Register Availability	<table border="1"> <thead> <tr> <th colspan="5">Status</th><th colspan="5">Availability</th></tr> </thead> <tbody> <tr> <td colspan="5">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="5">Yes</td></tr> <tr> <td colspan="5">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="5">Yes</td></tr> <tr> <td colspan="5">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="5">Yes</td></tr> <tr> <td colspan="5">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="5">Yes</td></tr> <tr> <td colspan="5">Sleep In</td><td colspan="5" rowspan="2">Yes</td></tr> </tbody> </table>													Status					Availability					Normal Mode On, Idle Mode Off, Sleep Out					Yes					Normal Mode On, Idle Mode On, Sleep Out					Yes					Partial Mode On, Idle Mode Off, Sleep Out					Yes					Partial Mode On, Idle Mode On, Sleep Out					Yes					Sleep In					Yes				
Status					Availability																																																																				
Normal Mode On, Idle Mode Off, Sleep Out					Yes																																																																				
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SW Reset					MTP Value		00h																																																																		
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HW Reset					MTP Value		00h																																																																		
Flow Chart	<pre> graph TD RDAx[RDAx(7Dh)] --> Send[Send Parameter Ax[9:2]] </pre>																																																																								
	<p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																																																																								

RDAy (7E00h): Read Ay

Inst/Para	R/W	RDAy																	
		Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX						
		MIPI	Other																
RDAy	R	7Eh	7E00h	x	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ay3	Ay2	00						
Description	This command returns the Ay bit (Ay[9:2]) of A color characteristic.																		
Restriction	-																		
Register Availability	Status								Availability										
	Normal Mode On, Idle Mode Off, Sleep Out								Yes										
	Normal Mode On, Idle Mode On, Sleep Out								Yes										
	Partial Mode On, Idle Mode Off, Sleep Out								Yes										
	Partial Mode On, Idle Mode On, Sleep Out								Yes										
	Sleep In								Yes										
Default	Status								Default Value										
	Power On Sequence								After MTP		Before MTP								
	SW Reset								MTP Value		00h								
	HW Reset								MTP Value		00h								
Flow Chart	<pre> graph TD RDAy[RDAy(7Eh)] --> Send[Send Parameter Ay[9:2]] </pre>																		
	<table border="1"> <tr> <td>Legend</td> </tr> <tr> <td>Command</td> </tr> <tr> <td>Parameter</td> </tr> <tr> <td>Display</td> </tr> <tr> <td>Action</td> </tr> <tr> <td>Mode</td> </tr> <tr> <td>Sequential transfer</td> </tr> </table>													Legend	Command	Parameter	Display	Action	Mode
Legend																			
Command																			
Parameter																			
Display																			
Action																			
Mode																			
Sequential transfer																			

RDDDBS(A1h) : Read_DDB_Start (A1h)

A1H		RDDDBS(Read_DDB_Start)																							
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
		MIPI	Other																						
RDDDBS	R	A1h	A100h	x	ID1[7]	ID1[6]	ID1[5]	ID1[4]	ID1[3]	ID1[2]	ID1[1]	ID1[0]	00												
			A101h	x	ID1[15]	ID1[14]	ID1[13]	ID1[12]	ID1[11]	ID1[10]	ID1[9]	ID1[8]	00												
			A102h	x	ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]	00												
			A103h	x	ID2[15]	ID2[14]	ID2[13]	ID2[12]	ID2[11]	ID2[10]	ID2[9]	ID2[8]	00												
			A104h	x	ID3[7]	ID3[6]	ID3[5]	ID3[4]	ID3[3]	ID3[2]	ID3[1]	ID3[0]	00												
			A105h	x	ID3[15]	ID3[14]	ID3[13]	ID3[12]	ID3[11]	ID3[10]	ID3[9]	ID3[8]	00												
			A106h	x	1	1	1	1	1	1	1	1	FF												
Description	1 st parameter: Dummy read 2 nd parameter: Supplier ID code 3 rd parameter: Supplier ID code 4 th parameter: Module ID 5 th parameter: Module ID 6 th parameter: Revision ID 7 th parameter: Revision ID																								
Restriction																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								

	Status	Default Value	
		After MTP	Before MTP
Default	Power On Sequence	MTP Value	00h
	SW Reset	MTP Value	00h
	HW Reset	MTP Value	00h

Flow Chart	Serial I/F Mode		Parallel I/F Mode	
	RDDDBS (A1h)	Dummy Clock	RDDDBS (A1h)	Dummy Read
		Send ID1[15:8]		Send ID1[15:8]
		Send ID1[7:0]		Send ID1[7:0]
		Send ID2[15:8]		Send ID2[15:8]
		Send ID2[7:0]		Send ID2[7:0]
		Send FFh		Send FFh

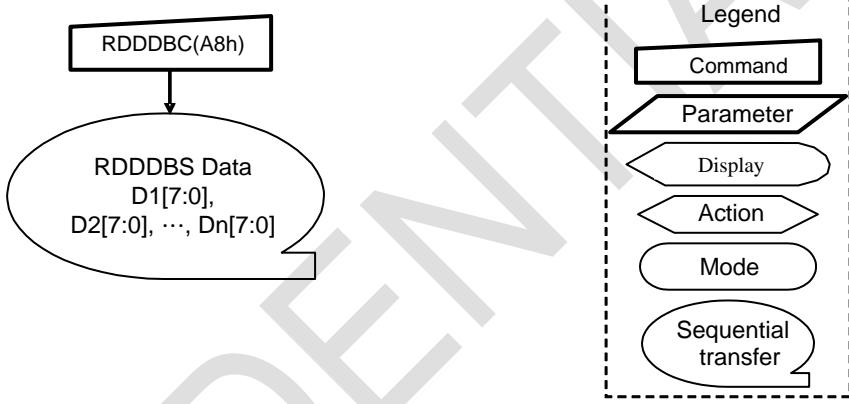
Host Driver

Legend

- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer

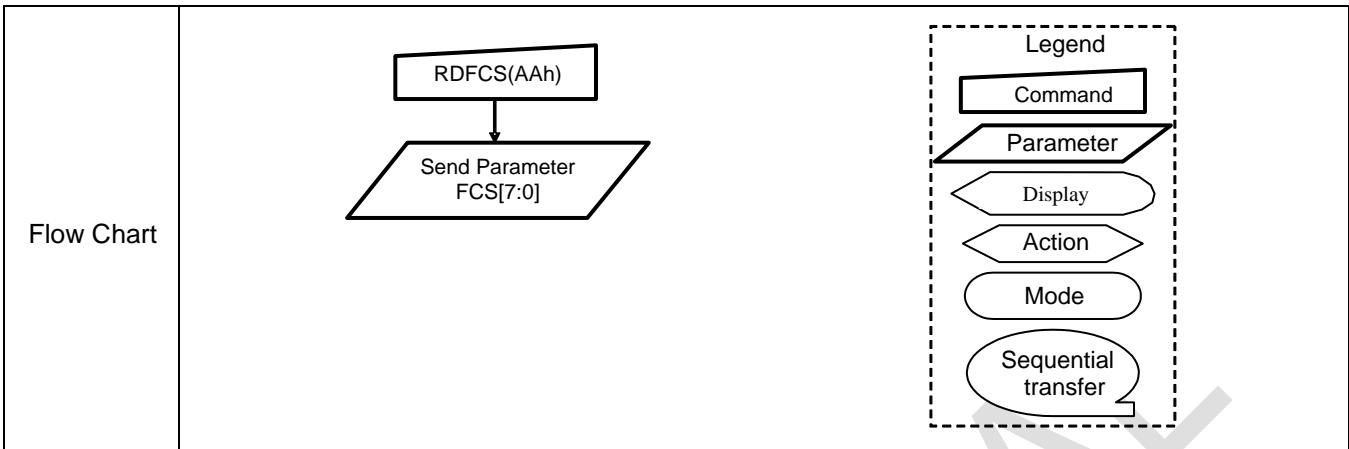
RDDDBC(A800h) : Read DDB Continous

Inst/Para	R/W	RDDDBC																							
		Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
		MIPI	Other																						
RDDDBC	R	A8h	A800h	x	ID1[7]	ID1[6]	ID1[5]	ID1[4]	ID1[3]	ID1[2]	ID1[1]	ID1[0]	00												
			A801h	x	ID1[15]	ID1[14]	ID1[13]	ID1[12]	ID1[11]	ID1[10]	ID1[9]	ID1[8]	00												
			A802h	x	ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]	00												
			A803h	x	ID2[15]	ID2[14]	ID2[13]	ID2[12]	ID2[11]	ID2[10]	ID2[9]	ID2[8]	00												
			A804h	x	ID3[7]	ID3[6]	ID3[5]	ID3[4]	ID3[3]	ID3[2]	ID3[1]	ID3[0]	00												
			A805h	x	ID3[15]	ID3[14]	ID3[13]	ID3[12]	ID3[11]	ID3[10]	ID3[9]	ID3[8]	00												
			A806h	x	1	1	1	1	1	1	1	1	FF												
Description	<p>This command returns the supplier identification and display module mode/revision information from the point where RDDDBS command was interrupted by an other command.</p> <p><i>Note: Parameter 0xFF is an "Exit Code", this means that there is no more data in the DDB block.</i></p> <p><i>Note: For use example,</i></p> <ol style="list-style-type: none"> 1. Set maximum return packet size=3 2. Read 0xA1, return 3 bytes SID[7:0], SID[15:8], MID[7:0] 3. Read 0xA8, return 2 bytes MID[15:8], RID[7:0], RID[15:8] and 0xFF 																								
Restriction	<p>A Read DDB Start command (RDDDBS) should be executed at least once before a Read DDB Continue command (RDDDBC) to define the read location. Otherwise, data read with a Read DDB Continue command is undefined.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								

	Status	Default Value	
		After MTP	Before MTP
Default	Power On Sequence	MTP Value	00h
	SW Reset	MTP Value	00h
	HW Reset	MTP Value	00h
Flow Chart	 <pre>graph TD; A[RDDDBC(A8h)] --> B((RDDDBS Data D1[7:0], D2[7:0], ..., Dn[7:0]))</pre> <p>Legend:</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer		

RDFCS(AA00h) : Read First Checksum

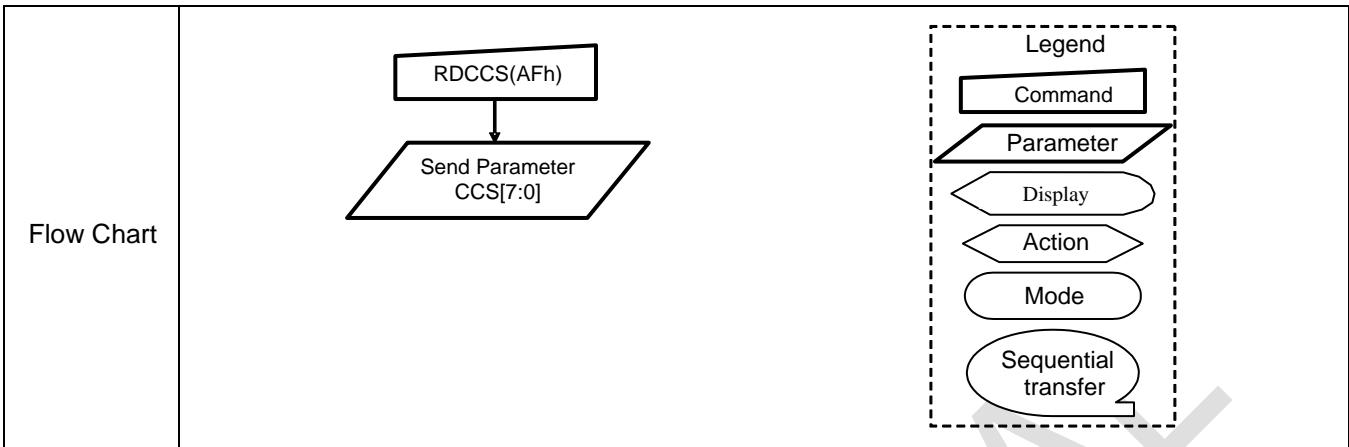
AA00H		RDFCS																																																																																								
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																													
		MIPI	Other																																																																																							
RDFCS	R	AAh	AA00h	x	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0	00																																																																													
Description	This command returns the first checksum what has been calculated from "User Command Set" area registers (not include "Manufacture Command Set") and the frame memory after the write access to those registers and/or frame memory has been done.																																																																																									
Restriction	It will be necessary to wait 150ms after there is the last write access on "User Command Set" area registers before there can read this checksum value.																																																																																									
Register Availability	<table border="1"> <thead> <tr> <th colspan="6">Status</th><th colspan="7">Availability</th></tr> </thead> <tbody> <tr> <td colspan="6">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="7">Yes</td></tr> <tr> <td colspan="6">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="7">Yes</td></tr> <tr> <td colspan="6">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="7">Yes</td></tr> <tr> <td colspan="6">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="7">Yes</td></tr> <tr> <td colspan="6">Sleep In</td><td colspan="7" rowspan="2">Yes</td></tr> </tbody></table>												Status						Availability							Normal Mode On, Idle Mode Off, Sleep Out						Yes							Normal Mode On, Idle Mode On, Sleep Out						Yes							Partial Mode On, Idle Mode Off, Sleep Out						Yes							Partial Mode On, Idle Mode On, Sleep Out						Yes							Sleep In						Yes						
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RDCCS(AF00h) : Read Continue Checksum

AF00H		RDCCS																																																																																									
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																														
		MIPI	Other																																																																																								
RDCCS	R	AFh	AF00h	x	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0	00																																																																														
Description	This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from "User Command Set" area registers and the frame memory after the write access to those registers and/or frame memory has been done.																																																																																										
Restriction	It will be necessary to wait 300ms after there is the last write access on "User Command Set" area registers before there can read this checksum value in the first time.																																																																																										
Register Availability	<table border="1"> <thead> <tr> <th colspan="6">Status</th><th colspan="7">Availability</th></tr> </thead> <tbody> <tr> <td colspan="6">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="7">Yes</td></tr> <tr> <td colspan="6">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="7">Yes</td></tr> <tr> <td colspan="6">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="7">Yes</td></tr> <tr> <td colspan="6">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="7">Yes</td></tr> <tr> <td colspan="6">Sleep In</td><td colspan="7" rowspan="2">Yes</td></tr> </tbody></table>													Status						Availability							Normal Mode On, Idle Mode Off, Sleep Out						Yes							Normal Mode On, Idle Mode On, Sleep Out						Yes							Partial Mode On, Idle Mode Off, Sleep Out						Yes							Partial Mode On, Idle Mode On, Sleep Out						Yes							Sleep In						Yes						
Status						Availability																																																																																					
Normal Mode On, Idle Mode Off, Sleep Out						Yes																																																																																					
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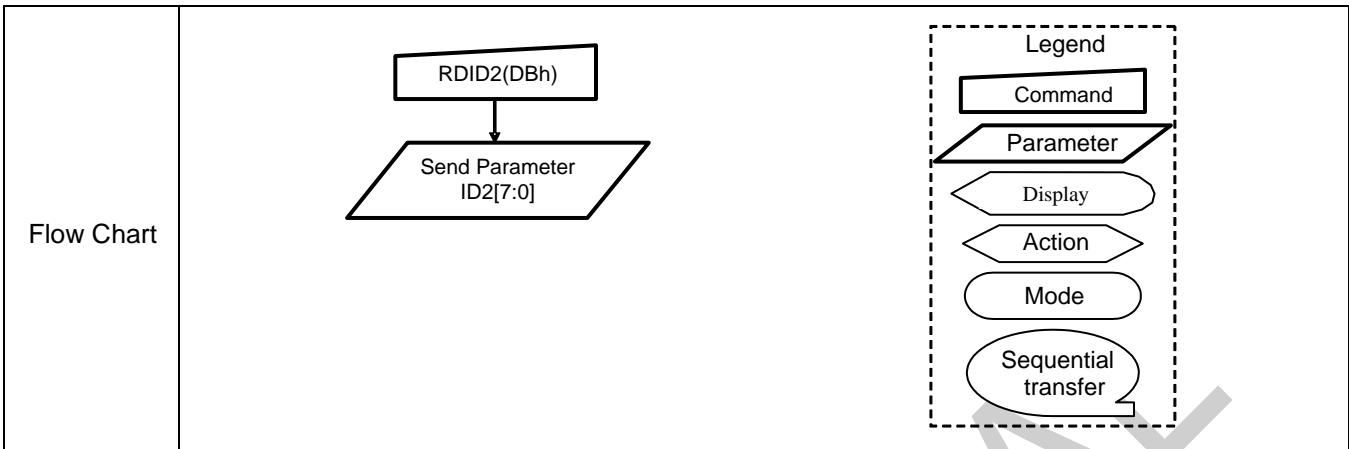


RDID1(DA00h) : Read ID1

DA00H	RDID1												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDID1	R	DAh	DA00h	x	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	00
Description	This read byte identifies the LTPS AMOLED module's manufacture ID.												
Restriction	-												
Register Availability	Status								Availability				
	Normal Mode On, Idle Mode Off, Sleep Out								Yes				
	Normal Mode On, Idle Mode On, Sleep Out								Yes				
	Partial Mode On, Idle Mode Off, Sleep Out								Yes				
	Partial Mode On, Idle Mode On, Sleep Out								Yes				
	Sleep In								Yes				
Default	Status								Default Value				
	Power On Sequence								00h				
	SW Reset								00h				
	HW Reset								00h				
Flow Chart	<pre> graph TD RDID1["RDID1(DAh)"] --> SendParam[/Send Parameter ID1[7:0]/] </pre> <p>The flowchart starts with a rectangular box labeled "RDID1(DAh)". An arrow points down to a trapezoidal box labeled "Send Parameter ID1[7:0]".</p> <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div>												

RDID2(DB00h) : Read ID2

Inst/Para	RDID2																								
	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
		MIPI	Other																						
RDID2	R	DBh	DB00h	x	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80												
Description	<p>This read byte is used to track the LTPS AMOLED module/driver version. It is changed each time a version is made to the display, material or construction specifications.</p> <p>Parameter Range: ID2 = 80h to FFh</p>																								
Restriction	-																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>After MTP</th> <th>Before MTP</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>MTP Value</td> <td>80h</td> </tr> <tr> <td>SW Reset</td> <td>MTP Value</td> <td>80h</td> </tr> <tr> <td>HW Reset</td> <td>MTP Value</td> <td>80h</td> </tr> </tbody> </table>												Status	Default Value		After MTP	Before MTP	Power On Sequence	MTP Value	80h	SW Reset	MTP Value	80h	HW Reset	MTP Value	80h
Status	Default Value																								
	After MTP	Before MTP																							
Power On Sequence	MTP Value	80h																							
SW Reset	MTP Value	80h																							
HW Reset	MTP Value	80h																							



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RDID3(DC00h) : Read ID3

DC00H	RDID3												
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDID3	R	DCh	DC00h	x	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	00
Description	This parameter read byte identifies the LTPS AMOLED module/driver.												
Restriction	-												
Register Availability	Status							Availability					
	Normal Mode On, Idle Mode Off, Sleep Out							Yes					
	Normal Mode On, Idle Mode On, Sleep Out							Yes					
	Partial Mode On, Idle Mode Off, Sleep Out							Yes					
	Partial Mode On, Idle Mode On, Sleep Out							Yes					
	Sleep In							Yes					
Default	Status							Default Value					
								After MTP		Before MTP			
	Power On Sequence							MTP Value		00h			
	SW Reset							MTP Value		00h			
Flow Chart	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer <pre> graph TD RDID3[DID3(DCh)] --> SendParam[/Send Parameter ID3[7:0]/] </pre>												

9. Electrical Characteristics

9.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When RM69032 is used out of the absolute maximum ratings, the RM69032 may be permanently damaged. To use the RM69032 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the RM69032 will malfunction and cause poor reliability.

item	Symbol	Value	Unit
Power supply voltage	VDDI	-0.3 ~ + 5.5	V
Power supply voltage	VDDA, VDBB, VDDR, VDDAM	-0.3 ~ + 5.5	V
Supply voltage (Digital)	DVDD, DIOPWR	-0.3 ~ + 2.0	V
Supply voltage (MV)	AVDD-AVSS	-0.3 ~ + 6.6	V
	AVEE-AVSS	-0.3 ~ + 6.6	V
Supply voltage (HV)	VGH - VGLX	-0.3 ~ + 33	V
Input voltage	VIN	-0.3 ~ VDDI+ 0.3	V
Output voltage	VO	-0.3 ~ VDDI+ 0.3	V
Differential input voltage	HSSI_CLK_P/N	-0.3 ~ +1.8	V
	HSSI_DATA0_P/N		
	HSSI_DATA1_P/N		
Operating temperature	Topr	-40 ~ + 85	°C
Storage temperature	Tstg	-55 ~ + 125	°C

Notes:
If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation. Therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

9.2 ESD Protection Level

Model	Test Condition	Level
Human Body Mode	R = 1.5 kohm / C = 100 pF	> 2KV
Machine Mode	R = 0 ohm / C = 200 pF	> 200V

9.3 Latch-Up Protection Level

The device will not latch up at trigger current levels less than ±200 mA.

9.4 Light Sensitivity

The operation of the IC will not be materially altered by incident light.

9.5 DC Characteristics

9.5.1 Basic Characteristics

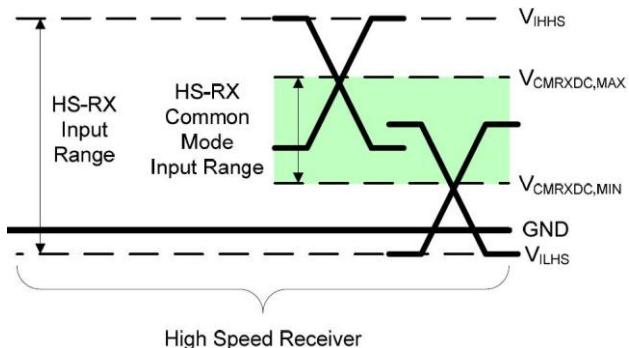
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Related Pins
Analog Power Supply Voltage	VCI	Operation Voltage	2.3	3.7	4.8	V	Note 1
I/O pin Power Supply Voltage	VDDI	I/O supply voltage	1.65	2.8	3.3	V	Note 1
	VDDIL	I/O supply voltage	1.1	1.2	1.3	V	Note 1
Logic High level input voltage	VIH	VDDI = 1.65V ~ 3.3V	0.8* VDDI	-	VDDI	V	Note 2
Logic Low level input voltage	VIL	VDDI = 1.65V ~ 3.3V	0.0	-	0.2* VDDI	V	Note 2
Logic High level Output voltage	VOH	Iout = -1 mA	0.8* VDDI	-	VDDI	V	Note 2
Logic Low level Output voltage	VOL	Iout = +1 mA	0.0	-	0.2* VDDI	V	Note 2
Logic High level input current (Except MIPI/MDDI)	IIHD	Vin=0~VDDI			1	uA	Note 2
Logic Low level input current (Except MIPI/MDDI)	IILD	Vin=0~VDDI	-1			uA	Note 2
Logic High level input current (MIPI/MDDI)	IIHD	Vin=0~VDDAM			1	uA	Note 2
Logic Low level input current (MIPI/MDDI)	IILD	Vin=0~VDDAM	-1			uA	Note 2
AVDD booster voltage	AVDD		4.5		6.5	V	
AVEE booster voltage	AVEE		-6.5		-4.5	V	
VCL booster voltage	VCL		-2.5		-4	V	
VGH booster voltage	VGH		AVDD +VDBB		2AVDD -AVEE	V	
VGLX booster voltage	VGLX		AVEE +VCL		2AVEE -AVDD	V	
Voltage difference between VGH and VGLX	VGHL	VGH-VGLX			30	V	
Gamma reference voltage	VGMP		3.0		6.3	V	Note 3
	VGSP		0.0		3.7	V	Note 3
Output offset voltage	VOFSET				45	mV	Note 3
Output deviation voltage	V _{DEV}	Sout≥4.0V, Sout≤1.0V			20	mV	Note 3
		1.0V < Sout < 4.0V			10	mV	Note 3
RC osc clock	Fosc		18.2	20	21.8	MHz	

Notes: 1. VDDI=1.65 to 3.3V, VDD=2.3 to 4.8V, VSSI=VSS=DVSS=0V, VDD means VDDA, VDDR, VDBB, VDDIM, VDDAM and VSS means VSSA, VSSR, VSSB, AVSS, VSSIM, VSSAM. VDBB, VDDA and VDDR should be the same input voltage level.
 2. TA = -30 to 85 °C.
 3. Source channel loading =13.7KΩ+35.5pF/channel.

9.5.2 MIPI Characteristics

High-Speed Receiver Specification

DC Specifications



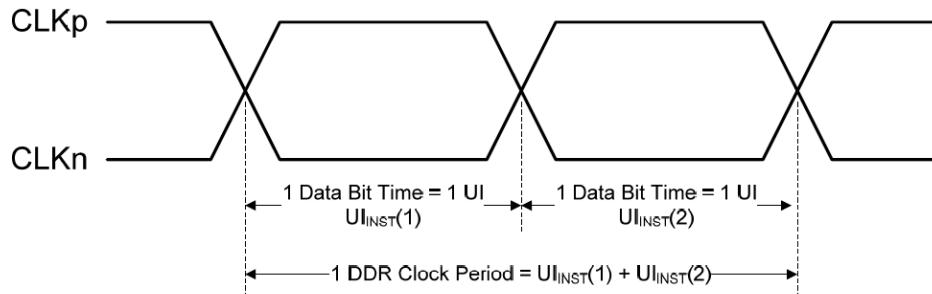
Parameter	Description	Min	Nom	Max	Units	Note
$V_{CMRX}(DC)$	Common-mode voltage HS receive mode	70		330	mV	1,2
VIDTH	Differential input high threshold			70	mV	
VIDTL	Differential input low threshold	-70			mV	
V_{IHHS}	Single-ended input high voltage			460	mV	1
V_{ILHS}	Single-ended input low voltage	-40			mV	1
ZID	Differential input impedance	80	100	125	Ω	

Notes:

1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Forward high speed transmissions

DDR Clock Definition



Clock Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UIINST	2		12.5	ns	1,2

Notes:

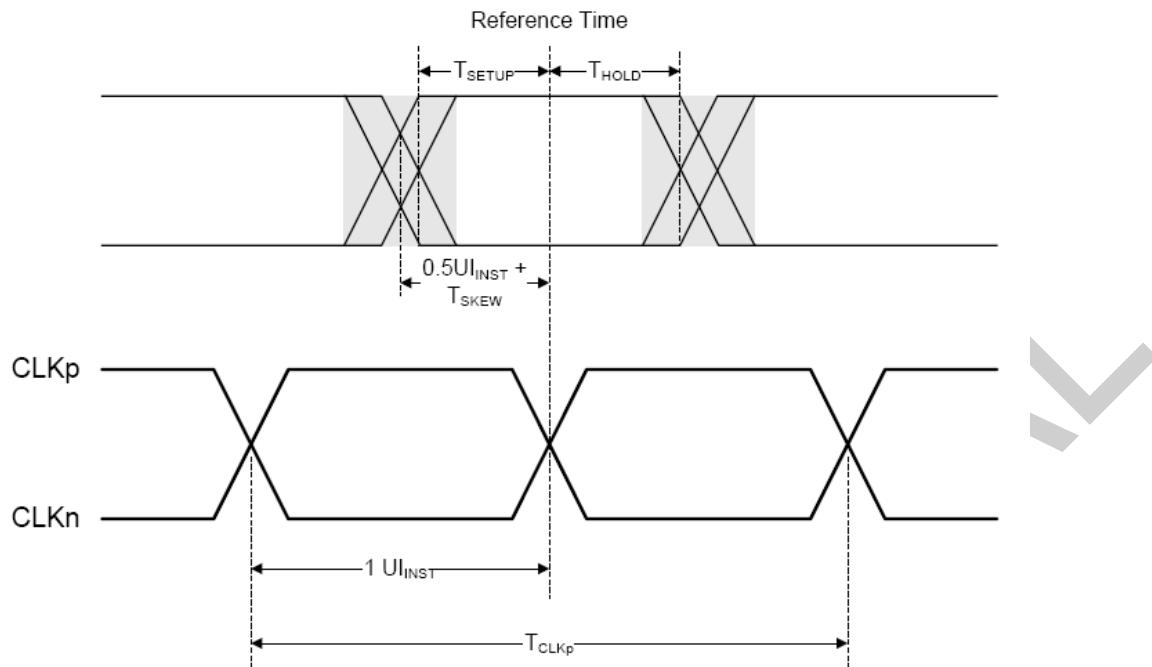
1. This value corresponds to a minimum 80 Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

Data-Clock Timing Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Data to Clock Skew [measured at transmitter]	T _{SKEW[TX]}	-0.15		0.15	UI _{INST}	1
Data to Clock Setup Time [receiver]	T _{SETUP[RX]}	0.15			UI _{INST}	2
Clock to Data Hold Time [receiver]	T _{HOLD[RX]}	0.15			UI _{INST}	2

Notes:

1. Total silicon and package delay budget of 0.3*UI_{INST}
2. Total setup and hold window for receiver of 0.3*UIINST

Data to Clock Timing Definitions

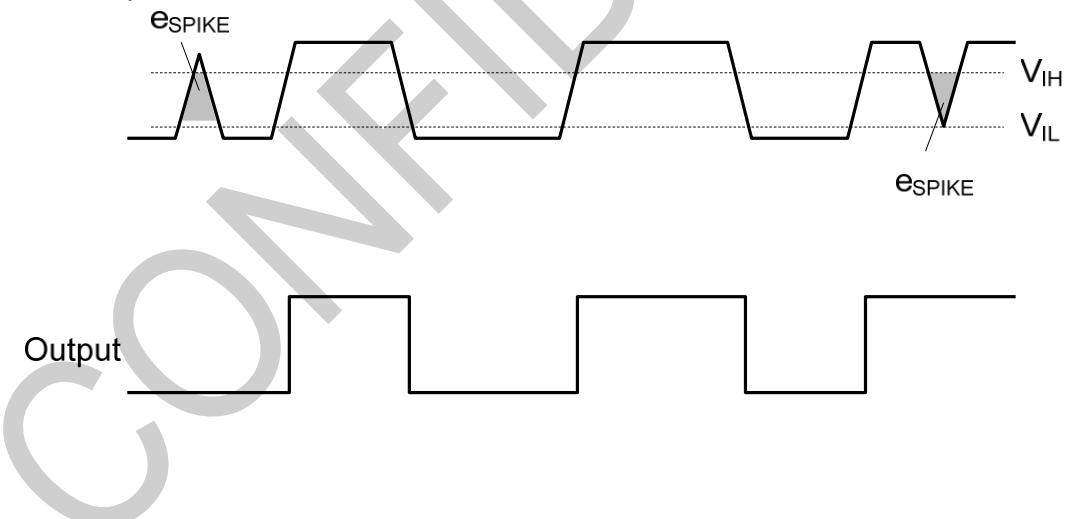
Low power transceiver specifications

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Logic high level input voltage	VIHCD	Contention Detection (Lane_D0)	450		1350	mV
Logic low level input voltage	VILCD	Contention Detection (Lane_D0)	0		200	mV
Logic high level input voltage	VIH-LPRX	LP-Rx (Lane_CK, Lane_D0, Lane_D1)	880	-	1350	mV
Logic low level input voltage	VIL-LPRX	LP-Rx (Lane_CK, Lane_D0, Lane_D1)	0		550	mV
Logic low level input voltage	VIL-ULPS	LP-Rx ULPS (Lane_CK, Lane_D0, Lane_D1)	0		300	mV
Logic high level input voltage	VOH-LPTX	Contention Detection (Lane_D0)	1.1	1.2	1.3	V
Logic low level input voltage	VOL-LPTX	Contention Detection (Lane_D0)	-50	0	50	mV
eSPIKE ^(1,2,3)	Fig. 2	Input pulse rejection			300	V.ps

Notes:

- Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 State.
- An impulse less than this will not change the receiver state.
- In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

Input Glitch Rejection of Low Power Receivers as follow.



9.5.3 MDDI Characteristics

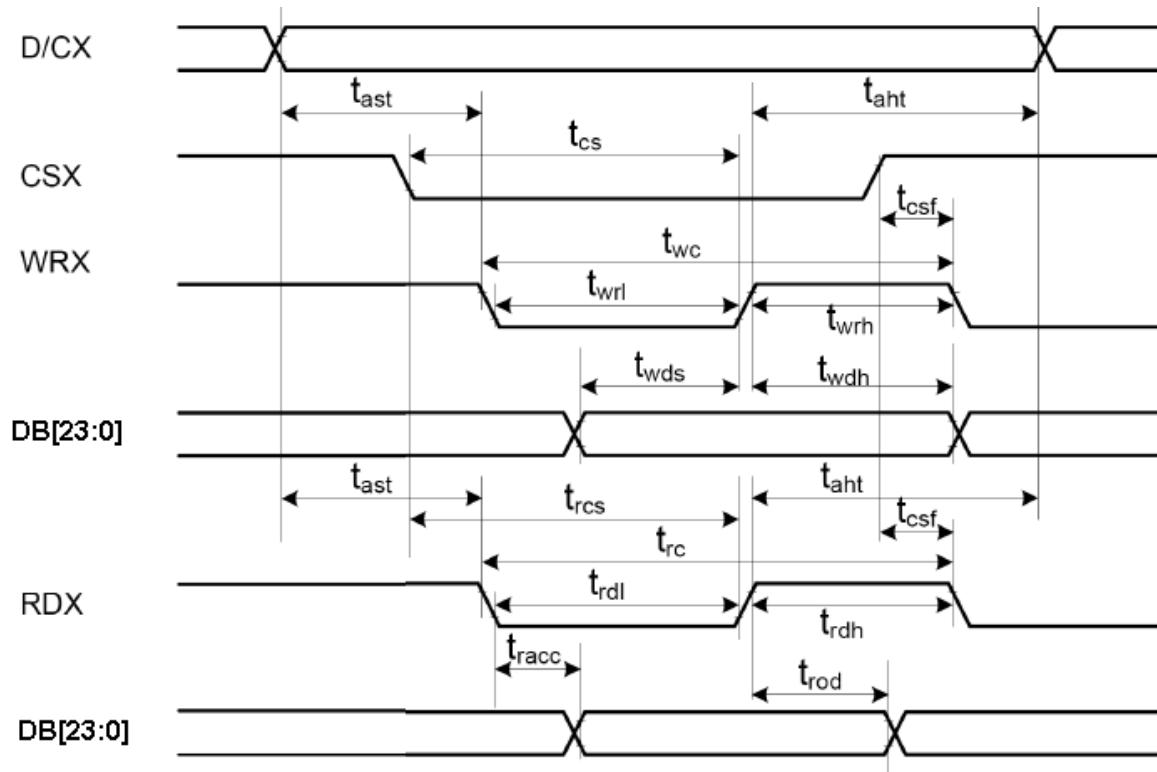
Characteristics

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Differential input "High" level voltage (hibernation wake-up)	V_{IT+} _{offset}	VT=125mv (MDDI_DATA_P/M)	-	100	125	mv
Differential input "Low" level voltage (hibernation wake-up)	V_{IT-} _{offset}	VT=125mv (MDDI_DATA_P/M)	75	100	-	mv
Differential input "High" level voltage	V_{IT+}	VT=0mv (MDDI_STB_P/M ,MDDI_DATA_P/M)	-	0	50	mv
Differential input "Low" level voltage	V_{IT-}	VT=0mv (MDDI_STB_P/M ,MDDI_DATA_P/M)	-50	0	-	mv
Terminal impedance	Zt	-	80	-	125	ohm

Note 1) VDDI= 1.65~3.3V, VDD=2.3 to 4.8V, VSSI=VSS=VSSAM=0V, Ta=-30 to 70 °C (to +85 °C no damage). VDD means VDDAM, VDDA, VDDR, VDDB and VSS means VSSAM, VSSA, VSSR, VSSB, AVSS.

9.6 AC Characteristics

9.6.1 Parallel Interface Characteristics (80-Series MCU)

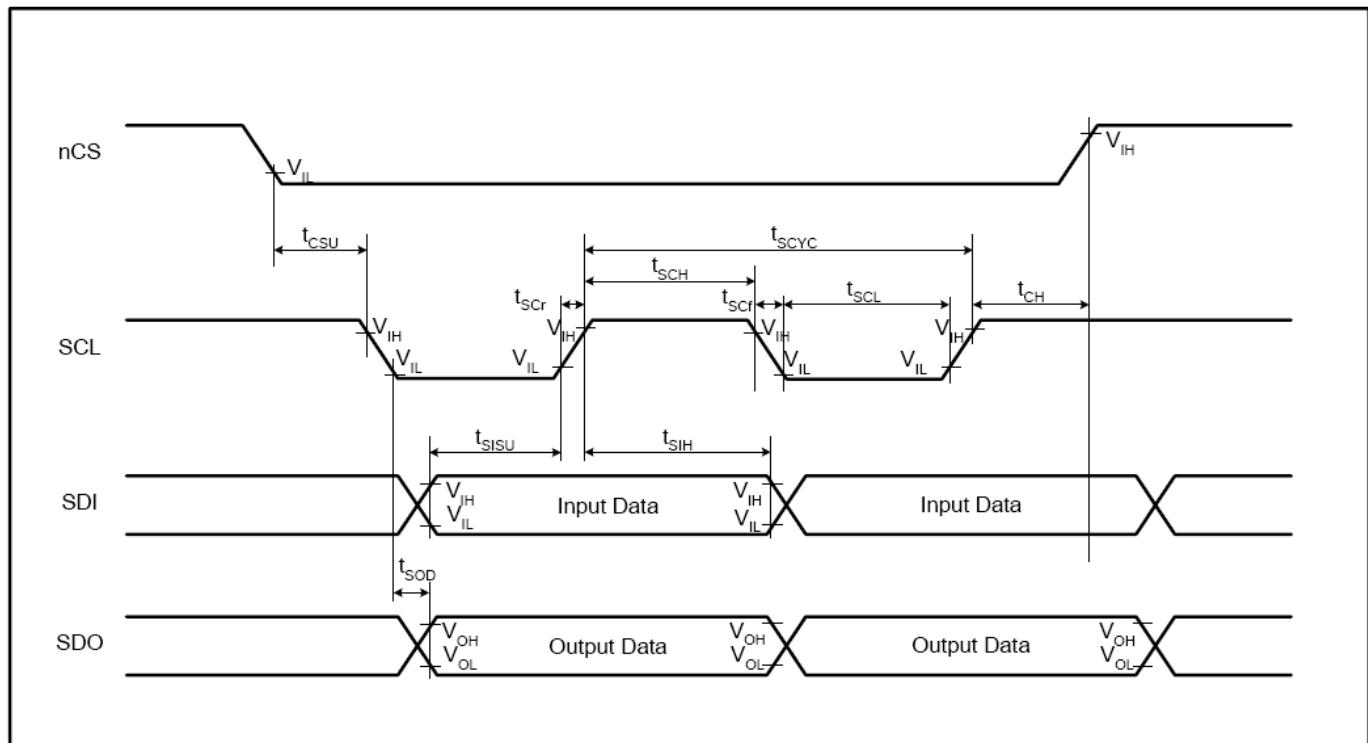


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	T _{ast}	Address setup time	10	-	ns	
	T _{aht}	Address hold time (Write/Read)	2	-	ns	
CSX	T _{cs}	Chip Select setup time (Write)	20	-	ns	
	T _{racs}	Chip Select setup time (Read)	20	-	ns	
	T _{csf}	Chip Select Wait time (Write/Read)	20	-	ns	
WRX	T _{wcs}	Write cycle	33	-	ns	
	T _{wrh}	Write Control pulse H duration	15	-	ns	
	T _{wrl}	Write Control pulse L duration	15	-	ns	
RDX	T _{rc}	Read cycle	400	-	ns	Read from frame memory
	T _{rdh}	Read Control pulse H duration	250	-	ns	
	T _{rdl}	Read Control pulse L duration	150	-	ns	
DB[23:0]	T _{wds}	Write data setup time	15	-	ns	
	T _{wdh}	Write data hold time	10	-	ns	
	T _{racc}	Read access time		150	ns	
	T _{rohd}	Read output disable time	5	-	ns	

Note: Logic high and low levels are specified as 20% and 80% of IOVCC for Input signals.

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.3V to 4.8V, GND=0V

9.6.2 Serial Interface Characteristics

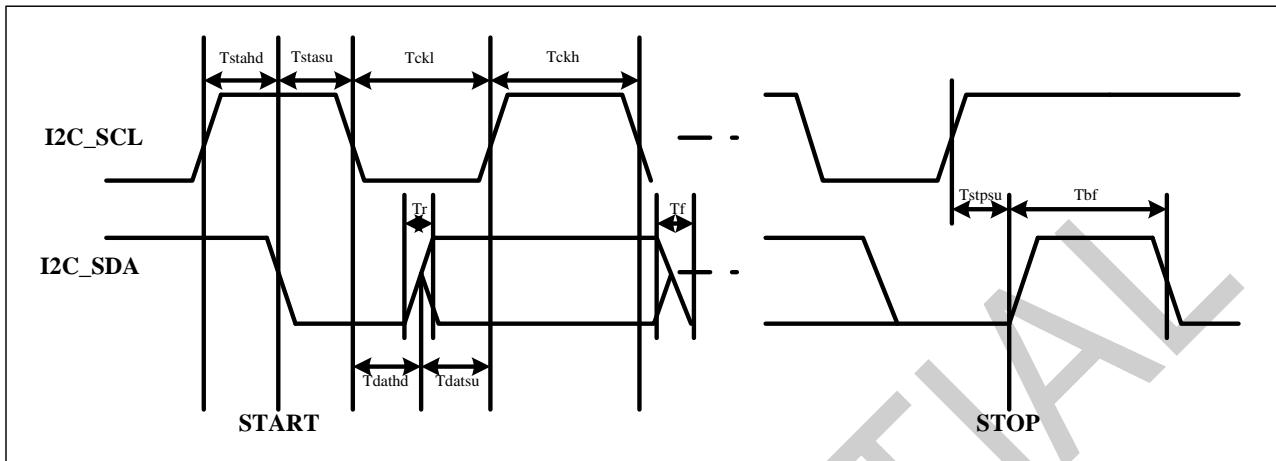


Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	T _{SCYC}	Clock cycle (Write)	100		ns	-
	T _{SCYC}	Clock cycle (Read)	300		ns	
	T _{SCH}	Clock "H" pulse width (Write)	40		ns	
	T _{SCH}	Clock "H" pulse width (Read)	140		ns	
	T _{SCL}	Clock "L" pulse width (Write)	40		ns	
	T _{SCL}	Clock "L" pulse width (Read)	140		ns	
	T _{SCR}	Clock rise time		5	ns	
	T _{SCF}	Clock fall time		5	ns	
nCS	T _{CSU}	Chip select setup time	20		ns	-
	T _{CH}	Chip select hold time	50		ns	
SDI	T _{SISU}	Data input setup time	20		ns	-
	T _{SIH}	Data input hold time	20		ns	
SDO	T _{SOD}	Data output setup time		120	ns	-
	T _{SOH}	Data output hold time	5		ns	

Note: Logic high and low levels are specified as 20% and 80% of IOVCC for Input signals.

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.3V to 4.8V, GND=0V

9.6.3 I2C Bus Timing Characteristics

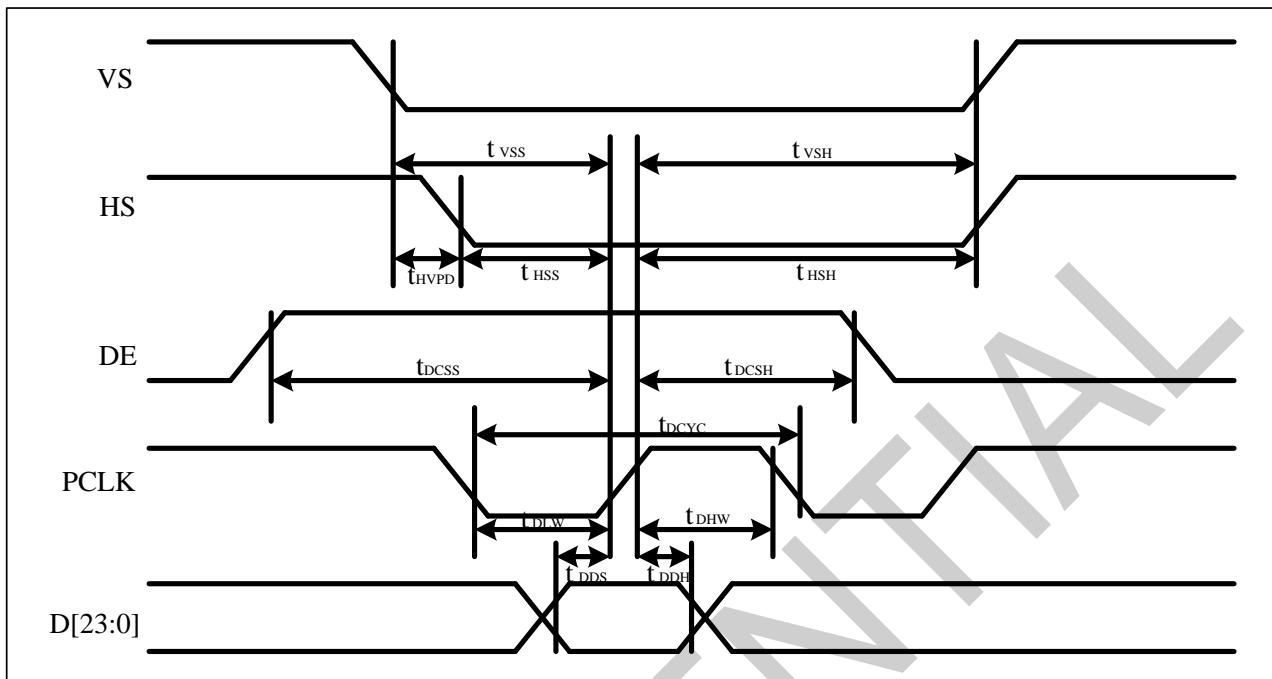


Signal	Symbol	Parameter	MIN	MAX	Unit
I2C_SCL	Tckl + Tckh	Operate frequency	-	400	KHz
	Tckl	CLK low	1300	-	ns
	Tckh	CLK high	600	-	ns
I2C_SDA	Tr	Data rising time	-	300	ns
	Tf	Data falling time	-	300	ns
	Tdathd	Data hold time	0	900	ns
	Tdatsu	Data setup time	100	-	ns
	Tstahd	Start hold time	600	-	ns
	Tstasu	Start setup time	600	-	ns
	Tstpsu	Stop setup time	600	-	ns
	Tbf	Bus free time	1300	-	ns

Note: Logic high and low levels are specified as 20% and 80% of IOVCC for Input signals.

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.3V to 4.8V, GND=0V

9.6.4 RGB Interface Characteristics



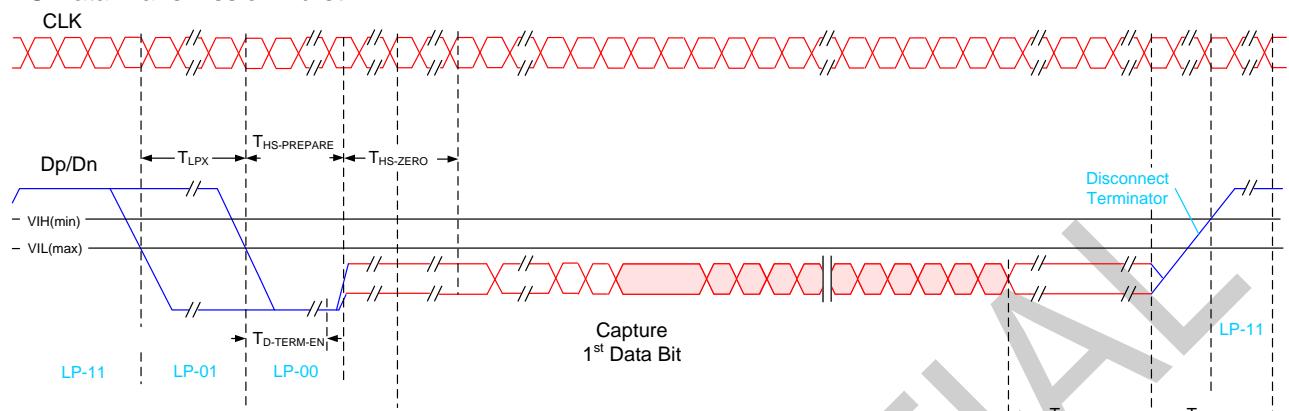
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit
VS	t _{VSS}	VS setup time	10	-	-	ns
	t _{VSH}	VS hold time	10	-	-	ns
HS	t _{HSS}	HS setup time	10	-	-	ns
	t _{HSH}	HS hold time	10	-	-	ns
	t _{HVPD}	HS to VS falling edge	400	-	-	ns
PCLK	t _{DCYC}	PCLK cycle time	25	-	125	ns
	t _{DLW}	PCLK low pulse width	11	-	-	ns
	t _{DHW}	PCLK high pulse width	11	-	-	ns
	f _{DFREQ}	PCLK frequency	8	-	40	MHz
DE	t _{DCSS}	DE setup time	10	-	-	ns
	t _{DCSH}	DE hold time	10	-	-	ns
D[23:0]	t _{DDS}	Data setup time	10	-	-	ns
	t _{DDH}	Data hold time	10	-	-	ns

Note: Logic high and low levels are specified as 20% and 80% of IOVCC for Input signals.

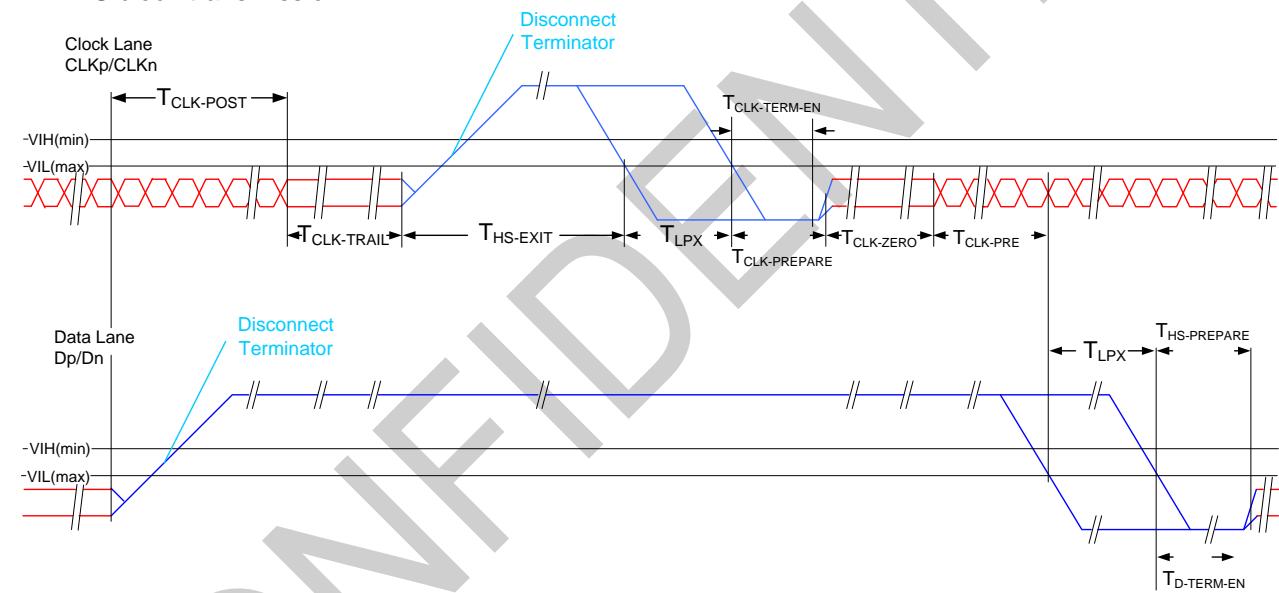
Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.3V to 4.8V, GND=0V

9.6.5 DSI Timing Characteristics

HS Data Transmission Burst



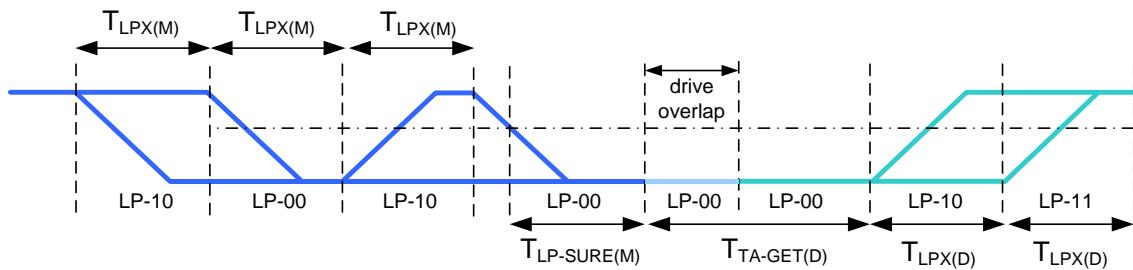
➤ HS clock transmission



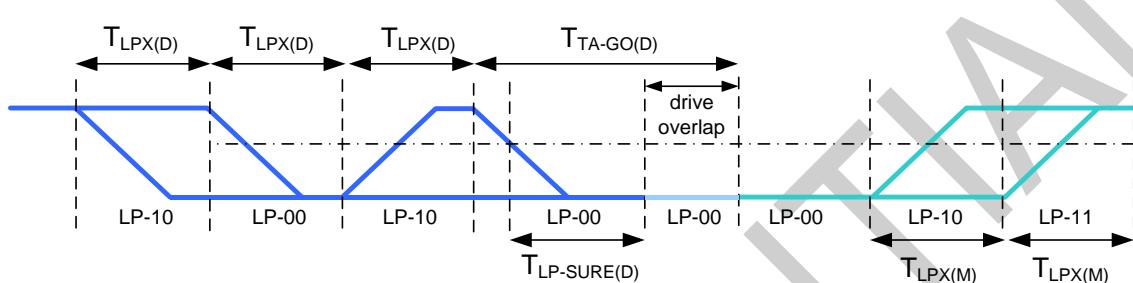
Timing Parameters:

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns

➤ Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

Low Power Mode :

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	$5*T_{LPX(D)}$			ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	$4*T_{LPX(D)}$			ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns	2

NOTE:

- T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
- Transmitter-specific parameters

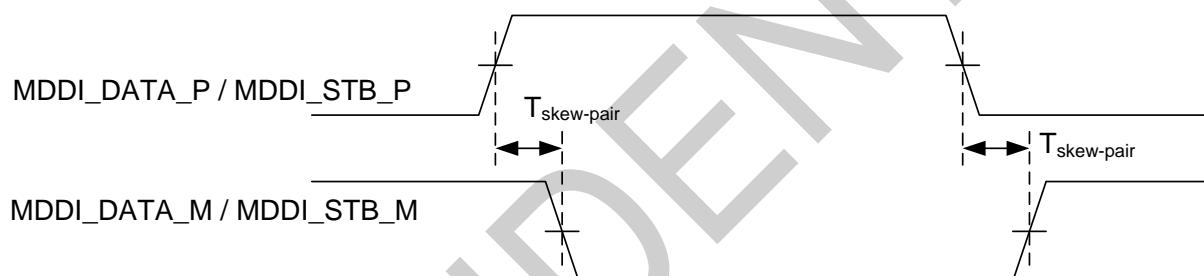
9.6.6 MDDI Timing Characteristics

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V, Ta = -30 to 70°C)

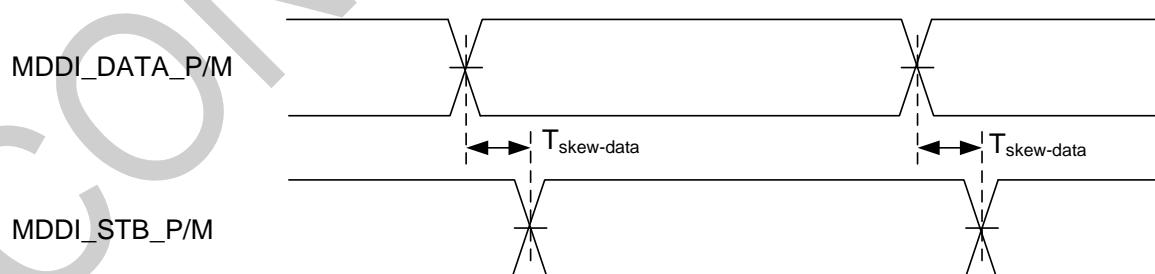
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit
MDDI_STB_P/M	1/Tbit	Data transfer rate	-	384	450	Mbps
MDDI_STB_P/M	Tskew-pair	Differential transfer input skew	-	-	0.05	ns
MDDI_STB_P/M	Tskew-data	Data/Strobe input skew	-	-	0.3	ns

Note) MDDI_DATA_P/M = MDDI_DATA0_P/M and MDDI_DATA1_P/M.

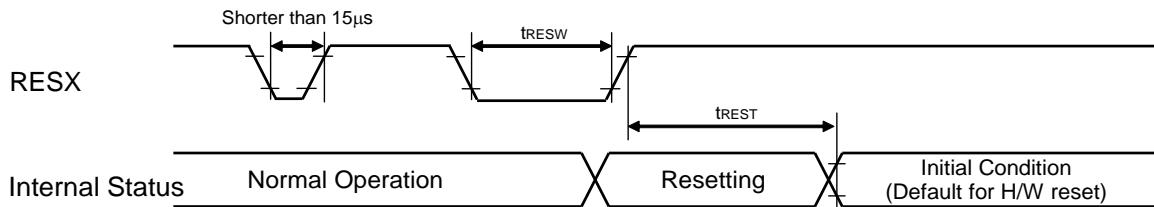
Skew between MDDI positive and negative signal pair



Skew between MDDI_DATA_P/M and MDDI_STB_P/M



9.6.7 Reset Timing



Reset input timing:

$IOVCC=1.65$ to $3.6V$, $VCI=2.3$ to $4.8V$, $AGND=DGND=0V$, $T_a=-40$ to $85^{\circ}C$

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	15	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

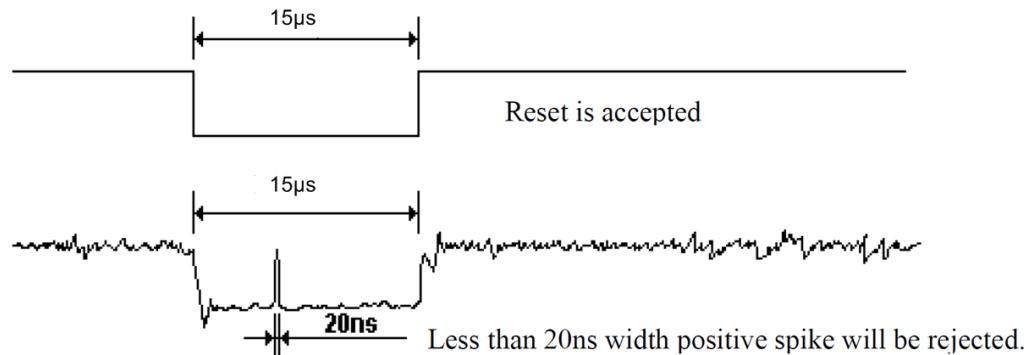
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 15μs	Reset
Between 5μs and 15μs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.