



»» **DATA SHEET**

( DOC No. HX8347-A01-DS )

»» **HX8347-A01**

240RGB x 320 dot, 262K color,  
with internal GRAM,  
TFT Mobile Single Chip Driver  
*Version 03 April, 2008*

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## 1. General Description

This document describes HX8347-A01 240RGBx320 dots resolution driving controller. The HX8347-A01 is designed to provide a single-chip solution that combines a gate driver, a source driver, power supply circuit for 262,144 colors to drive a TFT panel with 240RGBx320 dots at maximum.

The HX8347-A01 can be operated in low-voltage (1.65V) condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8347-A01 also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8347-A01 is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

The HX8347-A01 supports three interface modes: Command-Parameter interface mode, Register-Content interface mode and RGB interface mode. Command-Parameter interface mode and Register-Content interface mode are selected by the external pins IFSEL0 setting, and RGB interface mode is selected by internal bit RGB\_EN.

This manual description focuses on Register-Content interface mode and RGB interface mode, about the Command-Parameter interface mode, please refer to the HX8347-A(N) datasheet for detail.

## 2. Features

### 2.1 Display

- Resolution: 240(H) x RGB(H) x 320(V)
- Display Color modes
  - A. Normal Display Mode On
    - a. Command-Parameter interface mode
      - i. 262,144(R(6),G(6),B(6)) colors
    - b. Register-Content interface mode
      - i. 262,144(R(6),G(6),B(6)) colors
      - ii. 65,536(R(5),G(6),B(5)) colors
  - B. Idle Mode On
    - a. 8 (R(1),G(1),B(1)) colors.

### 2.2 Display Module

- AM-LCD glass 240xRGBx320
- Gamma correction (4 preset gamma curves)
- On module VCOM control (-2.0 to 5.5V Common electrode output voltage range)
- On module DC/DC converter
  - A. DDVDH = 4.6 to 6.0V (Source output voltage range)
  - B. VGH = +9.0 to +16.5V (Positive Gate output voltage range)
  - C. VGL = -6.0 to -13.5V (Negative Gate output voltage range)
- Frame Memory area 240 (H) x 320 (V) x 18 bit

### 2.3 Display/Control Interface

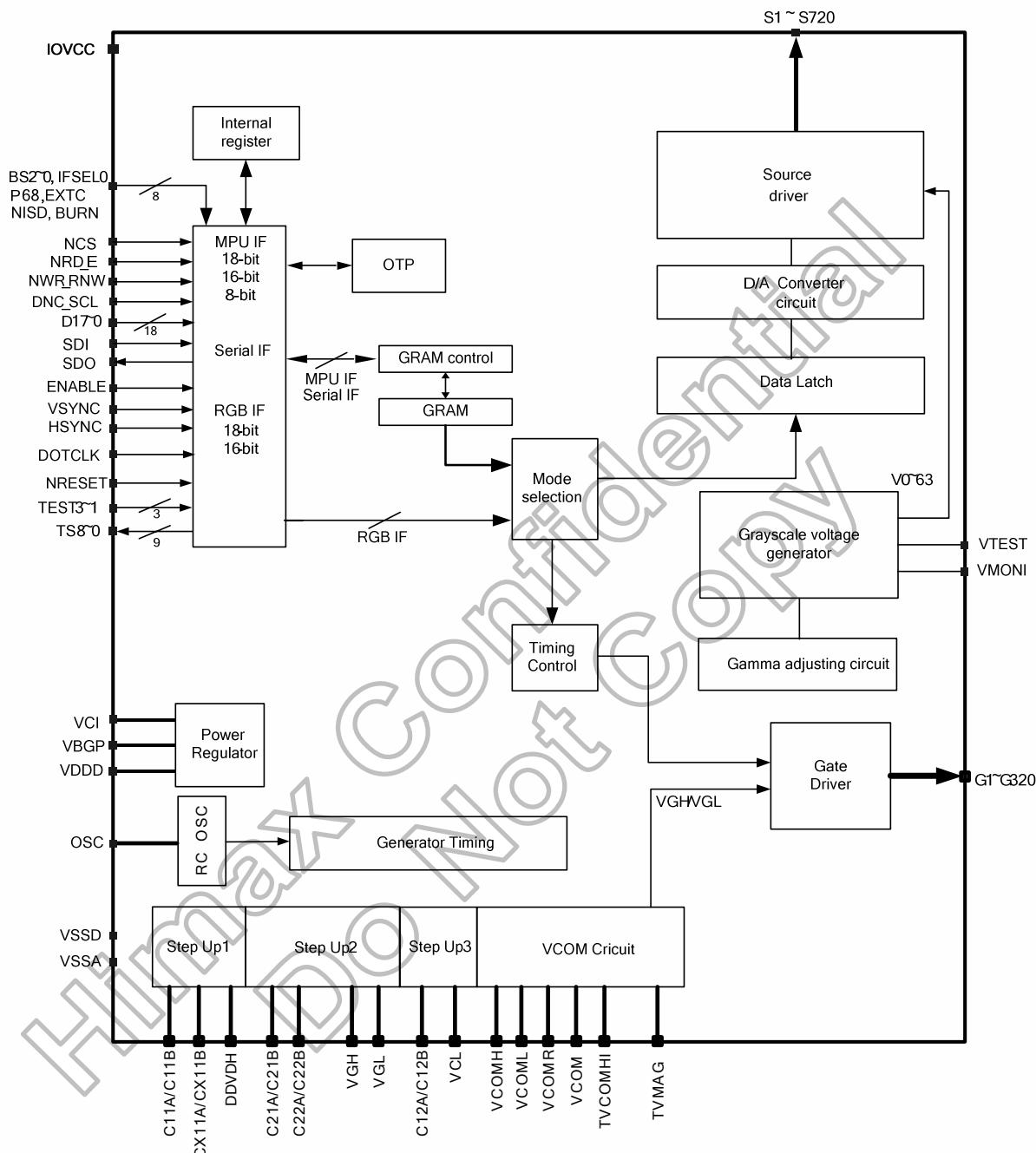
- Display Interface types supported
  - A. Command-Parameter interface mode
    - 8-/16-bit MPU parallel interface.
    - Serial data transfer interface.
    - 16, 18 data lines parallel video (RGB) interface.
  - B. Register-Content interface mode
    - 8-/16-/18-bit MPU parallel interface.
    - Serial data transfer interface.
    - 16, 18 data lines parallel video (RGB) interface.
- Control Interface types supported
  - A. Command-Parameter interface mode.( IFSEL0= 0 )
  - B. Register-Content interface mode (IFSEL0 = 1)
- Logic voltage (IOVCC): 1.65 ~ 3.3V
- Driver power supply (VCI): 2.3 ~ 3.3V
- Color modes
  - A. 16 bit/pixel: R(5), G(6), B(5)
  - B. 18 bit/pixel: R(6), G(6), B(6)

## 2.4 Miscellaneous

- Low power consumption, suitable for battery operated systems
- Image sticking eliminated function
- CMOS compatible inputs
- Optimized layout for COG assembly
  - Temperature range: -40 ~ +85 °C
- Proprietary multi phase driving for lower power consumption
- Support external VDDD for lower power consumption (such as 1.8 volts input)
- Support RGB through mode with lower power consumption
- Support normal black/normal white LCD
- Support wide view angle display
- Support burn-in mode for efficient test in module production
- On-chip OTP (one-time-programming) non-volatile memory

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### 3. Block Diagram



## 4. Pin Description

### 4.1 Pin Description

Input Parts									
Signals	I/O	Pin Number	Connected with	Description					
P68, BS2,BS1,BS0	I	4	VSSD/ IOVCC	Select the MPU interface mode as listed below Use with <b>IFSEL0=1</b> Register-content interface mode					
				P68   BS2   BS1   BS0	Interface mode	DB pins			
				0   0   0   0	16-bit bus interface, 80-system, 65K-Color	D17-D16: Unused, D15-D0: Data			
				0   0   0   1	16-bit bus interface, 80-system, 262K-color	D17-D16: Unused, D15-D0: Data			
				0   0   1   0	18-bit bus interface, 80-system, 262K-color	D17-D0: Data			
				0   0   1   1	8-bit bus interface, 80-system, 262K-Color	D17-D8: Unused D7-D0: Data			
				0   1   0   0	16-bit bus interface, 80-system, 262K-Color	D17-D16: Unused D15-D0: Data			
				0   1   0   1	18-bit bus interface, 80-system, 262K-color	D17-D0: Data			
				1   0   0   0	16-bit bus interface, 68-system, 65K-Color	D17-D16: Unused, D15-D0: Data			
				1   0   0   1	16-bit bus interface, 68-system, 262K-color	D17-D16: Unused, D15-D0: Data			
				1   0   1   0	18-bit bus interface, 68-system, 262K-Color	D17-D0: Data			
				1   0   1   1	8-bit bus interface, 68-system, 262K-color	D17-D8: Unused D7-D0: Data			
				1   1   0   0	16-bit bus interface, 68-system, 262K-Color	D17-D16: Unused D15-D0: Data			
				1   1   0   1	18-bit bus interface, 68-system, 262K-color	D17-D0: Data			
				X   1   1   ID	Serial bus IF	DNC_SCL, SDO,SDI			
IFSEL0	I	1	MPU	Interface format select pin					
				IFSEL0	Interface Format Selection				
				0	Command-Parameter interface mode				
				1	Register-content interface mode				
				In this case, the IFSEL0 has to be connected to IOVCC.					
EXTC	I	1	MPU	When operate in Register-content interface mode, the EXTC has to be connected to IOVCC or VSSD.					
NCS	I	1	MPU	Chip select signal. Low: chip can be accessed; High: chip cannot be accessed. Must be connected to VSSD if not in use.					
NWR_RNW	I	1	MPU	I80 system: Serves as a write signal and writes data at the rising edge. M68 system: 0: Write, 1: Read. Fix it to IOVCC or VSSD level when using serial buss interface.					
NRD_E	I	1	MPU	I80 system: Serves as a read signal and read data at the low level. M68 system: 0: Read/Write disable, 1: Read/Write enable. Fix it to IOVCC or VSSD level when using serial buss interface.					
BURN	I	1	MPU	Free Running mode If BURN=Hi, this can enable free running mode for burn in test. The display data alternates between full black and full white independent of input data in free running mode.					
SDI	I	1	MPU	Serial data input pin. If not used, please let it connected to IOVCC or VSSD.					
DNC_SCL	I	1	MPU	The signal for command or parameter select under parallel mode(i.e. Not serial interface): Low: command. High: parameter. When under serial interface, it servers as SCL.					
VSYNC	I	1	MPU	Frame synchronizing signal. <b>If not used, please let it connected to IOVCC or VSSD.</b>					
HSYNC	I	1	MPU	Frame synchronizing signal. <b>If not used, please let it connected to IOVCC or VSSD.</b>					

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Input Parts				
Signals	I/O	Pin Number	Connected with	Description
ENABLE	I	1	MPU	A data ENABLE signal in RGB I/F mode. <i>If not used, please let it connected to IOVCC or VSSD.</i>
DOTCLK	I	1	MPU	Dot clock signal. <i>If not used, please let it connected to IOVCC or VSSD.</i>
NRESET	I	1	MPU or reset circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
OSC	I	1	Oscillation Resistor	Oscillator input for test purpose. <i>If not used, please let it open or connected to VSSD.</i>
VCOMR	I	1	Resistor or open	A VcomH reference voltage. When adjusting VcomH externally, set registers to halt the VcomH internal adjusting circuit and place a variable resistor between VREG1 and VSSD. Otherwise, leave this pin open and adjust VcomH by setting the internal register of the HX8347-A01.
VGS	I	1	VSSD or external resistor	Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel used.

Output Part				
Signals	I/O	Pin Number	Connected with	Description
S1~S720	O	720	LCD	Output voltages applied to the liquid crystal.
G1~G320	O	320	LCD	Gate driver output pins. These pins output VGH, VGL.(If not used, should be open)
VCOM	O	1	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. Connect this pin to the common electrode in TFT panel.
TE	O	1	MPU	Tearing effect output. <i>If not used, please open this pin.</i>
SDO	O	1	MPU	Serial data output. If not use, let it to open.
NISD	O	1	Open	Image Sticking Discharge signal. This pin is used for monitoring image sticking discharge phenomena. When the NISD goes low, the VGL would be discharged to VSSA. When the NISD goes high, the VGL, Source and VCOM are normal operation.

Input/Output Part				
Signals	I/O	Pin Number	Connected with	Description
C11A,C11B C12A,C12B	I/O	4	Step-up Capacitor	Connect to the step-up capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.
CX11A, CX11B	I/O	2	Step-up Capacitor	Connect to the step-up capacitors for step up circuit 1 operation. Leave this pin open if the internal step-up circuit is not used.
C21A,C21B C22A,C22B	I/O	4	Step-up Capacitor	Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them.
D17~0	I/O	18	MPU	<p>1. 18-bit bi-directional data bus for system interface.            8-bit bus: use D7-D0 and D17-D8 unused.            16-bit bus: use D15-D0 and D17-D16 unused.            18-bit bus: use D17-D0</p> <p>2. 18-bit data bus for RGB interface            16-bit bus: use D17-D13, D11-D1 and D12, D0 unused.            18-bit bus: use D17-D0</p> <p>Those unused pins have to open.            Notice: When register RGB_EN=1 and pin ENABLE=1,            D[17:0] is used as stream image data for display. It means MPU data bus and RGB data bus is shared.</p>

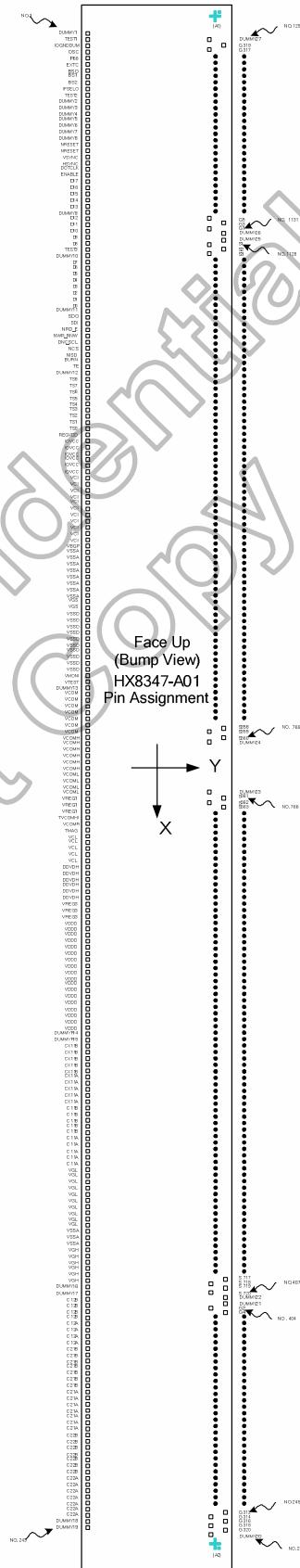
Power Part				
Signals	I/O	Pin Number	Connected with	Description
IOVCC	P	1	Power Supply	Digital IO Pad power supply
VCI	P	1	Power Supply	Analog power supply
VSSD	P	1	Ground	Digital ground
VSSA	P	1	Ground	Analog ground
VDDD	O	1	Stabilizing Capacitor	Output from internal logic voltage (1.6V). Connect to a stabilizing capacitor
REGVDD	I	1	MPU	If REGVDD = high, the internal VDDD regulator will be turned on. If REGVDD = low, the internal VDDD regulator will be turned off, VDDD should connect to external power supply, the VDDD voltage range is 1.65~1.95V. The REGVDD pin must be connected to IOVCC or VSSD.
VBGP	-	1	Open	Band Gap Voltage. Let it to be open.
VREG1	P	1	Stabilizing Capacitor	Internal generated stable power for source driver unit.
VREG3	P	1	Stabilizing Capacitor	A reference voltage for VGH&VGL.
VCOMH	P	1	Stabilizing capacitor	Connect this pin to the capacitor for stabilization. This pin indicates a high level of VCOM amplitude generated in driving the VCOM alternation.
VCOML	P	1	Stabilizing capacitor	When the VCOM alternation is driven, this pin indicates a low level of VCOM amplitude. Connect this pin to a capacitor for stabilization.
VCL	P	1	Stabilizing capacitor	A negative voltage for VCOML circuit, VCL=-VCI
DDVDH	P	1	Stabilizing capacitor	An output from the step-up circuit1. Connect to a stabilizing capacitor between VSSA and DDVDH. Place a schottkey barrier diode (see "configuration of the power supply").
VGH	P	1	Stabilizing capacitor	An output from the step-up circuit2.or 4 ~ 6 time the VCI level. The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSD and VGH. Place a schottkey barrier diode between VCI and VGH. Place a schottkey barrier diode (see "configuration of the power supply").
VGL	P	1	Stabilizing capacitor	An output from the step-up circuit2.or -3 ~ -5 time the VCI level. The step-up rate is determined with BT3-0 bits. Connect to a stabilizing capacitor between VSSD and VGL. Place a schottkey barrier diode between VSSD and VGL. Place a schottkey barrier diode (see "configuration of the power supply").

Test pin and others				
Signals	I/O	Pin Number	Connected with	Description
TEST3-1	I	3	GND	Test pin input (Internal pull low)
TS8~0	O	9	Open	A test pin. Disconnect it.
VMONI	O	1	Open	A test pin. Disconnect it.
VTEST	O	1	Open	Gamma voltage of Panel test pin output. Must be left open.
TVCOMHI	O	1	Open	A test pin output. Must be left open.
TVMAG	O	1	Open	A test pin output. Must be left open.
DUMMYR14-15	-	2	Open	Dummy pads. Available for measuring the COG contact resistance. DUMMYR14 and DUMMYR15 are short-circuited within the chip.
DUMMY1-13 DUMMY16-27	-	25	Open	Dummy pads
IOGNDDUM	O	1	Open	Short-circuited within the chip

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## 4.2 Pin Assignment

- Chip Size: 17820 um x 865 um  
(Including Seal-ring 20 um \*2,  
Scribe line 40 um \*2)
- Chip Thickness: 300 um (typ.)
- Pad Location: Pad center
- Coordinate Origin: Chip center
- Au Bump Size:
  1. 50 um x 120 um  
Input/Output  
(No. 1 ~ No. 243)
  2. 16 um x 98 um  
Staggered LCD output side  
(No. 244 ~ No. 1291)











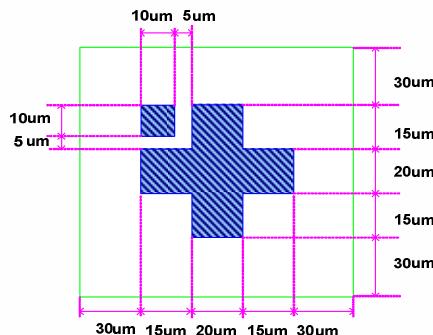
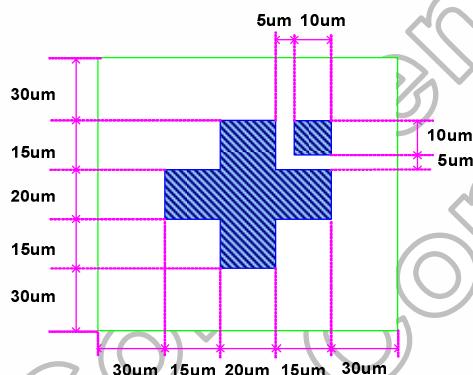


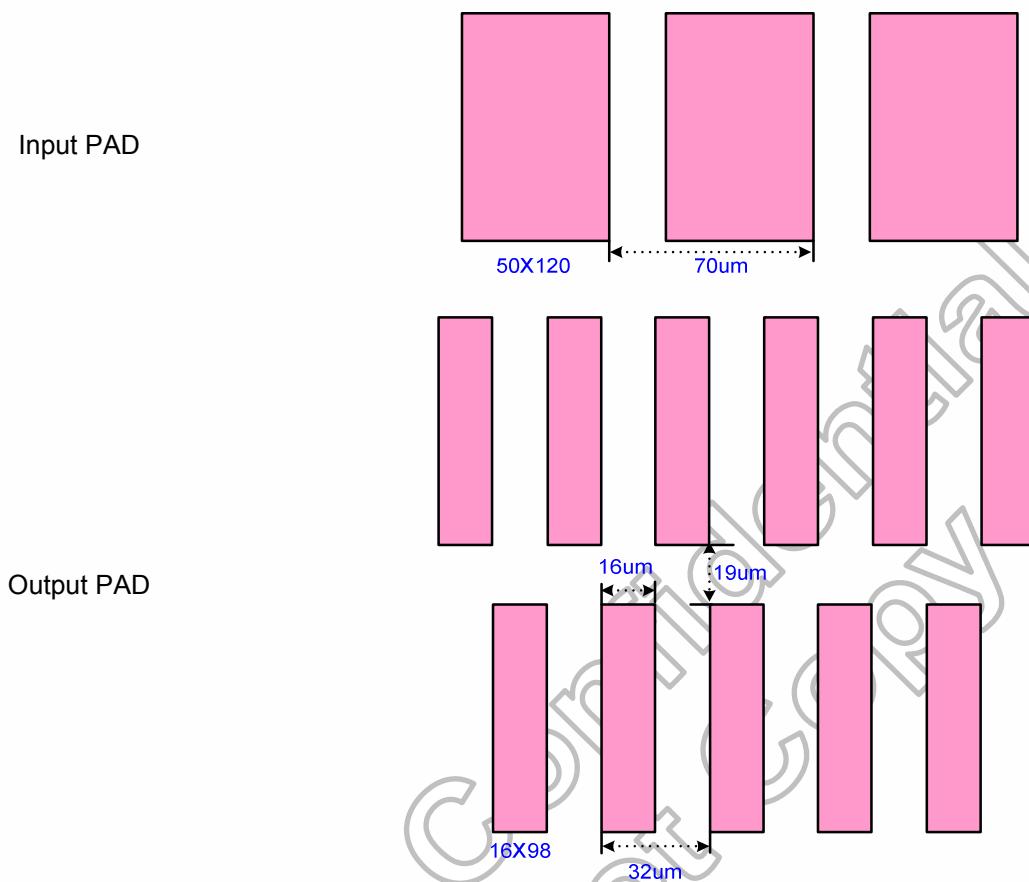
No.	Pad name	X	Y
1201	G141	-7219	202.5
1202	G143	-7235	319.5
1203	G145	-7251	202.5
1204	G147	-7267	319.5
1205	G149	-7283	202.5
1206	G151	-7299	319.5
1207	G153	-7315	202.5
1208	G155	-7331	319.5
1209	G157	-7347	202.5
1210	G159	-7363	319.5
1211	G161	-7379	202.5
1212	G163	-7395	319.5
1213	G165	-7411	202.5
1214	G167	-7427	319.5
1215	G169	-7443	202.5
1216	G171	-7459	319.5
1217	G173	-7475	202.5
1218	G175	-7491	319.5
1219	G177	-7507	202.5
1220	G179	-7523	319.5
1221	G181	-7539	202.5
1222	G183	-7555	319.5
1223	G185	-7571	202.5
1224	G187	-7587	319.5
1225	G189	-7603	202.5
1226	G191	-7619	319.5
1227	G193	-7635	202.5
1228	G195	-7651	319.5
1229	G197	-7667	202.5
1230	G199	-7683	319.5
1231	G201	-7699	202.5
1232	G203	-7715	319.5
1233	G205	-7731	202.5
1234	G207	-7747	319.5
1235	G209	-7763	202.5
1236	G211	-7779	319.5
1237	G213	-7795	202.5
1238	G215	-7811	319.5
1239	G217	-7827	202.5
1240	G219	-7843	319.5
1241	G221	-7859	202.5
1242	G223	-7875	319.5
1243	G225	-7891	202.5
1244	G227	-7907	319.5
1245	G229	-7923	202.5
1246	G231	-7939	319.5
1247	G233	-7955	202.5
1248	G235	-7971	319.5
1249	G237	-7987	202.5
1250	G239	-8003	319.5
1251	G241	-8019	202.5
1252	G243	-8035	319.5
1253	G245	-8051	202.5
1254	G247	-8067	319.5
1255	G249	-8083	202.5
1256	G251	-8099	319.5
1257	G253	-8115	202.5
1258	G255	-8131	319.5
1259	G257	-8147	202.5
1260	G259	-8163	319.5

No.	Pad name	X	Y
1261	G261	-8179	202.5
1262	G263	-8195	319.5
1263	G265	-8211	202.5
1264	G267	-8227	319.5
1265	G269	-8243	202.5
1266	G271	-8259	319.5
1267	G273	-8275	202.5
1268	G275	-8291	319.5
1269	G277	-8307	202.5
1270	G279	-8323	319.5
1271	G281	-8339	202.5
1272	G283	-8355	319.5
1273	G285	-8371	202.5
1274	G287	-8387	319.5
1275	G289	-8403	202.5
1276	G291	-8419	319.5
1277	G293	-8435	202.5
1278	G295	-8451	319.5
1279	G297	-8467	202.5
1280	G299	-8483	319.5
1281	G301	-8499	202.5
1282	G303	-8515	319.5
1283	G305	-8531	202.5
1284	G307	-8547	319.5
1285	G309	-8563	202.5
1286	G311	-8579	319.5
1287	G313	-8595	202.5
1288	G315	-8611	319.5
1289	G317	-8627	202.5
1290	G319	-8643	319.5
1291	DUMMY27	-8659	202.5

Alignment mark	X	Y
A1	-8751	269
A2	8751	269

#### 4.4 Alignment Mark

**A\_MARK (A1)****A\_MARK (A2)**

**4.5 Bump Size**

## 5. Function Description

### 5.1 Interface Control Mode

The HX8347-A01 supports three-type interface mode: Command-Parameter interface mode, Register-Content interface mode, and RGB interface mode

Command-Parameter interface mode or Register-Content interface mode is active by the external pins IFSEL0.

RGB interface mode is active by internal bit RGB\_EN setting as shown in Table5.1. There are two-type chip access formats in HX8347-A01. One is register command for chip internal operation; the other is display data for chip display.

RGB\_EN is stored in OTP for user application.

IFSEL0	RGB_EN	Register Data	Display Data
0	0	Command-parameter interface (Parallel interface)	From SRAM
0	1	Command-parameter interface (Serial interface)	Sleep out Normal Display On : From RGB interface Sleep out Partial Mode On : From SRAM
1	0	Register-content interface (Parallel interface)	From SRAM
1	1	Register-content interface (Serial interface)	Normal display: From RGB interface Partial Mode: From SRAM

**Table 5. 1 Interface Mode Selection**

There are two-type register groups in HX8347-A01. One is accessed only via Command-Parameter interface. The other is accessed only via Register-Content interface.

This manual description focuses on Register-Content interface mode and RGB interface mode, about the Command-Parameter interface mode, please refer to the HX8347-A(N) datasheet for detail.

### 5.1.1 Register-Content Interface Mode

The register-content interface circuit in HX8347-A01 supports 18-/16-/8-bit bus width parallel bus system interface for I80 series and M68 series CPU, and serial bus system interface for serial data input. When NCS = "L", the parallel and serial bus system interface of the HX8347-A01 become active and data transfer through the interface circuit is available. The DNC\_SCL pin specifies whether the system interface circuit access is to the register command or to the GRAM. The input bus width format of system interface circuit is selected by external pins BS (2-0) setting. For selecting the input bus format, please refer to Table5.2 and Table5.3.

In Register-Content interface, it includes an Index Register (IR) to store index data of internal control register and GRAM. Therefore, the IR can be written with the index pointer of the control register through data bus by setting DNC\_SCL=0. Then the command or GRAM data can be written to register at which that index pointer pointed by setting DNC\_SCL=1.

Furthermore, there are two 18-bit bus control registers used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the following read data operations are valid.

P68	Input Signal Format Selection
0	Format for I80 series MPU
1	Format for M68 series MPU

Table 5. 2 MPU Selection in Command-Parameter Interface Circuit

BS2	BS1	BS0	Interface	Transferring Method of GRAM data	Transferring Method of Command
0	0	0	16-bit system interface	16-bit 65K-color	8-bit collective
0	0	1	16-bit system interface	18-bit 262K-color (16+2)	
0	1	0	18-bit system interface	18-bit 262K-color	
0	1	1	8-bit system interface	18-bit 262K-color (6+6+6)	
1	0	0	16-bit system interface	18-bit 262K-color (6+6+6)	
1	0	1	18-bit system interface	18-bit 262K-color	
1	1	ID	Serial interface	RGB_EN=0,Select by register 72h	

Table 5. 3 Interface Selection in Register-Content Interface Mode

### 5.1.2 Parallel Bus System Interface

The input / output data from data pins (D17-0) and signal operation of the I80/M68 series parallel bus interface are listed in Table 5.4 and Table 5.5.

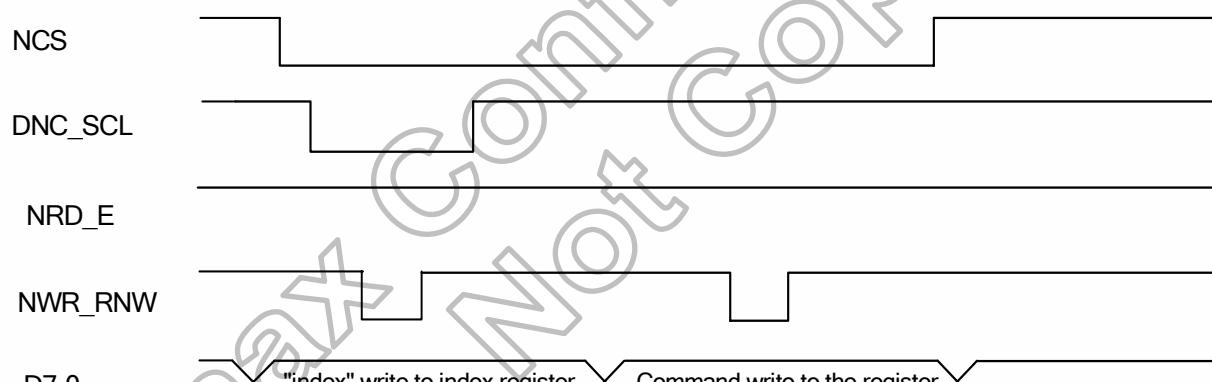
Operations	E_NWR	RW_NRD	DNC_SCL
Writes Indexes into IR	0	1	0
Reads internal status	1	0	0
Writes command into register or data into GRAM	0	1	1
Reads command from register or data from GRAM	1	0	1

Table 5. 4 Data Pin Function for I80 Series CPU

Operations	E_NWR	RW_NRD	DNC_SCL
Writes Indexes into IR	1	0	0
Reads internal status	1	1	0
Writes command into register or data into GRAM	1	0	1
Reads command from register or data from GRAM	1	1	1

Table 5. 5 Data Pin Function for M68 Series CPU

#### Write to the register



#### Read the register

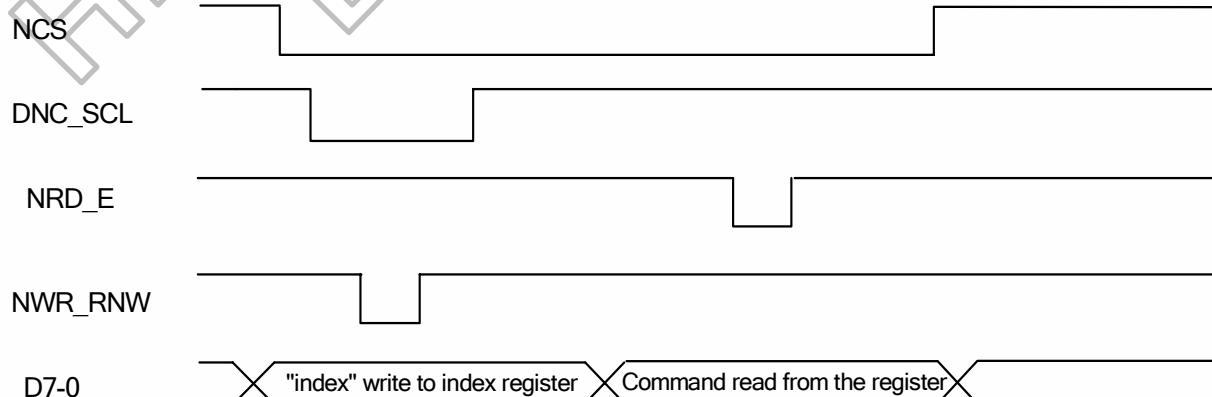
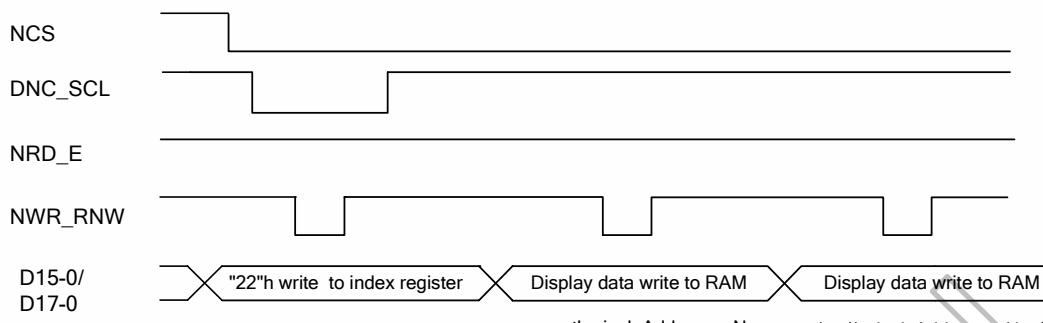
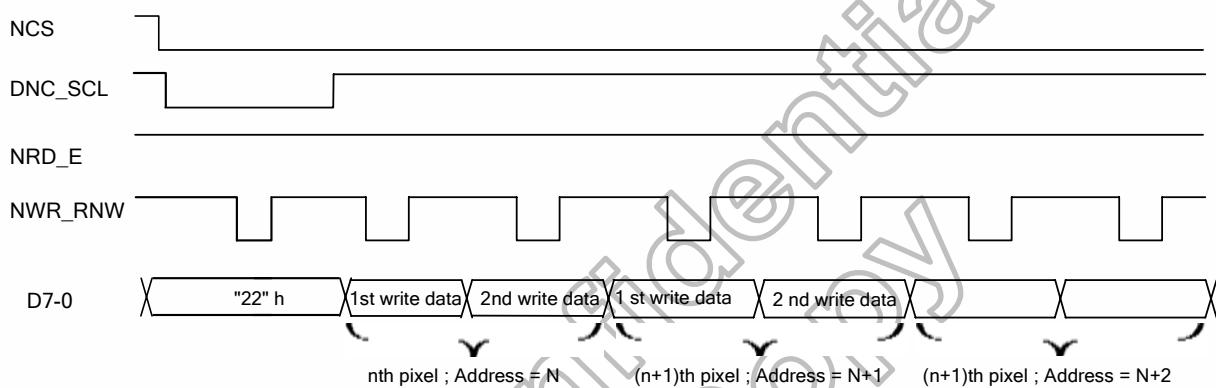


Figure 5. 1 Register Read/Write Timing in Parallel Bus System Interface (for I80 Series MPU)

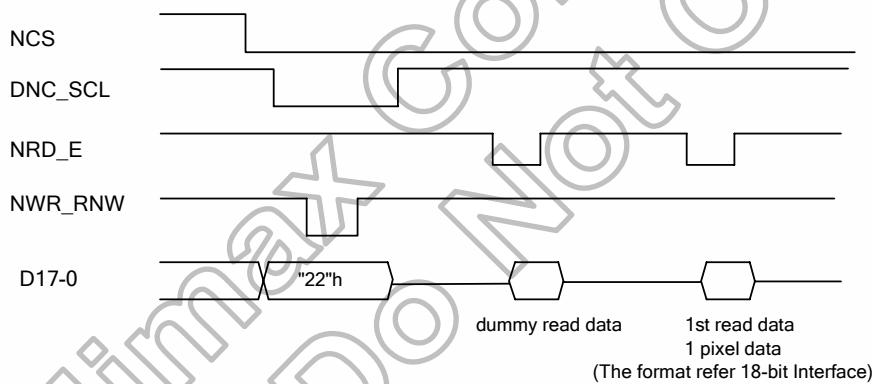
Write to the graphic RAM (16-bit 65K Color / 18-bit bit 262K Color)



Write to the graphic RAM (16-bit 262K Color)



Read the graphic RAM (18-bit 262K Color)



Read the graphic RAM (16-bit 65K/262K Color)

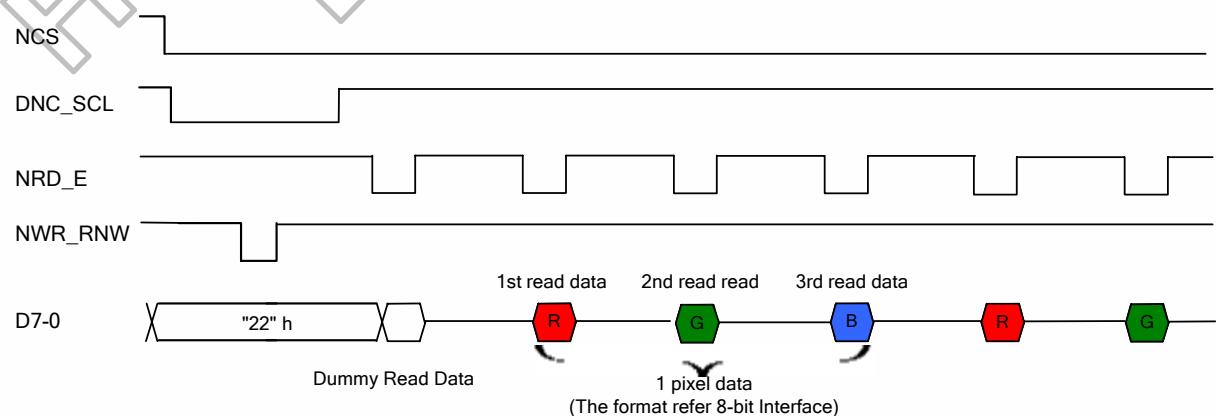
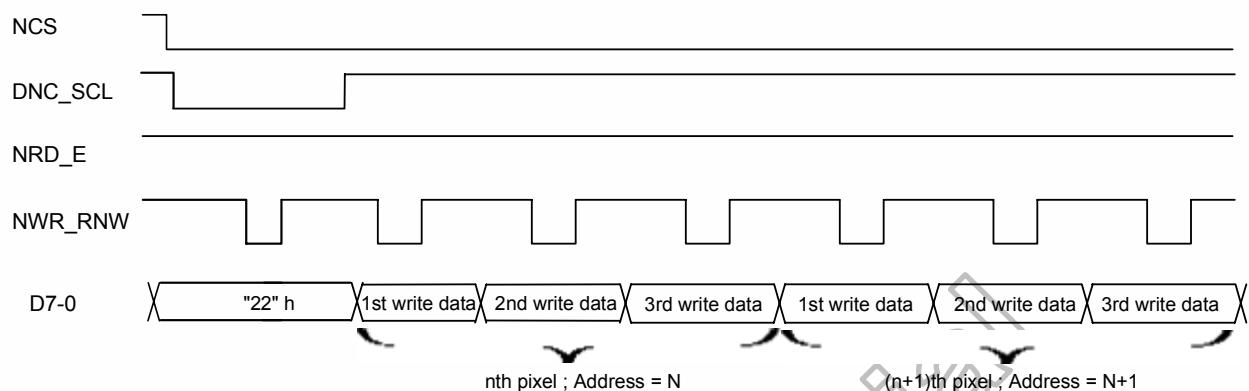
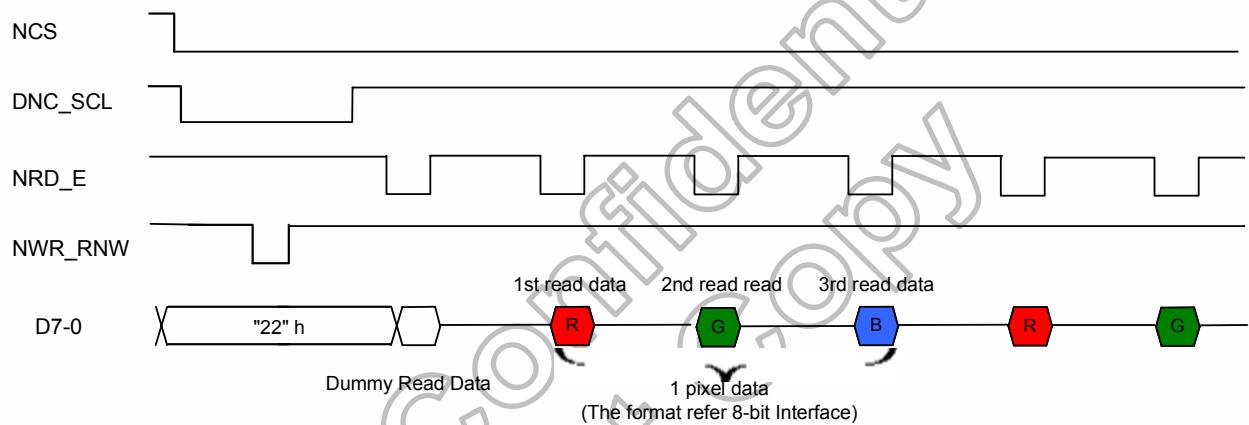


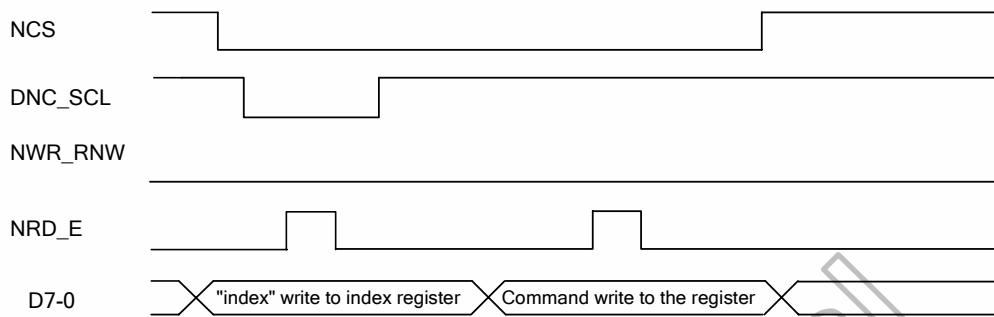
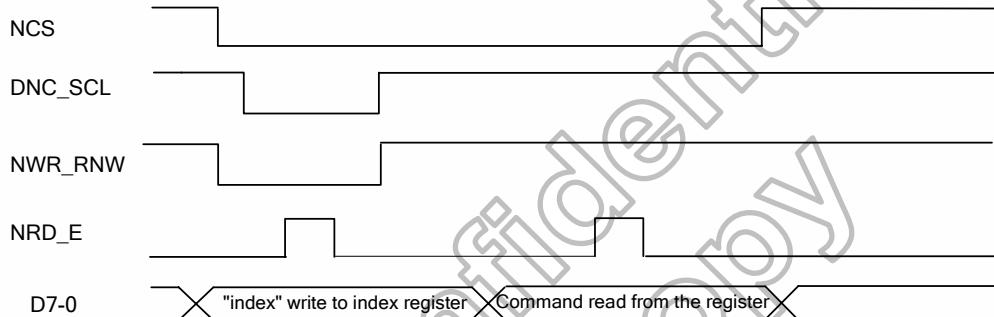
Figure 5. 2 GRAM Read/Write Timing in 16-/18-Bit Parallel Bus System Interface (for I80 Series MPU)

## Write to the graphic RAM (8-bit 262K Color)



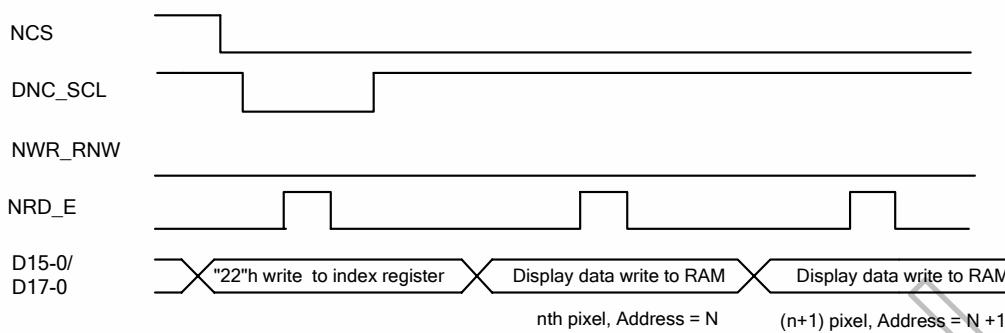
## Read the graphic RAM (8-bit 262K Color)

**Figure 5. 3 GRAM Read/Write Timing in 8-Bit Parallel Bus System Interface (for I80 Series MPU)**

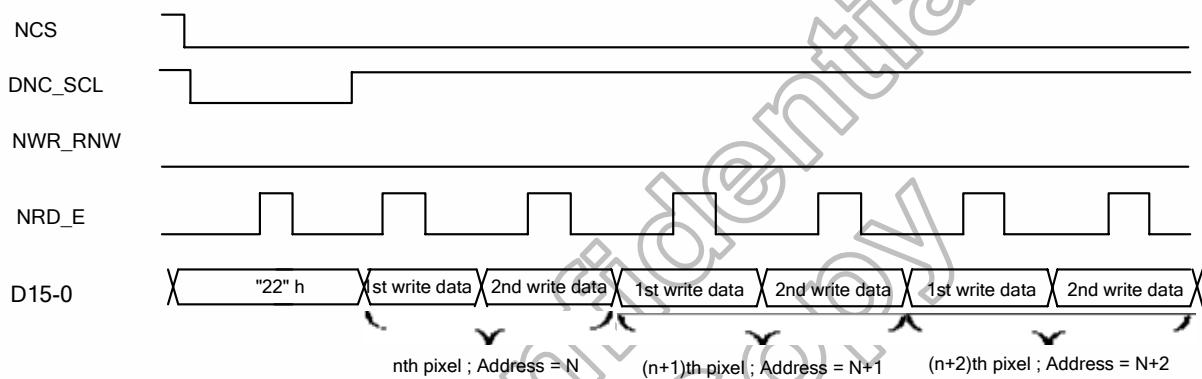
**Write to the register****Read the register**

**Figure 5. 4 Register Read/Write Timing in Parallel Bus System Interface (for M68 Series MPU)**

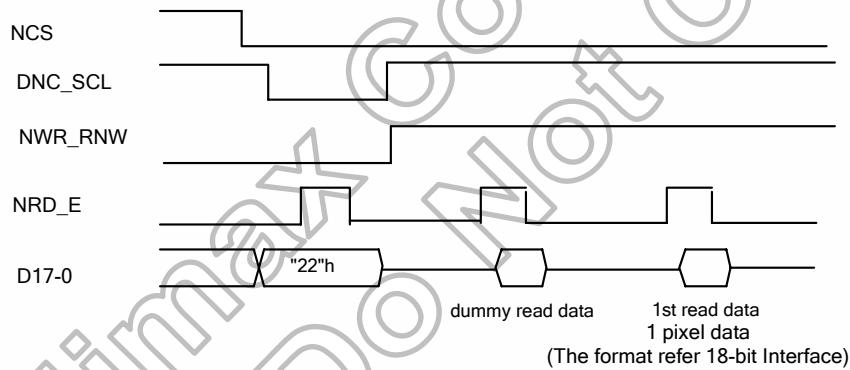
Write to the graphic RAM (16-bit 65K Color / 18-bit bit 262K Color)



Write to the graphic RAM (16+2-bit 262K Color)



Read the graphic RAM (18-bit bit 262K Color)



Read the graphic RAM (16-bit 65K/262K Color)

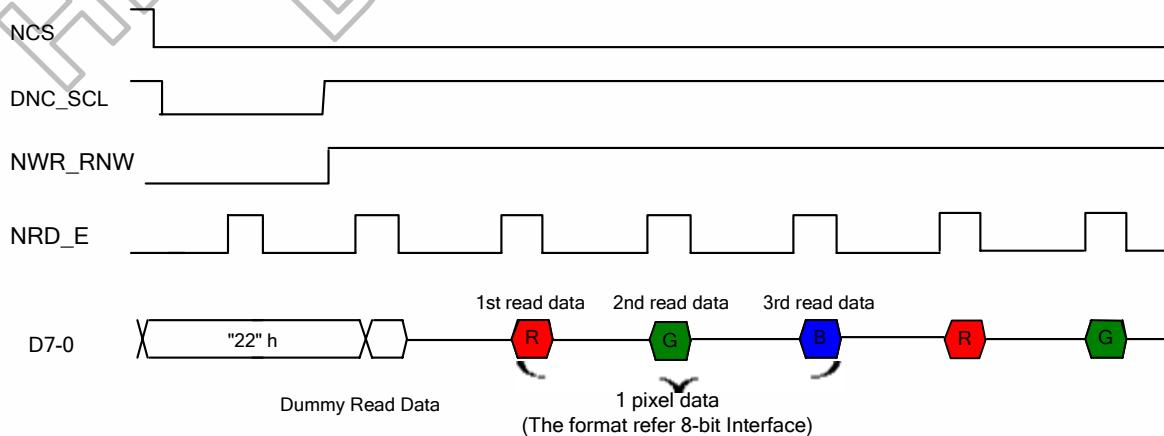
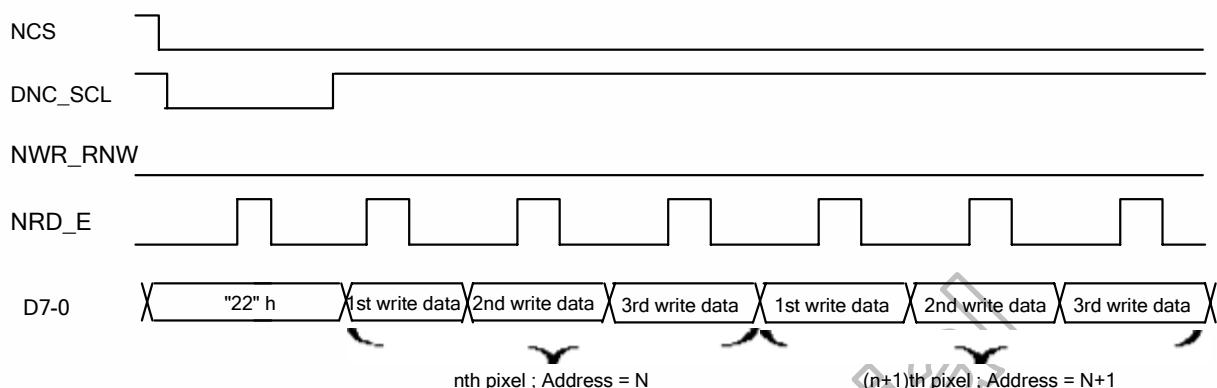
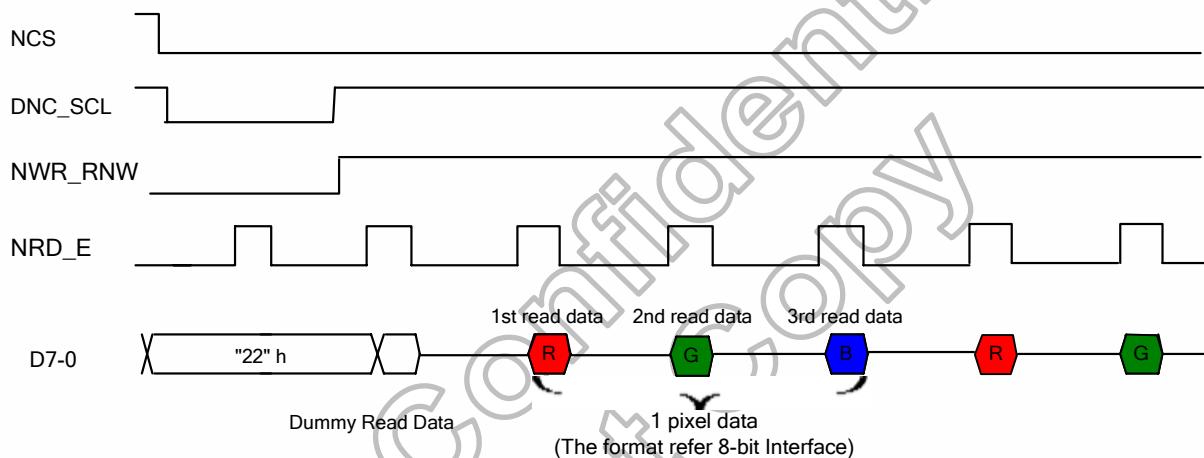


Figure 5. 5 GRAM Read/Write Timing in 16-/18-Bit Parallel Bus System Interface (for M68 Series MPU)

Write to the graphic RAM (8-bit 262K Color)



Read the graphic RAM (8-bit 262K Color)

**Figure 5. 6 GRAM Read/Write Timing in 8-bit Parallel Bus System Interface (for M68 Series MPU)**

**18-bit Parallel Bus System Interface**

The I80-system 18-bit parallel bus interface in command-parameter interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0010” or “0101”. And the M68-system 18-bit parallel bus interface in command-parameter interface mode can be used by setting “P68, BS2, BS1, BS0” pins to “1010” or “1101”. Figure 5.7 is the example of interface with I80/M68 microcomputer system interface.

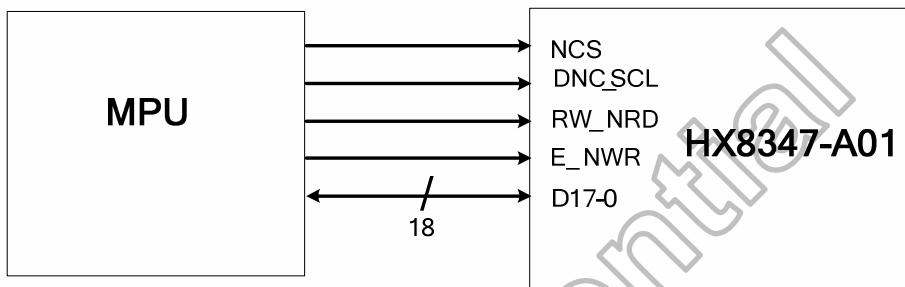


Figure 5.7 Example of I80- / M68- System 18-Bit Parallel Bus Interface

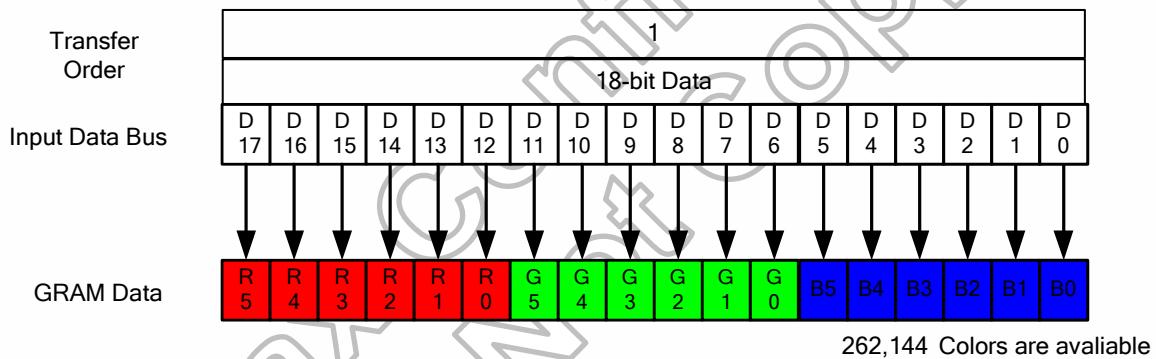
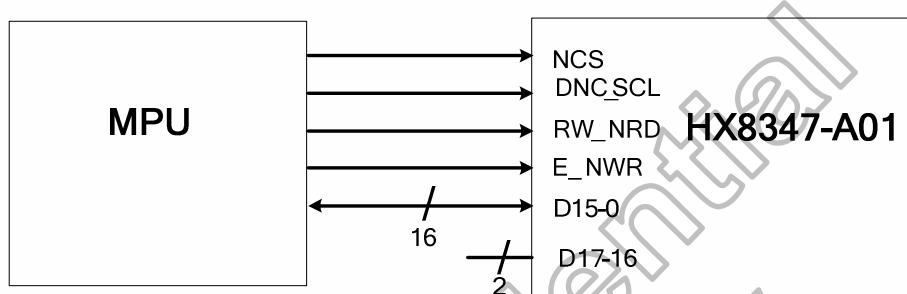


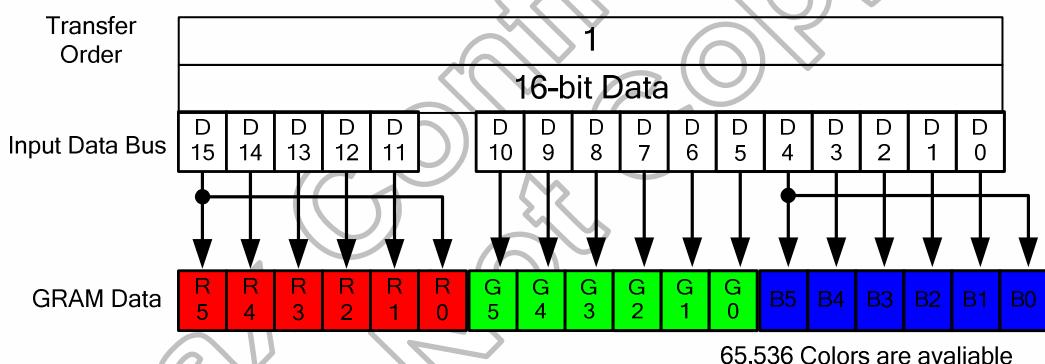
Figure 5.8 Input Data Bus and GRAM Data Mapping in 18-Bit Bus System Interface  
("BS2, BS1, BS0"="010" or "101")

## 16-bit Parallel Bus System Interface

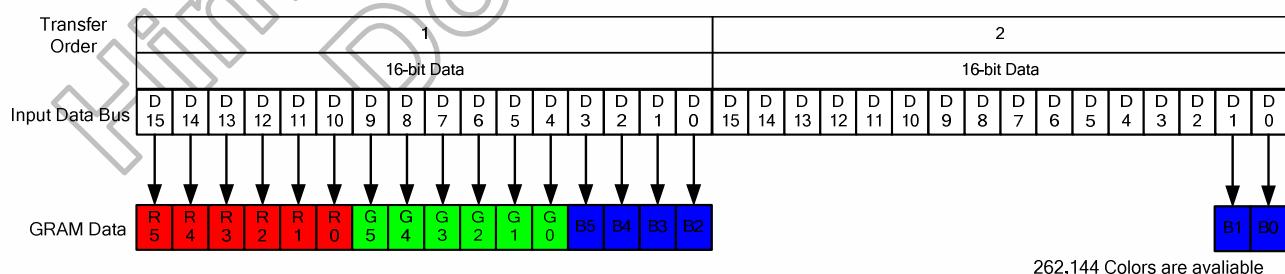
The I80-system 16-bit parallel bus interface in command-parameter interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0000”, “0001”, “0100”. And the M68-system 16-bit parallel bus interface in command-parameter interface mode can be used by setting “P68, BS2, BS1, BS0” pins to “1000”, “1001”, “1100”. Figure 5.9 is the example of interface with I80/M68 microcomputer system interface.



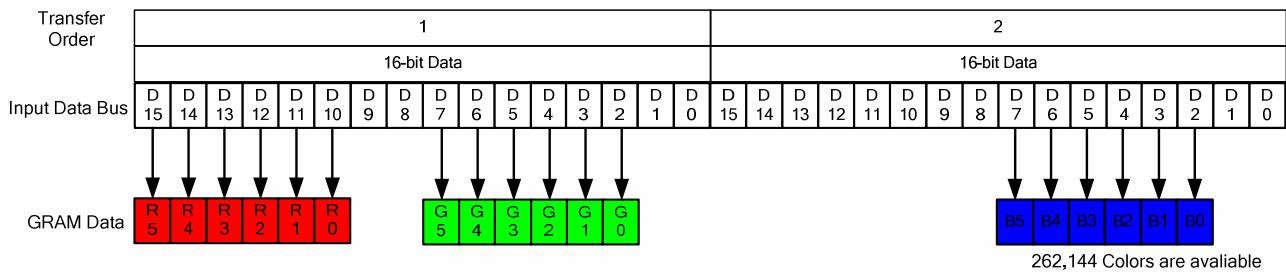
**Figure 5. 9 Example of I80- / M68- System 16-bit Parallel Bus Interface**



**Figure 5. 10 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 16 Bit-Data Input (“BS2, BS1, BS0”=“000”)**



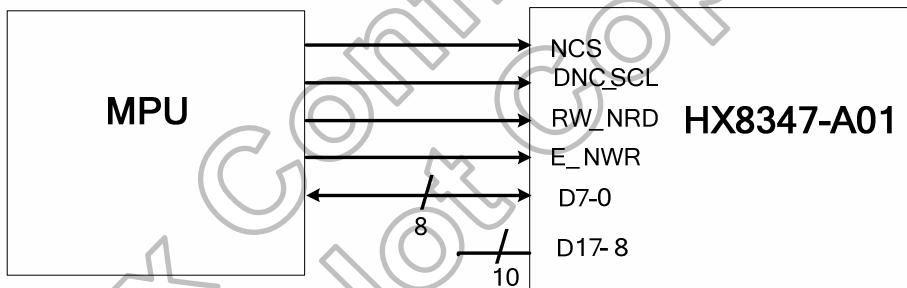
**Figure 5. 11 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 18(16+2) Bit-Data Input (“BS2, BS1, BS0”=“001”)**



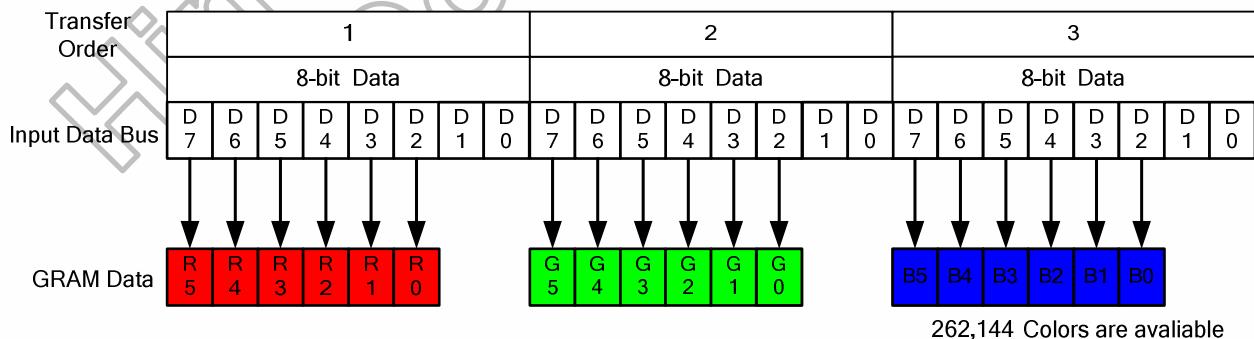
**Figure 5. 12 Input Data Bus and GRAM Data Mapping in 16-Bit Bus System Interface with 18(6+6+6) Bit-Data Input ("BS2, BS1, BS0"="100")**

### 8-bit Parallel Bus System Interface

The I80-system 8-bit parallel bus interface in register-content interface mode can be used by setting external pins "P68, BS2, BS1, BS0" pins to "0011". And the M68-system 8-bit parallel bus interface in command-parameter interface mode can be used by setting "P68, BS2, BS1, BS0" pins to "1011". Figure 5.13 is the example of interface with I80/M68 microcomputer system interface.



**Figure 5. 13 Example of I80- / M68- System 8-Bit Parallel Bus Interface**



**Figure 5. 14 Input Data Bus and GRAM Data Mapping in 8-Bit Bus System Interface with 18( 6 + 6 + 6 ) Bit-Data Input ("BS2, BS1, BS0"="011")**

### 5.1.3 Serial Bus System Interface

The HX8347-A01 supports the serial bus interface in register-content mode by setting external pins “BS2, BS1” pins to “11”. The serial bus system interface mode is enabled through the chip select line (NCS), and it is accessed via a control consisting of the serial input data (SDI), serial output data (SDO) and the serial transfer clock signal (DNC\_SCL).

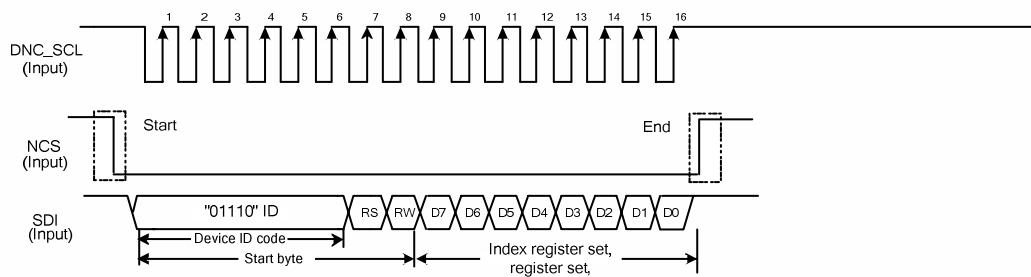
As the chip select signal (NCS) goes low, the start byte needs to be transferred first. The start byte is made up of 6-bit bus device identification code, register select (RS) bit and read/write operation (RW) bit. The five upper bits of 6-bit bus device identification code must be set to “01110”, and the least significant bit of the identification code must be set as the external pin BS0 input as “ID”.

The seventh bit (RS) of the start byte determines internal index register or register, GRAM accessing. RS must be set to “0” when writing data to the index register or reading the status, and it must be set to “1” when writing or reading an command or GRAM data. The read or write operation is selected by the eighth bit (RW) of the start byte. The data is written to the chip when R/W = 0, and read from chip when RW = 1.

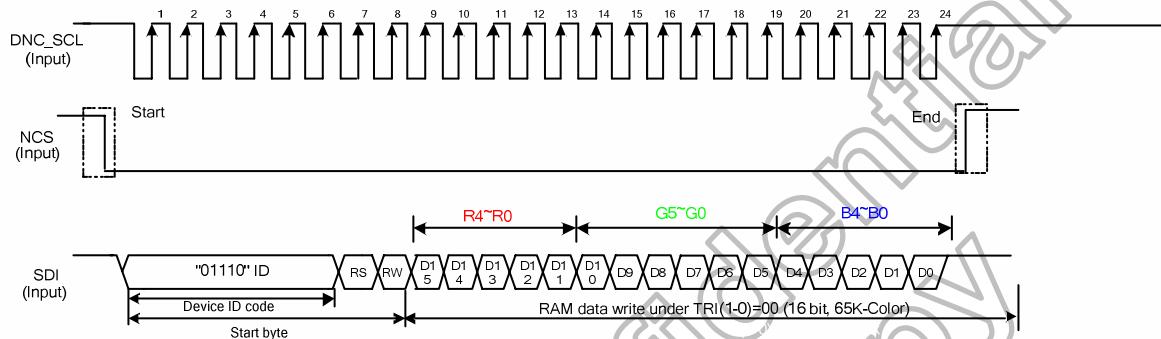
RS	R/W	Function
0	0	Writes Indexes into IR
1	0	Writes command into register or data into GRAM
1	1	Reads command from register or data from GRAM

Table 5. 6 The Function of RS and R/W Bit bus

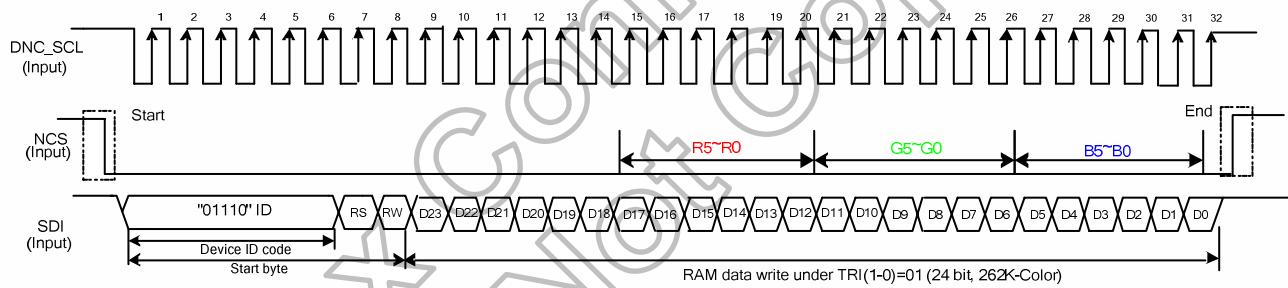
A) TransferTiming Format in Serial Bus Interface for Index Register or Register Write



B) TransferTiming Format in Serial Bus Interface for GRAM write (index = "22h") , TRI(1-0) = 00



C) TransferTiming Format in Serial Bus Interface for GRAM Write (index = "22h") , TRI(1-0) = 01



D) TransferTiming Format in Serial Bus Interface for GRAM Write (index = "22h") , TRI(1-0) = 1x

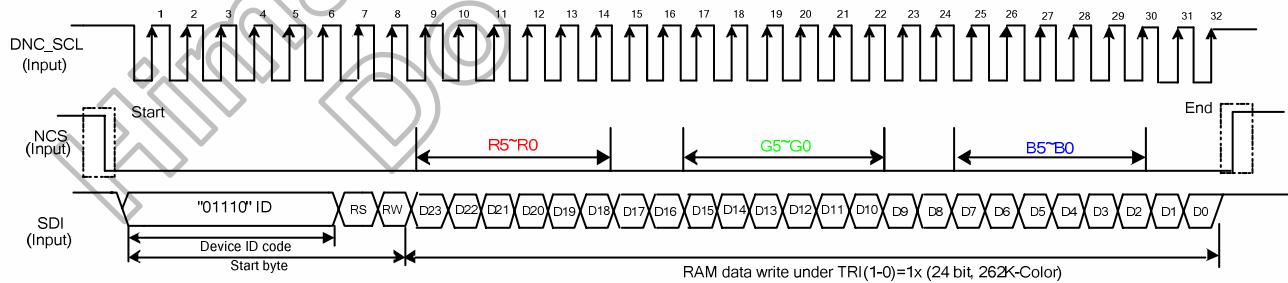
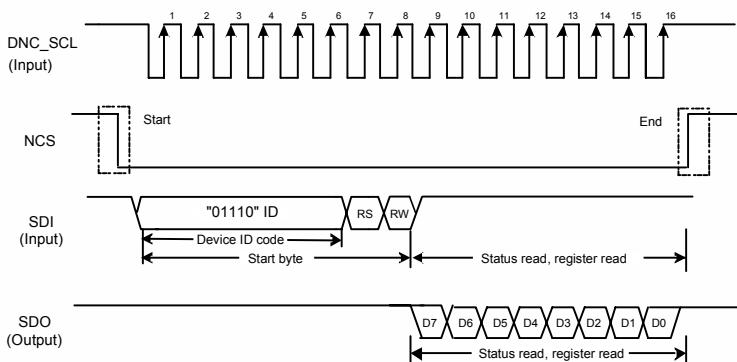
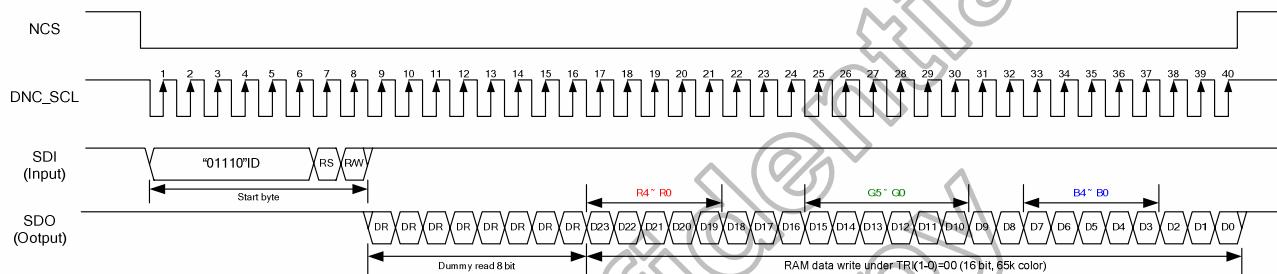
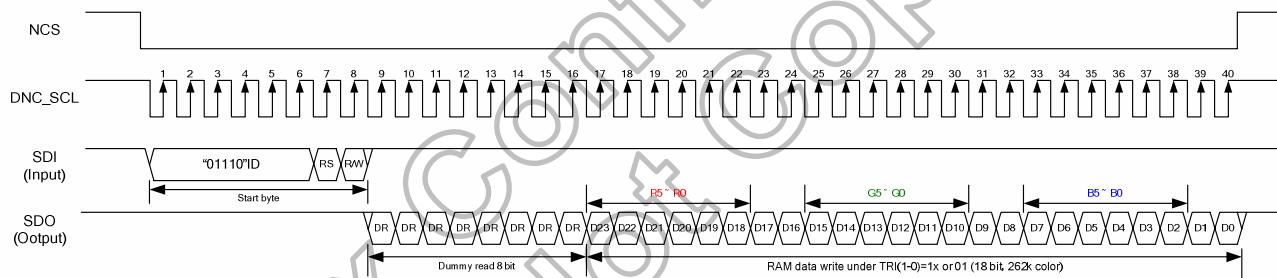
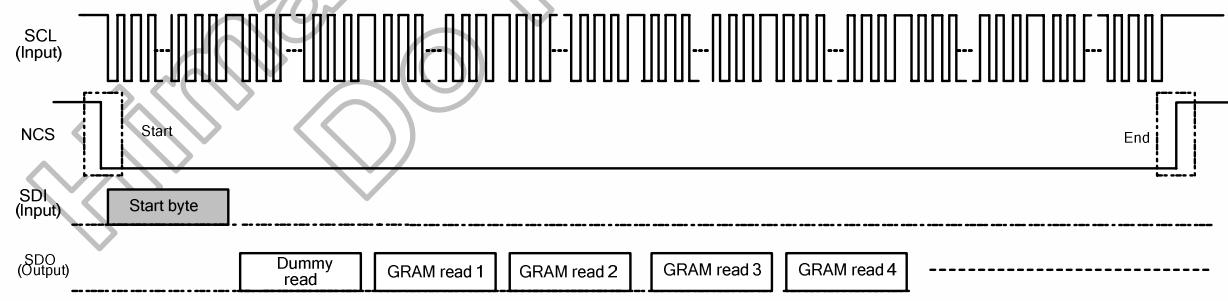


Figure 5. 15 Data Write Timing in Serial Bus System Interface

**A) TransferTiming Format in Serial Bus Interface for Register Read****B) TransferTiming Format in Serial Bus Interface for GRAM Read (index = "22h"), TR[1-0] = 00****C) TransferTiming Format in Serial Bus Interface for GRAM Read (index = "22h"), TR[1-0] = 1x or 01****D) Timing Format of GRAM -Data Read****Figure 5. 16 Data Read Timing in Serial Bus System Interface**

### 5.1.4 RGB Interface

The HX8347-A01 supports the RGB interface for writing animated display data. The RGB interface can be selected by setting internal RGB\_EN bit = 1. In RGB interface, the display operations is executed in synchronization with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC) and dot clock (DOTCLK), and the display data is inputted via RGB interface circuit without being written to the GRAM and display directly. The display data are transferred in pixel unit via D17-0 input pins. The display data input is latched on the rising edge of DOTCLK (DPL bit = 0) or the falling edge of DOTCLK (DPL bit = 1) by the chip when ENABLE signal is valid. Please refer to Table 5.7.

EPL	ENABLE	Display Data to Panel
0	0	Disable
0	1	Enable
1	0	Enable
1	1	Disable

Table 5. 7 EPL Bit Setting and Valid Enable Signal

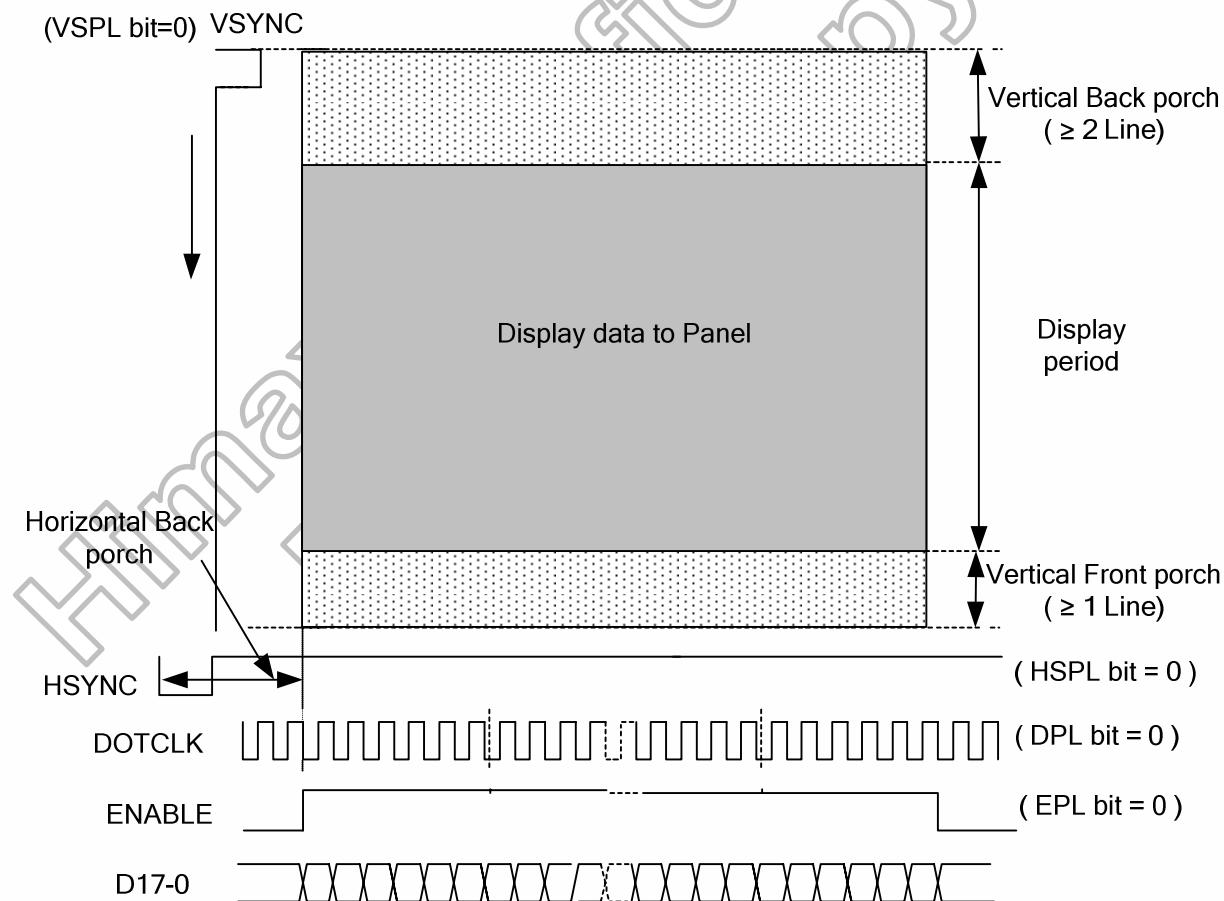
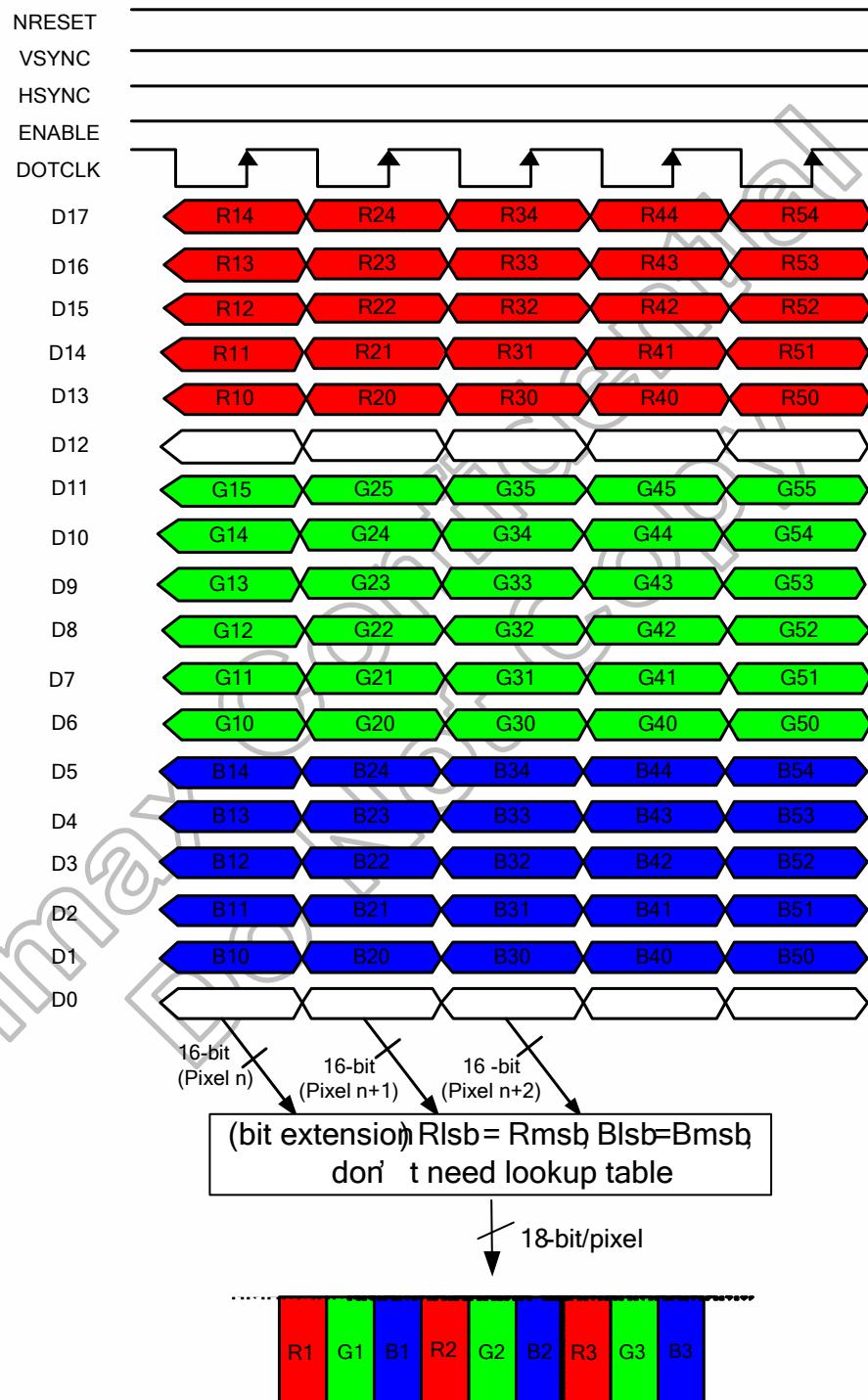


Figure 5. 17 RGB Interface Circuit Input Timing

There are two types bit format per pixel color order for writing GRAM data in 18-bit bus interface selected by internal bits CSEL(2-0). The setting is shown in Figure5. 18 and Figure 5. 19.

**(1) 16 bit/pixel color order (R 5-bit, G 6-bit, B 5-bit), 65,536 colors (CSEL(2-0) = "101")**



**Figure 5. 18 16-Bit / Pixel Data Input of RGB Interface**

## (2) 18 bit/pixel color order (R 6-bit, G 6-bit, B 6-bit), 262,144 colors (CSEL(2-0) = "110")

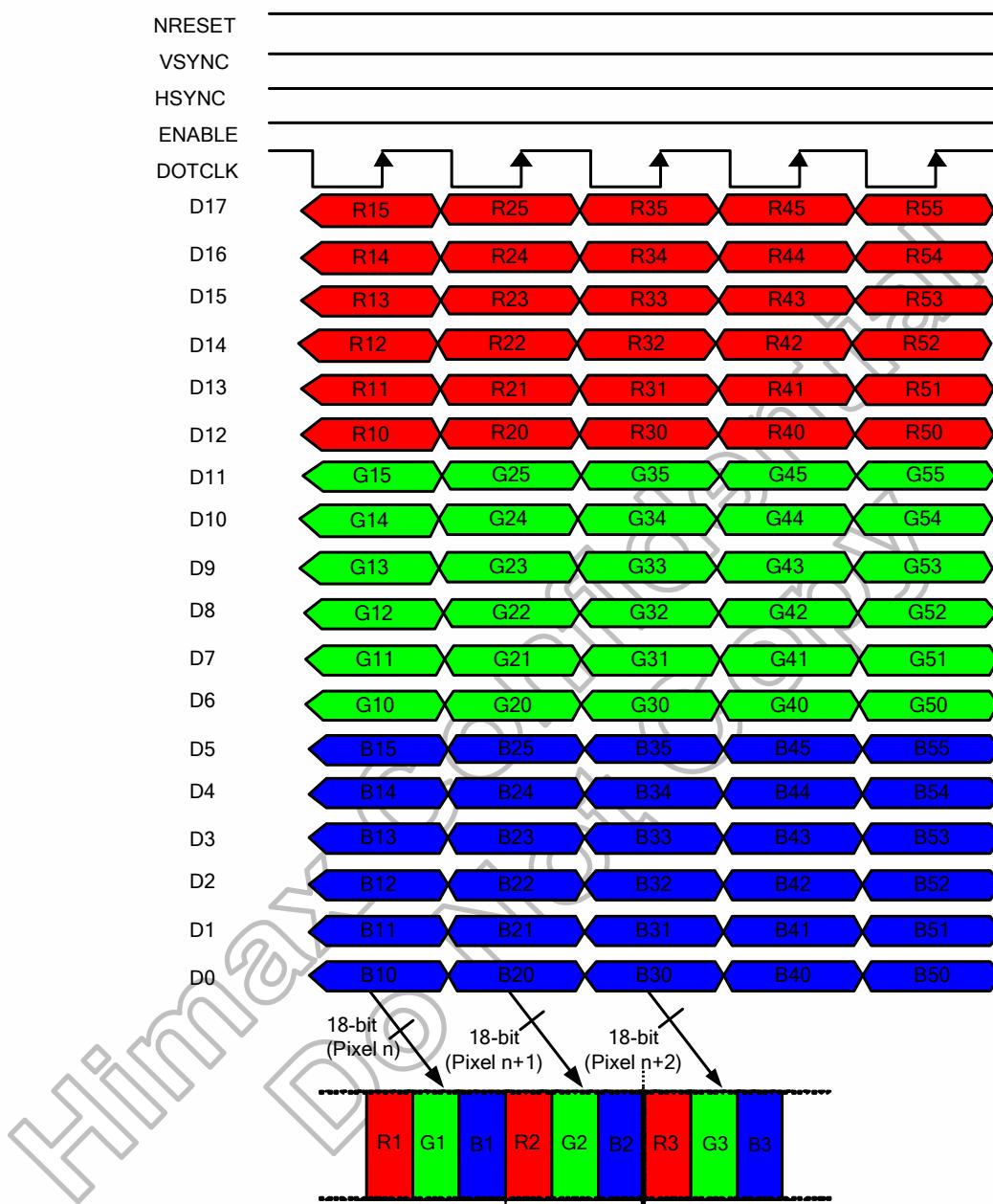


Figure 5. 19 18-Bit / Pixel Data Input of RGB Interface

## 5.2 Address Counter (AC)

The HX8347-A01 contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM whose addresses range X=0~239d and Y=0~319d.

Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (MV, MX and MY bit) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data is written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the horizontal address register (start: SC, end: EC) or the vertical address register (start: SP, end: EP). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

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### 5.2.1 MCU to Memory Write/Read Direction

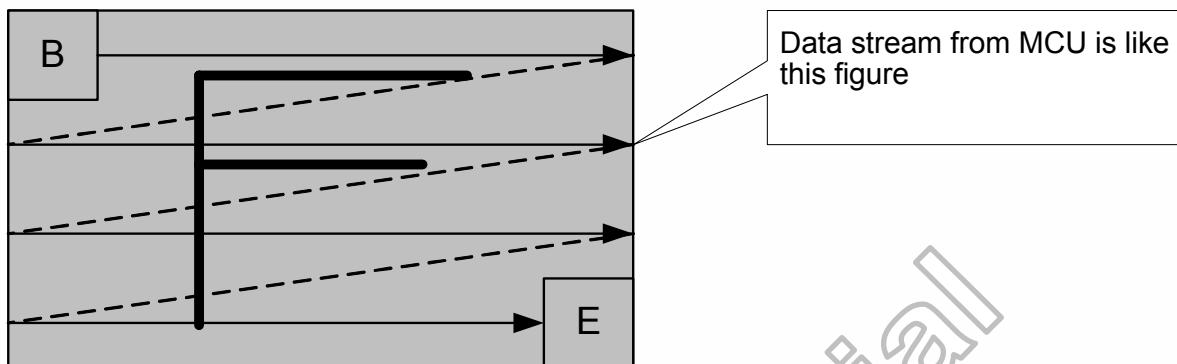


Figure 5. 20 MCU to Memory Write/Read Direction

The data is written in the order as illustrated above. The counter that dictates which physical memory the data is to be written is controlled by “Memory Access Control” Command, Bits MY, MX, MV as described below.

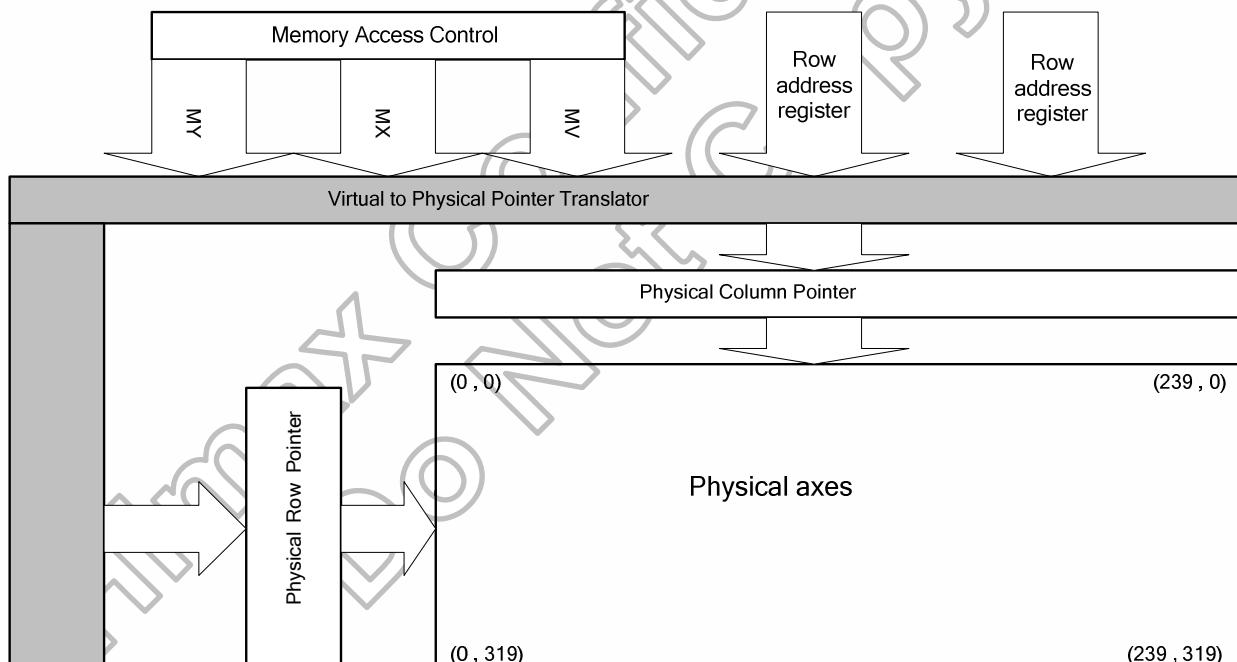


Figure 5. 21 MY, MX, MV Setting

MY	MX	MV	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

Table 5. 8 MY, MX, MV Setting

The following figure depicts the update method set by MV, MX and MY bit.

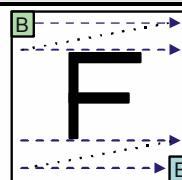
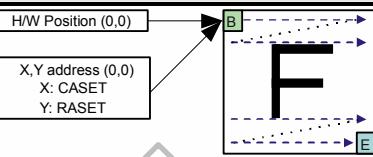
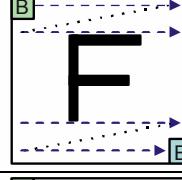
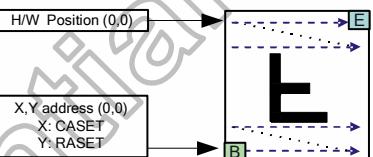
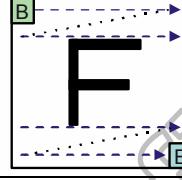
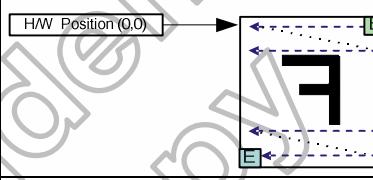
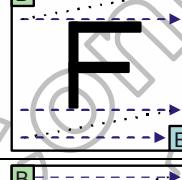
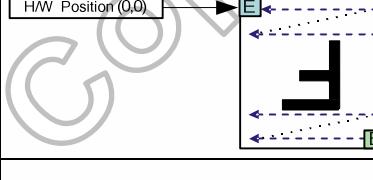
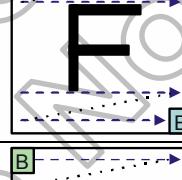
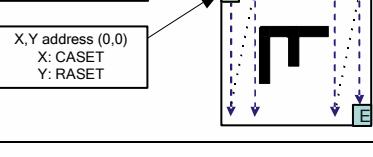
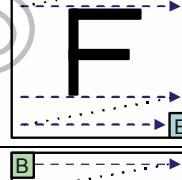
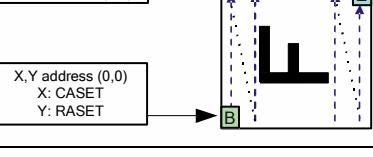
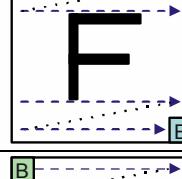
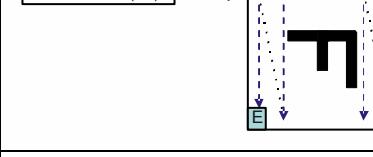
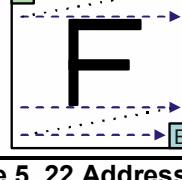
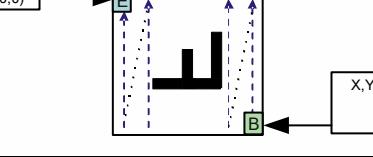
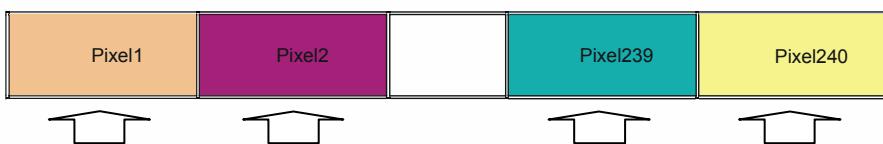
Display Data Direction	MADCTR parameter			Image in the Host	Image in the Driver (GRAM)
	MV	MX	MY		
Normal	0	0	0		 H/W Position (0,0) → B X,Y address (0,0) X: CASET Y: RASET
Y-Mirror	0	0	1		 H/W Position (0,0) → E X,Y address (0,0) X: CASET Y: RASET
X-Mirror	0	1	0		 H/W Position (0,0) → L X,Y address (0,0) X: CASET Y: RASET
X-Mirror Y-Mirror	0	1	1		 H/W Position (0,0) → E X,Y address (0,0) X: CASET Y: RASET
X-Y Exchange	1	0	0		 H/W Position (0,0) → B X,Y address (0,0) X: CASET Y: RASET
X-Y Exchange Y-Mirror	1	0	1		 H/W Position (0,0) → B X,Y address (0,0) X: CASET Y: RASET
X-Y Exchange X-Mirror	1	1	0		 H/W Position (0,0) → E X,Y address (0,0) X: CASET Y: RASET
X-Y Exchange X-Mirror Y-Mirror	1	1	1		 H/W Position (0,0) → E X,Y address (0,0) X: CASET Y: RASET

Figure 5. 22 Address Direction Settings

### 5.3 Source, Gate and Memory Map



Source Out	S1	S2	S3	S4	S5	S6	-----	S715	S716	S717	S718	S719	S720		
RA							RGB Order								
MY=0	0	319	RO <sub>5..0</sub>	G0 <sub>5..0</sub>	B0 <sub>5..0</sub>	R1 <sub>5..0</sub>	G1 <sub>5..0</sub>	B1 <sub>5..0</sub>	-	R238 <sub>5..0</sub>	G238 <sub>5..0</sub>	B238 <sub>5..0</sub>	R239 <sub>5..0</sub>	G239 <sub>5..0</sub>	B239 <sub>5..0</sub>
1	318														
2	317														
3	316														
4	315														
5	314														
6	313														
7	312														
8	311														
9	310														
10	309														
11	308														
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
312	7														
313	6														
314	5														
315	4														
316	3														
317	2														
318	1														
319	0												RN <sub>7..0</sub>	GN <sub>7..0</sub>	BN <sub>7..0</sub>
CA	MX=0	0			1					238			239		
	MX=1	239			238					1			0		

Figure 5. 23 Memory Map (240RGBx320)

Note: RA = Row Address,

CA = Column Address,

MX = Mirror X-axis (Column address direction parameter), D6 parameter of Memory Access Control command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of Memory Access Control command

BGR= Red, Green and Blue pixel position change, D3 parameter of Memory Access Control command

## 5.4 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

### 5.4.1 Tearing Effect Line Modes

**Mode 1**, the Tearing Effect Output signal consists of V-Blanking Information only:

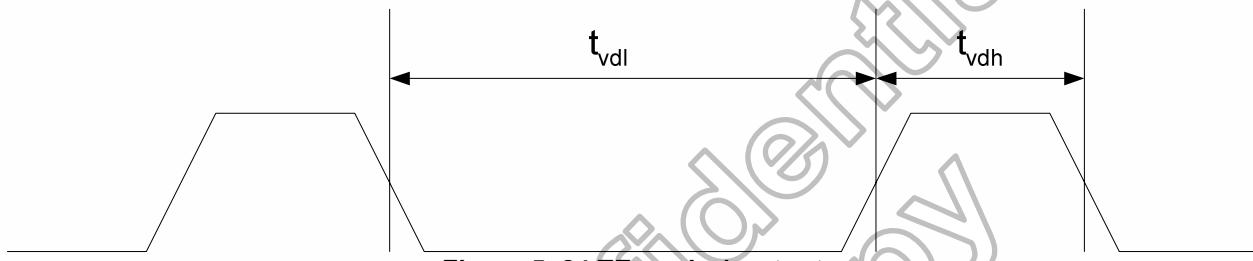


Figure 5. 24 TE mode 1 output

$t_{vdh}$  = The LCD display is not updated from the Frame Memory

$t_{vdl}$  = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

**Mode 2**, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 320 H-sync pulses per field.

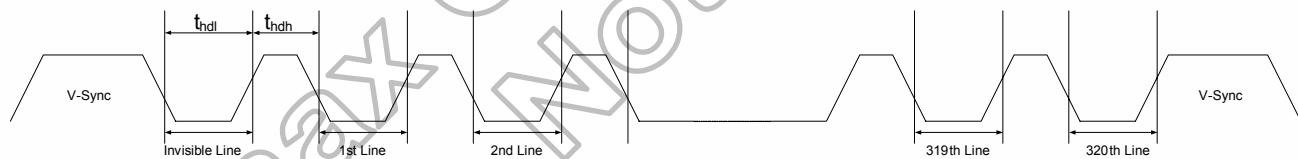


Figure 5. 25 TE mode 2 output

$t_{hdh}$  = The LCD display is not updated from the Frame Memory

$t_{hdl}$  = The LCD display is updated from the Frame Memory (except Invisible Line – see above)

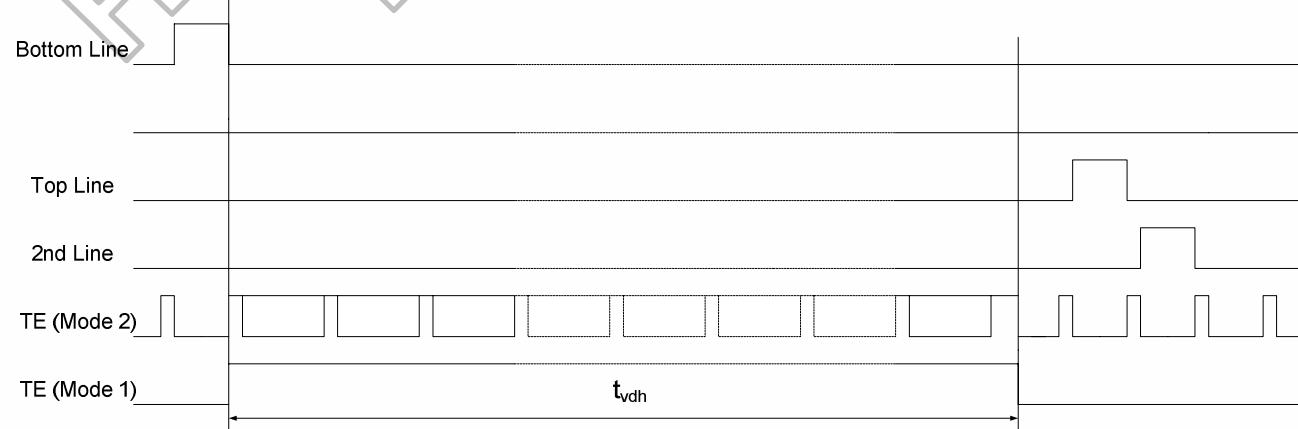
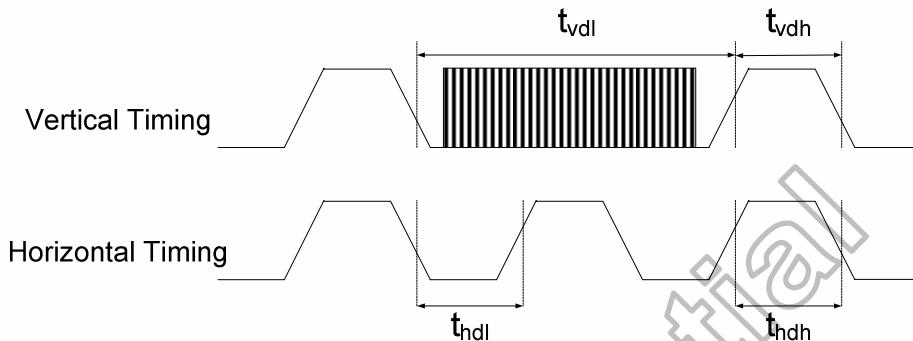


Figure 5. 26 TE output waveform

**Note:** During Sleep In Mode, the Tearing Output Pin is active Low

### 5.4.2 Tearing Effect Line Timing

The Tearing Effect signal is described below.



**Figure 5. 27 Waveform of Tearing Effect Signal**

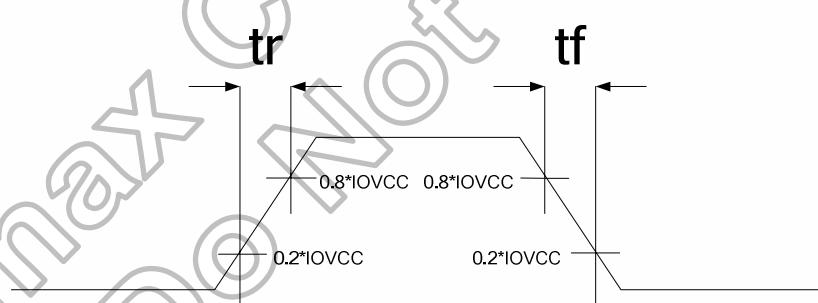
Idle Mode Off (Frame Rate = TBD Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	BP+FP <sup>(1)</sup>	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

Note: (1) BP = Back porch, FP = Font porch.

**Table 5. 9 AC characteristics of Tearing Effect Signal**

The signal's rise and fall times ( $tf$ ,  $tr$ ) are stipulated to be equal to or less than 15ns.



**Figure 5. 28 Timing of Tearing Effect Signal**

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

### 5.4.3 Example 1: MPU Write is faster than Panel Read

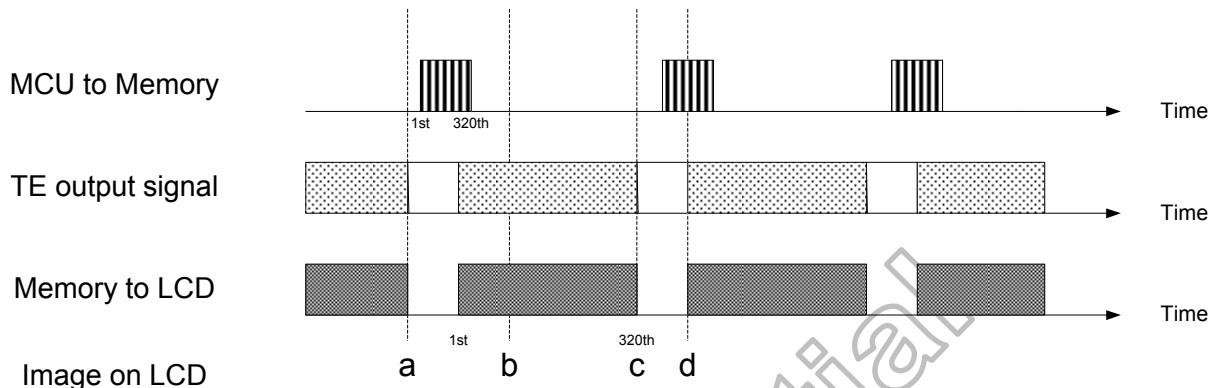


Figure 5. 29

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

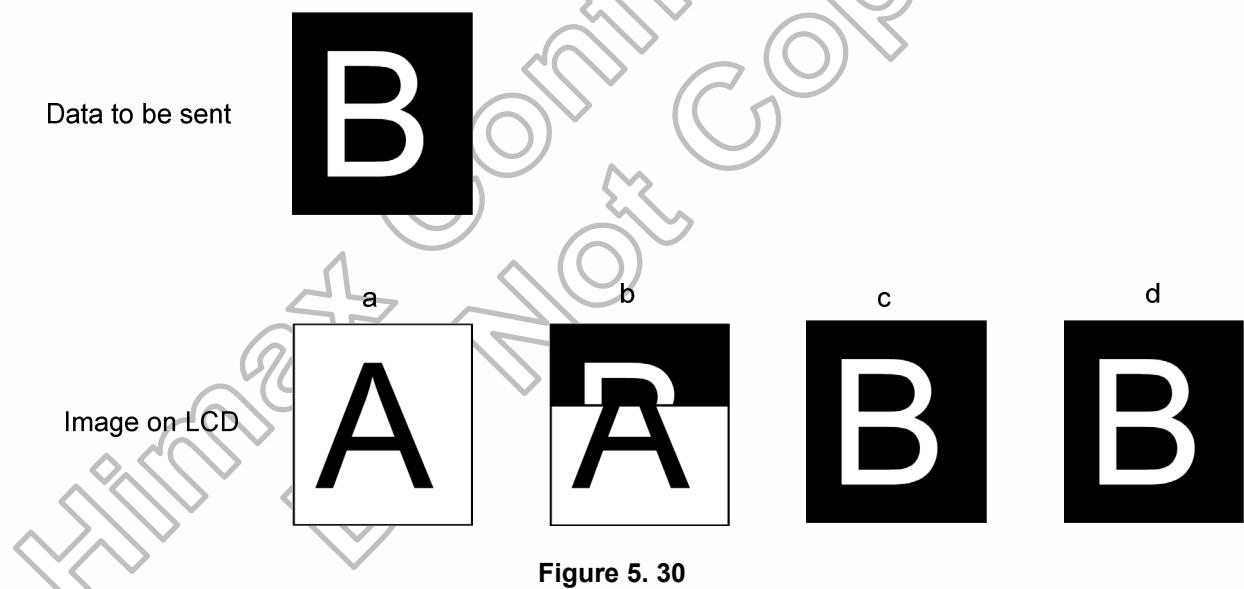


Figure 5. 30

#### 5.4.4 Example 2: MPU Write is slower than Panel Read

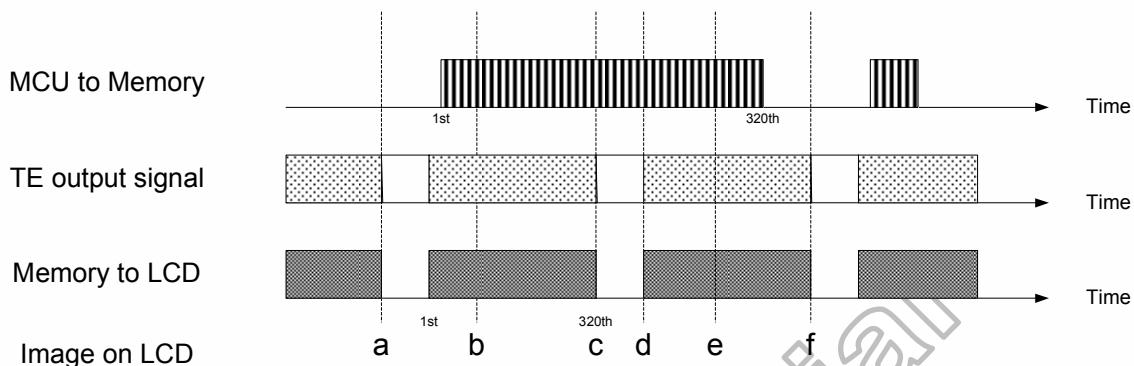


Figure 5. 31

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

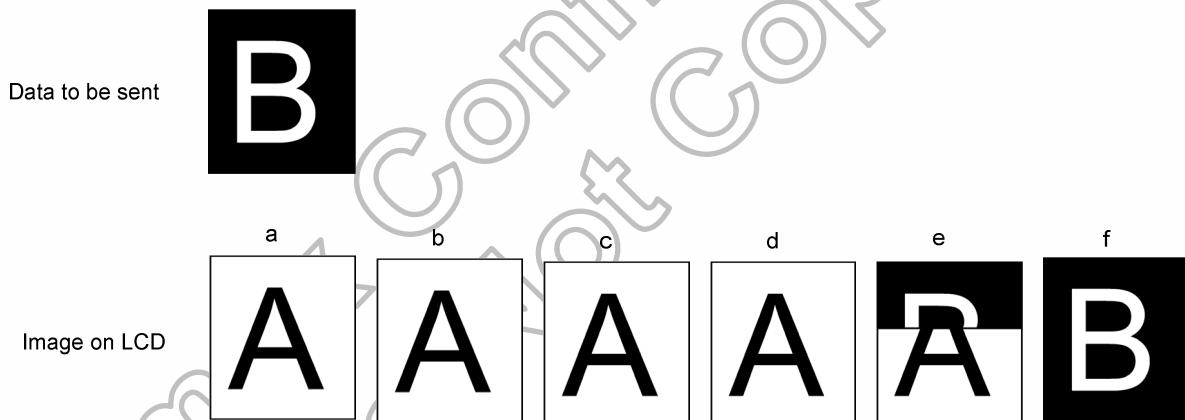


Figure 5. 32

## 5.5 Oscillator

The HX8347-A01 has an internal oscillator without extra external components that provide a source for system clock generator. The default frequency is 5.5MHz.

## 5.6 Source Driver

The HX8347-A01 contains a 720 channels of source driver (S1~S720) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 720 channels and generates corresponding gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

## 5.7 Gate Driver

The HX8347-A01 contains a 320 gate channels of gate driver (G1~G320) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

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## 5.8 LCD Power Generation Circuit

### 5.8.1 LCD Power Generation Scheme

The boost voltage generated is shown as below.

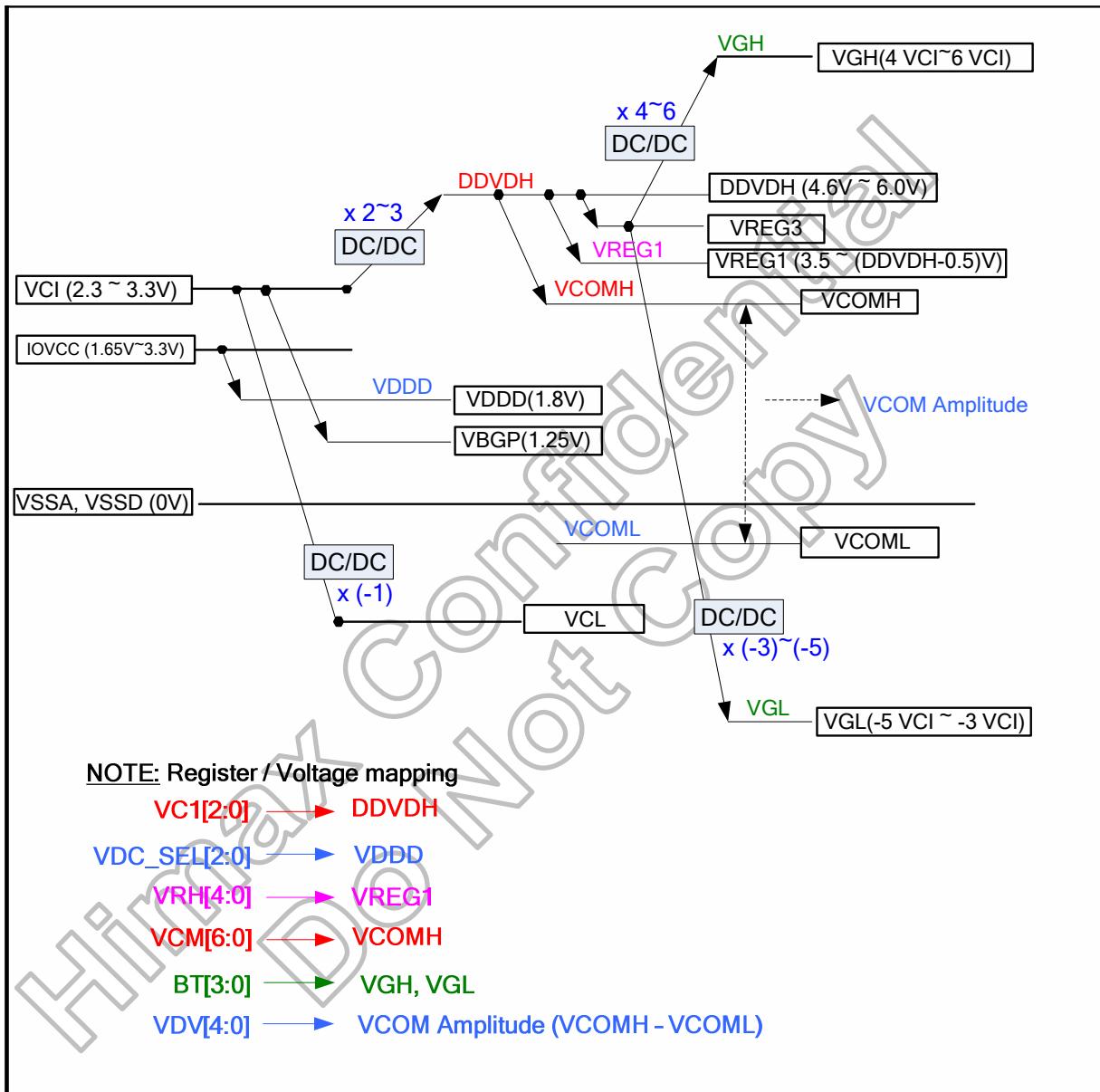
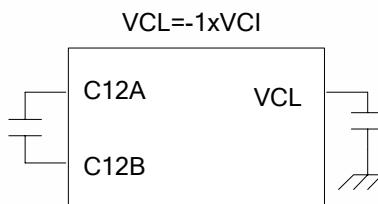
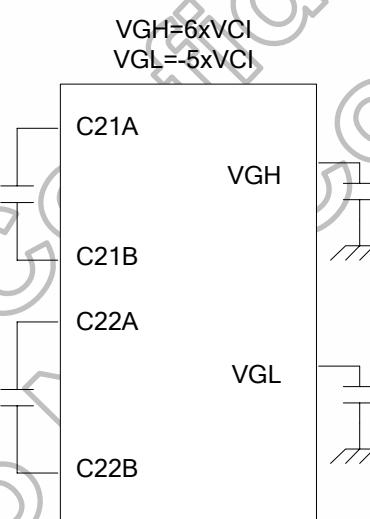
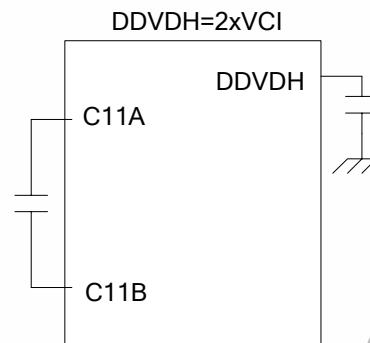


Figure 5. 33 LCD Power Generation Scheme

### 5.8.2 Various Boosting Steps

The boost steps of each boosting voltage are selected according to how the external capacitors are connected. Different booster applications are shown as below.



**Figure 5. 34 Various Boosting Steps**

## 5.9 Gray Voltage Generator for Source Driver

The HX8347-A01 incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available for both polarities.

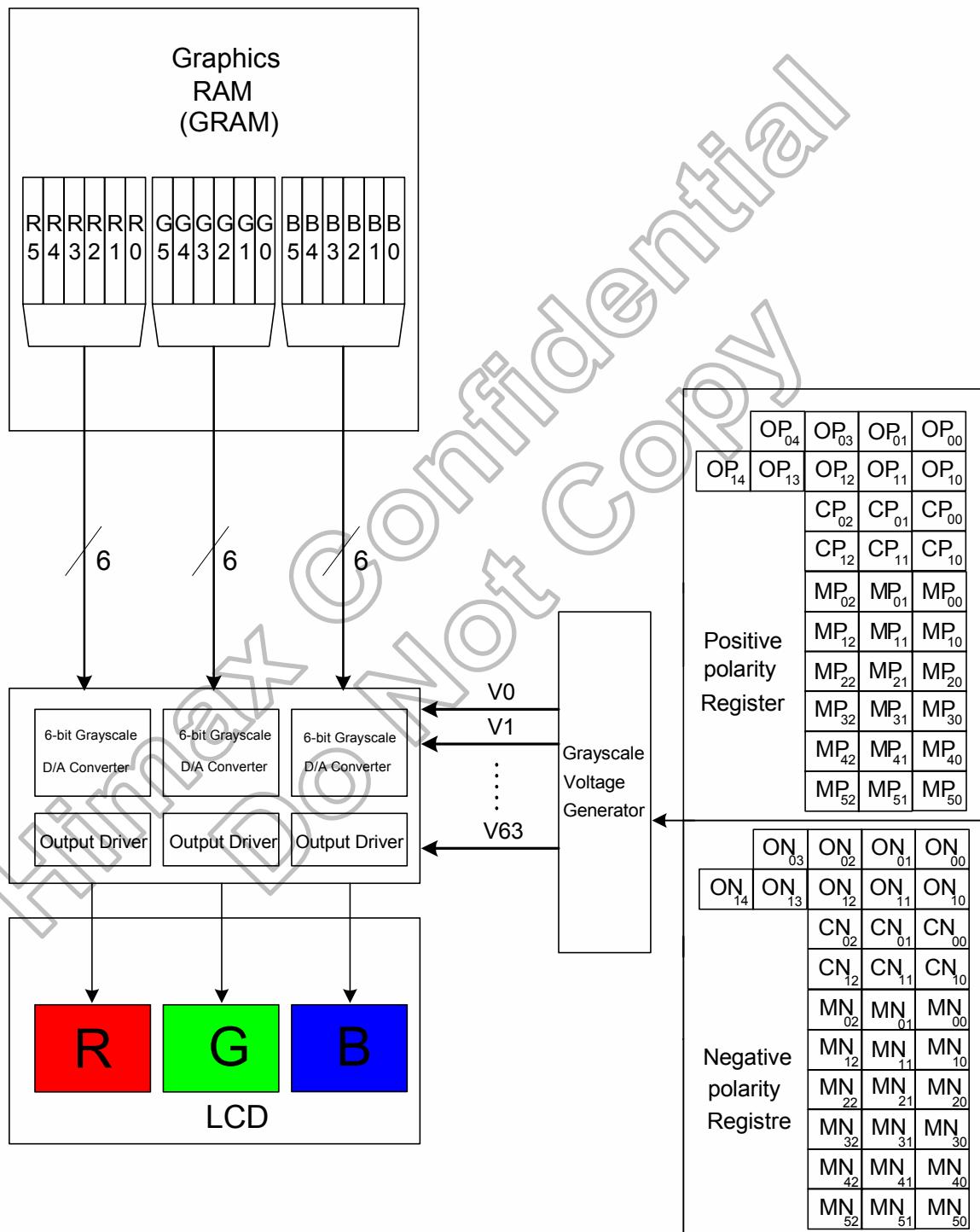
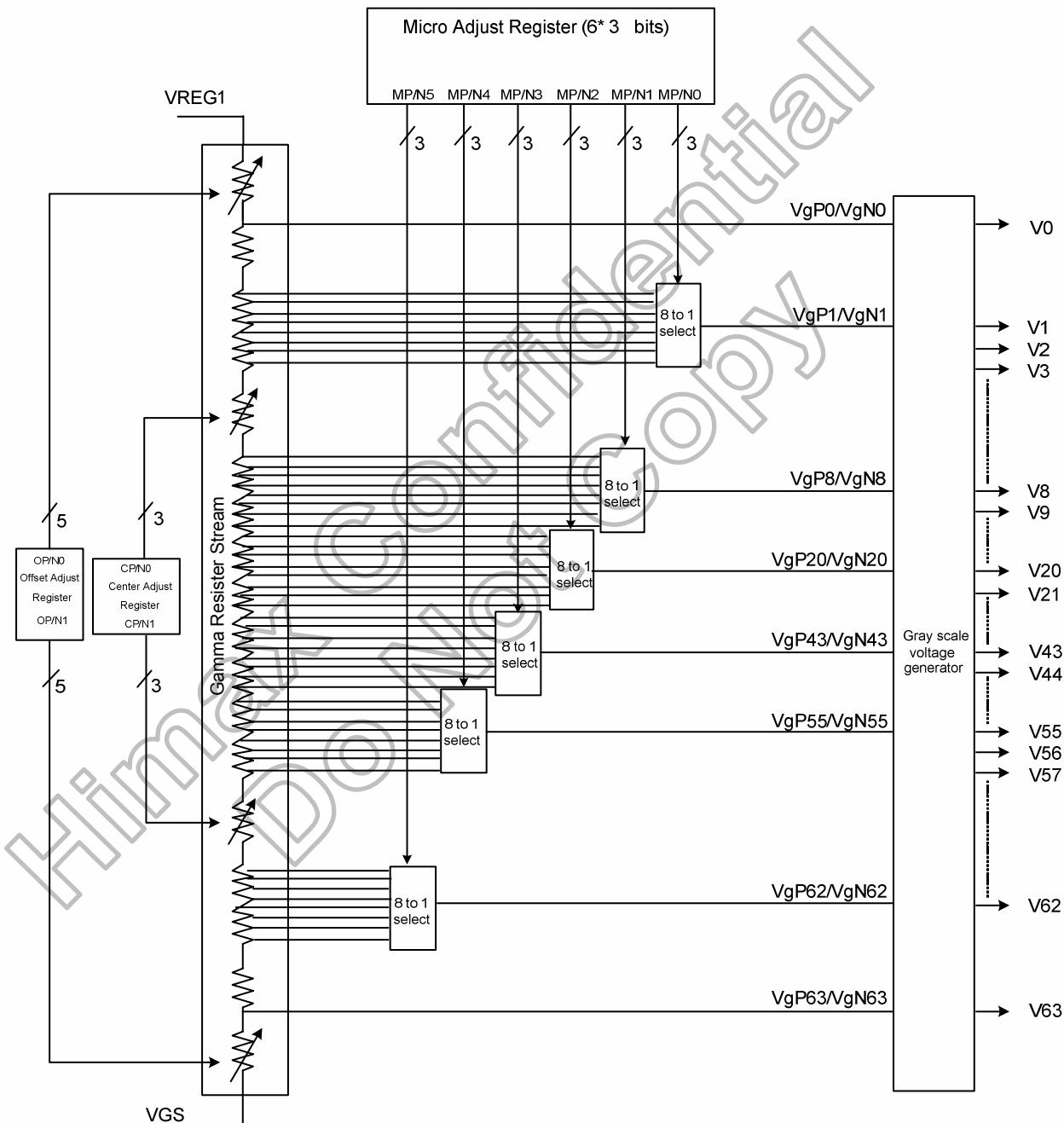


Figure 5. 35 Grayscale Control

### 5.9.1 Structure of Grayscale Voltage Generator

Eight reference gamma voltages  $V_{gP/N}(0, 1, 8, 20, 43, 55, 62, 63)$  for positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltage injected into specified node of grayscale voltage generator, totally 64 grayscale voltages ( $V_0-V_{63}$ ) can be generated from grayscale amplifier for LCD panel.



**Figure 5. 36 Structure of Grayscale Voltage Generator**

## 5.9.2 Gamma-Characteristics Adjustment Register

This HX8347-A01 has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common.)

### 5.9.2.1 Offset Adjustment Registers 0/1

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resistors in the top and bottom of the gamma resistor stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

### 5.9.2.2 Gamma Center Adjustment Registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 8 to 1 selector in the gamma resistor stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

### 5.9.3 Gamma Macro Adjustment Registers

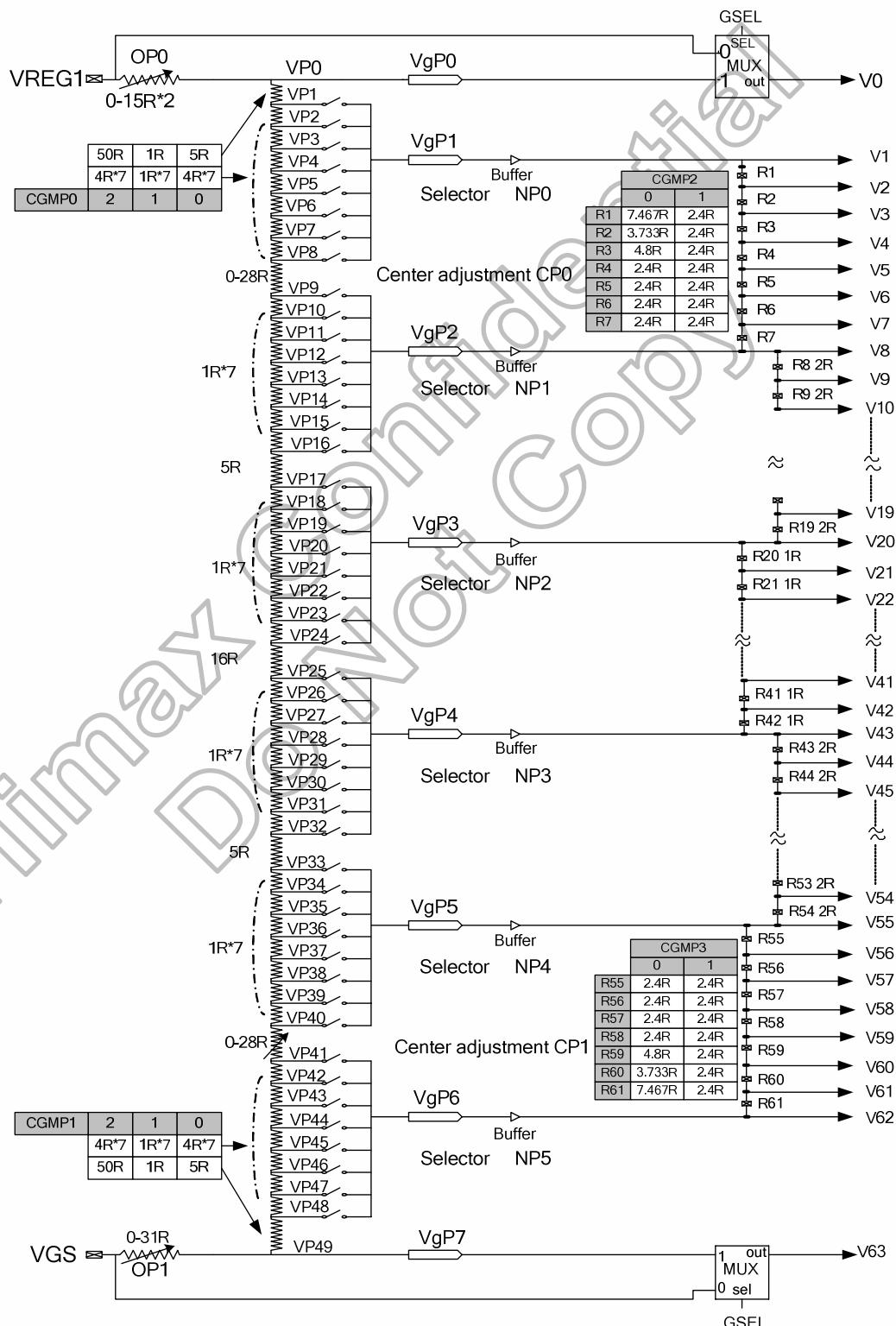
The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8-to-1 selectors (MP/N0~5), each of which has 8 inputs and generates one reference voltage output (Vg(P/N)1, 8, 20, 43, 55, 62). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	CP0 2-0	CN0 2-0	Variable resistor (VRCP/N0) for center adjustment
	CP1 2-0	CN1 2-0	Variable resistor (VRCP/N1) for center adjustment
Macro Adjustment	MP0 2-0	MN0 2-0	8-to-1 selector (voltage level of grayscale 1)
	MP1 2-0	MN1 2-0	8-to-1 selector (voltage level of grayscale 8)
	MP2 2-0	MN2 2-0	8-to-1 selector (voltage level of grayscale 20)
	MP3 2-0	MN3 2-0	8-to-1 selector (voltage level of grayscale 43)
	MP4 2-0	MN4 2-0	8-to-1 selector (voltage level of grayscale 55)
	MP5 2-0	MN5 2-0	8-to-1 selector (voltage level of grayscale 62)
Offset Adjustment	OP0 3-0	ON0 3-0	Variable resistor (VRDP/N0) for offset adjustment
	OP1 4-0	ON1 4-0	Variable resistor (VRDP/N1) for offset adjustment

Table 5. 10 Gamma-Adjustment Registers

### 5.9.4 Gamma Resister Stream and 8 to 1 Selector

The block consists of two gamma resister streams, one is for positive polarity and the other is for negative polarity, each one includes eight gamma reference voltages ( $V_{g(P/N)0}$ , 1, 8, 20, 43, 55, 62, 63). Furthermore, the block has a pin (VGS) to connect a variable resistor outside the chip for the variation between panels, if needed.



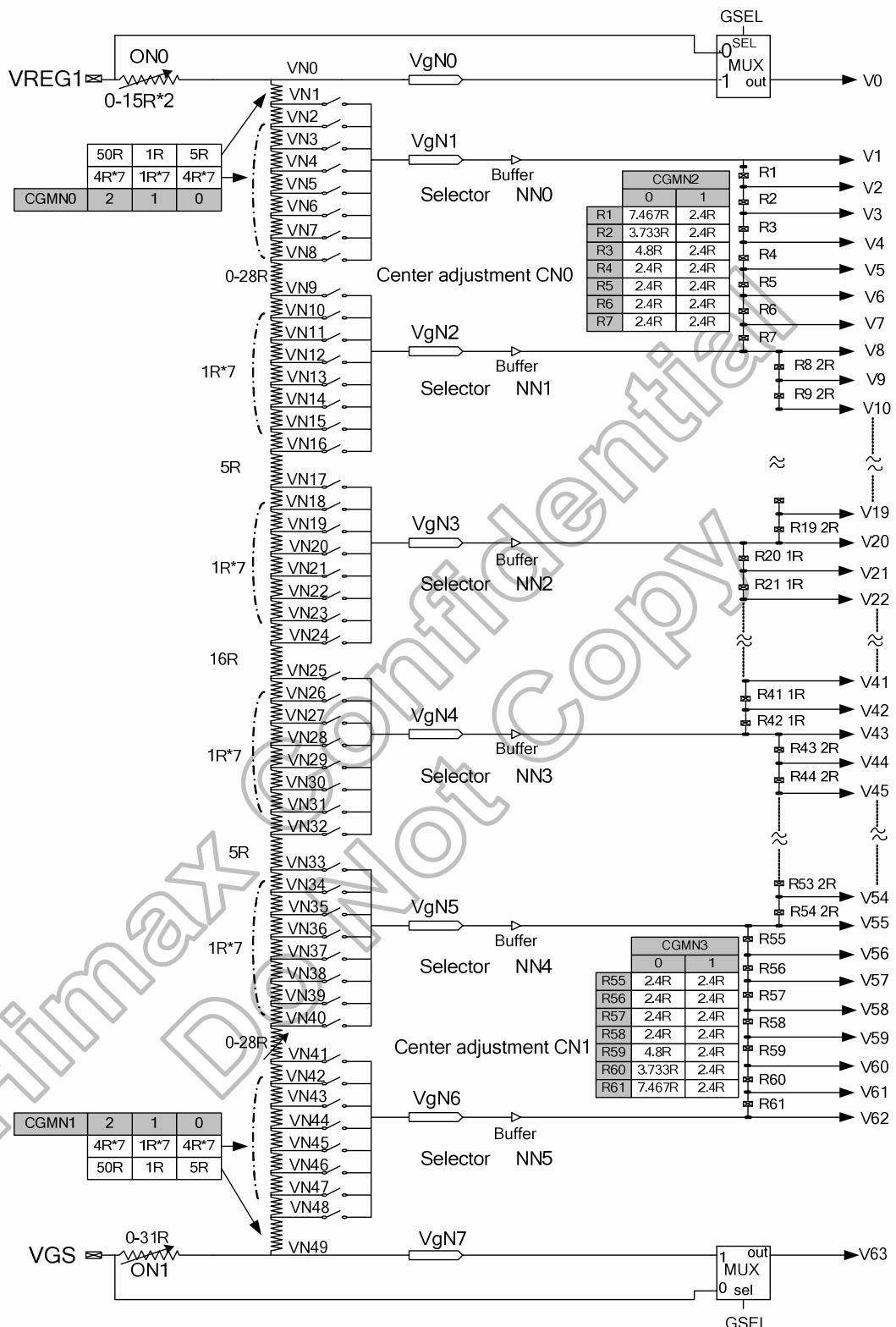


Figure 5.37 Gamma Resister Stream and Gamma Reference Voltage

### 5.9.5 Variable Resister

There are two types of variable resistors, one is for center adjustment, the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationship is shown as below.

Value in Register O(P/N)0 3-0	Resistance VRO(P/N)0
0000	0R
0001	2R
0010	4R
•	•
•	•
1101	26R
1110	28R
1111	30R

Table 5. 11 Offset Adjustment 0

Value in Register O(P/N)1 4-0	Resistance VRO(P/N)1
00000	0R
00001	1R
00010	2R
•	•
•	•
11101	29R
11110	30R
11111	31R

Table 5. 12 Offset Adjustment 1

Value in Register C(P/N)0/1 2-0	Resistance VRC(P/N)0/1
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 5. 13 Center Adjustment

### 8 to 1 Selector

The 8 to 1 selector has eight input voltages generated by gamma resister stream, and outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in macro adjustment register. There are six 8 to 1 selectors and the relationship is shown as below.

Value in Register M(P/N) 2-0	Voltage level					
	Vg(P/N) 1	Vg(P/N) 2	Vg(P/N) 3	Vg(P/N) 4	Vg(P/N) 5	Vg(P/N) 6
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Table 5. 14 Output Voltage of 8 to 1 Selector

The grayscale levels are determined by the following formulas:

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgP0	----	$[(VREG1-VD \cdot VROP0 / \text{SumRP}) \cdot GSEL + VREG1-(VREG1 \cdot GSEL)]$	VP0
VgP1	NP0 2-0=000	$VREG1-VD[(VROP0+(CGMP0*1R)+5R- (CGMP0*5R)) / \text{SumRP}]$	VP1
	NP0 2-0=001	$VREG1-VD[(VROP0+(CGMP0*2R)+9R- (CGMP0*9R)) / \text{SumRP}]$	VP2
	NP0 2-0=010	$VREG1-VD[(VROP0+(CGMP0*3R)+13R- (CGMP0*13R)) / \text{SumRP}]$	VP3
	NP0 2-0=011	$VREG1-VD[(VROP0+(CGMP0*4R)+17R- (CGMP0*17R)) / \text{SumRP}]$	VP4
	NP0 2-0=100	$VREG1-VD[(VROP0+(CGMP0*5R)+21R- (CGMP0*21R)) / \text{SumRP}]$	VP5
	NP0 2-0=101	$VREG1-VD[(VROP0+(CGMP0*6R)+25R- (CGMP0*25R)) / \text{SumRP}]$	VP6
	NP0 2-0=110	$VREG1-VD[(VROP0+(CGMP0*7R)+29R- (CGMP0*29R)) / \text{SumRP}]$	VP7
	NP0 2-0=111	$VREG1-VD[(VROP0+(CGMP0*8R)+33R- (CGMP0*33R)) / \text{SumRP}]$	VP8
VgP2	NP1 2-0=000	$VREG1-VD[(VROP0+(CGMP0*8R)+33R- (CGMP0*33R)) + VRCP0] / \text{SumRP}$	VP9
	NP1 2-0=001	$VREG1-VD[(VROP0+(CGMP0*9R)+34R- (CGMP0*34R)) + VRCP0] / \text{SumRP}$	VP10
	NP1 2-0=010	$VREG1-VD[(VROP0+(CGMP0*10R)+35R- (CGMP0*35R)) + VRCP0] / \text{SumRP}$	VP11
	NP1 2-0=011	$VREG1-VD[(VROP0+(CGMP0*11R)+36R- (CGMP0*36R)) + VRCP0] / \text{SumRP}$	VP12
	NP1 2-0=100	$VREG1-VD[(VROP0+(CGMP0*12R)+37R- (CGMP0*37R)) + VRCP0] / \text{SumRP}$	VP13
	NP1 2-0=101	$VREG1-VD[(VROP0+(CGMP0*13R)+38R- (CGMP0*38R)) + VRCP0] / \text{SumRP}$	VP14
	NP1 2-0=110	$VREG1-VD[(VROP0+(CGMP0*14R)+39R- (CGMP0*39R)) + VRCP0] / \text{SumRP}$	VP15
	NP1 2-0=111	$VREG1-VD[(VROP0+(CGMP0*15R)+40R- (CGMP0*40R)) + VRCP0] / \text{SumRP}$	VP16
VgP3	NP2 2-0=000	$VREG1-VD[(VROP0+(CGMP0*20R)+45R- (CGMP0*45R)) + VRCP0] / \text{SumRP}$	VP17
	NP2 2-0=001	$VREG1-VD[(VROP0+(CGMP0*21R)+46R- (CGMP0*46R)) + VRCP0] / \text{SumRP}$	VP18
	NP2 2-0=010	$VREG1-VD[(VROP0+(CGMP0*22R)+47R- (CGMP0*47R)) + VRCP0] / \text{SumRP}$	VP19
	NP2 2-0=011	$VREG1-VD[(VROP0+(CGMP0*23R)+48R- (CGMP0*48R)) + VRCP0] / \text{SumRP}$	VP20
	NP2 2-0=100	$VREG1-VD[(VROP0+(CGMP0*24R)+49R- (CGMP0*49R)) + VRCP0] / \text{SumRP}$	VP21
	NP2 2-0=101	$VREG1-VD[(VROP0+(CGMP0*25R)+50R- (CGMP0*50R)) + VRCP0] / \text{SumRP}$	VP22
	NP2 2-0=110	$VREG1-VD[(VROP0+(CGMP0*26R)+51R- (CGMP0*51R)) + VRCP0] / \text{SumRP}$	VP23
	NP2 2-0=111	$VREG1-VD[(VROP0+(CGMP0*27R)+52R- (CGMP0*52R)) + VRCP0] / \text{SumRP}$	VP24
VgP4	NP3 2-0=000	$VREG1-VD[(VROP0+(CGMP0*43R)+68R- (CGMP0*68R)) + VRCP0] / \text{SumRP}$	VP25
	NP3 2-0=001	$VREG1-VD[(VROP0+(CGMP0*44R)+69R- (CGMP0*69R)) + VRCP0] / \text{SumRP}$	VP26
	NP3 2-0=010	$VREG1-VD[(VROP0+(CGMP0*45R)+70R- (CGMP0*70R)) + VRCP0] / \text{SumRP}$	VP27
	NP3 2-0=011	$VREG1-VD[(VROP0+(CGMP0*46R)+71R- (CGMP0*71R)) + VRCP0] / \text{SumRP}$	VP28
	NP3 2-0=100	$VREG1-VD[(VROP0+(CGMP0*47R)+72R- (CGMP0*72R)) + VRCP0] / \text{SumRP}$	VP29
	NP3 2-0=101	$VREG1-VD[(VROP0+(CGMP0*48R)+73R- (CGMP0*73R)) + VRCP0] / \text{SumRP}$	VP30
	NP3 2-0=110	$VREG1-VD[(VROP0+(CGMP0*49R)+74R- (CGMP0*74R)) + VRCP0] / \text{SumRP}$	VP31
	NP3 2-0=111	$VREG1-VD[(VROP0+(CGMP0*50R)+75R- (CGMP0*75R)) + VRCP0] / \text{SumRP}$	VP32
VgP5	NP4 2-0=000	$VREG1-VD[(VROP0+(CGMP0*55R)+80R- (CGMP0*80R)) + VRCP0] / \text{SumRP}$	VP33
	NP4 2-0=001	$VREG1-VD[(VROP0+(CGMP0*56R)+81R- (CGMP0*81R)) + VRCP0] / \text{SumRP}$	VP34
	NP4 2-0=010	$VREG1-VD[(VROP0+(CGMP0*57R)+82R- (CGMP0*82R)) + VRCP0] / \text{SumRP}$	VP35
	NP4 2-0=011	$VREG1-VD[(VROP0+(CGMP0*58R)+83R- (CGMP0*83R)) + VRCP0] / \text{SumRP}$	VP36
	NP4 2-0=100	$VREG1-VD[(VROP0+(CGMP0*59R)+84R- (CGMP0*84R)) + VRCP0] / \text{SumRP}$	VP37
	NP4 2-0=101	$VREG1-VD[(VROP0+(CGMP0*60R)+85R- (CGMP0*85R)) + VRCP0] / \text{SumRP}$	VP38
	NP4 2-0=110	$VREG1-VD[(VROP0+(CGMP0*61R)+86R- (CGMP0*86R)) + VRCP0] / \text{SumRP}$	VP39
	NP4 2-0=111	$VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R)) + VRCP0] / \text{SumRP}$	VP40
VgP6	NP5 2-0=000	$VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R)) + VRCP0+VRCP1] / \text{SumRP}$	VP41
	NP5 2-0=001	$VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R)) + VRCP0+VRCP1+4R-(4R*CGMP1)+(CGMP1*1R)] / \text{SumRP}$	VP42
	NP5 2-0=010	$VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R)) + VRCP0+VRCP1+8R-(8R*CGMP1)+(CGMP1*2R)] / \text{SumRP}$	VP43
	NP5 2-0=011	$VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R)) + VRCP0+VRCP1+12R-(12R*CGMP1)+(CGMP1*3R)] / \text{SumRP}$	VP44
	NP5 2-0=100	$VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R)) + VRCP0+VRCP1+16R-(16R*CGMP1)+(CGMP1*4R)] / \text{SumRP}$	VP45
	NP5 2-0=101	$VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R)) + VRCP0+VRCP1+20R-(20R*CGMP1)+(CGMP1*5R)] / \text{SumRP}$	VP46
	NP5 2-0=110	$VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R)) + VRCP0+VRCP1+24R-(24R*CGMP1)+(CGMP1*6R)] / \text{SumRP}$	VP47
	NP5 2-0=111	$VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R)) + VRCP0+VRCP1+28R-(28R*CGMP1)+(CGMP1*7R)] / \text{SumRP}$	VP48
VgP7	----	$\{ VREG1-VD[(VROP0+(CGMP0*62R)+87R- (CGMP0*87R)) + VRCP0+VRCP1+33R-(33R*CGMP1)+(CGMP1*8R)] / \text{SumRP} \} * GSEL + VGS - (GSEL * VGS)$	VP49

Note: CGMP0=1 or 0, CGMP1=1 or 0.

Table 5. 15 Voltage Calculation Formula (Positive Polarity)

$$\text{SumRP} = 120R + VROP0 + VROP1 + VRCP0 + VRCP1 - (CGMP0*25R) - (CGMP0*25R);$$

$$\text{SumRN} = 120R + VRON0 + VRON1 + VRCN0 + VRCN1 - (CGMN1*25R) - (CGMN0*25R)$$

$$VD = (VREG1 - VGS)$$

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V0	VgP0	V32	VgP4+(VgP3-VgP4)*(11/23)
V1	VgP1	V33	VgP4+(VgP3-VgP4)*(10/23)
V2	VgP2+(VgP1-VgP2)*(CGMP2*14.4/16.8)+(VgP1-VgP2)*(1-CGMP2)*(18.133/25.6)	V34	VgP4+(VgP3-VgP4)*(9/23)
V3	VgP2+(VgP1-VgP2)*(CGMP2*12/16.8)+(VgP1-VgP2)*(1-CGMP2)*(4.4/25.6)	V35	VgP4+(VgP3-VgP4)*(8/23)
V4	VgP2+(VgP1-VgP2)*(CGMP2*9.6/16.8)+(VgP1-VgP2)*(1-CGMP2)*(9.6/25.6)	V36	VgP4+(VgP3-VgP4)*(7/23)
V5	VgP2+(VgP1-VgP2)*(CGMP2*7.2/16.8)+(VgP1-VgP2)*(1-CGMP2)*(7.2/25.6)	V37	VgP4+(VgP3-VgP4)*(6/23)
V6	VgP2+(VgP1-VgP2)*(CGMP2*4.8/16.8)+(VgP1-VgP2)*(1-CGMP2)*(4.8/25.6)	V38	VgP4+(VgP3-VgP4)*(5/23)
V7	VgP2+(VgP1-VgP2)*(CGMP2*2.4/16.8)+(VgP1-VgP2)*(1-CGMP2)*(2.4/25.6)	V39	VgP4+(VgP3-VgP4)*(4/23)
V8	VgP2	V40	VgP4+(VgP3-VgP4)*(3/23)
V9	VgP3+(VgP2-VgP3)*(22/24)	V41	VgP4+(VgP3-VgP4)*(2/23)
V10	VgP3+(VgP2-VgP3)*(20/24)	V42	VgP4+(VgP3-VgP4)*(1/23)
V11	VgP3+(VgP2-VgP3)*(18/24)	V43	VgP4
V12	VgP3+(VgP2-VgP3)*(16/24)	V44	VgP5+(VgP4-VgP5)*(22/24)
V13	VgP3+(VgP2-VgP3)*(14/24)	V45	VgP5+(VgP4-VgP5)*(20/24)
V14	VgP3+(VgP2-VgP3)*(12/24)	V46	VgP5+(VgP4-VgP5)*(18/24)
V15	VgP3+(VgP2-VgP3)*(10/24)	V47	VgP5+(VgP4-VgP5)*(16/24)
V16	VgP3+(VgP2-VgP3)*(8/24)	V48	VgP5+(VgP4-VgP5)*(14/24)
V17	VgP3+(VgP2-VgP3)*(6/24)	V49	VgP5+(VgP4-VgP5)*(12/24)
V18	VgP3+(VgP2-VgP3)*(4/24)	V50	VgP5+(VgP4-VgP5)*(10/24)
V19	VgP3+(VgP2-VgP3)*(2/24)	V51	VgP5+(VgP4-VgP5)*(8/24)
V20	VgP3	V52	VgP5+(VgP4-VgP5)*(6/24)
V21	VgP4+(VgP3-VgP4)*(22/23)	V53	VgP5+(VgP4-VgP5)*(4/24)
V22	VgP4+(VgP3-VgP4)*(21/23)	V54	VgP5+(VgP4-VgP5)*(2/24)
V23	VgP4+(VgP3-VgP4)*(20/23)	V55	VgP5
V24	VgP4+(VgP3-VgP4)*(19/23)	V56	VgP6+(VgP5-VgP6)*(CGMP3*14.4/16.8)+(VgP5-VgP6)*(1-CGMP3)*(23.2/25.6)
V25	VgP4+(VgP3-VgP4)*(18/23)	V57	VgP6+(VgP5-VgP6)*(CGMP3*12/16.8)+(VgP5-VgP6)*(1-CGMP3)*(20.8/25.6)
V26	VgP4+(VgP3-VgP4)*(17/23)	V58	VgP6+(VgP5-VgP6)*(CGMP3*9.6/16.8)+(VgP5-VgP6)*(1-CGMP3)*(18.4/25.6)
V27	VgP4+(VgP3-VgP4)*(16/23)	V59	VgP6+(VgP5-VgP6)*(CGMP3*7.2/16.8)+(VgP5-VgP6)*(1-CGMP3)*(16/25.6)
V28	VgP4+(VgP3-VgP4)*(15/23)	V60	VgP6+(VgP5-VgP6)*(CGMP3*4.8/16.8)+(VgP5-VgP6)*(1-CGMP3)*(11.2/25.6)
V29	VgP4+(VgP3-VgP4)*(14/23)	V61	VgP6+(VgP5-VgP6)*(CGMP3*2.4/16.8)+(VgP5-VgP6)*(1-CGMP3)*(7.467/25.6)
V30	VgP4+(VgP3-VgP4)*(13/23)	V62	VgP6
V31	VgP4+(VgP3-VgP4)*(12/23)	V63	VgP7

Table 5. 16 Voltage Calculation Formula of Grayscale Voltage (Positive Polarity)

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgN0	-	$[(VREG1-VD*VRON0 / \text{SumRN}) * \text{GSEL} + VREG1-(VREG1*\text{GSEL})]$	VN0
VgN1	NN0 2-0=000	$VREG1-VD[(VRON0+(CGMN0*1R)+5R- (CGMN0*5R)] / \text{SumRN}$	VN1
	NN0 2-0=001	$VREG1-VD[(VRON0+(CGMN0*2R)+9R- (CGMN0*9R)] / \text{SumRN}$	VN2
	NN0 2-0=010	$VREG1-VD[(VRON0+(CGMN0*3R)+13R- (CGMN0*13R)] / \text{SumRN}$	VN3
	NN0 2-0=011	$VREG1-VD[(VRON0+(CGMN0*4R)+17R- (CGMN0*17R)] / \text{SumRN}$	VN4
	NN0 2-0=100	$VREG1-VD[(VRON0+(CGMN0*5R)+21R- (CGMN0*21R)] / \text{SumRN}$	VN5
	NN0 2-0=101	$VREG1-VD[(VRON0+(CGMN0*6R)+25R- (CGMN0*25R)] / \text{SumRN}$	VN6
	NN0 2-0=110	$VREG1-VD[(VRON0+(CGMN0*7R)+29R- (CGMN0*29R)] / \text{SumRN}$	VN7
	NN0 2-0=111	$VREG1-VD[(VRON0+(CGMN0*8R)+33R- (CGMN0*33R)] / \text{SumRN}$	VN8
VgN2	NN1 2-0=000	$VREG1-VD[(VRON0+(CGMN0*8R)+33R- (CGMN0*33R) +VRCN0] / \text{SumRN}$	VN9
	NN1 2-0=001	$VREG1-VD[(VRON0+(CGMN0*9R)+34R- (CGMN0*34R) +VRCN0] / \text{SumRN}$	VN10
	NN1 2-0=010	$VREG1-VD[(VRON0+(CGMN0*10R)+35R- (CGMN0*35R) +VRCN0] / \text{SumRN}$	VN11
	NN1 2-0=011	$VREG1-VD[(VRON0+(CGMN0*11R)+36R- (CGMN0*36R) +VRCN0] / \text{SumRN}$	VN12
	NN1 2-0=100	$VREG1-VD[(VRON0+(CGMN0*12R)+37R- (CGMN0*37R) +VRCN0] / \text{SumRN}$	VN13
	NN1 2-0=101	$VREG1-VD[(VRON0+(CGMN0*13R)+38R- (CGMN0*38R) +VRCN0] / \text{SumRN}$	VN14
	NN1 2-0=110	$VREG1-VD[(VRON0+(CGMN0*14R)+39R- (CGMN0*39R) +VRCN0] / \text{SumRN}$	VN15
	NN1 2-0=111	$VREG1-VD[(VRON0+(CGMN0*15R)+40R- (CGMN0*40R) +VRCN0] / \text{SumRN}$	VN16
VgN3	NN2 2-0=000	$VREG1-VD[(VRON0+(CGMN0*20R)+45R- (CGMN0*45R) +VRCN0] / \text{SumRN}$	VN17
	NN2 2-0=001	$VREG1-VD[(VRON0+(CGMN0*21R)+46R- (CGMN0*46R) +VRCN0] / \text{SumRN}$	VN18
	NN2 2-0=010	$VREG1-VD[(VRON0+(CGMN0*22R)+47R- (CGMN0*47R) +VRCN0] / \text{SumRN}$	VN19
	NN2 2-0=011	$VREG1-VD[(VRON0+(CGMN0*23R)+48R- (CGMN0*48R) +VRCN0] / \text{SumRN}$	VN20
	NN2 2-0=100	$VREG1-VD[(VRON0+(CGMN0*24R)+49R- (CGMN0*49R) +VRCN0] / \text{SumRN}$	VN21
	NN2 2-0=101	$VREG1-VD[(VRON0+(CGMN0*25R)+50R- (CGMN0*50R) +VRCN0] / \text{SumRN}$	VN22
	NN2 2-0=110	$VREG1-VD[(VRON0+(CGMN0*26R)+51R- (CGMN0*51R) +VRCN0] / \text{SumRN}$	VN23
	NN2 2-0=111	$VREG1-VD[(VRON0+(CGMN0*27R)+52R- (CGMN0*52R) +VRCN0] / \text{SumRN}$	VN24
VgN4	NN3 2-0=000	$VREG1-VD[(VRON0+(CGMN0*43R)+68R- (CGMN0*68R) +VRCN0] / \text{SumRN}$	VN25
	NN3 2-0=001	$VREG1-VD[(VRON0+(CGMN0*44R)+69R- (CGMN0*69R) +VRCN0] / \text{SumRN}$	VN26
	NN3 2-0=010	$VREG1-VD[(VRON0+(CGMN0*45R)+70R- (CGMN0*70R) +VRCN0] / \text{SumRN}$	VN27
	NN3 2-0=011	$VREG1-VD[(VRON0+(CGMN0*46R)+71R- (CGMN0*71R) +VRCN0] / \text{SumRN}$	VNP8
	NN3 2-0=100	$VREG1-VD[(VRON0+(CGMN0*47R)+72R- (CGMN0*72R) +VRCN0] / \text{SumRN}$	VN29
	NN3 2-0=101	$VREG1-VD[(VRON0+(CGMN0*48R)+73R- (CGMN0*73R) +VRCN0] / \text{SumRN}$	VN30
	NN3 2-0=110	$VREG1-VD[(VRON0+(CGMN0*49R)+74R- (CGMN0*74R) +VRCN0] / \text{SumRN}$	VN31
	NN3 2-0=111	$VREG1-VD[(VRON0+(CGMN0*50R)+75R- (CGMN0*75R) +VRCN0] / \text{SumRN}$	VN32
VgN5	NN4 2-0=000	$VREG1-VD[(VRON0+(CGMN0*55R)+80R- (CGMN0*80R) +VRCN0] / \text{SumRN}$	VN33
	NN4 2-0=001	$VREG1-VD[(VRON0+(CGMN0*56R)+81R- (CGMN0*81R) +VRCN0] / \text{SumRN}$	VN34
	NN4 2-0=010	$VREG1-VD[(VRON0+(CGMN0*57R)+82R- (CGMN0*82R) +VRCN0] / \text{SumRN}$	VN35
	NN4 2-0=011	$VREG1-VD[(VRON0+(CGMN0*58R)+83R- (CGMN0*83R) +VRCN0] / \text{SumRN}$	VN36
	NN4 2-0=100	$VREG1-VD[(VRON0+(CGMN0*59R)+84R- (CGMN0*84R) +VRCN0] / \text{SumRN}$	VN37
	NN4 2-0=101	$VREG1-VD[(VRON0+(CGMN0*60R)+85R- (CGMN0*85R) +VRCN0] / \text{SumRN}$	VN38
	NN4 2-0=110	$VREG1-VD[(VRON0+(CGMN0*61R)+86R- (CGMN0*86R) +VRCN0] / \text{SumRN}$	VN39
	NN4 2-0=111	$VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0] / \text{SumRN}$	VN40
VgN6	NN5 2-0=000	$VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1] / \text{SumRN}$	VN41
	NN5 2-0=001	$VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+4R-(4R*CGMN1)+(CGMN1*1R)] / \text{SumRN}$	VN42
	NN5 2-0=010	$VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+8R-(8R*CGMN1)+(CGMN1*2R)] / \text{SumRN}$	VN43
	NN5 2-0=011	$VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+12R-(12R*CGMN1)+(CGMN1*3R)] / \text{SumRN}$	VN44
	NN5 2-0=100	$VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+16R-(16R*CGMN1)+(CGMN1*4R)] / \text{SumRN}$	VN45
	NN5 2-0=101	$VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+20R-(20R*CGMN1)+(CGMN1*5R)] / \text{SumRN}$	VN46
	NN5 2-0=110	$VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+24R-(24R*CGMN1)+(CGMN1*6R)] / \text{SumRN}$	VN47
	NN5 2-0=111	$VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+28R-(28R*CGMN1)+(CGMN1*7R)] / \text{SumRN}$	VN48
VgN7	-	{ $VREG1-VD[(VRON0+(CGMN0*62R)+87R- (CGMN0*87R) +VRCN0+VRCN1+33R-(33R*CGMN1)+(CGMN1*8R)] / \text{SumRN}}$ *GSEL+VGS-(GSEL*VGS) }	VN49

Note: CGMN0=1 or 0, CGMN1=1 or 0

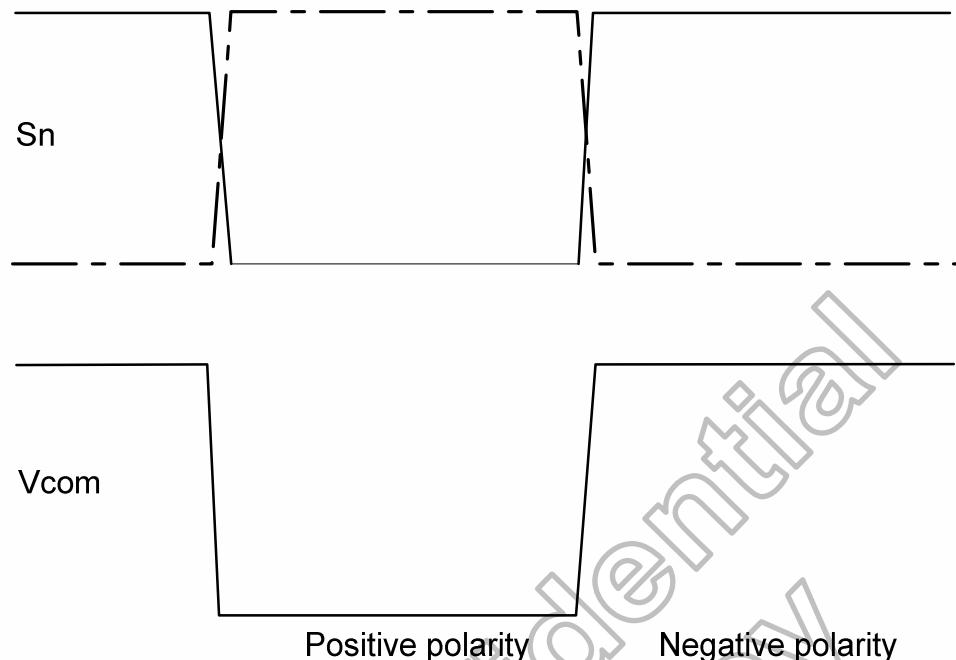
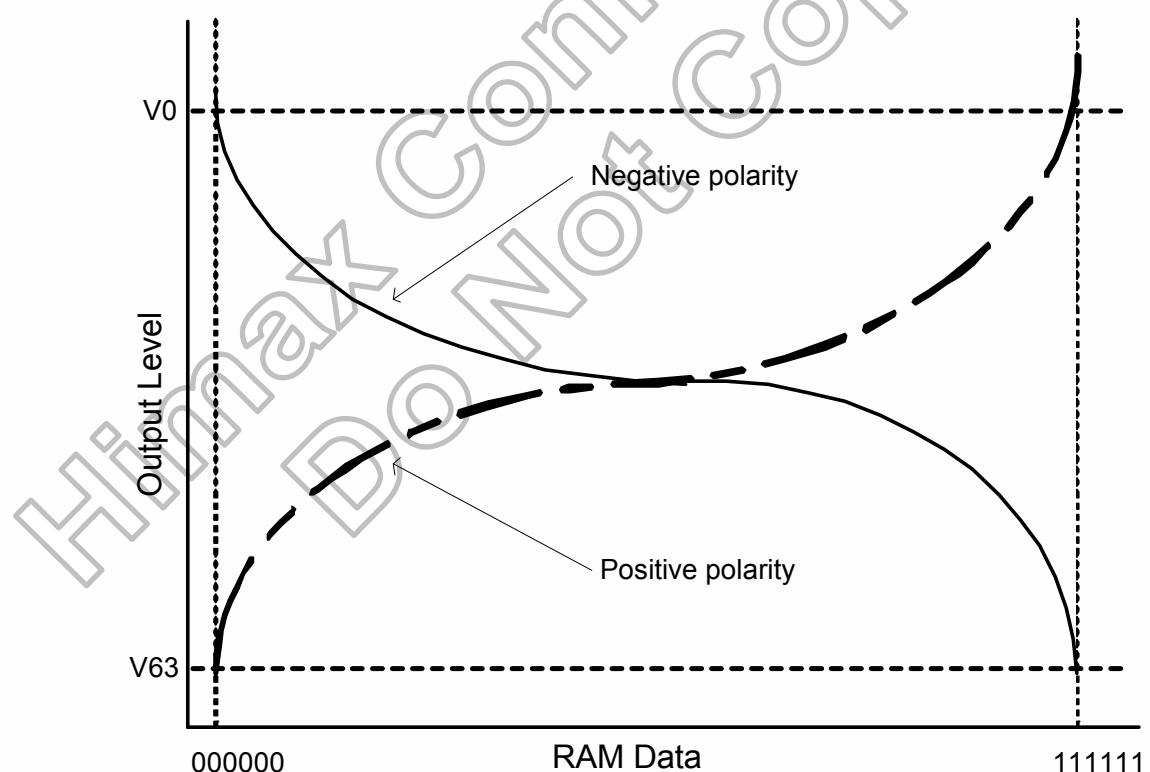
Table 5. 17 Voltage Calculation Formula (Negative Polarity)

SumRP = 120R +VROP0+ VROP1+ VRCP0+ VRCP1-(CGMP1\*25R)-(CGMP0\*25R);  
 SumRN = 120R+ VRON0+ VRON1+ VRCN0 + VRCN1-(CGMN1\*25R)-(CGMN0\*25R)  
 VD=(VREG1-VGS)

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V0	VgN0	V32	VgN4+(VgN3-VgN4)*(11/23)
V1	VgN1	V33	VgN4+(VgN3-VgN4)*(10/23)
V2	VgN2+(VgN1-VgN2)*(CGMN2*14.4/16.8)+ (VgN1-VgN2)*(1-CGMN2)*(18.133/25.6)	V34	VgN4+(VgN3-VgN4)*(9/23)
V3	VgN2+(VgN1-VgN2)*(CGMN2*12/16.8)+ (VgN1-VgN2)*(1-CGMN2)*(14.4/25.6)	V35	VgN4+(VgN3-VgN4)*(8/23)
V4	VgN2+(VgN1-VgN2)*(CGMN2*9.6/16.8)+ (VgN1-VgN2)*(1-CGMN2)*(9.6/25.6)	V36	VgN4+(VgN3-VgN4)*(7/23)
V5	VgN2+(VgN1-VgN2)*(CGMN2*7.2/16.8)+ (VgN1-VgN2)*(1-CGMN2)*(7.2/25.6)	V37	VgN4+(VgN3-VgN4)*(6/23)
V6	VgN2+(VgN1-VgN2)*(CGMN2*4.8/16.8)+ (VgN1-VgN2)*(1-CGMN2)*(4.8/25.6)	V38	VgN4+(VgN3-VgN4)*(5/23)
V7	VgN2+(VgN1-VgN2)*(CGMN2*2.4/16.8)+ (VgN1-VgN2)*(1-CGMN2)*(2.4/25.6)	V39	VgN4+(VgN3-VgN4)*(4/23)
V8	VgN2	V40	VgN4+(VgN3-VgN4)*(3/23)
V9	VgN3+(VgN2-VgN3)*(22/24)	V41	VgN4+(VgN3-VgN4)*(2/23)
V10	VgN3+(VgN2-VgN3)*(20/24)	V42	VgN4+(VgN3-VgN4)*(1/23)
V11	VgN3+(VgN2-VgN3)*(18/24)	V43	VgN4
V12	VgN3+(VgN2-VgN3)*(16/24)	V44	VgN5+(VgN4-VgN5)*(22/24)
V13	VgN3+(VgN2-VgN3)*(14/24)	V45	VgN5+(VgN4-VgN5)*(20/24)
V14	VgN3+(VgN2-VgN3)*(12/24)	V46	VgN5+(VgN4-VgN5)*(18/24)
V15	VgN3+(VgN2-VgN3)*(10/24)	V47	VgN5+(VgN4-VgN5)*(16/24)
V16	VgN3+(VgN2-VgN3)*(8/24)	V48	VgN5+(VgN4-VgN5)*(14/24)
V17	VgN3+(VgN2-VgN3)*(6/24)	V49	VgN5+(VgN4-VgN5)*(12/24)
V18	VgN3+(VgN2-VgN3)*(4/24)	V50	VgN5+(VgN4-VgN5)*(10/24)
V19	VgN3+(VgN2-VgN3)*(2/24)	V51	VgN5+(VgN4-VgN5)*(8/24)
V20	VgN3	V52	VgN5+(VgN4-VgN5)*(6/24)
V21	VgN4+(VgN3-VgN4)*(22/23)	V53	VgN5+(VgN4-VgN5)*(4/24)
V22	VgN4+(VgN3-VgN4)*(21/23)	V54	VgN5+(VgN4-VgN5)*(2/24)
V23	VgN4+(VgN3-VgN4)*(20/23)	V55	VgN5
V24	VgN4+(VgN3-VgN4)*(19/23)	V56	VgN6+(VgN5-VgN6)*(CGMN3*14.4/16.8)+ (VgN5-VgN6)*(1-CGMN3)*(23.2/25.6)
V25	VgN4+(VgN3-VgN4)*(18/23)	V57	VgN6+(VgN5-VgN6)*(CGMN3*12/16.8)+ (VgN5-VgN6)*(1-CGMN3)*(20.8/25.6)
V26	VgN4+(VgN3-VgN4)*(17/23)	V58	VgN6+(VgN5-VgN6)*(CGMN3*9.6/16.8)+ (VgN5-VgN6)*(1-CGMN3)*(18.4/25.6)
V27	VgN4+(VgN3-VgN4)*(16/23)	V59	VgN6+(VgN5-VgN6)*(CGMN3*7.2/16.8)+ (VgN5-VgN6)*(1-CGMN3)*(16/25.6)
V28	VgN4+(VgN3-VgN4)*(15/23)	V60	VgN6+(VgN5-VgN6)*(CGMN3*4.8/16.8)+ (VgN5-VgN6)*(1-CGMN3)*(11.2/25.6)
V29	VgN4+(VgN3-VgN4)*(14/23)	V61	VgN6+(VgN5-VgN6)*(CGMN3*2.4/16.8)+ (VgN5-VgN6)*(1-CGMN3)*(7.467/25.6)
V30	VgN4+(VgN3-VgN4)*(13/23)	V62	VgN6
V31	VgN4+(VgN3-VgN4)*(12/23)	V63	VgN7

Table 5. 18 Voltage Calculation Formula of Grayscale Voltage (Negative Polarity)

## Relationship between GRAM Data and Output Level (INVON = "0")

Figure 5. 38 Relationship between Source Output and  $V_{com}$ 

(Same characteristic for each RGB)

Figure 5. 39 Relationship between GRAM Data and Output Level

## 5.10 Scan Mode Setting

The HX8347-A01 can set internal register SM and GS bits to determine the pin assignment of gate. The combination of SM and GS settings allows changing the shift direction of gate outputs by connecting LCD panel with the HX8347-A01.

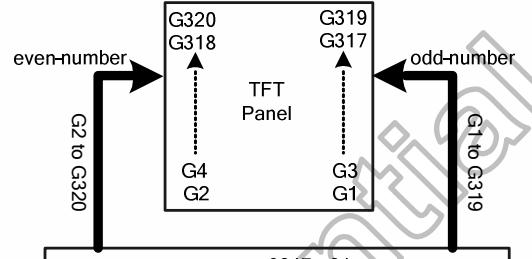
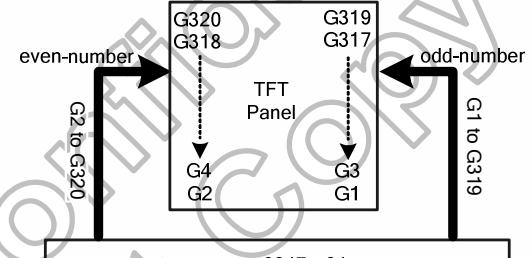
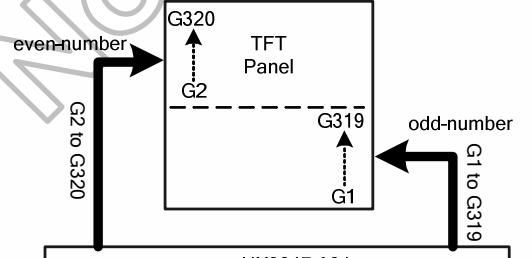
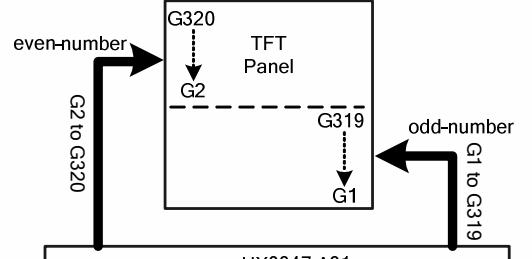
SM	GS	Scan direction
0	0	 <p>G2 to G320 G1 to G319</p> <p>TFT Panel G320, G318, G319, G317, G3, G1, G4, G2</p> <p>HX8347-A01 G1, G2, G3, ..., G157, G158, ..., G319, G320</p>
0	1	 <p>G2 to G320 G1 to G319</p> <p>TFT Panel G320, G318, G319, G317, G3, G1, G4, G2</p> <p>HX8347-A01 G320, G319, G318, ..., G158, G157, ..., G2, G1</p>
1	0	 <p>G2 to G320 G1 to G319</p> <p>TFT Panel G320, G319, G3, G1, G2, G4, ..., G318, G320</p> <p>HX8347-A01 G1, G3, G5, ..., G319, G2, G4, ..., G318, G320</p>
1	1	 <p>G2 to G320 G1 to G319</p> <p>TFT Panel G320, G319, G318, ..., G2, G319, G317, ..., G3, G1</p> <p>HX8347-A01 G320, G318, ..., G2, G319, G317, ..., G3, G1</p>

Figure 5. 40 Scan Function

## 5.11 Oscillator

The HX8347-A01 can oscillate an internal R-C oscillator with an internal oscillation resistor (Rf). The oscillation frequency is changed according to the RADJ[3:0] internal register. Please refer to extended command set **93h**. The default frequency is **5.58MHz**.

HX8347-A01

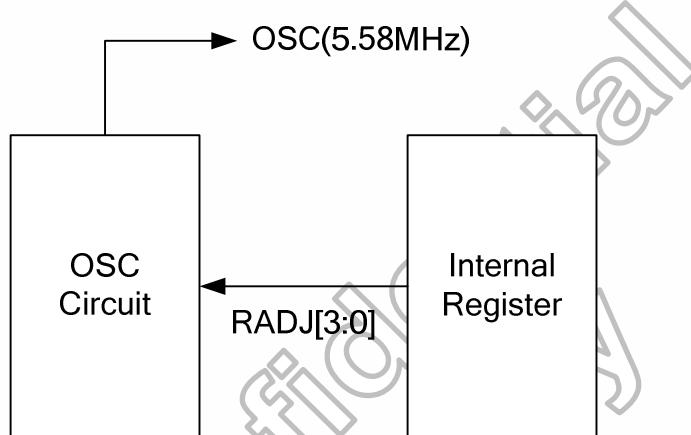


Figure 5.41 Oscillation Circuit

## 5.12 Register Setting Flow (Register-Content Interface mode only)

The following are the sequences of register setting flow that applied to the HX8347-A01 driving the TFT display, when operate in Register-Content interface mode.

### Display On/Off Set flow

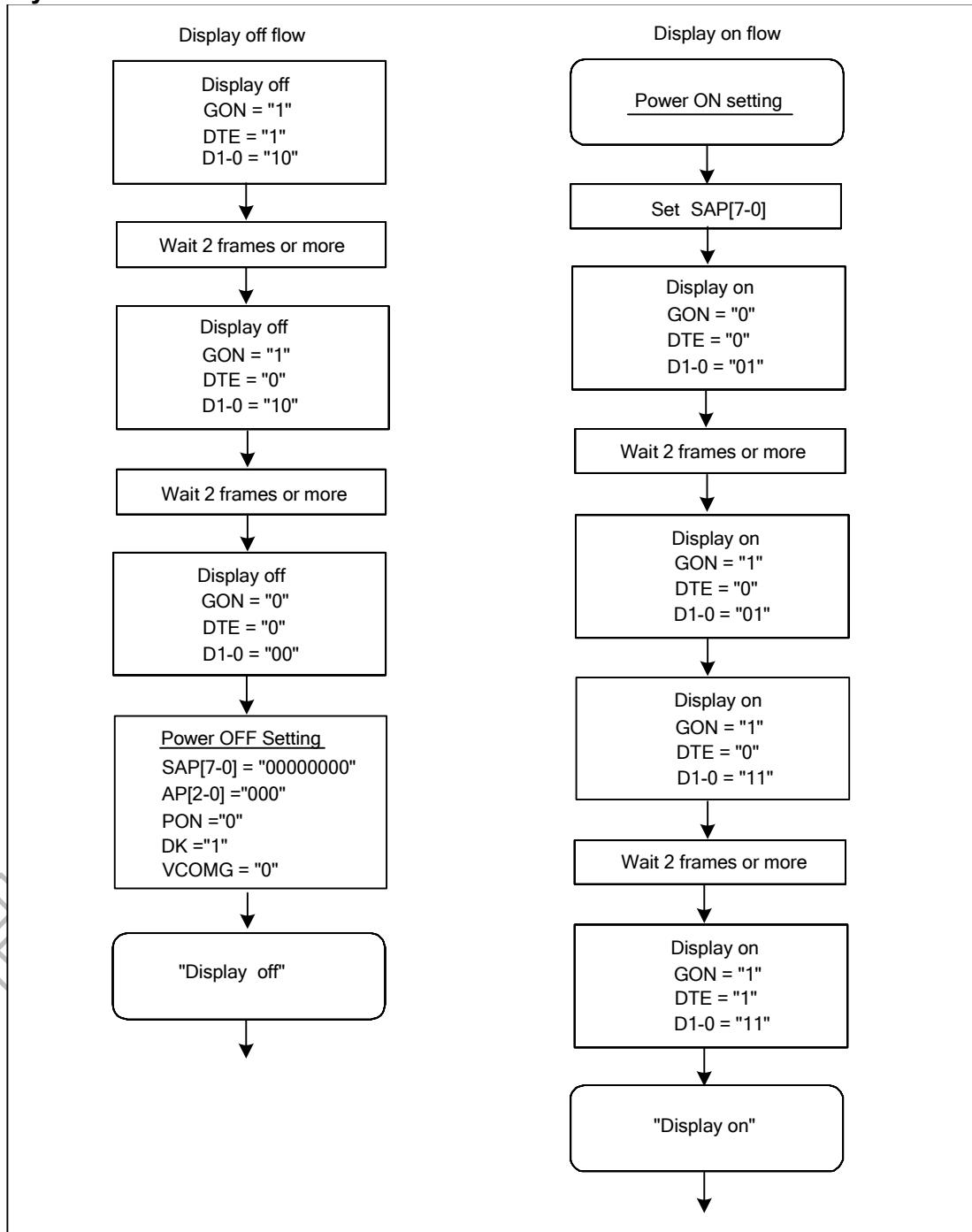
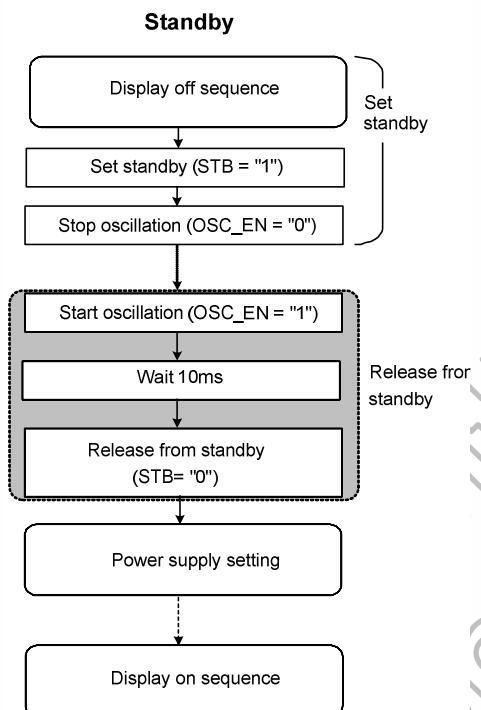


Figure 5. 42 Display On/Off Set Sequence

**Standby Mode Set flow**

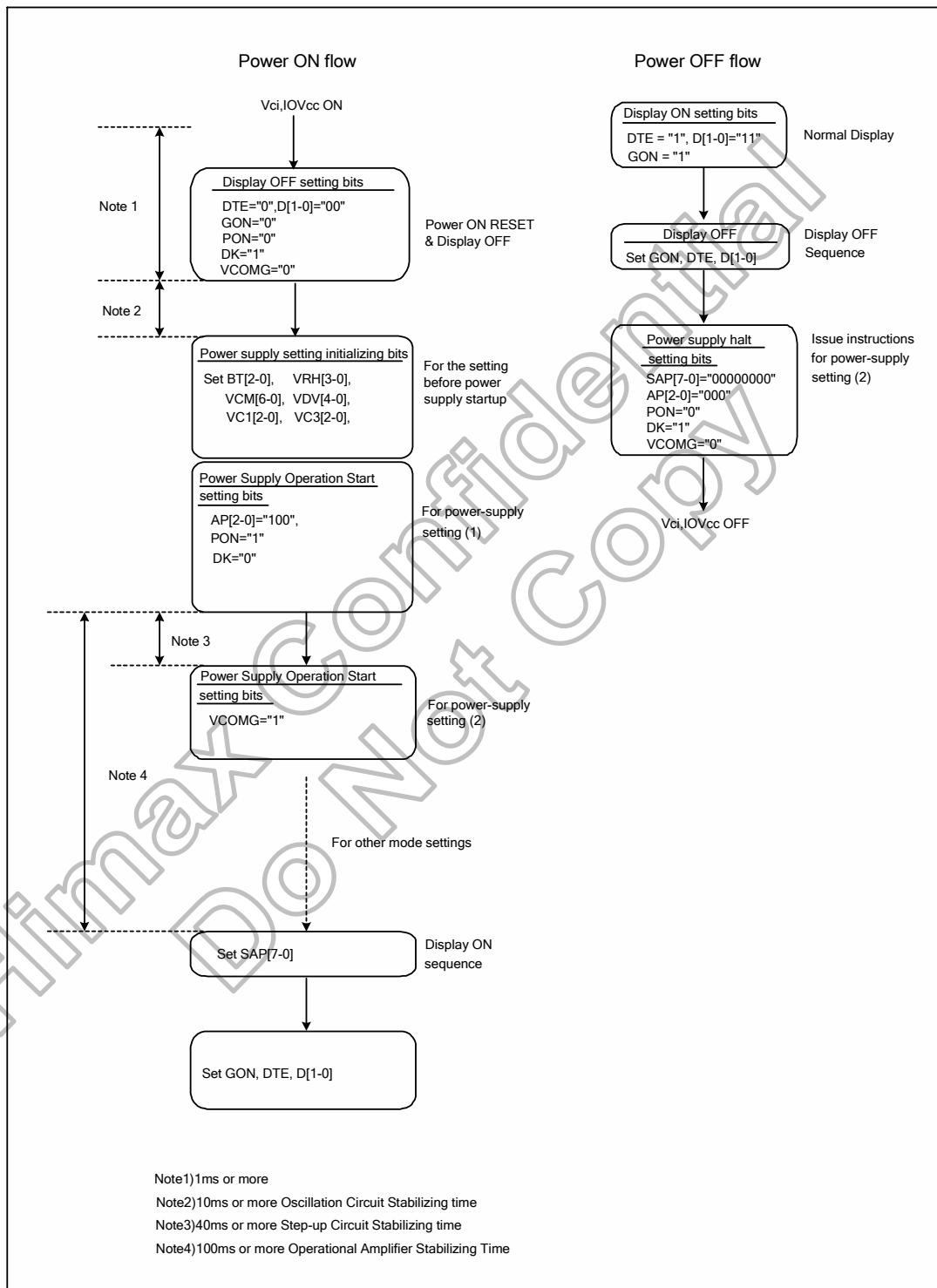
**Note:** HX8347-A01 doesn't have the Sleep mode in Register-Content interface mode.

**Figure 5. 43 Standby Mode Setting Sequence**

## 5.13 Power Supply Setting

The power supply setting sequence of the HX8347-A01 is follow as blew.

### Power Supply Setting Flow



**Figure 5. 44 Power Supply Setting Flow**

## 5.14 Input / Output Pin State

### 5.14.1 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D17 to D0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
VSYNC	Low	Low	Low
TEST1	Low	Low	Low

**Note:** There will be no output from D17-D0 during Power On/Off sequence, Hardware Reset and Software Reset.

Table 5. 19 State of Output or Bi-directional (I/O) Pins

### 5.14.2 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
NRESET	See Section 5.12	Input valid	Input valid	Input valid	See Section 5.12
NCS	Input valid	Input valid	Input valid	Input valid	Input valid
DNC_SCL	Input valid	Input valid	Input valid	Input valid	Input valid
NWR_RNW	Input valid	Input valid	Input valid	Input valid	Input valid
NRD_E	Input valid	Input valid	Input valid	Input valid	Input valid
D17 to D0	Input valid	Input valid	Input valid	Input valid	Input valid
HSYNC	Input valid	Input valid	Input valid	Input valid	Input valid
VSYNC	Input valid	Input valid	Input valid	Input valid	Input valid
DOTCLK	Input valid	Input valid	Input valid	Input valid	Input valid
ENABLE	Input valid	Input valid	Input valid	Input valid	Input valid
OSC, BURN, P68, BS2, BS1,BS0,	Input valid	Input valid	Input valid	Input valid	Input valid
EXTC	Input valid	Input valid	Input valid	Input valid	Input valid

Table 5. 20 State of Input Pins

## 5.15 OTP Programming

OTP_INDEX	D7	D6	D5	D4	D3	D2	D1	D0
0x00								Himax internal use(no open)
0x01								Himax internal use(no open)
0x02								Himax internal use(no open)
0x03								Himax internal use(no open)
0x04								Himax internal use(no open)
0x05								Himax internal use(no open)
0x06								Himax internal use(no open)
0x07								Himax internal use(no open)
0x08	BGR_PANEL	DIV_I[1:0]		DIV_PI[1:0]	DIV_N[1:0]			RGB_EN
0x09		VDV[3:0]		SM_PANEL	SS_PANEL GS_PANEL	GS_PANEL	REV_PANEL	
0x0A				VCM[6:0]				VDV[4]
0x0B								Himax internal use(no open)
0x0C								Himax internal use(no open)
0x0D				ID2[6:0]				NVALID3
0x0E					ID3[7:0]			
0x0F					ID1[7:0]			

Note: (1) The all OTP memory bit default value are "1".

(2) BGR\_PANEL, SM\_PANEL, SS\_PANEL, GS\_PANEL, REV\_PANEL are don't care in Register-Content Interface mode and these bit will program to "0".

(3) If OTP\_index 0x0Dh no programming, HX8347-A01 will no reload OTP value to related register.

Table 5. 21 OTP memory table

## Programming Flow

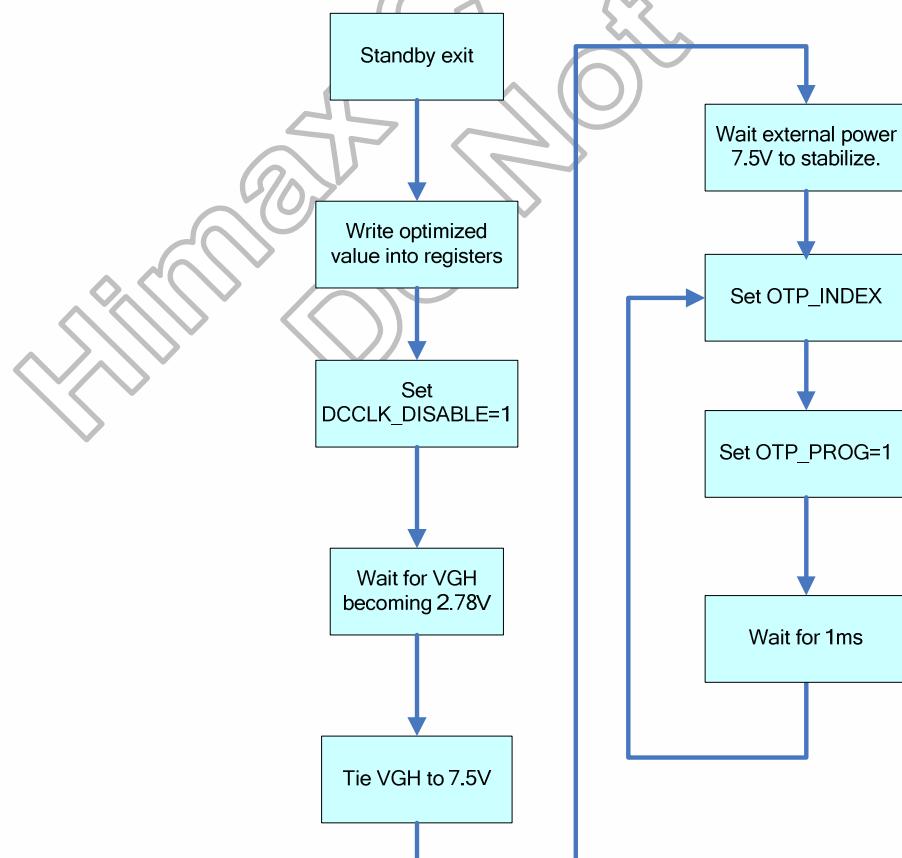
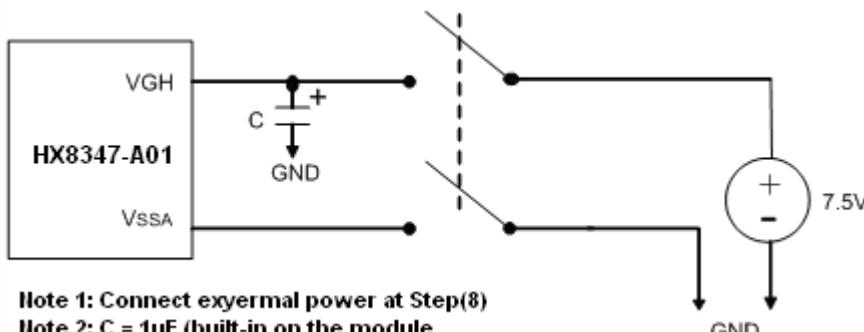


Figure 5. 45 OTP Programming Flow

## Programming sequence

Step	Operation		
	Command	Register	Description
1	Power on and reset the module		
2	Set OTP_LOAD_DISABLE=1, disable the auto-loading function.		
3	OSC_EN=1, STB=0		
4	Wait 120ms		
5	Write optimized value to related register		
	Command	Register	Description
	Cycle Control4 (3Dh)	DIV_I[1:0], DIV_PI[1:0], DIV_N[1:0]	The division ratio of clocks in display mode
	RGB interface control 1 (38h)	RGB_EN	RGB I/F Disable/Enable
	VCOM Control2 (44h)	VCM[6:0]	VcomH voltage (High level voltage of VCOM)
	VCOM Control3 (45h)	VDV[4:0]	Vcom amplitude (VcomL = VcomH – Vcom amplitude, VcomL ≥ VCL+0.5V)
	Internal Use16 (64h)	ID1[7:0]	LCD module/driver version
6	Set OTP_DCCLK_DISABLE=1, disable internal pumping clock.		
7	Wait 500ms for power down		
8	Connect external power 7.5V to VGH pin		
9	Wait 100ms for external power 7.5V to stabilize.		
10	Specify OTP_index		
	OTP_index	Parameter	
	0x08h	BGR_PANEL, DIV_I[1:0], DIV_PI[1:0], DIV_N[1:0], RGB_EN	
	0x09h	VDV[3:0], SM_PANEL, SS_PANEL, GS_PANEL, REV_PANEL	
	0x0Ah	VCM[6:0], VDV[4]	
	0x0Dh	ID2[6:0]	
	0x0Eh	ID3[7:0]	
	0x0Fh	ID1[7:0]	
Note: BGR_PANEL, SM_PANEL, SS_PANEL, GS_PANEL, REV_PANEL are don't care in Register-Content Interface mode and these bit will program to "0".			
11	Set OTP_Mask=0x00h, programming all of the bit of one parameter.		
12	Set OTP_PROG=1, Internal register begin write to OTP according to OTP_index.		
13	Wait 1 ms		
14	Complete programming one parameter to OTP. If continue to programming other parameter, return to step (10). Otherwise, power off the module and remove the external power on VGH pin.		

## Programming circuitry



## 5.16 Free Running Mode Specification

Burn-in of TFT displays consists of driving each module for 10hr at a temperature of 60°C. In order to drive the modules, it requires extra electronics. To reduce the burn-in cost, it is requested that the driver IC will generate the required display image without requiring extra electronics. We term this a free running mode (FR-mode). For burn-in, it is sufficient that the display is powered up with a plane saturated black or saturated white pattern. Black should be used for burn-in, since this result in a larger pixel voltage. White is used to verify if the free running mode is properly functioning. Please note that the black and the white pattern are reversed in case of a normally black display.

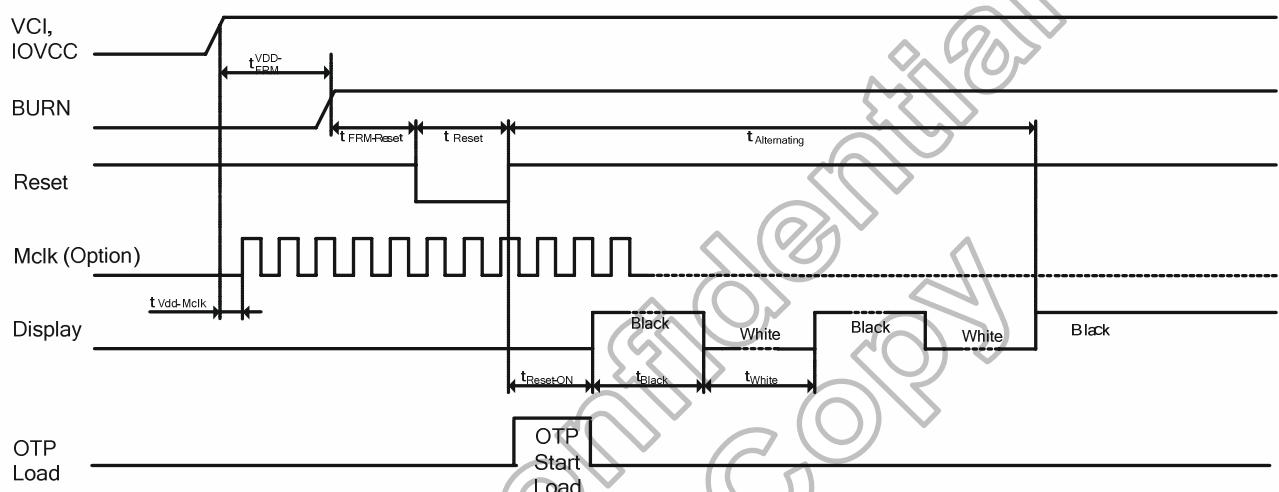
Parameter	Symbol	Description
Power supply pins	IOVCC, VCI	All power supply pins
Free running mode	BURN	BURN=1, FR-mode is enabled.
Reset	NRESET	Active low pulse in order to start the FR-mode.
Chip select <sup>(1)</sup>	NCS	This pin will be left open during FRM mode.
Data enable <sup>(1)</sup>	ENABLE	This pin will be left open during FRM mode.
Reads/not write <sup>(1)</sup>	NWR_RNW	This pin will be left open during FRM mode.
Data/not command <sup>(1)</sup>	DNC_SCL	This pin will be left open during FRM mode.
Interface select <sup>(1)</sup>	IFSEL0	This pin will be left open during FRM mode.
Horizontal sync <sup>(1)</sup>	H SYNC	This pin will be left open during FRM mode.
Vertical sync <sup>(1)</sup>	V SYNC	This pin will be left open during FRM mode.
Data clock	DOTCLK	This pin will be left open during FRM mode.
CPU I/F Data <sup>(1)</sup>	D[0..17]	This pin will be left open during FRM mode.
SPI I/F Data <sup>(1)</sup>	SDI, SDO	This pin will be left open during FRM mode.

**Note:** (1) As a general rule, all control pins of the interfaces like chip-select, data-enable, etc, must be disabled, all mode select pins like data-not-command, interface-select etc and all data-bus pins must be set to either logic high or logic low during the FR-mode.

**Table 5. 22 Pin Information**

## Power-on Sequence

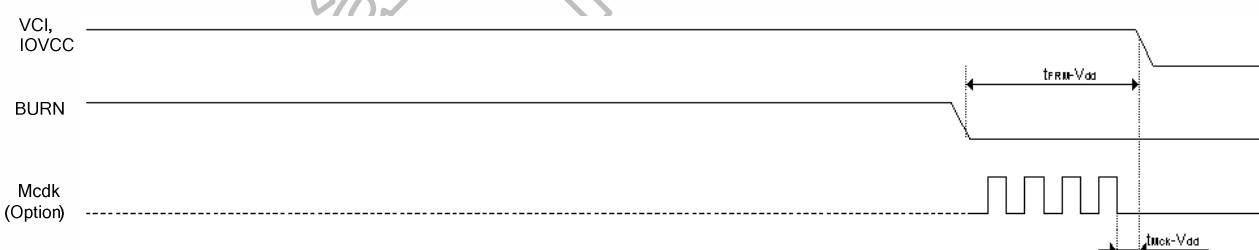
The FR-mode starts automatically after the power supply is switched on and a reset pulse is applied to the Reset-pin, if the BURN pin is set to logical high. In case of separate supply pins for the analogue supply and digital supply, both supply pins will be connected together, if it is supported by the driver specification. Otherwise, each supply voltage will be switched on separately according to the requested power-on sequence. The BURN and all other digital I/F pins, which will be set to logic high during the free running mode, can be switched to logic high together with the digital supply pin. The FR-mode will be restarted if the reset pulse is applied a second time. The OTP starts to load when Reset leaves low to high.



**Figure 5. 46 Power On Sequence of FR-mode (for Normally–White Panel)**

## Power off Sequence

The power supply can be switched off any time.



**Figure 5. 47 Power Off Sequence of FR-mode**

**Free Running Mode Display**

The display will show an alternating black and white picture for about the first 5 minutes. The black to white ratio shall be 50%/50%. The time of the black and white pattern shall be around 1 seconds in order to avoid a too long waiting time to verify that the FR-mode is functioning properly. The display is switched to a static black pattern after the alternating mode is finished. Thus, most efficient burn-in stress is ensured. The display shall work in idle-mode. There is no special restriction for the frame frequency. It can be between 5 and 100Hz. The frame frequency will be set according to the parameter in the OTP.

<b>Alternating Black and White Pattern</b>	$t_{\text{Alternating}}$	-	5	-	min
<b>Master Clock Frequency</b>	$f_{\text{Mclk}}$	-	-	10	MHz

Table 5. 23 Frequency Definition of Free Running Mode Display

## 6. Command

### 6.1 Command Set

**Table 6. 1 List Table of Register Set**

Register No.	Register	W/R	RS	Upper Code D[17:8]	Lower Code								Comment
					D7	D6	D5	D4	D3	D2	D1	D0	
R01h	Display Mode control	W/R	1	*	*	*	*	*	IDMON(0)	INVON(0)	NORON(1)	PTLO N(0)	
R02h	Column address start 2	W/R	1	*					SC[15:8] (8'b0)				
R03h	Column address start 1	W/R	1	*					SC[7:0] (8'b0)				
R04h	Column address end 2	W/R	1	*					EC[15:8] (8'b0)				
R05h	Column address end 1	W/R	1	*					EC[7:0] (8'b1110_1111)				
R06h	Row address start 2	W/R	1	*					SP[15:8] (8'b0)				
R07h	Row address start 1	W/R	1	*					SP[7:0] (8'b0)				
R08h	Row address end 2	W/R	1	*					EP[15:8] (8'b0000_0001)				
R09h	Row address end 1	W/R	1	*					EP[7:0] (8'b0011_1111)				
R0Ah	Partial area start row 2	W/R	1	*					PSL[15:8] (8'b0)				
R0Bh	Partial area start row 1	W/R	1	*					PSL[7:0] (8'b0)				
R0Ch	Partial area end row 2	W/R	1	*					PEL[15:8] (8'b0000_0001)				
R0Dh	Partial area end row 1	W/R	1	*					PEL[7:0] (8'b0011_1111)				
R0Eh	Vertical Scroll Top fixed area 2	W/R	1	*					TFA[15:8] (8'b0)				
R0Fh	Vertical Scroll Top fixed area 1	W/R	1	*					TFA[7:0] (8'b0)				
R10h	Vertical Scroll height area 2	W/R	1	*					VSA[15:8] (8'b0000_0001)				
R11h	Vertical Scroll height area 1	W/R	1	*					VSA[7:0] (8'b0100_0000)				
R12h	Vertical Scroll Button area 2	W/R	1	*					BFA[15:8] (8'b0)				
R13h	Vertical Scroll Button area 1	W/R	1	*					BFA [7:0] (8'b0)				
R14h	Vertical Scroll Start address 2	W/R	1	*					VSP [15:8] (8d'0)				
R15h	Vertical Scroll Start address 1	W/R	1	*					VSP [7:0] (8d'0)				
R16h	Memory Access control	W/R	1	*	MY(0)	MX(0)	MV(0)	*	BGR(0)	*	*	*	
R18h	Gate Scan control	W/R	1	*	*	*	*	*	*	*	*	SCROL L_ON(0)	SM(0)
R19h	OSC Control 1	W/R	1	*	*	CADJ[3:0] (1001)			CUADJ[2:0] (000)			OSC_EN(0)	
R1Ah	OSC Control 2	W/R	1	*	*	*	*	*	*	*	*	*	OSC_TEST(0)
R1Bh	Power Control 1	W/R	1	*	GASEN B(0)	*	*	PON(0)	DK(1)	XDK(0)	VLCD_TRI(0)	STB(1)	
R1Ch	Power Control 2	W/R	1	*								AP[2:0] (000)	
R1Dh	Power Control 3	W/R	1	*	*							VC1[2:0] (101)	
R1Eh	Power Control 4	W/R	1	*	*	*	*	*	*			VC3[2:0] (000)	
R1Fh	Power Control 5			*	*	*	*	*	*	VRH[3:0] (0100)			
R20h	Power Control 6	W/R	1	*	BT[3:0] (0100)				*	*	*	*	



Register No.	Register	W/R	RS	Upper Code	Lower Code								Comment	
					D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R67h	Himax ID code	R	1	*										
R70h	Internal Use 28	W/R	1	*	*	GS (0)	SS (0)	TEMO DE(0)	TEON (0)	CSEL[2:0] (110)				
R72h	Data control				*	*	DFM[1:0] (00)		*	*		TRI [1:0] (00)		
R90h	Display Control 8	W/R	1	*				SAP[7:0] (0000_1010)						
R91h	Display Control 11	W/R	1	*				GEN_OFF[7:0] (0001_0100)						
R93h	OSC Control 3	W/R	1	*	*	*	*	*		RADJ[3:0] (1111)				
R94h	SAP Idle mode	W/R	1	*			SAP_I[7:0] (0000_0010)							
R95h	DCCLK SYNC TO CL1	W/R	1	*	*	*	*	*	*	*	*	*	DCCL K_SY NC (0)	
R85h	OTP Control 4	R	1	*				OTP_DATA[7:0]						
R57h	Test Mode Control	W/R	1	*	0	0	0	0	0	0	TEST MODE	0		
R5Ch	Source Driver Control1	W/R	1	*	STBA 7	STBA 6	STBA 5	STBA 4	STBA 3	STBA 2	STBA 1	STBA 0		
R96h	Source Driver Control2	W/R	1	*	0	0	0	0	0	0	0	SD_P ULL_GND		

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## 6.2 Index Register

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 6. 1 Index Register

Index register (IR) specifies Index of the register from R00h to RFFh. It sets the register number (ID7-0) in the range from 000000b to 111111b in binary form.

## 6.3 Display Mode Control Register (R01h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	IDMON (0)	INVON (0)	NORON (1)	PTLON (0)
R	1	*	*	*	*	*	*	*	*	*	*	*	*	IDMON (0)	INVON (0)	NORON (1)	PTLON (0)

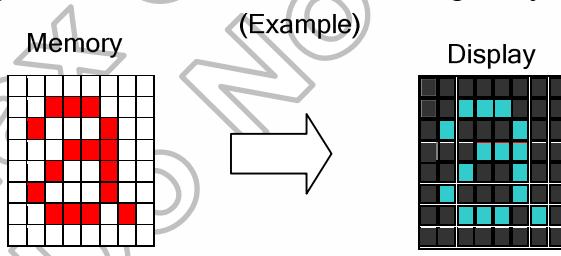
Figure 6. 2 Display Mode Control Register (R01h)

### IDMON:

This command is used for turning on/off IDLE (8-color display) mode by setting IDMON=1/0.

### INVON:

This command is used to enter into display inversion mode by setting INVON=1. Vice versa, it recovers from display inversion mode by setting INVON=0. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status.



### NORON:

This command is used for turning on/off NORMAL mode by setting NORON=1/0.

### PTLON:

This command is used for turning on/off PARTIAL mode by setting PTLON=1/0.

**6.4 Column Address Start Register (R02~03h)**

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC9	SC8
R	1	*	*	*	*	*	*	*	*	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC9	SC8

Figure 6. 3 Column Address Start Register Upper Byte (R02h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
R	1	*	*	*	*	*	*	*	*	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0

Figure 6. 4 Column Address Start Register Low Byte (R03h)

**6.5 Column Address End Register (R04~05h)**

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC9	EC8
R	1	*	*	*	*	*	*	*	*	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC9	EC8

Figure 6. 5 Column Address End Register Upper Byte (R04h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
R	1	*	*	*	*	*	*	*	*	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

Figure 6. 6 Column Address End Register Low Byte (R05h)

**6.6 Row Address Start Register (R06~07h)**

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP9	SP8
R	1	*	*	*	*	*	*	*	*	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP9	SP8

Figure 6. 7 Row Address Start Register Upper Byte (R06h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
R	1	*	*	*	*	*	*	*	*	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

Figure 6. 8 Row Address Start Register Low Byte (R07h)

## 6.7 Row Address End Register (R08~09h)

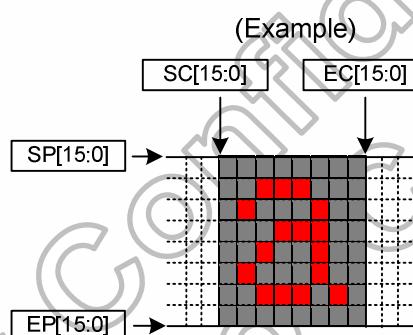
RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP9	EP8
R	1	*	*	*	*	*	*	*	*	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP9	EP8

Figure 6. 9 Row Address End Register Upper Byte (R08h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0
R	1	*	*	*	*	*	*	*	*	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0

Figure 6. 10 Row Address End Register Low Byte (R09h)

These commands (R02h~R09h) are used to define area of frame memory where MCU can access. These commands make no change on the other driver status. The values of SC[15:0], EC[15:0], SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



## 6.8 Partial Area Start Row Register (R0A~0Bh)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PSL 15	PSL 14	PSL 13	PSL 12	PSL 11	PSL 10	PSL 9	PSL 8
R	1	*	*	*	*	*	*	*	*	PSL 15	PSL 14	PSL 13	PSL 12	PSL 11	PSL 10	PSL 9	PSL 8

Figure 6. 11 Partial Area Start Row Register Upper Byte (R0Ah)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PSL 7	PSL 6	PSL 5	PSL 4	PSL 3	PSL 2	PSL 1	PSL 0
R	1	*	*	*	*	*	*	*	*	PSL 7	PSL 6	PSL 5	PSL 4	PSL 3	PSL 2	PSL 1	PSL 0

Figure 6. 12 Partial Area Start Row Register Low Byte (R0Bh)

## 6.9 Partial Area End Row Register (R0C~0Dh)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PEL 15	PEL 14	PEL 13	PEL 12	PEL 11	PEL 10	PEL 9	PEL 8
R	1	*	*	*	*	*	*	*	*	PEL 15	PEL 14	PEL 13	PEL 12	PEL 11	PEL 10	PEL 9	PEL 8

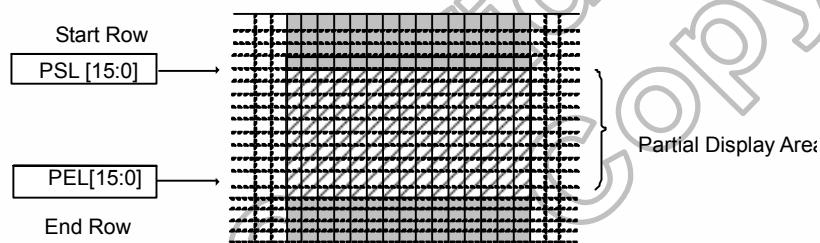
Figure 6. 13 Partial Area End Row Register Upper Byte (R0Ch)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PEL 7	PEL 6	PEL 5	PEL 4	PEL 3	PEL 2	PEL 1	PEL 0
R	1	*	*	*	*	*	*	*	*	PEL 7	PEL 6	PEL 5	PEL 4	PEL 3	PEL 2	PEL 1	PEL 0

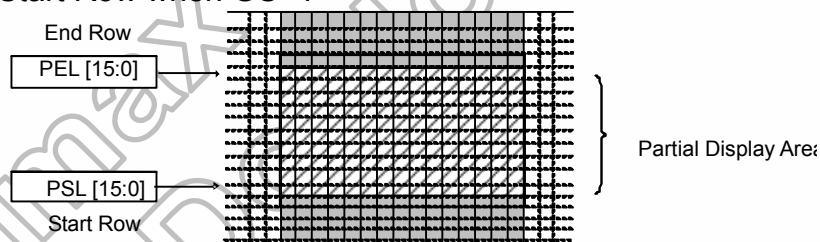
Figure 6. 14 Partial Area End Row Register Low Byte (R0Dh)

These commands (R0Ah~0Dh) define the partial mode's display area. There are 4 parameters associated with this command, PSL[15:0], PEL[15:0], as illustrated in the figures below. PSL and PEL refer to the Frame Memory Line Pointer.

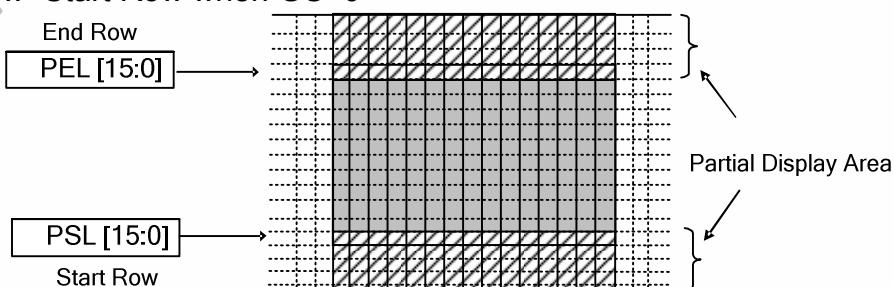
If End Row>Start Row when GS=0



If End Row>Start Row when GS=1



If End Row<Start Row when GS=0



If End Row = Start Row then the Partial Area will be one row deep.

**6.10 Vertical Scroll Top Fixed Area Register (R0E~0Fh)**

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8
R	1	*	*	*	*	*	*	*	*	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8

Figure 6. 15 Vertical Scroll Top Fixed Area Register Upper Byte (R0Eh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0
R	1	*	*	*	*	*	*	*	*	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0

Figure 6. 16 Vertical Scroll Top Fixed Area Register Low Byte (R0Fh)

**6.11 Vertical Scroll Height Area Register (R10~11h)**

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8
R	1	*	*	*	*	*	*	*	*	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8

Figure 6. 17 Vertical Scroll Height Area Register Upper Byte (R10h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0
R	1	*	*	*	*	*	*	*	*	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0

Figure 6. 18 Vertical Scroll Height Area Register Low Byte (R11h)

**6.12 Vertical Scroll Button Fixed Area Register (R12~13h)**

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8
R	1	*	*	*	*	*	*	*	*	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8

Figure 6. 19 Vertical Scroll Button Fixed Area Register Upper Byte (R12h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0
R	1	*	*	*	*	*	*	*	*	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0

Figure 6. 20 Vertical Scroll Button Fixed Area Register Low Byte (R13h)

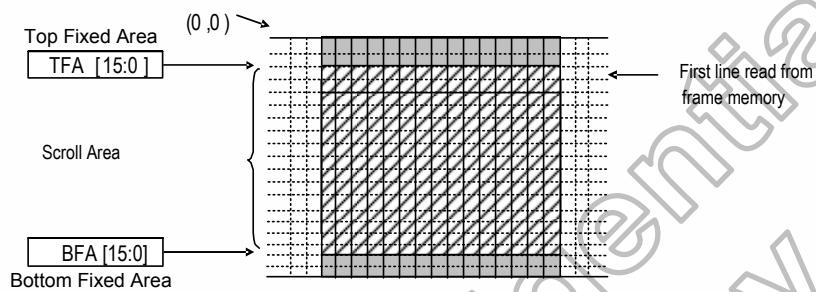
These commands (R0E~0Fh, R10~11h, R12~13h) define the Vertical Scrolling Area of the display. When GS=0,

**TFA[15..0]** describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

**VSA[15..0]** describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

**BFA[15..0]** describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory Line Pointer.

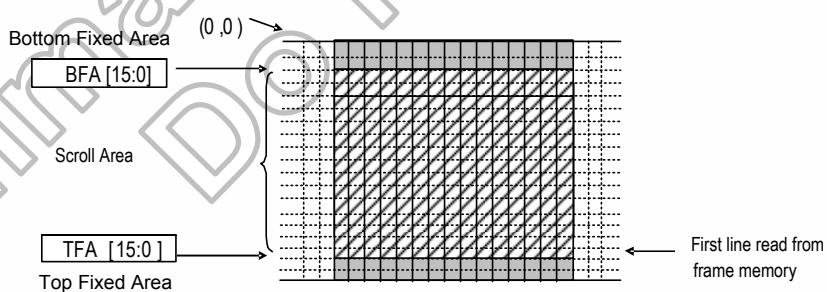


When  $GS=1$ ,

**TFA[15..0]** describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

**VSA[15..0]** describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

**BFA[15..0]** describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



### 6.13 Vertical Scroll Start Address Register (R14~15h)

<b>RW</b>	<b>RS</b>	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
<b>W</b>	<b>1</b>	*	*	*	*	*	*	*	*	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8
<b>R</b>	<b>1</b>	*	*	*	*	*	*	*	*	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8

Figure 6. 21 Vertical Scroll Start Address Register Upper Byte (R14h)

<b>RW</b>	<b>RS</b>	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
<b>W</b>	<b>1</b>	*	*	*	*	*	*	*	*	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0
<b>R</b>	<b>1</b>	*	*	*	*	*	*	*	*	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0

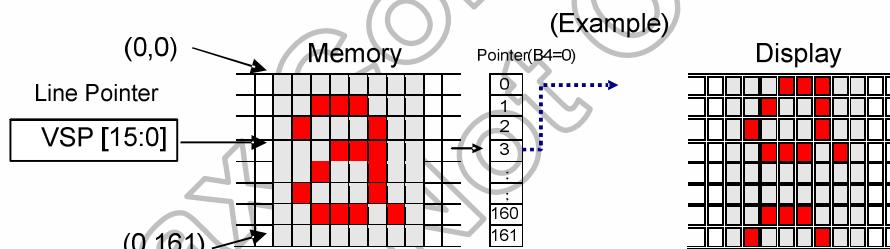
Figure 6. 22 Vertical Scroll Start Address Register Low Byte (R15h)

This command is used together with Vertical Scrolling Definition (18h). These two commands describe the scrolling area and the scrolling mode.

The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below: When GS=0

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and VSP=3



When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

VSP refers to the Frame Memory line Pointer.

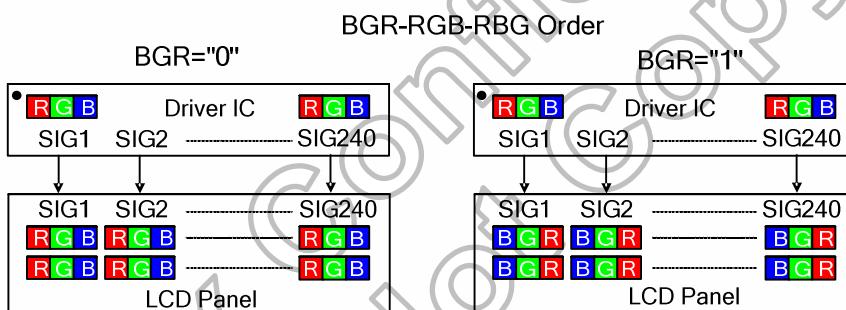
**6.14 Memory Access Control Register (R16h)**

R/W	R S 1	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	MY	MX	MV	*	BGR	*	*	*
R	1	*	*	*	*	*	*	*	*	MY	MX	MV	*	BGR	*	*	*

**Figure 6. 23 Memory Access Control Register (R16h)**

This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status.

Bit	Name	Description
<b>MY</b>	PAGE ADDRESS ORDER	
<b>MX</b>	COLUMN ADDRESS ORDER	These 3 bits controls MCU to memory write/read direction. "MCU to memory write/read direction"
<b>MV</b>	PAGE/COLUMN SELECTION	
<b>BGR</b>	RGB-BGR ORDER	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)



### 6.15 Gate scan Control Register (R18h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	SCROLL_ON	SM(0)
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	SCROLL_ON	SM(0)

Figure 6. 24 Gate Scan Control Register (R18h)

**SCROLL\_ON:** Vertical Scrolling Function enable, High active.

**SM:** Specify the scan order of gate driver. The scan order according to the mounting method of gate driver output pin

### 6.16 OSC Control 1 Register (R19h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	CADJ3	CADJ2	CADJ1	CADJ0	CUADJ2	CUADJ1	CUADJ0	OSC_EN
R	1	*	*	*	*	*	*	*	*	CADJ3	CADJ2	CADJ1	CADJ0	CUADJ2	CUADJ1	CUADJ0	OSC_EN

Figure 6. 25 OSC Control 1 Register (R19h)

This command is used to set internal oscillator related setting

**OSC\_EN:** Enable internal oscillator, High active

**CADJ[3:0], CUADJ[2:0]:** Internal oscillator frequency adjust, default is 5.58MHz

CUADJ2	CUADJ1	CUADJ0	Current
0	0	0	85%
0	0	1	90%
0	1	0	95%
0	1	1	100%
1	0	0	105%
1	0	1	110%
1	1	0	115%
1	1	1	120%

CADJ3	CADJ2	CADJ1	CADJ0	CAP
0	0	0	0	116%
0	0	0	1	114%
0	0	1	0	112%
0	0	1	1	110%
0	1	0	0	108%
0	1	0	1	106%
0	1	1	0	104%
0	1	1	1	102%
1	0	0	0	100%
1	0	0	1	98%
1	0	1	0	96%
1	0	1	1	94%
1	1	0	0	92%
1	1	0	1	90%
1	1	1	0	88%
1	1	1	1	86%

## 6.17 OSC Control Register 2 (R1Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	OSC_TEST
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	OSC_TEST

Figure 6. 26 OSC Control Register 2 (R1Ah)

**OSC\_TEST:** If OSC is fed from OSC pin, please set OSC\_TEST to 1

## 6.18 Power Control 1 Register (R1Bh)

R/W	R S	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	GAS ENB	*	*	PON	DK	XDK	VLCD TRI	STB
R	1	*	*	*	*	*	*	*	*	GAS ENB	*	*	PON	DK	XDK	VLCD TRI	STB

Figure 6. 27 Power Control 1 Register (R1Bh)

**GASENB:** This stands for abnormal power-off supervisal function when the power is off. It's for monitoring power status by NISD pad when GASENB is set to 0.

**PON:** Specify on/off control of step-up circuit 2 for VCL, VGL voltage generation. For detail, see the Power Supply Setting Sequence.

PON	Operation of step-up circuit 2
0	OFF
1	ON

**DK:** Specify on/off control of step-up circuit 1 for DDVDH voltage generation. For detail, see the Power Supply Setting Sequence.

DK	Operation of step-up circuit 1
0	ON
1	OFF

**STB:** When STB = "1", the HX8347-A01 into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. During the standby mode, only the following process can be executed. For details, please refer to STB mode flow.

- Start the oscillation
- Exit the Standby mode (STB = "0") ,

In the standby mode, the GRAM data and register content are retained.

**XDK, VLCD\_TRI:** Specify the ratio of step-up circuit for DDVDH voltage generation.

VLCD_TRI	XDK	Step up circuit 1	Capacitor connection pins
0	0	2 x VCI	C11A, C11B
0	1	2 x VCI	C11A, C11B, CX11A, CX11B
1	0	3 x VCI	C11A, C11B, CX11A, CX11B
1	1	Setting inhibited	Setting inhibited

## 6.19 Power Control 2 Register (R1Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	AP2	AP1	AP0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	AP2	AP1	AP0

Figure 6. 28 Power Control 3 Register (R1Ch)

### AP(2-0)

Adjust the amount of current driving for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff, Adjust the fixed current by considering both the display quality and the current consumption, AP(2-0) can be set as “000” when display is off, the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Power Circuit Off
0	0	1	Ignore
0	1	0	Ignore
0	1	1	Ignore
1	0	0	1
1	0	1	1.25
1	1	0	1.5
1	1	1	Ignore

**6.20 Power Control 3 Register (R1Dh)**

R/W	RS	RB 15	RB 14	RB 13	RB 12	RB 11	RB 10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	VC1 2	VC1 1	VC1 0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	VC1 2	VC1 1	VC1 0

**Figure 6. 29 Power Control 3 Register (R1Dh)****VC1(2-0):**

Specify the ratio of VBGP for DDVDH voltage adjusting.

VC12	VC11	VC10	DDVDH
0	0	0	VBGP * 5.47
0	0	1	VBGP * 5.13
0	1	0	VBGP * 4.82
0	1	1	VBGP * 4.56
1	0	0	VBGP * 4.32
1	0	1	VBGP * 4.10
1	1	0	VBGP * 3.91
1	1	1	VBGP * 3.73

**Note:** 1. VBGP is the internal reference voltage equals to 1.25V  
 2. When VLCD\_TRI=1, DDVDH  $\leq$  (3xVCI - 0.5V)  
 3. When VLCD\_TRI=0, DDVDH  $\leq$  (2xVCI - 0.5V)

**6.21 Power Control 4 Register (R1Eh)**

R/W	RS	RB 15	RB 14	RB 13	RB 12	RB 11	RB 10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	VC3 2	VC3 1	VC30
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	VC3 2	VC3 1	VC3 0

**Figure 6. 30 VREG3 Control Register (R1Eh)****VC3(2-0):**

Specify the reference voltage VREG3 (the factor of VCI) for VGL voltage adjusting

VC32	VC31	VC30	VREG3
0	0	0	DDVDH
0	0	1	2 X VCI
0	1	0	1.92 X VCI
0	1	1	1.84 X VCI
1	0	0	1.76 X VCI
1	0	1	1.68 X VCI
1	1	0	1.60 X VCI
1	1	1	Hz

## 6.22 Power Control 5 Register (R1Fh)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	VRH 3	VRH 2	VRH 1	VRH 0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	VRH 3	VRH 2	VRH 1	VRH 0

Figure 6. 31 Power Control 5 Register (R1Fh)

**VRH(3-0):**

Set the magnification of amplification for VREG1 voltage for gamma voltage setting. It allows magnify the amplification of VBGP from 2.8 to 4.8 times.

VRH3	VRH2	VRH1	VRH0	VREG1
0	0	0	0	VBGPx 2.8
0	0	0	1	VBGPx 3.0
0	0	1	0	VBGPx 3.2
0	0	1	1	VBGPx 3.3
0	1	0	0	VBGPx 3.4
0	1	0	1	VBGPx 3.5
•	•	•	•	•
•	•	•	•	•
1	0	0	1	VBGPx 3.9
1	0	1	0	VBGPx 4.0
1	0	1	1	VBGPx 4.2
1	1	0	0	VBGPx 4.4
1	1	0	1	VBGPx 4.6
1	1	1	0	VBGPx 4.8
1	1	1	1	Inhibited

Note: 1. VBGP is the internal reference voltage equals to 1.25V  
 2. VREG1  $\leq$  (DDVDH – 0.5V).

## 6.23 Power Control 6 Register (R20h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	BT3	BT2	BT1	BT0	*	*	*	*
R	1	*	*	*	*	*	*	*	*	BT3	BT2	BT1	BT0	*	*	*	*

Figure 6. 32 Power Control 6 Register (R20h)

**BT(3-0):**

Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.

BT3	BT2	BT1	BT0	VCL	VGH	VGL		Capacitor Connection Pins
						VCOMG=1	VCOMG=0	
0	0	0	0	-1 x VCI	VREG3X3 [x 6]	-(VREG3X2)+VCL [x -5]	-(VREG3X2) [x -4]	VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B
0	0	0	1	-1 x VCI	VREG3X3 [x 6]	-(VREG3X2) [x -4]	-(VREG3X2) [x -4]	VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B
0	0	1	0	-1 x VCI	VREG3X3 [x 6]	-(VREG3x2)+VCI [x -3]	-(VREG3x2)+VCI [x -3]	VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B
0	0	1	1	-1 x VCI	VREG3X2+VCI [x 5]	-(VREG3X2)+VCL [x -5]	-(VREG3X2) [x -4]	VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B
0	1	0	0	-1 x VCI	VREG3X2+VCI [x 5]	-(VREG3X2) [x -4]	-(VREG3X2) [x -4]	VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B
0	1	0	1	-1 x VCI	VREG3X2+VCI [x 5]	-(VREG3x2)+VCI [x -3]	-(VREG3x2)+VCI [x -3]	VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B
0	1	1	0	-1 x VCI	VREG3X2 [x 4]	-(VREG3X2) [x -4]	-(VREG3X2) [x -4]	VCL, VGH, VGL C12 A/B, C21 A/B, C21A/B
Other setting				Inhibited				

**Note:** 1. The conditions of  $VLCD \leq 6V$ ,  $VCL \leq -3.3V$ ,  $VGH-VGL \leq 32V$  must be satisfied.

2. If  $VCOMG=0$ , VCL output is float.

## 6.24 Power Control 7 Register (R21h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*		FS11	FS10	*		FS01	FS00
R	1	*	*	*	*	*	*	*	*	*		FS11	FS10	*		FS01	FS00

Figure 6. 33 Power Control 7 Register (R21h)

### FS0(1-0):

Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

DCDCf = DC / DC converter operating frequency

FS01	FS0	Operation Frequency of Step-up Circuit 1 and Extra Step-up circuit 1
0	0	DCDCf / 1
0	1	DCDCf / 2
1	0	DCDCf / 4
1	1	DCDCf / 8

### FS1(1-0):

Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL, VCL voltage generation. When using the higher frequency, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. The tradeoff is between the display quality and the current consumption.

DCDCf = DC / DC converter operating frequency

FS11	FS10	Operation Frequency of Step-up Circuit 2 , Step-up Circuit 3
0	0	DCDCf / 1
0	1	DCDCf / 2
1	0	DCDCf / 4
1	1	DCDCf / 8

Note: Ensure that the operation frequency of step-up circuit 1  $\geq$  step-up circuit 2

### 6.25 Read Data Register (R22h)

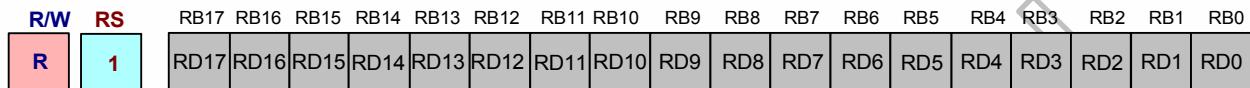


Figure 6. 34 Read Data Register (R22h)

**RD17-0:** Read 18-bit data from GRAM through the read data register (RDR). When the data is read by microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (D17–0) becomes invalid and the second-word read is normal.

### Write Data Register (R22h)

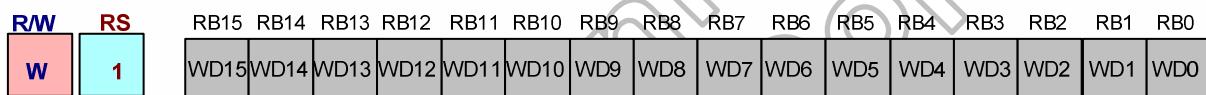


Figure 6. 35 Write Data Register (R22h)

**WD[15:0]** : Transforms the data into 16-bit bus before written to GRAM through the write data register (WDR). After a write operation is issued, the address is automatically updated according to the AM and I/D bits.

## 6.26 Cycle Control 1~3 Register (R23~25h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	N_DC7	N_DC6	N_DC5	N_DC4	N_DC3	N_DC2	N_DC1	N_DC0
R	1	*	*	*	*	*	*	*	*	N_DC7	N_DC6	N_DC5	N_DC4	N_DC3	N_DC2	N_DC1	N_DC0

Figure 6. 36 Cycle Control 1 Register (R23h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	P_DC7	P_DC6	P_DC5	P_DC4	P_DC3	P_DC2	P_DC1	P_DC0
R	1	*	*	*	*	*	*	*	*	P_DC7	P_DC6	P_DC5	P_DC4	P_DC3	P_DC2	P_DC1	P_DC0

Figure 6. 37 Cycle Control 2 Register (R24h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	I_DC7	I_DC6	I_DC5	I_DC4	I_DC3	I_DC2	I_DC1	I_DC0
R	1	*	*	*	*	*	*	*	*	I_DC7	I_DC6	I_DC5	I_DC4	I_DC3	I_DC2	I_DC1	I_DC0

Figure 6. 38 Cycle Control 3 Register (R25h)

**N\_DC:** Normal mode**P\_DC:** Partial mode + Idle mode**I\_DC:** Idle mode**DC(7-0):** specify the clock frequency for DC/DC converter operating.

fosc = R-C oscillation frequency

DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0	DCDCf
0	0	0	0	0	0	0	0	Inhibited
0	0	0	0	0	0	0	1	fosc
0	0	0	0	0	0	1	0	fosc/ 2
•							•	
•							•	
1	1	1	1	1	1	1	0	fosc/ 254
1	1	1	1	1	1	1	1	fosc / 255

Note: It is recommended to set DC(7-0) as "20"h, which means one charge bump clock periodis 32 internal oscillation clocks.

## 6.27 Display Control 1 Register (R26h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	PT1	PT0	GON	DTE	D1	D0	*	*
R	1	*	*	*	*	*	*	*	*	PT1	PT0	GON	DTE	D1	D0	*	*

Figure 6. 39 Display Control 1 Register (R26h)

**D[1:0]:** When D1 = 1, display is on; when D1 = 0, display is off. When display is off, the display data is retained in the GRAM, and can be instantly displayed by setting D1 = 1. When D1= 0, the display is off with the entire source outputs are set to the VSSD level. Because of this, the HX8347-A01 can control the charging current for the LCD with AC driving. When D1-0 = 01, the internal display of the HX8347-A01 is performed although the actual display is off. When D1-0 = 00, the internal display operation halts and the display is off.

### GON, DTE:

GON	DTE	Gate Output
0	X	VGH
1	0	VGL
1	1	VGH/VGL

**PT[1:0] :** Non-display area source output control see follow table

INVON /REV_PANEL		Source Output Level								
		GRAM Data		Display area		Non-display Area				
				PT1-0=(0,*)	PT1-0=(1,0)	PT1-0=(1,1)	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"
0	18'h00000 18'h3FFFF 18'h00000 18'h3FFFF	V63	V0	V63	V0	VSSD	VSSD	Hi-z	Hi-z	
		V0	V63	V63	V0	VSSD	VSSD	Hi-z	Hi-z	
1	18'h00000 18'h3FFFF 18'h00000 18'h3FFFF	V63	V0	V63	V0	VSSD	VSSD	Hi-z	Hi-z	
		V0	V63	V0	V0	VSSD	VSSD	Hi-z	Hi-z	

## 6.28 Display Control 2~7 Register (R27h~R2Ah, R2Ch, R2Dh)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	N_BP3	N_BP2	N_BP1	N_BP0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	N_BP3	N_BP2	N_BP1	N_BP0

Figure 6. 40 Display Control 2 Register (R27h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	N_BP3	N_BP2	N_BP1	N_BP0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	N_BP3	N_BP2	N_BP1	N_BP0

Figure 6. 41 Display Control 3 Register (R28h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	P1_B_P3	P1_B_P2	P1_B_P1	P1_B_P0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	P1_B_P3	P1_B_P2	P1_B_P1	P1_B_P0

Figure 6. 42 Display Control 4 Register (R29h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	P1_F_P3	P1_F_P2	P1_F_P1	P1_F_P0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	P1_F_P3	P1_F_P2	P1_F_P1	P1_F_P0

Figure 6. 43 Display Control 5 Register (R2Ah)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	I_BP3	I_BP2	I_BP1	I_BP0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	I_BP3	I_BP2	I_BP1	I_BP0

Figure 6. 44 Display Control 6 Register (R2Ch)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	I_FP3	I_FP2	I_FP1	I_FP0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	I_FP3	I_FP2	I_FP1	I_FP0

Figure 6. 45 Display Control 7 Register (R2Dh)

**N\_BP, N\_FP:** Back Porch and Front Porch setting in Normal mode

**P1\_BP, P1\_FP:** Back Porch and Front Porch setting in Partial mode + Idle mode

**I\_BP, I\_FP:** Back Porch and Front Porch setting in Idle mode

**FP[3:0]:** Specify the amount of scan line for front porch (FP).

**BP[3:0]:** Specify the amount of scan line for back porch (BP).

FP3	FP2	FP1	FP0	Number of FP Line	Number of BP Line
BP3	BP2	BP1	BP0		
0	0	0	0	Ignore	
0	0	0	1	Ignore	
0	0	1	0	2 lines	
0	0	1	1	4 lines	
0	1	0	0	6 lines	
0	1	0	1	8 lines	
0	1	1	0	10 lines	
0	1	1	1	12 lines	
1	0	0	0	14 lines	
1	0	0	1	16 lines	
1	0	1	0	18 lines	
1	0	1	1	20 lines	
1	1	0	0	22 lines	
1	1	0	1	24 lines	
1	1	1	0	26 lines	
1	1	1	1	Ignore	

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**6.29 Power Control 11 Register (R2Bh)**

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	PI_PRE_REFRES_H1	PI_PRE_REFRES_H0	BLANK_DIV3	BLANK_DIV2	BLANK_DIV1	BLANK_DIV0
R	1	*	*	*	*	*	*	*	*	*	*	PI_PRE_REFRES_H1	PI_PRE_REFRES_H0	BLANK_DIV3	BLANK_DIV2	BLANK_DIV1	BLANK_DIV0

Figure 6. 46 Power Control 11 Register (R2Bh)

**PI\_PRE\_PEFRESH:** Internal used, not open.

**BLANK\_DIV:** Internal used, not open.

**6.30 Display Control 9 Register (R35h)**

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	EQS 7	EQS 6	EQS 5	EQS 4	EQS 3	EQS 2	EQS 1	EQS 0
R	1	*	*	*	*	*	*	*	*	EQS 7	EQS 6	EQS 5	EQS 4	EQS 3	EQS 2	EQS 1	EQS 0

Figure 6. 47 Display Control 9 Register (R35h)

**EQS[7:0]** : Internal used and Not open.

**6.31 Display Control 10 Register (R36h)**

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	EQP 7	EQP 6	EQP 5	EQP 4	EQP 3	EQP 2	EQP 1	EQP 0
R	1	*	*	*	*	*	*	*	*	EQP 7	EQP 6	EQP 5	EQP 4	EQP 3	EQP 2	EQP 1	EQP 0

Figure 6. 48 Display Control 9 Register (R36h)

**EQP[7:0]** : Internal used and Not open.

### 6.32 Display Control 12 Register (R37h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	PTG 1	PTG 0	ISC 3	ISC 2	ISC 1	ISC 0
R	1	*	*	*	*	*	*	*	*	*	*	PTG 1	PTG 0	ISC 3	ISC 2	ISC 1	ISC 0

Figure 6. 49 Display Control 6 Register (R37h)

**PTG[1:0]:** Specify the scan mode of gate driver in non-display area.

PTG1	PTG0	Gate Outputs in Non-display Area
0	0	Normal Drive
0	1	Fixed VGL
1	0	Interval scan
1	1	Ignore

**ISC[3:0] :**Specify the scan cycle of gate driver when PTG1-0=10 in non-display area. Then scan cycle is set to an odd number from 0~31.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f <sub>FLM</sub> = 70Hz
0	0	0	0	0 frame	-
0	0	0	1	3 frames	50 ms
0	0	1	0	5 frames	84 ms
0	0	1	1	7 frames	117 ms
0	1	0	0	9 frames	150 ms
0	1	0	1	11 frames	184 ms
0	1	1	0	13 frames	217 ms
0	1	1	1	15 frames	251 ms
1	0	0	0	17 frames	284 ms
1	0	0	1	19 frames	317 ms
1	0	1	0	21 frames	351 ms
1	0	1	1	23 frames	384 ms
1	1	0	0	25 frames	418 ms
1	1	0	1	27 frames	451 ms
1	1	1	0	29 frames	484 ms
1	1	1	1	31 frames	518 ms

### 6.33 RGB Interface Control 1 Register (R38h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	RGB_EN	DPL	HSPL	VSPL	EPL
R	1	*	*	*	*	*	*	*	*	*	*	*	RGB_EN	DPL	HSPL	VSPL	EPL

Figure 6. 50 RGB Interface Control 1 Register (R38h)

This command is used to set RGB interface related register

**EPL:** Specify the polarity of Enable pin in RGB interface mode. EPL=0, the Enable is High active; EPL=1, the Enable is Low active

**VSPL:** The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.

**HSPL:** The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.

**DPL:** The polarity of DOTCLK pin. When DPL=0, the data is read on the rising edge of DOTCLK signal. When DPL=1, the data is read on the falling edge of DOTCLK signal.

### 6.34 RGB Interface Control 2 Register (R39h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	DOTCL_K_DIV7	DOTCL_K_DIV6	DOTCL_K_DIV5	DOTCL_K_DIV4	DOTCL_K_DIV3	DOTCL_K_DIV2	DOTCL_K_DIV1	DOTCL_K_DIV0
R	1	*	*	*	*	*	*	*	*	DOTCL_K_DIV7	DOTCL_K_DIV6	DOTCL_K_DIV5	DOTCL_K_DIV4	DOTCL_K_DIV3	DOTCL_K_DIV2	DOTCL_K_DIV1	DOTCL_K_DIV0

Figure 6. 51 RGB Interface Control 2 Register (R39h)

**DOTCLK\_DIV[7:0]:** Internal used, not open.

### 6.35 Cycle Control 1~3 Register (R3A~3Ch)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	N_RTNA 3	N_RTNA 2	N_RTNA 1	N_RTNA 0	*	N_NWA 2	N_NWA 1	N_NWA 0
R	1	*	*	*	*	*	*	*	*	N_RTNA 3	N_RTNA 2	N_RTNA 1	N_RTNA 0	*	N_NWA 2	N_NWA 1	N_NWA 0

Figure 6. 52 Cycle Control 1 Register (R3Ah)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	P_L_R TN3	P_L_R TN2	P_L_R TN1	P_L_R TN0	*	P_L_N W2	P_L_N W1	P_L_N W0
R	1	*	*	*	*	*	*	*	*	P_L_R TN3	P_L_R TN2	P_L_R TN1	P_L_R TN0	*	P_L_N W2	P_L_N W1	P_L_N W0

Figure 6. 53 Cycle Control 2 Register (R3Bh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	I_RTNA 3	I_RTNA 2	I_RTNA 1	I_RTNA 0	*	I_NWA 2	I_NWA 1	I_NWA 0
R	1	*	*	*	*	*	*	*	*	I_RTNA 3	I_RTNA 2	I_RTNA 1	I_RTNA 0	*	I_NWA 2	I_NWA 1	I_NWA 0

Figure 6. 54 Cycle Control 3 Register (R3Ch)

The driver IC support individual inversion type and clock per line for Normal display mode, Partial display mode and Idle (8-color) display mode. The resultant NW and RTN will be selected automatically according display mode.

**N\_NW, N\_RTNA:** Normal mode

**P\_L\_NW , P\_L\_RTNA:** Partial mode + Idle mode

**I\_NW, I\_RTNA:** Idle mode

**NW[2:0]:** Frame Inversion and N-line inversion control for normal display mode.

NW[2:0]	Inversion Type
0	Frame inversion
1	1-line inversion
2	2-line inversion
3	3-line inversion
..	..
7	7-line inversion

**RTN[3:0]:** Set the 1-line period in a clock unit for normal display mode.

Clock cycles=1/internal operation clock frequency

RTN[3:0]	Clock Cycles per Line
4'b0000	244
4'b0001	245
4'b0010	246
4'b0011	247
....	....
4'b1110	258
4'b1111	259

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### 6.36 Cycle Control 4 Register (R3Dh)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	DIV_I1	DIV_I0	DIV_PI1	DIV_PI0	DIV 1	DIV 0
R	1	*	*	*	*	*	*	*	*	*	*	DIV_I1	DIV_I0	DIV_PI1	DIV_PI0	DIV 1	DIV 0

Figure 6. 55 Cycle Control 4 Register (R3Dh)

**DIV\_N1-0:** The division ratio of clocks for Normal mode internal operation (DIV\_N1-0). Internal operations are base on the clocks which are frequency divided according to the value of DIV\_N1-0. Frame frequency can be adjusted along with the 1H period (RTN[3:0]). When the drive line count is changed, the frame frequency must be also adjusted.

**DIV\_PI1-0:** The division ratio of clocks for Partial mode + Idle mode internal operation (DIV\_PI1-0). Internal operations are base on the clocks which are frequency divided according to the value of DIV\_PI1-0. Frame frequency can be adjusted along with the 1H period (PI\_RTN[3:0]). When the drive line count is changed, the frame frequency must be also adjusted.

**DIV\_I1-0:** The division ratio of clocks for Idle mode internal operation (DIV\_I1-0). Internal operations are base on the clocks which are frequency divided according to the value of DIV\_I1-0. Frame frequency can be adjusted along with the 1H period (I\_RTN[3:0]). When the drive line count is changed, the frame frequency must be also adjusted.

fosc = R-C oscillation frequency

DIV_N1 / DIV_PI1 / DIV_I1	DIV_N0 / DIV_PI0 / DIV_I0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

#### Formula for the Frame Frequency:

$$\text{Frame frequency} = \text{fosc} / (\text{RTN} \times \text{DIV} \times (\text{NL} + \text{BP} + \text{FP})) \text{ [HZ]}$$

fosc: RC oscillation frequency

NL: 320 lines.

**6.37 Cycle Control 5 Register (R3Eh)**

<b>RW</b>	<b>RS</b>	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
<b>W</b>	<b>1</b>	*	*	*	*	*	*	*	*	SON 7	SON 6	SON 5	SON 4	SON 3	SON 2	SON 1	SON 0
<b>R</b>	<b>1</b>	*	*	*	*	*	*	*	*	SON 7	SON 6	SON 5	SON 4	SON 3	SON 2	SON 1	SON 0

Figure 6. 56 Display Control 5 Register (R3Eh)

**6.38 Cycle Control 6 Register (R40h)**

<b>RW</b>	<b>RS</b>	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
<b>W</b>	<b>1</b>	*	*	*	*	*	*	*	*	GDON 7	GDON 6	GDON 5	GDON 4	GDON 3	GDON 2	GDON 1	GDON 0
<b>R</b>	<b>1</b>	*	*	*	*	*	*	*	*	GDON 7	GDON 6	GDON 5	GDON 4	GDON 3	GDON 2	GDON 1	GDON 0

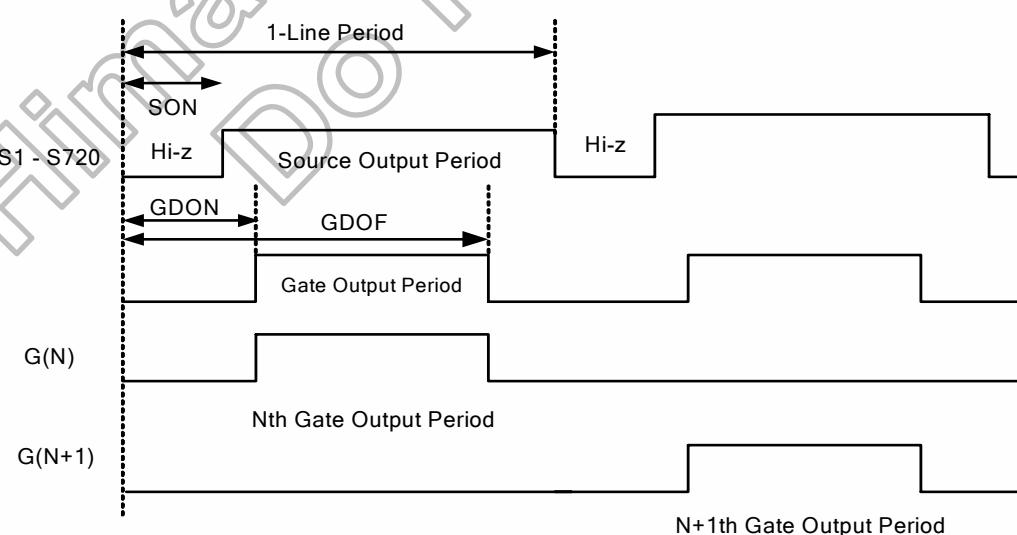
Figure 6. 57 Display Control 6 Register (R40h)

**6.39 Display Control 14 Register (R41h)**

<b>RW</b>	<b>RS</b>	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
<b>W</b>	<b>1</b>	*	*	*	*	*	*	*	*	GDOF 7	GDOF 6	GDOF 5	GDOF 4	GDOF 3	GDOF 2	GDOF 1	GDOF 0
<b>R</b>	<b>1</b>	*	*	*	*	*	*	*	*	GDOF 7	GDOF 6	GDOF 5	GDOF 4	GDOF 3	GDOF 2	GDOF 1	GDOF 0

Figure 6. 58 Display Control 3 Register (R41h)

The HX8347-A01 can control the display operation period time for LCD panel driving as follow:



**SON7-0:** Specify the valid source output start time in 1-line driving period. The period time is defined as SYSCLK clock number. (Please note that the setting “00h” and “01h” is inhibited).

**GDON7-0:** Specify the valid gate output start time in 1-line driving period. The period time is defined as SYSCLK clock number in internal clock display mode. The period time is defined as setting value x 8 DOTCLK clock number in external clock display mode. (Please note that the setting “00h”, “01h”, “02h” is inhibited).

**GDOF7-0:** Specify the gate output end time in 1-line driving period. The period time is defined as SYSCLK clock number in internal clock display mode. The period time is defined as setting value x 8 DOTCLK clock number in external clock display mode. (Please note that the GDOF7-0 ≤ HCK-1).

#### 6.40 BGP Control Register (R42h)

R/W	RS	RB 15	RB 14	RB 13	RB 12	RB 11	RB 10	RB 9	RB 8	RB 7	RB 6	RB 5	RB 4	RB 3	RB 2	RB 1	RB 0
W	1	*	*	*	*	*	*	*	*	*	*	*	VBG_P_OE	BGP3	BGP2	BGP1	BGP0
R	1	*	*	*	*	*	*	*	*	*	*	*	VBG_P_OE	BGP3	BGP2	BGP1	BGP0

Figure 6. 59 BGP Control 1 Register (R42h)

**BGP[3:0]:** band gap voltage control

BGP[3:0]	VBGP Output
4'b0000	X 0.936
4'b0001	X 0.944
4'b0010	X 0.952
4'b0011	X 0.96
4'b0100	X 0.968
4'b0101	X 0.976
4'b0110	X 0.984
4'b0111	X 0.992
<b>4'b1000</b>	<b>X 1.000</b>
4'b1001	X 1.008
4'b1010	X 1.016
4'b1011	X 1.024
4'b1100	X 1.032
4'b1101	X 1.040
4'b1110	X 1.048
4'b1111	X 1.056

**BGP\_OE:** If VBGP\_OE=1, HX8347-A01 outputs the band gap voltage to VBGP pin.

**6.41 Vcom Control 1 Register (R43h)**

R/W	RS	RB 15	RB 14	RB 13	RB 12	RB 11	RB 10	RB 9	RB 8	RB 7	RB 6	RB 5	RB 4	RB 3	RB 2	RB 1	RB 0
W	1	*	*	*	*	*	*	*	*	VCOMG	*	*	*	*	*	*	*
R	1	*	*	*	*	*	*	*	*	VCOMG	*	*	*	*	*	*	*

**Figure 6. 60 Vcom Control 1 Register (R43h)****VCOMG:**

When VCOMG = 1, VCOML voltage can output to negative voltage (1.0V ~ VCL+0.3V). When VCOMG = 0, VCOML outputs VSSA and VDV(4-0) setting are invalid. Then, low power consumption is accomplished.

**6.42 Vcom Control 2 Register (R44h)**

R/W	RS	RB 15	RB 14	RB 13	RB 12	RB 11	RB 10	RB 9	RB 8	RB 7	RB 6	RB 5	RB 4	RB 3	RB 2	RB 1	RB 0
W	1	*	*	*	*	*	*	*	*	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	
R	1	*	*	*	*	*	*	*	*	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	

**Figure 6. 61 Vcom Control 2 Register****VCM(6-0):**

Set the VCOMH voltage (High level voltage of VCOM). It is possible to amplify from 0.4 to 0.98 times of VREG1 voltage.

VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	0	0	0	0	0	VREG1 * 0.4
0	0	0	0	0	0	1	VREG1 * 0.405
0	0	0	0	0	1	0	VREG1 * 0.41
0	0	0	0	0	1	1	VREG1 * 0.415
0	0	0	0	1	0	0	VREG1 * 0.42
0	0	0	0	1	0	1	VREG1 * 0.425
0	0	0	0	1	1	0	VREG1 * 0.43
0	0	0	0	1	1	1	VREG1 * 0.435
0	0	0	1	0	0	0	VREG1 * 0.44
0	0	0	1	0	0	1	VREG1 * 0.445
0	0	0	1	0	1	0	VREG1 * 0.45
0	0	0	1	0	1	1	VREG1 * 0.455
0	0	0	1	1	0	0	VREG1 * 0.46
0	0	0	1	1	0	1	VREG1 * 0.465
0	0	0	1	1	1	0	VREG1 * 0.47
0	0	0	1	1	1	1	VREG1 * 0.475
0	0	1	0	0	0	0	VREG1 * 0.48
0	0	1	0	0	0	1	VREG1 * 0.485
0	0	1	0	0	1	0	VREG1 * 0.49
0	0	1	0	0	1	1	VREG1 * 0.495
0	0	1	0	1	0	0	VREG1 * 0.5
0	0	1	0	1	0	1	VREG1 * 0.505
0	0	1	0	1	1	0	VREG1 * 0.51
0	0	1	0	1	1	1	VREG1 * 0.515
0	0	1	1	0	0	0	VREG1 * 0.52
0	0	1	1	0	0	1	VREG1 * 0.525
0	0	1	1	0	1	0	VREG1 * 0.53
0	0	1	1	0	1	1	VREG1 * 0.535
0	0	1	1	1	0	0	VREG1 * 0.54

VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
0	0	1	1	1	0	1	VREG1 * 0.545
0	0	1	1	1	1	0	VREG1 * 0.55
0	0	1	1	1	1	1	VREG1 * 0.555
0	1	0	0	0	0	0	VREG1 * 0.56
0	1	0	0	0	0	1	VREG1 * 0.565
0	1	0	0	0	1	0	VREG1 * 0.57
0	1	0	0	0	1	1	VREG1 * 0.575
0	1	0	0	1	0	0	VREG1 * 0.58
0	1	0	0	1	0	1	VREG1 * 0.585
0	1	0	0	1	1	0	VREG1 * 0.59
0	1	0	0	1	1	1	VREG1 * 0.595
0	1	0	1	0	0	0	VREG1 * 0.6
0	1	0	1	0	0	1	VREG1 * 0.605
0	1	0	1	0	1	0	VREG1 * 0.61
0	1	0	1	0	1	1	VREG1 * 0.615
0	1	0	1	1	0	0	VREG1 * 0.62
0	1	0	1	1	0	1	VREG1 * 0.625
0	1	0	1	1	1	0	VREG1 * 0.63
0	1	0	1	1	1	1	VREG1 * 0.635
0	1	1	0	0	0	0	VREG1 * 0.64
0	1	1	0	0	0	1	VREG1 * 0.645
0	1	1	0	0	1	0	VREG1 * 0.65
0	1	1	0	0	1	1	VREG1 * 0.655
0	1	1	0	1	0	0	VREG1 * 0.66
0	1	1	0	1	0	1	VREG1 * 0.665
0	1	1	0	1	1	0	VREG1 * 0.67
0	1	1	0	1	1	1	VREG1 * 0.675
0	1	1	1	0	0	0	VREG1 * 0.68
0	1	1	1	0	0	1	VREG1 * 0.685
0	1	1	1	0	1	0	VREG1 * 0.69
0	1	1	1	0	1	1	VREG1 * 0.695
0	1	1	1	1	0	0	VREG1 * 0.7
0	1	1	1	1	0	1	VREG1 * 0.705
0	1	1	1	1	1	0	VREG1 * 0.71
0	1	1	1	1	1	1	VCOMH can be adjusted from VCOMR with a external VR (variable resister),
1	0	0	0	0	0	0	VREG1 * 0.715
1	0	0	0	0	0	1	VREG1 * 0.72
1	0	0	0	0	1	0	VREG1 * 0.725
1	0	0	0	0	1	1	VREG1 * 0.73
1	0	0	0	1	0	0	VREG1 * 0.735
1	0	0	0	1	0	1	VREG1 * 0.74
1	0	0	0	1	1	0	VREG1 * 0.745
1	0	0	0	1	1	1	VREG1 * 0.75
1	0	0	1	0	0	0	VREG1 * 0.755
1	0	0	1	0	0	1	VREG1 * 0.76
1	0	0	1	0	1	0	VREG1 * 0.765
1	0	0	1	0	1	1	VREG1 * 0.77
1	0	0	1	1	0	0	VREG1 * 0.775
1	0	0	1	1	0	1	VREG1 * 0.78
1	0	0	1	1	1	0	VREG1 * 0.785
1	0	0	1	1	1	1	VREG1 * 0.79
1	0	1	0	0	0	0	VREG1 * 0.795
1	0	1	0	0	0	1	VREG1 * 0.8
1	0	1	0	0	1	0	VREG1 * 0.805
1	0	1	0	0	1	1	VREG1 * 0.81
1	0	1	0	1	0	0	VREG1 * 0.815
1	0	1	0	1	0	1	VREG1 * 0.82
1	0	1	0	1	1	0	VREG1 * 0.825
1	0	1	0	1	1	1	VREG1 * 0.83
1	0	1	1	0	0	0	VREG1 * 0.835

VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH
1	0	1	1	0	0	1	VREG1 * 0.84
1	0	1	1	0	1	0	VREG1 * 0.845
1	0	1	1	0	1	1	VREG1 * 0.85
1	0	1	1	1	0	0	VREG1 * 0.855
1	0	1	1	1	0	1	VREG1 * 0.86
1	0	1	1	1	1	0	VREG1 * 0.865
1	0	1	1	1	1	1	VREG1 * 0.87
1	1	0	0	0	0	0	VREG1 * 0.875
1	1	0	0	0	0	1	VREG1 * 0.88
1	1	0	0	0	1	0	VREG1 * 0.885
1	1	0	0	0	1	1	VREG1 * 0.89
1	1	0	0	1	0	0	VREG1 * 0.895
1	1	0	0	1	0	1	VREG1 * 0.9
1	1	0	0	1	1	0	VREG1 * 0.905
1	1	0	0	1	1	1	VREG1 * 0.91
1	1	0	1	0	0	0	VREG1 * 0.915
1	1	0	1	0	0	1	VREG1 * 0.92
1	1	0	1	0	1	0	VREG1 * 0.925
1	1	0	1	0	1	1	VREG1 * 0.93
1	1	0	1	1	0	0	VREG1 * 0.935
1	1	0	1	1	0	1	VREG1 * 0.94
1	1	0	1	1	1	0	VREG1 * 0.945
1	1	0	1	1	1	1	VREG1 * 0.95
1	1	1	0	0	0	0	VREG1 * 0.955
1	1	1	0	0	0	1	VREG1 * 0.96
1	1	1	0	0	1	0	VREG1 * 0.965
1	1	1	0	0	1	1	VREG1 * 0.97
1	1	1	0	1	0	0	VREG1 * 0.975
1	1	1	0	1	0	1	VREG1 * 0.98
1	1	1	0	1	1	0	inhibit
1	1	1	0	1	1	1	inhibit
1	1	1	1	0	0	0	inhibit
1	1	1	1	0	0	1	inhibit
1	1	1	1	0	1	0	inhibit
1	1	1	1	0	1	1	inhibit
1	1	1	1	1	0	0	inhibit
1	1	1	1	1	0	1	inhibit
1	1	1	1	1	1	0	inhibit
1	1	1	1	1	1	1	inhibit
1	1	1	1	1	1	1	VCOMH can be adjusted from VCOMR with a external VR (variable resister)

### 6.43 Vcom Control 3 Register (R45h)

R/W	RS	RB 15	RB 14	RB 13	RB 12	RB 11	RB 10	RB 9	RB 8	RB 7	RB 6	RB 5	RB 4	RB 3	RB 2	RB 1	RB 0
W	1	*	*	*	*	*	*	*	*	*	*	*	VDV4	VDV3	VDV2	VDV1	VDV0
R	1	*	*	*	*	*	*	*	*	*	*	*	VDV4	VDV3	VDV2	VDV1	VDV0

Figure 6. 62 Vcom Control 3 Register (R45h)

#### VDV(4-0):

Specify the VCOM amplitude factors for panel common driving ( $VCOML = VCOMH - VCOM$  amplitude,  $VCOML \geq VCL + 0.3V$ ). It is possible to setup from 0.6 to 1.23 times of VREG1. When  $VCOMG = 0$ , the VDV(4-0) setup is invalid and  $VCOML$  is output VSSA

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM Amplitude
0	0	0	0	0	$VREG1*0.6$
0	0	0	0	1	$VREG1*0.63$
0	0	0	1	0	$VREG1*0.66$
0	0	0	1	1	$VREG1*0.69$
0	0	1	0	0	$VREG1*0.72$
0	0	1	0	1	$VREG1*0.75$
0	0	1	1	0	$VREG1*0.78$
0	0	1	1	1	$VREG1*0.81$
0	1	0	0	0	$VREG1*0.84$
0	1	0	0	1	$VREG1*0.87$
0	1	0	1	0	$VREG1*0.9$
0	1	0	1	1	$VREG1*0.93$
0	1	1	0	0	$VREG1*0.96$
0	1	1	0	1	$VREG1*0.99$
0	1	1	1	0	$VREG1*1.02$
0	1	1	1	1	Inhibit
1	0	0	0	0	$VREG1*1.05$
1	0	0	0	1	$VREG1*1.08$
1	0	0	1	0	$VREG1*1.11$
1	0	0	1	1	$VREG1*1.14$
1	0	1	0	0	$VREG1*1.17$
1	0	1	0	1	$VREG1*1.2$
1	0	1	1	0	$VREG1*1.23$
1	0	1	1	1	Inhibit
1	1	0	0	0	Inhibit
1	1	0	0	1	Inhibit
1	1	0	1	0	Inhibit
1	1	0	1	1	Inhibit
1	1	1	0	0	Inhibit
1	1	1	0	1	Inhibit
1	1	1	1	0	Inhibit
1	1	1	1	1	Inhibit

Note:  $VCOML \geq (VCL + 0.3)$ ,  $VCOMH \leq (DDVDH - 0.3)$  when set VDV[4:0]

**6.44 GAMMA Control 1~12 Register (R46~51h)**

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	GSEL	CP12	CP11	CP10	*	CP02	CP01	CP00
R	1	*	*	*	*	*	*	*	*	GSEL	CP12	CP11	CP10	*	CP02	CP01	CP00

**Figure 6. 63 GAMMA Control 1 Register (R46h)**

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	CN12	CN11	CN10	*	CN02	CN01	CN00	
R	1	*	*	*	*	*	*	*	*	CN12	CN11	CN10	*	CN02	CN01	CN00	

**Figure 6. 64 GAMMA Control 2 Register (R47h)**

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	NP12	NP11	NP10	*	NP02	NP01	NP00	
R	1	*	*	*	*	*	*	*	*	NP12	NP11	NP10	*	NP02	NP01	NP00	

**Figure 6. 65 GAMMA Control 3 Register (R48h)**

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	NP32	NP31	NP30	*	NP22	NP21	NP20	
R	1	*	*	*	*	*	*	*	*	NP32	NP31	NP30	*	NP22	NP21	NP20	

**Figure 6. 66 GAMMA Control 4 Register (R49h)**

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	NP52	NP51	NP50	*	NP42	NP41	NP40	
R	1	*	*	*	*	*	*	*	*	NP52	NP51	NP50	*	NP42	NP41	NP40	

**Figure 6. 67 GAMMA Control 5 Register (R4Ah)**

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	NN12	NN11	NN10	*	NN02	NN01	NN00	
R	1	*	*	*	*	*	*	*	*	NN12	NN11	NN10	*	NN02	NN01	NN00	

**Figure 6. 68 GAMMA Control 6 Register (R4Bh)**

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	NN32	NN31	NN30	*	NN22	NN21	NN20
R	1	*	*	*	*	*	*	*	*	*	NN32	NN31	NN30	*	NN22	NN21	NN20

Figure 6. 69 GAMMA Control 7 Register (R4Ch)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	NN52	NN51	NN50	*	NN52	NN51	NN50
R	1	*	*	*	*	*	*	*	*	*	NN52	NN51	NN50	*	NN52	NN51	NN50

Figure 6. 70 GAMMA Control8 Register (R4Dh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	CGM P11	CGM P10	CGM P01	CGMP 00	OP03	OP02	OP01	OP00
R	1	*	*	*	*	*	*	*	*	CGM P11	CGM P10	CGM P01	CGMP 00	OP03	OP02	OP01	OP00

Figure 6. 71 GAMMA Control 9 Register (R4Eh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	CGM P3	CGM P2	*	OP14	OP13	OP12	OP11	OP10
R	1	*	*	*	*	*	*	*	*	CGM P3	CGM P2	*	OP14	OP13	OP12	OP11	OP10

Figure 6. 72 GAMMA Control 10 Register (R4Fh)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	CGMN 10	CGMN 10	CGMN 01	CGMN 00	ON03	ON02	ON01	ON00
R	1	*	*	*	*	*	*	*	*	CGMN 10	CGMN 10	CGMN 01	CGMN 00	ON03	ON02	ON01	ON00

Figure 6. 73 GAMMA Control 11 Register (R50h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	CGMN N3	CGMN2	*	ON14	ON13	ON12	ON11	ON10
R	1	*	*	*	*	*	*	*	*	CGMN N3	CGMN2	*	ON14	ON13	ON12	ON11	ON10

Figure 6. 74 GAMMA Control 12 Register (R51h)

- CP1-0 [2:0]:** Gamma Center Adjustment registers for positive polarity output  
**CN1-0 [2:0]:** Gamma Center Adjustment registers for negative polarity output  
**NP5-0 [2:0]:** Gamma Macro Adjustment registers for positive polarity output  
**NN5-0 [2:0]:** Gamma Macro Adjustment registers for negative polarity output  
**OP0 [3:0]/OP1 [4:0]:** Gamma Offset Adjustment register for positive polarity output  
**ON0 [3:0]/ON1 [4:0]:** Gamma Offset Adjustment register for negative polarity output  
**CGMP0[1:0], CGMP1[1:0]:** Gamma Tap Adjustment register for positive polarity output  
**CGMN0[1:0], CGMN1[1:0]:** Gamma Tap Adjustment register for negative polarity output

**CGMP2, CGMP3:** Gamma Harmony adjustment register for positive polarity output  
**CGMN2, CGMN3:** Gamma Harmony adjustment register for negative polarity output  
**GSEL:** V0, V256 reference voltage selection. GSEL=1, V0=VgP/N0, V63= VgP/N7; If GSEL=0, V0=VREG1, V63= VGS. For details, please refer to 5.9.4 Gamma register stream and 8 to 1 Selector.

This command is used to set Gamma Curve Related Setting

Register Groups	Positive Polarity	Negative Polarity	Description											
Center Adjustment	CP0 2-0	CN0 2-0	Variable resistor (VRCP/N0) for center adjustment											
	CP1 2-0	CN1 2-0	Variable resistor (VRCP/N1)for center adjustment											
Macro Adjustment	NP0 2-0	NN0 2-0	8-to-1 selector (voltage level of grayscale 1)											
	NP1 2-0	NN1 2-0	8-to-1 selector (voltage level of grayscale 8)											
	NP2 2-0	NN2 2-0	8-to-1 selector (voltage level of grayscale 20)											
	NP3 2-0	NN3 2-0	8-to-1 selector (voltage level of grayscale 43)											
	NP4 2-0	NN4 2-0	8-to-1 selector (voltage level of grayscale 55)											
	NP5 2-0	NN5 2-0	8-to-1 selector (voltage level of grayscale 62)											
Offset Adjustment	OP0 3-0	ON0 3-0	Variable resistor (VROP/N0)for offset adjustment											
	OP1 4-0	ON1 4-0	Variable resistor (VROP/N1)for offset adjustment											

#### 6.45 Internal Use 16 (R64h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
R	1	*	*	*	*	*	*	*	*	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10

Figure 6. 75 Internal Use 16 (R64h)

For internal use and not open.

#### 6.46 Internal Use 17 (R65h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	0	ID26	ID25	ID24	ID23	ID22	ID21	ID20
R	1	*	*	*	*	*	*	*	*	0	ID26	ID25	ID24	ID23	ID22	ID21	ID20

Figure 6. 76 Internal Use 17 (R65h)

For internal use and not open.

### 6.47 Internal Use 18 (R66h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30
R	1	*	*	*	*	*	*	*	*	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30

Figure 6. 77 Internal Use 18 (R66h)

For internal use and not open.

### 6.48 Himax ID code (R67h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	Himax ID7	Himax ID6	Himax ID5	Himax ID4	Himax ID3	Himax ID2	Himax ID1	Himax ID0
R	1	*	*	*	*	*	*	*	*	Himax ID7	Himax ID6	Himax ID5	Himax ID4	Himax ID3	Himax ID2	Himax ID1	Himax ID0

Figure 6. 78 Himax ID code (R67h)

HimaxID[7:0]: The value is 0x47h of HX8347-A01.

### 6.49 Internal Use 28 (R70h)

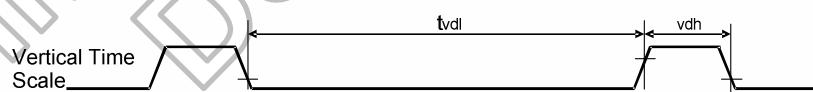
R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	GS	SS	TEMODE	TEON	CSEL 2	CSEL 1	CSEL 0
R	1	*	*	*	*	*	*	*	*	*	GS	SS	TEMODE	TEON	CSEL 2	CSEL 1	CSEL 0

Figure 6. 79 Internal Use 28 (R70h)

**TEMODE:** Specify the Tearing-Effect mode.

When TEMODE=0:

The Tearing Effect Output line consists of V-Blanking information only.



When TEMODE =1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information



**Note:** During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin active low

**TEON:**

This command is used to turn ON the Tearing Effect output signal from the TE signal line.

**CSEL[2:0]:**

This command is used to define the format of RGB picture data, which is to be transferred via the RGB Interface. The formats are shown in the table:

Interface Format	CSEL2	CSEL1	CSEL0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0

**SS:** The source driver output shift direction selected. When SS=0, the shift direction from S1 to S720. When SS = 1, the shift direction from S720 to S1.

**GS:** The gate driver output shift direction selected. When GS=0, the shift direction from G1 to G320. When GS = 1, the shift direction from G320 to G1.

**6.50 Data control register (R72h)**

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	DFM1	DFMO	*	*	TRI1	TRI0
R	1	*	*	*	*	*	*	*	*	*	*	DFM1	DFMO	*	*	TRI1	TRI0

Figure 6. 80 Serial Bus Interface Control Register (R72h)

TRI[1:0]	GRAM
00	16 bit-color/per pixel data
01	18 bit-color/per pixel data
1X	18 bit-color/per pixel data

For details, please refer to serial bus system interface.

**6.51 Display Control 8 (R90h)**

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*		SAP[7:0]					
R	1	*	*	*	*	*	*	*	*	*		SAP[7:0]					

Figure 6. 81 Display Control 8 (R90h)

**SAP [7:0]:** Adjust the amount of fixed current from the fixed current source for the source driver operational amplifier in the Normal display .

**6.52 Display Control 11 (R91h)**

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*		GEN_OFF[7:0]					
R	1	*	*	*	*	*	*	*	*	*		GEN_OFF[7:0]					

Figure 6. 82 Display Control 11 (R91h)

For internal use and not open.

**6.53 OSC Control 3 (R93h)**

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	RADJ 3	RADJ 2	RADJ 1	RADJ 0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	RADJ 3	RADJ 2	RADJ 1	RADJ 0

**Figure 6. 83 OSC Control 3 (R93h)**

**RADJ[4:0]:** Internal oscillator frequency adjust, default is 5.58MHz.

RADJ3	RADJ2	RADJ1	RADJ0	Internal Oscillator Frequency
0	0	0	0	175%
0	0	0	1	170%
0	0	1	0	165%
0	0	1	1	160%
0	1	0	0	155%
0	1	0	1	150%
0	1	1	0	145%
0	1	1	1	140%
1	0	0	0	135%
1	0	0	1	130%
1	0	1	0	125%
1	0	1	1	120%
1	1	0	0	115%
1	1	0	1	110%
1	1	1	0	105%
1	1	1	1	100%

### 6.54 SAP Idle Mode (R94h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*								SAP_I[7:0]
R	1	*	*	*	*	*	*	*	*								SAP_I[7:0]

Figure 6. 84 SAP Idle Mode (R94h)

**SAP\_I[7:0]:** Adjust the amount of fixed current from the fixed current source for the source driver operational amplifier in the Idle display mode.

### 6.55 DCCLK SYNC TO CL1 (R95h)

R/W	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	DCCL_K_SY_NC
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	DCCL_K_SY_NC

Figure 6. 85 DCCLK SYNC TO CL1 (R95h)

For internal use and not open.

### 6.56 OTP Related register 1 (R52h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	OTP_MASK_7	OTP_MASK_6	OTP_MASK_5	OTP_MASK_4	OTP_MASK_3	OTP_MASK_2	OTP_MASK_1	OTP_MASK_0
R	1	*	*	*	*	*	*	*	*	OTP_MASK_7	OTP_MASK_6	OTP_MASK_5	OTP_MASK_4	OTP_MASK_3	OTP_MASK_2	OTP_MASK_1	OTP_MASK_0

Figure 6. 86 OTP Related Register 1 (R52h)

**OTP\_MASK7 [7:0]:** Bit programming mask, if set to 1, it means that it doesn't program this bit

### 6.57 OTP Related register 2 (R53h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	OTP_J_NDEX_7	OTP_J_NDEX_6	OTP_J_NDEX_5	OTP_J_NDEX_4	OTP_J_NDEX_3	OTP_J_NDEX_2	OTP_J_NDEX_1	OTP_J_NDEX_0
R	1	*	*	*	*	*	*	*	*	OTP_J_NDEX_7	OTP_J_NDEX_6	OTP_J_NDEX_5	OTP_J_NDEX_4	OTP_J_NDEX_3	OTP_J_NDEX_2	OTP_J_NDEX_1	OTP_J_NDEX_0

Figure 6. 87 OTP Related Register 2 (R53h)

**OTP\_INDEX[7:0]:** Set location of OTP programming.

### 6.58 OTP Related register 3 (R54h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	OTP_L LOADABLE	DCCL K_DISABLE	OTP_POR	OTP_PWE	OTP_PTM	*	VPP_SEL	OTP_PROG
R	1	*	*	*	*	*	*	*	*	OTP_L LOADABLE	DCCL K_DISABLE	OTP_POR	OTP_PWE	OTP_PTM	*	VPP_SEL	OTP_PROG

Figure 6. 88 OTP Related Register 3 (R54h)

**OTP\_LOAD\_DISABLE:** Normally the internal registers are auto-loaded from OTP. The bit must set “1” in OTP programming.

**DCCLK\_DISABLE:** When written to 1, disable internal pumping Clock.

**OTP\_POR:** OTP read control bit.

**OTP\_PWE:** Internal use, please set to “0”.

**OTP\_PTM:** Internal use, please set to “0”.

**VPP\_SEL:** OTP powers select and please set to “0”. The bit will automatic setting.

**OTP\_PROG:** When it set to 1, the internal register begin to write to OTP.

### 6.59 OTP Related register 4 (R85h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	OTP_D ATA7	OTP_D ATA6	OTP_D ATA5	OTP_D ATA4	OTP_D ATA3	OTP_D ATA2	OTP_D ATA1	OTP_D ATA0
R	1	*	*	*	*	*	*	*	*	OTP_D ATA7	OTP_D ATA6	OTP_D ATA5	OTP_D ATA4	OTP_D ATA3	OTP_D ATA2	OTP_D ATA1	OTP_D ATA0

Figure 6. 89 OTP Related Register 4 (R85h)

**OTP\_DATA:** OTP data for OTP read.

## 6.60 TEST MODE Control (R57h)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	TEST_MODE	0
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	TEST_MODE	0

Figure 6. 89 TEST MODE Control (R57h)

**TEST\_MODE:** TEST mode Enable/Disable. The bit must set to “0” in normal use.

1: Enable.

0: Disable.

## 6.61 Source Driver Control 1 (R5Ch)

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	STBA 7	STBA 6	STBA 5	STBA 4	STBA 3	STBA 2	STBA 1	STBA 0
R	1	*	*	*	*	*	*	*	*	STBA 7	STBA 6	STBA 5	STBA 4	STBA 3	STBA 2	STBA 1	STBA 0

Figure 6. 90 Source Driver Control 1 (R5Ch)

STBA[1:0] : Please set 01, IC internal test mode

STBA[7:5] : Please set 100, IC internal test mode

STBA[4:2] : Gamma Bias Current, adjust internal gamma bias current, larger number , larger current

STBA[4:2]	Setting
000	Level 0
001	Level 1
010	Level 2
011	Level 3
100	Level 4
101	Level 5
110	Level 6
111	Level 7

**6.62 TEST MODE Control (R96h)**

RW	RS	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	SD_P ULL_GND
R	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	SD_P ULL_GND

Figure 6. 91 Source Driver Control 2 (R96h)

**SD\_PULL\_GND:** It is select S1~S720 states in STB mode.

1: Pull to GND.

0: floating.

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## 7. Electrical Characteristic

### 7.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage 1	IOVCC	-0.3 ~ +4.0	V
Supply Voltage 2	VCI	-0.3 ~ +4.0	V
Supply Voltage 3	DDVDH	-0.3 ~ +9	V
Supply Voltage 4	VCL	-4.0 ~ +0.3	V
Supply Voltage 5	VGH	-0.3 ~ +18.5	V
Supply Voltage 6	VGL	-18.5 ~ +0.3	V
Input Voltage Range	VIN	-0.3 ~ VCI+0.3	V
Operating Temperature Range	TOPR	-40 ~ +85	°C
Storage Temperature Range	TSTG	-55 ~ +110	°C

### 7.2 ESD Protection Level

Mode	Test Condition	Protection Level	Unit
Human Body Model	C = 100 pF, R = 1.5 kΩ	±2.0K	V
Machine Model	C = 200 pF, R = 0.0 Ω	±200	V

Table 7. 1

### 7.3 Latch-Up Protection Level

TBD

### 7.4 Light Sensitivity

TBD

**7.5 Maximum Series Resistance**

Name	Type	Maximum Series Resistance	Unit
IOVCC	Power supply	10	Ω
VCI	Power supply	10	Ω
VSSA	Power supply	10	Ω
VSSD	Power supply	10	Ω
OSC	Input	100	Ω
P68, BS[2:0], EXTC, IFSEL0, BURN, REGVDD,	Input	100	Ω
NRD_E, NWR_RNW, DNC_SCL, NCS, SDI	Input	100	Ω
NRESET	Input	100	Ω
D[17:0], DOTCLK, ENABLE, VSYNC, HSYNC	Input	100	Ω
VGH	Capacitor connection	10	Ω
VGL	Capacitor connection	10	Ω
VCL	Capacitor connection	10	Ω
DDVDH	Capacitor connection	10	Ω
VDDD	Capacitor connection	10	Ω
VREG1	Capacitor connection	30	Ω
VREG3	Capacitor connection	20	Ω
VCOMH, VCOML	Capacitor connection	20	Ω
C11A, C11B, CX11A, CX11B	Capacitor connection	10	Ω
C12A, C12B	Capacitor connection	10	Ω
C21A, C21B	Capacitor connection	15	Ω
C22A, C22B	Capacitor connection	15	Ω
VCOMR	Input	100	Ω
VGS	Input	30	Ω
TEST[3:1]	Input	100	Ω
VBGP, SDO	Output	100	Ω

Table 7. 2

## 7.6 DC Characteristics

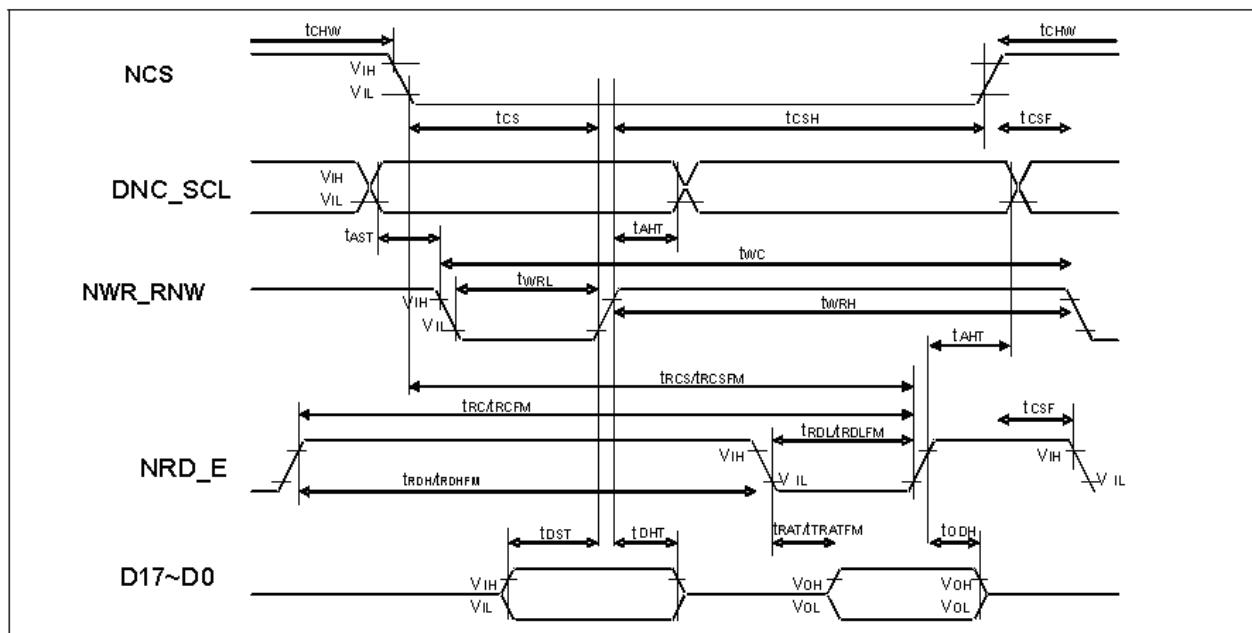
(Vci = 2.4 ~ 3.3V, IOVcc = 1.65~3.3V, Ta = -40 ~ 85 °C)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V <sub>IH</sub>	V	IOVcc= 1.65 ~ 3.3V	0.7xIOVcc	-	IOVcc	-
Input low voltage	V <sub>IL</sub>	V	IOVcc= 1.65 ~ 3.3V	-0.3V	-	0.3xIOVcc	-
Output high voltage ( D0-17 Pins )	V <sub>OH1</sub>	V	I <sub>OH</sub> = -0.1 mA	0.8xIOVcc	-	-	-
Output low voltage ( D0-17 Pins )	V <sub>OL1</sub>	V	IOVcc= 1.65 ~ 3.3V I <sub>OL</sub> = 0.1mA	-	-	0.2xIOVcc	-
I/O leakage current	I <sub>Li</sub>	μA	Vin = 0 ~ Vcc	-1	-	1	-
Current consumption during normal operation (IOVcc-VSSD)	I <sub>OP(IOVcc)</sub>	μA	Vci =2.8V ,IOVcc=2.8V Ta=25°C , GRAM data = 0000h, Frame rate = 70Hz, REV=0, SAP=01111111, AP=100, FS0=00, FS1=11, BT=0100, VC1=111, VC3=000 VRH=0100, VCM=0100000,VDV=01110, VCOMG=1 No panel load	-	400	600	-
Current consumption during normal operation ( Vci – VSSD )	I <sub>OP(Vci)</sub>	mA	Vci =2.8V ,IOVcc=2.8V Ta=25°C , GRAM data = 0000h, Frame rate = 70Hz, REV=0, SAP=01111111, AP=100, FS0=00, FS1=11, BT=0100, VC1=111, VC3=000 VRH=0100, VCM=0100000,VDV=01110, VCOMG=1 No panel load	-	2.7	3.0	-
Current consumption during standby mode (IOVcc-VSSD)	I <sub>ST(IOVcc)</sub>	μA	IOVcc=2.8V , Ta=25°C	-	5	20	-
Current consumption during standby mode ( Vci – VSSD )	I <sub>ST(Vci)</sub>	μA	Vcc=2.8V , Ta=25°C (SD_PULL_GND=0)	-	0.5	1	
			Vcc=2.8V , Ta=25°C (SD_PULL_GND=1)	-		50	
Output voltage deviation	-	mV	-	-	5	-	-
Dispersion of the Average Output Voltage	V	mV	-	-	-	35	-

Table 7. 3 DC Characteristic

## 7.7 AC CHARACTERISTICS

### 7.7.1 Parallel Interface Characteristics (8080-series MPU)



**Figure 7. 1 Parallel Interface Characteristics (8080-series MPU)**

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, Ta = -40 to 85° C)

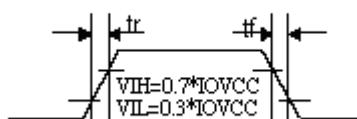
Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DNC_SCL	tAST tAHT	Address setup time Address hold time (Write/Read)	10 10	- -	ns	-
NCS	tCHW tcs trCSFM tCSF tCSH	Chip select "H" pulse width Chip select setup time (Write) Chip select setup time Chip select wait time (Write/Read) Chip select hold time	0 35 180 10 10	- - - - -	ns	-
NWR_RNW	tWC tWRH tWRRL	Write cycle Control pulse "H" duration Control pulse "L" duration	100 15 20	- - -	ns	-
NRD_E	trCFM trDHFM trDLFM	Read cycle Control pulse "H" duration Control pulse "L" duration	250 15 180	- - -	ns	When read from GRAM
D17 to D0	tDST tDHT tRAT trAFM todH	Data setup time Data hold time Read access time (ID) Read access time (FM) Output disable time	10 10 - - 20	- - 180 340 80	ns	For maximum CL=30pF For minimum CL=8pF

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

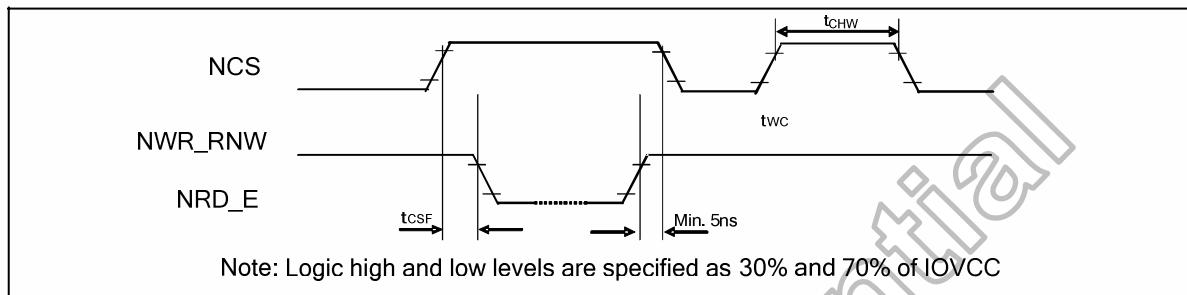
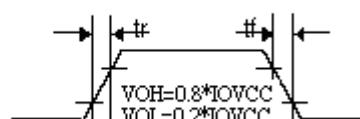
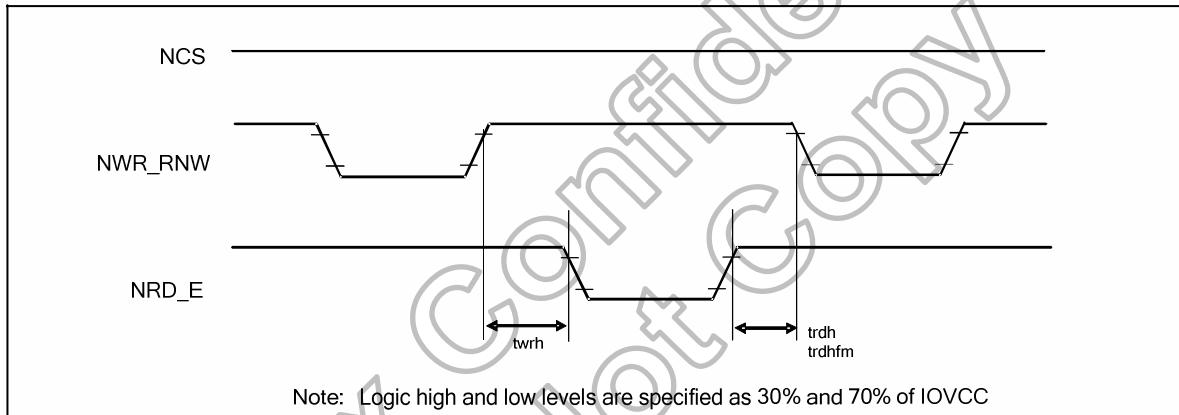
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

**Table 7. 4 AC Characteristic of 8080-series Interface**

Input Signal Slope



Output Signal Slope

**Figure 7. 2 Chip Select Timing****Figure 7. 3 Write to Read and Read to Write Timing**

### 7.7.2 Parallel Interface Characteristics (6800-series MPU)

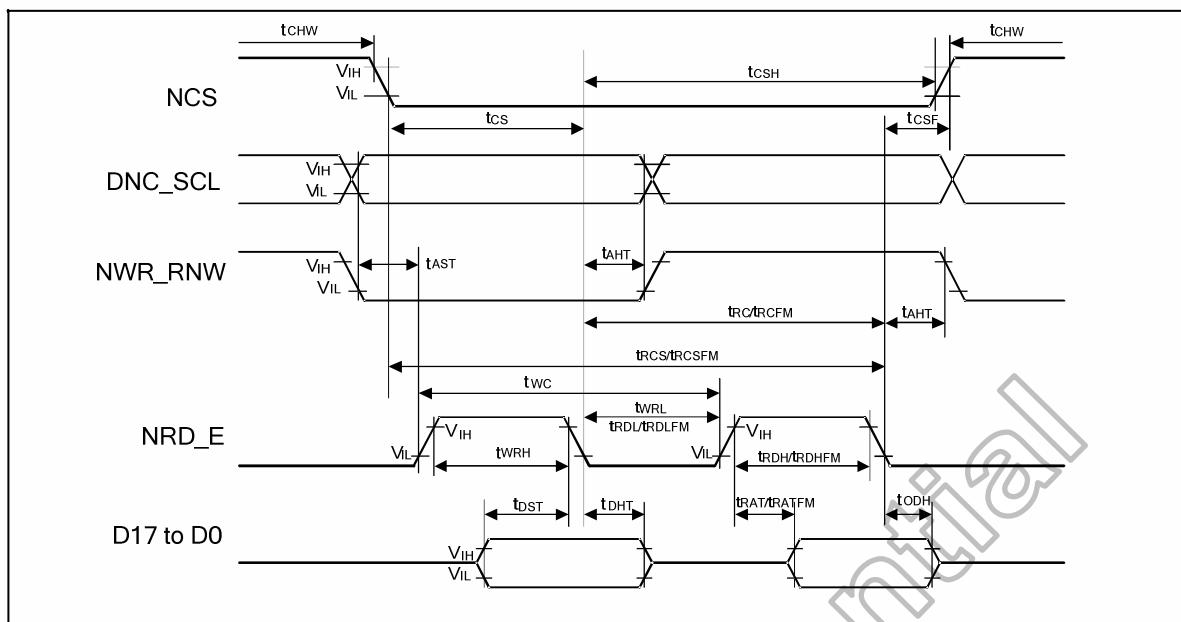


Figure 7. 4 Parallel Interface Characteristics (6800-series MPU)

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, Ta = -40 to 85° C)

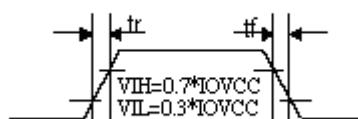
Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DNC_SCL	tAST	Address setup time	10	-	-	-
	taHT	Address hold time (Write/Read)	10	-	ns	
NCS	tCHW	Chip select "H" pulse width	0	-	-	-
	tcs	Chip select setup time (Write)	35	-	-	
	trCSFM	Chip select setup time	150	-	ns	
	tCSF	Chip select wait time (Write/Read)	10	-	-	
	tCSH	Chip select hold time	10	-	-	
NWR_RNW	tWC	Write cycle	100	-	-	-
	tWRH	Control pulse "H" duration	35	-	ns	
	tWRLL	Control pulse "L" duration	35	-	-	
NRD_E	trCFM	Read cycle	450	-	-	When read from GRAM
	trDHFM	Control pulse "H" duration	90	-	ns	
	trDLFM	Control pulse "L" duration	355	-	-	
D17 to D0	T <sub>dst</sub>	Data setup time	10	-	-	For maximum C <sub>L</sub> =30pF For minimum C <sub>L</sub> =8pF
	tDHT	Data hold time	10	-	-	
	tRAT	Read access time (ID)	-	180	ns	
	trATFM	Read access time (FM)	-	340	-	
	tODH	Output disable time	20	80	-	

Table 7. 5 AC Characteristic of 6800-series Interface

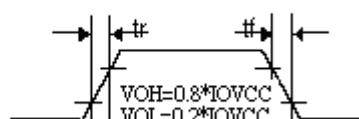
Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

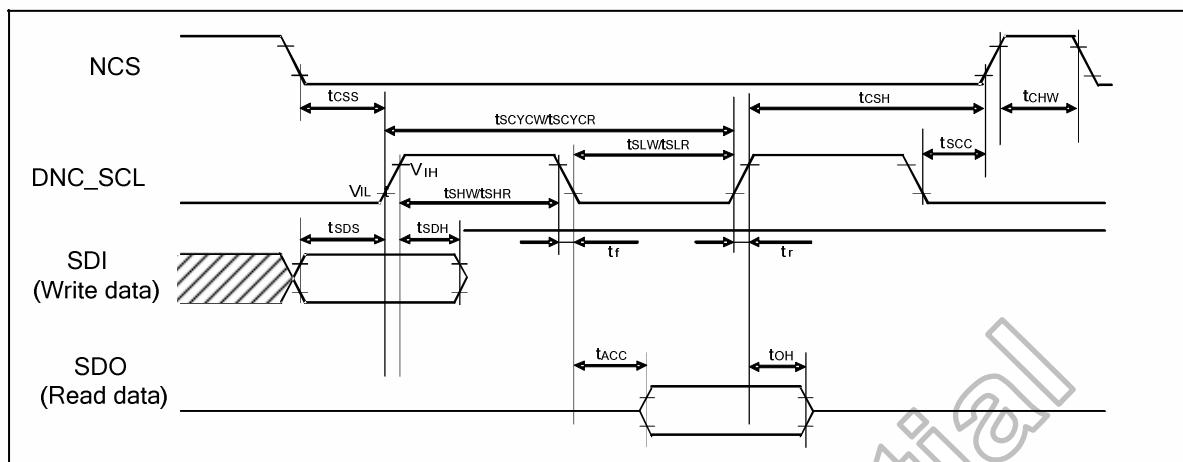
Input Signal Slope



Output Signal Slope



### 7.7.3 Serial Interface Characteristics



**Figure 7. 5 Serial Interface Characteristics**

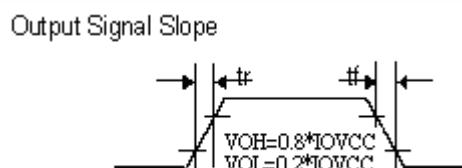
(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, Ta = -40 to 85° C)

Parameter	Symbol	Conditions	Min.	Typ.	Maz.	Unit
Serial clock cycle (Write)	tscycw		100	-	-	
DNC_SCL "H" pulse width (Write)	tshw	DNC_SCL	35	-	-	ns
DNC_SCL "L" pulse width (Write)	tslw		35	-	-	
Data setup time (Write)	tsds		30	-	-	ns
Data hold time (Write)	tsdh	SDI	30	-	-	ns
Serial clock cycle (Read)	tscycr		150	-	-	
DNC_SCL "H" pulse width (Read)	tshr	DNC_SCL	60	-	-	ns
DNC_SCL "L" pulse width (Read)	tslr		100	-	-	
Access Time	tacc	SDO for maximum CL=30pF For minimum CL=8pF	10	-	100	ns
Output disable time	toh	SDO For maximum CL=30pF For minimum CL=8pF	15	-	100	ns
DNC_SCL to Chip select	tscc	DNC_SCL, NCS	50	-	-	ns
NCS "H" pulse width	tchw	NCS	45	-	-	ns
Chip select setup time	tcss	NCS	60	-	-	ns
Chip select hold time	tcsf	NCS	80	-	-	ns

**Table 7. 6 AC Characteristic of SPI Interface**

**Note:** The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.



### 7.7.4 RGB Interface Characteristics

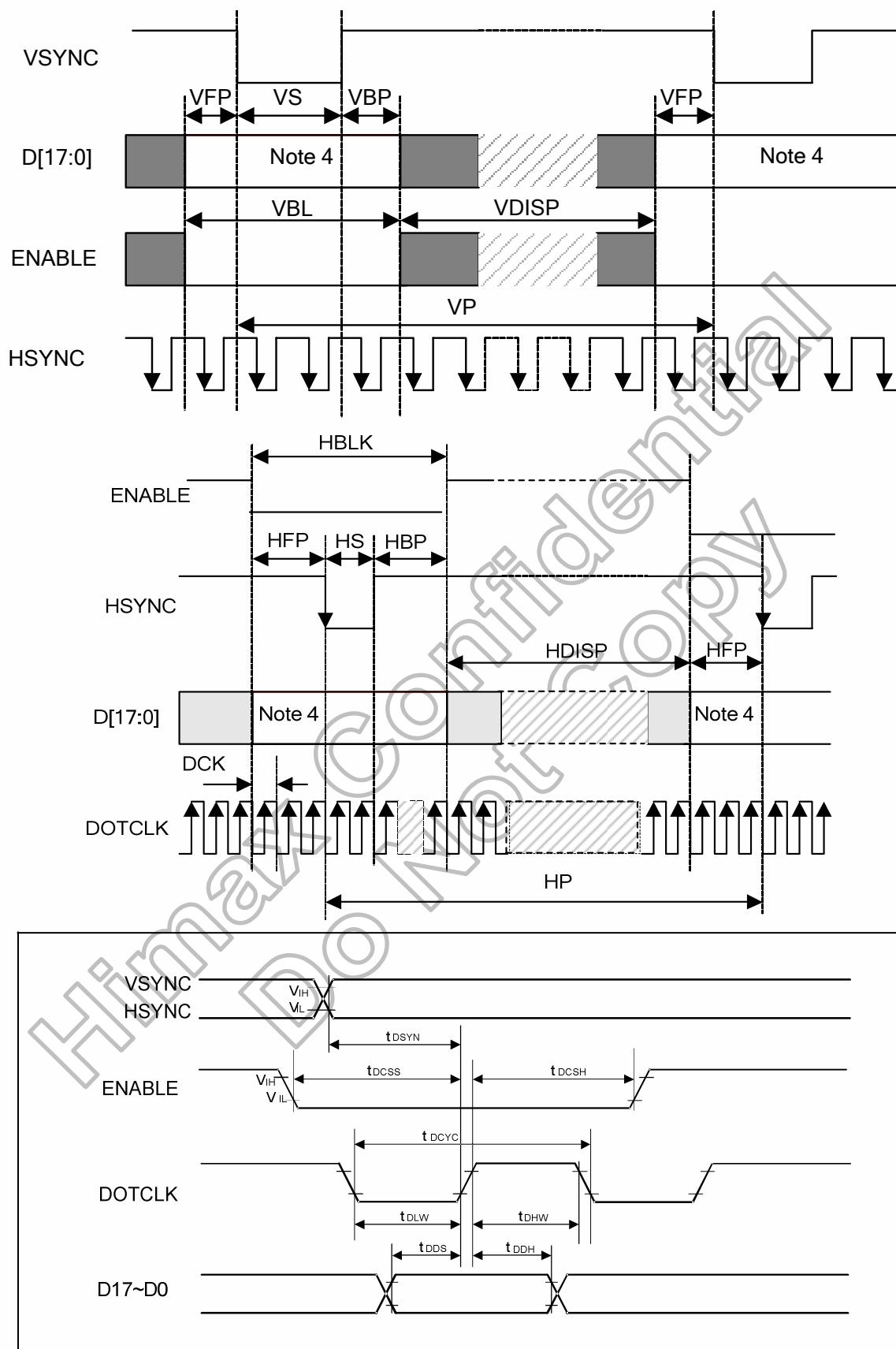


Figure 7. 6 RGB Interface Characteristics

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, Ta = -40 to 85° C)

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-P.127-  
April, 2008

Symbol	Parameter	Conditions	Related Pins	Min.	Typ.	Max.	Unit
VS	VSYNC Low Pulse Width	-	VSYNC	1	-	-	Line
VBP	Vertical Back Porch	-	VSYNC	1	-	-	Line
VFP	Vertical Front Porch	-	VSYNC	1	-	-	Line
VDISP	Vertical Active Area	-	VSYNC, HSYNC	-	320	-	Line
HS	HSYNC Low Pulse Width	-	HSYNC	2	-	-	DOTCLK
HBP	Horizontal Back Porch	-	HSYNC	2	-	-	DOTCLK
HFP	Horizontal Front Porch	-	HSYNC	2	-	-	DOTCLK
HDISP	Horizontal Active Area	-	HSYNC, DOTCLK	-	240	-	DOTCLK
t <sub>DCYC</sub>	DOTCLK cycle time	VRR = Min . 50 Hz Max. 65 Hz	DOTCLK	100 (note2)		226 (note3)	ns
t <sub>DLOW</sub> t <sub>DHIGH</sub>	DOTCLK Low time DOTCLK High time	-		50 15	-	-	ns
t <sub>DDS</sub> t <sub>DHH</sub>	RGB Data setup time RGB Data hold time	-	DOTCLK, D17-D0	15 15	-	-	ns
t <sub>DSS</sub> t <sub>DCHS</sub>	ENABLE setup time ENABLE hold Time	-	ENABLE	15 15	-	-	ns
t <sub>DSYN</sub>	SYNC setup time	-	DOTCLK, HSYNC, VSYNC	15	-	-	ns

Table 7. 7 AC Characteristic of RGB Interface

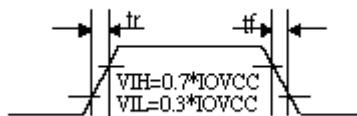
Note: (1) The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

(2) 16.6 MHz

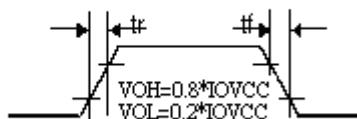
(3) 4.4MHz

(4) Data line can be set to "H" or "L" during blanking time – Don't care.

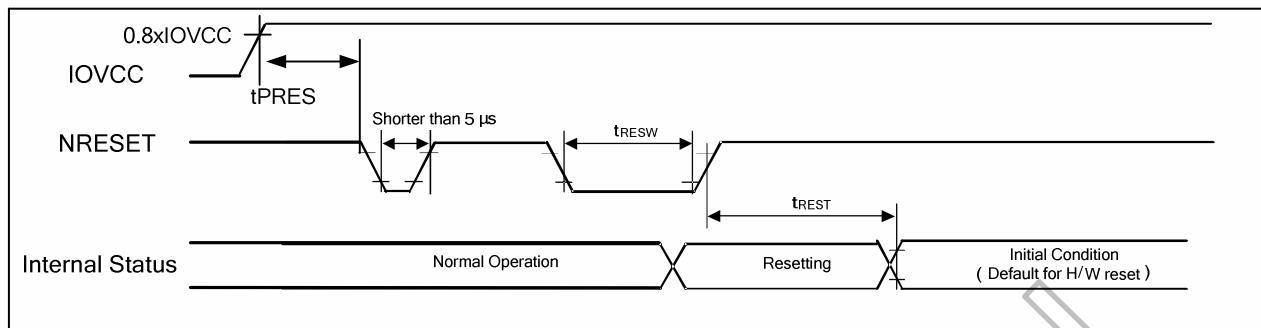
Input Signal Slope



Output Signal Slope



### 7.7.5 Reset Input Timing



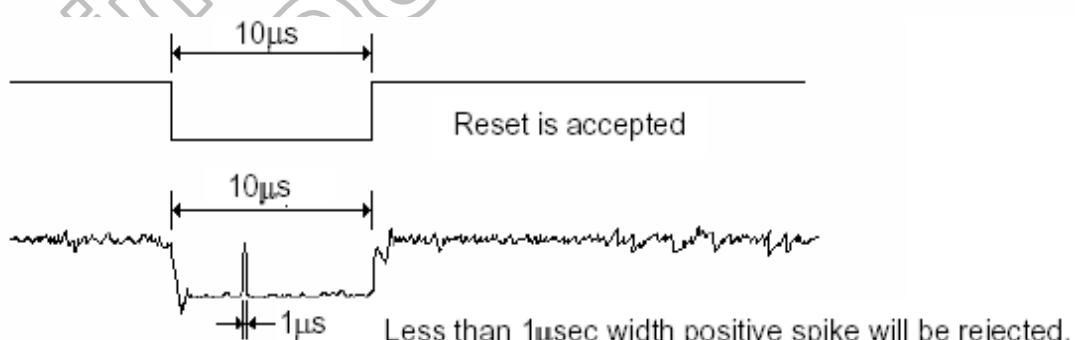
**Figure 7.7 Reset input timing**

Symbol	Parameter	Related Pins	Min.	Typ.	Max.	Note	Unit
tRESW	Reset low pulse width <sup>(1)</sup>	NRESET	10	-	-	-	μs
tREST	Reset complete time <sup>(2)</sup>	-	-	-	5	When reset applied during STB mode	ms
		-	-	-	120	When reset applied during STB mode	ms
tPRES	Reset goes high level after Power on time	NRESET & IOVCC	1	-	-	Reset goes high level after Power on	ms

**Note:** (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below.

NRESET Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

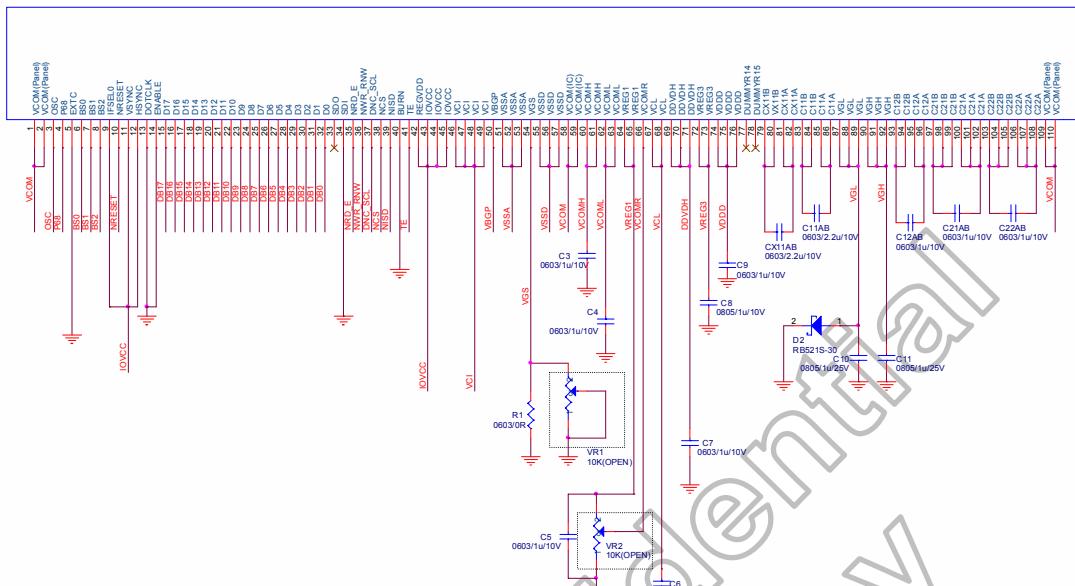
- (2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in STB Out –mode. The display remains the blank state in STB –mode) and then return to Default condition for H/W reset.
- (3) During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.
- (4) Spike Rejection also applies during a valid reset pulse as shown below:



- (5) It is necessary to wait 5msec after releasing !RES before sending commands. Also STB Out command cannot be sent for 120msec.

## 8. Reference Applications

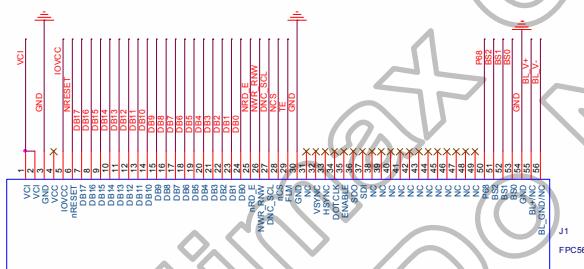
### 8.1 Parallel Interface of Register-Content Mode (For CMO Panel)



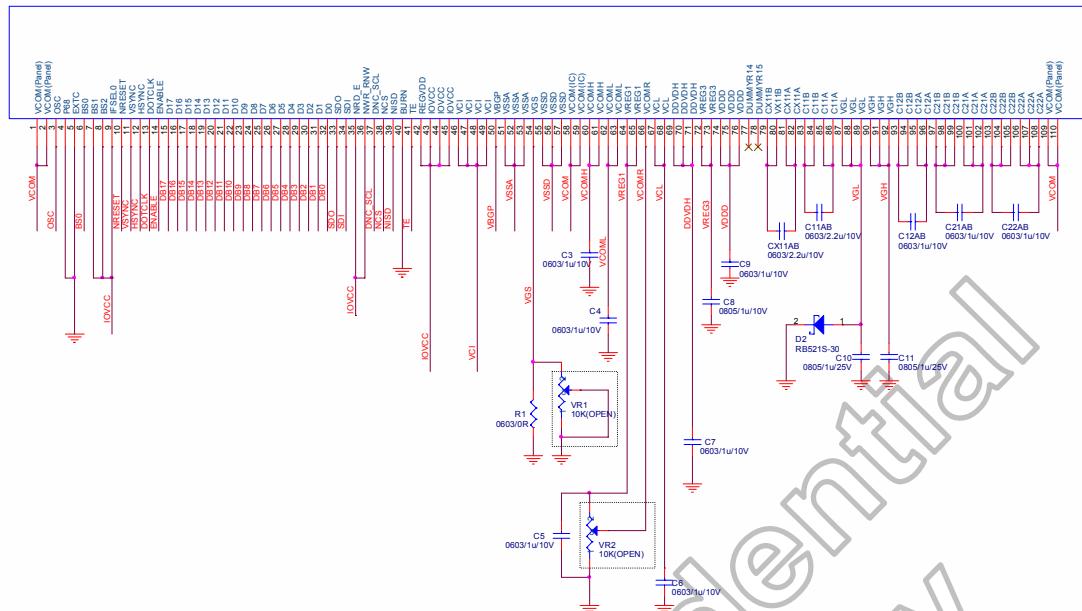
1. VCI = 2.3V~3.3V, IOVCC = 1.65V~3.3V.
2. SDO pin is output pin. SDO pin must be left floating when no use.
3. The input pin must be fixed IOVCC or GND when no use. Refer to "Pin Description".

Interface mode			
P68	BS2	BS1	BS0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1

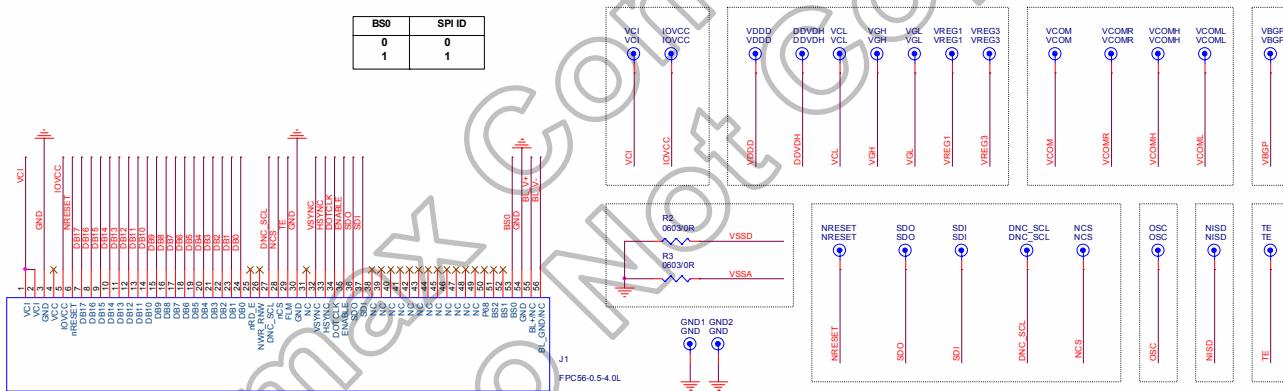
16-bit bus interface, 80-system, 65K-Color  
16-bit bus interface, 80-system, 262K-Color  
16-bit bus interface, 68-system, 65K-Color  
16-bit bus interface, 68-system, 262K-Color  
16-bit bus interface, 68-system, 262K-Color  
16-bit bus interface, 68-system, 262K-Color



## 8.2 RGB + SPI Interface of Register-Content Mode (For CMO Panel)



1. VCI = 2.3V~3.3V, IOVCC = 1.65V~3.3V.
2. SDO pin is output pin. SDO pin must be left floating when no use.
3. The input pin must be fixed IOVCC or GND when no use. Refer to "Pin Description".



### 8.3 External Components Connection

Pad Name	Connection	Component Spec
VCOMH	Connect to Capacitor (Max 6V): VCOMH---(+)---   --- (-)---- VSSA	1.0 uF
VCOML	Connect to Capacitor (Max 3V): VCOML ---(-)---   --- (+)---- VSSA	1.0 uF
VGL	Connect to Capacitor (Max 16V): VGL ---(-)---   --- (+)---- VSSA	1.0 uF
VGH	Connect to Capacitor (Max 21V): VGH ---(+)---   --- (-)---- VSSA	1.0 uF
VCL	Connect to Capacitor (Max 5V): VCL ---(-)---   --- (+)---- VSSA	1.0 uF
C22A - C22B	Connect to Capacitor (Max 7V): C22A ---(+)---   --- (-)----C22B	1.0 uF
C21A - C21B	Connect to Capacitor (Max 7V): C21A ---(+)---   --- (-)----C21B	1.0 uF
CX11A - CX11B	Connect to Capacitor (Max 7V): CX11A ---(+)---   --- (-)----CX11B	2.2 uF
C11A - C11B	Connect to Capacitor (Max 5V): C11A ---(+)---   --- (-)----C11B	2.2 uF
C12A - C12B	Connect to Capacitor (Max 6V): C12A ---(+)---   --- (-)----C12B	1.0 uF
VREG1	Connect to Capacitor (Max 6V): VREG1 ---(+)---   --- (-)----VSSA	1.0 uF
VREG3	Connect to Capacitor (Max 6V): VREG3 ---(+)---   --- (-)----VSSA	1.0 uF
VDDD	Connect to Capacitor (Max 6V): VDDD ---(+)---   --- (-)----VSSA	1.0 uF
DDVDH	Connect to Capacitor (Max 6V): DDVDH ---(+)---   --- (-)----VSSA	1.0 uF
VGL - GND	Connect to Schottky Diode	VF < 0.4V / 20mA at 25°C, VR ≥30V (Recommended diode: RB521S-30)

Table 8. 1 External component table

## 9. Ordering Information

Part No.	Package
<b>HX8347-A010 PD<u>xxx</u>-E</b>	PD : mean COG xxx : mean chip thickness ( $\mu\text{m}$ ), (default: 300 $\mu\text{m}$ )

## 10. Revision History

Version	Date	Description of Changes
01	2007/06/29	1. New setup(HX8347-A01Datasheet)
	2007/07/02	1. Modify Figure 5.24~25 of TE mode output.(P.46)
	2007/07/20	1. Update Gamma formula.(P.59~P.62) 2. Modify Figure 5.37 Gamma Register Stream and Gamma Reference Voltage.(P.57) 3. Update 5.14 Output Voltage of 8 to 1 Selector.(P.58)
	2007/07/23	1. Update chip thickness (300 $\mu\text{m}$ ).(P.16)
	2007/08/03	1. Modify NISD pin description (P.13)
	2007/08/24	1. Update 5.15 OTP programming.(P.70) 2. Add RGB+SPI interface circuit.(P.127) 3. Modify D17-D0 pin description.(P.14)
	2007/09/04	1. Update AC timing.(P.120~P.124)
02	2007/10/13	1. Update Table5.7 EPL Bit Setting and Valid Enable Signal.(P.39) 2. Modify 6.33 RGB Interface Control 1 Register - EPL bit setting description.(P.99)
	2007/11/07	1. Modify state of Data bus unused pins.(P.14) 2. Modify Figure 5.11~12 and 5.15.(P.34~P.35) 3. Add tRAT timing in Table 7. 4 AC Characteristic of 8080-series Interface.(P.120) 4. Upfate Ordering Information(P.129)
	2008/02/13	1. Modify Figure 5. 40 Scan Function.(P.64)
	2008/03/18	1. Remove Schottky Diode(D1, D3) and Capacitor(C1, C2) in 8. Reference Applications.(P.126~P.128)
	2008/03/31	1. Add OTP Related register1~3 command description in P116~117. 2. Modify VSYNC, HSYNC ENABLE DOTCLK pin description. (P.11~P.12)
03	2008/04/20	1. Update Figure 5. 37 Gamma Resister Stream and Gamma Reference Voltage.(P.57) 2. Update Table 5. 18 Voltage Calculation Formula of Grayscale Voltage.(P.62)
	2008/07/21	1. Update BP[3:0] and FP[3:0] setting value.(P.96) 2. Update RTN[3:0] setting value.(P.101)
	2008/08/29	1. Modify OTP Related register 1~3 command description.(P.116)
	2008/10/24	1. Update "7.7.4 RGB Interface Characteristics".(P.127~P.128) 2. Add OTP Related register 4 command.(P.117) 3. Add TEST MODE Control command.(P.118) 4. Add Source Driver Control 1 command.(P.118) 5. Add Source Driver Control 2 command.(P.119) 6. Add Ivci in STB mode and SD_PULL_GND=1.(P122)
	2009/07/23	1. Modify VCI, IOVCC and VCL maximum ratings.(P.120)