## RCET 0253 Systems Analog and Digital Lab Linear Regulated Power Supply Check-Off Sheet

## Student Information

Name	Start Date		
Check-Offs			
Action item	Date (DD/MM/YY)	Status	Instructor Initials
Calculated rectifier section, document oredicted waveforms		☐ Satisfactory ☐ Unsatisfactory	
2a. Assemble/solder: Power cord, fuses, on/of switch, transformer, & rectifier. Perform continuity check.	f	□ Satisfactory □ Unsatisfactory	
2b. Measure and document rectified unloaded voltage waveforms		□ Satisfactory □ Unsatisfactory	
2c. Measured and document loaded voltage waveforms		□ Satisfactory □ Unsatisfactory	
3a. Calculate appropriate filter cap & On/Off ndication circuit		☐ Satisfactory ☐ Unsatisfactory	
3b. Assemble Filter Capacitor and measure unloaded and loaded voltage waveforms.		□ Satisfactory □ Unsatisfactory	
4a. Calculate and document the op-amp regulated variable voltage section		□ Satisfactory □ Unsatisfactory	
4b. Assemble/solder op-amp regulated variable voltage section. With no load (10K RL) verify variable voltage operation.		□ Satisfactory □ Unsatisfactory	
5a. Calculated and document the current- imiting section		☐ Satisfactory ☐ Unsatisfactory	
5b. Assemble/solder the current-limiting section. Verify current-limiting operation by incrementally increase load until output is shorted through your current meter. Verify imiting range		□ Satisfactory □ Unsatisfactory	
6a. Calculated and document over-voltage protection circuit		☐ Satisfactory ☐ Unsatisfactory	
6b. Assemble/solder over-voltage section. Verify operation		□ Satisfactory □ Unsatisfactory	
7a. Calculate overvoltage/output-shorted ndication circuit		□ Satisfactory □ Unsatisfactory	
7b. Assemble/solder overvoltage/output- shorted indication circuit. Verify.		□ Satisfactory □ Unsatisfactory	
Ba. Final Check-Off: Verify variable voltage, current limiting, and over-voltage.		☐ Satisfactory ☐ Unsatisfactory	
Bb. Final Check-Off: 60min output shorted test		□ Satisfactory □ Unsatisfactory	
Bc. Final Check-Off: Final Check-Off: Verify variable voltage, current limiting, and overvoltage.		□ Satisfactory □ Unsatisfactory	

Action item	Date (DD/MM/YY)	Status	Instructor Initials
Check-Off Redo			
(write in Action Item!)	Date (DD/MM/YY)	Status	Instructor Initials
		Satisfactory 🗆 Unsatisfact	ory
		Satisfactory 🗆 Unsatisfact	ory
		Satisfactory 🗆 Unsatisfact	ory
		Satisfactory 🗆 Unsatisfact	ory
		Satisfactory 🗆 Unsatisfact	ory
		Satisfactory 🗆 Unsatisfact	ory
		Satisfactory 🗆 Unsatisfact	ory
		Satisfactory 🗆 Unsatisfact	ory
		Satisfactory 🗆 Unsatisfact	ory
		Satisfactory 🗆 Unsatisfact	ory
		Satisfactory 🗆 Unsatisfact	ory