

Practice Problems

- 3-7.1 Design a 12 V dc reference source (consisting of a Zener diode and series-connected resistor) to operate from a 25 V supply. Determine the effect on the diode current when the supply drops to 22 V.
- 3-7.2 An 8 V dc reference source is to be designed to produce the maximum possible output current from a low-power Zener diode. The supply voltage is 20 V. Design the circuit and determine the maximum load current.
- 3-7.3 Calculate the line effect, load effect, and ripple rejection for the circuit designed in Problem 3-7.2.

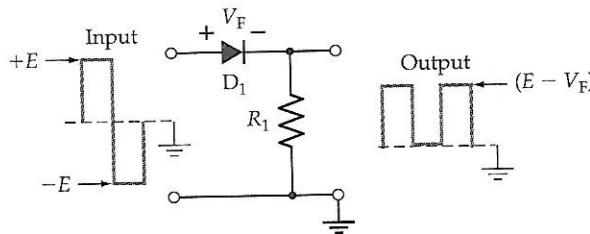
3-8 SERIES CLIPPING CIRCUITS

Series Clipper

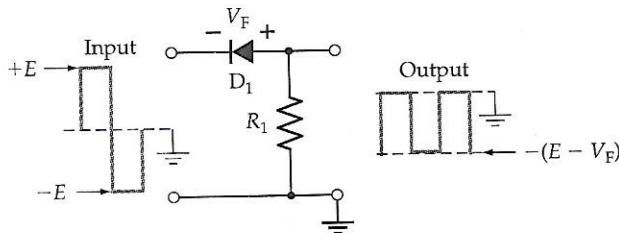
The function of a *clipper* (or *limiter*) is to clip off an unwanted portion of a waveform. This is sometimes necessary to protect a device or circuit that might be destroyed by a large-amplitude signal (negative or positive).

A half-wave rectifier can be described as a clipper because it passes only the positive (or negative) half-cycle of an alternating waveform and clips off the other half-cycle. In fact, a diode *series clipper* is simply a half-wave rectifier circuit.

Figure 3-36a shows a *negative series clipper* circuit with a square wave input symmetrical above and below ground level. While the input is positive, D_1 is forward-biased and the positive half-cycle is passed to the output.



(a) Negative series clipper



(b) Positive series clipper

Figure 3-36 Diode series clipping circuits clip off unwanted portions of input waveforms. These are essentially half-wave rectifier circuits.

$$V_o = E - V_F \quad (3-49)$$

During the negative half-cycle of the input, the diode is reverse-biased. Consequently, the output remains at zero and the negative half-cycle is effectively clipped off. The *zero level* output from a series clipper circuit is not exactly zero. The reverse saturation current (I_R) of the diode produces a voltage drop across resistor R_1 :

$$V_o = -I_R R_1 \quad (3-50)$$

This voltage drop is almost always so small that it can be ignored.

If the diode in Fig. 3-36a is reconnected with reversed polarity, as shown in Fig. 3-36b, the positive half-cycles are clipped off and the circuit becomes a positive series clipper. The input waveforms to a clipper may be square, sinusoidal, or any other shape.

The output terminals of series clippers are usually connected to circuits that have a high input resistance; so the (current-limiting) resistor R_1 is selected to pass an acceptable minimum current through the diode. This current must be sufficient to operate the diode beyond the *knee* of its forward characteristic (see Fig. 2-4). Usually, a current of 1 mA is adequate. The resistor value is calculated from the output voltage and the selected current level. The remaining part of the design process is specifying the diode.

Example 3-19

The negative series clipper in Fig. 3-37 has a ± 9 V input and zero load current. Determine a suitable resistance for R_1 , and specify the diode forward current and reverse voltage. Use a silicon diode.

Solution

$$\begin{aligned} V_o &= E - V_F \\ &= 9 \text{ V} - 0.7 \text{ V} \\ &= 8.3 \text{ V} \end{aligned}$$

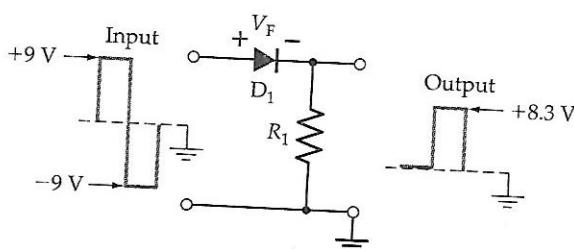


Figure 3-37 Series clipper circuit for Ex. 3-19.

Select $I_F = 1 \text{ mA}$

$$R_1 = \frac{V_o}{I_F} = \frac{8.3 \text{ V}}{1 \text{ mA}}$$

$$= 8.3 \text{ k}\Omega \text{ (use } 8.2 \text{ k}\Omega \text{ standard value)}$$

Diode specification:

$$V_R = E = 9 \text{ V}$$

$$I_F = 1 \text{ mA}$$

Current Level Selection

In most electronic circuits it is best to select the smallest possible level of current. One reason is to keep the total supply current to a minimum. High supply currents require larger, more expensive power supplies than low current levels. Where a battery supply is used, batteries last longer with low supply currents. Another reason to keep circuit current levels low whenever possible is to minimize component power dissipation. Low power dissipation allows the smallest components to be used and avoids circuit heating problems.

Series Noise Clipper

Digital signal waveforms sometimes have unwanted lower-level *noise* voltages. The noise can be removed by a *series noise clipping circuit*, which simply consists of two inverse-parallel connected diodes, as illustrated in Fig. 3-38. When the noise amplitude is much smaller than the diode forward voltage drop (V_F), and the signal amplitude is larger than V_F , the signals are passed and the noise is blocked. The signal peak output voltage is $E - V_F$.

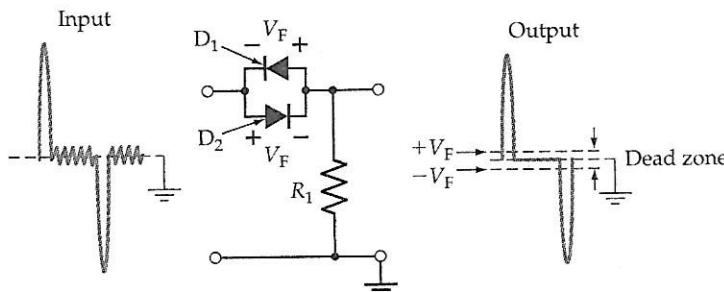


Figure 3-38 Series noise clipping circuit. Noise amplitudes lower than $\pm V_F$ cannot pass to the output.

A *dead zone* of $\pm V_F$ exists around ground level in the output waveform, indicating that inputs must exceed $\pm V_F$ to pass to the output. For noise voltage amplitudes that approach $\pm V_F$, two diodes may be connected in series to give a larger dead zone.

Practice Problems

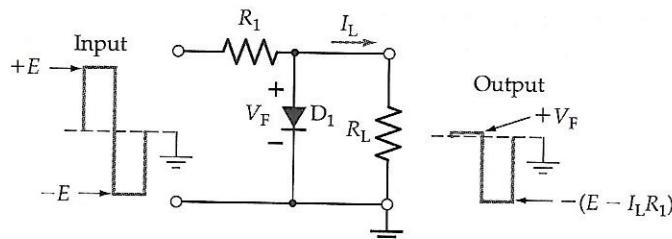
- 3-8.1** A positive series clipping circuit, as in Fig. 3-36b, has a ± 7 V input and zero load current. Calculate a suitable resistance for R_1 , and specify the diode.
- 3-8.2** A ± 6 V square wave is applied via a series clipping circuit to a device that cannot survive $+6$ V. The device input current is $100 \mu\text{A}$ when its input voltage is negative. Select a suitable clipping circuit, determine the required resistance, and specify the diode.

3-9 SHUNT CLIPPING CIRCUITS

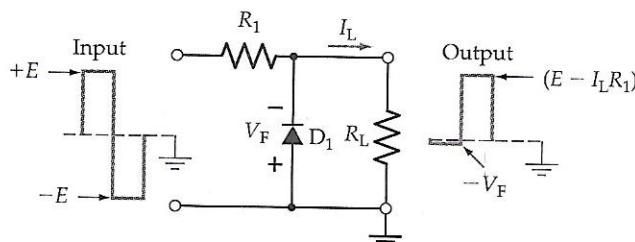
Shunt Clipper

A *positive shunt clipper circuit* is illustrated in Fig. 3-39a. Here the diode is connected in *shunt* (or parallel) with the output terminals. When the input is negative, the diode is reverse-biased and there is only a small voltage drop across R_1 , due to load current I_L . This means that the circuit output voltage (V_o) is approximately equal to the negative input peak ($-E$). When the input is $+E$, D_1 is forward-biased and the output voltage equals the diode voltage drop ($+V_F$). Thus, the positive half of the waveform is clipped off. As illustrated, the upper and lower levels of the output of a positive shunt clipper are approximately $+V_F$ and $-E$.

A *negative shunt clipper circuit* is exactly the same as a positive shunt clipper with the diode polarity reversed (see Fig. 3-39b). The negative half-cycle of the waveform is clipped off.



(a) Positive shunt clipper



(b) Negative shunt clipper

Figure 3-39 Shunt clipping circuits. The output voltage cannot exceed the diode voltage drop (V_F) when the input voltage forward-biases the diode.

The load current on a shunt clipper produces a voltage drop ($I_L R_1$) across the resistor; this might be insignificant where the load current is very low:

$$V_o = E - (I_L R_1) \quad (3-51)$$

As in the case of series clipping circuits, shunt clippers may be used with square, sinusoidal, or other input waveforms.

Example 3-20

The negative shunt clipper in Fig. 3-40 has a ± 5 V input, and is to produce a $+4.5$ V minimum output when the load current is 2 mA. Determine a suitable resistance for R_1 , and specify the diode forward current and reverse voltage.

Solution

When the diode is reverse-biased:

$$\text{Eq. 3-51:} \quad V_o = E - (I_L R_1)$$

$$\text{or} \quad R_1 = \frac{E - V_o}{I_L} = \frac{5 \text{ V} - 4.5 \text{ V}}{2 \text{ mA}} \\ = 250 \Omega \text{ (use } 220 \Omega\text{)}$$

Diode reverse voltage:

$$V_R = E = 5 \text{ V}$$

When the diode is forward-biased:

$$I_F = \frac{E - V_F}{R_1} = \frac{5 \text{ V} - 0.7 \text{ V}}{220 \Omega} \\ = 19.5 \text{ mA}$$

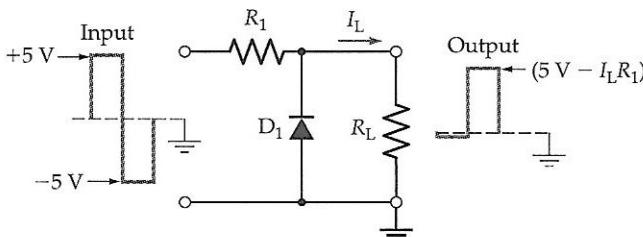


Figure 3-40 Negative shunt clipper for Ex. 3-20.

Shunt Noise Clipper

The shunt noise clipper shown in Fig. 3-41 removes noise riding on the peaks of an input waveform. The signal amplitude must be greater than the diode forward voltage drop. The output waveform is clipped at $\pm V_F$, so that the noise is not passed to the output. This type of clipper is used with pulse signals where the pulse amplitude is not important. In this case, information is contained in the pulse width or simply in its presence or absence.

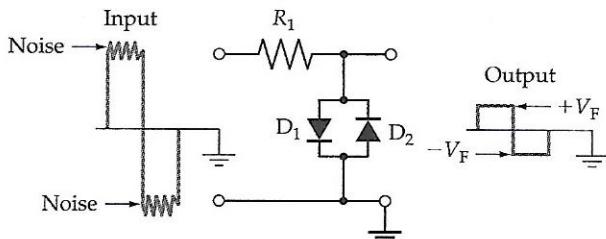


Figure 3-41 Shunt noise clipper circuit. Input amplitudes greater than $\pm V_F$ are clipped off.

Biased Shunt Clipper

Figure 3-42 shows a clipping circuit that uses two diodes that have different bias voltages. The cathode of D_1 is connected to a $+2$ V bias (V_{B1}), and the anode of D_2 has a -2 V bias (V_{B2}). While the input waveform amplitude is less than $\pm(V_B + V_F)$, neither diode is forward-biased, and the input is simply passed to the output. When the positive input is greater than $(V_{B1} + V_F)$, D_1 becomes forward-biased, and the output cannot exceed this voltage. Similarly, when the negative input goes below $(-V_{B2} - V_F)$, D_2 is forward-biased and the output is limited to $-(V_{B2} + V_F)$.

$$V_o = \pm(V_B + V_F) \quad (3-52)$$

For obvious reasons, the circuit is termed a *biased shunt clipper*. Biased shunt clippers are used to protect circuits or devices from (positive/negative) input voltages that must not exceed specified levels.

The voltage across resistor R_1 is $(E - V_o)$ in Fig. 3-42, and the resistor current is the sum of the load current and the diode forward current ($I_L + I_F$). As in other diode circuits, a minimum level of I_F is selected, and the resistor value is calculated as

$$R_1 = \frac{E - V_o}{I_L + I_F} \quad (3-53)$$

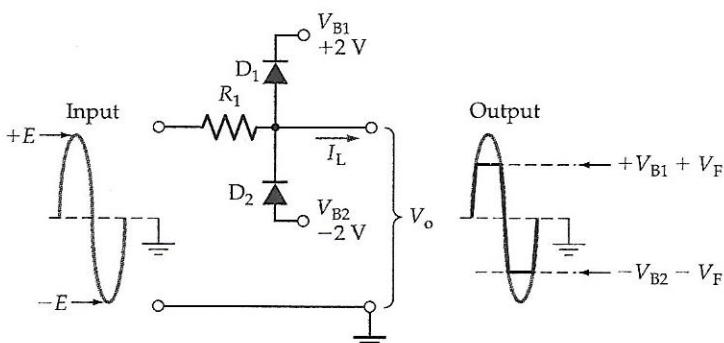


Figure 3-42 Biased shunt clipper circuit. Input amplitudes greater than $\pm(V_B + V_F)$ are clipped off.

Example 3-21

The biased shunt clipper in Fig. 3-42 has a ± 9 V input, and its output is to be limited to ± 2.7 V. Determine a suitable resistance for R_1 if the clipper output current is to be ± 1 mA.

Solution

$$\text{Eq. 3-52:} \quad V_o = \pm (V_B + V_F)$$

$$\text{giving} \quad V_B = \pm (V_o - V_F)$$

$$= \pm (2.7 \text{ V} - 0.7 \text{ V})$$

$$= \pm 2 \text{ V}$$

Select the diode forward current as

$$I_F = 1 \text{ mA}$$

$$\text{Eq. 3-53:} \quad R_1 = \frac{E - V_o}{I_L + I_F} = \frac{9 \text{ V} - 2.7 \text{ V}}{1 \text{ mA} + 1 \text{ mA}}$$

$$= 3.15 \text{ k}\Omega \quad (\text{use } 2.7 \text{ k}\Omega \text{ to give } I_F > 1 \text{ mA})$$

Zener Diode Shunt Clipper

A Zener diode shunt clipper produces the same kind of result as a biased shunt clipper without the need for bias voltages. The clipper circuit in Fig. 3-43 has two back-to-back series-connected Zener diodes. When the input voltage is positive and has sufficient amplitude, D_1 is forward-biased and D_2 is biased into reverse breakdown. At this time, the output voltage is limited to $(V_F + V_{Z2})$. A negative input voltage produces a maximum negative output of $-(V_F + V_{Z1})$. With equal-voltage Zener diodes, the maximum output voltage is

$$V_o = \pm (V_F + V_Z) \quad (3-54)$$

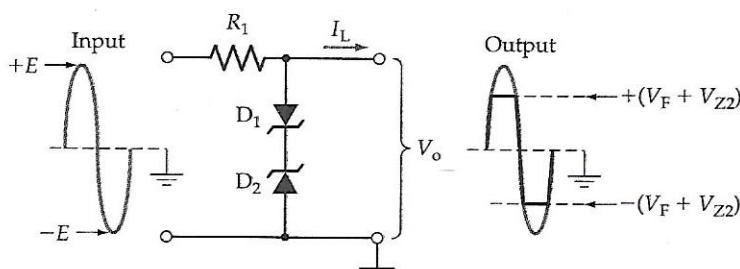


Figure 3-43 Zener diode shunt clipper circuit. Input amplitudes greater than $\pm(V_F + V_Z)$ are clipped off.

The resistor voltage is $(E - V_o)$, and the resistor current is $(I_L + I_Z)$. A minimum level of I_Z (greater than the device knee current) is selected, and the resistor value is calculated as

$$R_1 = \frac{E - V_o}{I_L + I_Z} \quad (3-55)$$

Example 3-22

A Zener diode shunt clipper, as in Fig. 3-43, is to be connected between a ± 20 V square wave signal and a circuit that cannot accept inputs greater than ± 5 V. Select suitable Zener diodes, and determine R_1 . The clipper output current is to be ± 1 mA.

Solution

$$\begin{aligned} \text{From Eq. 3-54, } V_Z &= V_o - V_F \\ &= 5 \text{ V} - 0.7 \text{ V} \\ &= 4.3 \text{ V} \end{aligned}$$

From data sheet A-4 in Appendix A, it is seen that the 1N749 has $V_Z = 4.3$ V. Use 1N749 Zener diodes.

Select $I_{Z(\min)} = 5$ mA

$$\begin{aligned} \text{Eq. 3-55: } R_1 &= \frac{E - V_o}{I_L + I_Z} = \frac{20 \text{ V} - 5 \text{ V}}{1 \text{ mA} + 5 \text{ mA}} \\ &= 1.86 \text{ k}\Omega \quad (\text{use } 1.8 \text{ k}\Omega \text{ to give } I_Z > 5 \text{ mA}) \end{aligned}$$

Practice Problems

- 3-9.1 A positive shunt clipper, as in Fig. 3-39a, has a ± 7 V input. The negative output voltage is to be 6.5 V when the load current is 1.5 mA. Calculate the required resistance for R_1 , and specify the diode forward current and reverse voltage.
- 3-9.2 A ± 8 V square wave is applied to a device that cannot accept inputs greater than ± 3.5 V. The device input current is $\pm 600 \mu\text{A}$. Design a suitable biased shunt clipping circuit.
- 3-9.3 A Zener diode shunt clipping circuit is to be used to clip a ± 18 V square wave off at approximately ± 7 V. The output current is to be ± 1.2 mA. Design the circuit.

3-10 CLAMPING CIRCUITS

Negative and Positive Voltage Clamping Circuits

A *clamping circuit*, also known as a dc *restorer*, changes the dc voltage level of a waveform but does not affect its shape. Consider the clamping circuit shown in Fig. 3-44. When the square wave input is positive, diode D₁ is forward-biased and the output voltage equals the diode forward voltage drop V_F.

$$V_o = V_F \quad (3-56)$$

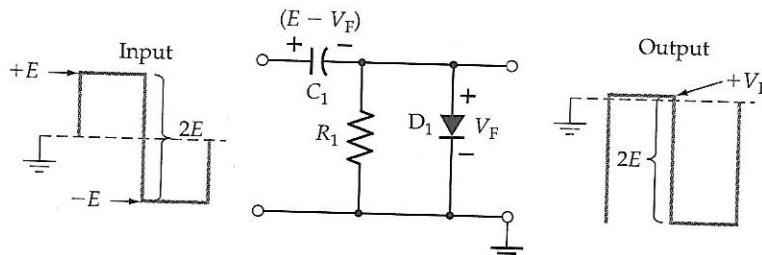


Figure 3-44 A negative voltage clamping circuit passes the complete input waveform to the output but clamps the positive peak of the output close to ground level.

During the positive half-cycle of the input, the voltage on the right side of the capacitor is +V_F, while that on the left side is +E. Thus, C₁ is charged with the polarity shown to a voltage:

$$V_C = (E - V_F) \quad (3-57)$$

When the input goes negative, the diode is reverse-biased and has no further effect on the capacitor voltage. Also, R₁ has a very high resistance, so that it cannot discharge C₁ significantly during the negative portion of the input waveform. While the input is negative, the output voltage is the sum of the input and capacitor voltages. Since the polarity of the capacitor voltage is the same as the (negative) input, the output is

$$\begin{aligned} V_o &= -(E + V_C) \\ &= -[E + (E - V_F)] \end{aligned}$$

or

$$V_o = -(2E - V_F) \quad (3-58)$$

The peak-to-peak output voltage ($V_{o(pp)}$) is the difference between the positive output peak (V_F) and negative output peak $-(2E - V_F)$:

$$V_{o(pp)} = V_F - [-(2E - V_F)]$$

or

$$V_{o(pp)} = 2E \quad (3-59)$$

It is seen that the peak-to-peak amplitude of the output waveform from the clamping circuit is exactly the same as the peak-to-peak input. Instead of the waveform being symmetrical above and below ground, however, the output positive peak is clamped at a level of $+V_F$.

The circuit in Fig. 3-44 is known as a *negative voltage clamping circuit*, because the output waveform is almost completely negative. Reversing the polarity of the diode and capacitor in Fig. 3-44 creates the *positive voltage clamping circuit* shown in Fig. 3-45. As illustrated, the output waveform is clamped to keep it almost completely positive.

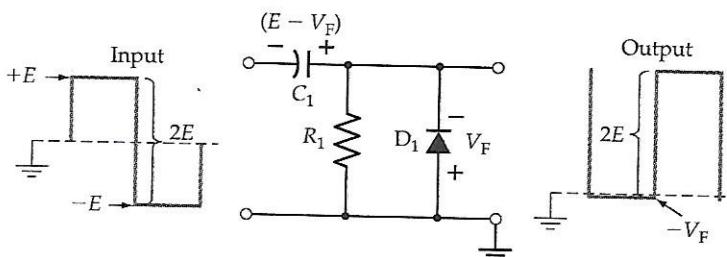


Figure 3-45 A positive voltage clamping circuit passes the complete input waveform to the output but clamps the negative peak of the output close to ground level.

Output Slope

Resistor R_1 in both Figs 3-44 and 3-45 is sometimes termed as *bleeder resistor*. Its function is to discharge the capacitor gradually over several cycles of input waveform, so that it can be charged to a new voltage level if the input changes. However, R_1 partially discharges the capacitor during the time that D_1 is reverse-biased, and this produces a *slope* or *tilt* (ΔV_C) on the output waveform, as illustrated in Fig. 3-46. The tilt voltage can be calculated from a knowledge of the waveform frequency and the circuit component values. The constant-current equation for charging or discharging a capacitor may be applied:

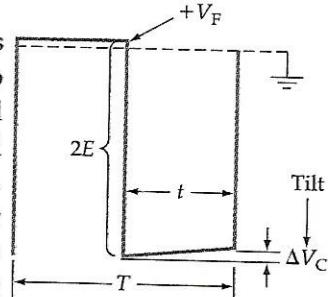


Figure 3-46 The output voltage from a clamping circuit has a slope (ΔV_C) produced by capacitor discharge. The capacitance value is determined from the acceptable slope.

$$\Delta V_C = \frac{I_C \times t}{C_1} \quad (3-60)$$

Example 3-23

The diode clamping circuit in Fig. 3-47 has a ± 10 V, 1 kHz square wave input. Calculate the tilt on the output waveform.

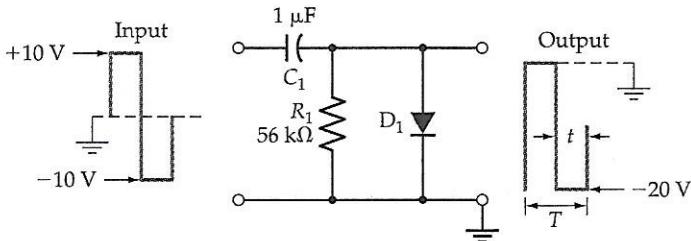


Figure 3-47 Clamping circuit for Ex. 3-23.

Solution

While the diode is reverse-biased,

$$\begin{aligned}V_{o(pp)} &= 2E \\&= 2 \times 10 \text{ V} \\&= 20 \text{ V}\end{aligned}$$

and

$$\begin{aligned}I_C &\approx \frac{V_{o(pp)}}{R_1} = \frac{20 \text{ V}}{56 \text{ k}\Omega} \\&= 367 \mu\text{A} \\t &= \frac{T}{2} = \frac{1}{2f} = \frac{1}{2 \times 1 \text{ kHz}} \\&= 500 \mu\text{s} \\ \text{Eq. 3-60: } \Delta V_C &= \frac{I_C \times t}{C_1} = \frac{367 \mu\text{A} \times 500 \mu\text{s}}{1 \mu\text{F}} \\&= 184 \text{ mV}\end{aligned}$$

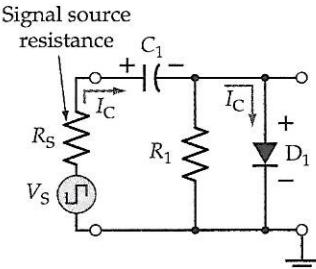
Component Determination

When a clamping circuit is designed, capacitor C_1 is selected so that it becomes completely charged in approximately five cycles of the input waveform. As already explained (and illustrated in Fig. 3-48), diode D_1 is forward-biased when C_1 is being charged. Resistor R_1 is not part of the C_1 charging circuit, because D_1 bypasses R_1 . As illustrated, the C_1 charge is controlled by the signal source resistance (R_S). A capacitor is completely charged in approximately five time constants of the circuit. In the case of a resistor-capacitor circuit, the time constant is RC . So the charging time is

$$5 RC = 5 \times [\text{input pulse width (PW)}]$$

or

$$RC = PW$$

Figure 3-48 Capacitor C_1 is charged via signal source resistance R_S .

This gives

$$C_1 R_S = PW \quad (3-61)$$

When the pulse width and source resistance of the input waveform are known, C_1 can be determined from Eq. 3-61.

As long as the slope on the output waveform is very small, the capacitor discharge current is essentially a constant quantity.

$$I_C = \frac{V_o}{R_1}$$

Or

$$I_C = \frac{2E}{R_1} \quad (3-62)$$

When the output waveform slope is specified, I_C can be calculated from Eq. 3-60, and a suitable resistance for R_1 is then determined by substituting I_C into Eq. 3-62.

Example 3-24

The negative voltage clamping circuit in Fig. 3-49 has a ± 8 V, 500 Hz square wave input with a 600Ω signal source resistance. The output waveform is to have a maximum slope of 1%. Determine suitable values for R_1 and C_1 .

Solution

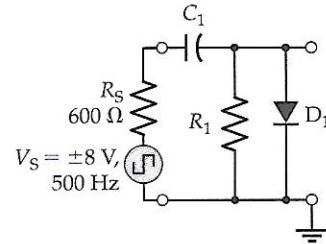


Figure 3-49 Clamping circuit for Ex. 3-24.

$$\begin{aligned} t &= \frac{T}{2} = \frac{1}{2f} = \frac{1}{2 \times 500 \text{ Hz}} \\ &= 1 \text{ ms} \end{aligned}$$

$$PW = t = 1 \text{ ms}$$

$$\begin{aligned} \text{From Eq. 3-61, } C_1 &= \frac{PW}{R_S} = \frac{1 \text{ ms}}{600 \Omega} \\ &= 1.7 \mu\text{F} \text{ (use } 1.8 \mu\text{F)} \end{aligned}$$

$$\begin{aligned} V_{o(pp)} &= 2E = 2 \times 8 \text{ V} \\ &= 16 \text{ V} \end{aligned}$$

$$\begin{aligned} \Delta V_C &= 1\% \text{ of } V_{o(pp)} = 1\% \text{ of } 16 \text{ V} \\ &= 0.16 \text{ V} \end{aligned}$$

$$\begin{aligned} \text{From Eq. 3-60, } I_C &= \frac{\Delta V_C C_1}{t} = \frac{0.16 \text{ V} \times 1.8 \mu\text{F}}{1 \text{ ms}} \\ &= 288 \mu\text{A} \end{aligned}$$

From Eq. 3-62,

$$R_1 = \frac{2E}{I_C} = \frac{16 \text{ V}}{288 \mu\text{A}} \\ = 55.5 \text{ k}\Omega \text{ (use } 56 \text{ k}\Omega\text{)}$$

Biased Clamping Circuit

The biased clamping circuit shown in Fig. 3-50 has a bias voltage (V_B) at the cathode of diode D_1 . In this case, the output voltage cannot exceed ($V_{B1} + V_F$), as illustrated. The capacitor charges to ($E - V_{B1} - V_F$) when the input is positive. When the input goes negative, the output voltage is $-(E + V_C)$, giving

$$V_o = -[E + (E - V_{B1} - V_F)] \\ = -2E + V_{B1} + V_F$$

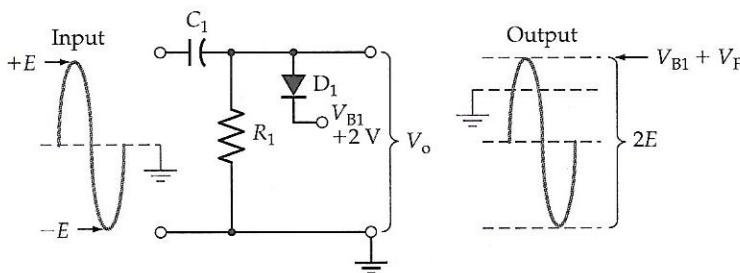


Figure 3-50 A biased clamping circuit clamps one peak of the output voltage at a selected voltage level.

The peak-to-peak output voltage is the difference between the positive and negative output peak levels.

$$V_o = (V_{B1} + V_F) - [-2E + V_{B1} + V_F] \\ = 2E$$

It is seen that, as for other clamping circuits, the peak-to-peak output waveform from the biased clamer is the same as the input. The positive level of the output is clamped to ($V_B + V_F$).

Virtually any bias voltage level (positive or negative) can be used with a biased clamping circuit. The diode polarity determines whether the positive or the negative peak of the output is clamped. Care must be taken to ensure that the capacitor is connected with the correct polarity. Biased clamping circuits are designed in exactly the same way as unbiased clamping circuits.

Example 3-25

Determine the upper and lower levels of the output voltage for the circuits shown in Fig. 3-51 when the input voltage is $\pm 6 \text{ V}$. Calculate the capacitor voltage in each case.

Solution

For Fig. 3-51a, D_1 is forward-biased when the input goes negative. When the input is $-E$,

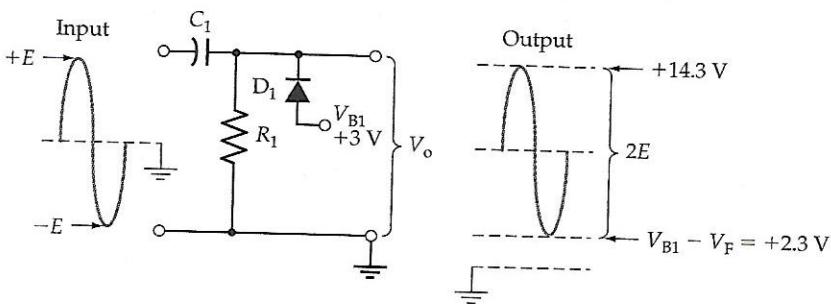
$$\begin{aligned}V_C &= V_{B1} - V_F - E \\&= 3 \text{ V} - 0.7 \text{ V} - (-6 \text{ V}) \\&= 8.3 \text{ V} (+ \text{ on the right})\end{aligned}$$

$$\begin{aligned}V_o &= V_{B1} - V_F \\&= 3 \text{ V} - 0.7 \text{ V} \\&= 2.3 \text{ V} (\text{low level of output})\end{aligned}$$

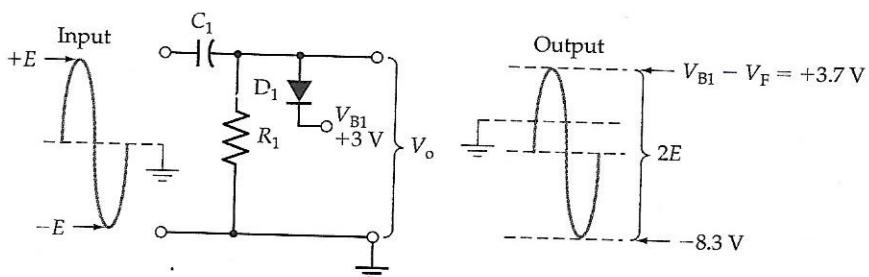
When the input is $+E$, $V_o = E + V_C$

$$\begin{aligned}&= 6 \text{ V} + 8.3 \text{ V} \\&= 14.3 \text{ V} (\text{high level of output})\end{aligned}$$

For Fig. 3-51b, D_1 is forward-biased when the input goes positive.



(a) Output voltage cannot go below $(V_{B1} - V_F)$



(b) Output voltage cannot go above $(V_{B1} - V_F)$

Figure 3-51 Biased clamping circuits use positive or negative bias voltages to clamp the level of one of the peaks of the output waveform above or below the bias voltage level.

When the input is $+E$, $V_C = E - V_{B1} - V_F$

$$= 6 \text{ V} - 3 \text{ V} - 0.7 \text{ V}$$

$$= 2.3 \text{ V (+ on the left)}$$

$$V_o = V_{B1} + V_F$$

$$= 3 \text{ V} + 0.7 \text{ V}$$

$$= 3.7 \text{ V (high level of output)}$$

When the input is $-E$, $V_o = E + V_C$

$$= -6 \text{ V} - 2.3 \text{ V}$$

$$= -8.3 \text{ V (low level of output)}$$

Zener Diode Clamping Circuit

Zener diode clamping circuits operate just like biased voltage clampers, with the Zener diode voltage (V_Z) replacing the bias voltage. The circuit in Fig. 3-52 has an ordinary diode (D_1) connected in series with a Zener diode (D_2). When the input voltage is at its positive peak, the output voltage is

$$V_o = V_Z + V_F$$

and C_1 charges (+ on the left) to

$$V_C = E - (V_Z + V_F)$$

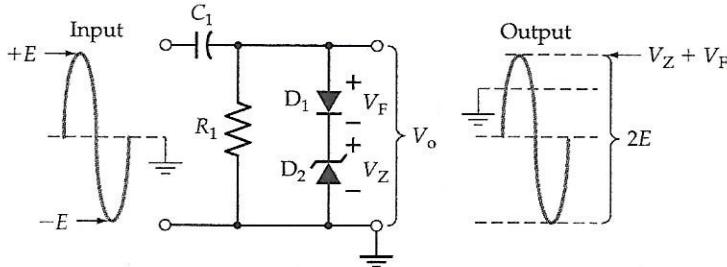


Figure 3-52 Zener diode clamping circuits clamp the output voltage at $(V_Z + V_F)$. The positive peak or the negative peak of the waveform can be clamped above or below ground.

When the input goes to its negative peak, the output voltage is

$$V_o = -(E + V_C)$$

$$V_o = -[E + E - (V_Z + V_F)]$$

$$= -(2E - V_Z - V_F)$$

The peak-to-peak output remains equal to the peak-to-peak input voltage ($2E$). If the polarity of the diodes (and the capacitor) are reversed, the negative output peak is clamped at $-(V_Z + V_F)$.

Practice Problems

- 3-10.1 A ± 8 V, 300 Hz square wave is applied to the clamping circuit in Fig. 3-45. If $C_1 = 1.5 \mu\text{F}$ and $R_1 = 33 \text{k}\Omega$, determine the tilt on the output waveform.
- 3-10.2 A positive voltage clamping circuit, as in Fig. 3-45, is to have an output waveform with a maximum tilt of 0.5%. The signal is a ± 7 V, 1 kHz square wave with a 500Ω source resistance. Calculate suitable values for R_1 and C_1 .
- 3-10.3 A clamping circuit, as in Fig. 3-52, uses a 1N754 Zener diode. Determine the upper and lower levels of the output voltage if the input is a ± 12 V square wave. Calculate the capacitor voltage.

3-11 DC VOLTAGE MULTIPLIERS

Voltage Doubler

A *voltage-doubling circuit* produces an output voltage which is approximately double the peak voltage of the input waveform. Consideration of the voltage doubling circuit in Fig. 3-53 shows that it is simply a combination of two diode-capacitor clamping circuits without the discharge resistors. In fact, the circuit operation is similar to that of clamping circuits.

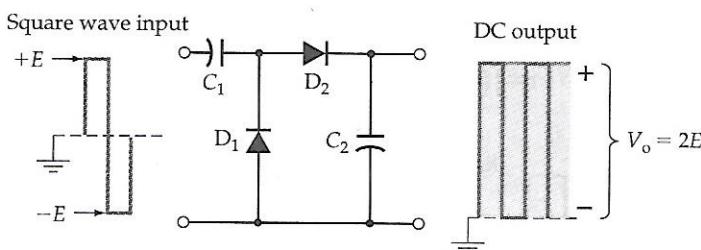


Figure 3-53 A voltage-doubling circuit produces a dc output voltage which is approximately double the peak input voltage.

When the input voltage is negative, as shown in Fig. 3-54a, diode D_1 is forward-biased and C_1 charges to $(E - V_{F1})$ with the polarity illustrated. D_2 is reverse-biased during the negative half-cycle of the input, and so the charge on C_2 is not affected at this time.

Figure 3-54b shows what occurs during the input positive half-cycle. D_1 is now reverse-biased, and D_2 is forward-biased. The voltage applied to D_2 and C_2 is the sum of the input voltage and the voltage on C_1 . So, as illustrated, capacitor C_2 is charged to

$$\begin{aligned}V_{C2} &= E + V_{C1} - V_{F2} \\&= E + (E - V_{F1}) - V_{F2} \\&= 2(E - V_F)\end{aligned}$$

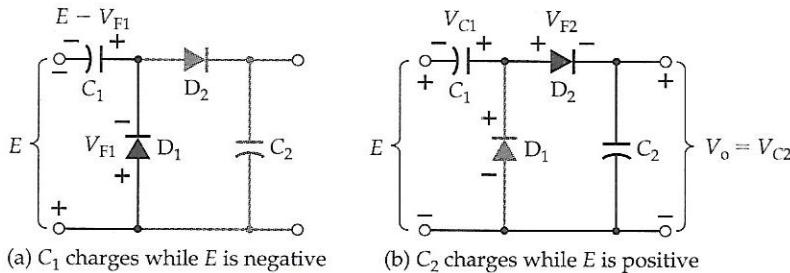


Figure 3-54 In a voltage-doubling circuit, capacitor C_1 charges to $(E - V_{F1})$ during the negative half-cycle of the input. Then, $+[E + (E - V_{F1}) - V_{F2}]$ is passed to C_2 during the input positive half-cycle.

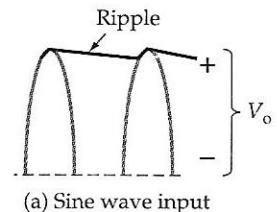
So

$$V_o = 2(E - V_F) \quad (3-63)$$

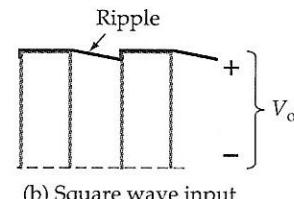
It is seen that, when the diode voltage drop is much smaller than the input voltage, the output is approximately double the peak input amplitude. The polarity of the output voltage can be reversed by reversing the polarity of the diodes and capacitors.

The output terminals of the voltage doubler are the terminals of capacitor C_2 . The load current partially discharges the capacitors, producing a drop in output voltage in the same way that tilt is created on a clamping circuit output. The repeated charge and discharge of C_1 and C_2 results in a ripple waveform on the output. A sinusoidal input waveform applied to a voltage doubler produces exactly the same type of output ripple that occurs with a half-wave rectifier (Fig. 3-55a). However, the input most often used is a dc voltage source that has been *chopped*, or converted into a square waveform (Fig. 3-55b).

Figure 3-56a shows that capacitor C_2 supplies the load current (I_L) while diode D_2 is reverse biased. The discharge of C_2 accounts for half the output ripple voltage amplitude, and the discharge of C_1 produces the other half of the ripple amplitude. Equation 3-60 can be modified for calculating the capacitance of C_2 .



(a) Sine wave input



(b) Square wave input

Figure 3-55 A ripple waveform occurs at the output of a voltage doubler. The ripple amplitude depends upon the capacitance value, the input frequency, and the load current.

$$C_2 = \frac{I_L t}{\Delta V_C} \quad (3-64)$$

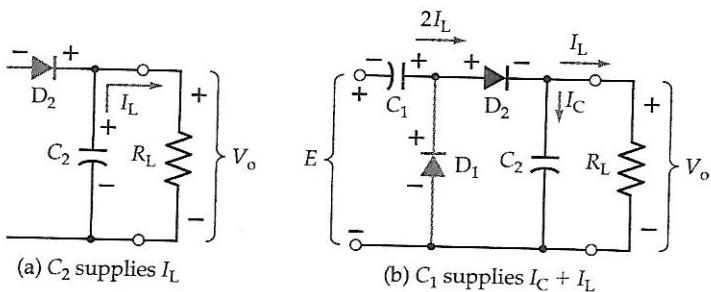


Figure 3-56 In a voltage-doubling circuit, capacitor C_2 supplies I_L while diode D_2 is reverse biased, and C_1 supplies $2I_L$ when D_2 is forward-biased.

When D_2 is forward-biased (Fig. 3-56b), capacitor C_1 supplies I_L and the recharging current to C_2 . The recharging current must equal I_L to maintain the full charge on C_2 , so C_1 supplies $2I_L$. Applying Eq. 3-60 to calculate C_1 , it is found that

$$C_1 = 2C_2 \quad (3-65)$$

Example 3-26

Determine C_1 and C_2 for the voltage-doubling circuit in Fig. 3-57 to produce a 1% maximum output ripple. The input is a ± 12 V, 5 kHz square wave.

Solution

$$\text{Eq. 3-63: } V_o = 2(E - V_F)$$

$$= 2(12 \text{ V} - 0.7 \text{ V})$$

$$= 22.6 \text{ V}$$

$$I_L = \frac{V_o}{R_L} = \frac{22.6 \text{ V}}{47 \text{ k}\Omega}$$

$$= 481 \mu\text{A}$$

$$\text{Capacitor discharge time } t = \frac{T}{2} = \frac{1}{2f} = \frac{1}{2 \times 5 \text{ kHz}}$$

$$= 100 \mu\text{s}$$

For 1% output ripple, allow 0.5% due to discharge of C_2 and 0.5% due to discharge of C_1 .

$$\Delta V_C = 0.5\% \text{ of } V_{o(\text{pp})}$$

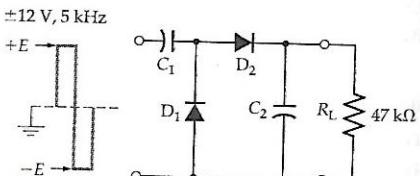


Figure 3-57 Diode voltage doubling circuit for Ex. 3-26.

$$= 0.5\% \text{ of } 22.6 \text{ V}$$

$$= 113 \text{ mV}$$

$$\text{Eq. 3-64: } C_2 = \frac{I_L t}{\Delta V_C} = \frac{481 \mu\text{A} \times 100 \mu\text{s}}{113 \text{ mV}}$$

$$= 0.43 \mu\text{F} (\text{use } 0.47 \mu\text{F})$$

$$\text{Eq. 3-65: } C_1 = 2C_2$$

$$= 2 \times 0.47 \mu\text{F}$$

$$= 0.94 \mu\text{F} (\text{use } 1 \mu\text{F})$$

Multi-Stage Voltage Multipliers

A four-stage dc voltage multiplier is shown in Fig. 3-58. Compared with the voltage doubler in Fig. 3-53, this circuit consists of two cascade-connected voltage-doubling circuits. To simplify the explanation of the circuit operation, assume ideal diodes where $V_F = 0$.

- When $V_i = -E$, D_1 is forward-biased and C_1 charges via D_1 to E .
- When $V_i = +E$, point A is at $+2E$, D_1 is reverse-biased, D_2 is forward-biased, and C_2 charges via D_2 to $2E$.
- When $V_i = -E$, point A is close to ground level, point B is at $2E$ (because of V_{C2}), D_2 is reverse-biased, D_3 is forward-biased, and C_3 charges via D_3 to $2E$ volts.

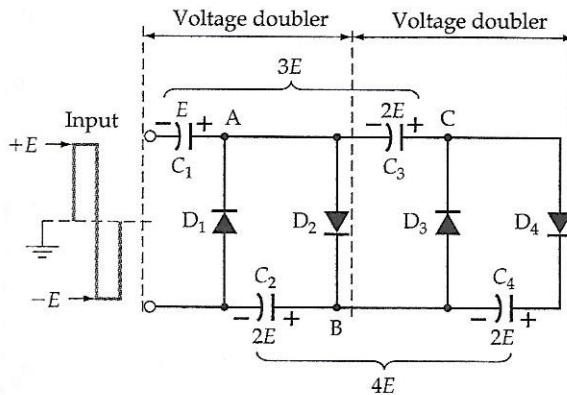


Figure 3-58 Four-stage dc voltage-multiplying circuit. Disregarding the diode voltage drops, C_1 is charged to E volts, and all other capacitors are charged to approximately $2E$. The final output is $4E$ volts.

- When $V_i = +E$, point A is at $+2E$, point B is at $+2E$, point C is at $+4E$ ($V_{C1} + V_{C3}$), D_4 is forward-biased, and C_4 charges via D_4 to $2E$ volts.

The resulting output voltage, taken across C_2 and C_4 , is $4E$ volts as illustrated. Additional stages may be added to the circuit to produce higher levels of dc output voltage. Figure 3-59 shows another way that dc voltage-multi-

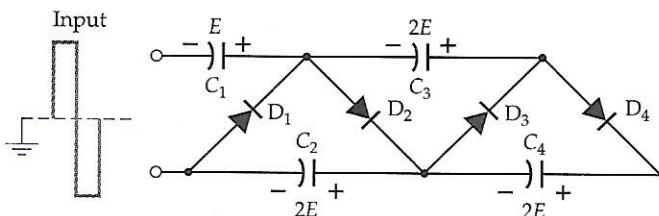


Figure 3-59 Another way of drawing the circuit of a four-stage dc voltage multiplier. The component connections are exactly as in Fig. 3-58.

plier circuit diagrams are often drawn. Examination of the circuit shows that it is exactly the same as Fig. 3-58.

Practice Problems

- 3-11.1** For the circuit designed in Ex. 3-26, determine the effect on the output ripple: (a) when R_L is changed to 27 k Ω , and (b) when the input square-wave frequency is increased to 7 kHz.
- 3-11.2** A voltage-doubling circuit with a 39 k Ω load resistor is to have a 20 V output. Determine the required amplitude for a 700 Hz square wave input, and calculate suitable capacitor values to produce a 0.2 V maximum output ripple. Use silicon diodes.

3-12 DIODE LOGIC CIRCUITS

AND Gate

A logic circuit produces an output voltage that is either high or low, depending upon the levels of several input voltages.

The two basic logic circuits are the AND gate and the OR gate.

Figure 3-60 shows the circuit diagram of a diode AND gate. It is seen that the diode anodes are connected to a 5 V supply (V_{CC}) via resistor R_1 . The circuit has a single output terminal at the diode anodes and three input terminals at the device cathodes. (An AND gate could have any number of inputs from 2 up to perhaps 50.)

If one (or more) of the input terminals is grounded, current flows from the supply through R_1 and through the forward-biased diode to ground. In this case, the output voltage is just V_F above ground (0.7 V for silicon). The output is said to be at a *low* level. When input levels of 5 V are applied to all three

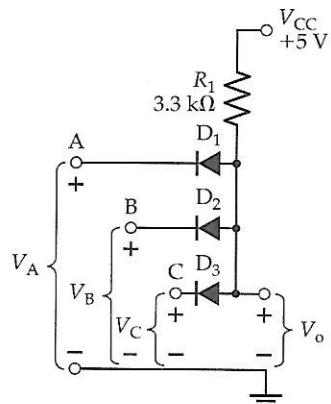


Figure 3-60 Circuit of a three-input diode AND gate. A high output occurs only when high inputs are present at input A, AND input B, AND input C.

input terminals, none of the diodes is forward-biased, no resistor current flows, and no significant voltage drop occurs across R_1 . Thus, the output voltage is equal to V_S , and is referred to as a *high* output level.

An AND gate produces a high output only when input A is high, AND input B is high, AND input C is high.

Example 3-27

For the AND gate circuit in Fig. 3-60, determine each diode forward current level: (a) when all three inputs are *low*; (b) when only input A is *high*; (c) when inputs A and B are both *high* and C is *low*.

Solution

$$(a) I_{R1} = \frac{V_{CC} - V_F}{R_1} = \frac{5\text{ V} - 0.7\text{ V}}{3.3\text{ k}\Omega} = 1.3\text{ mA}$$

For each diode,

$$I_F = \frac{I_{R1}}{3} = \frac{1.3\text{ mA}}{3} = 433\text{ }\mu\text{A}$$

(b) $I_{R1} = 1.3\text{ mA}$ (as above)

$$I_{F2} = I_{F3} = \frac{I_{R1}}{2} = \frac{1.3\text{ mA}}{2} = 650\text{ }\mu\text{A}$$

$$(c) I_{F3} = I_{R1} = 1.3\text{ mA}$$

OR Gate

The circuit diagram of an OR gate with three input terminals is shown in Fig. 3-61. Like the AND gate, the OR gate could have two or more inputs. It is obvious that the output voltage (V_o) of the OR gate in Fig. 3-61 is low when all three inputs are low. Now suppose that a +5 V input is applied to terminal A, while terminals B and C remain grounded. Diode D_1 becomes forward-biased, and its cathode voltage is $V_o = (5\text{ V} - V_F)$. The gate output voltage is $+V_o$ at the cathodes and ground at the

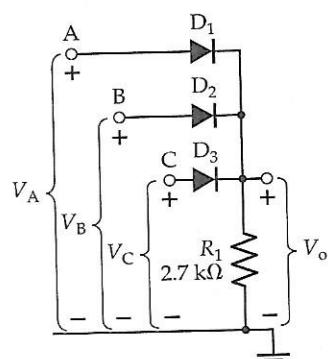


Figure 3-61 Circuit of a three-input OR gate. A high output occurs when high inputs are present at input A, OR at input B, OR at input C.

anodes. The output will be high if a high input voltage is applied to any one (or more) of the inputs.

An OR gate produces a high output when input A is high, OR when input B is high, OR when input C is high.

Diode AND and OR gates can be made with discrete components. However, *integrated-circuit* (IC) packages containing many diodes already fabricated in the form of one or more gates are available.

Practice Problems

- 3-12.1 The diodes in the AND gate in Fig. 3-60 are each to have a 2 mA maximum forward current. Calculate the required resistance for R_1 .
- 3-12.2 Calculate the maximum and minimum levels of diode forward current for the OR gate in Fig. 3-61 when $V_i = 4.5$ V and $R_1 = 2.7$ k Ω .

Review Questions

Section 3-1

- 3-1 Draw the circuit diagram of a half-wave rectifier for producing a positive output voltage. Sketch the input and output waveforms, and explain the circuit operation.
- 3-2 Draw circuit diagrams to show two methods of producing a negative output voltage from a half-wave rectifier. Briefly explain.

Section 3-2

- 3-3 Sketch a two-diode full-wave rectifier circuit for producing a positive output voltage. Sketch the input and output waveforms and explain the circuit operation.
- 3-4 Draw the circuit diagram for a bridge rectifier, together with its input and output waveforms. Carefully explain the operation of the bridge rectifier circuit, identifying the forward-biased and reverse-biased diodes during each half-cycle of the input waveform.
- 3-5 Draw diagrams to show how a negative output voltage can be obtained from:
(a) a two-diode full-wave rectifier circuit, (b) a bridge rectifier circuit. Briefly explain.

Section 3-3

- 3-6 Draw the circuit diagram for a dc power supply that uses a half-wave rectifier and a capacitor filter. Sketch the input and output waveforms, and explain the circuit operation and the shape of the waveforms.
- 3-7 For a rectifier circuit with capacitor filtering, explain ripple voltage, repetitive surge current, non-repetitive surge current, and diode peak reverse voltage.

- 3-8 Discuss the selection of a reservoir capacitor for a dc power supply, and the importance of connecting the capacitor with the correct polarity.
- 3-9 List the factors involved in diode selection for a half-wave rectifier circuit. Briefly explain.
- 3-10 Explain the function of a transformer in a dc power supply, and discuss the factors involved in the specification of power supply transformers.

Section 3-4

- 3-11 Draw the circuit diagram for a dc power supply that uses a bridge rectifier and a capacitor filter circuit. Sketch the input and output waveforms, and explain the circuit operation and the shape of the waveforms.
- 3-12 List the factors involved in diode selection for a full-wave rectifier circuit. Briefly explain.
- 3-13 Compare half-wave and full-wave rectifier circuits with capacitor filtering, referring to capacitor size for a given ripple amplitude, diode specification, and transformer selection.

Section 3-5

- 3-14 Draw the circuit diagram of an $RC\pi$ filter for use with a full-wave rectifier power supply. Sketch typical filter input and output waveforms, and explain how the circuit functions.
- 3-15 Draw the circuit diagram of an $RL\pi$ filter. Explain how the circuit reduces the output ripple voltage, and how it affects the dc output of a rectifier power supply.
- 3-16 Sketch the circuit of an L -input filter, and explain how the filter reduces the ac component of the rectifier output voltage. Also, discuss how the filter affects the power supply dc output voltage.

Section 3-6

- 3-17 Define power supply source effect, load effect, line regulation, and load regulation. Write equations for each item.
- 3-18 Sketch a circuit diagram for testing a dc power supply for source effect, load effect, and ripple. List the steps in an appropriate test procedure and discuss any necessary precautions.
- 3-19 List possible faults that might occur in a dc power supply, and discuss the actions that should be taken.

Section 3-7

- 3-20 Sketch the circuit diagram for a Zener diode voltage regulator. Briefly explain the circuit operation and discuss the effects of load current.
- 3-21 Sketch the ac equivalent circuit for a Zener diode voltage regulator. Write equations for source effect and load effect.

Section 3-8

- 3-22 Draw circuit diagrams for negative and positive series clipping circuits. Show input and output waveforms and explain the operation of each circuit.

- 3-23 Sketch the circuit of a diode series noise clipper. Sketch input and output waveforms and explain the circuit operation.

Section 3-9

- 3-24 Draw circuit diagrams for negative and positive shunt clipping circuits. Sketch input and output waveforms and explain the operation of each circuit.
- 3-25 Sketch a shunt noise clipping circuit. Sketch input and output waveforms and explain the circuit operation.
- 3-26 Draw a biased shunt clipping circuit. Sketch input and output waveforms and explain the circuit operation.
- 3-27 A biased shunt clipper has ± 9 V bias voltages. Sketch the output waveform produced by a ± 12 V square wave input.
- 3-28 Draw a diagram for a Zener diode shunt clipping circuit together with input and output waveforms. Explain the circuit operation.

Section 3-10

- 3-29 Explain the difference between clipping circuits and clamping circuits. A positive voltage clamping circuit and a positive shunt clipping circuit each have a ± 12 V square wave input. Sketch the output waveform from each circuit.
- 3-30 Draw circuit diagrams for negative and positive voltage clamping circuits. Show input and output waveforms and explain the operation of each circuit.
- 3-31 Draw a circuit diagram for a voltage clamping circuit using a positive bias voltage. Sketch the output waveforms and explain the circuit operation.
- 3-32 Draw a circuit diagram for a voltage clamping circuit using a Zener diode in place of a positive bias voltage. Sketch the output waveforms and explain the circuit operation.

Section 3-11

- 3-33 Draw a voltage doubling circuit. Sketch input and output waveforms and explain the circuit operation.
- 3-34 Draw the circuit diagram for a four-stage voltage-multiplier circuit. Briefly explain its operation, and identify the output terminals and the output voltage level relative to the input. Show how two additional diode-capacitor circuits may be added, and estimate the new output-to-input voltage ratio.

Section 3-12

- 3-35 Sketch the circuit diagram for a diode AND gate with five input terminals. Briefly explain the circuit operation.
- 3-36 Sketch the circuit diagram for a diode OR gate with five input terminals. Briefly explain the circuit operation.

Problems

Section 3-1

- 3-1 A half-wave rectifier circuit has a 25 V (rms) sinusoidal ac input and a $600\ \Omega$ load resistance. Calculate the peak output voltage, peak load current, and diode peak reverse voltage. Assume that $V_F = 0.7$ V.

- 3-2** A half-wave rectifier circuit produces a 55 mA peak current in an $820\ \Omega$ load resistor. Calculate the rms ac input voltage and the diode peak reverse voltage if $V_F = 0.7\text{ V}$.
- 3-3** Calculate the power dissipated in a $560\ \Omega$ load resistor connected to the output of a half-wave rectifier circuit. The ac input is 25 V (rms), and the diode voltage drop is 0.7 V.

Section 3-2

- 3-4** A $470\ \Omega$ load resistor is connected at the output of a bridge rectifier circuit that has a 15 V (rms) input. Calculate the peak output voltage, peak load current, and load power dissipation. Assume the diodes have 0.3 V forward voltage drop.
- 3-5** A bridge rectifier circuit has a 25 V (rms) sinusoidal ac input and a $600\ \Omega$ load resistance. Calculate the peak output voltage, peak load current, diode power dissipation, and diode peak reverse voltage. Assume the diodes have a V_F of 0.7 V.
- 3-6** A two-diode full-wave rectifier circuit (as in Fig. 3-3) dissipates 640 mW in a $400\ \Omega$ load resistor. If the diodes are silicon, calculate the peak output voltage from each half of the transformer secondary.

Section 3-3

- 3-7** A dc power supply consisting of a half-wave rectifier and a reservoir capacitor is required to supply 24 V with a 200 mA maximum load current. The output ripple is not to exceed $\pm 500\text{ mV}$, and the ac input frequency is 60 Hz. Determine a suitable capacitance for the reservoir capacitor.
- 3-8** Recalculate the capacitance approximately for the circuit in Problem 3-7, assuming that the capacitor discharge time is much greater than the charge time.
- 3-9** Specify the diodes required for the half-wave rectifier circuit in Problem 3-7. Select a suitable device from Appendix A, and calculate the required surge limiting resistance.
- 3-10** Specify a suitable transformer for the power supply in Problem 3-7.
- 3-11** Calculate the reservoir capacitance for a half-wave rectifier dc power supply which produces a 15 V output with a 300 mA maximum load current. The peak-to-peak output ripple voltage is to be a maximum of $\pm 10\%$ of V_o , and the ac input frequency is 60 Hz.
- 3-12** Specify the diodes required for the power supply in Problem 3-11. Select a suitable device from Appendix A, and calculate the required surge-limiting resistance.
- 3-13** Specify a suitable transformer for the power supply in Problem 3-11.
- 3-14** Recalculate the capacitance for the power supply described in Problem 3-11 if the ac input frequency is to be 400 Hz.

Section 3-4

- 3-15** A dc power supply consisting of a bridge rectifier circuit and a reservoir capacitor is to supply 24 V with a 200 mA maximum load current. The output ripple is not to exceed $\pm 500\text{ mV}$, and the ac input frequency is 60 Hz. Determine a suitable capacitance for the reservoir capacitor.

- 3-16** Recalculate the capacitance for the circuit in Problem 3-15, using the approximation that the capacitor discharge time is much greater than the charge time.
- 3-17** Specify the diodes required for the rectifier circuit in Problem 3-15. Select a suitable device from Appendix A, and calculate the required surge limiting resistance.
- 3-18** Specify a suitable transformer for the power supply in Problem 3-15.
- 3-19** Calculate the reservoir capacitance for a dc power supply which produces an 18 V output with a 300 mA maximum load current. A bridge rectifier circuit is used, and the ac input frequency is 60 Hz. The peak-to-peak output ripple voltage is to be a maximum of $\pm 10\%$ of V_o .
- 3-20** Specify the diodes required for the power supply in Problem 3-19. Select a suitable device from Appendix A, and calculate the required surge limiting resistance.
- 3-21** Recalculate the capacitance for the power supply in Problem 3-19 for a 400 Hz ac supply.
- 3-22** Specify a suitable transformer for the power supply in Problem 3-19.

Section 3-5

- 3-23** A dc power supply consists of a full-wave rectifier with a 200 μF reservoir capacitor (C_1). The rectifier peak output is 30 V, and the (sawtooth) ripple voltage is 5 V peak-to-peak when the load current is 120 mA. A resistor $R_1 = 15 \Omega$ and a capacitor $C_2 = C_1 = 200 \mu\text{F}$ are connected to C_1 to create an $RC \pi$ filter. Calculate the output voltage and ripple amplitude.
- 3-24** A full-wave rectifier power supply with a 200 μF reservoir capacitor has $V_{o(\text{dc})} = 45 \text{ V}$ and $V_{r(p-p)} = 8 \text{ V}$ when the load current is 190 mA. A resistor and capacitor (R_1 and C_1) are to be added to the circuit to reduce the ripple voltage by a factor of 4. Allowing a 3 V dc drop across R_1 , determine suitable component values.
- 3-25** A dc power supply using full-wave rectification is to be designed to produce a 25 V, 60 mA output with a 200 mV (p-p) ripple. The circuit is to use an $LC \pi$ filter, and the input ripple to the filter is to be 3 V (p-p). Determine suitable component values for the filter, and calculate the required peak output voltage from the rectifiers. Assume that the inductor has a 10 Ω winding resistance.
- 3-26** An $LC \pi$ filter has $C_1 = C_2 = 220 \mu\text{F}$, and $L_1 = 300 \text{ mH}$ with $R_W = 6 \Omega$. Determine the dc output voltage and ripple amplitude when the load current is 75 mA, and the full-wave rectifier supply has $E_{o(\text{max})} = 33 \text{ V}$.
- 3-27** Capacitor C_1 in the circuit in Problem 3-26 is removed and reconnected in parallel with C_2 , so that the filter becomes an L -input type. Calculate the dc output voltage and the peak output ripple voltage.
- 3-28** A dc power supply using full-wave rectification is to be designed to produce a 25 V, 60 mA output with a 200 mV (p-p) ripple, as in Problem 3-25. Calculate the critical inductance for an L -input filter, and determine a suitable output capacitor value. Also, determine the required peak output voltage from the rectifiers.

Section 3-6

- 3-29 A dc power supply output voltage changes from 12 V to 11.6 V when the input drops by 10%, and from 12 V to 11.5 V when the load current increases from zero to maximum. Determine the source and load effects and the line and load regulations.
- 3-30 A dc power supply with a 20 V output has a 3% line regulation and a 5% load regulation. Calculate the source effect and the load effect.
- 3-31 Calculate the line and load regulation for the dc power supply circuit designed for Problem 3-7.
- 3-32 Calculate the line and load regulation for the dc power supply circuit designed for Problem 3-19.

Section 3-7

- 3-33 A series-connected Zener diode and resistor are to be used as a 10 V reference source with a load current less than 1 mA. The available supply voltage is 25 V. Select suitable components and calculate the effect of a $\pm 10\%$ change in supply voltage on the diode current.
- 3-34 A 5 V Zener diode voltage source is to be designed to produce maximum possible output current from a low-power Zener diode. Design the circuit to operate from a 22 V supply, and calculate the maximum load current.
- 3-35 Determine the source effect, load effect, and ripple rejection for the circuit designed for Problem 3-34.
- 3-36 Recalculate the maximum output current for the circuit designed for Problem 3-34 when the ambient temperature is raised to 100°C . The diode derating factor is $3.2 \text{ mW}/^\circ\text{C}$ for temperatures above 50°C .
- 3-37 A 1N751 Zener diode is connected in series with a 330Ω resistor to a 25 V supply. Determine the maximum and minimum level of the Zener diode voltage, and calculate the minimum resistance that may be connected in parallel with the diode.
- 3-38 Calculate the source effect, load effect, and ripple rejection for the circuit in Problem 3-37.

Section 3-8

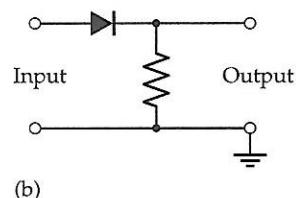
- 3-39 A diode-resistor negative series clipping circuit (as in Fig. 3-36a) has a $\pm 12 \text{ V}$ input and zero load current. Determine a suitable resistor value and specify the diode.
- 3-40 A device is to be protected from the negative half-cycle of a $\pm 8 \text{ V}$ square wave input. The device input current is $50 \mu\text{A}$ when the input is positive. Select a suitable clipping circuit, determine an appropriate resistor, and specify the diode.
- 3-41 Specify the diodes for the series noise clipper circuit in Fig. 3-38 if $R_1 = 270 \Omega$ and the input peaks are $\pm 7 \text{ V}$.

Section 3-9

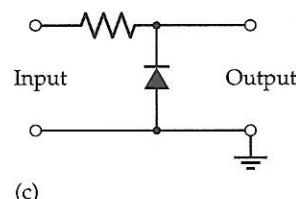
- 3-42** A positive shunt clipping circuit (as in Fig. 3-39a) with a ± 10 V input is to produce a -9 V output when the load current is $500 \mu\text{A}$. Determine a suitable resistor value and specify the diode.
- 3-43** A device is to be protected from the negative half-cycle of a ± 6 V square wave input. The device current is $750 \mu\text{A}$ when its input is $+4$ V. Select a suitable shunt clipping circuit, determine an appropriate resistor, and specify the diode.
- 3-44** Specify the diodes for the shunt noise clipper circuit in Fig. 3-41 if $R_1 = 470 \Omega$ and the input peaks are ± 5 V.
- 3-45** A ± 12 V square wave is applied to a circuit that cannot accept inputs in excess of ± 4 V. The circuit input current is $\pm 100 \mu\text{A}$. Design a suitable biased shunt clipping circuit.
- 3-46** Design a Zener diode shunt clipping circuit to satisfy the requirements in Problem 3-45.
- 3-47** A Zener diode shunt clipping circuit with a ± 15 V input is to have a maximum output of ± 9 V with an output current of $\pm 750 \mu\text{A}$. Design the circuit.
- 3-48** A biased shunt clipper circuit is to produce a maximum output of ± 6 V to a $10 \text{ k}\Omega$ load. The input voltage peaks can be as high as ± 11 V. Design the circuit.
- 3-49** Design a Zener diode shunt clipping circuit to satisfy the requirements in Problem 3-48.
- 3-50** Sketch the output waveforms from each of the circuits in Fig. 3-62 when a ± 8 V square wave is applied at the input.

Section 3-10

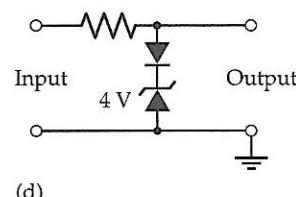
- 3-51** A positive voltage-clamping circuit (as in Fig. 3-45) has $C_1 = 2 \mu\text{F}$ and $R_1 = 27 \text{ k}\Omega$. Determine the tilt on the output when a ± 5 V, 700 Hz square wave input is applied.
- 3-52** A negative voltage clamping circuit has a ± 9 V, 1 kHz square wave input with a 500Ω source resistance. The slope on the output waveform is not to exceed 0.5% . Determine suitable resistance and capacitance values.
- 3-53** A biased clamping circuit (as in Fig. 3-50) has a ± 12 V, 330 Hz sine wave input with a 600Ω



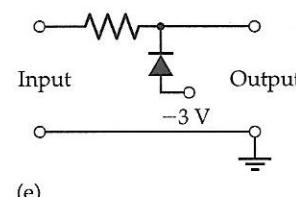
(b)



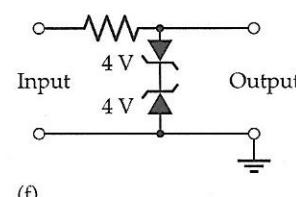
(d)



(e)



(f)

**Figure 3-62** Diode clipping circuits for Problem 3-50.

source resistance. The positive output peak is to be clamped at 5 V, and the slope between peaks is not to exceed 1%. Determine the required bias voltage and suitable resistance and capacitance values.

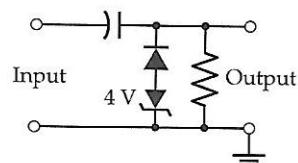
- 3-54** Design a Zener diode clamping circuit that will perform as specified in Problem 3-53.
- 3-55** A Zener diode clamping circuit, as in Fig. 3-53, uses a germanium diode and a 1N746 Zener diode. The input voltage is a ± 8 V, 1 kHz square wave. Determine the output voltage levels, and calculate the capacitor voltage.
- 3-56** Sketch the output waveforms from each of the circuits in Fig. 3-63 when a ± 15 V square wave is applied at the input.
- 3-57** A ± 20 V, 700 Hz square wave with a 500Ω source resistance is to be clamped to a maximum level of approximately 12 V. Design a suitable Zener diode circuit that will produce a maximum output tilt of 3%.

Section 3-11

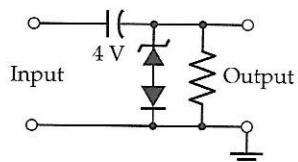
- 3-58** A voltage doubling circuit is to be designed to produce an output of 25 V to a $56 \text{ k}\Omega$ resistor. Determine the required amplitude for a 1 kHz square wave input; calculate suitable capacitor values if the output ripple is to be a maximum of 0.5 V.
- 3-59** A voltage doubling circuit with a ± 10 V, 2 kHz square wave input has a $33 \text{ k}\Omega$ load resistance. Determine suitable capacitance values to give a 1% maximum output ripple.
- 3-60** Refer to the voltage doubling circuit designed for Problem 3-58. Determine the effect of (a) changing R_L to $33 \text{ k}\Omega$, (b) changing the input frequency to 1.5 kHz.

Section 3-12

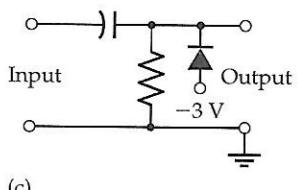
- 3-61** A three-input diode AND gate, as in Fig. 3-60, is to have a minimum diode current of 1 mA. If the circuit supply voltage is 9 V, determine a suitable resistance for R_1 .
- 3-62** A five-input diode OR gate used diodes that require a $500 \mu\text{A}$ minimum forward current. Determine a suitable resistance value if the input voltages are $+5$ V.



(a)



(b)



(c)

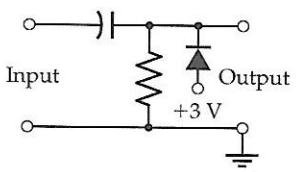


Figure 3-63 Diode clamping circuits for Problem 3-56.

Practice Problem Answers

- 3-1.1** 20.51 V, 62.2 mA, 21.2 V
3-1.2 33.95 V, 48.7 V
3-2.1 32.54 V, 69.2 mA, 1.12 V
3-2.2 238 mW, 13.7 V
3-3.1 1000 μ F
3-3.2 835 μ F
3-3.3 25.2 V, 60 mA, 860 mA, 1N4001, 0.42 Ω ,
(115 V, 17.7 mA), (9.5 V, 216 mA)
3-4.1 500 μ F
3-4.2 557 μ F
3-4.3 17.5 V, 100 mA, 714 mA, 1N4001, 0.57 Ω
(115 V, 16.8 mA), (12.1 V, 160 mA)
3-5.1 18.15 V, 126 mV
3-5.2 19 V, 17 mV
3-5.3 12.6 V, 147 mV
3-6.1 50 mV, 100 mV, 0.33%, 0.66%
3-7.1 1N756, 680 Ω , 14.7 mA
3-7.2 1N756, (220 Ω + 22 Ω), 43.8 mA
3-7.3 61.4 mV, 336 mV, 3.07×10^{-2}
3-8.1 5.6 k Ω , 7 V, 1 mA
3-8.2 4.7 k Ω , 6 V, 1 mA
3-9.1 330 Ω , 7 V, 19 mA
3-9.2 ± 2.8 V, 2.7 k Ω
3-9.3 1N753, 1.8 k Ω
3-10.1 550 mV
3-10.2 1 μ F, 100 k Ω
3-10.3 7.5 V, -16.5 V, 4.5 V
3-11.1 1.6%, 0.65%
3-11.2 ± 10.7 V, 3.9 μ F, 8 μ F
3-12.1 680 Ω
3-12.2 1.41 mA, 469 μ A