

RCET 2251

Systems Analog & Digital Theory

Advanced Review Copy

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Chapter 1

Oscilloscope & Test Equipment Familiarization

1.1 Objectives

Review Bench Equipment Specifications, General Operation, and Test and Measurement Procedures as Identified in the Operator's Manual.

1. **Equipment Specifications:** Students should be able to review and understand the specifications of bench equipment, including details such as voltage ranges, current limits, frequency response, and other relevant parameters as outlined in the operator's manual.
2. **General Operation:** Gain knowledge of the general operation principles of bench equipment, understanding functions, controls, and interface features described in the operator's manual.
3. **Test and Measurement Procedures:** Familiarize themselves with the recommended test and measurement procedures provided in the operator's manual for various bench equipment. This includes understanding how to perform accurate measurements, set appropriate parameters, and interpret results.

By achieving this theory objective, students will develop a solid theoretical foundation regarding the specifications, operation, and testing procedures for bench equipment. This knowledge is crucial for the effective and accurate utilization of the equipment in practical applications.

1.2 Reference Documents:

Tektronix XYZs of Oscilloscopes PDF [1]

Tektronix TDS Oscilloscope User Manual PDF [2]

Tektronix AFG1022 Arbitrary/Function Generator Quick Start User Manual PDF [3]

Power Supply GPS-4303 User Manual PDF [4]

Tektronix - Get more from your basic oscilloscope with the FFT function [5]

1.3 Tektronix XYZs of Oscilloscopes Part I

Review the Tektronix XYZs of Oscilloscopes and answer the following section questions:

1.3.1 Match the following:

- | | | |
|--|---|--|
| 1. <input type="checkbox"/> Acquisition | 7. <input type="checkbox"/> Period | 13. <input type="checkbox"/> Digital Storage |
| 2. <input type="checkbox"/> Analog | 8. <input type="checkbox"/> Phase | 14. <input type="checkbox"/> Time Base |
| 3. <input type="checkbox"/> Bandwidth | 9. <input type="checkbox"/> Pulse | 15. <input type="checkbox"/> Transient |
| 4. <input type="checkbox"/> Digital Phosphor | 10. <input type="checkbox"/> Waveform Point | 16. <input type="checkbox"/> ADC Resolution |
| 5. <input type="checkbox"/> Frequency | 11. <input type="checkbox"/> Rise Time | 17. <input type="checkbox"/> Volt |
| 6. <input type="checkbox"/> Glitch | 12. <input type="checkbox"/> Sample Point | |

- A The unit of electric potential difference.
- B A performance measurement indicating the precision of an ADC, measured in bits.
- C Term used when referring to degree points of a signal's period.
- D The number of times a signal repeats in one second.
- E The amount of time it takes a wave to complete one cycle.
- F A stored digital value that represents the voltage of a signal at a specific point in time on the display.
- G A common waveform shape that has a rising edge, a width, and a falling edge.
- H A performance measurement indicating the rising edge speed of a pulse.
- I Oscilloscope circuitry that controls the timing of the sweep.

- J An intermittent spike in a circuit.
- K A signal measured by an oscilloscope that only occurs once.
- L The oscilloscope's process of collecting sample points from the ADC, processing them, and storing them in memory.
- M Something that operates with continuously changing values.
- N Digital oscilloscope that captures 3 dimensions of signal information in real-time.
- O Digital oscilloscope with serial processing.
- P A sine wave frequency range, defined by the -3dB point.
- Q The raw data from an ADC used to calculate and display waveform points.

1.3.2 Multiple Choice:

1. With an oscilloscope you can:
 - (a) Calculate the frequency of a signal.
 - (b) Find malfunctioning electrical components.
 - (c) Analyze signal details.
 - (d) All the above.
2. The difference between analog and digitizing oscilloscopes is:
 - (a) Analog oscilloscopes do not have on-screen menus.
 - (b) Analog oscilloscopes apply a measurement voltage directly to the display system, while digital oscilloscopes first convert the voltage into digital values.
 - (c) Analog oscilloscopes measure analogs, whereas digitized oscilloscopes measure digits.
 - (d) Analog oscilloscopes do not have an acquisition system.
3. An oscilloscope's vertical section does the following:
 - (a) Acquires sample points with an ADC.
 - (b) Starts a horizontal sweep.
 - (c) Lets you adjust the brightness of the display.
 - (d) Attenuates or amplifies the input signal.
4. The time base control of the oscilloscope does the following:
 - (a) Adjusts the vertical scale.
 - (b) Shows you the current time of day.

- (c) Sets the amount of time represented by the horizontal width of the screen.
 - (d) Sends a clock pulse to the probe.
5. On an oscilloscope display:
- (a) Voltage is on the vertical axis and time is on the horizontal axis.
 - (b) A straight diagonal trace means voltage is changing at a steady rate.
 - (c) A flat horizontal trace means voltage is constant.
 - (d) All the above.
6. All repeating waves have the following properties:
- (a) A frequency measured in Hertz.
 - (b) A period measured in seconds.
 - (c) a bandwidth measured in Hertz.
 - (d) All the above.
7. If you probe inside a computer with an oscilloscope, you are likely to find the following types of signals:
- (a) Pulse trains.
 - (b) Ramp waves.
 - (c) Sine waves.
 - (d) All the above.
8. When evaluating the performance of an analog oscilloscope, some things you might consider are:
- (a) The bandwidth.
 - (b) The vertical sensitivity.
 - (c) The ADC resolution.
 - (d) The sweep speed.
9. The difference between digital storage oscilloscopes (DSO) and digital phosphor oscilloscopes (DPO) is:
- (a) The DSO has a higher bandwidth.
 - (b) The DPO captures three dimensions of waveform information in real-time.
 - (c) The DSO has a color display.
 - (d) The DSO captures more signal details.

1.4 Tektronix XYZs of Oscilloscopes Part II

Review the Tektronix XYZs of Oscilloscopes and answer the following section questions:

1.4.1 Match the following:

- | | | |
|---|---|---|
| 1. <input type="checkbox"/> Averaging Mode | 5. <input type="checkbox"/> Earth Ground | 9. <input type="checkbox"/> Real Time |
| 2. <input type="checkbox"/> Circuit Loading | 6. <input type="checkbox"/> Equivalent-Time | 10. <input type="checkbox"/> Signal Generator |
| 3. <input type="checkbox"/> Compensation | 7. <input type="checkbox"/> Graticule | 11. <input type="checkbox"/> Single Sweep |
| 4. <input type="checkbox"/> Coupling | 8. <input type="checkbox"/> Interpolation | 12. <input type="checkbox"/> Sensor |

- A The unintentional interaction of the probe and oscilloscope with the circuit being tested which distorts a signal.
- B A conductor that connects electrical currents to the Earth.
- C A sampling mode in which the digital oscilloscope collects as many samples as it can as the signal occurs, then constructs a display, using interpolation if necessary.
- D A sampling mode in which the digital oscilloscope constructs a picture of a repetitive signal by capturing a little bit of information from each repetition.
- E A device that converts a specific physical quantity such as sound, pressure, strain, or light intensity into an electrical signal.
- F A test device for injecting a signal into a circuit input.
- G A processing technique used by digital oscilloscopes to eliminate noise in a displayed signal.
- H The method of connecting two circuits together.
- I A "connect-the-dots" processing technique to estimate what a fast waveform looks like based on only a few sampled points.
- J The grid lines on a screen for measuring oscilloscope traces.
- K A trigger mode that triggers the sweep once, must be reset to accept another trigger event.
- L A probe adjustment for 10X attenuator probes that balances the electrical properties of the probe with the electrical properties of the oscilloscope.

1.4.2 Multiple Choice:

1. To operate an oscilloscope safely, you should:
 - (a) Ground the oscilloscope with the proper three-pronged power cord.
 - (b) Learn to recognize potentially dangerous electrical components.
 - (c) Avoid touching exposed connections in a circuit being tested even if the power is off.
 - (d) All the above.
2. Grounding an oscilloscope is necessary:
 - (a) For safety reasons.
 - (b) To provide a reference point for making measurements.
 - (c) To align the trace with the screen's horizontal axis.
 - (d) All the above.
3. Circuit loading is caused by:
 - (a) An input signal having too large a voltage.
 - (b) The probe and oscilloscope interacting with the circuit being tested.
 - (c) a 10X attenuator probe being uncompensated.
 - (d) Putting too much weight on a circuit.
4. Compensating a probe is necessary to:
 - (a) Balance the electrical properties of the 10X attenuator probe with the oscilloscope.
 - (b) Prevent damaging the circuit being tested.
 - (c) Improve the accuracy of your measurements.
 - (d) All the above.
5. The trace rotation control is useful for:
 - (a) Scaling waveforms on the screen.
 - (b) Detecting sine wave signals.
 - (c) Aligning the waveform trace with the screen's horizontal axis on an analog oscilloscope.
 - (d) Measuring pulse width.

6. The volts per division control is used to:(select all that apply)
- Scale a waveform vertically.
 - Position a waveform vertically.
 - Attenuate or amplify an input signal.
 - Set the number of volts each division represents.
7. Setting the vertical input coupling to ground does the following:
- Disconnects the input signal from the oscilloscope.
 - Causes a horizontal line to appear with auto trigger.
 - Lets you see where zero volts is on the screen.
 - All the above.
8. The trigger is necessary to:
- Stabilize repeating waveforms on the screen.
 - Capture single-shot waveforms.
 - Mark a particular point of an acquisition.
 - All the above.
9. The difference between auto and normal trigger mode is:
- In normal mode the oscilloscope only sweeps once and then stops.
 - In normal mode the oscilloscope only sweeps if the input signal reaches the trigger point; otherwise the screen is blank.
 - Auto mode makes the oscilloscope sweep continuously even without being triggered.
 - All the above.
10. The acquisition mode that best reduces noise in a repeating signal is:
- Sample mode.
 - Peak detect mode.
 - Envelope mode.
 - Averaging mode.

11. The two most basic measurements you can make with an oscilloscope are:
 - Time and frequency measurements.
 - Time and voltage measurements.
 - Voltage and pulse width measurements.
 - Pulse width and phase shift measurements.
12. If the volts/division is set at 0.5, the largest signal that can fit on the screen (assuming an 8 x 10 division screen) is:
 - 62.5 millivolts peak-to-peak.
 - 8 volts peak-to-peak.
 - 4 volts peak-to-peak.
 - 0.5 volts peak-to-peak.
13. If the seconds/division is set at 0.1 ms, the amount of time represented by the width of the screen is:
 - 0.1 ms.
 - 1 ms.
 - 1 second.
 - 0.1 kHz.
14. By convention, pulse width is measured:
 - At 10% of the pulse's peak-to-peak (pk-pk) voltage.
 - At 50% of the pulse's peak-to-peak (pk-pk) voltage.
 - At 90% of the pulse's peak-to-peak (pk-pk) voltage.
 - At 10% and 90% of the pulse's peak-to-peak (pk-pk) voltage.
15. You attach a probe to your test circuit but the screen is blank. You should:
 - Check that the screen intensity is turned up.
 - Check that the oscilloscope is set to display the channel that the probe is connected to.
 - Set the trigger mode to auto since norm mode blanks the screen.
 - Set the vertical input coupling to AC and set the volts/division to its largest value since a large DC signal may go off the top or bottom of the screen.
 - Check that the probe isn't shorted and make sure it is properly grounded.
 - Check that the oscilloscope is set to trigger on the input channel you are using.
 - All of the above.

1.5 Probe Compensation

Review the Tektronix XYs of Oscilloscopes and answer the following section questions:



Figure 1.1: Probe Adjustment Signal

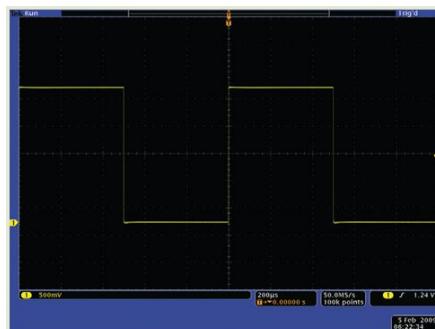


Figure 1.2: Probe Adjustment Signal

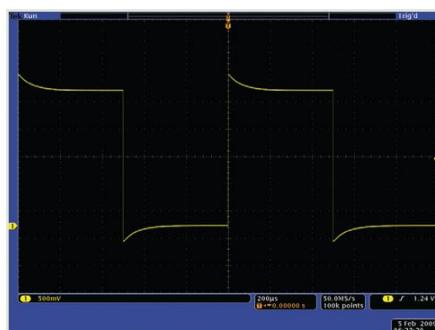


Figure 1.3: Probe Adjustment Signal

1. The Probe Adjustment Signal as seen in **Figure 1.1** represents a:
 - under-compensated probe.
 - properly compensated probe.
 - over-compensated probe.

2. The Probe Adjustment Signal as seen in **Figure 1.2** represents a:
 - under-compensated probe.
 - properly compensated probe.
 - over-compensated probe.

3. The Probe Adjustment Signal as seen in **Figure 1.3** represents a:
 - under-compensated probe.
 - properly compensated probe.
 - over-compensated probe.

1.6 AFG1022

Review the Tektronix AFG1022 Quick Start User Manual and answer the following section questions:

1. The AFG1022 can produce which of the following waveforms:

- Sine
- Square
- Ramp
- Pulse
- Noise

2. The Output impedance of the AFG1022 is _____.

- 50Ω
- 600Ω
- 1KΩ
- 1MΩ
- 10MΩ

3. Push the front-panel _____ button to control the screen display. You can toggle between the two channels.

- On/Off
- Both
- Ch1
- Ch2
- Ch1/2

4. To enable CH1 signal output, push the front-panel On/Off with _____ color.

- Red
- Green
- Blue
- Yellow

5. To enable CH2 signal output, push the front-panel On/Off with _____ color.
- Red
 - Green
 - Blue
 - Yellow
6. The Sweep outputs a waveform with the output signal frequency varying _____ or _____ .
- continuously, non-continuously
 - linearly, logarithmically
 - synchronized, non-synchronized
 - sweep, digital pulse sweep
7. According to the AFG1022 Quick Start User Manual, What fuse should be used?
- 250,F0.5AL
 - 250,F1AL
 - 250,F1.5AL
 - 250,F2AL

Chapter 2

RC Circuits

2.1 Objectives:

Understand and Identify Different Types and Characteristics of Waveforms.

- Students should be able to identify and understand different types of waveforms, including periodic and aperiod waveforms.

Understand Pulse Waveform Terminology and Formulas.

- Develop a solid understanding of pulse waveform terminology, including Period, Pulse Width, Pulse Space, Pulse Repetition Frequency, Duty Cycle, Tilt, Rise Time, Average Pulse Amplitude, Average Waveform Voltage, Capacitor Charge, Cycles to Stabilization, V_{Max} , and V_{Min} .

Understand Frequency Synthesis and the Process of Combining Sine Waves.

- Gain insight into the process of combining sine waves to produce complex waveforms. Understand the principles of frequency synthesis and its application.

Calculate Critical Frequencies using Tilt and Rise Time.

- Develop the ability to calculate critical frequencies using tilt and rise time measurements. Understand how series and parallel capacitance influence these parameters and the critical frequencies.

Identify Capacitor Charge Percentage in Terms of Time and τ .

- Students should be able to identify and calculate capacitor charge percentages concerning time and the time constant (τ) in RC circuits.

Calculate and Predict Waveforms for RC Integration Circuits

- Develop a comprehensive understanding of RC Integration circuits. Gain proficiency in calculating and predicting output waveforms for these circuits.

Calculate and Predict Waveforms for RC Differentiation Circuits

- Develop a comprehensive understanding of RC Differentiation circuits. Gain proficiency in calculating and predicting output waveforms for these circuits.

By achieving these objectives, students will acquire a deep understanding of waveform characteristics, pulse waveform terminology, frequency synthesis, critical frequencies, capacitor charge calculations, and the principles behind RC integration, differentiation, and sine wave analysis. These objectives aim to enhance their knowledge and proficiency in working with various waveforms and circuits.

2.2 References:

- Solid State Pulse Circuits [6]

2.3 Graphs and Waveforms

2.3.1 What is a Graph?

- **Horizontal Axis (X-Axis):** This axis runs horizontally from left to right and is usually used to represent the independent variable or input.
- **Vertical Axis (Y-Axis):** This axis runs vertically from bottom to top and is usually used to represent the dependent variable or output.
- The point where the two axes intersect is called the **Origin**. The coordinates of the origin are typically represented as (0,0). The horizontal and vertical distances from the origin to any point on the graph are called the x-coordinate and y-coordinate, respectively. The combination of these coordinates uniquely identifies a point in the coordinate system. This system is fundamental in graphing and visualizing mathematical functions and relationships.

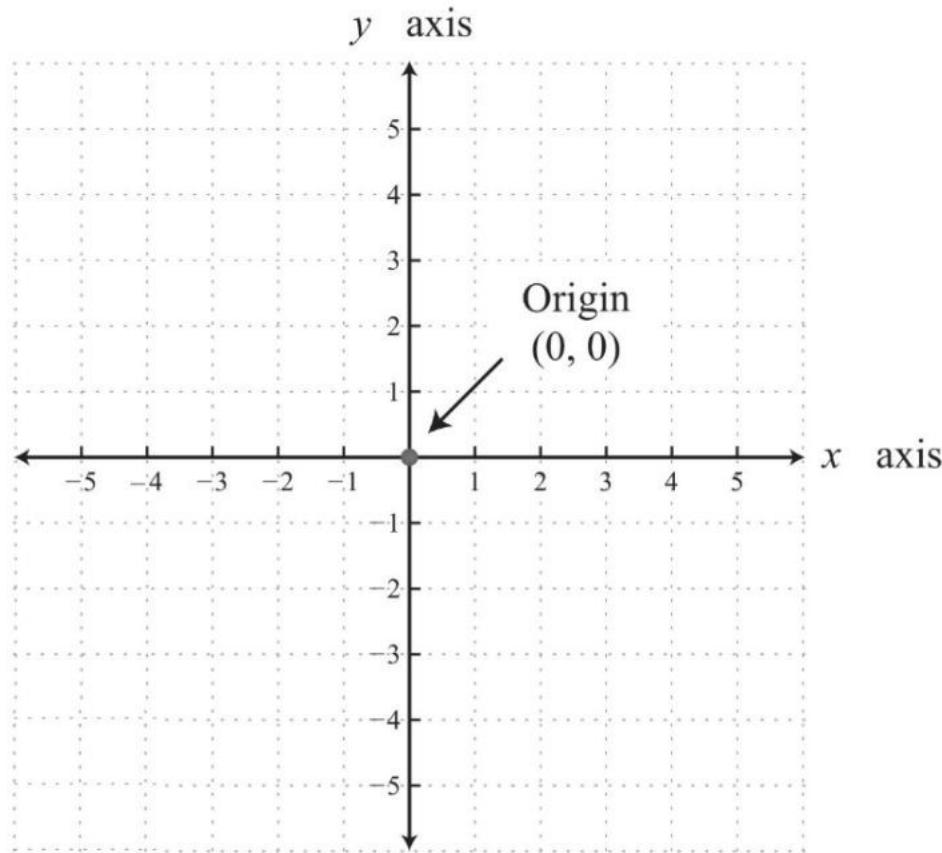


Figure 2.1: Graph

2.3.2 Periodic Waveforms

A **periodic waveform** is a type of waveform that repeats its shape over regular intervals of time. In other words, the waveform exhibits a regular and predictable pattern, and the pattern repeats itself after a specific period. The time it takes for one complete cycle to occur is called the period.

Key characteristics of periodic waveforms include:

1. **Frequency (f):** The frequency of a periodic waveform is the number of cycles that occur in one second. It is the reciprocal of the period and is measured in Hertz (Hz).

$$\text{Frequency} = \frac{1}{\text{Time}}$$

2. **Amplitude:** The amplitude of a periodic waveform represents the maximum displacement from the equilibrium position. It is a measure of the strength or intensity of the waveform. Amplitude is typically measured in *volts peak* or *volts peak to peak* using an oscilloscope.

3. **Phase:** The phase of a periodic waveform indicates the relative position of the waveform at a specific point in time within its cycle. It is often measured in degrees or radians.

Common examples of periodic waveforms include:

- **Sine Wave:** A smooth, oscillating waveform characterized by its sinusoidal shape.
- **Square Wave:** A waveform that alternates between two constant levels, resembling a square shape.
- **Triangular Wave:** A waveform that linearly increases and decreases in amplitude, forming a triangular shape.
- **Ramp Wave:** A waveform characterized by a linear increase or decrease in amplitude over time.
- **Sawtooth Wave:** A waveform that rises linearly and then falls abruptly, creating a sawtooth-like pattern.
- **Exponential Wave:** A waveform in which the amplitude changes exponentially over time.
- **Spike Wave:** A waveform characterized by a sudden, brief increase in amplitude, often appearing as a sharp spike in the signal.

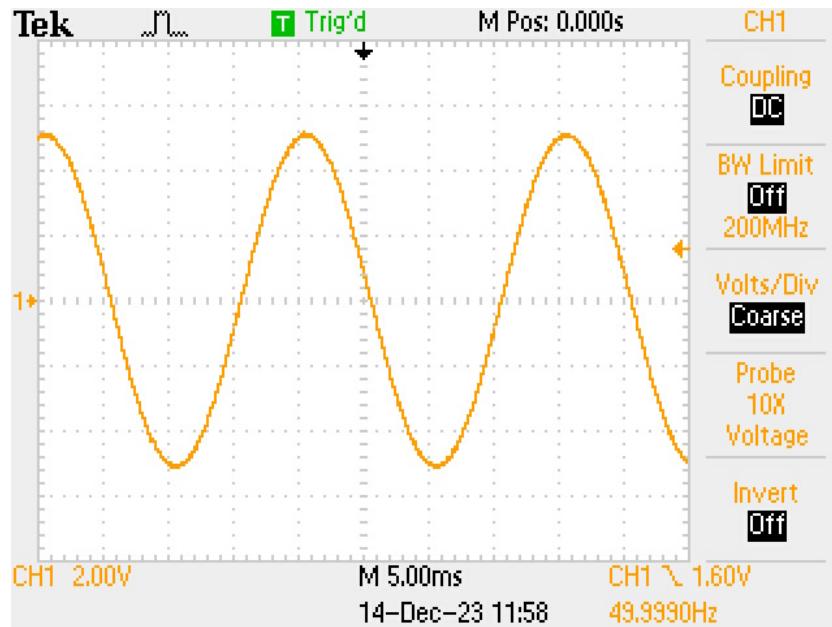


Figure 2.2: Sine Wave

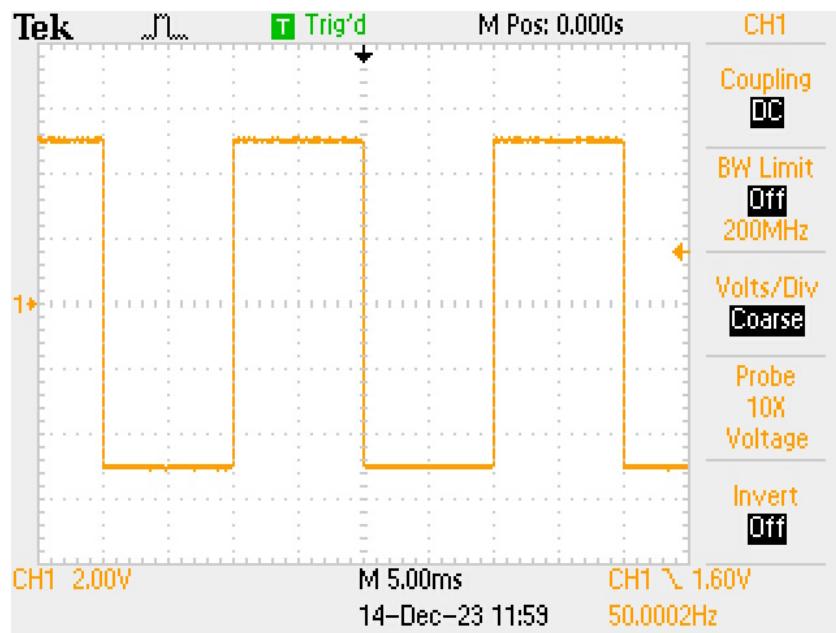


Figure 2.3: Square Wave

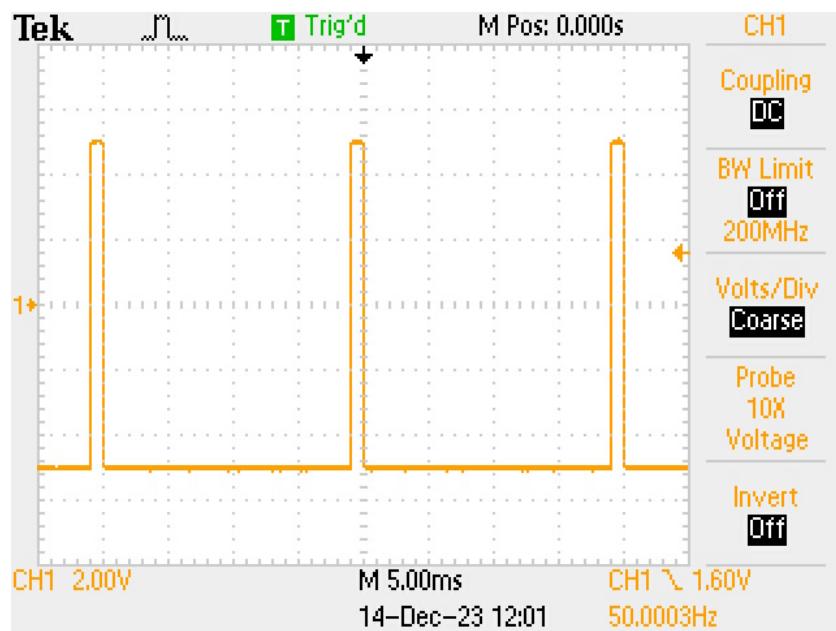


Figure 2.4: Pulse Wave

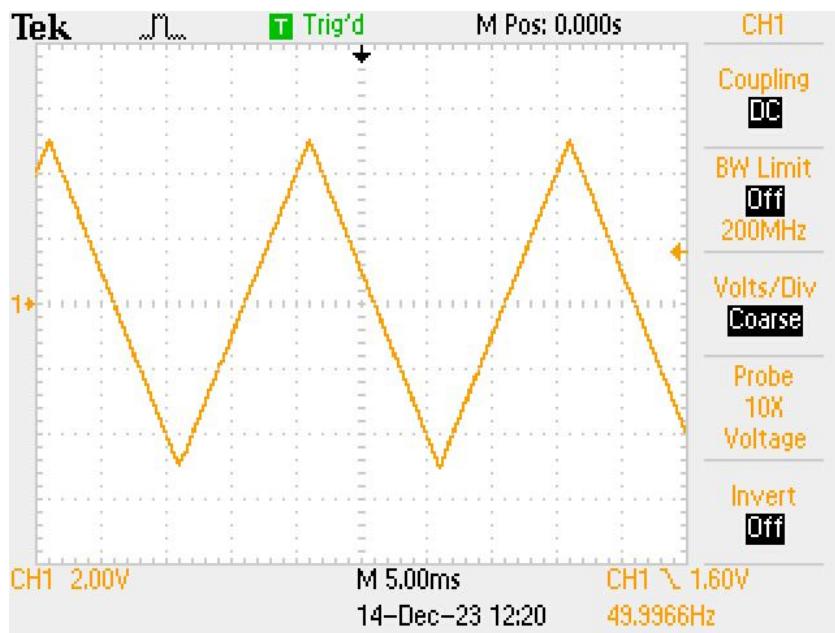


Figure 2.5: Triangle Wave

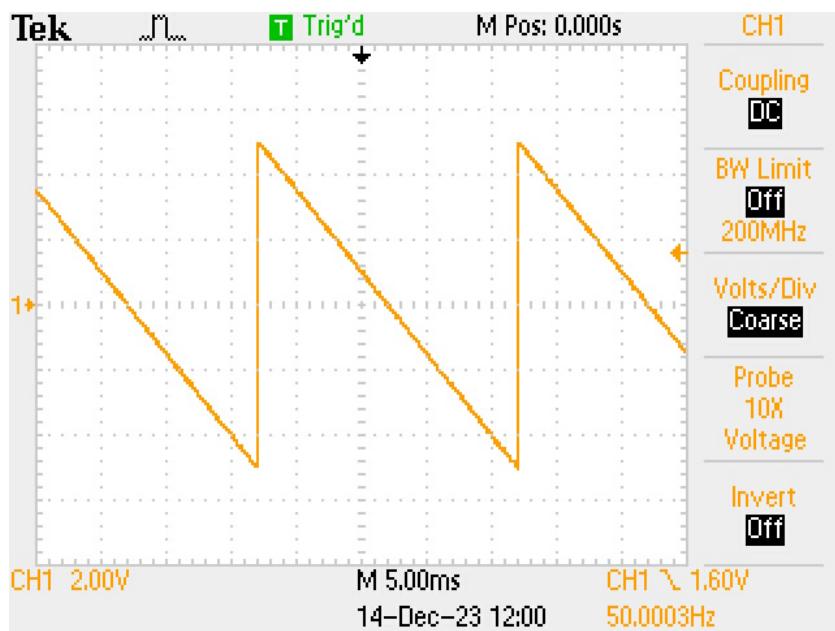


Figure 2.6: Sawtooth Wave

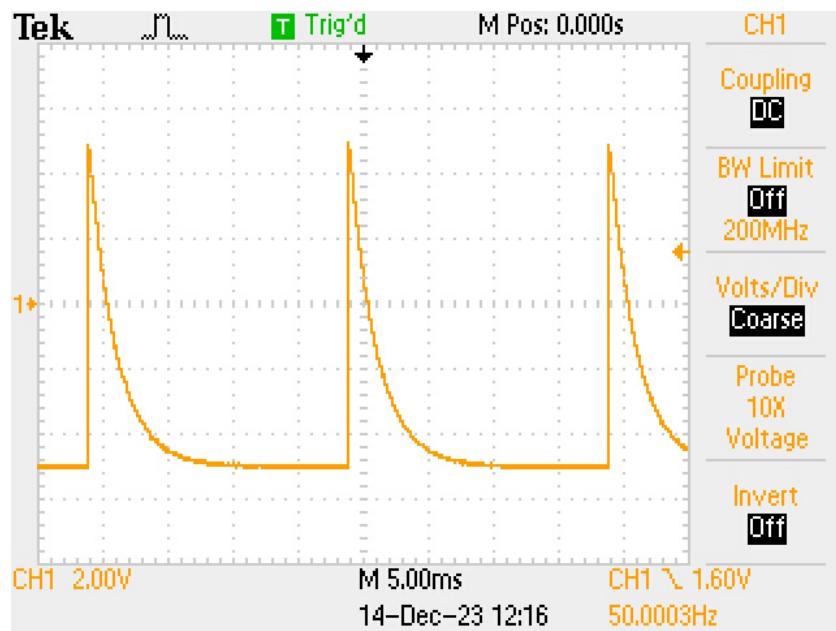


Figure 2.7: Exponential Spike Wave

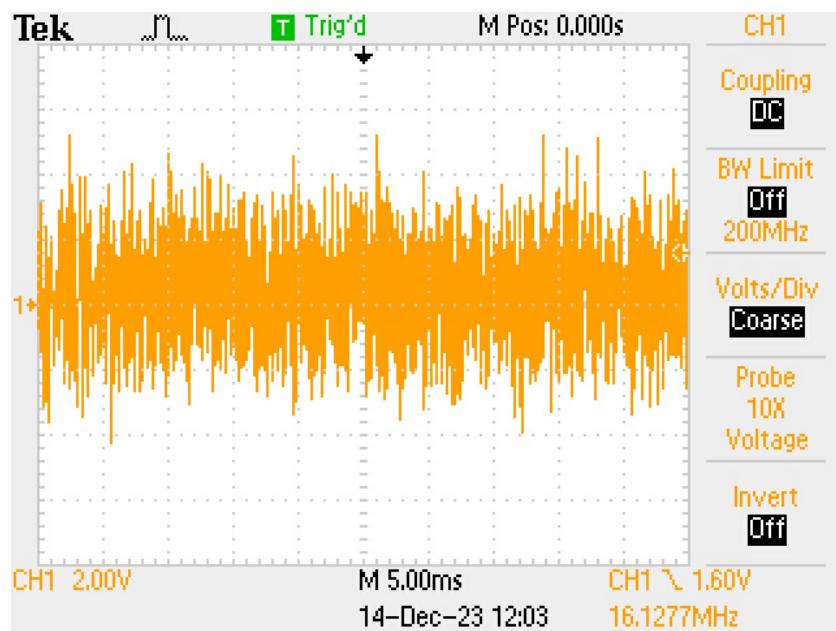


Figure 2.8: Noise Wave

2.3.3 Aperiodic Waveforms

Aperiodic waveforms, in contrast to periodic waveforms, do not exhibit a regular and repeating pattern over time. These waveforms lack a well-defined period, and their shapes do not recur in a predictable manner. Aperiodic waveforms are often associated with transient or non-repetitive signals.

Examples and characteristics:

1. **Impulse or Spike:** A waveform characterized by an instantaneous, brief increase in amplitude, representing an abrupt change.
2. **Step Function:** A waveform that changes abruptly from one constant level to another, creating a step-like pattern.
3. **Random Noise:** A waveform characterized by random variations in amplitude over time, without a discernible pattern.
4. **Exponential Decay:** A waveform where the amplitude decreases exponentially over time.
5. **Chirp Signal:** A waveform with a continuously changing frequency, often used in radar and communication systems.
6. **Pulse Train:** A series of individual pulses, where the intervals between pulses may not be constant.

2.4 Pulse Waveform Characteristics

2.4.1 Ideal Pulse Waveform

The **Ideal Pulse Waveform** has perfectly vertical leading and lagging edges (instantaneous rise and fall times) and perfectly flat tops and bottoms.

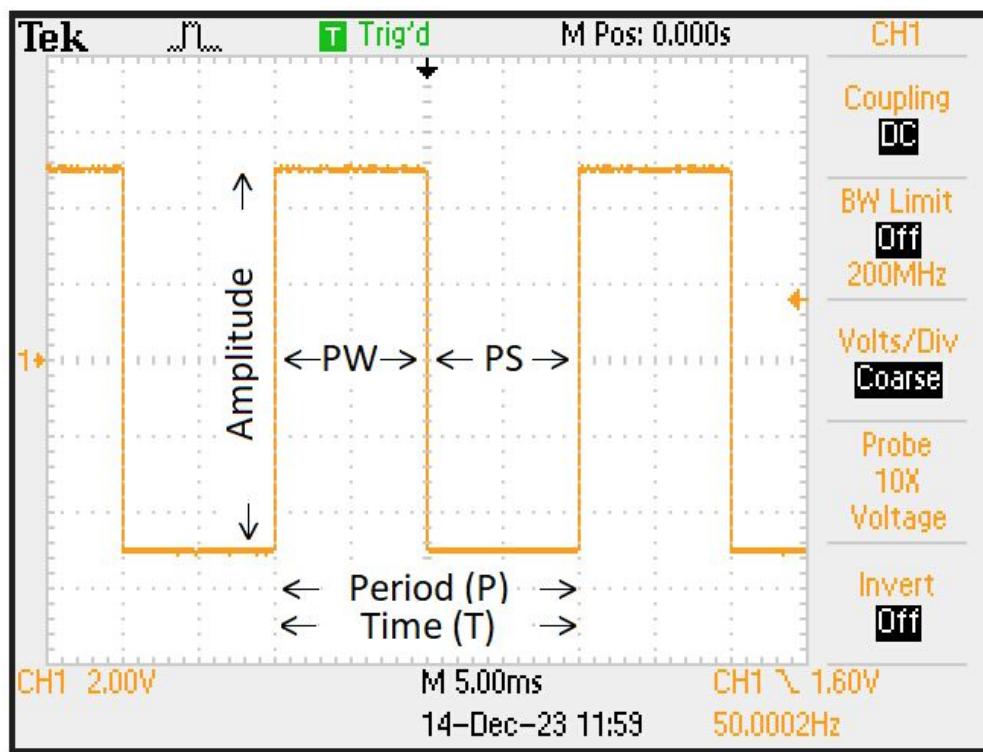


Figure 2.9: Ideal Pulse Waveform

2.4.2 Pulse Waveform Terminology:

- **Period (P):** The time it takes for one complete cycle, from one rising edge to the next rising edge.
- **Pulse Width (PW):** Also known as Time High/On, it is the duration of time during which the waveform is at its maximum amplitude. Typically measured at 50% of the waveform amplitude.
- **Pulse Space (PS):** Also known as Time Low/Off, it is the duration of time during which the waveform is at its minimum amplitude. Also measured at 50% of the waveform amplitude.
- **Pulse Repetition Frequency (PRF):** The reciprocal of the period, representing the number of pulses per unit time.

$$PRF = \frac{1}{\text{Period}}$$

- **Duty Cycle (DC%):** The ratio of the pulse width to the period, expressed as a percentage.

$$DC\% = \frac{PW}{\text{Period}} \times 100$$

2.4.3 Practical Pulse Waveform

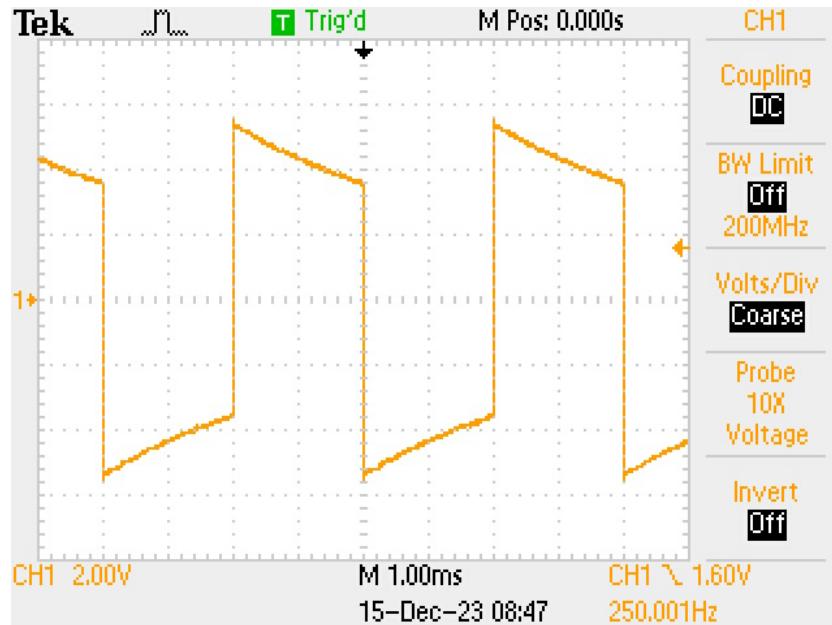


Figure 2.10: Practical Pulse Waveform

The RC circuit practical pulse waveform as seen in Fig 2.10 at 250Hz is outputting a square wave with significant tilt. Tilt represents circuit low-frequency attenuation.

2.4.4 Vmax & Vmin

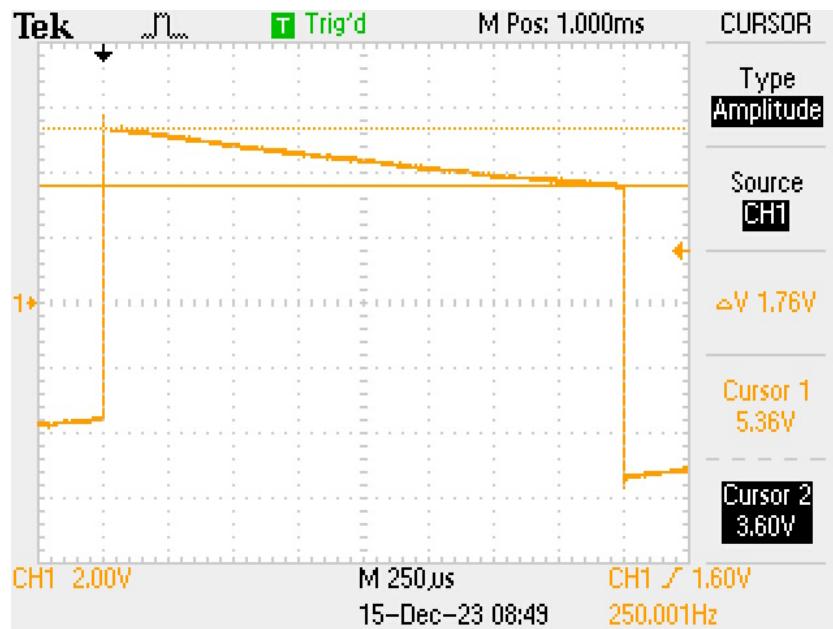


Figure 2.11: Measuring Vmax & Vmin on a Tilt waveform

Defined

- **Vmax** is the highest point of the positive peak.
- **Vmin** is the lowest point of the positive peak.

Measurement Steps

1. Lower the square-wave test signal frequency until tilt is observable.
2. Expand the waveform across the display of the oscilloscope using the horizontal control, see Fig 2.11.
3. Use the cursors to measure Vmax and Vmin of the pulse, see Fig 2.11. Cursor 1 (Vmax) is 5.56V and Cursor 2 (Vmin) is 3.6V.

2.4.5 Rise & Fall Time

Defined

- Rise Time (t_r) is defined as the time required for the voltage to go from 10% to 90% of the average pulse amplitude (APA).

$$APA = \frac{V_{max} + V_{min}}{2}$$

- Fall Time (t_f) is defined as the time required for the voltage to go from 90% to 10% of the average pulse amplitude (APA).

$$APA = \frac{V_{max} + V_{min}}{2}$$

Measurements Steps

1. Increase the square-wave test signal frequency until the tilt is mostly gone, see Fig 2.12.
2. Use the **Fine** Volts/Div to adjust the signal to have exactly 5 major divisions peak to peak, see Fig 2.12.
3. Center the waveform vertically, trigger on the rising edge, and set the trigger point on the y-axis.
4. Zoom in on the rising edge of the waveform, see Fig 2.13
5. Measure the rise time at the -2 divisions (10%) and +2 divisions (90%), see Fig 2.13.

$$t_r = 410nS$$

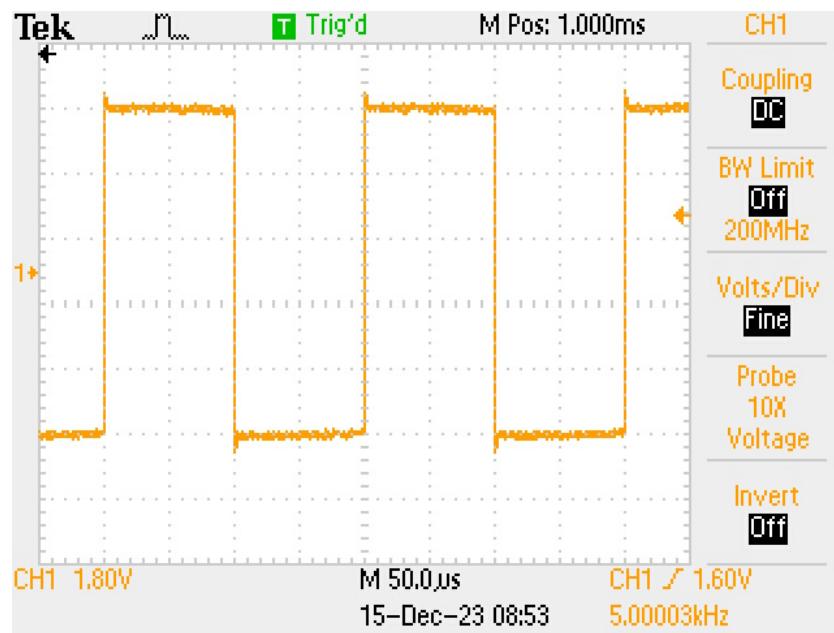


Figure 2.12: Rise Time Set-up Waveform

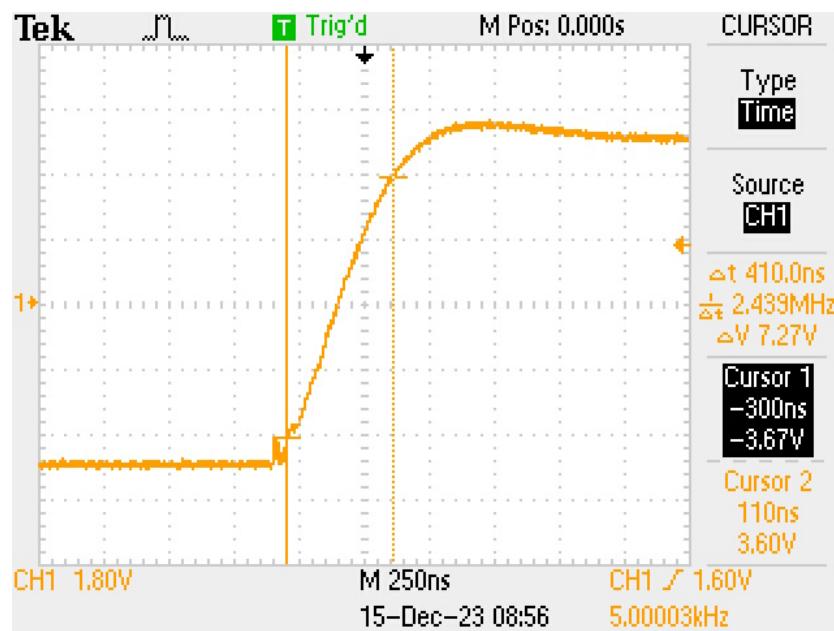


Figure 2.13: Rise Time Measurement

2.4.6 APA (Average Pulse Amplitude) formula

$$APA = \frac{V_{max} + V_{min}}{2}$$

2.4.7 Tilt formulas

$$Tilt = \frac{V_{max} - V_{min}}{APA}$$

$$Tilt\% = \frac{V_{max} - V_{min}}{APA} \times 100$$

2.4.8 AWV (Average Waveform Voltage)

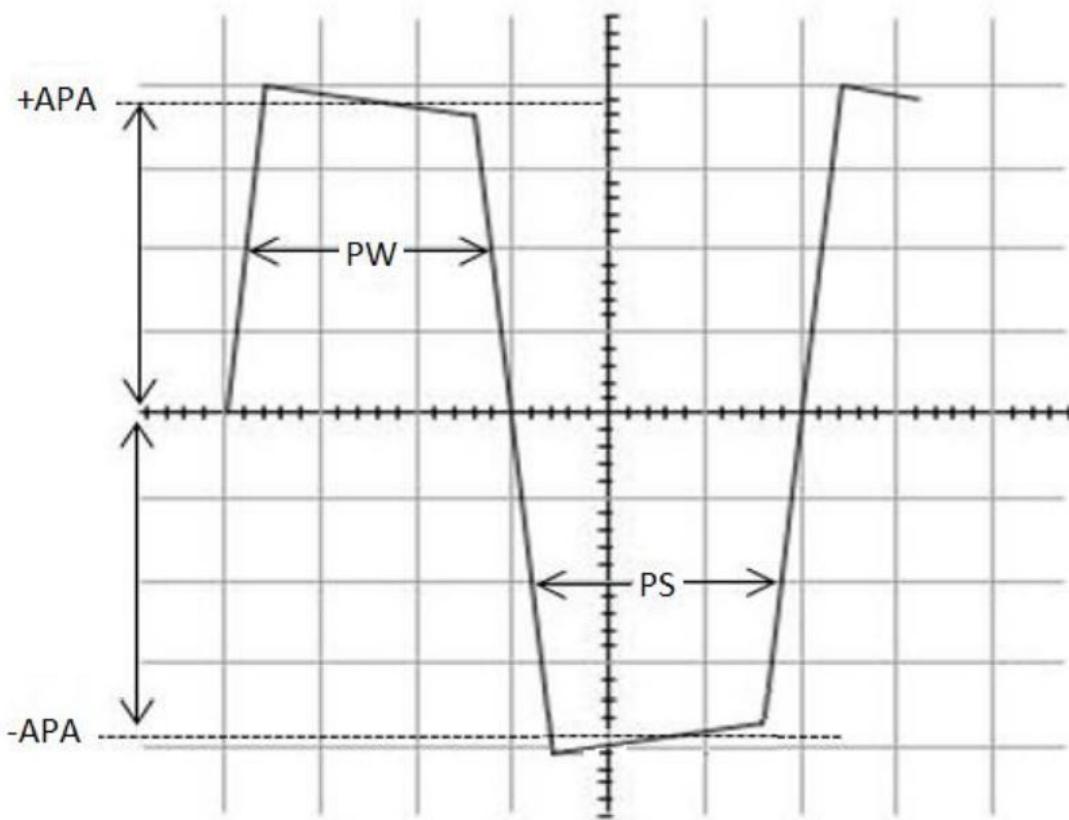


Figure 2.14: AWV (Average Waveform Voltage)

AWV formula

$$AWV = \frac{(+APA \times PW) + (-APA \times PS)}{Period}$$

AWV explained

If the positive peak and negative peak are equal in amplitude, and the pulse width and pulse space are equal, then the waveform is symmetric, and the average voltage is indeed zero. This is because, over a complete cycle, the positive and negative voltages cancel each other out.

However, if the positive peak and negative peak amplitudes are different, or if the pulse width and pulse space are different, the waveform is no longer symmetric, and the average voltage will not be zero. In this case, you would use the above formula to calculate the average voltage.

AWV examples

1. AWV Practice Problem

Given:

- $+APA = 8V$
- $-APA = -10V$
- $PW\&PS = 50\mu S$

$$AWV = \frac{(+APA \times PW) + (-APA \times PS)}{\text{Period}}$$

$$AWV = \frac{(8V \times 50\mu S) + (-10V \times 50\mu S)}{100\mu S}$$

$$AWV = \frac{400 \times 10^{-6} + -500 \times 10^{-6}}{100 \times 10^{-6}}$$

$$AWV = \frac{-100 \times 10^{-6}}{100 \times 10^{-6}}$$

$$AWV = -1V$$

2. AWV Practice Problem

Given:

- $+APA = 8V$
- $-APA = -10V$
- $PW = 30\mu S$
- $PS = 10\mu S$

$$AWV = \frac{(+APA \times PW) + (-APA \times PS)}{Period}$$

$$AWV = \frac{(8V \times 30\mu S) + (-10V \times 10\mu S)}{40\mu S}$$

$$AWV = \frac{240 \times 10^{-6} + -100 \times 10^{-6}}{40 \times 10^{-6}}$$

$$AWV = \frac{140 \times 10^{-6}}{40 \times 10^{-6}}$$

$$AWV = 3.5V$$

2.5 Frequency Synthesis & Analysis

2.5.1 Frequency Synthesis

Frequency synthesis involves combining two or more signals to create a new waveform. Just like an AC signal will superimpose on a DC signal, two AC signals present at the same time will also combine to form a new waveform. When this occurs it is referred to as Frequency Synthesis.

synthesis noun: the composition or combination of parts or elements so as to form a whole. Merriam Webster

Frequency Synthesis is the process of combining multiple sine waves to produce a new desired waveform.

Harmonics

- ✓ A harmonic is a multiple of the fundamental.
- ✓ Harmonics are numbered according to their ratio to the fundamental.
- ✓ The number of harmonics is infinite; however, the amplitude of each harmonic will successively decrease as frequency increases.

Table 2.1: Sinusoidal Harmonics

Harmonic Number	Frequency	Amplitude
<i>Fundamental</i>	F	V
<i>2nd harmonic</i>	2F	$\frac{V}{2}$
<i>3rd harmonic</i>	3F	$\frac{V}{3}$
<i>4th harmonic</i>	4F	$\frac{V}{4}$
<i>5th harmonic</i>	5F	$\frac{V}{5}$
<i>6th harmonic</i>	6F	$\frac{V}{6}$
<i>7th harmonic</i>	7F	$\frac{V}{7}$
<i>100th harmonic</i>	100F	$\frac{V}{100}$

2.5.2 Perfect Square Waves

A **Perfect Square Wave** is comprised of an infinite number of odd harmonic sine waves.

Sawtooth, Exponential, and Triangle Waveforms are comprised of a combination of odd and even harmonic sine waves.

Can a Square Wave really be created using Sine Wave Frequency Synthesis?

To test this theory we can use Desmos Graphing Calculator [7]. Link to final graph <https://www.desmos.com/calculator/bbjnjmrxyz>.

Sine-wave formulas:

$$\text{Fundamental} = \frac{4}{\pi} \frac{1}{1} \sin(1\pi x)$$

$$3^{rd} \text{harmonic} = \frac{4}{\pi} \frac{1}{3} \sin(3\pi x)$$

$$5^{th} \text{harmonic} = \frac{4}{\pi} \frac{1}{5} \sin(5\pi x)$$

$$7^{th} \text{harmonic} = \frac{4}{\pi} \frac{1}{7} \sin(7\pi x)$$

$$9^{th} \text{harmonic} = \frac{4}{\pi} \frac{1}{9} \sin(9\pi x)$$

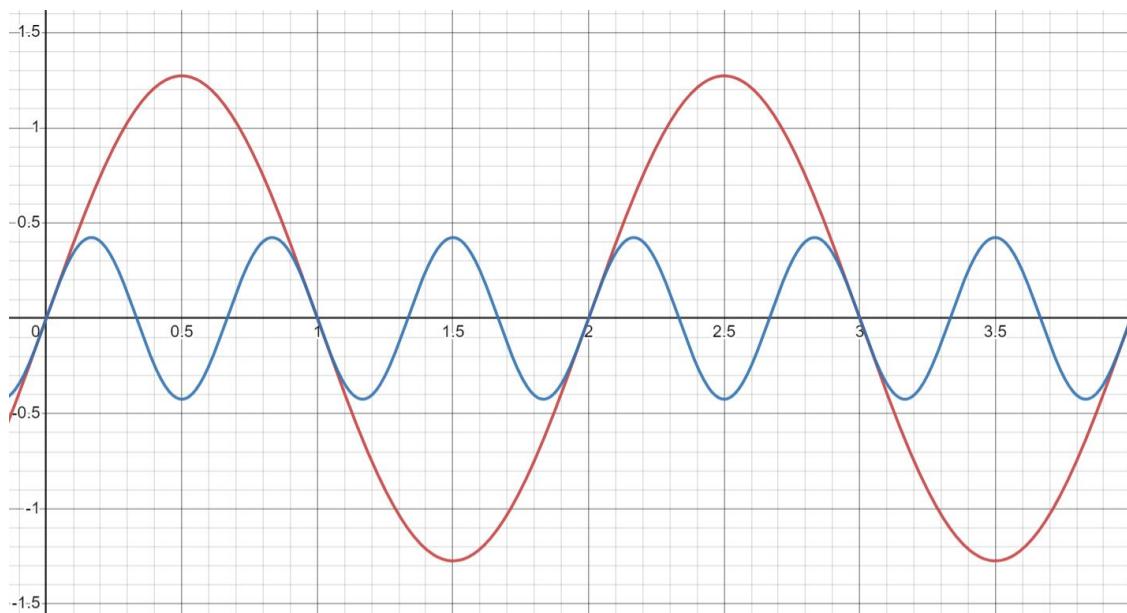


Figure 2.15: Fundamental & Third Harmonic

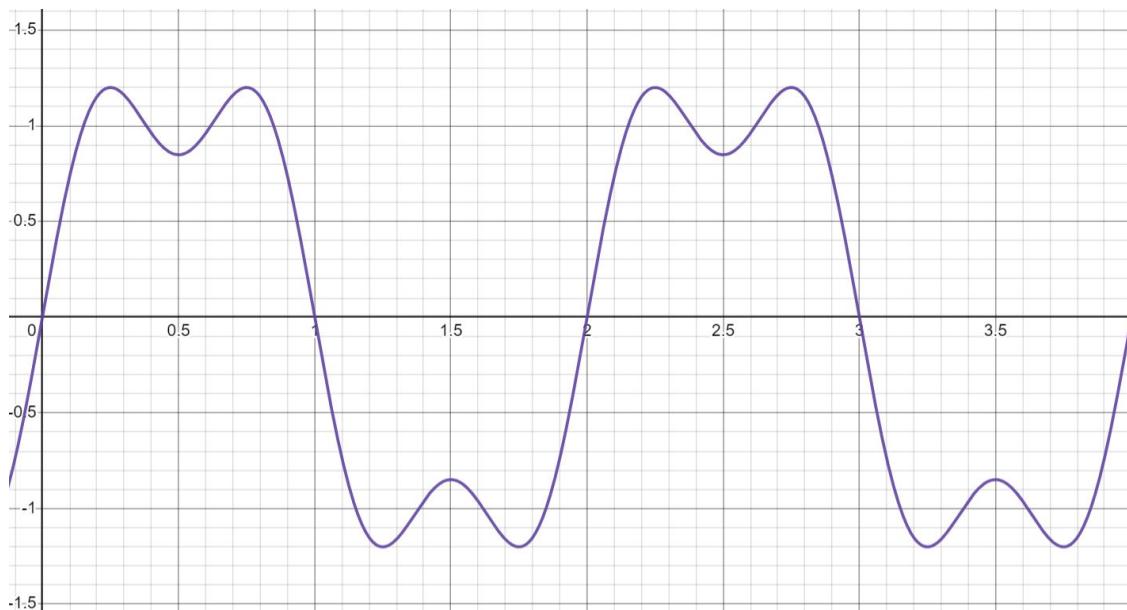


Figure 2.16: Fundamental & Third Harmonic Synthesis

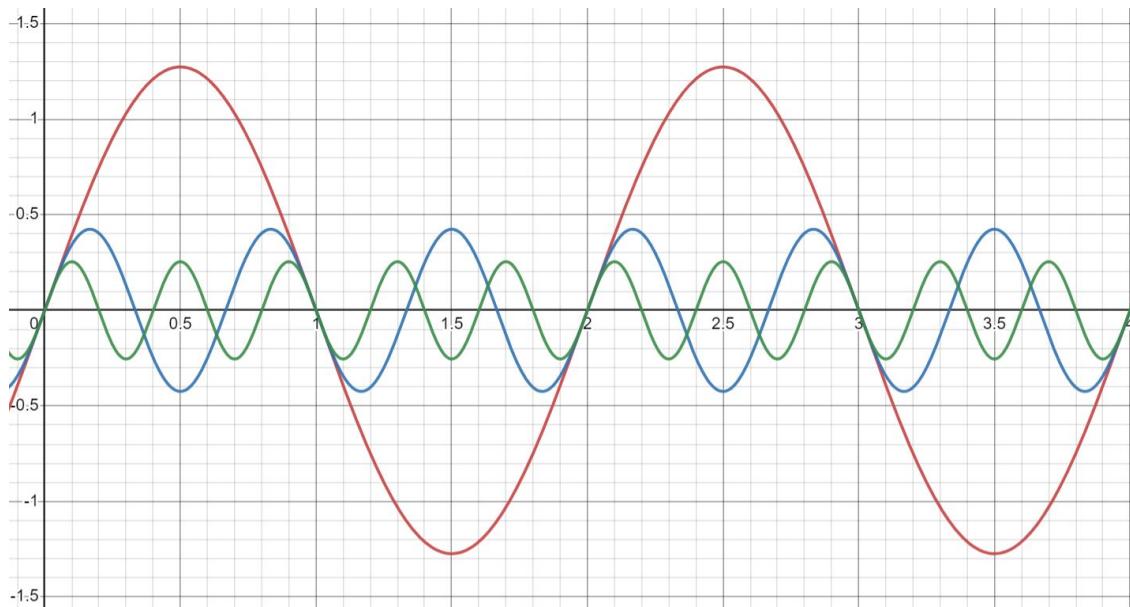


Figure 2.17: Fundamental, Third & Fifth Harmonics

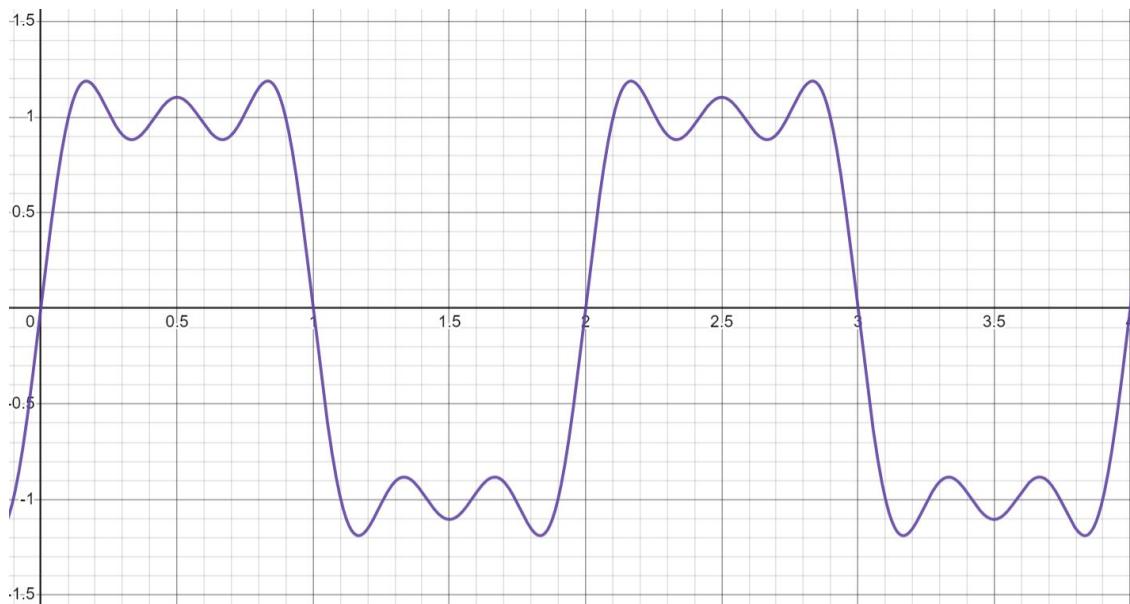


Figure 2.18: Fundamental, Third & Fifth Harmonics Synthesis

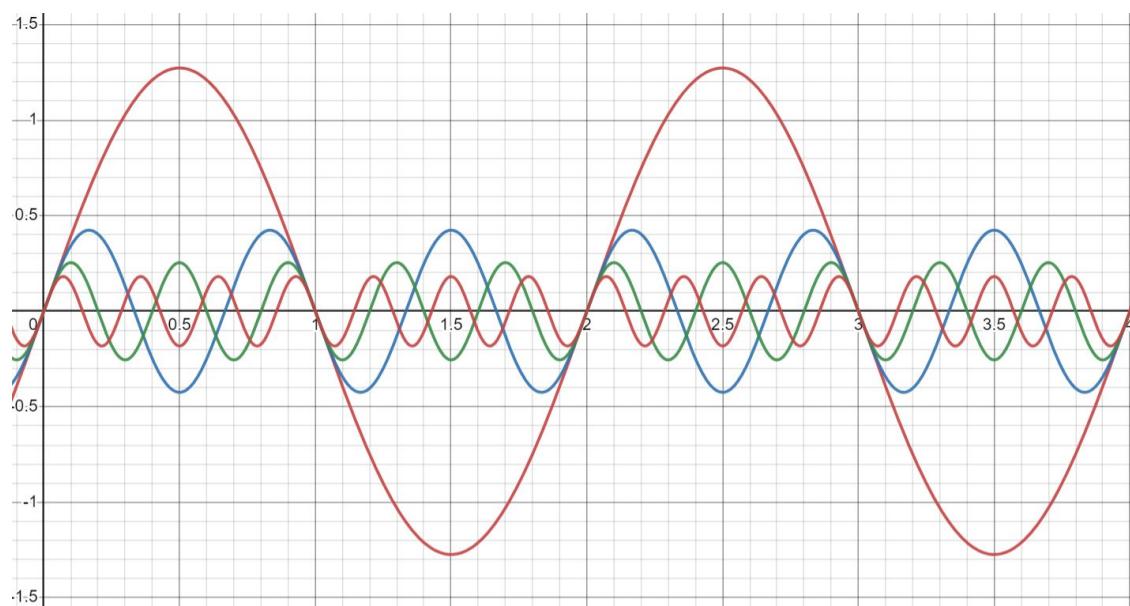


Figure 2.19: Fundamental, Third, Fifth, & Seventh Harmonics

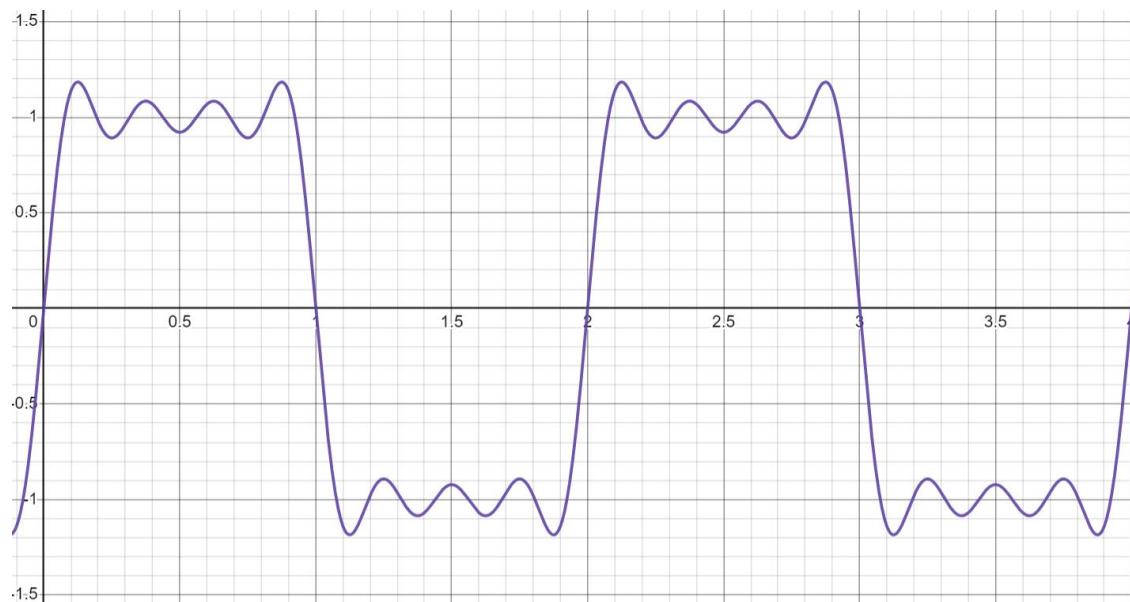


Figure 2.20: Fundamental, Third, Fifth, & Seventh Harmonics Synthesis

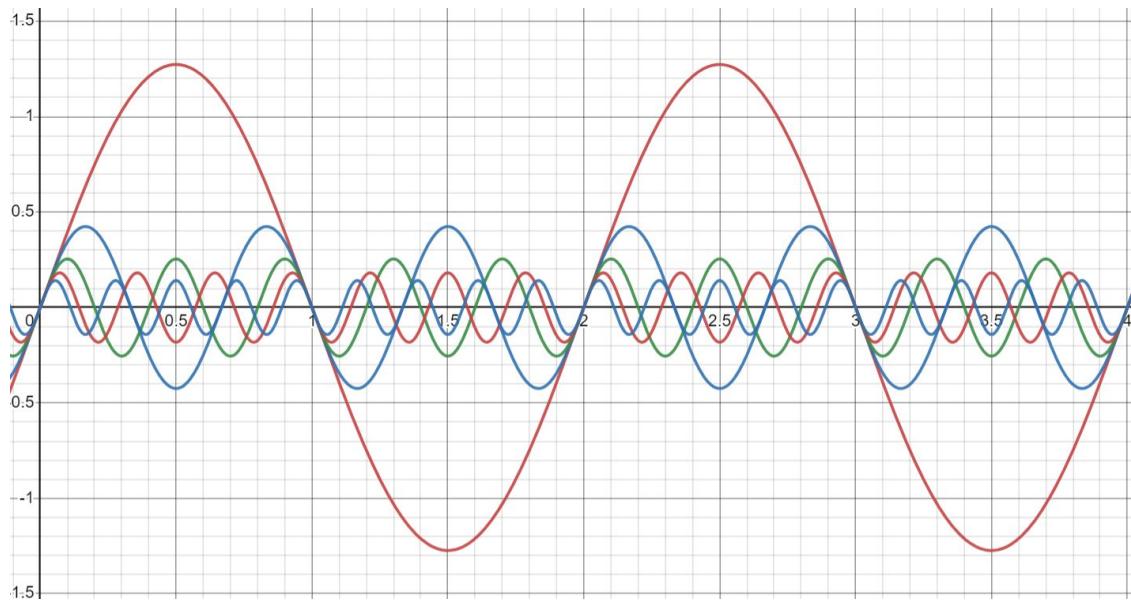


Figure 2.21: Fundamental, Third, Fifth, Seventh, & Ninth Harmonics

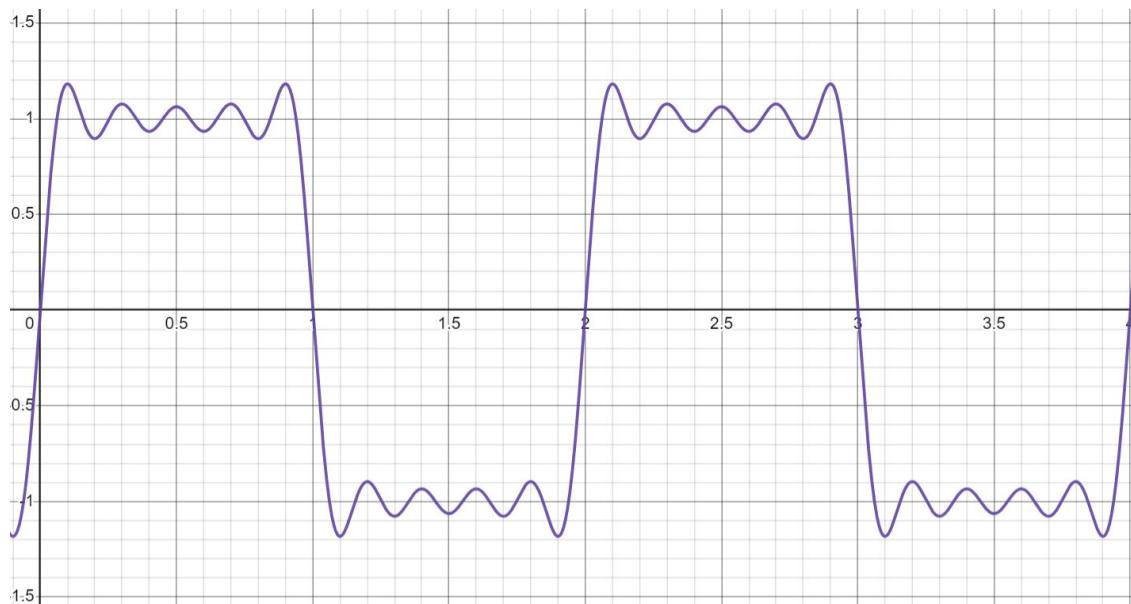


Figure 2.22: Fundamental, Third, Fifth, Seventh, & Ninth Harmonics Synthesis

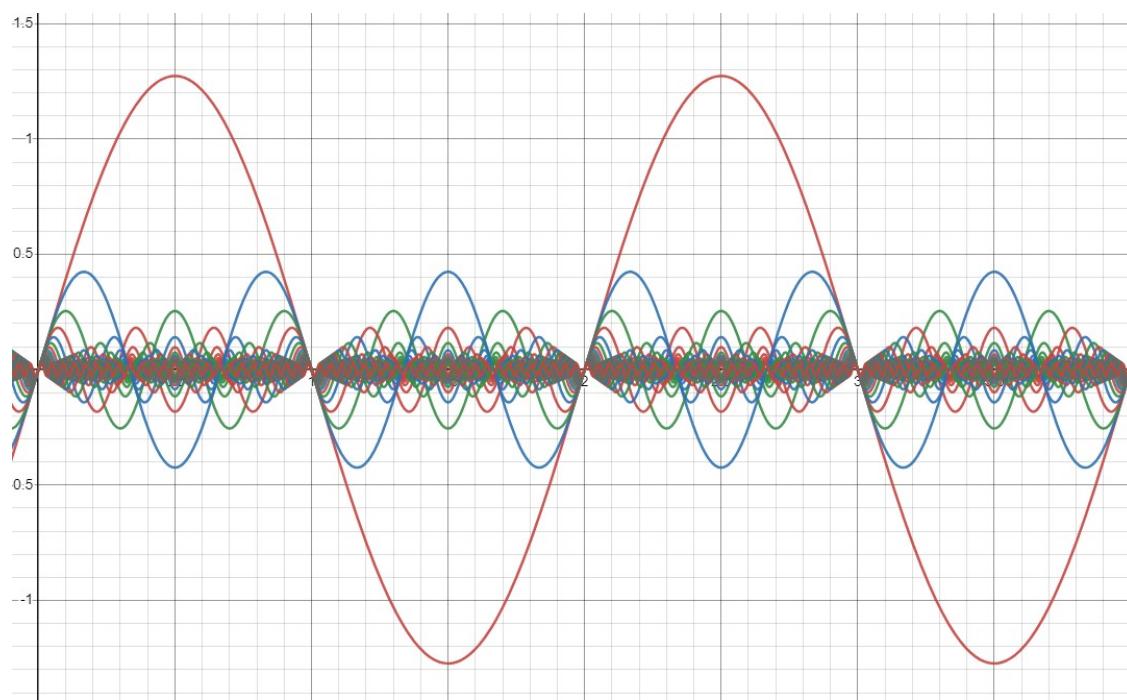


Figure 2.23: Fundamental with odd harmonics up to harmonic 49

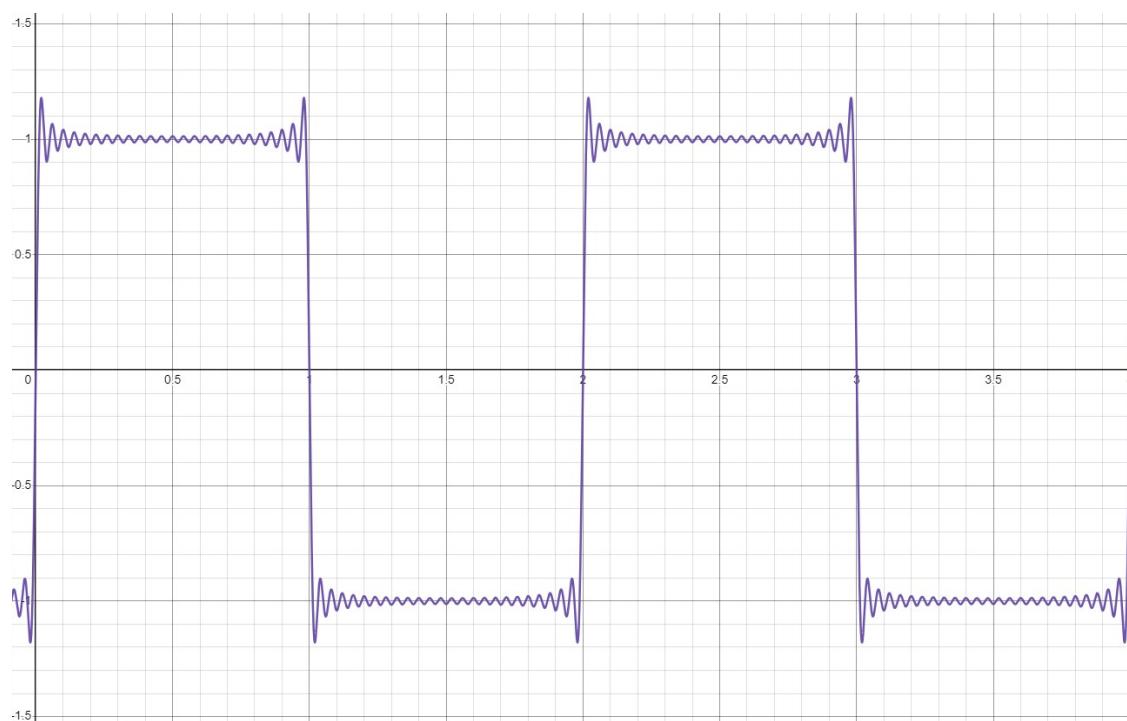


Figure 2.24: Fundamental with odd harmonics up to harmonic 49 Synthesis

2.5.3 Harmonic Analysis

Harmonic Analysis could be thought of as the opposite of, or inversely related to, Frequency Synthesis.

Harmonic Analysis involves breaking down a complex waveform into its individual sinusoidal components or harmonics and is typically achieved through techniques like Fourier Analysis.

Fourier Analysis is a mathematical technique used to decompose a complex waveform into its individual sinusoidal components, representing different frequencies.

2.5.4 Fast Fourier Transformation FFT

The "Fast Fourier Transform" (FFT) is an important measurement method in the science of audio and acoustics measurement. It converts a signal into individual spectral components and thereby provides frequency information about the signal. FFTs are used for fault analysis, quality control, and condition monitoring of machines or systems. NTI Audio [8]

Strictly speaking, the FFT is an optimized algorithm for the implementation of the "Discrete Fourier Transformation" (DFT). A signal is sampled over a period of time and divided into its frequency components. These components are single sinusoidal oscillations at distinct frequencies each with their own amplitude and phase. This transformation is illustrated in figure 2.25 FFT Time, Frequency, Amplitude - Image from NTI Audio [8]. Over the time period measured, the signal contains 3 distinct dominant frequencies. NTI Audio [8].

There are a variety of uses that can benefit from viewing the frequency spectrum of a signal. Using the FFT math function on a time domain signal provides the user with frequency domain information and can provide the user a different view of the signal quality, resulting in improved measurement productivity when troubleshooting a device-under-test. Tektronix[9]

Examples include:

- Analyze harmonics in power lines
- Measure harmonic content and distortion in systems
- Characterize noise in DC power supplies
- Test impulse response of filters and systems
- Analyze vibration Tektronix[9]

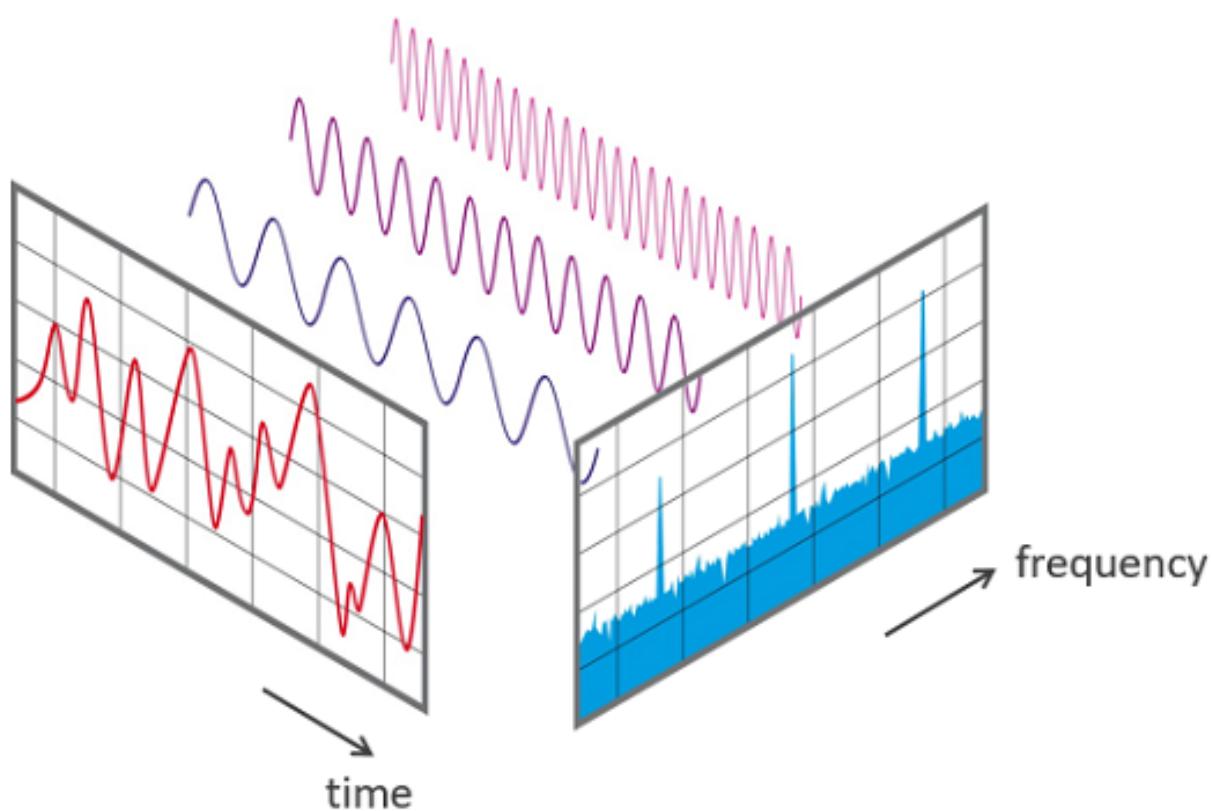


Figure 2.25: FFT Time, Frequency, Amplitude - Image from NTI Audio [8]

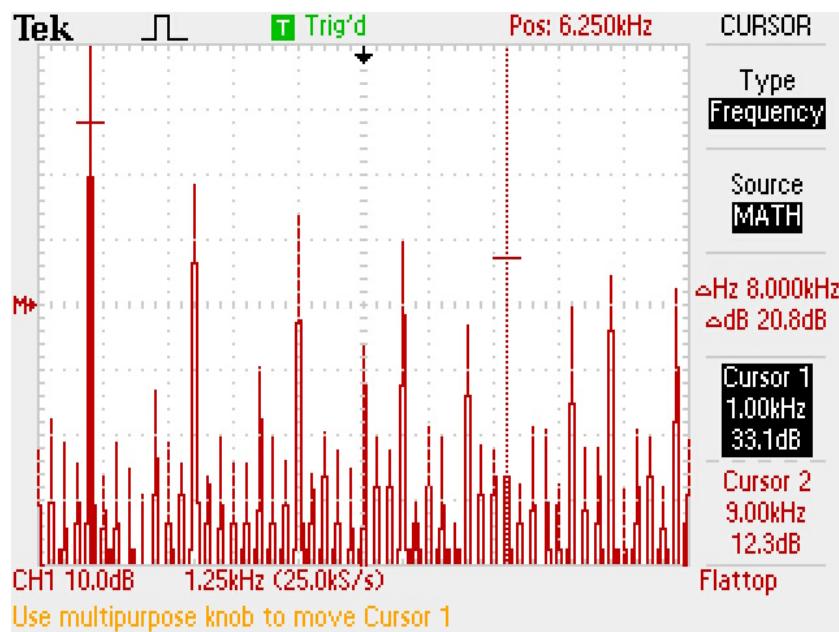


Figure 2.26: Oscilloscope FFT Measurement

2.6 Waveform Distortion

Consider an amplifier or filter circuit with a particular set of band-pass frequencies. What will happen if a square wave is applied to a circuit that limits the amplitude of the square wave harmonic content of the frequencies outside the pass-band? The answer is **waveform distortion**. The two types of square wave distortion that are useful for circuit frequency response analysis are Tilt and Rise Time (t_r).

- **Tilt** represents low frequency amplitude attenuation and can be used to determine Frequency Critical Low (FC_L).
- **Rise Time (t_r)** represents high-frequency amplitude attenuation and can be used to determine Frequency Critical High (FC_H).

2.7 Tilt and Frequency Critical Low (FC_L)

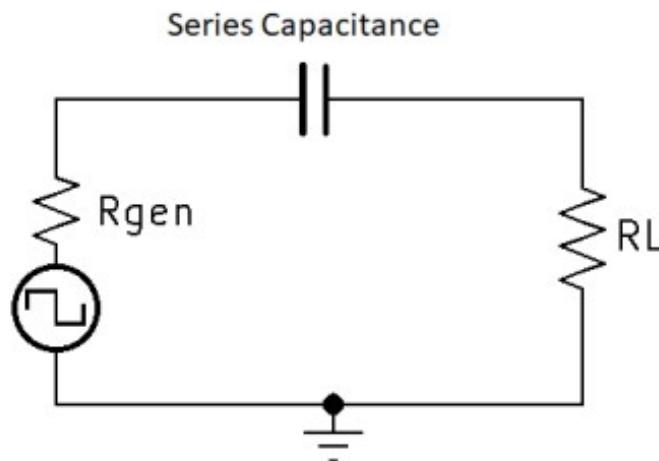


Figure 2.27: Series Capacitance, Tilt, & FC_L

Consider the circuit of figure 2.27 Series Capacitance, Tilt, & FC_L .

- Series capacitance will allow high frequencies through but will attenuate frequencies below FC_L .
- The horizontal component of the square wave represents higher to lower (left to right) frequency amplitude of the odd harmonics.
- X_C of the series capacitance increases as frequency decreases.
- Tilt represents the attenuation of low frequencies.

2.7.1 FC_{Low} formula using Tilt

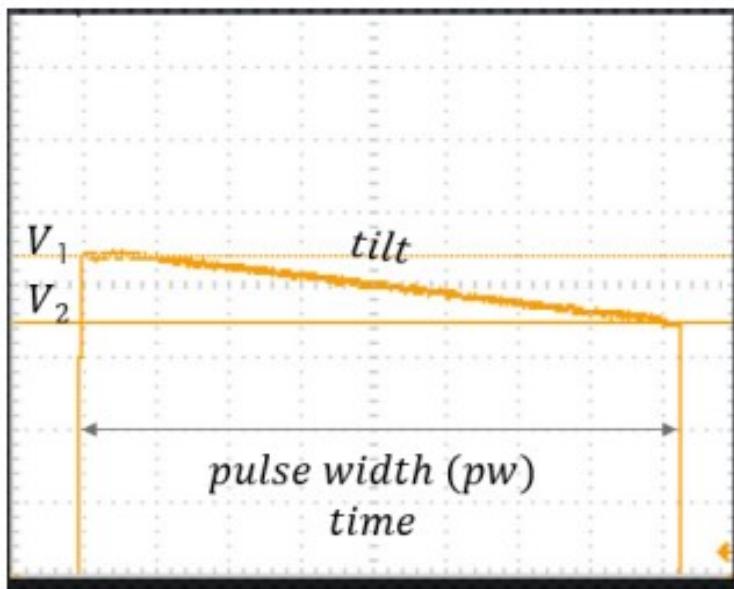


Figure 2.28: Tilt Measurement

$$FC_{Low} = \frac{\text{fractional tilt}}{2\pi PW}$$

$$\text{fractional tilt} = \frac{V1 - V2}{APA}$$

$$APA = \frac{V1 + V2}{2}$$

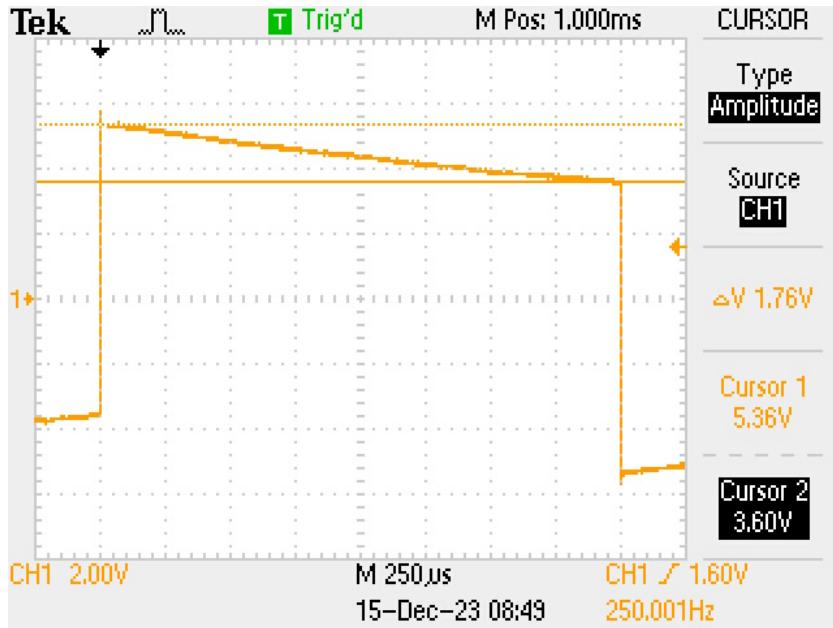


Figure 2.29: Measuring Vmax & Vmin on a Tilt waveform

2.7.2 FC_{Low} Tilt Example

Example 1. See Figure 2.29 Measuring Vmax & Vmin on a Tilt waveform.

- $V_{Cursor1} = 5.36V$
- $V_{Cursor2} = 3.6V$
- Frequency = 250Hz

Solution Steps:

1. Find APA:

$$APA = \frac{V1 + V2}{2}$$

$$APA = \frac{5.36V + 3.6V}{2}$$

$$APA = \frac{8.96V}{2}$$

$APA = 4.48V$

2. Find Fractional Tilt:

$$fractional\ tilt = \frac{V1 - V2}{APA}$$

$$fractional\ tilt = \frac{5.36V - 3.6V}{4.48V}$$

$$fractional\ tilt = \frac{1.76V}{4.48V}$$

$$fractional\ tilt = 0.393$$

3. Find Pulse Width:

$$PW = \frac{Period}{2}$$

$$Period = \frac{1}{Frequency}$$

$$Period = \frac{1}{250HZ}$$

$$Period = 4mS$$

$$PW = \frac{4mS}{2}$$

$$PW = 2mS$$

4. Find Frequency Critical Low:

$$FC_{Low} = \frac{fractional\ tilt}{2\pi PW}$$

$$FC_{Low} = \frac{0.393}{2\pi(2mS)}$$

$$FC_{Low} = \frac{0.393}{12.566 \times 10^{-3}}$$

$$FC_{Low} = 31.274HZ$$

2.8 Rise Time t_r and Frequency Critical High FC_H

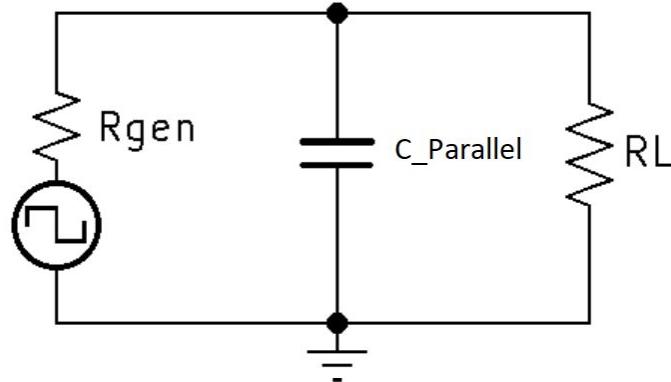


Figure 2.30: Parallel Capacitance, Rise Time, & FC_H

Consider the circuit of figure 2.30 Parallel Capacitance, Rise Time, & FC_H .

- **High Frequency Distortion** is caused by **parallel capacitance**.
- **Parallel capacitance** can include stray capacitance, probe capacitance, generator capacitance, and device capacitance.
- The attenuation of high frequencies caused by parallel capacitance will slow or decrease the **Rise Time** t_r of a measured square wave.

2.8.1 FC_{High} formula using Rise Time t_r

Using Pulse Theory or Square-Wave Analysis, we can calculate the circuit's high critical frequency using the following formula:

$$FC_{High} = \frac{0.35}{t_r}$$

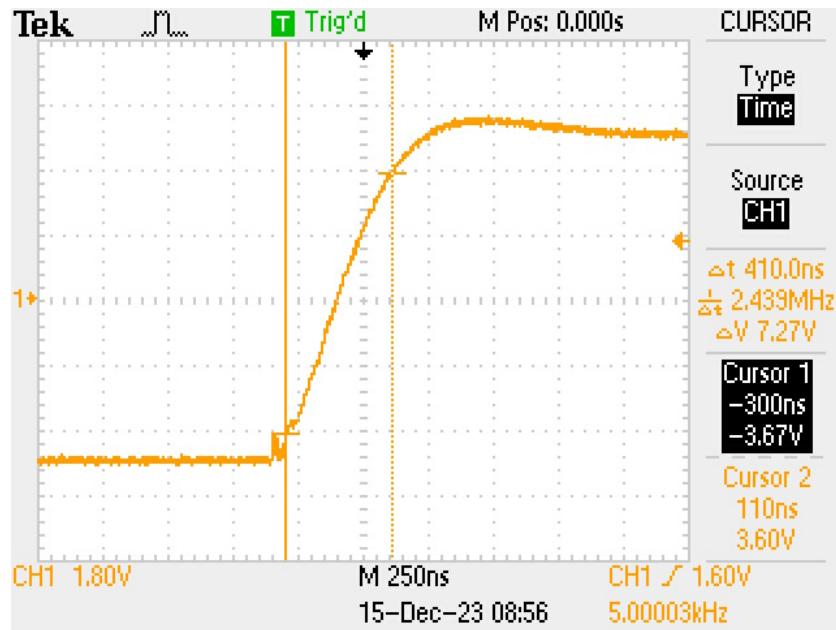


Figure 2.31: Rise Time Measurement

2.8.2 FC_{High} and Rise Time t_r Example

See Figure 2.31 Rise Time Measurement.

1. Measure Rise Time

$$t_r = 410nS$$

2. Calculated FC_{High}

$$FC_{High} = \frac{0.35}{t_r}$$

$$FC_{High} = \frac{0.35}{410nS}$$

$$FC_{High} = 853.659Khz$$

2.9 Capacitor Charge Formula

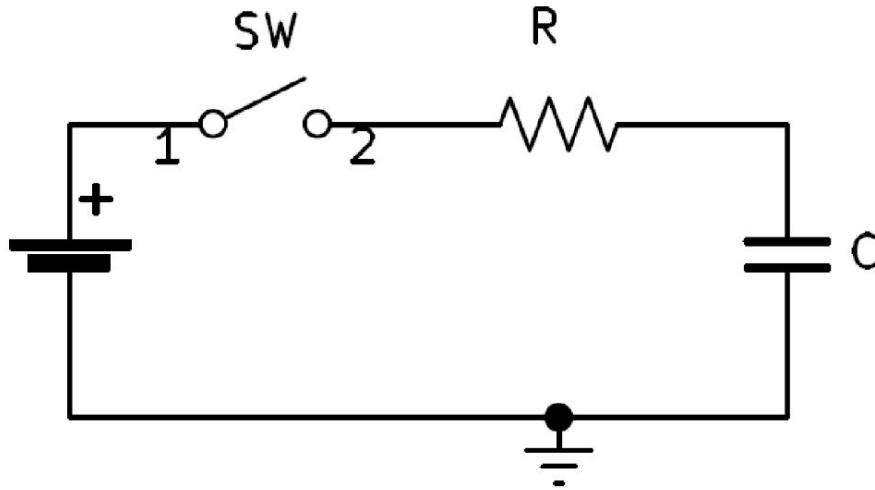


Figure 2.32: Capacitor Charge

After the switch is closed, how long will it take for the capacitor to fully charge?

$$V_{Capacitor} = V_{Final} - (V_{Final} - V_{Initial})e^{(\frac{-t}{\tau})}$$

- * V_{Final} is the voltage that the capacitor would charge or discharge to if time is greater than 5τ .
- * $V_{Initial}$ is the initial voltage that the capacitor is initially at.
- * t is the amount of charge time.
- * Tau (τ) is RC.

2.9.1 Capacitor Charge Formula in terms of % and time vs. τ

Percent of Charge at time equals 1τ :

$$V_C = 100\%V_{Fin} - (100\%V_{Fin} - 0V_{init})e^{(\frac{-1}{1})}$$

- * $V_C = 100\%V_{Fin} - (100\%V_{Fin})e^{-1}$
- * $V_C = 100\%V_{Fin} - (100\%V_{Fin})(0.36787944)$
- * $V_C = 100\%V_{Fin} - 36.787944\%V_{Fin}$

$$* V_C = 63.212056\% V_{Fin}$$

- ✓ At 1τ , the capacitor will charge to 63.212% of the final voltage.

Percent of Charge at time equals 2τ :

$$V_C = 100\% V_{Fin} - (100\% V_{Fin} - 0V_{init})e^{(\frac{-2}{1})}$$

$$* V_C = 100\% V_{Fin} - (100\% V_{Fin})e^{-2}$$

$$* V_C = 100\% V_{Fin} - (100\% V_{Fin})(0.13533528)$$

$$* V_C = 100\% V_{Fin} - 13.533528\% V_{Fin}$$

$$* V_C = 86.466471\% V_{Fin}$$

- ✓ At 2τ , the capacitor will charge to 86.466% of the final voltage.

Percent of Charge at time equals 3τ :

$$V_C = 100\% V_{Fin} - (100\% V_{Fin} - 0V_{init})e^{(\frac{-3}{1})}$$

$$* V_C = 100\% V_{Fin} - (100\% V_{Fin})e^{-3}$$

$$* V_C = 100\% V_{Fin} - (100\% V_{Fin})(0.049787068)$$

$$* V_C = 100\% V_{Fin} - 4.9787068\% V_{Fin}$$

$$* V_C = 95.02129316\% V_{Fin}$$

- ✓ At 3τ , the capacitor will charge to 95.021% of the final voltage.

Percent of Charge at time equals 4τ :

$$V_C = 100\% V_{Fin} - (100\% V_{Fin} - 0V_{init})e^{(\frac{-4}{1})}$$

$$* V_C = 100\% V_{Fin} - (100\% V_{Fin})e^{-4}$$

$$* V_C = 100\%V_{Fin} - (100\%V_{Fin})(0.018315639)$$

$$* V_C = 100\%V_{Fin} - 1.8315639\%V_{Fin}$$

$$* V_C = 98.1684361\%V_{Fin}$$

- ✓ At 4τ , the capacitor will charge to 98.168% of the final voltage.

Percent of Charge at time equals 5τ :

$$V_C = 100\%V_{Fin} - (100\%V_{Fin} - 0V_{init})e^{(\frac{-5}{1})}$$

$$* V_C = 100\%V_{Fin} - (100\%V_{Fin})e^{-5}$$

$$* V_C = 100\%V_{Fin} - (100\%V_{Fin})(0.006737947)$$

$$* V_C = 100\%V_{Fin} - 0.6737947\%V_{Fin}$$

$$* V_C = 99.3262\%V_{Fin}$$

- ✓ At 5τ , the capacitor will charge to 99.326% of the final voltage.

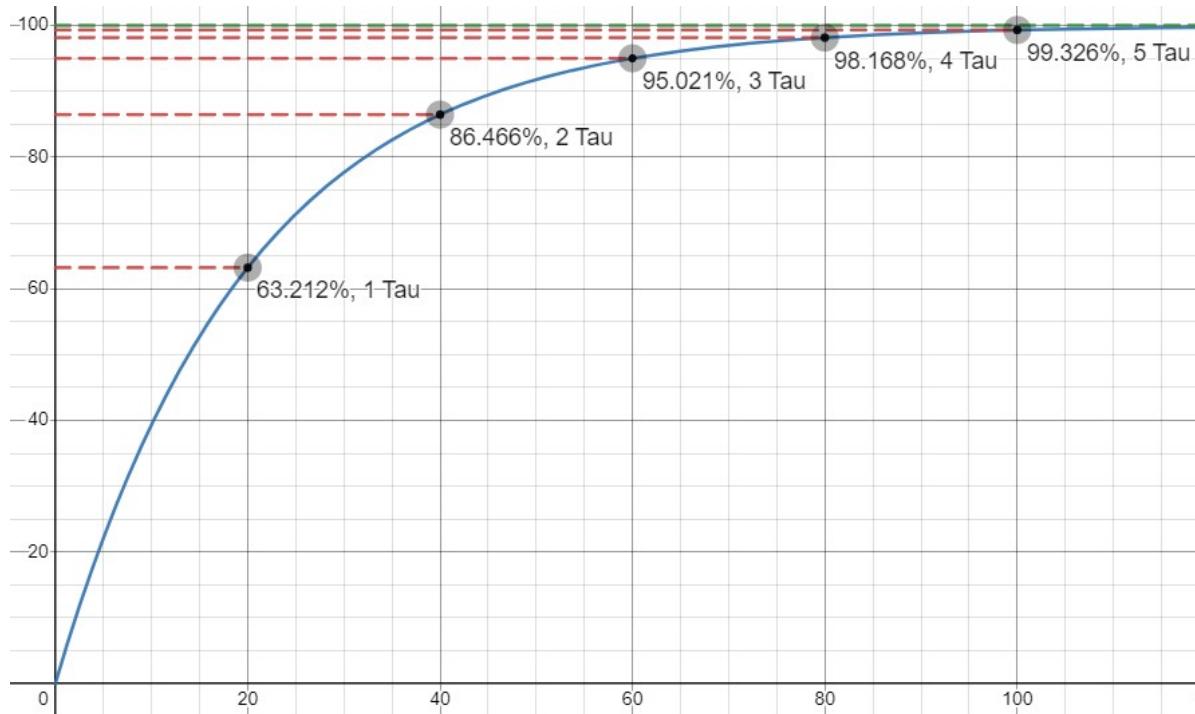


Figure 2.33: Capacitor % of Charge vs. Tau

Table 2.2: RC Circuits Capacitor % of Charge vs. Tau

Tau	V_C % of Charge
1	63.212%
2	86.466%
3	95.021%
4	98.168%
5	99.326%

2.10 RC Circuits Stability, V_{max} & V_{min} Calculations

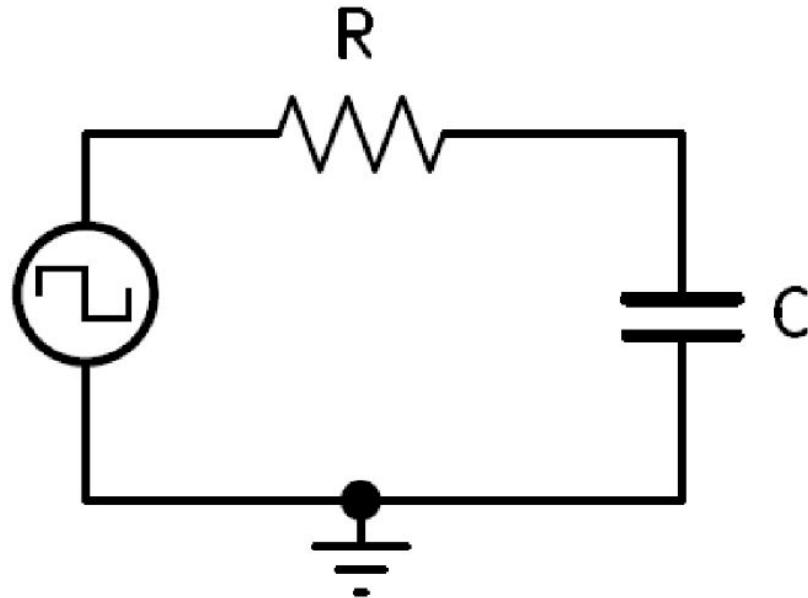


Figure 2.34: RC Circuit Stability

Consider the circuit of Figure 2.34 RC Circuit Stability. What happens to the capacitor voltage if the generator pulse width and pulse space are less than 5τ ? In other words, there is not enough time to fully charge or fully discharge the capacitor. If the time on/off is less than 5 tau the capacitor voltage will not be able to charge up to the full generator voltage, likewise, V_c will not be able to fully discharge during the time off. Assuming the Duty Cycle is 50%, time on & off time are equal, the V_c waveform will appear to center itself vertically between the peak pulse width voltage and the peak pulse space voltage, as though superimposed on an average DC voltage.

$$V_{Capacitor} = V_{Final} - (V_{Final} - V_{Initial})e^{(\frac{-t}{\tau})}$$

The $V_{Capacitor}$ charge formula could be used to calculate cycle after cycle until the charge and discharge voltages stabilized. Next the number of cycles could be counted to find Cycles to Stabilization. This method can be tedious and mathematically error-prone if there are many cycles to stabilization.

2.10.1 Cycles to Stabilization Formula

$$\text{Stability} = 5\tau \text{ (Stable?)}$$

How many cycles to Stabilization?

If:

$$1 \text{ Cycle} = \text{Period}$$

$$\text{Stability} = 5\tau$$

Then:

$$\frac{\text{Stability}}{5\tau(\text{Sec})} = \frac{1\text{Cycle}}{\text{Period}(\text{Sec})}$$

$$\text{Stability} = \frac{1\text{Cycle} \times 5\tau(\text{Sec})}{\text{Period}(\text{Sec})}$$

Notice that the seconds/time unit cancels and we are left with cycles.

✓ $\text{Stability}_{\text{Cycles}} = \frac{5\tau}{\text{Period}}$

The $\text{Stability}_{\text{Cycles}}$ formula only works if the Duty Cycle is 50%. If the generator signal is not at 50% Duty Cycle, the capacitor charge formula long method must be used to calculate the number of cycles to stability.

2.10.2 Vmax and Vmin formulas

Now that we can predict the number of cycles to stabilization, What will the stable capacitor voltage waveform voltage be? What will the maximum and minimum voltage be?

$$V_C = V_{fin} - (V_{fin} - V_{In})e^{\frac{-t}{RC}}$$

$$t = PW$$

$$V_C = V_{Max}$$

$$V_{gen+} = V_{fin}$$

$$V_{In} = V_{Min}$$

$$V_{Min} = V_{gen+} - V_{Max}$$

$$V_{In} = V_{gen+} - V_{Max}$$

$$V_{Max} = V_{gen+} - (V_{gen+} - (V_{gen+} - V_{Max}))e^{\frac{-PW}{RC}}$$

$$V_{Max} = V_{gen+} - (V_{gen+} - V_{gen+} + V_{Max})e^{\frac{-PW}{RC}}$$

$$V_{Max} = V_{gen+} - (V_{Max})e^{\frac{-PW}{RC}}$$

$$V_{Max} + (V_{Max})e^{\frac{-PW}{RC}} = V_{gen+}$$

$$V_{Max}(1 + e^{\frac{-PW}{RC}}) = V_{gen+}$$

$$V_{Max} = \frac{V_{gen+}}{1 + e^{\frac{-PW}{RC}}}$$

$$V_{Min} = V_{gen+} - V_{Max}$$

The V_{Max} & V_{Min} formulas only works if the Duty Cycle is 50% .

2.10.3 RC Circuit Stability Example Problem:

Refer to Figure 2.34 RC Circuit Stability schematic.

Given:

- V_{gen} is 0 to 10v, 1Khz, 50%DC, square-wave.
- $R = 1K\Omega$
- $C = 1\mu F$
- $\tau = RC = 1mS$
- $5\tau = 5 \times 10^{-3} \text{ seconds } (5mS)$
- $\text{Period} = \frac{1}{1Khz} = 1mS$
- $PW \text{ and } PS = \frac{\text{Period}}{2} = 0.5mS$

Solving using the Capacitor Charge Formula:

$$V_{Capacitor} = V_{Final} - (V_{Final} - V_{Initial})e^{(\frac{-t}{\tau})}$$

- time = 0 to 0.5mSec

$$V_C = 10V - (10V - 0V)e^{(\frac{-0.5mS}{1mS})}$$

$$V_C = 3.935V$$

- time = 0.5 to 1.0mSec

$$V_C = 0V - (0V - 3.935V)e^{(\frac{-0.5mS}{1mS})}$$

$$V_C = 2.387V$$

- time = 1 to 1.5mSec

$$V_C = 10V - (10V - 2.387V)e^{(\frac{-0.5mS}{1mS})}$$

$$V_C = 5.382V$$

- time = 1.5 to 2.0mSec

$$V_C = 0V - (0V - 5.382V)e^{(\frac{-0.5mS}{1mS})}$$

$$V_C = 3.265V$$

- time = 2.0 to 2.5mSec

$$V_C = 10V - (10V - 3.265V)e^{(\frac{-0.5mS}{1mS})}$$

$$V_C = 5.915V$$

- time = 2.5 to 3.0mSec

$$V_C = 0V - (0V - 5.915V)e^{(\frac{-0.5mS}{1mS})}$$

$$V_C = 3.587V$$

- time = 3.0 to 3.5mSec

$$V_C = 10V - (10V - 3.587V)e^{(\frac{-0.5mS}{1mS})}$$

$$V_C = 6.111V$$

- time = 3.5 to 4.0mSec

$$V_C = 0V - (0V - 6.111V)e^{(\frac{-0.5mS}{1mS})}$$

$$V_C = 3.706V$$

- time = 4.0 to 4.5mSec

$$V_C = 10V - (10V - 3.706V)e^{(\frac{-0.5mS}{1mS})}$$

$$V_C = 6.182V$$

- time = 4.5 to 5.0mSec

$$V_C = 0V - (0V - 6.182V)e^{(\frac{-0.5mS}{1mS})}$$

$$V_C = 3.740V$$

- time = 5.0 to 5.5mSec

$$V_C = 10V - (10V - 3.740V)e^{(\frac{-0.5mS}{1mS})}$$

$$V_C = 6.209V$$

- time = 5.5 to 6.0mSec

$$V_C = 0V - (0V - 6.209V)e^{(\frac{-0.5mS}{1mS})}$$

$$V_C = 3.766V$$

- time = 6.0 to 6.5mSec

$$V_C = 10V - (10V - 3.766V)e^{(\frac{-0.5mS}{1mS})}$$

$$V_C = 6.219V$$

- time = 6.5 to 7.0mSec

$$V_C = 0V - (0V - 6.219V)e^{(-\frac{0.5mS}{1mS})}$$

$$V_C = 3.772V$$

- time = 7.0 to 7.5mSec

$$V_C = 10V - (10V - 3.772V)e^{(-\frac{0.5mS}{1mS})}$$

$$V_C = 6.223V$$

- time = 7.5 to 8.0mSec

$$V_C = 0V - (0V - 6.223V)e^{(-\frac{0.5mS}{1mS})}$$

$$V_C = 3.774V$$

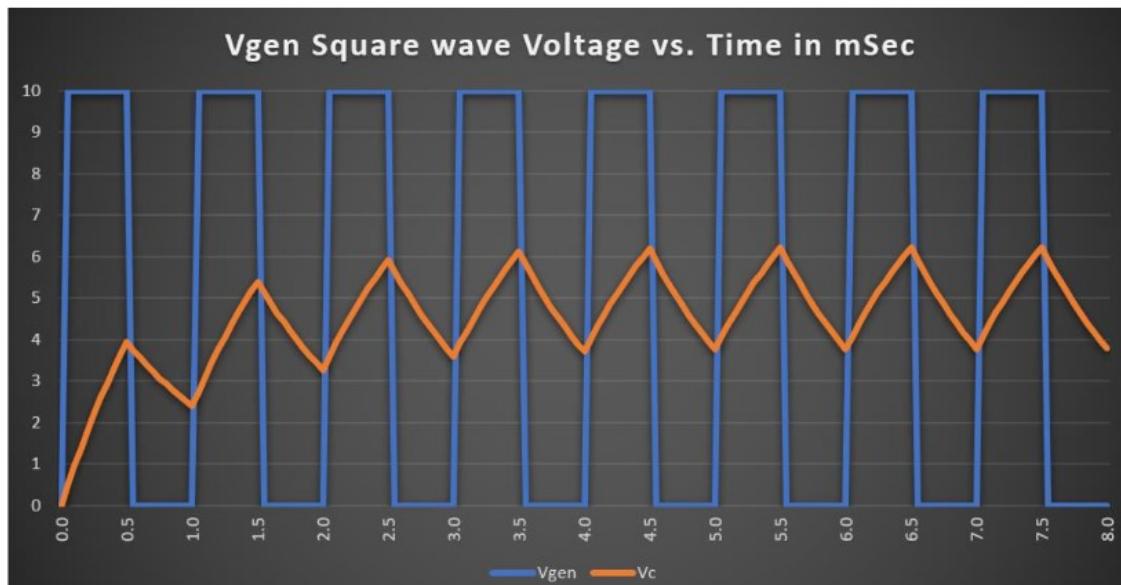


Figure 2.35: VC Stability

See Figure 2.35, observe that the capacitor waveform voltage is stable at 5τ ($5mS$) & 5 cycles.

Solving using the Stability, V_{Max} , & V_{Min} using formulas derived in Sections 2.10.1 & 2.10.2:

Refer to Figure 2.34 RC Circuit Stability schematic.

Given:

- V_{gen} is 0 to 10v, 1Khz, 50%DC, square-wave.
- $R = 1K\Omega$
- $C = 1\mu F$
- $\tau = RC = 1mS$
- $5\tau = 5 \times 10^{-3} \text{ seconds } (5mS)$
- $\text{Period} = \frac{1}{1Khz} = 1mS$
- $PW \text{ and } PS = \frac{\text{Period}}{2} = 0.5mS$

Formulas:

$$\text{Stability}_{\text{Cycles}} = \frac{5\tau}{\text{Period}}$$

$$V_{Max} = \frac{V_{gen+}}{1 + e^{\frac{-PW}{RC}}}$$

$$V_{Min} = V_{gen+} - V_{Max}$$

Calculating The Number of Cycles to Stability:

$$Stability_{Cycles} = \frac{5\tau}{Period}$$

$$Stability_{Cycles} = \frac{5(RC)}{1mS}$$

$$Stability_{Cycles} = \frac{5(1K\Omega \times 1\mu F)}{1mS}$$

$$Stability_{Cycles} = \frac{5(1mS)}{1mS}$$

$Stability_{Cycles} = 5 \text{ cycles}$

Calculating V_{Max} :

$$V_{Max} = \frac{V_{gen+}}{1 + e^{\frac{-PW}{RC}}}$$

$$V_{Max} = \frac{10V}{1 + e^{\frac{-0.5mS}{1K\Omega \times 1\mu F}}}$$

$$V_{Max} = \frac{10V}{1 + 0.606531}$$

$V_{Max} = 6.225vp$

Calculating V_{Min} :

$$V_{Min} = V_{gen+} - V_{Max}$$

$$V_{Min} = 10V - 6.225vp$$

$V_{Min} = 3.775vp$

Additionally, we can check our work by taking the average voltage of V_{Max} and V_{Min} . We know that the waveform voltage should be centered around the average generator voltage, in this case 5volts, ($5v = \frac{0+10}{2}$).

Calculating V_{avg} :

$$V_{avg} = \frac{V_{Max} + V_{Min}}{2}$$

$$V_{avg} = \frac{6.225v + 3.775v}{2}$$

$$V_{avg} = \frac{10v}{2}$$

$$\boxed{V_{avg} = 5v}$$

2.11 RC Integration

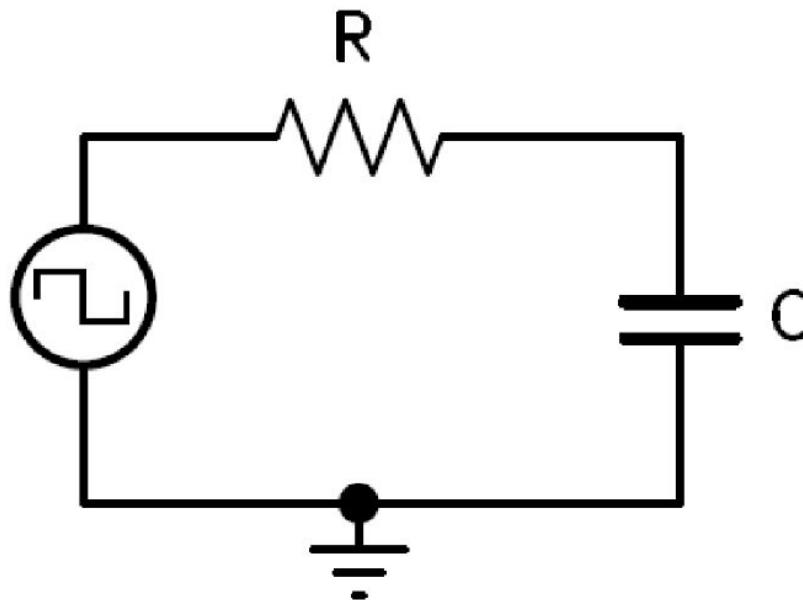


Figure 2.36: RC Integration

2.11.1 Characteristics of RC Integration Circuits

- Think Averaging!
- The output is across the capacitor
- There is not enough time for the capacitor to fully charge or discharge.
- PW and PS is less than 5τ
- $RC \geq (10 \times PW)$
- $PW(\text{time}) \leq \frac{RC}{10}$ (not enough time)
- Additional Formulas:

$$* \text{StabilityCycles} = \frac{5\tau}{\text{Period}}$$

$$* V_{Max} = \frac{V_{gen+}}{1 + e^{\frac{-PW}{RC}}}$$

$$* V_{Min} = V_{gen+} - V_{Max}$$

2.11.2 RC Integration Circuit Example

Calculate an RC Integration Circuit using a $1Khz$ frequency and a $1\mu F$ capacitor.

Given:

- $V_{gen} = 0\text{vp}$ to 10vp , 50% DC, square-wave.
- $F_{gen} = 1Khz$
- $C = 1\mu F$

Find charge/discharge time($time$):

$$Period = \frac{1}{Frequency}$$

$$Period = \frac{1}{1Khz}$$

$$Period = 1mS$$

$$time = \frac{Period}{2}$$

$$time = \frac{1mS}{2}$$

$time = 0.5mS$

Find the series resistance (R):

$$PW(\text{time}) \leq \frac{RC}{10}$$

$$0.5mS \leq \frac{R(1\mu F)}{10}$$

$$5mS \leq R(1\mu F)$$

$$\frac{5mS}{1\mu F} \leq R$$

$$R \geq \frac{5mS}{1\mu F}$$

$$R \geq 5K\Omega$$

Find the number of cycles to stabilization ($Stability_{Cycles}$):

$$Stability_{Cycles} = \frac{5\tau}{\text{Period}}$$

$$Stability_{Cycles} = \frac{5(5K\Omega \times 1\mu F)}{1mS}$$

$$Stability_{Cycles} = \frac{5(5mS)}{1mS}$$

$$Stability_{Cycles} = \frac{25mS}{1mS}$$

$$Stability_{Cycles} = 25_{Cycles}$$

Find V_{Max} :

$$V_{Max} = \frac{V_{gen+}}{1 + e^{\frac{-PW}{RC}}}$$

$$V_{Max} = \frac{10vp}{1 + e^{\frac{-0.5mS}{5K\Omega \times 1\mu F}}}$$

$$V_{Max} = \frac{10vp}{1 + e^{\frac{-0.5mS}{5K\Omega \times 1\mu F}}}$$

$$V_{Max} = \frac{10vp}{1 + 0.905}$$

$V_{Max} = 5.250vp$

Find V_{Min} :

$$V_{Min} = V_{gen+} - V_{Max}$$

$$V_{Min} = 10vp - 5.250vp$$

$V_{Min} = 4.750vp$

*****Add here Measured Image Integrator Gen=10vp squarewave 1KHZ Waveform,
 $R=5K$, $C=1\text{microF}$ *****

2.12 RC Differentiation

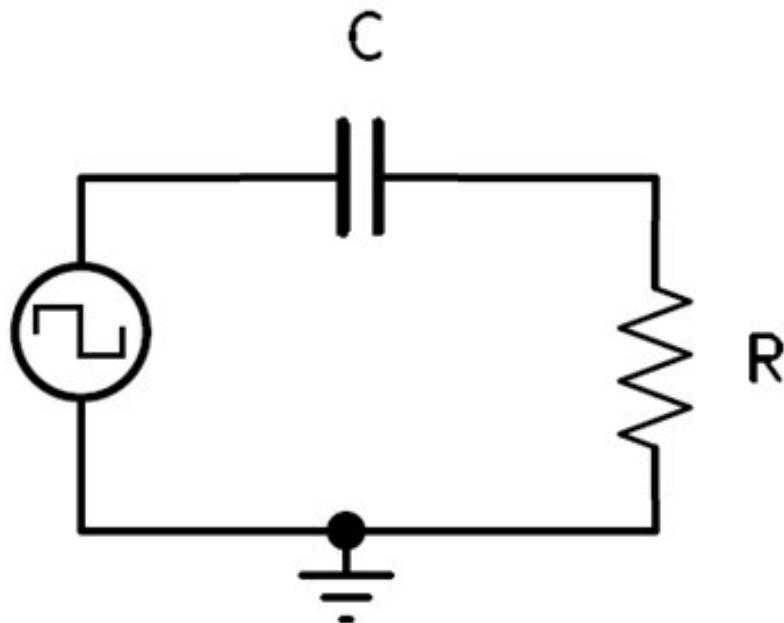


Figure 2.37: RC Differentiation

2.12.1 Characteristics of RC Differentiation Circuits

- When RC is less than one-tenth of the pulse width, the capacitor is charged very rapidly. Only a brief pulse of current is necessary to charge and discharge the capacitor at the beginning and end of the pulse. The resultant waveform of the resistor voltage is a series of positive and negative spikes at the pulse leading and lagging edges, respectively. Bell p.56[6]
- The output is across the resistor.
- There is more than enough time for the capacitor to fully charge or discharge.
- PW and PS is more than 5τ
- $RC \leq \frac{PW}{10}$
- $PW(\text{time}) \geq 10 \times RC$ (lots of time)

2.12.2 RC Differentiation Circuit Example

Calculate an RC Differentiation Circuit using a $1Khz$ frequency and a $1\mu F$ capacitor.

Given:

- $V_{gen} = 0vp$ to $10vp$, 50% DC, square-wave.
- $F_{gen} = 1Khz$
- $R = 5K\Omega$

Find charge/discharge time(*time*):

$$\text{Period} = \frac{1}{\text{Frequency}}$$

$$\text{Period} = \frac{1}{1Khz}$$

$$\text{Period} = 1mS$$

$$\text{time} = \frac{\text{Period}}{2}$$

$$\boxed{\text{time} = 0.5mS}$$

Find the series capacitance (C):

$$PW(\text{time}) \geq 10 \times RC$$

$$0.5mS \geq 10 \times 5K\Omega \times C$$

$$0.5mS \geq 50K\Omega \times C$$

$$\frac{0.5mS}{50K\Omega} \geq C$$

$$C = 10nF \text{ or } 10,000pF$$

Calculating the capacitor voltage based on Tau:

In Section 2.9 Capacitor Charge Formula the capacitor charge formula was simplified in terms of Tau. We can now apply this to our current example to find the capacitor charge voltage in terms of Tau and percentage of charge. Additionally, the same percentages also apply to the discharge time of a capacitor. For this example the capacitor was initially charged to 10V and will discharge 63.212% at 1τ leaving the capacitor voltage at 3.679V. Table ?? ?? has the compiled data and Figure 2.38 RC Differentiation, Generator and Capacitor Waveforms shows a graph of the generator and capacitor waveform voltages.

Once the capacitor voltages are calculated, the resistor voltage can be determined using Kirchhoff's Voltage Law. A tricky spot to pay attention to is the points where the generator voltage is vertical, 0 to 10v & 10v to 0. For example, you will need to do two Kirchhoff calculations at time equals 0.5mS, one where the generator voltage is equal to 0V and one where the generator voltage is equal to 10V. See Figure 2.39 RC Differentiation, Generator, Capacitor, and Resistor Waveforms. Notice how the resistor voltage goes negative, this is because at the instance that the generator voltage goes to zero, the capacitor voltage is still 10V, therefore to Kirchhoff, the resistor voltage must go negative.

$$V_R = V_{Gen} - V_C$$

Table 2.3: RC Circuits Capacitor Voltage

Capacitor Charge				
Tau	Time	Generator Voltage	VC % of Charge	Capacitor Voltage
0	$0\mu\text{S}$	10V	0%	0V
1	$50\mu\text{S}$	10V	63.212%	6.321V
2	$100\mu\text{S}$	10V	86.466%	8.647V
3	$150\mu\text{S}$	10V	95.021%	9.502V
4	$200\mu\text{S}$	10V	98.168%	9.817V
5	$250\mu\text{S}$	10V	99.326%	9.933V
$\geq 5\tau$	$500\mu\text{S}$	10V	100%	10V
250 μS to 500 μS the capacitor is fully charged to 10V				
Capacitor Discharge				
Tau	Time	Generator Voltage	VC % of Discharge	Capacitor Voltage
0	$500\mu\text{S}$	0V	0%	10V
1	$550\mu\text{S}$	0V	63.212%	3.679V
2	$600\mu\text{S}$	0V	86.466%	1.353V
3	$650\mu\text{S}$	0V	95.021%	0.498V
4	$700\mu\text{S}$	0V	98.168%	0.183V
5	$750\mu\text{S}$	0V	99.326%	0.067V
$\geq 5\tau$	1mS	0V	100%	0V

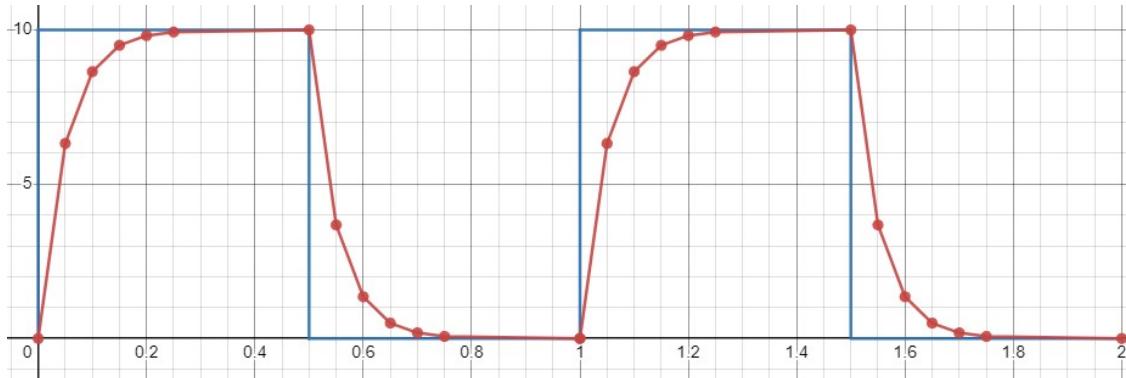
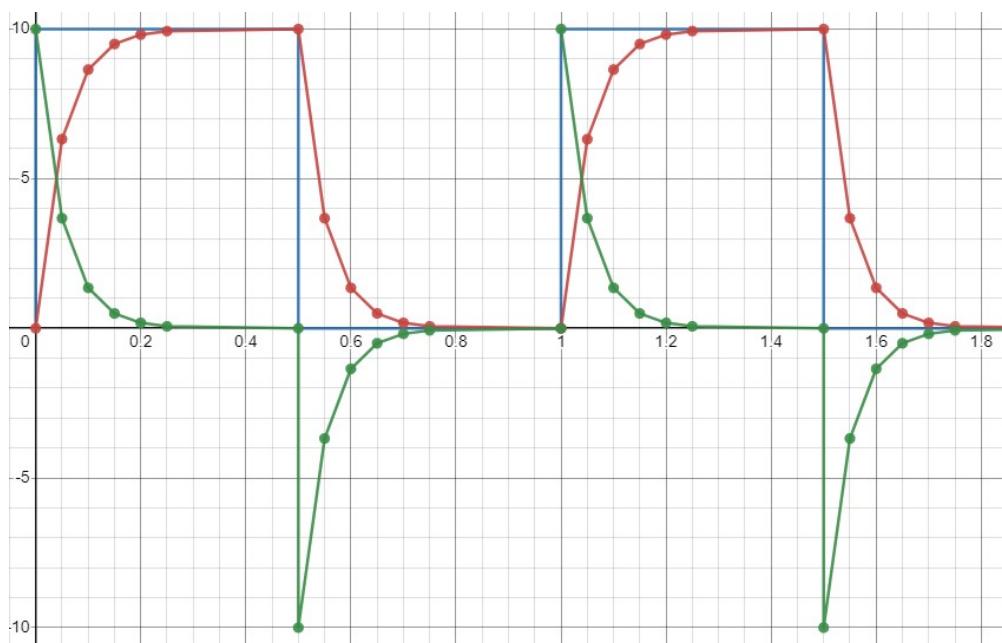
**Figure 2.38:** RC Differentiation, Generator and Capacitor Waveforms

Table 2.4: RC Circuits Capacitor & Resistor waveform voltages

Capacitor Charge					
Tau	Time	Generator Voltage	VC % of Charge	Capacitor Voltage	Resistor Voltage
0	0 μ S	10V	0%	0V	10V
1	50 μ S	10V	63.212%	6.321V	3.679V
2	100 μ S	10V	86.466%	8.647V	1.353V
3	150 μ S	10V	95.021%	9.502V	0.498V
4	200 μ S	10V	98.168%	9.817V	0.183V
5	250 μ S	10V	99.326%	9.933V	0.067V
$\geq 5\tau$	500 μ S	10V	100%	10V	0V

250 μ S to 500 μ S the capacitor is fully charged to 10V

Capacitor Discharge					
Tau	Time	Generator Voltage	VC % Discharge	Capacitor Voltage	Resistor Voltage
0	500 μ S	0V	0%	10V	-10V
1	550 μ S	0V	63.212%	3.679V	-3.679V
2	600 μ S	0V	86.466%	1.353V	-1.353V
3	650 μ S	0V	95.021%	0.498V	-0.498V
4	700 μ S	0V	98.168%	0.183V	-0.183V
5	750 μ S	0V	99.326%	0.067V	-0.067V
$\geq 5\tau$	1mS	0V	100%	0V	0V

**Figure 2.39:** RC Differentiation, Generator, Capacitor, and Resistor Waveforms

2.13 Sine-waves and Instantaneous Voltage

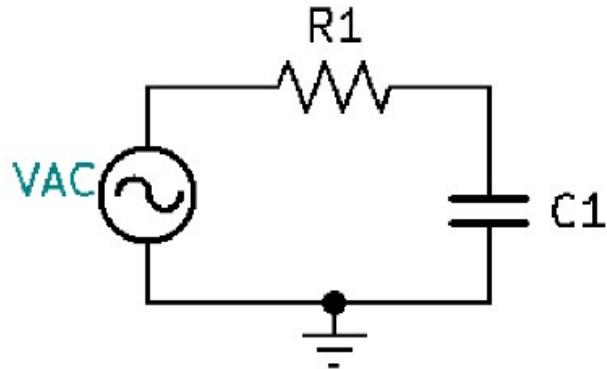


Figure 2.40: RC Circuit Sine-wave

2.13.1 Sine-wave analysis at resonance (F_C):

Consider Figure 2.40 RC Circuit Sine-wave.

Formulas:

- At F_C , $X_{C1} = R1$
- $X_{C1} = \frac{1}{2\pi F_C C1}$
- $R1 = \frac{1}{2\pi F_C C1}$
- ✓ $F_C = \frac{1}{2\pi R1 C1}$

- ✓ $Z_T = \sqrt{(R1)^2 + (X_{C1})^2}$, $\angle = \tan^{-1} \frac{X_{C1}}{R1}$
- ✓ $I_T = \frac{V_{gen}}{Z_T}$
- ✓ $V_{R1} = I_T \times R1$
- ✓ $V_{C1} = I_T \times X_{C1}$
- ✓ $V_{inst} = V_{Max} \sin(360Ft \pm \theta)$

2.13.2 Sine-wave Instantaneous Example 1

Consider circuit Figure 2.40, and let's assume that V_{gen} is set to 10vp at 1Khz, and X_{C1} and $R1$ both are equal to $1K\Omega$.

Given:

- $V_{gen} = 10vp \angle 0^\circ, 1Khz$
- $X_{C1} = 1K\Omega \angle -90^\circ$
- $R1 = 1K\Omega \angle 0^\circ$

Find: $Z_T, I_T, V_R, V_C, VGen_{inst}, VR_{inst}, VC_{inst}$

Solve:

$$Z_T = \sqrt{(R1)^2 + (X_{C1})^2}, \angle = \tan^{-1} \frac{X_{C1}}{R1}$$

$$Z_T = \sqrt{(1K)^2 + (1K)^2}, \angle = \tan^{-1} \frac{-1K}{1K}$$

$Z_T = 1.414K\Omega, \angle = -45^\circ$

$$I_T = \frac{V_{gen}}{Z_T}$$

$$I_T = \frac{10vp \angle 0^\circ}{1.414K\Omega \angle -45^\circ}$$

$I_T = 7.071mA p \angle 45^\circ$

$$V_{R1} = I_T \times R_1$$

$$V_{R1} = 7.071mA p \angle 45^\circ \times 1K\Omega \angle 0^\circ$$

$V_{R1} = 7.071vp \angle 45^\circ$

$$V_{C1} = I_T \times X_C 1$$

$$V_{C1} = 7.071mA p \angle 45^\circ \times 1K\Omega \angle -90^\circ$$

$$V_{C1} = 7.071vp \angle -45^\circ$$

$$V_{inst} = V_{Max} \sin(360Ft \pm \theta)$$

$$V_{Gen_{inst}} = 10vp \sin(360 \times 1Khz \times time \pm 0^\circ)$$

$$V_{R_{inst}} = 7.071vp \sin(360 \times 1Khz \times time + 45^\circ)$$

$$V_{C_{inst}} = 7.071vp \sin(360 \times 1Khz \times time - 45^\circ)$$

Table 2.5: Instantaneous Voltages for Example 1. section 2.13.2

Time	VGen	VR1	VC1
0μS	0.000vp	5.000vp	-5.000vp
50μS	3.090vp	6.300vp	-3.210vp
100μS	5.878vp	6.984vp	-1.106vp
150μS	8.090vp	6.984vp	1.106vp
200μS	9.511vp	6.300vp	3.210vp
250μS	10.00vp	5.000vp	5.000vp
300μS	9.511vp	3.210vp	6.300vp
350μS	8.090vp	1.106vp	6.984vp
400μS	5.878vp	-1.106vp	6.984vp
450μS	3.090vp	-3.210vp	6.300vp
500μS	0.000vp	-5.000vp	5.000vp
550μS	-3.090vp	-6.300vp	3.210vp
600μS	-5.878vp	-6.984vp	1.106vp
650μS	-8.090vp	-6.984vp	-1.106vp
700μS	-9.511vp	-6.300vp	-3.210vp
750μS	-10.00vp	-5.000vp	-5.000vp
800μS	-9.511vp	-3.210vp	-6.300vp
850μS	-8.090vp	-1.106vp	-6.984vp
900μS	-5.878vp	1.106vp	-6.984vp
950μS	-3.090vp	3.210vp	-6.300vp
1mS	0.000vp	5.000vp	-5.000vp

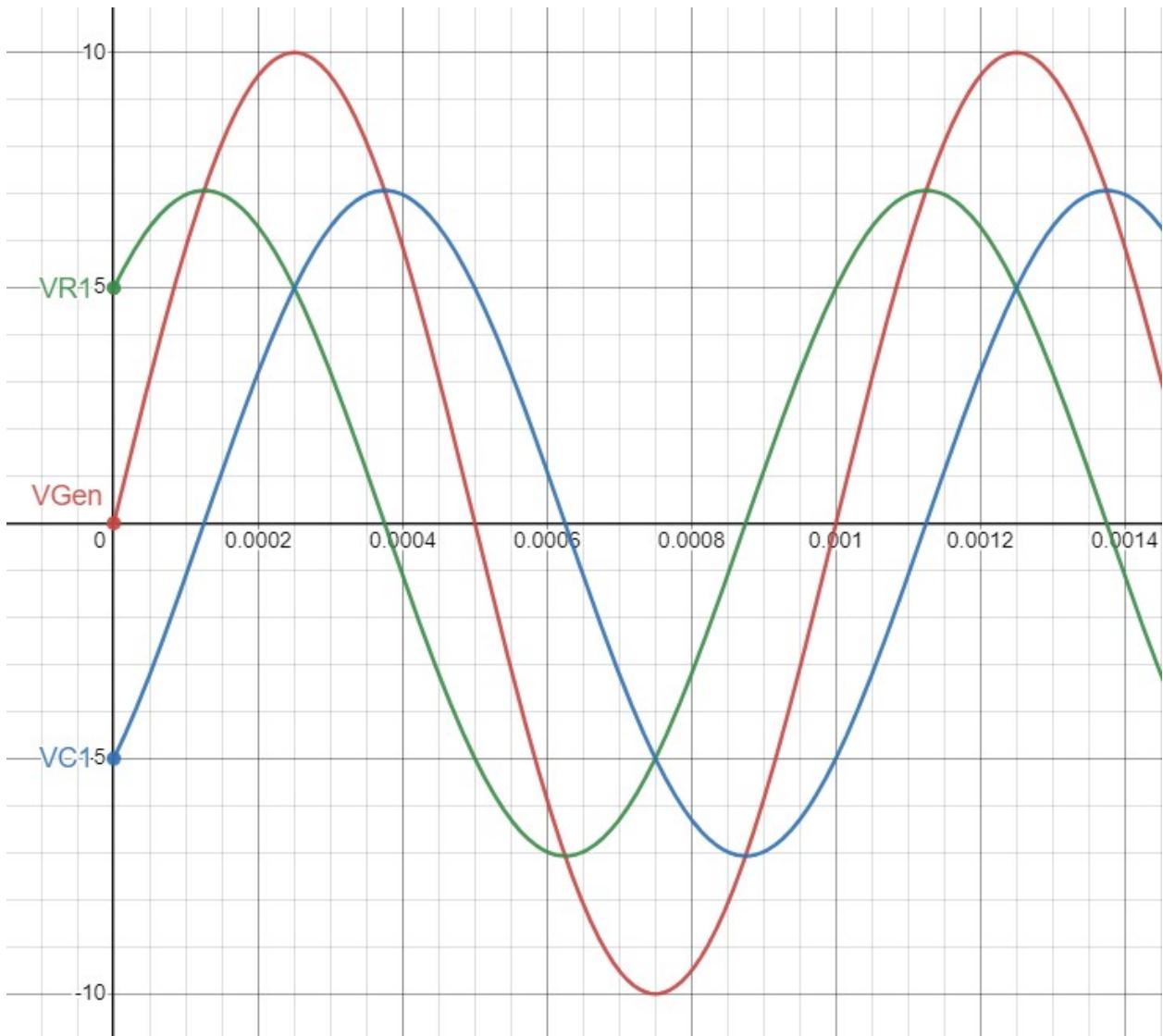


Figure 2.41: RC Circuit Instantaneous Waveforms Example 1. section 2.13.2

2.13.3 Sine-wave Instantaneous Example 2

What happens if double the resistance of the previous example?

Given:

- $V_{gen} = 10vp \angle 0^\circ, 1Khz$
- $X_{C1} = 1K\Omega \angle -90^\circ$
- $R1 = 2K\Omega \angle 0^\circ$

Find: $Z_T, I_T, V_R, V_C, VGen_{inst}, VR_{inst}, VC_{inst}$

Solve:

$$Z_T = \sqrt{(R1)^2 + (X_{C1})^2}, \angle = \tan^{-1} \frac{X_{C1}}{R1}$$

$$Z_T = \sqrt{(2K)^2 + (1K)^2}, \angle = \tan^{-1} \frac{-1K}{2K}$$

$Z_T = 2.236K\Omega, \angle = -26.565^\circ$

$$I_T = \frac{V_{gen}}{Z_T}$$

$$I_T = \frac{10vp \angle 0^\circ}{2.236K\Omega \angle -26.565^\circ}$$

$I_T = 4.472mA p \angle 26.565^\circ$

$$V_{R1} = I_T \times R_1$$

$$V_{R1} = 4.472mA p \angle 26.565^\circ \times 2K\Omega \angle 0^\circ$$

$V_{R1} = 8.944vp \angle 26.565^\circ$

$$V_{C1} = I_T \times X_C 1$$

$$V_{C1} = 4.472mA p \angle 26.565^\circ \times 1K\Omega \angle -90^\circ$$

$$V_{C1} = 4.472vp \angle -63.435^\circ$$

$$V_{inst} = V_{Max} \sin(360Ft \pm \theta)$$

$$V_{Gen_{inst}} = 10vp \sin(360 \times 1Khz \times time \pm 0^\circ)$$

$$V_{R_{inst}} = 8.944vp \sin(360 \times 1Khz \times time + 26.565^\circ)$$

$$V_{C_{inst}} = 4.472vp \sin(360 \times 1Khz \times time - 63.435^\circ)$$

Table 2.6: Instantaneous Voltages for Example 2. section 2.13.3

Time	VGen	VR1	VC1
0μS	0.000vp	4.000vp	-4.000vp
50μS	3.090vp	6.276vp	-3.186vp
100μS	5.878vp	7.938vp	-2.060vp
150μS	8.090vp	8.823vp	-0.733vp
200μS	9.511vp	8.844vp	0.666vp
250μS	10.00vp	8.000vp	2.000vp
300μS	9.511vp	6.372vp	3.138vp
350μS	8.090vp	4.121vp	3.969vp
400μS	5.878vp	1.466vp	4.412vp
450μS	3.090vp	-1.332vp	4.422vp
500μS	0.000vp	-4.000vp	4.000vp
550μS	-3.090vp	-6.276vp	3.186vp
600μS	-5.878vp	-7.938vp	2.060vp
650μS	-8.090vp	-8.823vp	0.733vp
700μS	-9.511vp	-8.844vp	-0.666vp
750μS	-10.00vp	-8.000vp	-2.000vp
800μS	-9.511vp	-6.372vp	-3.138vp
850μS	-8.090vp	-4.121vp	-3.969vp
900μS	-5.878vp	-1.466vp	-4.412vp
950μS	-3.090vp	1.332vp	-4.422vp
1mS	0.000vp	4.000vp	-4.000vp

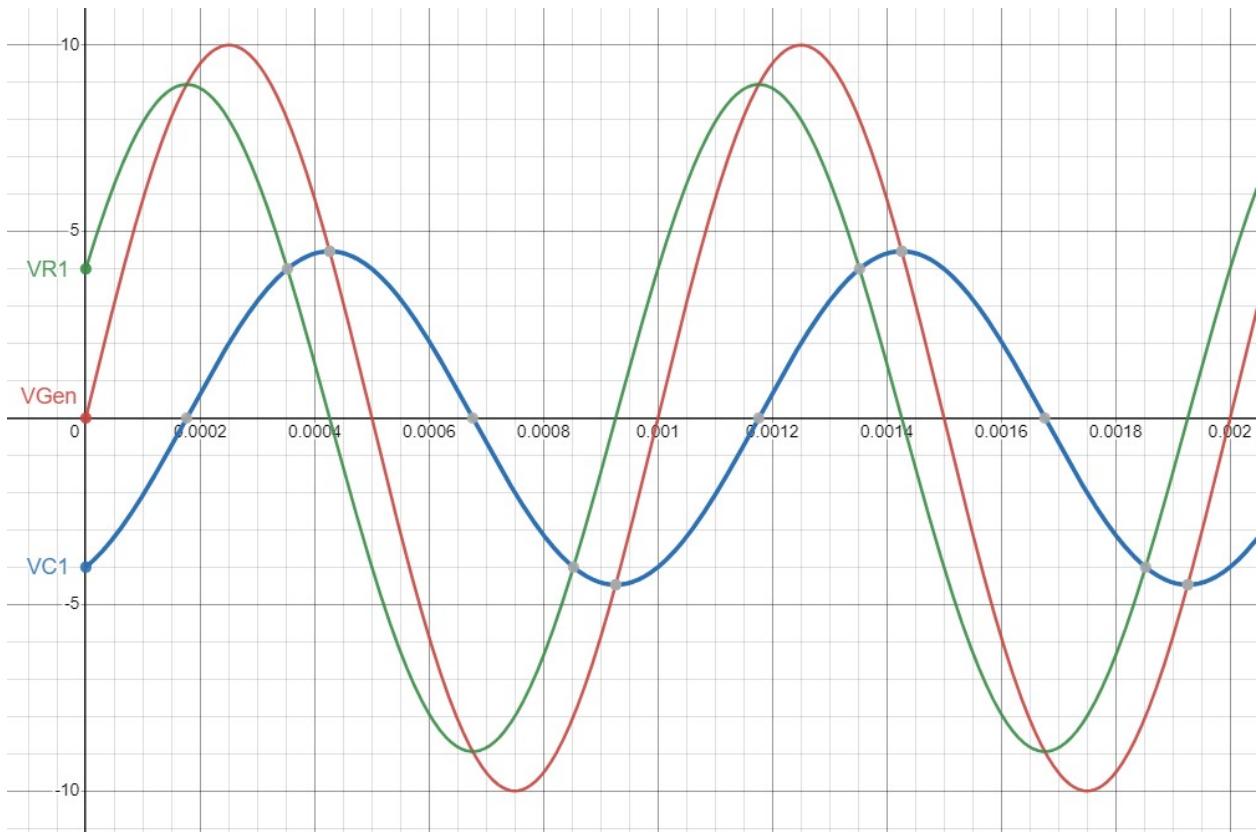


Figure 2.42: RC Circuit Instantaneous Waveforms Example 2. section 2.13.3

2.14 RC Circuits Questions

2.3 Graphs and Waveforms

1. On the graph, this axis represents the independent variable. (select all that apply)
 - X-Axis
 - Horizontal-Axis
 - Y-Axis
 - Vertical-Axis
2. This axis on the graph is used to represent the dependent variable. (select all that apply)
 - X-Axis
 - Horizontal-Axis
 - Y-Axis
 - Vertical-Axis
3. The point on the graph, where the two axis intersect is called the _____.
4. A _____ waveform is a type of waveform that repeats its shape over regular intervals of time.
5. _____ waveforms do not exhibit a regular and repeating pattern over time.
6. Common examples of periodic waveforms include which of the following waveforms?
 - Sine
 - Ramp
 - Noise
 - Sawtooth
 - Exponetial

2.4 Pulse Waveform Characteristics

Matching:

1. _____ Period

5. _____ DC%

9. _____ Tilt%

2. _____ PW

6. _____ t_r

10. _____ AWV

3. _____ PS

7. _____ t_f

4. _____ PRF

8. _____ APA

(a) $= \frac{(+APA \times PW) + (-APA \times PS)}{Period}$

(f) Time Low/Off

(b) The time it takes for one cycle.

(g) The time required for the voltage to go from 90% to 10% of APA.

(c) $= \frac{V_{max} - V_{min}}{APA} \times 100$

(h) $= \frac{1}{Period}$

(d) Time High/On

(i) $= \frac{PW}{Period} \times 100$

(e) $= \frac{V_{max} + V_{min}}{2}$

(j) The time required for the voltage to go from 10% to 90% of APA.

Questions:

- The _____ waveform has perfectly vertical leading and lagging edges and perfectly flat tops and bottoms.
- PW and PS are measured at _____ of the waveform amplitude.
- What is the DC% of a 1Khz waveform having with a pulse width equal to $250\mu S$? Answer _____ %.
- What is the APA of a pulse that has a Vmax equal to 1.5V and a Vmin equal to 1V? Answer _____ V.
- What is the Tilt% of a pulse that has a Vmax equal to 1.5V and a Vmin equal to 1V? Answer _____ %.
- What is the AWV if +APA is equal to 10V and -APA is equal to -8V and PW is equal to $10\mu S$ and PS is equal to $20\mu S$? Answer _____ V.

2.5 Frequency Synthesis & Analysis

1. _____ involves combining two or more signals to create a new waveform.
2. Select each true statement concerning Harmonics:
 - A harmonic is a multiple of the fundamental.
 - Harmonics are numbered according to their ratio to the fundamental.
 - The number of harmonics is infinite.
 - The 5th harmonic frequency is equal to 5 times the Fundamental Frequency and the 5th harmonic amplitude is equal to the Fundamentals Amplitude divided by 5.
3. A Perfect Square Wave is comprised of an infinite number of _____ harmonic sine waves.
4. _____ involves breaking down a complex waveform into its individual sinusoidal components or harmonics.
5. _____ is a mathematical technique used to decompose a complex waveform into its individual sinusoidal components, representing different frequencies.
6. FFT stands for _____.
7. FFT can be used to analyze which of the following:
 - Analyze harmonics in power lines
 - Measure harmonic content and distortion in systems
 - Characterize noise in DC power supplies
 - Test impulse response of filters and systems
 - Analyze vibration

2.6 Waveform Distortion

1. The two types of square wave distortion that are useful for circuit frequency response analysis are _____ and _____ .

2.7 Tilt and Frequency Critical Low (FC_L)

1. _____ capacitance will attenuate frequencies below FC_L .
2. _____ represents the square wave distortion and attenuation of low frequencies.
3. FC_{Low} is equal to _____ divided by 2π _____ .
4. What is FC_{Low} if the measured Tilt is 49.867% on a 630hz square wave.
Answer: $FC_{Low} =$ _____ hz.

2.8 Rise Time t_r and Frequency Critical High FC_H

1. The attenuation of high frequencies is caused by _____ capacitance and will affect the _____ _____ of a measured square wave.
2. FC_{High} is equal to _____ divided by _____ .
3. If the measured Rise Time is $35\mu S$, $FC_{High} =$ _____ Khz.

2.9 Capacitor Charge Formula

1. At what percent of the Final Voltage will a capacitor charge in 1τ ?
Answer _____ %
2. At what percent of the Final Voltage will a capacitor charge in 2τ ?
Answer _____ %
3. At what percent of the Final Voltage will a capacitor charge in 3τ ?
Answer _____ %
4. At what percent of the Final Voltage will a capacitor charge in 4τ ?
Answer _____ %
5. At what percent of the Final Voltage will a capacitor charge in 5τ ?
Answer _____ %

2.10 RC Circuits Stability, Vmax & Vmin Calculations

Matching:

- | | |
|---|--|
| 1. _____ $V_{Capacitor}$ | 3. _____ V_{Max} |
| 2. _____ $Stability_{Cycles}$ | 4. _____ V_{Min} |
| (a) $= V_{gen+} - V_{Max}$ | (c) $= \frac{5\tau}{Period}$ |
| (b) $= \frac{V_{gen+}}{1+e^{\frac{-PW}{RC}}}$ | (d) $= V_{Final} - (V_{Final} - V_{Initial})e^{\frac{-t}{\tau}}$ |

Questions:

1. How many cycles will it take for the output to stabilize if the square wave frequency is 1Khz and τ is equal to 2mS? Answer _____ cycles.
2. If the square wave voltage in question 1. is set at 0 to 10v, what is the stabilized V_{Max} ?
Answer $V_{Max} =$ _____ V.
3. Considering the previous questions, What is V_{Min} ? Answer $V_{Min} =$ _____ V.

2.11 RC Integration

1. Correctly select the **RC Integration Formula(s)** from the following:

- $RC \geq (10 \times PW)$
- $RC \leq (10 \times PW)$
- $PW \geq \frac{RC}{10}$
- $PW \leq \frac{RC}{10}$

2. Calculate the correct capacitance for an integrator circuit operating at 5Khz with a series resistance of $4.7\text{K}\Omega$. Select the correct answer:

- $0.220\mu\text{F}$
- $0.210\mu\text{F}$
- $0.120\mu\text{F}$
- $0.110\mu\text{F}$

3. For the previous question, Calculate the Cycles to Stabilization, V_{Max} , and V_{Min} with a generator voltage that is 0V to 10Vp.

Stability = _____ cycles

V_{Max} = _____ V

V_{Min} = _____ V

2.12 RC Differentiation

1. Correctly select the **RC Differentiation Formula(s)** from the following:

- $PW \geq (10 \times RC)$
- $PW \leq (10 \times RC)$
- $RC \geq \frac{PW}{10}$
- $RC \leq \frac{PW}{10}$

2. Calculate the correct capacitance for a differentiating circuit operating at 5Khz with a series resistance of $4.7\text{K}\Omega$. Select the correct answer:

- $0.022\mu\text{F}$
- $0.021\mu\text{F}$
- $2,200\text{pF}$
- $2,100\text{pF}$

2.13 Sine-waves and Instantaneous Voltage

Matching:

1. ____ At F_C ,

4. ____ Z_T

7. ____ V_{Inst}

2. ____ X_C

5. ____ \angle

3. ____ F_C

6. ____ I_T

$$(a) = V_{Max} \sin(360Ft \pm \theta)$$

$$(e) = \frac{V_T}{Z_T}$$

$$(b) \sqrt{(R)^2 + (X_C)^2}$$

$$(f) = \frac{1}{2\pi RC}$$

$$(c) X_C = R$$

$$(g) = \frac{1}{2\pi FC}$$

$$(d) = \tan^{-1} \frac{X_C}{R}$$

Questions:

- If a series RC circuit is operating at resonance with a generator voltage is $10vp$, $1Khz$ and circuit resistance equal to $2K\Omega$. Find the generator, resistor, and capacitor instantaneous voltage after $0.375mSec$.

$$V_{Gen_{0.375mS}} = \text{_____ } V$$

$$V_{R_{0.375mS}} = \text{_____ } V$$

$$V_{C_{0.375mS}} = \text{_____ } V$$

Chapter 3

Multi-Stage Amplifier: Design, Circuit Analysis, and Low-Frequency Response

3.1 Objectives:

Multi-Stage Amplifier Design and Analysis:

DC Biasing Calculations - Kirchhoff's and Thevenin Review.

- Kirchhoff's Laws: Students should be able to apply Kirchhoff's laws for DC biasing calculations in multi-stage amplifiers, considering voltage and current relationships in transistor amplifier circuits.
- Thevenin Equivalent: Understand and utilize Thevenin's theorem in transistor DC biasing calculations for simplifying complex circuits into simpler equivalent circuits.

AC Gain Calculations.

- AC Gain Analysis: Develop proficiency in calculating AC voltage gain for multi-stage amplifiers, considering the configuration and characteristics of each stage.

Load-Lines, Vout Max, and Vin Max.

- Load-Line Analysis: Understand load-line concepts and how to use them for analyzing the performance of multi-stage amplifiers.
- Vout Max Calculation: Calculate the maximum output voltage ($V_{out\ Max}$) for a multi-stage amplifier, considering various factors and load conditions.
- Vin Max Calculation: Calculate the maximum input voltage ($V_{in\ Max}$) that can be applied to a multi-stage amplifier without distortion or clipping.

Critical Frequencies.

- Low Critical Frequency (FCL): Understand and calculate the low critical frequency (FCL) for multi-stage amplifiers, considering the impact of coupling and bypass capacitors.
- High Critical Frequency (FCH): Understand and calculate the high critical frequency (FCH) for multi-stage amplifiers, taking into account the internal capacitances and parasitic elements in the amplifier stages.

By achieving these objectives, students will develop a comprehensive understanding of DC biasing calculations, AC gain, load-line analysis, maximum output and input voltage calculations, and critical frequencies for multi-stage amplifiers. These objectives aim to enhance their proficiency in designing and analyzing multi-stage amplifier circuits, particularly in terms of frequency response.

3.2 Circuit Design, DC Biasing Stage 2:

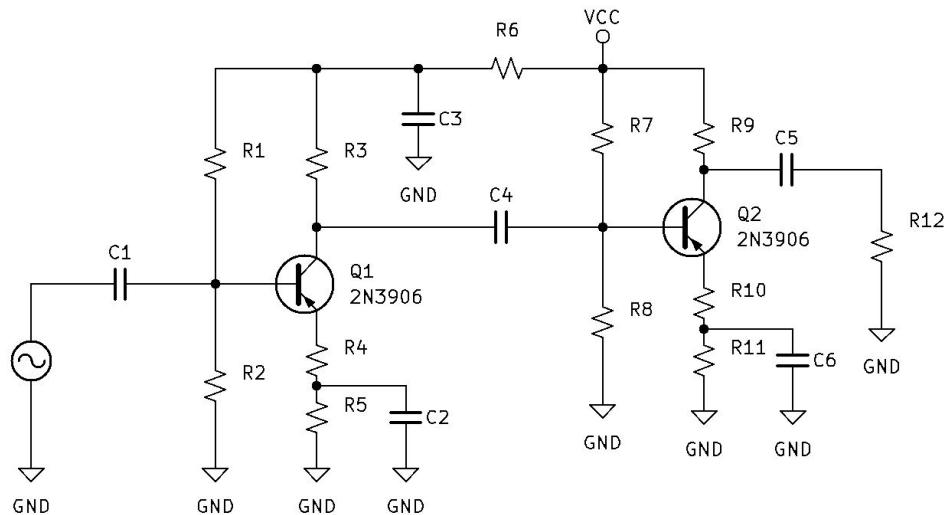


Figure 3.1: Two Stage Amplifier

Determine the Maximum Power for the 2N3906 Transistor

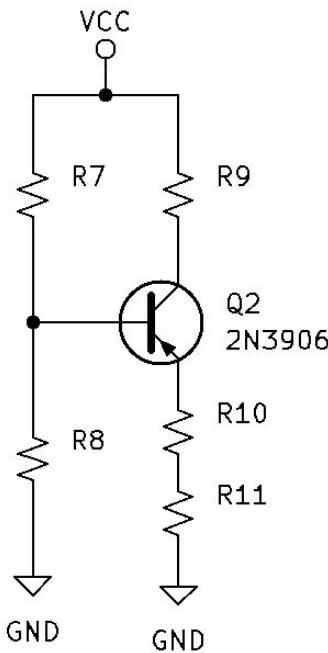
See Figure 3.2. P_D Total Device Dissipation.

DC Redraw for Stage 2:

Complete a DC redraw of the second stage of the amplifier making note of the DC biasing voltage polarities for each resistor and the transistor. See Figure 3.3.

Thermal CharacteristicsValues are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Maximum			Unit
		2N3906 ⁽³⁾	MMBT3906 ⁽²⁾	PZT3906 ⁽³⁾	
P_D	Total Device Dissipation	625	350	1,000	mW
	Derate Above 25°C	5.0	2.8	8.0	mW/ $^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	$^\circ\text{C}/\text{W}$

Figure 3.2: Maximum Power for the 2n3906 transistor**Figure 3.3:** Second Stage DC Redraw**Determine Optimized Voltages and Transistor Power:**

Optimize the biasing voltage using the 45, 45, 10 VCC ratios.

Voltage Optimization:

$$V_{RC} = 45\%VCC$$

$$V_{CE} = 45\%VCC$$

$$V_{RE} = 10\%VCC$$

Make the transistor power \approx half of the Maximum Power.

Q2 Power:

$$P_{Q2} = \frac{P_{MAX}}{2} = 0.5P_{MAX}$$

Collector Current:

$$P_{Q2} = IC \times V_{CE}$$

$$IC = \frac{P_{Q2}}{V_{CE}}$$

$$IC = \frac{P_{MAX}}{2V_{CE}}$$

$$IC = \frac{P_{MAX}}{2 \times 45\%VCC}$$

$$IC = \frac{P_{MAX}}{0.9VCC}$$

Base Current:

$$IB = \frac{IC}{Beta}$$

$$Beta_{2N3906} \approx 200$$

$$IB = \frac{P_{MAX}}{0.9VCC \times 200}$$

$$IB = \frac{P_{MAX}}{180VCC}$$

Emitter Current:

$$IE = IB \times (Beta + 1)$$

$$IE = \frac{P_{MAX}}{180VCC} \times (200 + 1)$$

$$IE = \frac{P_{MAX} \times 201}{180VCC}$$

$$IE = \frac{67P_{MAX}}{60VCC}$$

R9:

$$R9 = \frac{V_{R8}}{I_{R8}}$$

$$R9 = \frac{45\%VCC}{I_C}$$

$$R9 = \frac{45\%VCC}{\frac{P_{MAX}}{0.9VCC}}$$

$$R9 = \frac{45\%VCC \times 0.9VCC}{P_{MAX}}$$

$$R9 = \frac{0.405VCC^2}{P_{MAX}}$$

Power R9:

$$P_{R9} = IC \times V_{R8}$$

$$P_{R9} = IC \times 45\%VCC$$

$$P_{Q2} = IC \times 45\%VCC$$

$$P_{R9} = P_{Q2}$$

$$P_{R9} = \frac{P_{MAX}}{2} = 0.5P_{MAX}$$

RE = R10 + R11:

$$RE = \frac{V_{RE}}{I_{R9}}$$

$$RE = \frac{V_{RE}}{I_E}$$

$$RE = \frac{10\%VCC}{I_E}$$

$$RE = \frac{10\%VCC}{\frac{67P_{MAX}}{60VCC}}$$

$$RE = \frac{6VCC^2}{67P_{MAX}}$$

Power RE ($P_{R10} + P_{R11}$)

$$P_{RE} = IE \times V_{R9}$$

$$P_{RE} = \frac{67P_{MAX}}{60VCC} \times 10\%VCC$$

$$P_{RE} = \frac{6.7P_{MAX} \times VCC}{60VCC}$$

$$P_{RE} = \frac{6.7P_{MAX}}{60}$$

R8:

$$R8 = \frac{V_{R8}}{I_{R8}}$$

$$V_{R8} = V_{RE} + V_{BE}$$

$$V_{R8} = 10\%VCC + 0.7V$$

$$I_{R8} = IB \times 10$$

$$I_{R8} = \frac{P_{MAX}}{180VCC} \times 10$$

$$I_{R8} = \frac{10P_{MAX}}{180VCC}$$

$$I_{R8} = \frac{P_{MAX}}{18VCC}$$

Multi-Stage Amplifier: Design, Circuit Analysis, and Low-Frequency Response

$$R8 = \frac{10\%VCC + 0.7V}{\frac{P_{MAX}}{18VCC}}$$

$$R8 = \frac{18VCC(10\%VCC + 0.7V)}{P_{MAX}}$$

$$R8 = \frac{1.8VCC^2 + 12.6VCC}{P_{MAX}}$$

Power R8:

$$P_{R8} = I_{R8} \times V_{R8}$$

$$P_{R8} = \frac{P_{MAX}}{18VCC} \times (10\%VCC + 0.7V)$$

$$P_{R8} = \frac{P_{MAX}(10\%VCC + 0.7V)}{18VCC}$$

R7:

$$R7 = \frac{V_{R7}}{I_{R7}}$$

$$V_{R7} = VCC - V_{R8}$$

$$V_{R7} = VCC - (10\%VCC + 0.7V)$$

$$V_{R7} = VCC - 10\%VCC - 0.7V$$

$$V_{R7} = 0.9VCC - 0.7V$$

$$I_{R7} = I_{R7} + IB$$

$$I_{R7} = \frac{P_{MAX}}{180VCC} + \frac{P_{MAX}}{18VCC}$$

$$I_{R7} = \frac{P_{MAX}}{180VCC} + \frac{10P_{MAX}}{180VCC}$$

$$I_{R7} = \frac{P_{MAX} + 10P_{MAX}}{180VCC}$$

$$I_{R7} = \frac{P_{MAX}(1+10)}{180VCC}$$

$$I_{R7} = \frac{11P_{MAX}}{180VCC}$$

$$R7 = \frac{0.9VCC - 0.7V}{\frac{11P_{MAX}}{180VCC}}$$

$$R7 = \frac{180VCC(0.9VCC - 0.7V)}{11P_{MAX}}$$

$$R7 = \frac{162VCC^2 - 126VCC}{11P_{MAX}}$$

Power R7:

$$P_{R7} = I_{R7} \times V_{R7}$$

$$P_{R7} = \frac{11P_{MAX}}{180VCC} \times (0.9VCC - 0.7V)$$

$$P_{R7} = \frac{P_{MAX}(0.9VCC + 7.7V)}{180VCC}$$

3.3 Gain Calculations for Stage 2

R12

Make R12 ten times larger than R9.

$$R12 = R9 \times 10$$

Determine the Voltage Gain for Stage 2

$$\Delta V = \frac{V_{OUT}}{V_{IN}}$$

$$\Delta V = \frac{IC(R9//R12)}{IB(R10+r'e)(B+1)}$$

$$\Delta V = \frac{IC}{IB} \times \frac{(R9//R12)}{(R10+r'e)(B+1)}$$

$$\Delta V = \beta \times \frac{(R9//R12)}{(R10+r'e)(B+1)}$$

$$\Delta V = \frac{\beta}{\beta+1} \times \frac{(R9//R12)}{(R10+r'e)}$$

$$\Delta V = \alpha \times \frac{(R9//R12)}{(R10+r'e)}$$

$$\Delta V = \frac{\alpha(R9//R12)}{(R10+r'e)}$$

Calculating R10 to set the Desired Gain for Stage 2

Choose the desired gain, $\Delta V_{desired}$ and solve for a $R10$ value.

$$\Delta V_{desired} = \frac{\alpha(R9//R12)}{(R10+r'e)}$$

$$R10 + r'e = \frac{\alpha(R9//R12)}{\Delta V_{desired}}$$

$$R10 = \frac{\alpha(R9//R12)}{\Delta V_{desired}} - r'e$$

R11

$$RE = R10 + R11$$

$$R11 = RE - R10$$

3.4 Circuit Design, DC Biasing Stage 1:

DC Redraw for Stage 1:

Complete a DC redraw of the second stage of the amplifier making note of the DC biasing voltage polarities for each resistor and the transistor. See Figure 3.4.

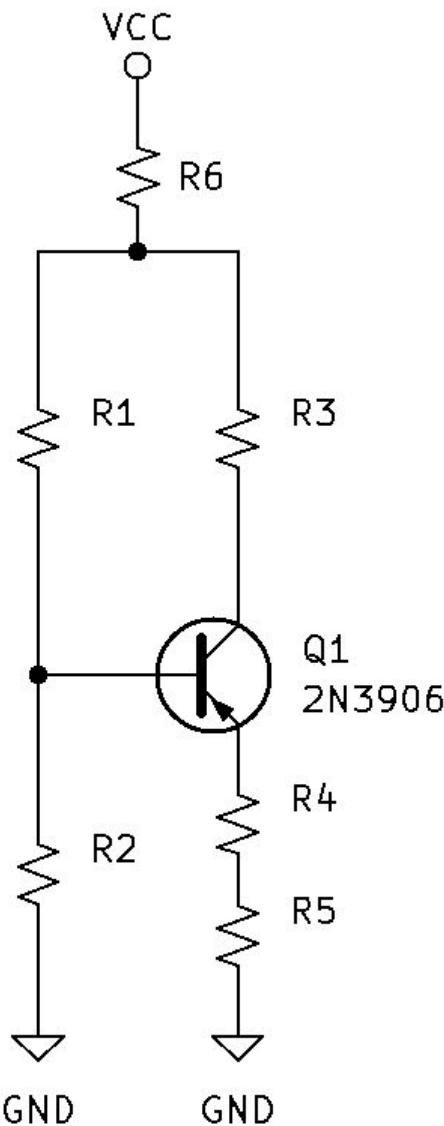


Figure 3.4: First Stage DC Redraw with polarities

Decoupling Resistor R6

The primary objective of the Decoupling Resistor R6 is to prevent oscillations by eliminating any positive feedback from the output of Q2 back to the input of Q1. C2 of Figure 3.1 will act like an AC short to ground allowing any potential feedback signal to be dropped on R6.

Additionally, R6 can be used to significantly lower the power for Q1 if needed.

Find the equivalent load resistance RL_{EqQ1} for Q1:

$$RL_{EqQ1} = ((R10 + r'e_{Q2}) \times (\beta_{Q2} + 1)) // R7 // R8$$

R3:

Make $R3$ ten times smaller than RL_{EqQ1} .

$$R3 = \frac{RL_{EqQ1}}{10}$$

Make P_{R3} equal to half the maximum power of Q1.

$$P_{R3} = \frac{P_{MAXQ1}}{2}$$

Calculate I_{R3} .

$$P = I^2 \times R$$

$$P_{R3} = I_{R3}^2 \times R3$$

$$I_{R3}^2 = \frac{P_{R3}}{R3}$$

$$I_{R3} = \sqrt{\frac{P_{R3}}{R3}}$$

Calculate V_{R3} .

$$P = \frac{V^2}{R}$$

$$P_{R3} = \frac{V_{R3}^2}{R3}$$

$$V_{R3}^2 = P_{R3} \times R3$$

$$V_{R3} = \sqrt{P_{R3} \times R3}$$

Multi-Stage Amplifier: Design, Circuit Analysis, and Low-Frequency Response

Q1:

$$IC = I_{R3}$$

$$IB = \frac{IC}{\beta}$$

$$IE = IB \times (\beta + 1)$$

Make V_{CE} of Q1 equal to V_{R3} .

$$V_{CE} = V_{R3}$$

$$P_{Q1} = P_{R3} = \frac{P_{MAX_{Q1}}}{2}$$

RE:

$$RE = R4 + R5$$

Following the 45, 45, 10 optimization, Find VRE.

$$V_{CE} = .45X$$

$$X = \frac{V_{CE}}{.45}$$

$$V_{RE} = .10X$$

$$X = \frac{V_{RE}}{.10}$$

if X=X, then:

$$\frac{V_{CE}}{.45} = \frac{V_{RE}}{.10}$$

$$V_{RE} = \frac{.10V_{CE}}{.45}$$

$$V_{RE} = \frac{V_{CE}}{4.5}$$

R2:

$$V_{R2} = V_{BE} + V_{RE}$$

$$V_{R2} = 0.7v + V_{RE}$$

Make IR2 ten times larger than the base current of Q1.

$$I_{R2} = IB \times 10$$

$$R2 = \frac{V_{R2}}{I_{R2}}$$

R1:

Find VR1.

$$V_{R1} + V_{R2} = V_{R3} + V_{CE} + V_{RE}$$

$$V_{R1} = V_{R3} + V_{CE} + V_{RE} - V_{R2}$$

Calculate IR1.

$$I_{R1} = I_{R2} + I_B$$

Solve for R1.

$$R1 = \frac{V_{R1}}{I_{R1}}$$

R6:

Find VR6.

$$V_{R2} + V_{R1} + V_{R6} - V_{CC} = 0$$

$$V_{R6} = V_{CC} - V_{R2} - V_{R1}$$

Calculate IR6.

$$I_{R6} = I_{R1} + I_{R3}$$

Solve for R6.

$$R6 = \frac{V_{R6}}{I_{R6}}$$

3.5 Gain Calculations for Stage 1

Find the equivalent load resistance RL_{EqQ1} for Q1:

$$RL_{EqQ1} = ((R10 + r'e_{Q2}) \times (\beta_{Q2} + 1)) // R7 // R8$$

Find $r'e$ for Q1

$$r'e = \frac{0.026}{IE}$$

Multi-Stage Amplifier: Design, Circuit Analysis, and Low-Frequency Response

Determine the Voltage Gain for Stage 1

$$\Delta V = \frac{V_{OUT}}{V_{IN}}$$

$$\Delta V = \frac{IC(R3//RL_{EqQ1})}{IB(R4+r'e)(B+1)}$$

$$\Delta V = \frac{IC}{IB} \times \frac{(R3//RL_{EqQ1})}{(R4+r'e)(B+1)}$$

$$\Delta V = \beta \times \frac{(R3//RL_{EqQ1})}{(R4+r'e)(B+1)}$$

$$\Delta V = \frac{\beta}{\beta+1} \times \frac{(R3//RL_{EqQ1})}{(R4+r'e)}$$

$$\Delta V = \alpha \times \frac{(R3//RL_{EqQ1})}{(R4+r'e)}$$

$$\Delta V = \frac{\alpha(R3//RL_{EqQ1})}{(R4+r'e)}$$

Calculating R4 to set the Desired Gain for Stage 1

Choose the desired gain, $\Delta V_{desired}$ and solve for a $R4$ value.

$$\Delta V_{desired} = \frac{\alpha(R3//RL_{EqQ1})}{(R4+r'e)}$$

$$R4 + r'e = \frac{\alpha(R3//RL_{EqQ1})}{\Delta V_{desired}}$$

$$R4 = \frac{\alpha(R3//RL_{EqQ1})}{\Delta V_{desired}} - r'e$$

R5

$$RE = R4 + R4$$

$$R5 = RE - R4$$

Q2, DC Loadline

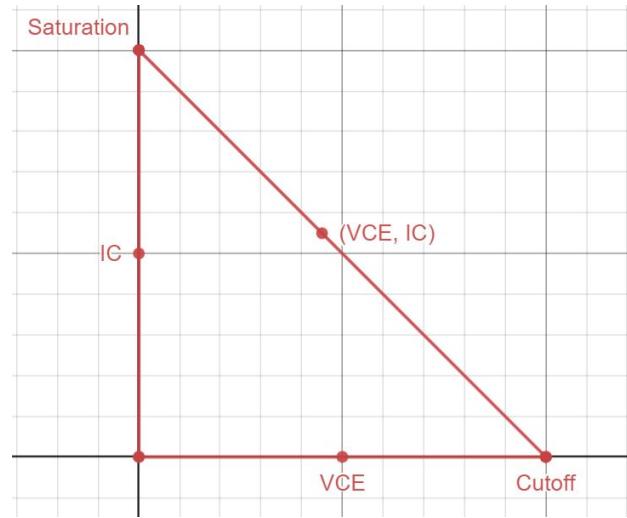


Figure 3.5: Second Stage DC Loadline

IC Saturation in terms of VCC and Max Power:

$$IC_{Sat} = \frac{VCC}{R9+RE}$$

$$IC_{Sat} = \frac{VCC}{\frac{0.405VCC^2}{P_{MAX}} + \frac{6VCC^2}{67P_{MAX}}}$$

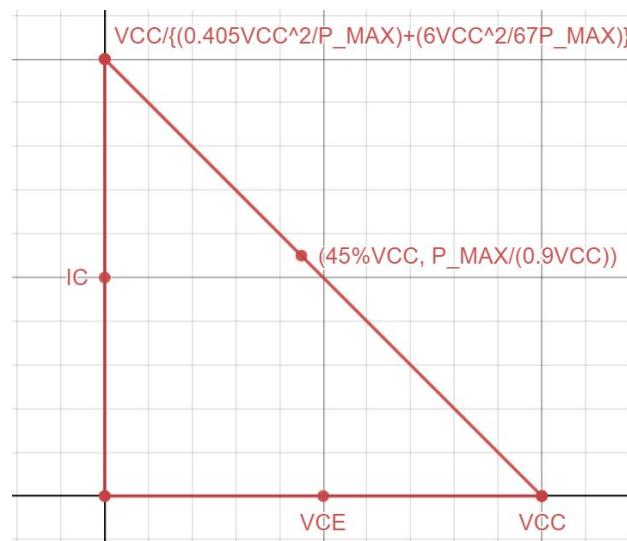


Figure 3.6: Second Stage DC Loadline in Terms of VCC and Max Power

Q2, AC Loadline

Because the load resistor R12 is ten times larger than R9 and the biasing is optimized, $V_{out_{MAXp}}$ will be just less than VCE.

$$V_{out_{MAXp}} \approx 0.9(V_{CE_Q2})$$

$$V_{CE_AC_Cutoff} = V_{CE_Q2} + I_{R9}(R9//R12) \quad IC_{AC_Sat} = I_{R9} + \frac{V_{CE_Q2}}{R9//R12}$$

$$V_{out_{MAXp}} = V_{CE_AC_Cutoff} - V_{CE_Q2}$$

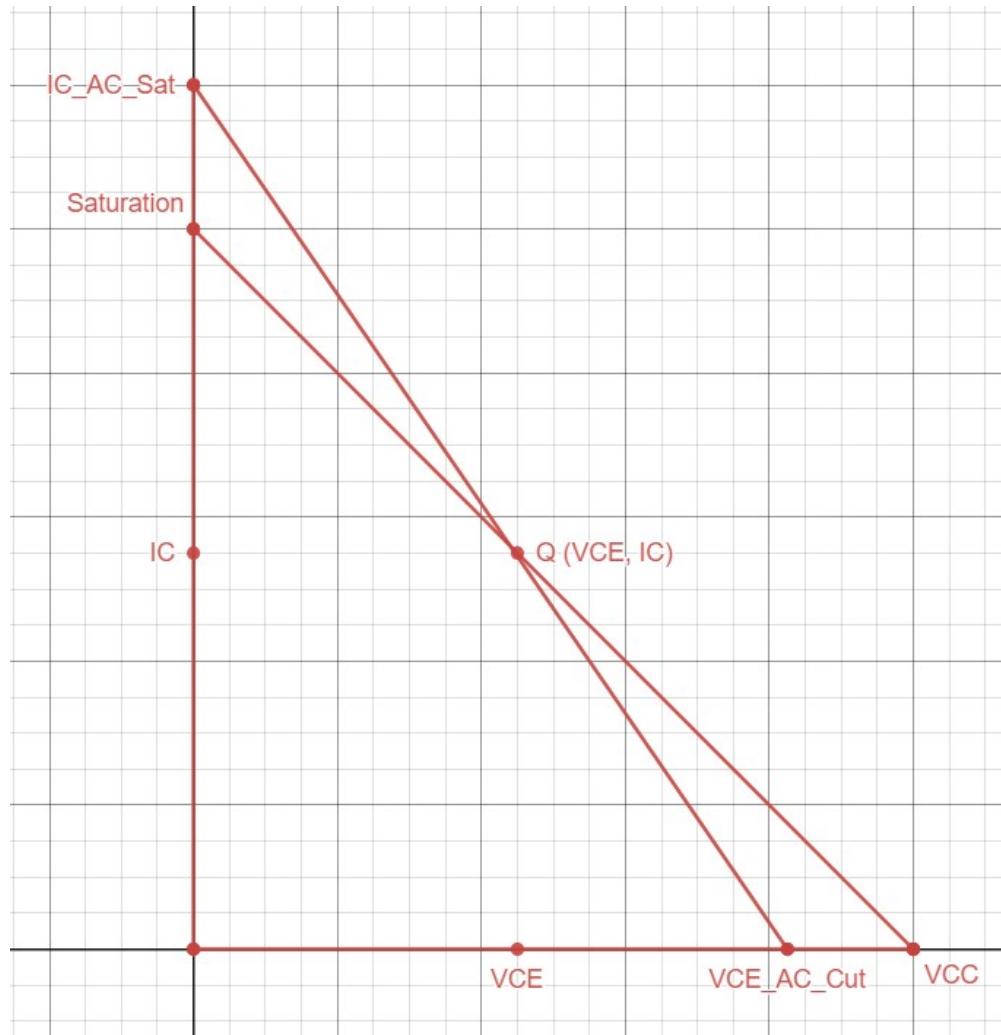


Figure 3.7: Second Stage DC & AC Loadline

Q1, Loadline

Because of the Decoupling Resistor R6, the DC Load Line is not Optimized at 45, 45 10 and will need to be calculated. However, because the equivalent load resistance of Q1 is ten times larger than R3, stage 1 maximum peak output should also be just below Q1's VCE.

$$V_{out,MaxP,Q1} \approx 0.9(V_{CE,Q1})$$

Additionally, if the voltage gain of the first stage is approximately equal to or less than the voltage gain of the second stage, the actual maximum peak voltage out will be determined by the second stage. This can be verified by using the following steps:

1. Divide the second stage Vout max peak voltage by the voltage gain of the second stage.

$$X = \frac{V_{out,Q2-MAXP}}{\Delta V_{Q2}}$$

2. Verify that Q1 VCE is greater than X.

✓ $V_{CE,Q1} > X$

3. If X is greater than or equal to Q1 VCE, biasing could be adjusted by redesigning the circuit to raise Q1's VCE and lower the decoupling voltage. However, it may be quicker and easier to lower Q1's voltage gain and raise Q2's voltage gain by the same factor.

3.6 Circuit Analysis

Universal Biasing

The Universal Bias Circuit can be analyzed using either Thevenin or Kirchhoff analysis. Kirchhoff's analysis is based on Kirchhoff's Voltage and Current Laws and will always produce an accurate analysis. Thevenin Analysis is based on Thevenin's Theorem and produces accurate analysis as long as certain circuit parameters are met.

Universal Bias, Thevenin Analysis

Thevenin Analysis converts a complex circuit into a simple, easier-to-analyze, series circuit see Figure 3.8.

Thevenin Analysis Steps:

Find the Thevenin Voltage V_{Thev} .

V_{Thev} is the maximum voltage that the load will see. Consider Q2 and RE as the load, see Figure 3.1.

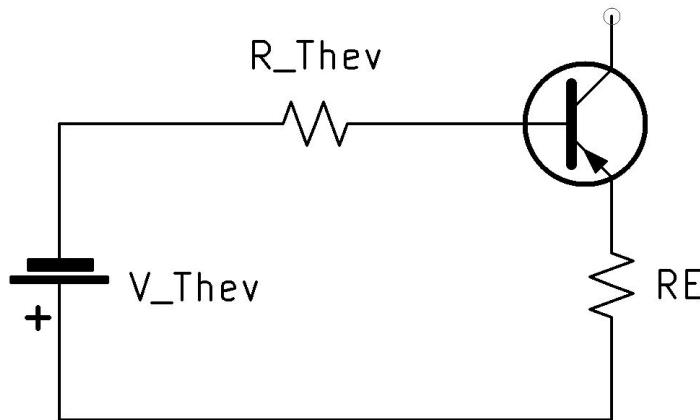


Figure 3.8: Thevenin Equivalent Circuit for Q2

Imagine that Q2 and RE (R_{10} and R_{11}) are removed from the circuit. R_7 and R_8 now make a series circuit, and V_{Thev} is equal to V_{R8} . See Figure 3.9

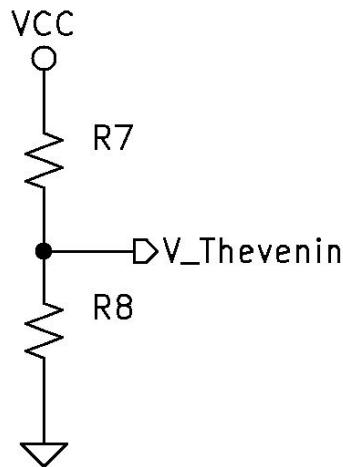


Figure 3.9: Thevenin Voltage

Find the Thevenin Resistance R_{Thev} .

R_{Thev} is equal to the total resistance that the load sees, for our example, R_7 in parallel with R_8 .

$$R_{Thev} = R_7 // R_8$$

Find the base current IB of the transistor.

Write a loop equation:

$$V_{Thev} - V_{R_{Thev}} - V_{BE} - V_{RE} = 0$$

$$\begin{aligned}
 V_{R_Thev} + V_{RE} &= V_{Thev} - V_{BE} \\
 IB(R_Thev) + IE(RE) &= V_{Thev} - V_{BE} \\
 IB(R_Thev) + (IB(\beta + 1))(RE) &= V_{Thev} - V_{BE} \\
 IB((R_Thev) + (\beta + 1)(RE)) &= V_{Thev} - V_{BE} \\
 \\
 IB &= \frac{V_{Thev} - V_{BE}}{(R_Thev) + (\beta + 1)(RE)}
 \end{aligned}$$

Verify that IR8 is greater than or equal to IB. If IR8 is not greater than or equal to ten times IB, the circuit will need to be analyzed using Kirchhoff Analysis.

✓ $I_{R8} \geq 10 \times IB$

Universal Bias, Kirchhoff Analysis

Kirchhoff's Analysis of Universal Biasing requires two loop equations.

Kirchhoff Loop Equation 1 (solve for IR8 in terms of IR8 and IB):

$$\begin{aligned}
 VCC - V_{R7} - V_{R8} &= 0 \\
 VCC - I_{R7}(R7) - I_{R8}(R8) &= 0 \\
 VCC - (IB + I_{R8})(R7) - I_{R8}(R8) &= 0 \\
 VCC - IB(R7) - I_{R8}(R7) - I_{R8}(R8) &= 0 \\
 VCC - IB(R7) - I_{R8}(R7 + R8) &= 0 \\
 I_{R8}(R7 + R8) &= VCC - IB(R7) \\
 \checkmark I_{R8} &= \frac{VCC - IB(R7)}{(R7 + R8)}
 \end{aligned}$$

Kirchhoff Loop Equation 2 (solve for IR8 in terms of IB):

$$\begin{aligned}
 VCC - V_{R7} - V_{BE} - V_{RE} &= 0 \\
 VCC - I_{R7}(R7) - 0.7 - IE(RE) &= 0 \\
 VCC - (IB + I_{R8})(R7) - 0.7 - IB(\beta + 1)(RE) &= 0 \\
 VCC - IB(R7) - I_{R8}(R7) - 0.7 - IB(\beta + 1)(RE) &= 0 \\
 VCC - IB(R7) - 0.7 - IB(\beta + 1)(RE) &= I_{R8}(R7) \\
 I_{R8}(R7) &= VCC - IB(R7) - 0.7 - IB(\beta + 1)(RE) \\
 I_{R8}(R7) &= VCC - 0.7 - IB(R7 + (\beta + 1)(RE)) \\
 \checkmark I_{R8} &= \frac{VCC - 0.7 - IB(R7 + (\beta + 1)(RE))}{R7}
 \end{aligned}$$

Use the substitution method to solve for IB by setting each equation equal to the other.

$$\frac{VCC - IB(R7)}{(R7 + R8)} = \frac{VCC - 0.7 - IB(R7 + (\beta + 1)(RE))}{R7}$$

Multi-Stage Amplifier: Design, Circuit Analysis, and Low-Frequency Response

$$R7(VCC - IBR7) = (R7 + R8)(VCC - 0.7 - IB(R7 + (\beta + 1)(RE)))$$

$$R7VCC - IBR7^2 = (R7 + R8)(VCC - 0.7 - IBR7 - IB(\beta + 1)(RE))$$

$$R7VCC - IBR7^2 = R7VCC - R7(0.7) - IBR7^2 - IBR7(\beta + 1)(RE) + R8VCC - R8(0.7) - IBR7R8 - IBR8(\beta + 1)(RE)$$

$$0 = -R7(0.7) - IBR7(\beta + 1)(RE) + R8VCC - R8(0.7) - IBR7R8 - IBR8(\beta + 1)(RE)$$

$$IBR7(\beta + 1)(RE) + IBR7R8 + IBR8(\beta + 1)(RE) = -R7(0.7) + R8VCC - R8(0.7)$$

$$IB\{R7(\beta + 1)(RE) + R7R8 + R8(\beta + 1)(RE)\} = R8(VCC - 0.7) - R7(0.7)$$

$$IB = \frac{R8(VCC - 0.7) - R7(0.7)}{(R7)(\beta + 1)(RE) + R7R8 + R8(\beta + 1)(RE)}$$

$$\checkmark \quad IB = \frac{R8(VCC - 0.7) - R7(0.7)}{(R7)(\beta + 1)(RE) + R8(R7 + (\beta + 1)(RE))}$$

Universal Bias with Decoupling Resistor, Kirchhoff Analysis

Kirchhoff's Analysis of Universal Biasing requires two loop equations.

Kirchhoff Loop Equation 1 (solve for IR2 in terms of IB):

$$VCC - VR6 - VR1 - VR2 = 0$$

$$VCC - I_{R6}R6 - I_{R1}R1 - I_{R2}R2 = 0$$

$$VCC - (IC + I_{R1})R6 - I_{R1}R1 - I_{R2}R2 = 0$$

$$VCC - (IB(\beta) + I_{R2} + IB)R6 - (I_{R2} + IB)R1 - I_{R2}R2 = 0$$

$$VCC - IB(\beta)R6 - I_{R2}R6 - IBR6 - I_{R2}R1 - IBR1 - I_{R2}R2 = 0$$

$$I_{R2}R6 + I_{R2}R1 + I_{R2}R2 = VCC - IB(\beta)R6 - IBR6 - IBR1$$

$$I_{R2}(R6 + R1 + R2) = VCC - (IB)((\beta)R6 + R6 + R1)$$

✓ $I_{R2} = \frac{VCC - (IB)((\beta)R6 + R6 + R1)}{R6 + R1 + R2}$

Kirchhoff Loop Equation 2 (solve for IR2 in terms of IB):

$$-V_{BE} - V_{RE} + V_{R2} = 0$$

$$-0.7V - (IE)RE + I_{R2}R2 = 0$$

$$-0.7V - IB(\beta + 1)RE + I_{R2}R2 = 0$$

$$I_{R2}R2 = 0.7V + IB(\beta + 1)RE$$

✓ $I_{R2} = \frac{0.7V + IB(\beta + 1)RE}{R2}$

Use the substitution method to solve for IB by setting each equation equal to the other.

$$\frac{VCC - (IB)((\beta)(R6 + R6 + R1))}{R6 + R1 + R2} = \frac{0.7V + IB(\beta + 1)RE}{R2}$$

$$R2[VCC - (IB)((\beta)(R6 + R6 + R1))] = (R6 + R1 + R2)(0.7V + IB(\beta + 1)(RE))$$

$$VCC(R2) - (IB)(R2)((\beta)R6 + R6 + R1) = 0.7V(R6 + R1 + R2) + IB(\beta + 1)(RE)(R6 + R1 + R2)$$

$$VCC(R2) - 0.7V(R6 + R1 + R2) = (IB)(R2)((\beta)R6 + R6 + R1) + IB(\beta + 1)(RE)(R6 + R1 + R2)$$

$$VCC(R2) - 0.7V(R6 + R1 + R2) = (IB)\{(R2)((\beta)R6 + R6 + R1) + (\beta + 1)(RE)(R6 + R1 + R2)\}$$

$$\frac{VCC(R2) - 0.7V(R6 + R1 + R2)}{\{(R2)((\beta)R6 + R6 + R1) + (\beta + 1)(RE)(R6 + R1 + R2)\}} = (IB)$$

✓ $IB = \frac{VCC(R2) - 0.7V(R1 + R2 + R6)}{R2(R1 + R6 + (\beta \times R6)) + RE(\beta + 1)(R1 + R2 + R6)}$

→ Find all resistor voltages and powers.

Q2, Power and Load-line Analysis

Find $V_{CE.Q2}$

$$V_{CE.Q2} = VCC - V_{R9} - V_{R10} - V_{R11}$$

Find IC

$$IC_{R9} = \frac{V_{R9}}{R9}$$

Find P_{Q2}

$$P_{Q2} = V_{CE.Q2} \times IC_{R9}$$

Find $IC_{Sat.Q2}$

$$IC_{Sat.Q2} = \frac{VCC}{R9 + R10 + R11}$$

Find $V_{cut.Q2}$

$$V_{cut.Q2} = VCC$$

Find $v_{cut.ac.Q2}$

$$v_{cut.ac.Q2} = V_{CE.Q2} + IC_{R9}(R12//R9)$$

Find $ic_{ac.Q2}$

$$ic_{ac.Q2} = IC_{Sat.Q2} + \frac{V_{CE.Q2}}{(R12//R9)}$$

Depending on the biasing (Q point), the smaller of the two following equations will represent $Vout_{MaxP.Q2}$. If the amplifier is designed for a Z_{out} (R9) that is ten times smaller than the load (R12) and the biasing is optimized, Vout Max Peak will be approximately equal to 90% of VCE.

$$Vout_{MaxP.Q2} \approx 0.9(V_{CE.Q2})$$

Vout max peak actual will be the smaller of the following:

$$VoutP_{Max.Q2} = v_{cut.ac.Q2} - V_{CE.Q2}$$

OR

$$VoutP_{Max.Q2} = V_{CE.Q2}$$

Q1, Power and Load-line Analysis

Find V_{CE_Q1} , $V_{CE_Q1} = VCC - V_{R6} - V_{R3} - V_{R4} - V_{R5}$

Find IC , $IC_{R3} = \frac{V_{R3}}{R3}$

Find P_{Q1} , $P_{Q1} = V_{CE_Q1} \times IC_{R3}$

Find $VoutP_{Max_Q1}$, $VoutP_{Max_Q1} \approx 0.9(V_{CE_Q1})$

Q2, Voltage Gain Analysis

Find ΔV_{Q2} , $\Delta V_{Q2} \approx \frac{R9}{R10}$

$$\Delta V_{Q2} = \frac{V_{OUT}}{V_{IN}}$$

$$\Delta V_{Q2} = \frac{IC(R9//R12)}{IB(\beta+1)(R10+r'e)}$$

$$\Delta V_{Q2} = \frac{IC(R9//R12)}{IE(R10+r'e)}$$

$$\Delta V_{Q2} = \alpha \frac{(R9//R12)}{R10+r'e}$$

Q1, Voltage Gain Analysis

Find ΔV_{Q1} , $\Delta V_{Q1} \approx \frac{R3}{R4}$

$$\Delta V_{Q1} = \frac{V_{OUT}}{V_{IN}}$$

$$\Delta V_{Q1} = \frac{IC(R3//R7//R8//((R10+r'e)(\beta+1))}{IB(\beta+1)(R4+r'e)}$$

$$\Delta V_{Q1} = \frac{IC(R3//R7//R8//((R10+r'e)(\beta+1))}{IE(R4+r'e)}$$

$$\Delta V_{Q1} = \alpha \frac{R3//R7//R8//((R10+r'e)(\beta+1))}{R4+r'e}$$

Total Voltage Gain Analysis

Find ΔV_{Total} ,

$$\Delta V_{Total} = \Delta V_{Q1} \times \Delta V_{Q2}$$

Maximum Peak Input Voltage

Find $VinP_{Max}$,

$$VinP_{Max} = \frac{VoutP_{Max}}{\Delta V_{Total}}$$

3.7 Frequency Response Low

Rules and Steps for Calculating Frequency Response Low

Rules:

1. Treat all capacitors like opens.
2. Find $R_{Thevenin}$ for each capacitor.
3. Calculate Fc_{Low_C} for each capacitor:

$$Fc_{Low_C} = \frac{1}{2\pi R_{Thevenin} C}$$

4. Calculate Fc_{LOW} Total

$$Fc_{Low} = \sqrt{(Fc_{C1})^2 + (Fc_{C2})^2 + (Fc_{C3})^2 \dots}$$

Steps:

Calculate the Capacitor Thevenin Resistances for Figure 3.1.

$$R_{Thevenin1} = \{(R5 + R4 + r'e_{Q1})(\beta + 1) // R2 // (R1 + R5)\} + R_{Gen}$$

$$R_{Thevenin2} = \{\left(\frac{R2 // (R1 + R6)}{\beta + 1}\right) + r'e_{Q1} + R4\} // R5$$

$$R_{Thevenin3} = R6 // \{R1 + (R2 // ((\beta + 1)(r'e_{Q1} + R4 + R5)))\}$$

$$R_{Thevenin4} = \{(R11 + R10 + r'e_{Q2})(\beta + 1) // R7 // R8\} + \{(((R5 + R4 + r'e_{Q1})(\beta + 1) // R2) + R1) // R6\} + R3$$

$$R_{Thevenin5} = R9 + R12$$

$$R_{Thevenin6} = \left(\frac{R7 // R8}{\beta + 1}\right) + r'e_{Q2} + R10 // R11$$

Design: Calculating capacitor values for a desired Frequency Critical Low

Choose a desired Frequency Critical Low $Fc_{Low_Desired}$.

$$Fc_{Low_Desired} = \sqrt{x^2 + x^2 + x^2 \dots}$$

$$(Fc_{Low_Desired})^2 = x^2 + x^2 + x^2 \dots$$

$$(Fc_{Low_Desired})^2 = (Number\ of\ Caps)x^2$$

$$x^2 = \frac{(Fc_{Low_Desired})^2}{Number\ of\ Caps}$$

$$xhz = \sqrt{\frac{(Fc_{Low_Desired})^2}{Number\,Of\,Caps}}$$

Calculate the capacitance value for each capacitor using its $R_{Thevinin}$ and the previously calculated Xhz for the desired Frequency Critical Low.

$$C_X = \frac{1}{2\pi(R_{Thevinin})(xhz)} \text{ (farads)}$$

Chapter 4

Multi-Stage Amplifier: High-Frequency Response & Peaking

4.1 Objectives:

Multi-Stage Amplifier Design and Analysis:

High Frequency Response

- High Critical Frequency $F_{C_{High}}$: Understand and calculate the high critical frequency $F_{C_{High}}$ for a multi-stage amplifier, taking into account the internal device capacitance and parasitic circuit elements in the amplifier stages.

Emitter Peaking

- Investigate the theory of Emitter Peaking.
- Calculate the Emitter Peaking capacitor and the Improvement Factor for a given circuit.

Shunt Peaking

- Investigate the theory of Shunt Peaking.
- Calculate the Shunt Peaking Inductor and the Improvement Factor for a given circuit.

Series Peaking

- Investigate the theory of Series Peaking.
- Calculate the Series Peaking Inductor and the Improvement Factor for a given circuit.

By achieving these objectives, students will develop a comprehensive understanding of an amplifier's High-Frequency Response and how to modify a circuit to improve frequency response using Emitter, Shunt, and Series Peaking.

4.2 Frequency Critical High:

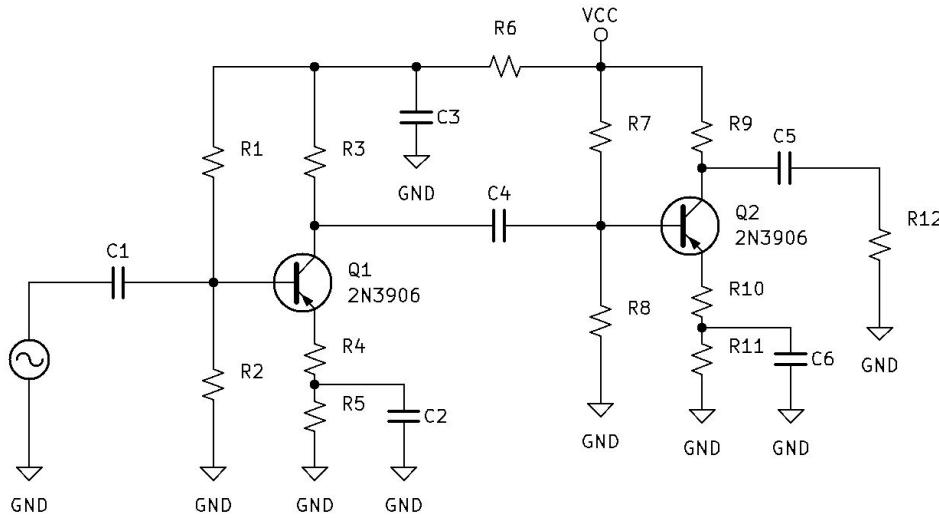


Figure 4.1: Two Stage Amplifier

4.2.1 Frequency Critical High Formula

For the two-stage amplifier, Frequency Critical High F_{cHigh} can be found using the following formula:

$$F_{cHigh} = \frac{0.35}{\sqrt{\left(\frac{0.35}{F_{cH_{In}}}\right)^2 + \left(\frac{0.35}{F_{cH_{Mid}}}\right)^2 + \left(\frac{0.35}{F_{cH_{Out}}}\right)^2}}$$

SMALL-SIGNAL CHARACTERISTICS

Current-Gain - Bandwidth Product ($I_C = 10 \text{ mA}$, $V_{CE} = 20 \text{ Vdc}$, $f = 100 \text{ MHz}$)	f_T	250	-	MHz
Output Capacitance ($V_{CB} = 5.0 \text{ Vdc}$, $I_E = 0$, $f = 1.0 \text{ MHz}$)	C_{obo}	-	4.5	pF
Input Capacitance ($V_{EB} = 0.5 \text{ Vdc}$, $I_C = 0$, $f = 1.0 \text{ MHz}$)	C_{ibo}	-	10	pF
Input Impedance ($I_C = 1.0 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{ie}	2.0	12	kΩ
Voltage Feedback Ratio ($I_C = 1.0 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{re}	0.1	10	$\times 10^{-4}$
Small-Signal Current Gain ($I_C = 1.0 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	100	400	-
Output Admittance ($I_C = 1.0 \text{ mA}$, $V_{CE} = 10 \text{ Vdc}$, $f = 1.0 \text{ kHz}$)	h_{oe}	3.0	60	μmhos
Noise Figure ($I_C = 100 \mu\text{A}$, $V_{CE} = 5.0 \text{ Vdc}$, $R_S = 1.0 \text{ kΩ}$, $f = 1.0 \text{ kHz}$)	NF	-	4.0	dB

Figure 4.2: ON Semiconductor 2n3906 Data Sheet Excerpt

4.2.2 Frequency Critical High In

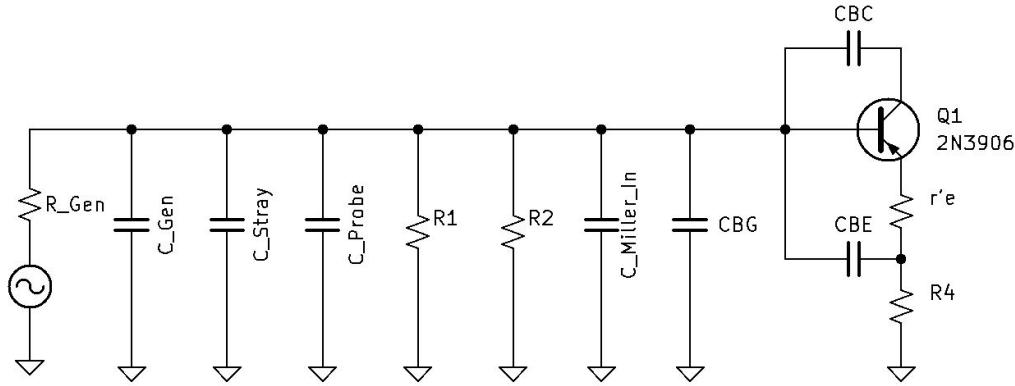


Figure 4.3: Input AC equivalent circuit at High Frequencies

Calculate the total capacitance at the input of the amplifier.

$$C_{total_{IN}} = C_{Gen} + C_{Stray} + C_{Probe} + C_{Miller_{IN}} + C_{BG}$$

C_{Gen} = Specification in Manual

$$C_{Stray} \approx 10\text{pF}$$

$C_{Probe} \approx 16\text{pF}$, Specification in Manual

$$C_{Miller_{IN}} = C_{OBO}(1 + \Delta V_{CE(Q1)})$$

C_{OBO} = transistor datasheet specification

$$\Delta V_{CE} = \frac{V_{out}}{V_{in}} = \frac{i_c(RC//RL)}{i_e(r'e+RE)} = \alpha \frac{RC//RL}{r'e+RE} = \alpha \frac{R3//RL_{eq}}{r'e+R4}$$

$$C_{BG} = C_{BE}(1 - \Delta V_{CC(Q1)})$$

$$C_{BE} = \frac{1}{2\pi f_\tau r'e}$$

f_τ = transistor datasheet specification

$$\Delta V_{CC} = \frac{RE}{r'e+RE} = \frac{R4}{r'e+R4}$$

Calculate the Thevenin resistance for C_Total_{In} .

$$R_Thevenin_{C_Total_{In}} = (R4 + r'e)(\beta + 1)//R2//R1//R_{Gen}$$

$$R_Thevenin_{C_Total_{In}} \approx R_{Gen}$$

Calculate the Input High Critical Frequency.

$$FcH_{In} = \frac{1}{2\pi \times R_Thevenin_{C_Total_{In}} \times C_Total_{IN}}$$

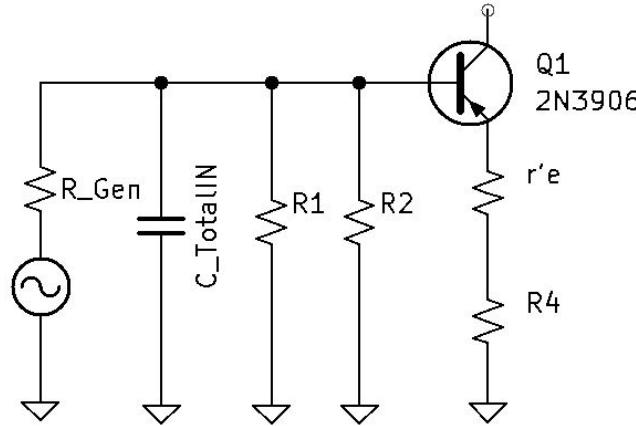


Figure 4.4: Capacitance Total In equivalent circuit at High Frequencies

4.2.3 Frequency Critical High Middle

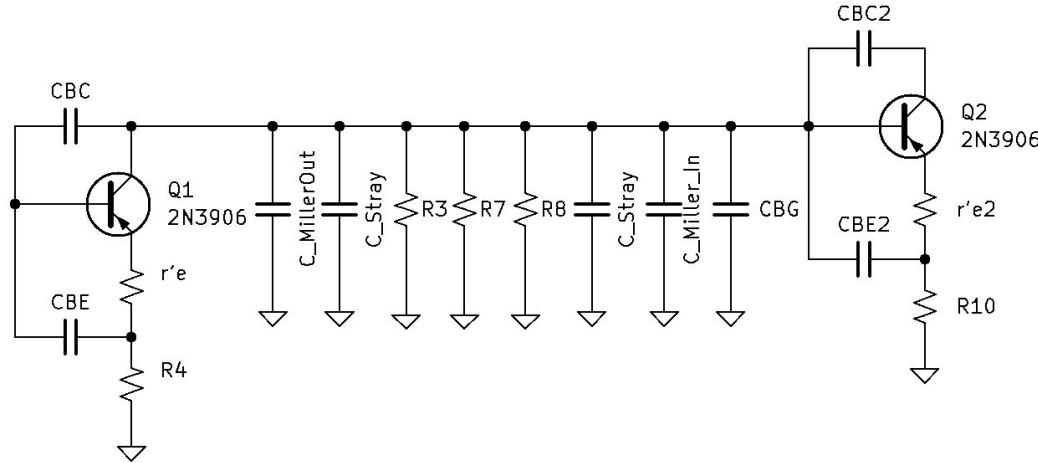


Figure 4.5: Middle AC equivalent circuit at High Frequencies

Calculate the total capacitance at the middle stage of the amplifier.

$$C_{total Mid} = C_{MillerOut} + C_{Stray} + C_{Stray} + C_{MillerIN} + C_{BG}$$

$$C_{MillerOut} = CBC \left(\frac{1 + \Delta V_{CE}(Q1)}{\Delta V_{CE}(Q1)} \right)$$

$$CBC \approx C_{OBO}(\text{Data Sheet})$$

$$C_{Stray} \approx 10\text{pF}$$

$$C_{MillerIN} = C_{OBO}(1 + \Delta V_{CE}(Q2))$$

C_{OBO} = transistor datasheet specification

$$\Delta V_{CE(Q2)} = \frac{V_{out}}{V_{in}} = \frac{i_c(RC//RL)}{i_e(r'e+RE)} = \alpha \frac{RC//RL}{r'e+RE} = \alpha \frac{R9//R12}{r'e+R10}$$

$$C_{BG} = C_{BE}(1 - \Delta V_{CC})$$

$$C_{BE} = \frac{1}{2\pi f_\tau r'e}$$

f_τ = transistor datasheet specification

$$\Delta V_{CC(Q2)} = \frac{RE}{r'e+RE} = \frac{R10}{r'e+R10}$$

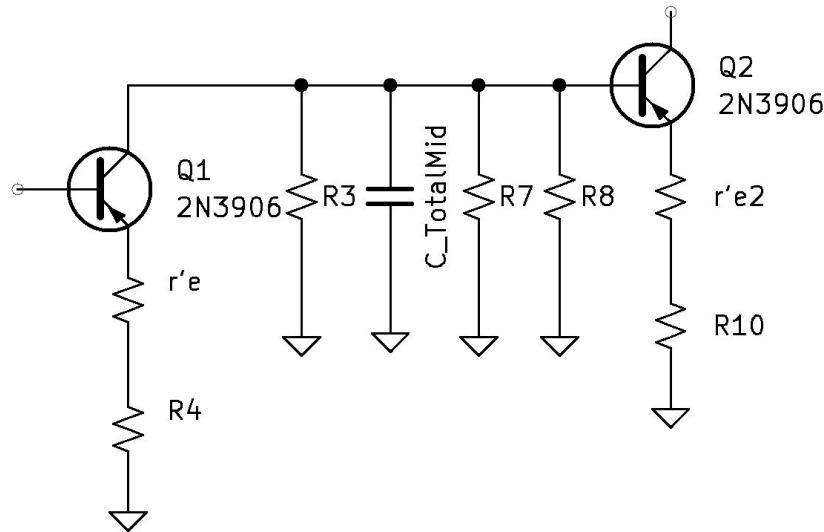


Figure 4.6: Capacitance Total Middle AC equivalent circuit at High Frequencies

Calculate the Thevenin resistance for $C_{TotalMid}$.

$$R_{TheveninC_{TotalMid}} = (R10 + r'e2)(\beta + 1) // R3 // R7 // R8$$

Calculate the Input High Critical Frequency.

$$FcH_{Mid} = \frac{1}{2\pi \times R_{TheveninC_{TotalMid}} \times C_{TotalMid}}$$

4.2.4 Frequency Critical High Out

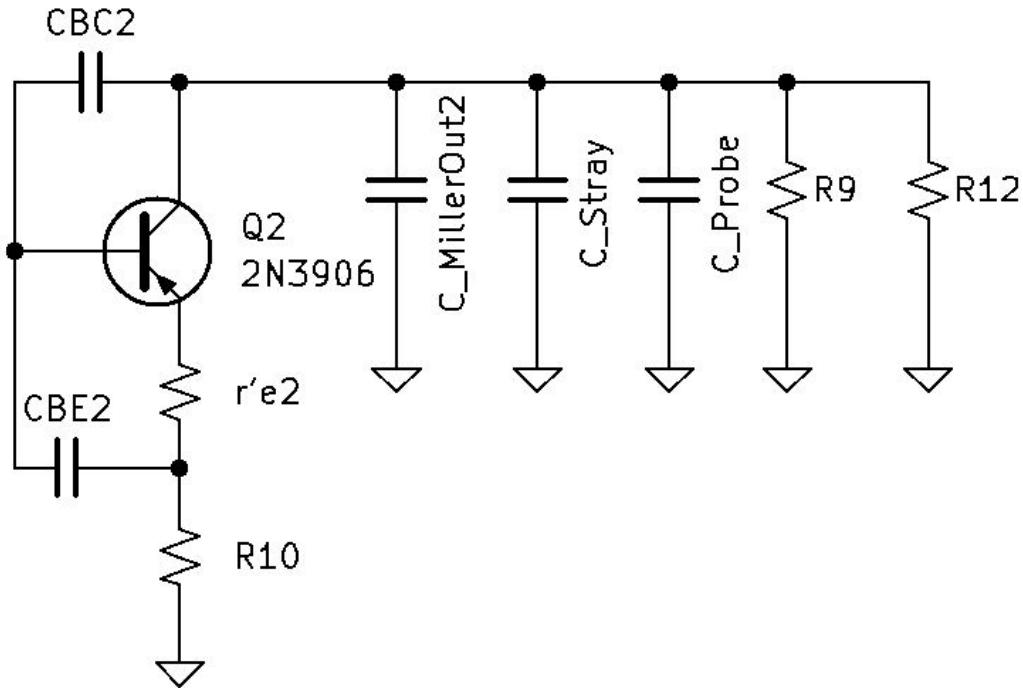


Figure 4.7: Output AC equivalent circuit at High Frequencies

Calculate the total capacitance at the output stage of the amplifier.

$$C_{totalOut} = C_{MillerOut2} + C_{Stray} + C_{Probe}$$

$$C_{MillerOut2} = CBC \left(\frac{1 + \Delta V_{CE(Q2)}}{\Delta V_{CE(Q2)}} \right)$$

$$CBC \approx C_{OBO} (\text{Data Sheet})$$

$$C_{Stray} \approx 10 \mu F$$

$$C_{Probe} \approx 16 \mu F, \text{ Specification in Manual}$$

Calculate the Thevenin resistance for $C_{TotalOut}$.

$$R_{Thevenin_{C_{TotalOut}}} = R9 // R12$$

Calculate the Out High Critical Frequency.

$$FcH_{Mid} = \frac{1}{2\pi \times R_{Thev_{C_{TotalMid}}} \times C_{TotalMid}}$$

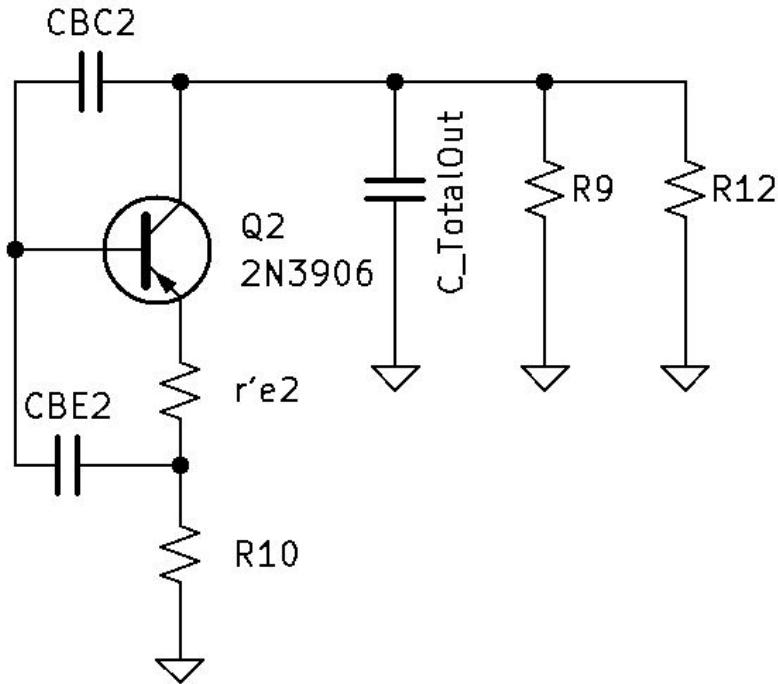


Figure 4.8: Capacitance Total Out AC equivalent circuit at High Frequencies

4.2.5 Frequency Critical High final calculation

Calculate the High Critical Frequency for the circuit using the previously calculated $F_{cH_{In}}$, $F_{cH_{Mid}}$, and $F_{cH_{Out}}$.

$$F_{cH_{High}} = \frac{0.35}{\sqrt{\left(\frac{0.35}{F_{cH_{In}}}\right)^2 + \left(\frac{0.35}{F_{cH_{Mid}}}\right)^2 + \left(\frac{0.35}{F_{cH_{Out}}}\right)^2}}$$

4.3 Emitter Peaking

4.3.1 Voltage Gain at Frequency Critical High

See figure 4.8 from the previous section. If we evaluate the ΔV formula we can see that at the F_{cH} the numerator of the formula begins to roll off due to the parallel capacitive reactance.

$$\Delta V = \frac{V_{out}}{V_{in}}$$

$$\Delta V_{MidBand} = \alpha \frac{RL//RC}{RE+r'3} = \alpha \frac{R9//R12}{R10+r'e2}$$

$$\Delta V_{FcHigh} = \alpha \frac{R9//R12//XC_{C_Out}}{R10+r'e2}$$

4.3.2 Emitter Peaking Explained

Knowing that the numerator is rolling off at a 20db/decade rate at the High Critical Frequency and that delta-V gap or difference is shrinking between the output voltage and the input voltage, how can we extend or prolong the difference between the output and the input?

One way is to apply Emitter Peaking. If the numerator is rolling off at F_{cHigh} , can we also roll off the denominator of the formula at the same time? As both the numerator and the denominator roll the difference between them stays the same maintaining the gain. This can be achieved by placing an Emitter Peaking Capacitor in parallel R10 in our formula.

4.3.3 Solving for Emitter Peaking Capacitance

$$\Delta V_{FcHigh} = \alpha \frac{R9//R12//XC_{C_Out}}{(XC_{EP}//R10)+r'e2}$$

Solve for the Emitter Peaking Capacitance value:

$$XC_{EP} = R10 \text{ at } F_{cHigh}$$

$$C_{EP} = \frac{1}{2\pi \times R10 \times F_{cHigh}}$$

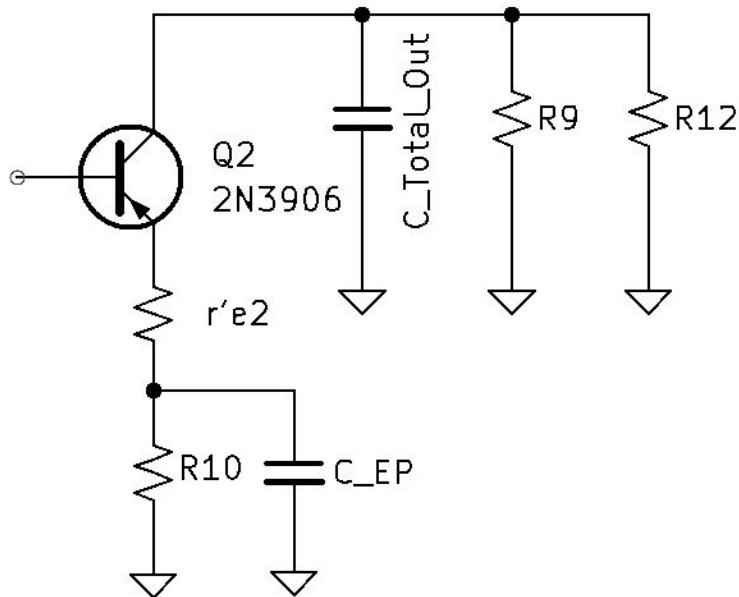


Figure 4.9: Emitter Peaking AC equivalent circuit

4.3.4 Improvement Factor (K)

Because Emitter Peaking involves RC circuits, we know that the roll-off will be 20dB/decade. If the old F_{cHigh} was at -3dB and is now at 0dB with Emitter Peaking, it is reasonable to predict that the old -6dB frequency is now the new F_{cHigh_EP} .

Solving for the Emitter Peaking Improvement Factor (K)

$$-6dB = 20 \log \frac{1}{\sqrt{1+(\frac{F}{F_{cHigh}})^2}} \quad (\text{standard RC Roll-Off dB formula set to } -6dB)$$

$$-6dB = 20 \log \frac{1}{\sqrt{1+(\frac{K_{EP}}{1})^2}} \quad (\text{By setting } F_{cHigh} \text{ to 1, F becomes the Improvement Factor})$$

Solve for The Improvement Factor K_{EP} :

$$-6dB = 20 \log \frac{1}{\sqrt{1+(\frac{K_{EP}}{1})^2}}$$

$$\frac{-6}{20} = \log \frac{1}{\sqrt{1+(\frac{K_{EP}}{1})^2}}$$

$$10^{\frac{-6}{20}} = \frac{1}{\sqrt{1+(\frac{K_{EP}}{1})^2}}$$

$$\sqrt{1 + \left(\frac{K_{EP}}{1}\right)^2} = \frac{1}{10^{\frac{-6}{20}}}$$

$$1 + \left(\frac{K_{EP}}{1}\right)^2 = \left(\frac{1}{10^{\frac{-6}{20}}}\right)^2$$

$$\left(\frac{K_{EP}}{1}\right)^2 = \left(\frac{1}{10^{\frac{-6}{20}}}\right)^2 - 1$$

$$K_{EP} = \sqrt{\left(\frac{1}{10^{\frac{-6}{20}}}\right)^2 - 1}$$

✓ $K_{EP} = 1.727$ (The Improvement Factor for Emitter Peaking is 1.727)

$$FcH_{EP} = K_{EP} \times Fc_{High}$$

✓ $FcH_{EP} = 1.727 \times Fc_{High}$

4.4 Shunt Peaking

4.4.1 Voltage Gain at Frequency Critical High

See figure 4.8 from the previous section. If we evaluate the ΔV formula we can see that at the F_{cH} the numerator of the formula begins to roll off due to the parallel capacitive reactance.

$$\Delta V = \frac{V_{out}}{V_{in}}$$

$$\Delta V_{MidBand} = \alpha \frac{RL//RC}{RE+r'3} = \alpha \frac{R9//R12}{R10+r'e2}$$

$$\Delta V_{FcHigh} = \alpha \frac{R9//R12//XC_{C_Out}}{R10+r'e2}$$

4.4.2 Shunt Peaking Explained

Emitter Peaking extends the High Critical Frequency by rolling off the denominator of the gain formula at the same time that the numerator is rolling off. Shunt Peaking attempts to prevent or delay the roll-off of the numerator. This is achieved by placing an inductor in series with the RC resistance of the final transistor stage. See Figure 4.10.

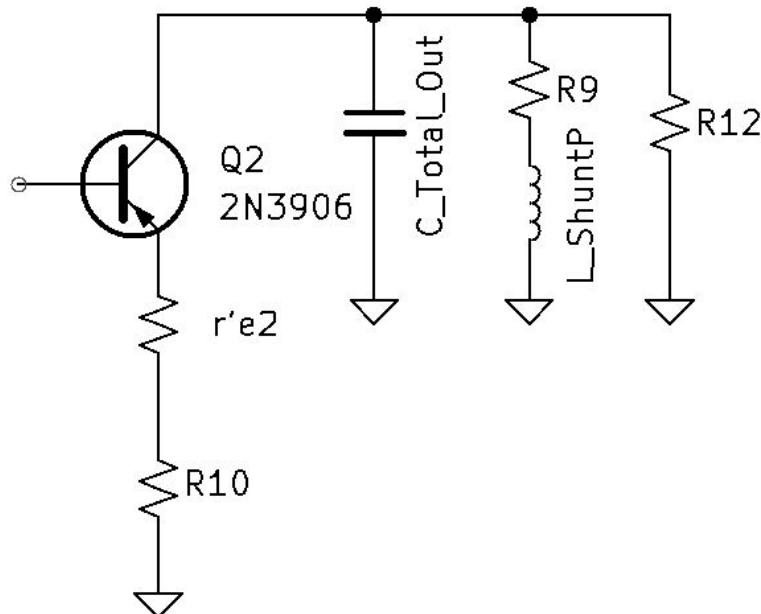


Figure 4.10: Shunt Peaking AC equivalent circuit

4.4.3 Improvement Factor (K)

For calculation purposes, we will design all Shunt Peaking with an improvement factor of 1.414.

✓ $K_{Shunt} = 1.414$

$$FcH_{ShuntP} = K_{Shunt} \times Fc_{High}$$

✓ $FcH_{ShuntP} = 1.414 \times Fc_{High}$

4.4.4 Solving for Shunt Peaking Inductance

For optimal flatness, make X_L 1.414 times larger than X_C at the High Critical Frequency of the circuit.

$$X_L(1.414) = 2\pi \times Fc_{High} \times L_{Shunt} \quad X_C = \frac{1}{2\pi \times Fc_{High} \times C_{totalOut}}$$

$$X_L = \frac{2\pi \times Fc_{High} \times L_{Shunt}}{(1.414)} \quad X_C = \frac{1}{2\pi \times Fc_{High} \times C_{totalOut}}$$

Substitute:

$$\frac{2\pi \times Fc_{High} \times L_{Shunt}}{(1.414)} = \frac{1}{2\pi \times Fc_{High} \times C_{totalOut}}$$

$$2\pi \times Fc_{High} \times L_{Shunt} = \frac{1.414}{2\pi \times Fc_{High} \times C_{totalOut}}$$

$$L_{Shunt} = \frac{1.414}{2\pi \times Fc_{High} \times 2\pi \times Fc_{High} \times C_{totalOut}}$$

✓ $L_{Shunt} = \frac{1.414}{(2\pi \times Fc_{High})^2 \times C_{totalOut}}$

4.5 Series Peaking

4.5.1 Voltage Gain at Frequency Critical High

See figure 4.8 from the previous section. If we evaluate the ΔV formula we can see that at the F_{cH} the numerator of the formula begins to roll off due to the parallel capacitive reactance.

$$\Delta V = \frac{V_{out}}{V_{in}}$$

$$\Delta V_{MidBand} = \alpha \frac{RL//RC}{RE+r'3} = \alpha \frac{R9//R12}{R10+r'e2}$$

$$\Delta V_{FcHigh} = \alpha \frac{R9//R12//XC_{C_Out}}{R10+r'e2}$$

4.5.2 Series Peaking Explained

If Emitter Peaking extends the High Critical Frequency by rolling off the denominator of the gain formula at the same time that the numerator is rolling off and Shunt Peaking attempts to prevent or delay the roll-off of the numerator of the gain formula. Then you can think of Series Peaking as independent of the gain formula. Series peaking relies on the concept of LC circuit voltage magnification, where at resonance, the capacitive reactance will appear to have more voltage than the source. This is achieved by placing an inductor in series with the load of the final transistor stage. See Figure 4.11.

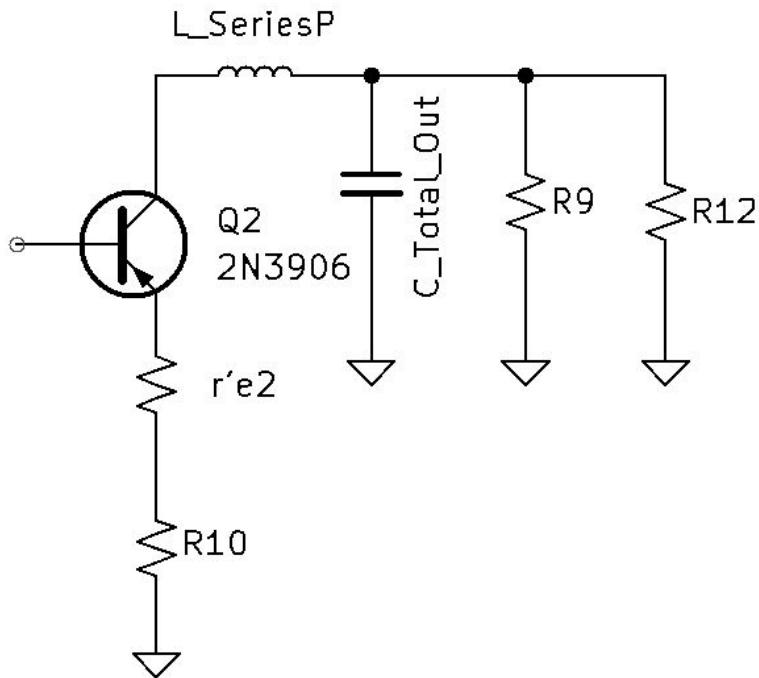


Figure 4.11: Series Peaking AC equivalent circuit

4.5.3 Improvement Factor (K)

For calculation purposes, we will design all Series Peaking with an improvement factor of 1.414.

✓ $K_{Series} = 1.414$

$$FcH_{SeriesP} = K_{Series} \times Fc_{High}$$

✓ $FcH_{SeriesP} = 1.414 \times Fc_{High}$

4.5.4 Solving for Series Peaking Inductance

For optimal flatness, make X_L 1.414 times smaller than X_C at the High Critical Frequency of the circuit.

$$\frac{X_L}{1.414} = 2\pi \times Fc_{High} \times L_{Series} \quad X_C = \frac{1}{2\pi \times Fc_{High} \times C_{totalOut}}$$

$$X_L = 1.414 \times 2\pi \times Fc_{High} \times L_{Series} \quad X_C = \frac{1}{2\pi \times Fc_{High} \times C_{totalOut}}$$

Substitute:

$$1.414 \times 2\pi \times Fc_{High} \times L_{Series} = \frac{1}{2\pi \times Fc_{High} \times C_{totalOut}}$$

$$2\pi \times Fc_{High} \times L_{Series} = \frac{1.414}{2\pi \times Fc_{High} \times C_{totalOut}}$$

$$L_{Series} = \frac{1}{1.414 \times 2\pi \times Fc_{High} \times 2\pi \times Fc_{High} \times C_{totalOut}}$$

✓ $L_{Series} = \frac{1}{(2\pi \times Fc_{High})^2 \times C_{totalOut} \times 1.414}$

4.6 Factors that affect Frequency Response

Factors that affect Low Critical Frequency F_{cLow}

- Coupling Capacitors & Bypass Capacitors
- Decoupling Networks
- Power Supply Filters
- Resistance Values

Factors that affect High Critical Frequency F_{cHigh}

- Device Capacitance
- Stray Capacitance
- Generator Capacitance
- Gain
- $f\tau$ & Slew Rate
- Resistance Values
- Probe Capacitance

4.7 Types of Amplifier Distortion

Amplitude Distortion

- **Amplitude Distortion** is defined as the inability of an amplifier to reproduce an output that is a linear function of the input. Clipping and Cross-Over Distortion are types of amplitude distortion.
- In high-fidelity audio systems, minimizing amplitude distortion is crucial to maintaining the accuracy and faithfulness of the reproduced sound. Engineers and designers aim to create amplifiers with low levels of amplitude distortion to ensure that the output closely matches the input signal, preserving the integrity of the audio source.

Frequency Distortion

- **Frequency Distortion** is defined as the inability of an amplifier to amplify all of the desired frequencies with the same gain.
- Measuring frequency distortion often involves analyzing the system's frequency response. Engineers aim to design systems with flat and linear frequency responses to minimize frequency distortion and ensure accurate reproduction of the input signal.

Phase Distortion

- **Phase Distortion** is defined as the inability of desired frequencies with the same time delay.
- Phase distortion is undesirable in stereo systems, and careful attention is given to signal polarity as well as speaker placement to ensure accurate phase coherence and faithful audio reproduction.

Crossover Distortion

- **Crossover Distortion** occurs in a Push-Pull, Class AB amplifier when both transistors are off.
- Crossover distortion is undesirable in audio amplification systems because it can introduce odd-order harmonics into the signal, leading to a harsh and distorted sound. To mitigate crossover distortion, amplifier designers often use techniques like biasing, which involves applying a small DC voltage to the transistors to keep them slightly conducting even when there is no input signal, reducing the gap between their active regions and minimizing crossover distortion.

Chapter 5

Amplifier Classifications, Push-Pull Amplifiers, and Heat-Sinks

5.1 Objectives

Amplifier Classifications:

Define the different types of amplifier classifications.

- Identify the following for each amplifier classification:
 - Linearity and fidelity qualities
 - Efficiency characteristics
 - Typical applications

Push-Pull Amplifiers:

- Design and design considerations for Push-Pull amplifiers.
- Analysis of Push-Pull amplifiers to include Z_{IN} , Z_{OUT} , and gains.

Heat-Sinks:

- Locate and identify the thermal resistance for a given heat sink using a data sheet.
- Calculate practical power usage for a given heat-sink circuit application using thermal resistance.

5.2 Amplifier Classifications

Class A Amplifiers

- The Universal Biased Common Emitter Amplifier is an example of a Class A amplifier.
- Transistor Amplification is active for 360° of the input cycle (always on).
- Achieves the highest degree of linearity.
- Low Efficiency, $\text{MaxEfficiency}_{\text{ClassA}} \approx 25\%$

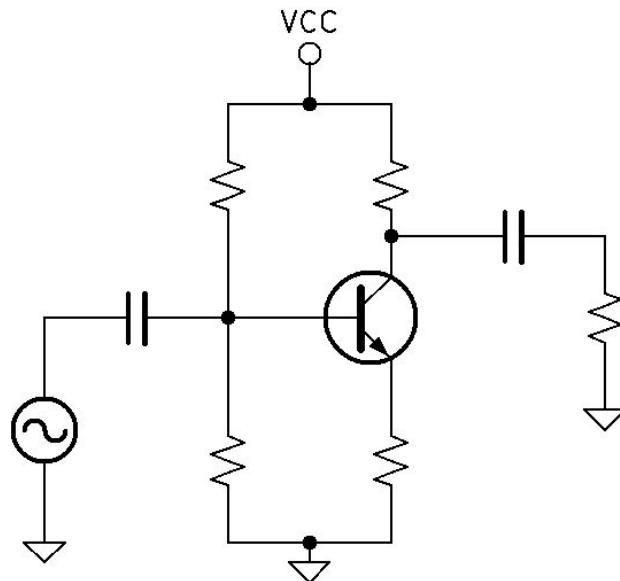


Figure 5.1: Class A Amplifier

Class B Amplifiers

- Transistor Amplification is active for 180° of the input cycle (on half the time).
- Achieves a moderate degree of linearity.
- moderate Efficiency, $\text{MaxEfficiency}_{\text{ClassA}} \approx 50\%$

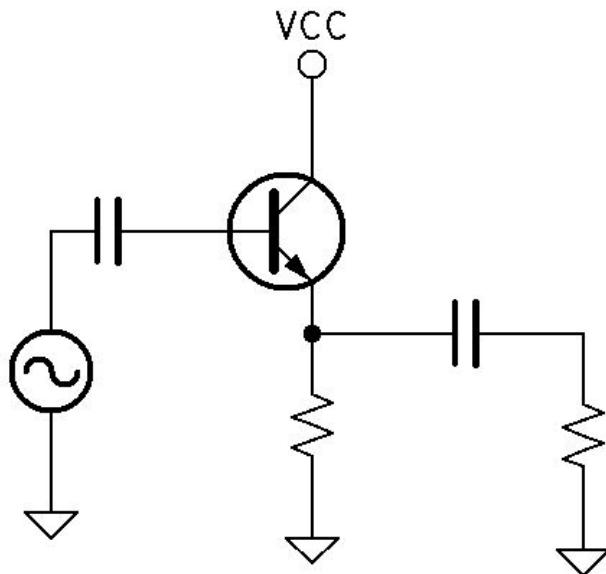


Figure 5.2: Class B Amplifier

Class AB Amplifiers

- Also known as Push-Pull.
- Transistor Amplification is active for each transistor nearly 180° of the input cycle. This means that nearly 360° of the input signal is amplified.
- Crossover distortion occurs when both transistors are off.
- Achieves a high degree of linearity.
- moderate Efficiency, $\text{MaxEfficiency}_{\text{ClassA}} \approx 50\%$

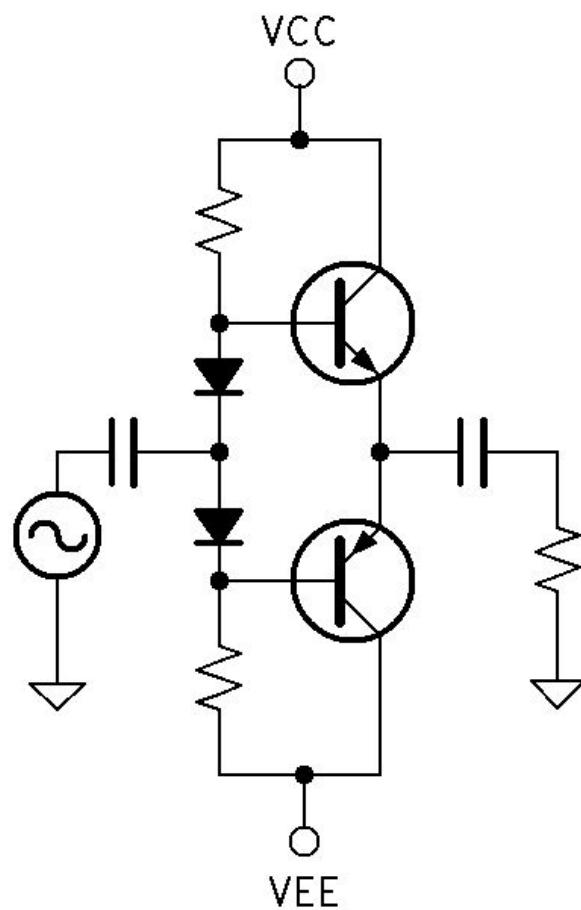


Figure 5.3: Class AB Amplifier

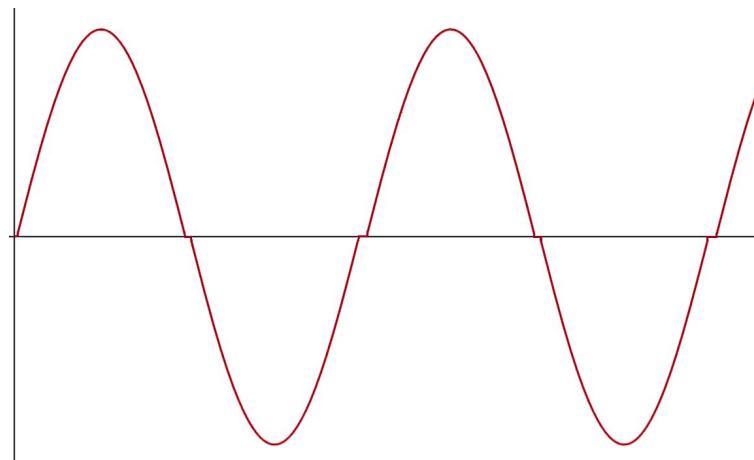


Figure 5.4: Class AB, Crossover Distortion

Class C Amplifiers

- Transistor Amplification is active less than 180° of the input cycle (less than 50% of the time).
- Common uses high-frequency sine-wave oscillators & radio frequency amplifiers.
- Achieves a low degree of linearity.
- moderate Efficiency, $\text{MaxEfficiency}_{\text{ClassA}} \approx 75\%$

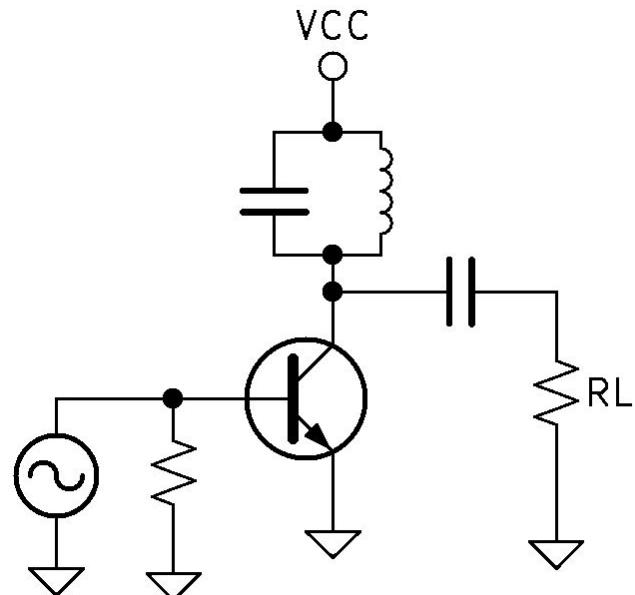


Figure 5.5: Class C Amplifier

Class D Amplifiers

- Non-linear switching amplifier also known as a PWM amplifier.
- Voltage and current waveforms do not overlap. The transistor is operating in either the Saturation or Cutoff region.
- Can achieve a high degree of linearity using an additional integration circuit that converts the PWM signal back to intelligence.
- Highly Efficient, $\text{MaxEfficiency}_{\text{ClassA}} \approx 100\%$

5.3 Push-Pull, Class AB Amplifiers

Push-Pull, Class AB Amplifier Characteristics:

- $\Delta V \approx 1$, and ΔI is high.
- Z_{IN} is high, and Z_{OUT} is low.
- Class AB amplifiers have improved efficiency when compared to Class A amplifiers.
- $MaxEfficiency_{ClassAB} \approx 50\%$, $MaxEfficiency_{ClassA} \approx 25\%$.
- Class AB amplifiers achieve a high degree of linearity.
- Class AB amplifiers are susceptible to Crossover Distortion which occurs when both transistors are off.

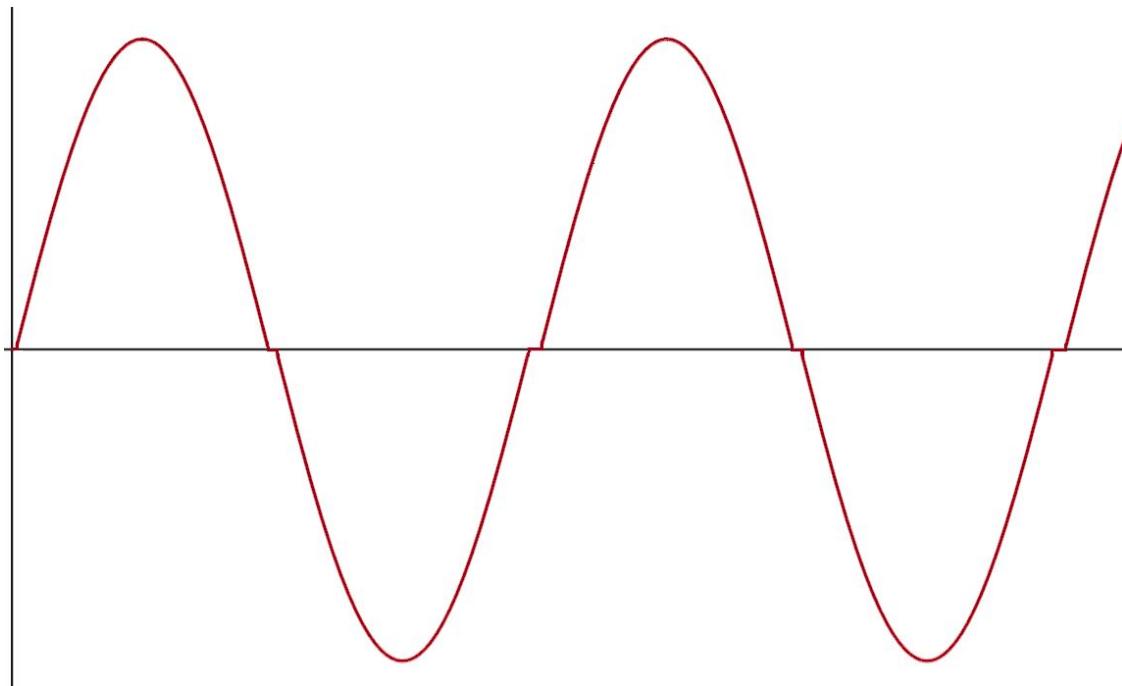


Figure 5.6: Class AB, Crossover Distortion

5.3.1 Push-Pull Amplifier Design

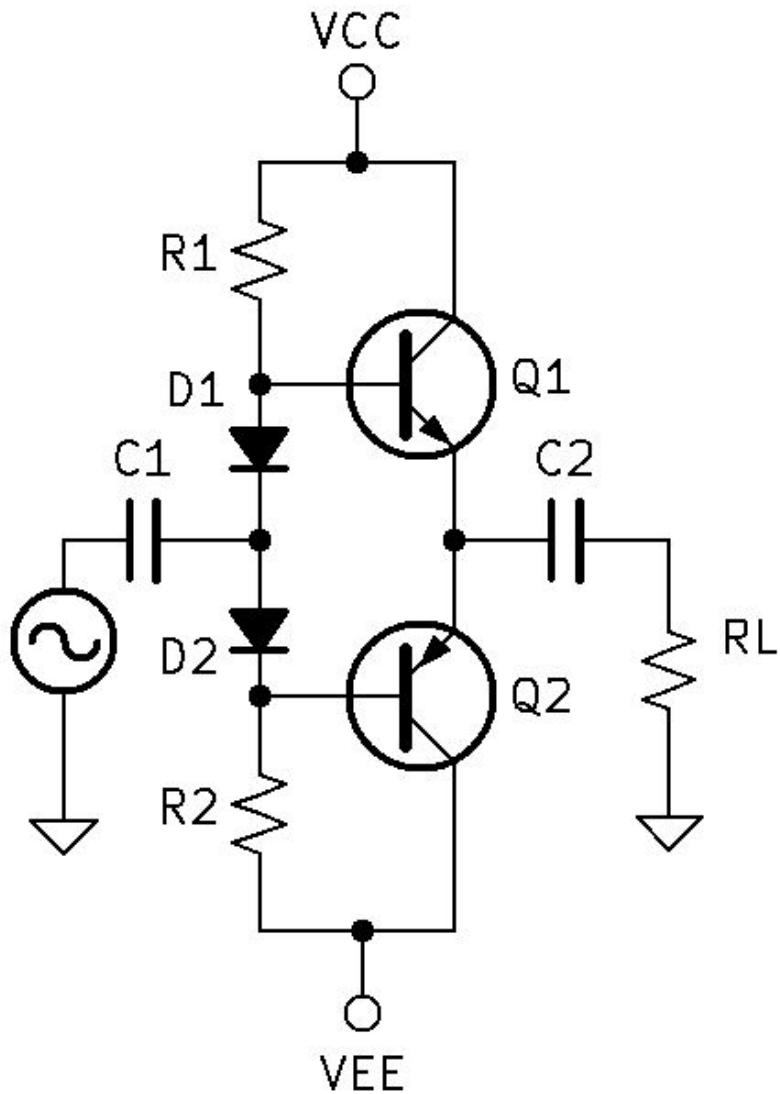


Figure 5.7: Class AB Amplifier

Split Rail Voltage VCC & VEE

The main benefit when using split rail voltage is the potential to ground between the two transistors will be at zero volts allowing the output coupling capacitor C2 to be a relatively low voltage which reduces the capacitor's cost. High Voltage High Capacitance capacitors are expensive. Low Voltage High Capacitance capacitors are less expensive.

Design steps and formulas:

$$Q1_{\beta eta} \approx Q2_{\beta eta}$$

$$\Delta V \approx 1$$

$$Vin_{MaxP} \approx Vout_{MaxP} \approx \frac{VCC+VEE}{2}$$

$$Ie_{MaxP} = \frac{Vout_{MaxP}}{RL}$$

$$Ib_{MaxP} = \frac{Ie_{MaxP}}{\beta+1}$$

$$IR1 \geq 11 \times Ib_{maxP}$$

$$VR1 = \frac{VCC+VEE}{2} - V_{D1}$$

$$R1 = \frac{VR1}{IR1}$$

$$R2 = R1$$

Z_{in} : (Analyze with Q1 on and Q2 off)

$$Z_{in} = (((((RL + r'e_{Q1})(\beta + 1))//R1) + r'd1)//(r'd2 + R2)$$

$$r'd = \frac{0.026}{I_{D1}}$$

$$Z_{in} \approx R1//R2$$

Z_{out} : (Analyze with Q1 on and Q2 off)

$$Z_{out} = \frac{((R_{Gen}//(r'd2+R2))+r'd1)//R1}{\beta+1} + r'e1$$

$$Z_{out} \approx r'e1$$

$$PRL_{Max} \approx \frac{(0.707 \times Vout_{MaxP})^2}{RL}$$

$$PQ1_{Max} \approx \frac{PRL_{Max}}{2}$$

$$PQ2_{Max} = PQ1_{Max}$$

5.3.2 Improved Input Impedance Z_{in} and Power Capabilities using the Darlington Pair

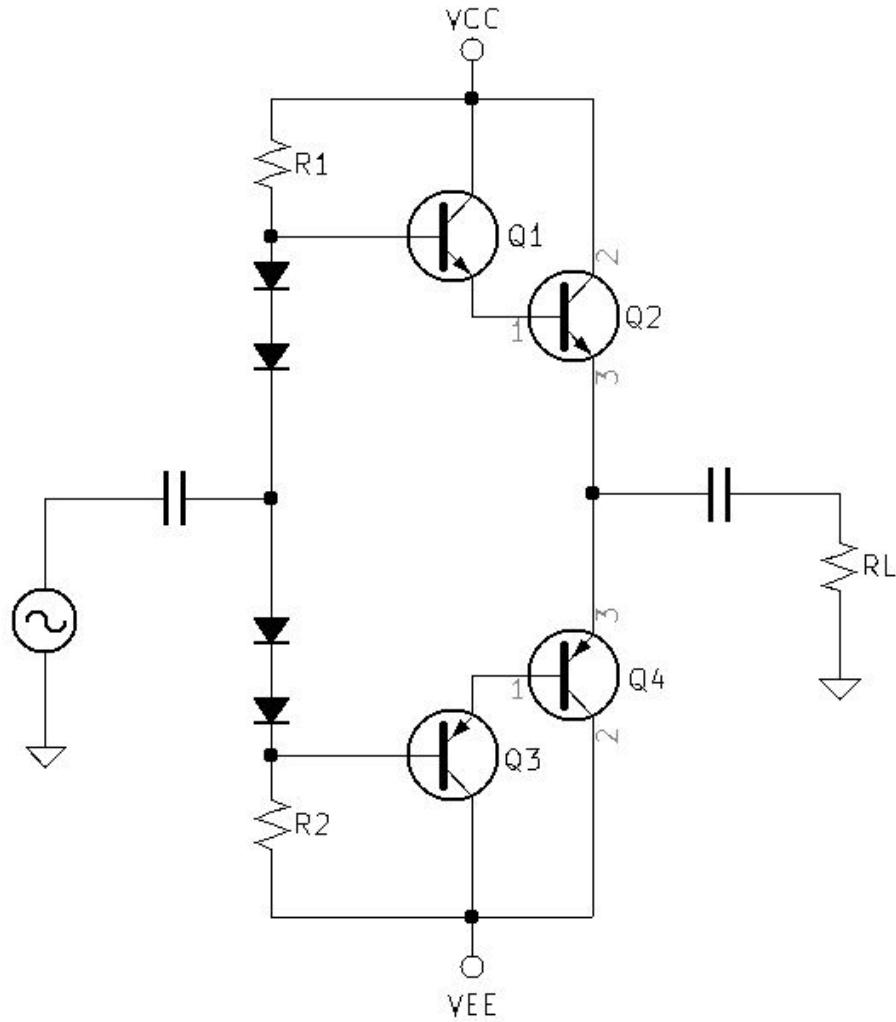


Figure 5.8: Class AB Amplifier with Darlington Pair for High Power Applications

Using Darlington Pairs will improve both power capabilities and the input impedance Z_{in} of the amplifier. Q2 and Q4 can be power transistors like the TIP41 and TIP42. Power transistors typically have a lower beta than their low-power general-purpose counterparts. Design using the previous section steps while adjusting the formulas to account for the additional components in the circuit.

5.3.3 Shoot-Through Protection using Swamping Resistors

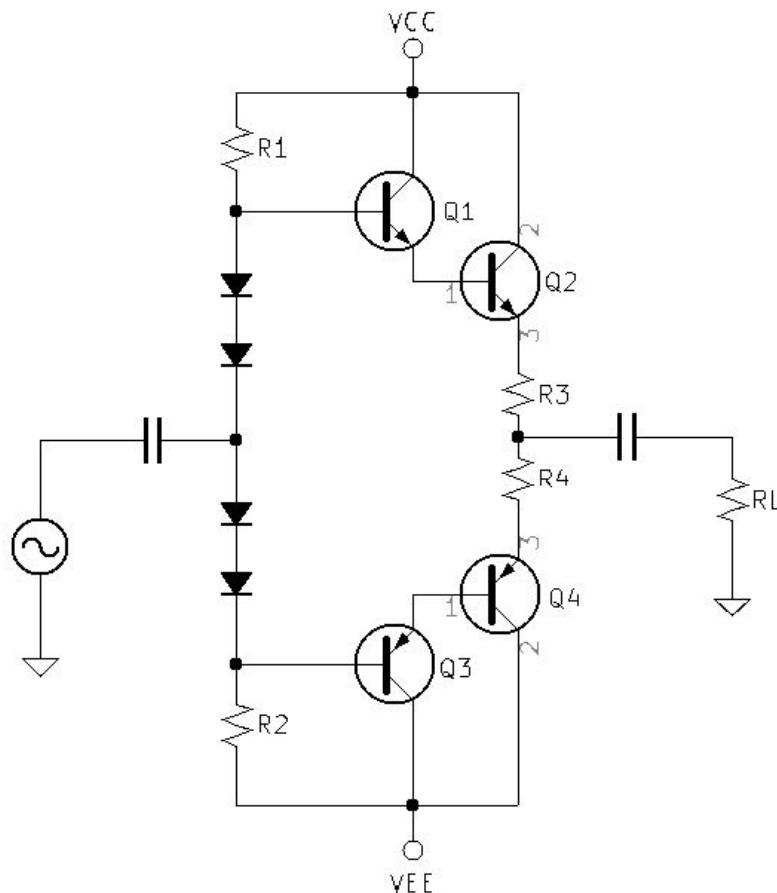


Figure 5.9: Class AB Amplifier with Swamping Resistors R3 and R4

Shoot-Through

Observe Figure 5.9. A potentially serious problem with Push-Pull Amplifiers is Shoot-Through. Shoot-Through occurs when both power transistors (Q2 and Q4) turn on at the same time due to excessive bias voltage. This creates a path for current from VCC directly to VEE with little or no opposition (resistance). By placing Swamping Resistors R3 and R4 in the current path we can limit the Shoot-Through current.

Swamper Resistor Value

Typically, a Push-Pull Amplifier is used to provide high current gain for a small load resistance, for example, an 8Ω speaker. Considering our load resistance if we used 8Ω Swamping

Resistors we would lose half of our signal voltage across at the Swampers. Ideally, the Swamper Resistors will be at a minimum 10x smaller than the load resistance.

$$R_{Swamper} \leq \frac{RL}{10}$$

$$R3 \leq \frac{RL}{10}$$

$$R4 = R3$$

5.3.4 Crossover Distortion

Observe Figure 5.10. Crossover distortion occurs when both power transistors are off at the same time and the input signal has not overcome the biasing needs to turn on one of the transistors. Observe Figure 5.10. By removing two of the diodes, the Crossover Distortion should become observable.

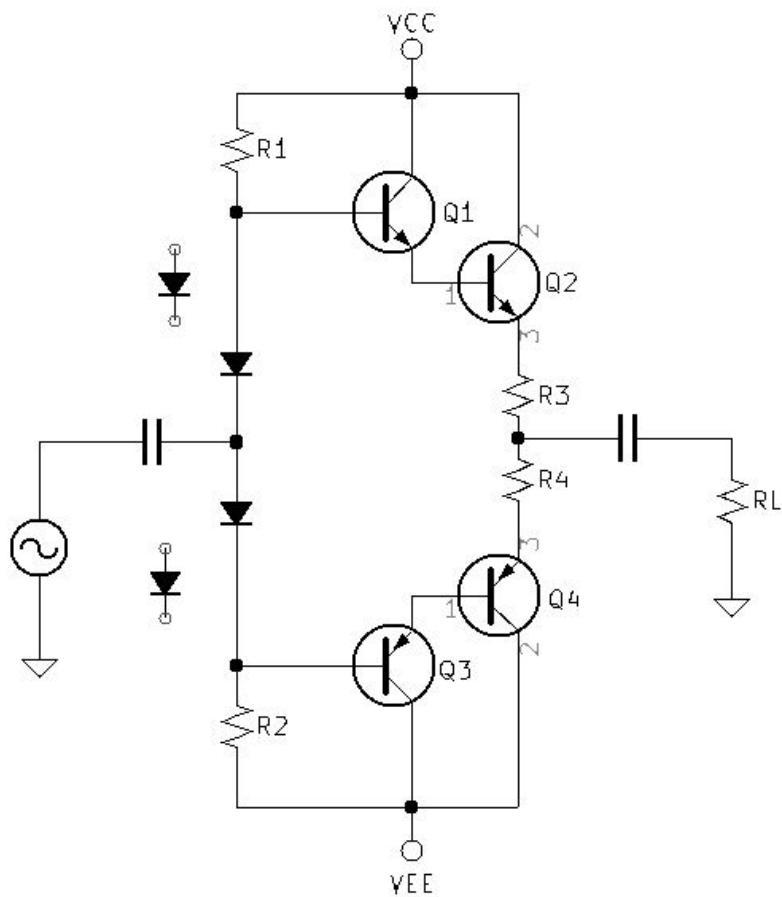


Figure 5.10: Measuring Crossover Distortion

5.3.5 Push-Pull Calibration

Calibrating the circuit to have a small amount of acceptable Shoot-Through current will eliminate Crossover Distortion. This is accomplished by adjusting the bias voltage.

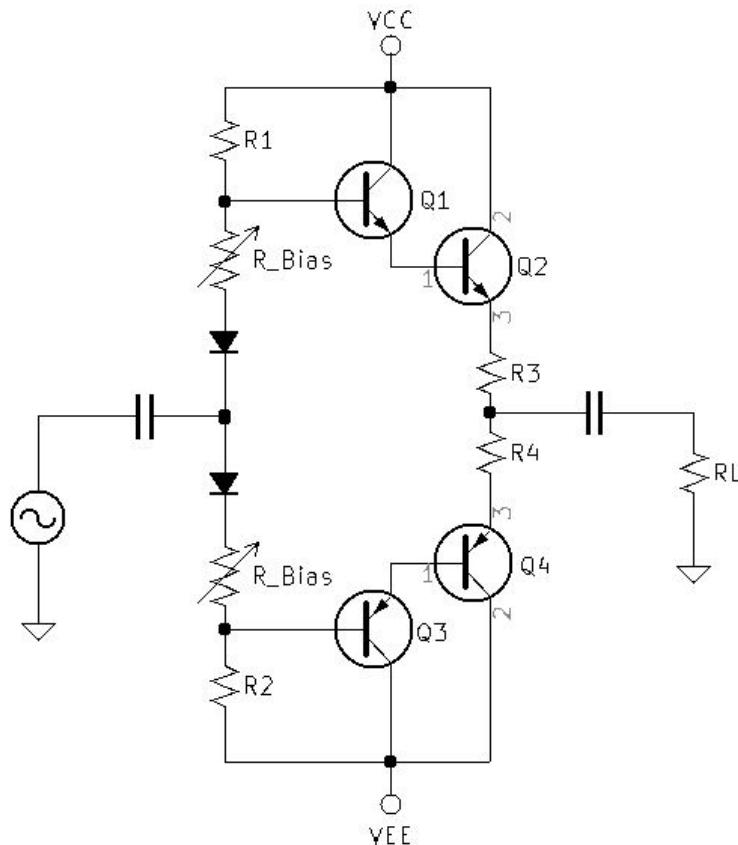


Figure 5.11: Push-Pull Calibration

Bias Voltage Calibration

A Shoot-Through current of $\approx 30mA$ will eliminate Crossover Distortion. When testing the DC biasing of the designed Push-Pull circuit with the Swamping Resistors (Fig. 5.9), one of three scenarios will occur.

Scenario One: The measured current through the Swamper resistors is approximately 30mA indicating that the Push-Pull is properly calibrated.

$$\checkmark I_{ShootThrough} = \frac{V_{R3}}{R3} \approx 30mA$$

Scenario Two: The measured current through the Swamper resistors is greater than 30mA indicating that the Push-Pull is over-biased.

X $I_{ShootThrough} = \frac{V_{R3}}{R3} > 30mA$

Reduce the bias voltage across the Swamping Resistors. Measure the voltage from the base of Q1 to the Emitter of Q2 then add the desired voltage for R3. Remove one diode per side as seen in Fig. 5.11. Calculate the proper resistor value to achieve the desired voltage.

$$R_{Bias} < \frac{V_{Diode}}{I_{Diode}}$$

Scenario Three: The measured current through the Swamper resistors is less than 30mA indicating that the Push-Pull is under-biased.

X $I_{ShootThrough} = \frac{V_{R3}}{R3} < 30mA$

Increase the bias voltage across the Swamping Resistors. Measure the voltage from the base of Q1 to the Emitter of Q2 then add the desired voltage for R3. Remove one diode per side as seen in Fig. 5.11. Calculate the proper resistor value to achieve the desired voltage.

$$R_{Bias} > \frac{V_{Diode}}{I_{Diode}}$$

Once bias calibration is complete and the Shoot-through is approximately 30mA, the Crossover Distortion will be eliminated.

5.3.6 Push-Pull Vout Max Peak Calculations

The Vout Max Peak of a Push-Pull Amplifier should be approximately equal to the VCE voltage of one of the power transistors, as long as the Swamping resistor is ten times smaller than the load resistance.

$$Vout_{MaxP} \approx VCE_{Q2}$$

$$Vout_{MaxP} = \frac{VCE_{Q2}}{R3+RL} \times RL$$

5.3.7 Push-Pull Zin Calculations

Referencing Figure 5.9. Zin is the impedance that the Generator sees.

$$Zin \approx R1//R2$$

Analyze as though Q1 is on and Q4 is off:

$$Zin = (((((RL + R3 + r'e_{Q2}) \times (\beta_{Q2} + 1)) + r'e_{Q1}) \times (\beta_{Q1} + 1)) // R1) + r'd + r'd) // (r'd + r'd + R2)$$

$$\Rightarrow r'd = \frac{0.026v}{I_D}$$

5.3.8 Push-Pull Zout Calculations

Referencing Figure 5.9. Zout is the impedance that the Load sees.

$$Z_{out} \approx r'e_{Q2} + R3$$

Analyze as though Q1 is on and Q4 is off:

$$Z_{out} = \frac{\left(\frac{((R_{gen}/(2r'd+R2))+2r'd)/R1+r'e_{Q1})}{\beta_{Q1}+1} \right)}{\beta_{Q2}+1} + r'e_{Q2} + R3$$

$$\Rightarrow r'd = \frac{0.026v}{I_D}$$

5.4 Heat Sinks

Heat Sink Calculation examples:

5.4.1 TIP41 Thermal Considerations

Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +150	°C
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Figure 5.12: TIP41 Maximum Temperature data

The Maximum Operating Temperature for a TIP41 according to the data-sheet is 150°C. To avoid part damage, I like to design for a Maximum Design Temperature of 90% of the absolute maximum temperature.

$$MaxTemp_{Design} = 0.9(MaxTemp_{Absolute})$$

$$TIP41_MaxTemp_{90\%} = 0.9(TIP41_MaxTemp_{Absolute})$$

$$TIP41_MaxTemp_{90\%} = 0.9(150^{\circ}C)$$

$$TIP41_MaxTemp_{90\%} = 135^{\circ}C$$

Compensate for ambient temperature.

$$TIP41_MaxTemp_{Design} = 135^{\circ}C - Ambient$$

$$TIP41_MaxTemp_{Design} = 135^{\circ}C - 25^{\circ}C$$

$$TIP41_MaxTemp_{Design} = 110^{\circ}C$$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	R_{thJC}	1.67	°C/W
Thermal Resistance, Junction-to-Ambient	R_{thJA}	57	°C/W

Figure 5.13: TIP41 Thermal Resistance data

The Junction-to-Ambient Thermal Resistance is used when the device has no heat sink attached.

$$ThermalR_{Ambient} = \frac{57}{1W}$$

If the Maximum desired Temperature is 135 degrees C, Solve for the Maximum power in Watts.

$$\frac{57^\circ}{1W} = \frac{110^\circ}{X}$$

$$X(57^\circ) = (110^\circ)1W$$

$$X = \frac{(110^\circ)1W}{(57^\circ)}$$

$$X = \frac{110W}{57} \text{ (degrees cancel)}$$

$$X = 1.93W$$

$$MaxPowerDissipation_{TIP_Ambient} = 1.93W \text{ (No Heat Sink)}$$

SERIES: HSE-BX-02 | **DESCRIPTION:** HEAT SINK

FEATURES

- TO-220 package
- placement pins for secure PCB attachment
- round hole for component attachment
- multiple available cut lengths

**MODEL**

model	length [mm]	thermal resistance ¹				power dissipation ¹ @ 75°C ΔT, nat conv [W]
		@ 75°C ΔT, nat conv [°C/W]	@ 1 W, nat conv [°C/W]	@ 1 W, 200 LFM [°C/W]	@ 1 W, 400 LFM [°C/W]	
HSE-B20254-035H	25.4	12.93	14.40	3.28	2.49	5.80
HSE-B20381-035H	38.1	11.54	13.64	3.66	2.76	6.50
HSE-B20508-035H	50.8	9.62	12.98	5.17	3.28	7.80
HSE-B20508-035H-W ²	50.8	9.62	12.98	5.17	3.28	7.80
HSE-B20635-035H	63.5	8.15	10.92	4.35	2.86	9.20
HSE-B20635-035H-W ²	63.5	8.15	10.92	4.35	2.86	9.20

Figure 5.14: HSE-BX-02 series Heat Sink data

5.4.2 HSE-B20254-035H

When using a heat sink, add the Thermal Resistance in series to find the Total Thermal Resistance between the device and the heat sink.

HSE-B20254-035H Thermal Resistance = 12.93°C/W

TIP41 Thermal Resistance Junction to Case= $1.67^{\circ}\text{C}/\text{W}$

Total Thermal Resistance = $12.93^{\circ}\text{C}/\text{W} + 1.67^{\circ}\text{C}/\text{W}$

Total Thermal Resistance = $14.6^{\circ}\text{C}/\text{W}$

Divide the Total Thermal Resistance into the Designed Maximum Temperature to find the Maximum Power for the HSE-B20254-035H.

$$\text{HSE-B20254-035H}_{MaxPower} = \frac{MaxTemp_{Design}}{ThermalR_{Total}}$$

$$\text{HSE-B20254-035H}_{MaxPower} = \frac{110^{\circ}\text{C}}{14.6^{\circ}\text{C}/\text{W}}$$

✓ HSE-B20254-035H_{MaxPower} = 7.534 Watts

5.4.3 HSE-B20635-035H

When using a heat sink, add the Thermal Resistance in series to find the Total Thermal Resistance between the device and the heat sink.

HSE-B20635-035H Thermal Resistance = $8.15^{\circ}\text{C}/\text{W}$

TIP41 Thermal Resistance Junction to Case= $1.67^{\circ}\text{C}/\text{W}$

Total Thermal Resistance = $8.15^{\circ}\text{C}/\text{W} + 1.67^{\circ}\text{C}/\text{W}$

Total Thermal Resistance = $9.82^{\circ}\text{C}/\text{W}$

Divide the Total Thermal Resistance into the Designed Maximum Temperature to find the Maximum Power for the HSE-B20635-035H.

$$\text{HSE-B20635-035H}_{MaxPower} = \frac{MaxTemp_{Design}}{ThermalR_{Total}}$$

$$\text{HSE-B20635-035H}_{MaxPower} = \frac{110^{\circ}\text{C}}{9.82^{\circ}\text{C}/\text{W}}$$

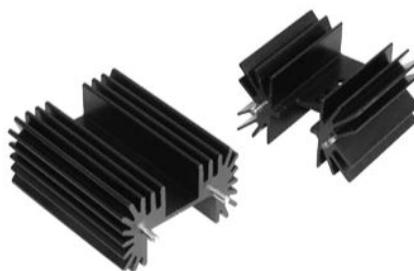
✓ HSE-B20635-035H_{MaxPower} = 11.2 Watts

F and R Series Heatsinks

For TO-218, TO-220 and TO-247 devices

FEATURES

- For vertical mounting with solderable pins
- For TO-220, TO-218, TO-247



SERIES SPECIFICATIONS

Heatsink Part Number	Height (in. $\pm .010$ / $mm \pm .25$)	For Package Type	Ohmite Resistor Series	Surface Area (mm^2)	Weight (g)	Thermal Res.* ($^{\circ}C/W$)
RA-T2X-25E	1.0/25.4	TO-220, -218, -247	TBH25, TCH35, TEH70, TEH100	8,901	25	4.8
RA-T2X-38E	1.5/38.1	TO-220, -218, -247	TBH25, TCH35, TEH70, TEH100	12,983	38	3.9
RA-T2X-51E	2.0/50.8	TO-220, -218, -247	TBH25, TCH35, TEH70, TEH100	17,065	51	3.5
RA-T2X-64E	2.5/63.5	TO-220, -218, -247	TBH25, TCH35, TEH70, TEH100	21,148	63	3.1
FA-T220-25E	1.0 / 25.4	TO-220, -218, -247	TBH25, TCH35, TEH70, TEH100	9,285	18	4.7
FA-T220-38E	1.5 / 38.1	TO-220, -218, -247	TBH25, TCH35, TEH70, TEH100	13,756	27	3.8
FA-T220-51E	2.0 / 50.8	TO-220, -218, -247	TBH25, TCH35, TEH70, TEH100	18,222	37	3.4
FA-T220-64E	2.5 / 63.5	TO-220, -218, -247	TBH25, TCH35, TEH70, TEH100	22,814	46	3

*Natural convection

Figure 5.15: RA-T2X series Heat Sink data

5.4.4 RA-T2X-25E

When using a heat sink, add the Thermal Resistance in series to find the Total Thermal Resistance between the device and the heat sink.

$$\text{RA-T2X-25E Thermal Resistance} = 4.8^{\circ}C/W$$

$$\text{TIP41 Thermal Resistance Junction to Case} = 1.67^{\circ}C/W$$

$$\text{Total Thermal Resistance} = 4.8^{\circ}C/W + 1.67^{\circ}C/W$$

$$\text{Total Thermal Resistance} = 6.47^{\circ}C/W$$

Divide the Total Thermal Resistance into the Designed Maximum Temperature to find the Maximum Power for the RA-T2X-25E.

$$\text{RA-T2X-25E}_{\text{MaxPower}} = \frac{\text{MaxTemp}_{\text{Design}}}{\text{ThermalR}_{\text{Total}}}$$

$$\text{RA-T2X-25E}_{\text{MaxPower}} = \frac{110^{\circ}C}{6.47^{\circ}C/W}$$

✓ RA-T2X-25E_{MaxPower} = 17 Watts

5.4.5 RA-T2X-64E

When using a heat sink, add the Thermal Resistance in series to find the Total Thermal Resistance between the device and the heat sink.

$$\text{RA-T2X-64E Thermal Resistance} = 3.1^\circ\text{C}/\text{W}$$

$$\text{TIP41 Thermal Resistance Junction to Case} = 1.67^\circ\text{C}/\text{W}$$

$$\text{Total Thermal Resistance} = 3.1^\circ\text{C}/\text{W} + 1.67^\circ\text{C}/\text{W}$$

$$\text{Total Thermal Resistance} = 4.77^\circ\text{C}/\text{W}$$

Divide the Total Thermal Resistance into the Designed Maximum Temperature to find the Maximum Power for the RA-T2X-64E.

$$\text{RA-T2X-64E}_{MaxPower} = \frac{\text{MaxTemp}_{Design}}{\text{ThermalR}_{Total}}$$

$$\text{RA-T2X-64E}_{MaxPower} = \frac{110^\circ\text{C}}{4.77^\circ\text{C}/\text{W}}$$

✓ RA-T2X-64E_{MaxPower} = 23 Watts

Table 5.1: Heat Sink Max Power Dissipation Calculations for the TIP41 T0220.

Heat Sink	Total Thermal Resistance	$\text{Power}_{Max} = \frac{110}{\text{ThermalR}_{Total}}$
TIP41 (No Heat Sink)	57°C/W	1.930W
HSE-B20254-035H	14.6°C/W	7.534W
HSE-B20635-035H	9.82°C/W	11.202W
RA-T2X-25E	6.47°C/W	17.002W
RA-T2X-64E	4.77°C/W	23.061W

Chapter 6

Differential Amplifiers

6.1 Objectives

Differential Amplifiers:

- Define Differential Amplification and Operating Modes.
- Design and design considerations for both a Differential Amplifier with an R_{Tail} and a Differential Amplifier with Constant Current Source.
- Analysis of Differential Amplifiers to include Calculating DC Currents and Voltages, Z_{IN} , Z_{OUT} , and Gains.
- Calculate the Common Mode Rejection Ratio
- Implementation of Differential Amplifier Gain Control.

6.2 Differential Amplifier Introduction

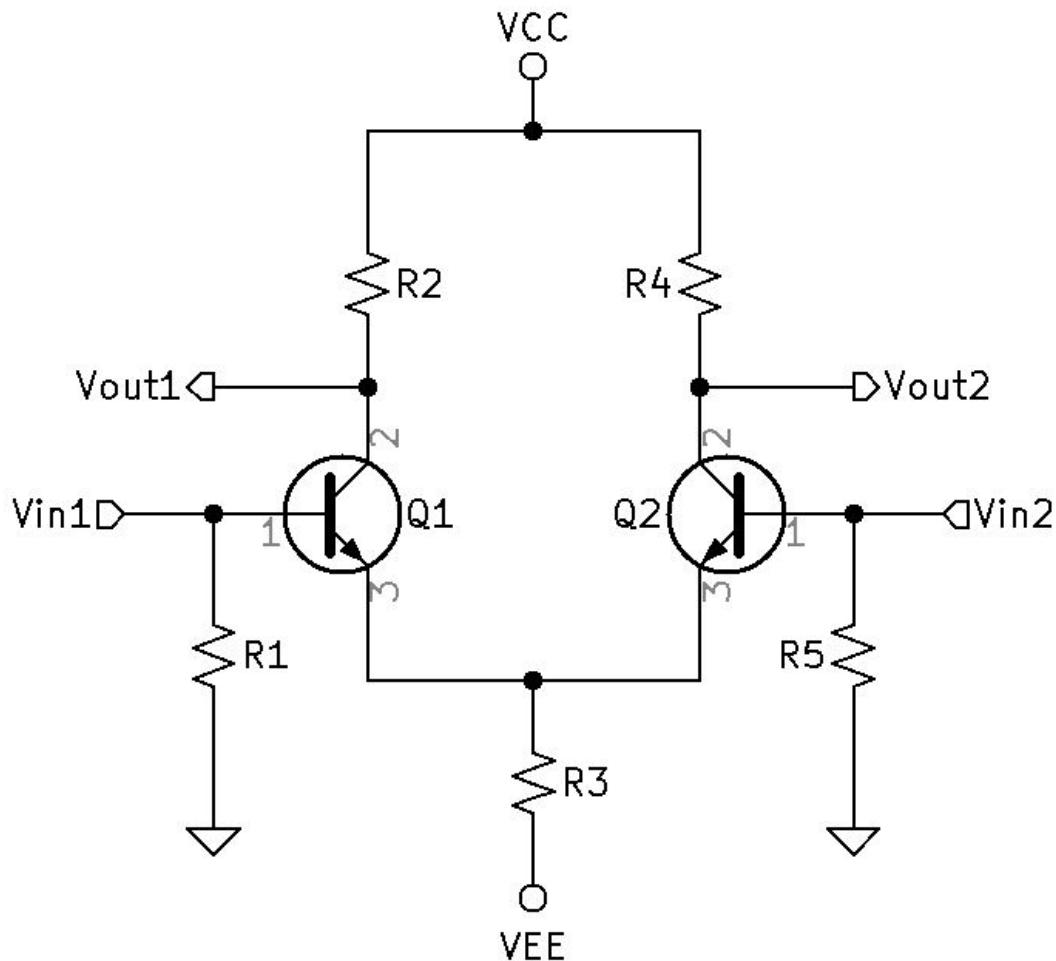


Figure 6.1: Differential Amplifier Introduction

A **Differential Amplifier** is an amplifier that produces outputs that are a function of the difference between the two inputs.

Refer to Figure 6.1.

- ✓ Transistors Q1 and Q2 are Beta matched.
- ✓ The Collector Resistors are matched ($R_2 = R_4$).
- ✓ The Base Resistors are matched ($R_1 = R_5$).
- ✓ The tail current, I_{R3} is equal to $2 \times I_E$.

6.3 Differential Amplifier Operational Modes

6.3.1 Single-Ended Differential Input

The Differential Amplifier is operated with one input grounded while signal voltage is applied to the other input.

Single-Ended Differential Input *Inverting Amplification*

The output waveform is 180° out of phase with the input.

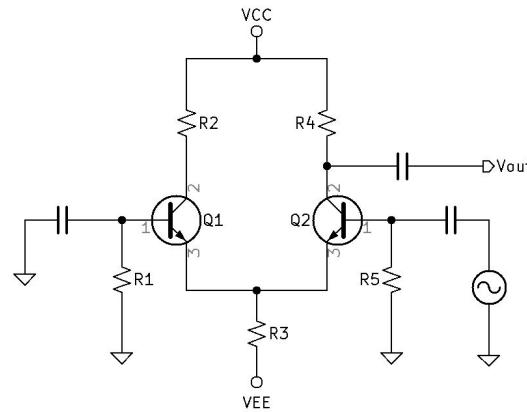


Figure 6.2: Differential Amplifier Single-Ended Differential Input *Inverting Amplifier*

Single-Ended Differential Input *Non-Inverting Amplification*

The output waveform is in phase with the input.

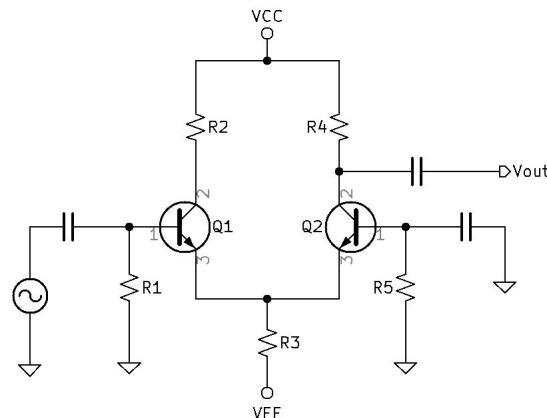


Figure 6.3: Differential Amplifier Single-Ended Differential Input *Non-Inverting Amplifier*

6.3.2 Double-Ended Differential Inputs

The two inputs are 180° out of phase with each other and the gain doubled, $2 \times \Delta V$.

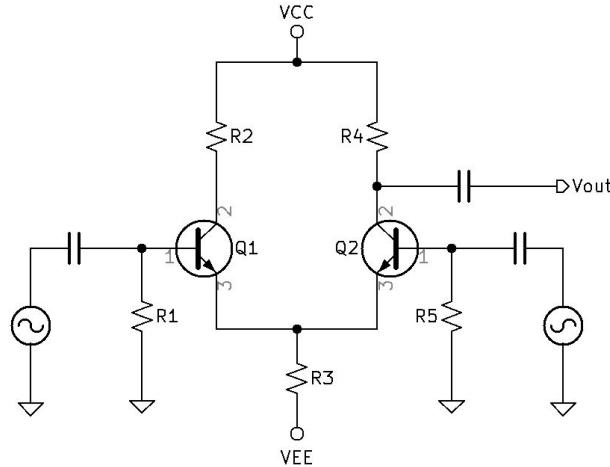


Figure 6.4: Differential Amplifier Double-Ended Differential Input

Double-Ended Common-Mode Inputs

The two inputs are in phase with each other and the gain is approximately zero, $\Delta V \approx 0$.

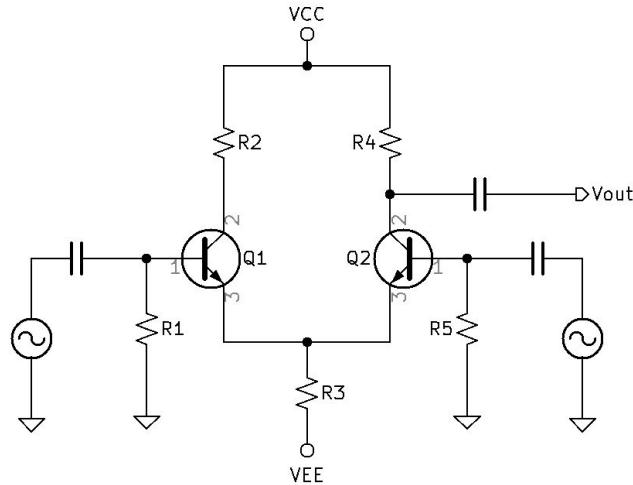


Figure 6.5: Differential Amplifier Double-Ended Common-Mode Input

Differential Amplification XLR Example

The beauty of the Differential Amplifier is that can achieve the benefits of both Differential and Common-Mode amplification within the same application and at the same time. Imagine a mono guitar signal is sent to a Diff-Amp and Right (out of phase) and Left (in phase) signals are produced and sent down a long XLR cable. On the way the XLR cable will pick up lots of noise, that noise will be in phase on both the Left and Right channels. At the other end of the cable, a second Diff-Amp is ready to provide Diff Gain ($2 \times \Delta V$) to the original guitar signal and Common-Mode gain of approximately zero to the in-phase noise that was picked up along the way.

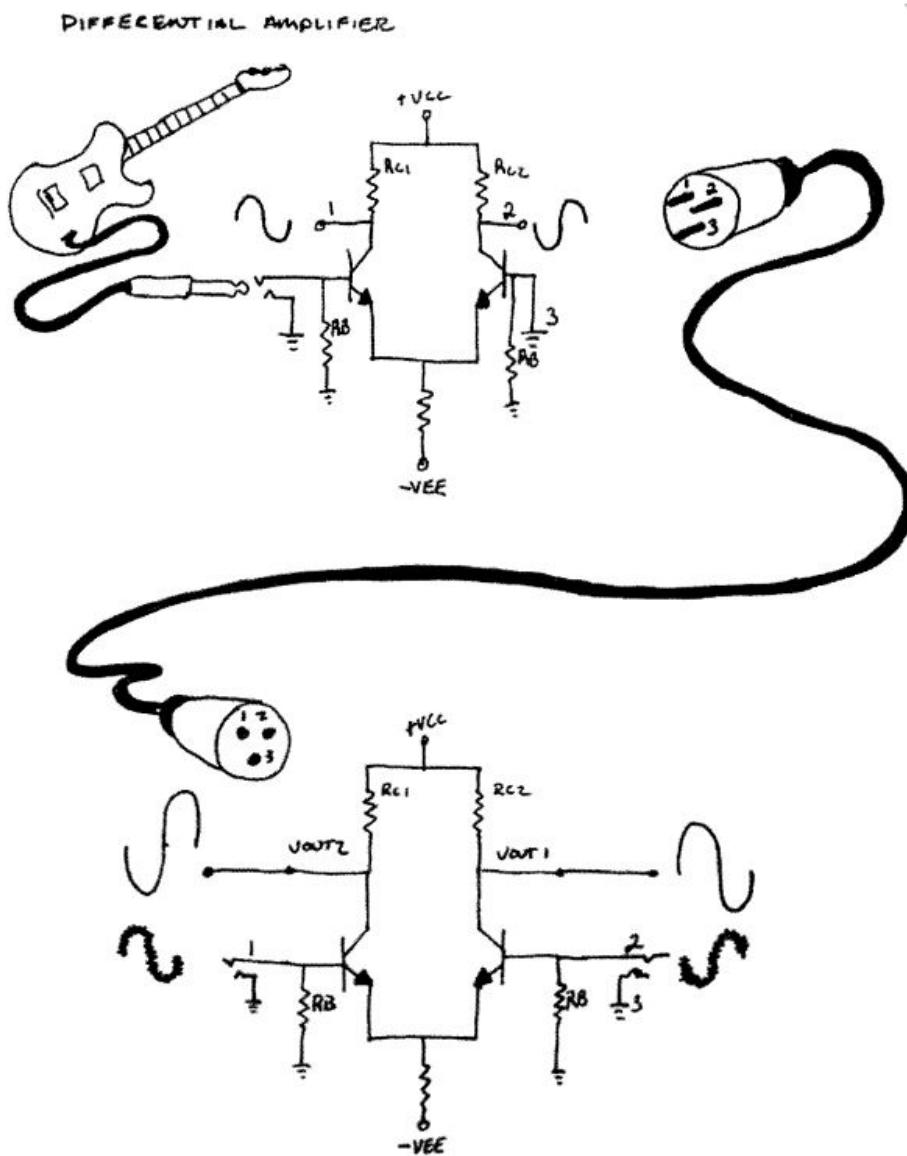


Figure 6.6: Differential Amplifiers: Concurrent $2 \times \Delta V$ with Common-Mode noise rejection.

6.4 Differential Amplifier R-Tail Practical Design

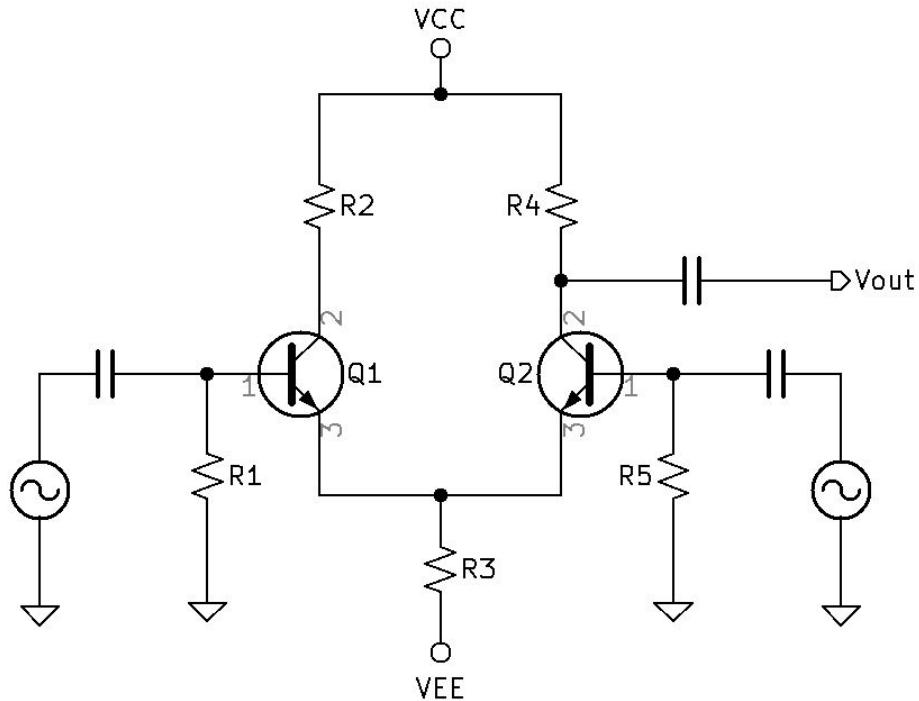


Figure 6.7: Differential Amplifier with Tail Resistor

DC Biasing

Maximum Desired Peak Output Voltage

Determining the Maximum Peak Output Voltage needed for the amplifier.

$$V_{out,MaxP} = ?$$

Determine VCC and VEE based on Maximum Desired Peak Output Voltage

If the amplifier is biased correctly, using the following procedure, 45% of the total DC voltage ($VCC + VEE$) will be approximately equal to the Maximum Peak Output Voltage.

$$V_{out,MaxP} \approx 45\%(VCC + VEE)$$

Solve for $VCC + VEE$.

$$VCC + VEE \approx \frac{V_{out,MaxP}}{45\%}$$

Making VCC equal to VEE, we can solve for VCC in terms of our desired Maximum Peak Output Voltage.

$$VCC + VCC \approx \frac{V_{outMaxP}}{45\%}$$

$$2VCC \approx \frac{V_{outMaxP}}{45\%}$$

$$VCC \approx \frac{V_{outMaxP}}{2 \times 0.45}$$

Headroom, adjusting VCC and VEE to prevent amplifier distortion

To prevent undesired distortion caused by the amplifier operating near Vout Max Peak, we need to add headroom to the biasing circuit. For design purposes, 10% of additional should be adequate. This means multiplying the calculated VCC by 110%

$$VCC = \frac{V_{outMaxP}}{2 \times 0.45} \times 1.1$$

VEE is equal to VCC but negative in polarity.

$$VEE = -VCC$$

Voltage Optimization 45, 45, 10

The total bias voltage is equal to $VCC + VEE$.

$$VDC_{Total} = VEE + VCC$$

Make VRC equal to 45% of the total bias voltage.

$$V_{RC} = 0.45 \times VDC_{Total}$$

Make VCE equal to 45% of the total bias voltage.

$$V_{CE} = 0.45 \times VDC_{Total}$$

Make the Tail Voltage equal to 10% of the total bias voltage.

$$V_{RTail} = 0.1 \times VDC_{Total}$$

The Collector Resistor

The Ideal output impedance of any amplifier is low. Because Z_{out} is equal to RC , we want RC to be as small as possible. We know V_{RC} is equal to V_{CE} . Using the power rating of the transistor, we can determine a suitable RC value.

Look up the Maximum Power Rating for the transistor.

Set the transistor power to safely operate at half of its max power.

$$P_Q = \frac{P_{Q1Max}}{2}$$

Because V_{CE} and V_{RC} are equal and they have I_C in common, they will also dissipate the same power.

$$P_{RC} = P_Q$$

Calculate RC in terms of Voltage and Power.

$$P = \frac{V^2}{R}$$

$$P_{RC} = \frac{(V_{RC})^2}{RC}$$

$$RC = \frac{(V_{RC})^2}{P_{RC}}$$

Solve for I_C in terms of Power and Resistance.

$$P = I^2 \times R$$

$$P_{RC} = (I_{RC})^2 \times RC$$

$$(I_{RC})^2 = \frac{P_{RC}}{RC}$$

$$I_{RC} = \sqrt{\frac{P_{RC}}{RC}}$$

Referencing Figure 6.8. R_2 and R_4 are equal to RC .

$$R_2 = R_4 = RC$$

The Base Resistor

Using Kirchhoff's Voltage Law, calculate VRB.

$$-V_{RTail} - V_{BE} - V_{RB} + VEE = 0$$

$$V_{RB} = VEE - V_{BE} - V_{RTail}$$

Solve for IB.

$$IB = \frac{IC}{\beta}$$

Note: Differential Amplifier transistors, ideally, are beta-matched. Also, The Differential Amplifier circuit is Beta dependent.

Solve for RB using Ohm's Law.

$$RB = \frac{V_{RB}}{I_{RB}}$$

Reference Figure 6.8. $R1 = R5 = RB$

The Tail Resistor

Using Kirchhoff, the Tail Resistor Current is equal to $2 \times IE$.

Find IE

$$IE = IB \times (\beta + 1)$$

Find the Tail Resistor Current

$$I_{Tail} = 2 \times IE$$

The dynamic emitter resistance ($r'e$)

$$r'e \approx \frac{0.026}{IE}$$

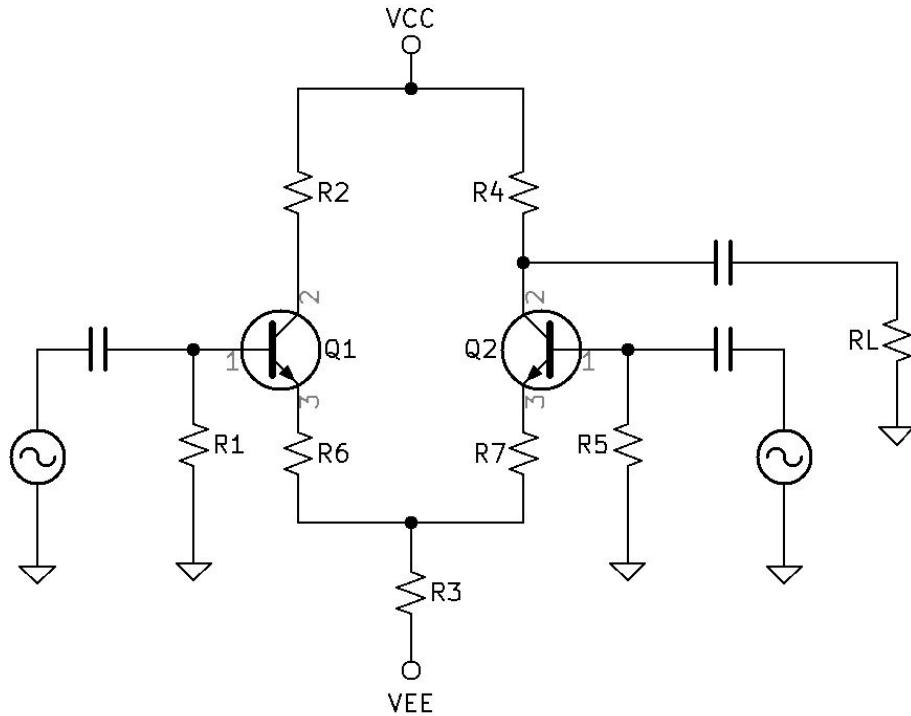


Figure 6.8: Differential Amplifier with Swamp Resistors and Load Resistance

Swamping Resistors

Adding the Swamping Resistors R_6 and R_7 will improve stability and Z_{in} of the Differential Amplifier, while reducing the dependency on $r'e$.

$$R_{Swamp} = 10 \times r'e$$

$$r'e = \frac{0.026}{IE}$$

$$R6 = R7 = R_{Swamp}$$

Load Resistance

To Maximize V_{out} Peak, ensure that RL is ten times larger than Z_{out} ($R4$) of the Differential Amplifier. Understand that RL may also represent the Z_{In} of the next stage, perhaps a Push-Pull Amplifier or an additional voltage gain stage if needed.

$$RL = 10 \times Z_{out, DiffAmp}$$

$$RL = 10 \times R4$$

$$RL = Z_{in, Stage2}$$

$$Z_{in, Stage2} \geq 10 \times R4$$

6.5 Differential Amplifier R-Tail Calculations

Input Impedance

Refer to Figure 6.8. Z_{In} is equal to the impedance that the Generator sees.

$$Z_{In} = [(((\frac{R_{Gen}}{\beta+1} + r'e + R_{Swamp}) // R_{Tail}) + R_{Swamp} + r'e) \times (\beta + 1)] // RB$$

Output Impedance

The Output Impedance Z_{Out} is equal to the Impedance that the Load sees.

$$Z_{Out} = RC$$

Single-Ended Inverting Voltage Gain

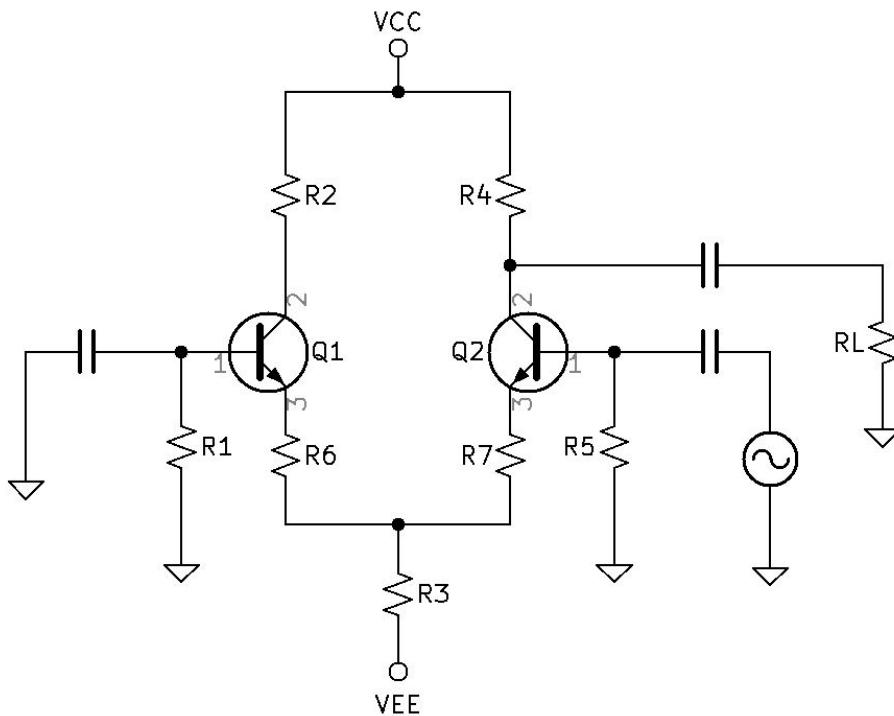


Figure 6.9: Single-Ended Inverting Differential Amplifier

$$\Delta V_{CE} = \frac{V_{out}}{V_{in}}$$

$$\Delta V_{CE} = \frac{IC(RL//RC)}{IB(((r'e+R_{Swamp})//R_{Tail})+r'e+R_{Swamp}) \times (\beta+1)}$$

$$\Delta V_{CE} = \alpha \frac{RL//RC}{((r'e+R_{Swamp})//R_{Tail})+r'e+R_{Swamp}}$$

Single-Ended Non-Inverting Voltage Gain

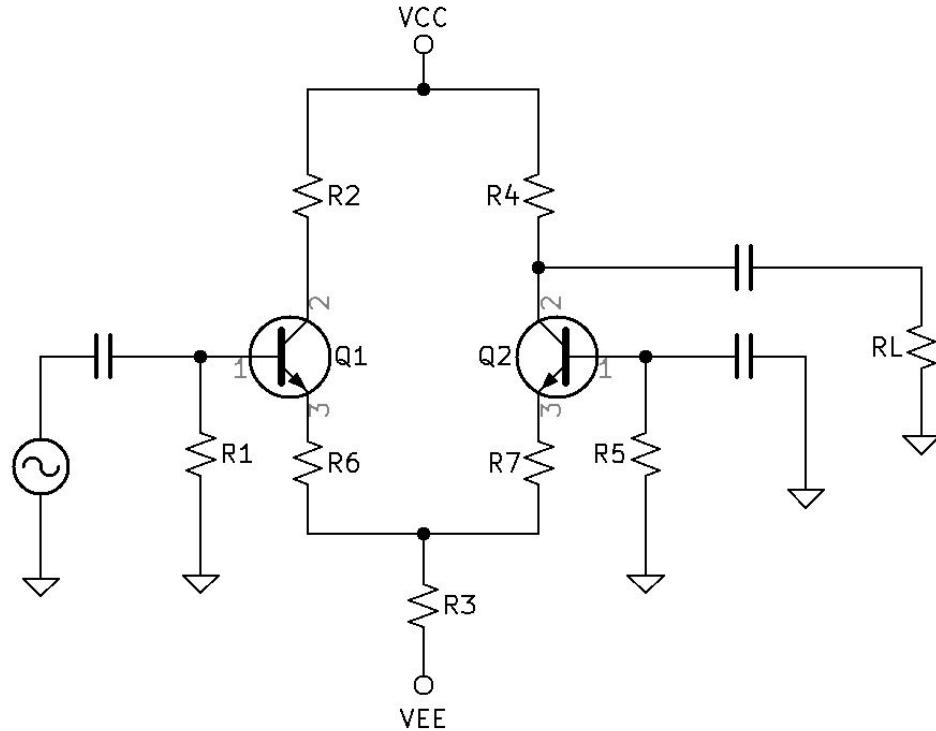


Figure 6.10: Single-Ended Non-Inverting Differential Amplifier

$$\Delta V_{CC} = \frac{V_{out}}{V_{in}} \approx 0.5$$

$$\Delta V_{CC} = \frac{IE((r'e + R_{Swamp})//R_{Tail})}{IB(((r'e + R_{Swamp})//R_{Tail}) + R_{Swamp} + r'e) \times (\beta + 1)}$$

$$\Delta V_{CC} = \frac{IE((r'e + R_{Swamp})//R_{Tail})}{IE(((r'e + R_{Swamp})//R_{Tail}) + R_{Swamp} + r'e)}$$

$$\Delta V_{CC} = \frac{(r'e + R_{Swamp})//R_{Tail}}{((r'e + R_{Swamp})//R_{Tail}) + R_{Swamp} + r'e}$$

$$\Delta V_{CB} = \frac{V_{out}}{V_{in}} \approx 2 \times \Delta V_{CE}$$

$$\Delta V_{CB} = \frac{IC(RL//RC)}{IE(R_{Swamp} + r'e)}$$

$$\Delta V_{CB} = \alpha \frac{RL//RC}{R_{Swamp} + r'e}$$

$$\Delta V_{CCCB} = \Delta V_{CC} \times \Delta V_{CB}$$

Double-Ended Gain

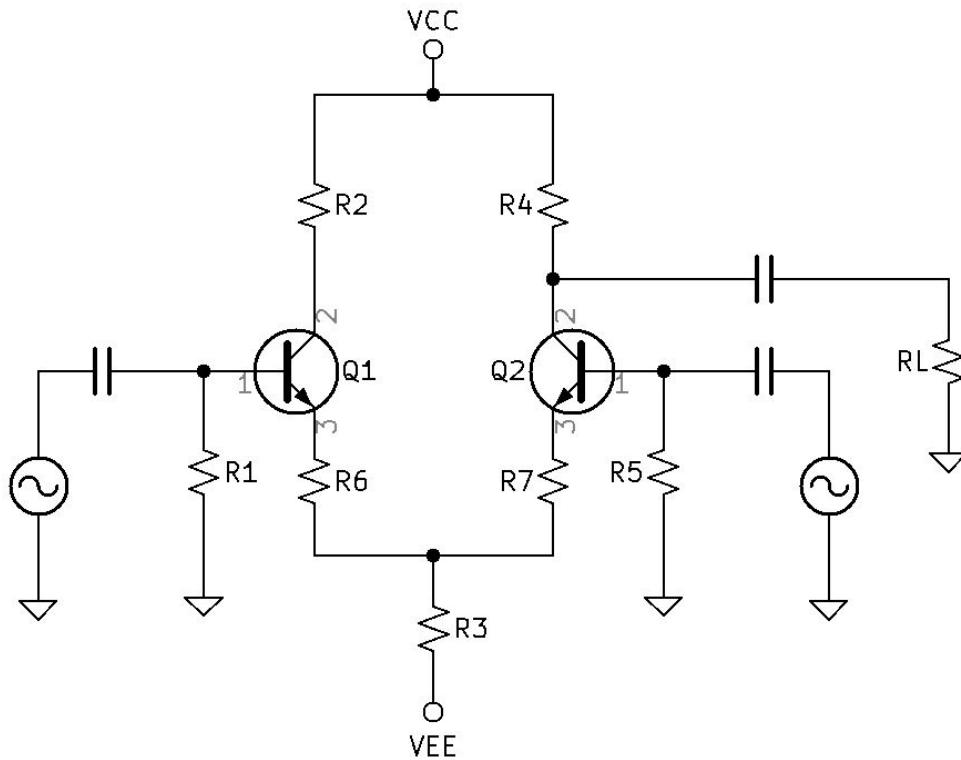


Figure 6.11: Double-Ended Common-Mode Differential Amplifier

Common-Mode

In Common-Mode, the two input signals are in phase will essentially cancel each-other at the output.

$$\Delta V_{CM} \approx 0$$

$$\Delta V_{CM} = \Delta V_{CCCB} - |\Delta V_{CE}|$$

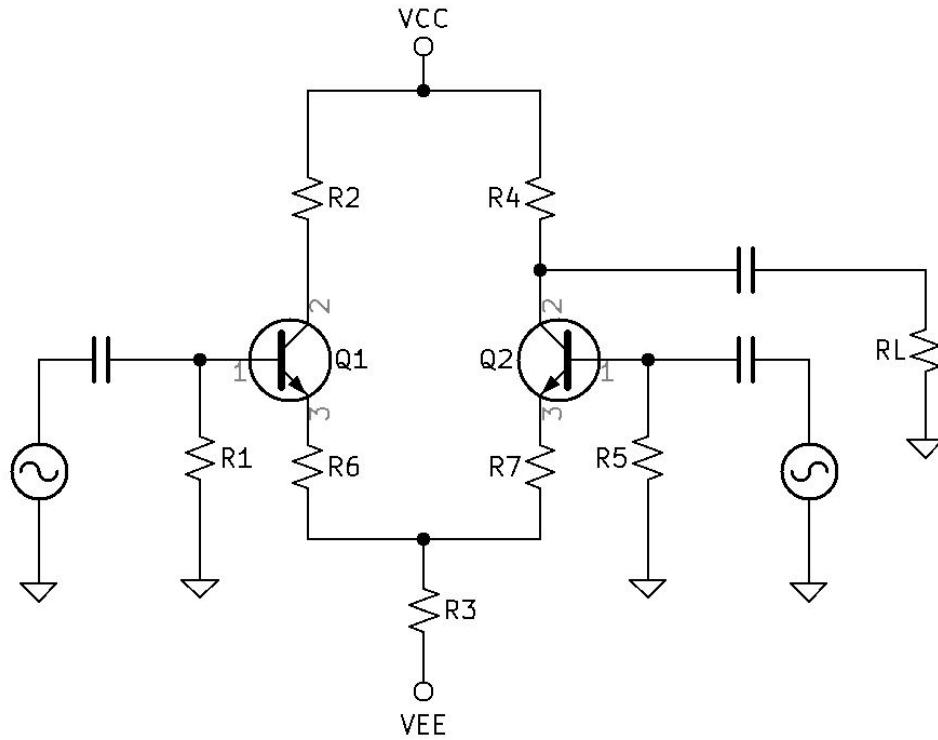


Figure 6.12: Double-Ended Differential-Mode Differential Amplifier

Differential-Mode

In Differential-Mode, the two input signals are out of phase will essentially double the signal voltage gain at the output.

$$\Delta V_{DM} \approx 2 \times \Delta V_{CE}$$

$$\Delta V_{DM} = \Delta V_{CCCB} + |\Delta V_{CE}|$$

Common Mode Rejection Ratio

The Common Mode Rejection Ratio is the ratio of Common-Mode signal to Differential-Mode signal.

$$CMMR = \frac{\Delta V_{CM}}{\Delta V_{DM}}$$

Common Mode Rejection Ratio in decibels

$$CMMR_{dB} = 20 \log \frac{\Delta V_{CM}}{\Delta V_{DM}}$$

6.6 Differential Amplifier Constant Current Source Practical Design

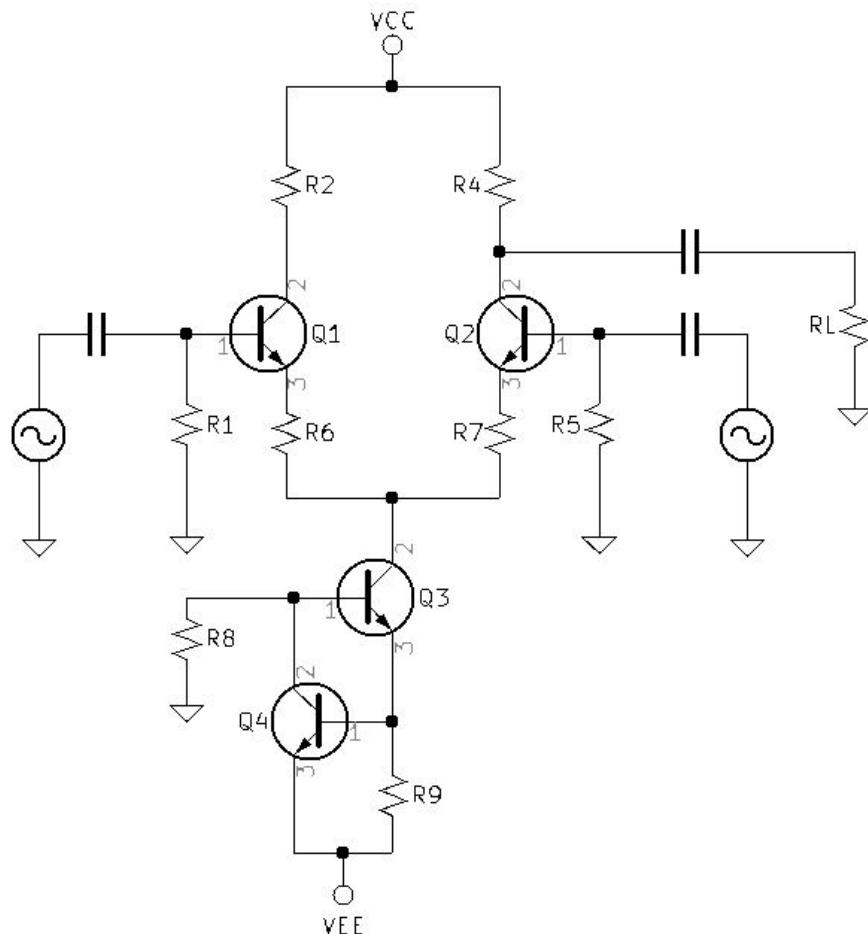


Figure 6.13: Differential Amplifier with a Constant Current Source

Reference Figure 6.13. Notice that R3 the Tail Resistor from the previous section has been replaced with the Constant Current Source which is comprised of Q3, Q4, R8, and R9.

VCC, VEE, Base Resistors, Collector Resistors, and Swamping Resistors are all calculated in the previous section.

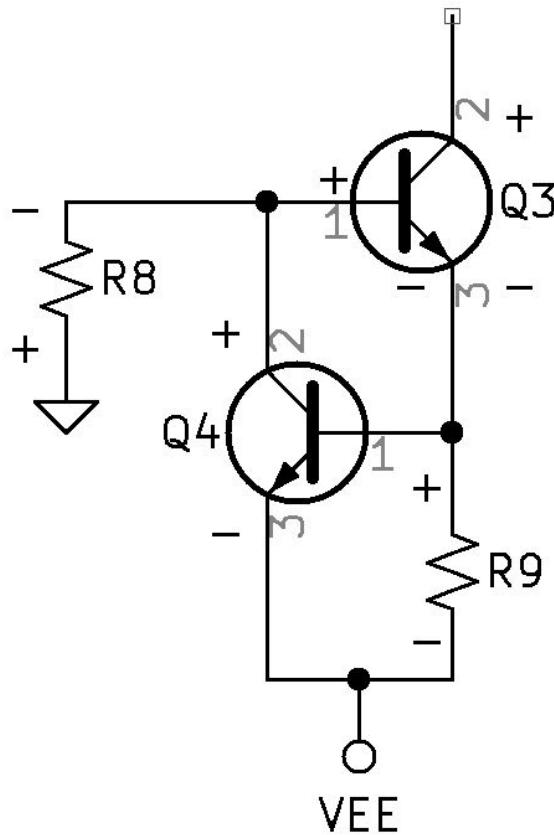


Figure 6.14: Constant Current Source

DC Biasing:

Q3 and Q4 Beta Match

Beta Q3 and Q4 are equal or nearly equal.

$$\beta_{Q3} \approx \beta_{Q4}$$

Designing in Terms of Tail Current

The collector current of Q3 is equal to the desired tail current.

$$IC_{Q3} = I_{Tail} = 2 \times IE$$

The base current of Q3 is equal to the desired tail current divided by beta.

$$IB_{Q3} = \frac{I_{Tail}}{\beta}$$

The emitter current of Q3 is equal to the desired tail current (IC) plus the base current of Q3.

$$IE_{Q3} = IC_{Q3} + IB_{Q3}$$

$$IE_{Q3} = I_{Tail} + \frac{I_{Tail}}{\beta}$$

Notice the emitter current of Q3 equation can also be written as being equal to I_{R9} plus IB_{Q4}

$$IE_{Q3} = I_{R9} + IB_{Q4}$$

R9

Make the current of R9 equal to the tail current.

$$I_{R9} = I_{Tail}$$

Use Kirchhoff's Voltage Law to find the R9 Voltage.

$$V_{R9} = VBE_{Q4}$$

$$V_{R9} = 0.7V$$

Use Ohm's Law to find the R9.

$$R9 = \frac{V_{R9}}{I_{R9}}$$

$$R9 = \frac{0.7V}{I_{tail}}$$

R8

Find IB Q4. If the emitter current of Q3 is equal to the tail current plus the tail current divided by beta and IR9 is now equal to the tail current, then the base current of Q4 must be equal to the tail current divided by beta. Which is also equal to IB_{Q3} .

$$IE_{Q3} = IC_{Q3} + IB_{Q3}$$

$$IE_{Q3} = I_{Tail} + \frac{I_{Tail}}{\beta}$$

$$IE_{Q3} = I_{R9} + \frac{I_{Tail}}{\beta}$$

$$IB_{Q4} = \frac{I_{Tail}}{\beta}$$

$$IB_{Q4} = IB_{Q3}$$

Find IC Q4. Again, assuming that Q3 and Q4 are beta matched, then the betas cancel and IC Q4 is equal to the Tail Current.

$$IC_{Q4} = IB_{Q4} \times \beta$$

$$IC_{Q4} = \frac{I_{Tail}}{\beta} \times \beta$$

$$IC_{Q4} = I_{Tail}$$

Find R8's current. IR8 is equal to the base current of Q3 plus the collector current of Q4.

$$I_{R8} = IB_{Q3} + IC_{Q4}$$

$$I_{R8} = \frac{I_{tail}}{\beta} + I_{tail}$$

Factor out the I_{tail} :

$$I_{R8} = I_{tail}\left(\frac{1}{\beta} + 1\right)$$

$$I_{R8} \approx I_{tail}$$

Use Kirchhoff's Voltage Law to calculate the R8 Voltage.

$$V_{R8} + VBE_{Q3} + VBE_{Q4} - VEE = 0$$

$$V_{R8} = VEE - VBE_{Q3} - VBE_{Q4}$$

$$V_{R8} = VEE - 1.4V$$

Find R8 using Ohm's Law.

$$R8 = \frac{V_{R8}}{I_{R8}}$$

$$R8 = \frac{VEE - 1.4V}{I_{tail}\left(\frac{1}{\beta} + 1\right)} \approx \frac{VEE - 1.4V}{I_{tail}}$$

6.7 Differential Amplifier Constant Current Source Calculations

Input Impedance

Refer to Figure 6.13. Z_{In} is equal to the impedance that the Generator sees. Notice the collector resistance of Q3 will appear as open or infinitely large.

$$Z_{In} = \left(\left(\frac{R_{Gen}/RB}{\beta+1} + r'e + R_{Swamp} + R_{Swamp} + r'e \right) \times (\beta + 1) \right) // RB$$

Output Impedance

The Output Impedance Z_{Out} is equal to the Impedance that the Load sees.

$$Z_{Out} = RC$$

Load

Make the load (RL) a minimum of ten times larger than Z_{Out} .

Single-Ended Gains:

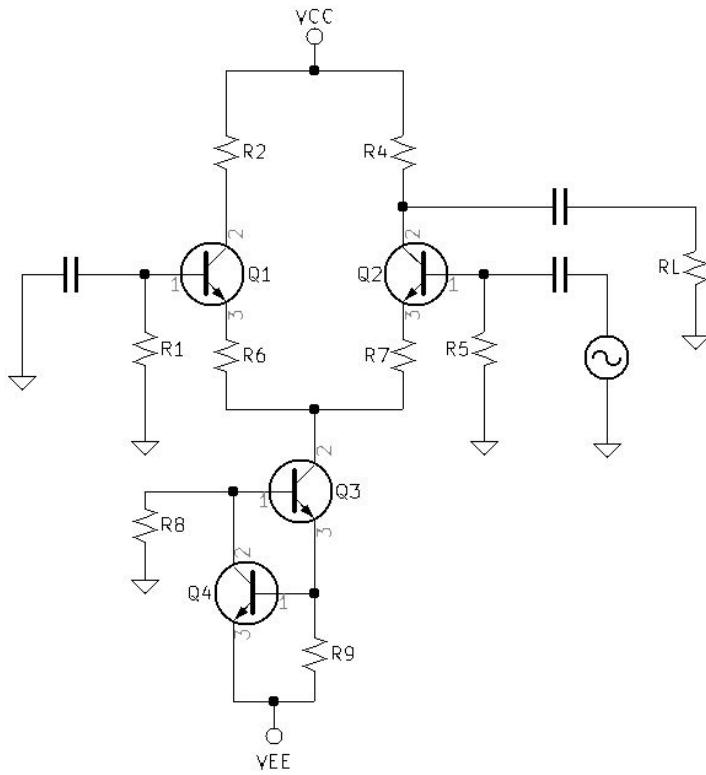


Figure 6.15: Single-Ended Inverting Differential Amplifier with Constant Current Source

Single-Ended Inverting Voltage Gain

See Figure 6.15.

$$\Delta V_{CE} = \frac{V_{out}}{V_{in}}$$

$$\Delta V_{CE} = \frac{IC(RL//RC)}{IB((r'e+R_{Swamp})+r'e+R_{Swamp}) \times (\beta+1)}$$

$$\Delta V_{CE} = \alpha \frac{RL//RC}{2r'e+2R_{Swamp}}$$

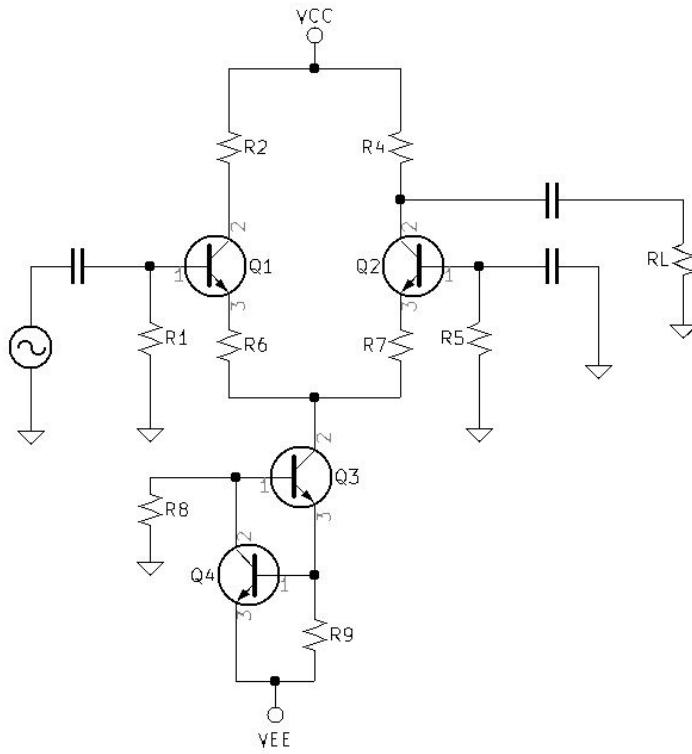


Figure 6.16: Single-Ended Non-Inverting Differential Amplifier with Constant Current Source

Single-Ended Non-Inverting Voltage Gain

See Figure 6.16.

$$\Delta V_{CC} = \frac{V_{out}}{V_{in}}$$

$$\Delta V_{CC} = \frac{IE(r'e + R_{Swamp})}{IB(r'e + R_{Swamp} + R_{Swamp} + r'e) \times (\beta + 1)}$$

$$\Delta V_{CC} = \frac{IE((r'e + R_{Swamp})}{IE(r'e + R_{Swamp} + R_{Swamp} + r'e)}$$

$$\Delta V_{CC} = \frac{r'e + R_{Swamp}}{2r'e + 2R_{Swamp}}$$

$$\Delta V_{CC} = \frac{r'e + R_{Swamp}}{2(r'e + R_{Swamp})}$$

$$\Delta V_{CC} = \frac{1}{2} \times \frac{r'e + R_{Swamp}}{r'e + R_{Swamp}}$$

$$\Delta V_{CC} = \frac{1}{2} \times 1$$

$$\boxed{\Delta V_{CC} = \frac{1}{2} = 0.5}$$

$$\Delta V_{CB} = \frac{V_{out}}{V_{in}} \approx 2 \times \Delta V_{CE}$$

$$\Delta V_{CB} = \frac{IC(RL//RC)}{IE(R_{Swamp} + r'e)}$$

$$\boxed{\Delta V_{CB} = \alpha \frac{RL//RC}{R_{Swamp} + r'e}}$$

$$\Delta V_{CCCB} = \Delta V_{CC} \times \Delta V_{CB}$$

$$\Delta V_{CCCB} = 0.5 \times \Delta V_{CB}$$

Double-Ended Gains:

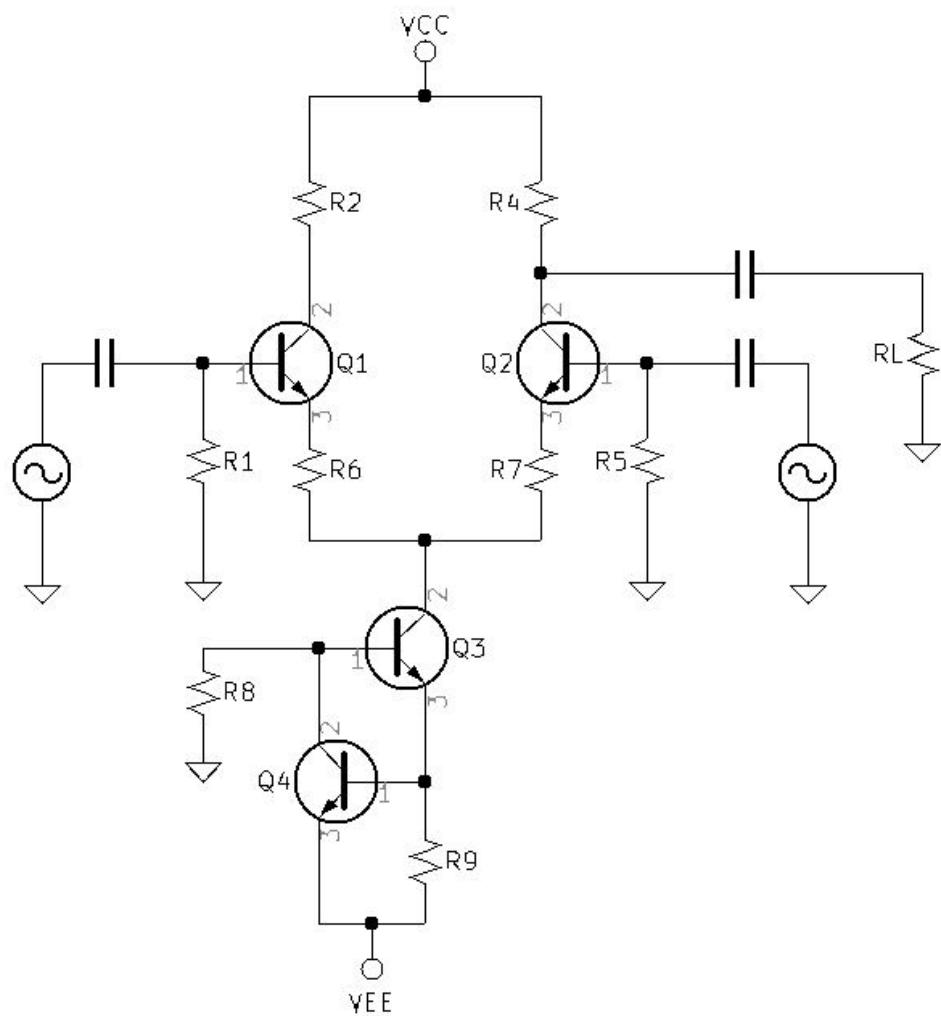


Figure 6.17: Double-Ended Common-Mode Differential Amplifier with Constant Current Source

Common-Mode

In Common-Mode, the two input signals are in phase and will essentially cancel each other at the output.

$$\Delta V_{CM} \approx 0$$

$$\Delta V_{CM} = \Delta V_{CCCB} - |\Delta V_{CE}|$$

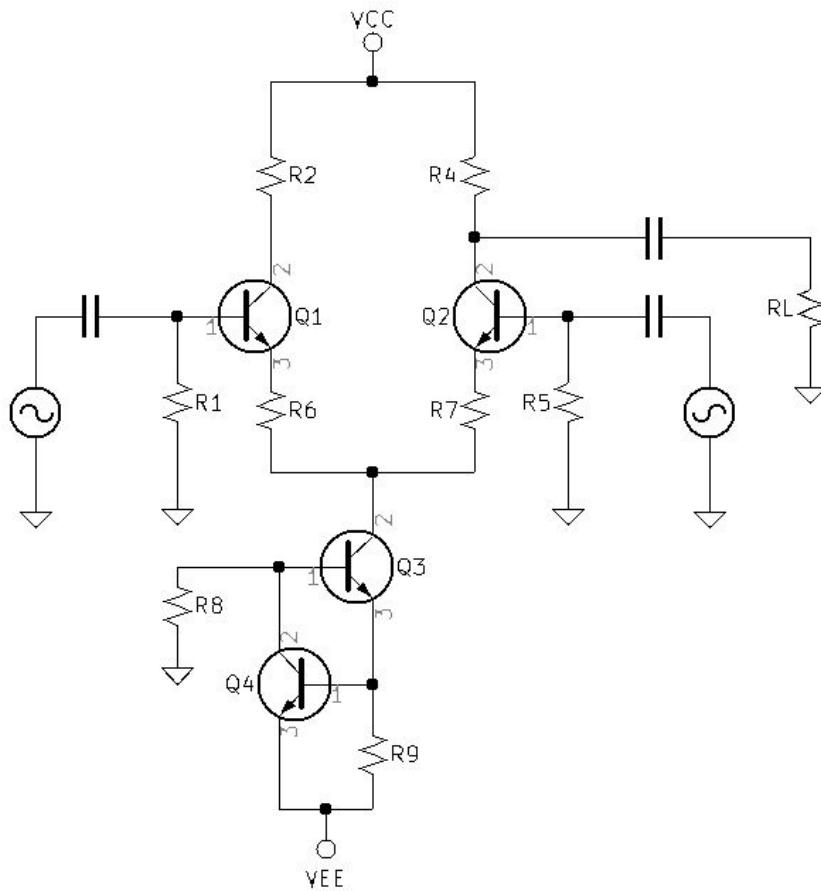


Figure 6.18: Double-Ended Differential-Mode Differential Amplifier with Constant Current Source

Differential-Mode

In Differential-Mode, the two input signals are out of phase will essentially double the signal voltage gain at the output.

$$\Delta V_{DM} \approx 2 \times \Delta V_{CE}$$

$$\Delta V_{DM} = \Delta V_{CCCB} + |\Delta V_{CE}|$$

Common Mode Rejection Ratio

The Common Mode Rejection Ratio is the ratio of Common-Mode signal to Differential-Mode signal.

$$CMMR = \frac{\Delta V_{CM}}{\Delta V_{DM}}$$

$$CMMR_{dB} = 20 \log \frac{\Delta V_{CM}}{\Delta V_{DM}}$$

6.8 Differential Amplifier Constant Current Source Practical Design

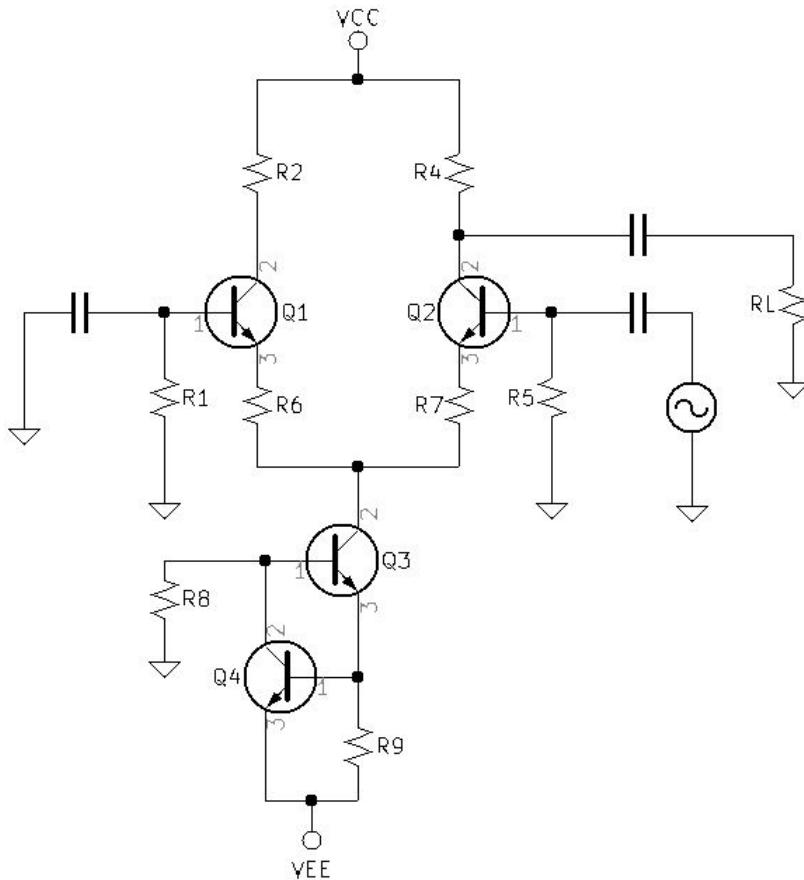


Figure 6.19: Differential Amplifier with a Constant Current Source and Open Loop Gain

Just like Operational Amplifiers, we can control the gain of the Differential Amplifier using negative feedback. This is accomplished by feeding back a fraction of the output signal back to the negative input.

6.8.1 Inverting Diff Amp with Gain Control

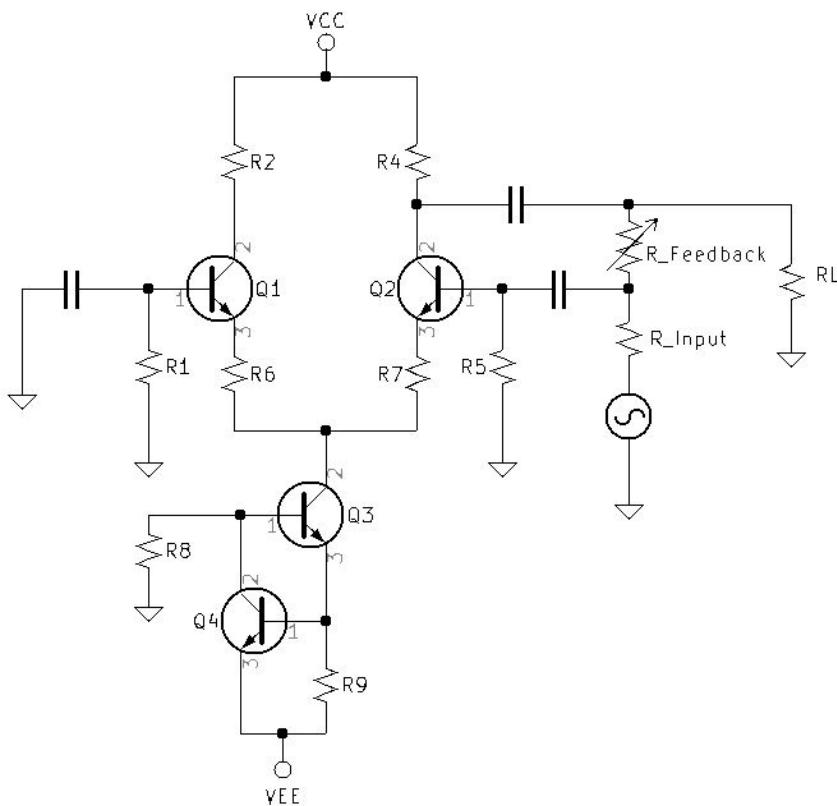


Figure 6.20: Inverting Differential Amplifier with Gain Control

See Figure 6.20. The Inverting Gain will be approximately equal to the feedback resistance divided by the input resistance.

$$\Delta V \approx -\frac{R_{Feedback}}{R_{Input}}$$

6.8.2 Non-Inverting Diff Amp with Gain Control

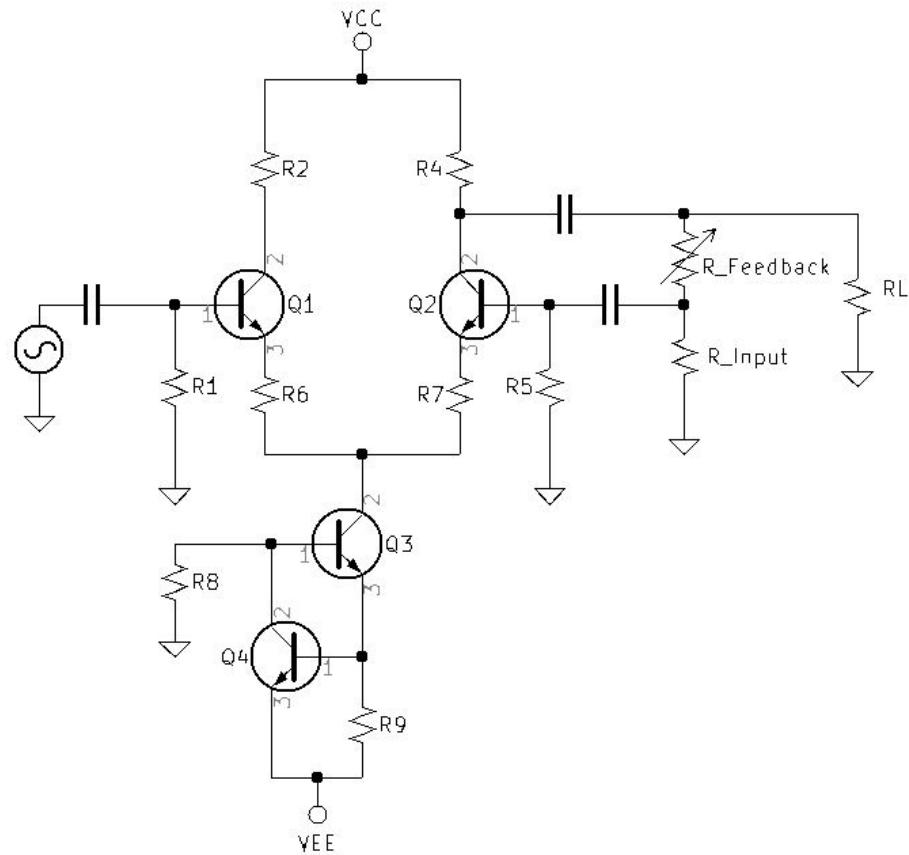


Figure 6.21: Non-Inverting Differential Amplifier with Gain Control

See Figure 6.21. The Non-Inverting Gain will be approximately equal to the feedback resistance divided by the input resistance plus one.

$$\Delta V \approx \frac{R_{Feedback}}{R_{Input}} + 1$$

6.8.3 Non-Inverting Diff Amp with Gain Control and Push-Pull Amplifier

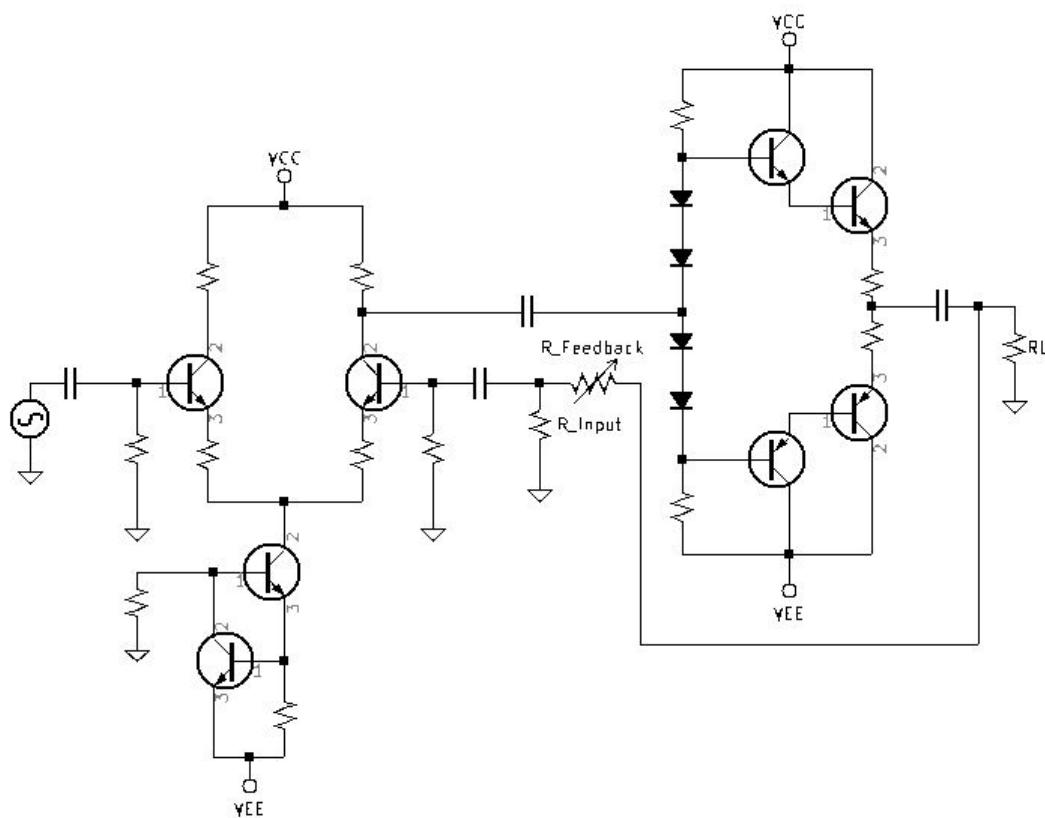


Figure 6.22: Non-Inverting Differential Amplifier with Gain Control and Push-Pull Amplifier

Figure 6.22 is an example of a Differential Amplifier using a Push-Pull Amplifier for current gain. For increased signal stability and voltage gain control, the negative feedback comes from the load.

Chapter 7

Operational Amplifiers

7.1 Objectives

Operational Amplifiers:

- Define the Ideal Characteristics Operational Amplifiers.
- Define the Practical Characteristics of the LM741 and TL071
- Define the Ideal Characteristics Operational Amplifiers.
- Identify the basic internal arrangement of an Operational Amplifier.
- Define Operational Amplifier Modes.
- Review the Rules and Steps for calculating Operational Amplifiers
- Identify and locate important specifications using the datasheet.
- Calculate Gains, Frequency Response, and Input & Output Impedances.
- Review Operational Amplifier Comparator Circuits.
- Explore Operational Amplifier Voltage Bounding Circuits.

7.2 Operational Amplifier General Information

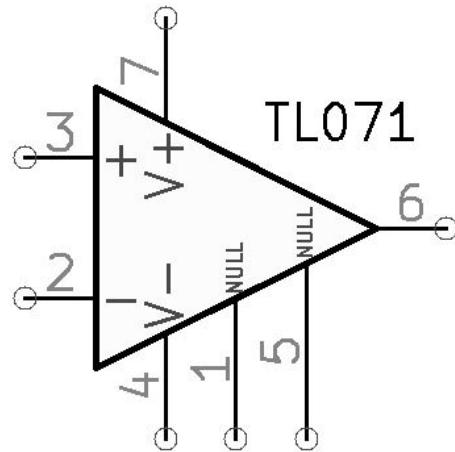


Figure 7.1: Operational Amplifier Introduction

7.2.1 The Ideal Characteristics of the Operational Amplifier

The Ideal Operational Amplifier will have the following characteristics:

- Infinite Gain ($\Delta V = \infty$)
- Infinite Bandwidth (*Frequency* = 0 to ∞ hz)
- Infinite Input Impedance ($Z_{in} = \infty\Omega$)
- Zero Output Impedance ($Z_{out} = 0\Omega$)

7.2.2 The Practical Characteristics of the LM741 Operational Amplifier

The Practical Characteristics of the LM741 Operational Amplifier:

- Very High Voltage Gain ($\Delta V = 200,000$)
- Very High Bandwidth (*Frequency* $\leq 1.5Mhz$)
- Very High Input Impedance ($Z_{in} \approx 2M\Omega$)
- Very Low Output Impedance ($Z_{out} \leq 75\Omega$)

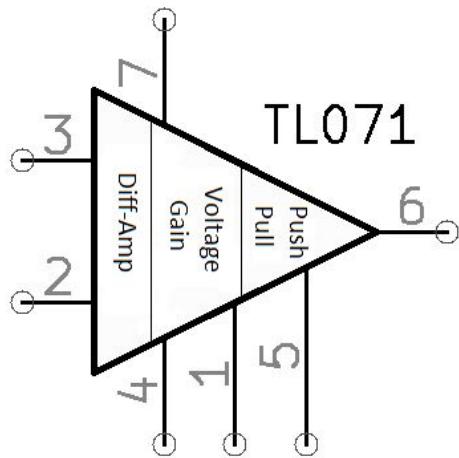


Figure 7.2: Operational Amplifier Basic Internal Arrangement

7.2.3 Basic Internal Arrangement of the Operational Amplifier

The basic internal arrangement of an Operational Amplifier consists of an input Differential Amplifier stage which provides the two out-of-phase inputs, the plus and minus inputs. The next stage is the Voltage Gain stage which provides all the necessary gain. The final stage of the Operational Amplifier is the Push-Pull Amplifier, which provides a current gain capable of up to approximately 50mA. Additionally, the operational amplifier has built-in output short-circuit protection allowing the output to be shorted.

7.2.4 Modes of Operation

Negative Feedback is a highly valuable concept in operational amplifier applications. It involves returning a portion of the amplifier's output voltage to the input with a phase angle that opposes or subtracts from the input signal.

Differential Mode

In Differential Mode the Operational Amplifier will have a signal applied to one input with the other input grounded OR two 180° (opposite) polarity signals are applied to the inputs.

Single-Ended Differential Mode:

- **Non-Inverting, Single-Ended Differential Mode** Signal is applied to the Non-Inverting Input. The Inverting Input is connected to the reference.
- **Inverting, Single-Ended Differential Mode** Signal is applied to the Inverting Input. The Non-Inverting Input is connected to the reference.

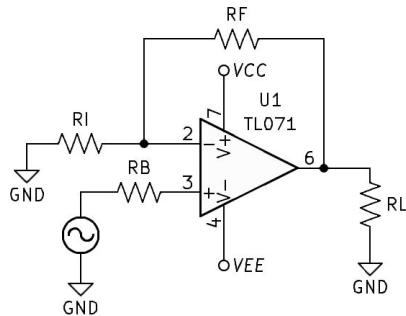


Figure 7.3: Non-Inverting, Single-Ended Differential Mode

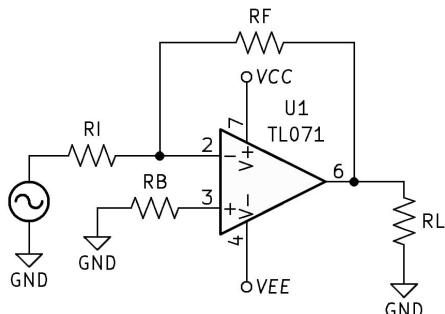


Figure 7.4: Inverting, Single-Ended Differential Mode

Double-Ended Differential Mode:

- **Differential Mode** Inputs are 180° out of phase.
- **Common Mode** Inputs are in-phase.

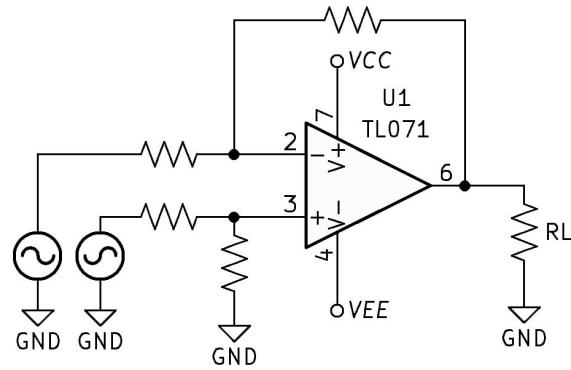


Figure 7.5: Differential Mode, Inputs are 180° out of phase

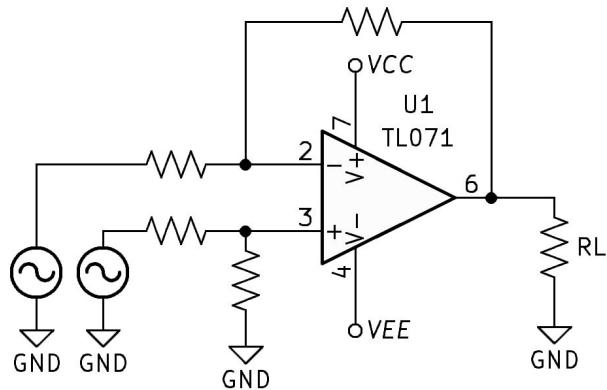


Figure 7.6: Common Mode, Inputs are in phase

7.2.5 Op-Amp Rules:

1. The output will do whatever it can to make the two input voltages equal.
2. No signal current will flow into or out of the inputs.

7.2.6 Op-Amp Steps:

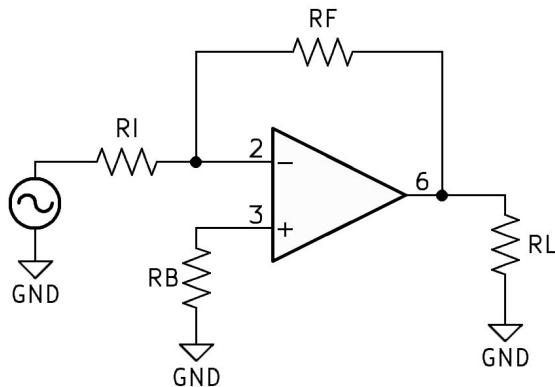


Figure 7.7: Inverting Operational Amplifier

1. Find $V_{(+)}$.
2. With feedback, $V_{(-)} = V_{(+)}$.
3. Find V_{RI} .
4. Find I_{RI} .
5. Find V_{RF} .
6. Kirchhoff to find V_{RL} .

7.2.7 Biasing Resistor (RB):

The two inputs of an Operational Amplifier should see the same or equivalent impedance. The op-amp will operate with mismatched impedances between the inputs however, this is not ideal and may cause DC offset at the output.

For example Figure 7.7.

$$RB = RI//RF$$

7.3 Operational Amplifier Specification Information

7.3.1 Terminology

Δ_{OL} = Open Loop Gain

Δ_{CM} = Common Mode Gain

Common Mode Rejection Ration:

$$CMRR = \frac{\Delta_{OL}}{\Delta_{CM}}$$

$$CMRR_{dB} = 20 \log \frac{\Delta_{OL}}{\Delta_{CM}} \text{ (dB)}$$

Slew Rate is the maximum rate of output voltage change in response to an instantaneous change in input voltage. Slew Rate is often expressed in data sheets as volts per microsecond.

$$SlewRate_{LM741} = \frac{0.5V}{1\mu S}$$



LM741

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6.5 Electrical Characteristics, LM741⁽¹⁾

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset voltage	$R_S \leq 10 \text{ k}\Omega$	$T_A = 25^\circ\text{C}$		1	5	mV
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$			6	mV
Input offset voltage adjustment range	$T_A = 25^\circ\text{C}, V_S = \pm 20 \text{ V}$		± 15			mV
Input offset current	$T_A = 25^\circ\text{C}$	$T_A = 25^\circ\text{C}$	20	200		nA
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	85	500		
Input bias current	$T_A = 25^\circ\text{C}$	$T_A = 25^\circ\text{C}$	80	500		nA
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$			1.5	
Input resistance	$T_A = 25^\circ\text{C}, V_S = \pm 20 \text{ V}$		0.3	2		MΩ
Input voltage range	$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		± 12	± 13		V
Large signal voltage gain	$V_S = \pm 15 \text{ V}, V_O = \pm 10 \text{ V}, R_L \geq 2 \text{ k}\Omega$	$T_A = 25^\circ\text{C}$	50	200		V/mV
		$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$	25			
Output voltage swing	$V_S = \pm 15 \text{ V}$	$R_L \geq 10 \text{ k}\Omega$	± 12	± 14		V
		$R_L \geq 2 \text{ k}\Omega$	± 10	± 13		
Output short circuit current	$T_A = 25^\circ\text{C}$		25			mA
Common-mode rejection ratio	$R_S \leq 10 \Omega, V_{CM} = \pm 12 \text{ V}, T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		80	95		dB
Supply voltage rejection ratio	$V_S = \pm 20 \text{ V to } V_S = \pm 5 \text{ V}, R_S \leq 10 \Omega, T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		86	96		dB
Transient response	Rise time Overshoot	$T_A = 25^\circ\text{C}$, unity gain	0.3			μs
			5%			
Slew rate	$T_A = 25^\circ\text{C}$, unity gain		0.5			V/μs
Supply current	$T_A = 25^\circ\text{C}$		1.7	2.8		mA
Power consumption	$V_S = \pm 15 \text{ V}$	$T_A = 25^\circ\text{C}$	50	85		mW
		$T_A = T_{A\text{MIN}}$	60	100		
		$T_A = T_{A\text{MAX}}$	45	75		

Figure 7.8: LM741 Operational Amplifier Data Sheet Slew Rate

The **Bandwidth** of the Operational Amplifier is given at Unity Gain and is sometimes referred to as Gain Bandwidth Product. The LM741 with a voltage gain of one will have a Bandwidth of 1.5Mhz according to the specifications of Figure 7.9.

Electrical Characteristics, LM741A⁽¹⁾ (continued)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage swing	$V_S = \pm 20 \text{ V}$	$R_L \geq 10 \text{ k}\Omega$	± 16			V
		$R_L \geq 2 \text{ k}\Omega$			± 15	
Output short circuit current	$T_A = 25^\circ\text{C}$		10	25	35	mA
	$T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		10	40		
Common-mode rejection ratio	$R_S \leq 50 \Omega$, $V_{CM} = \pm 12 \text{ V}$, $T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		80	95		dB
Supply voltage rejection ratio	$V_S = \pm 20 \text{ V}$ to $V_S = \pm 5 \text{ V}$, $R_S \leq 50 \Omega$, $T_{A\text{MIN}} \leq T_A \leq T_{A\text{MAX}}$		86	96		dB
Transient response	Rise time	$T_A = 25^\circ\text{C}$, unity gain	0.25	0.8	μs	
	Overshoot				6%	20%
Bandwidth ⁽²⁾	$T_A = 25^\circ\text{C}$		0.437	1.5		MHz

Figure 7.9: LM741 Operational Amplifier Data Sheet Bandwidth at unity gain

7.4 Op-Amp Input and Output Impedance

7.4.1 Inverting Op-Amp Zin and Zout

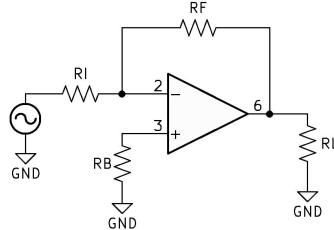


Figure 7.10: Inverting Op-Amp

$$Z_{IN(InvOpAmp)} = (RI + R_{Miller}) // [Zin_{dev}(1 + \Delta vol(\frac{RI}{RI+RF}))]$$

$$R_{Miller} = \frac{RF}{1 + \Delta vol}$$

$$LM741, Zin_{dev} = 2M\Omega$$

$$LM741, \Delta vol = 200,000$$

$$Z_{OUT(InvOpAmp)} = \frac{Zout_{dev}}{1 + \Delta vol(\frac{RI}{RI+RF})}$$

$$LM741, Zout_{dev} = 75\Omega$$

7.4.2 Non-Inverting Op-Amp Zin and Zout

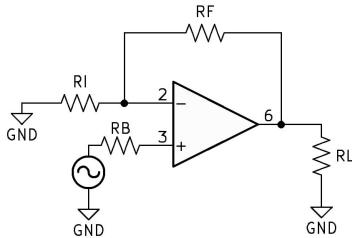


Figure 7.11: Non-Inverting Op-Amp

$$Z_{IN(NonInvertOpAmp)} = Zin_{dev}(1 + \Delta vol(\frac{RI}{RI+RF}))$$

$$LM741, Zin_{dev} = 2M\Omega$$

$$LM741, \Delta vol = 200,000$$

$$Z_{OUT(NonInvertOpAmp)} = \frac{Zout_{dev}}{1 + \Delta vol(\frac{RI}{RI+RF})}$$

$$LM741, Zout_{dev} = 75\Omega$$

7.5 Op-Amp Frequency Response

Frequency Critical Low

The operational amplifier is capable of amplifying DC voltage. Low frequencies can be amplified without attenuation resulting in an F_{cLow} equal to 0hz.

Frequency Critical High

Frequency critical high is determined largely by one of two factors in an operational amplifier. Either the Gain Bandwidth Product or the Slew Rate.

Gain Bandwidth Product sometimes referred to as *FAB*, is equal to the critical frequency multiplied by the voltage gain. Because the frequency critical low is essentially zero, the bandwidth of the operational amplifier is determined by the high critical frequency. The circuit gain and bandwidth have an inverse proportional relationship, as the circuit's gain increases, the frequency response or critical frequency will decrease. The data sheet will typically provide the bandwidth specification at unity gain.

$$GBP = \Delta V \times BW$$

$$GBP = \Delta V \times F_{cHigh}$$

$$F_{cHigh} = \frac{GBP}{\Delta V}$$

The **Slew Rate** and output peak voltage will also impact the bandwidth of the operational amplifier. Both are used in the following formula to determine the critical frequency high.

$$F_{cHigh} = \frac{SlewRate}{2\pi v_p}$$

We now have two formulas representing F_{cHigh} . The actual predicted F_{cHigh} will be the smaller of the two calculated formulas.

$$F_{cHigh} = \frac{GBP}{\Delta V} \text{ OR } F_{cHigh} = \frac{SlewRate}{2\pi v_p} \text{ (The smaller of the two will be } F_{cHigh}!)$$

7.6 Operational Amplifiers Active Integration and Differentiation

7.6.1 Active Integration

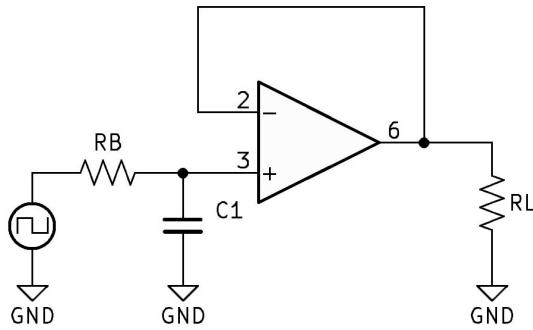


Figure 7.12: Active Integration Circuit

In figure 7.12 the Operational Amplifier is used as a buffer. Connecting the load directly to the integrator would alter the characteristics of the integrator, therefore it is necessary to connect the Op Amp as a buffer to provide circuit isolation between the load and the integrator circuit. Review RC Integration Section 2.11 on page 57.

- Op-Amp is being used as a buffer

7.6.2 Active Integration with Gain

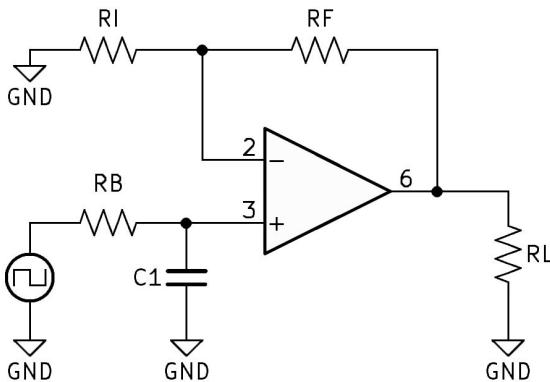


Figure 7.13: Active Integration with Gain Circuit

In addition to circuit isolation (buffer), the Op-Amp can also be used to provide signal gain.

- $\Delta V = \frac{RF}{RI}$

7.6.3 Active Differentiation

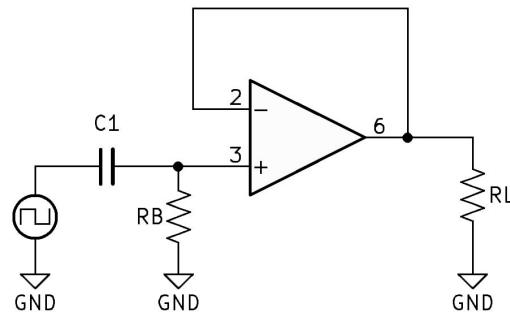


Figure 7.14: Active Differentiation Circuit

In figure 7.14 the Operational Amplifier is used as a buffer. Connecting the load directly to the differentiator would alter the characteristics of the differentiator, therefore it is necessary to connect the Op Amp as a buffer to provide circuit isolation between the load and the differentiator circuit. Review RC Differentiation Section 2.12 on page 61.

- Op-Amp is being used as a buffer

7.6.4 Active Differentiation with Gain

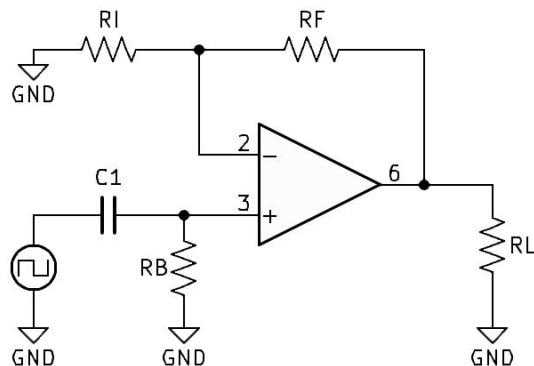


Figure 7.15: Active Differentiation with Gain Circuit

In addition to circuit isolation (buffer), the Op-Amp can also be used to provide signal gain.

- $\Delta V = \frac{RF}{RI}$

7.7 Operational Amplifier Filtering

7.7.1 First Order Active Filtering

Low-Pass Buffer

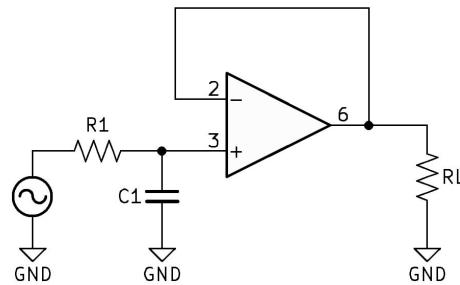


Figure 7.16: First Order Low-Pass Active Filter Buffer Circuit

In figure 7.16 the Operational Amplifier is used as a buffer. Connecting the load directly to the RC filter would alter the characteristics of the filter, therefore it is necessary to connect the Op Amp as a buffer to provide circuit isolation between the load and the filter circuit.

- Op-Amp is being used as a buffer
- Frequency roll-off is $20dB/Decade$

Low-Pass with Gain

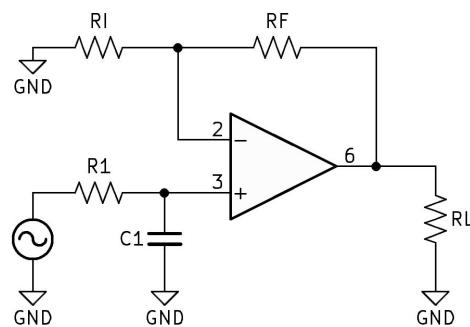


Figure 7.17: First Order Low-Pass Active Filter with Gain Circuit

In figure 7.17 the Operational Amplifier is used to provide circuit isolation and signal gain.

- $\Delta V = \frac{RF}{RI} + 1$
- Frequency roll-off is $20dB/Decade$

High-Pass Buffer

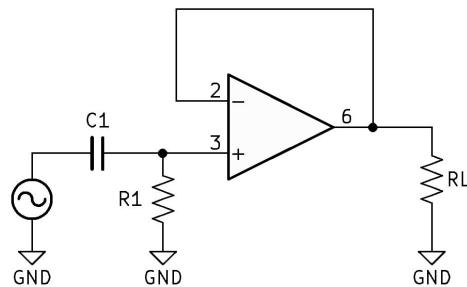


Figure 7.18: First Order High-Pass Active Filter Buffer Circuit

In figure 7.18 the Operational Amplifier is used as a buffer. Connecting the load directly to the RC filter would alter the characteristics of the filter, therefore it is necessary to connect the Op Amp as a buffer to provide circuit isolation between the load and the filter circuit.

- Op-Amp is being used as a buffer
- Frequency roll-off is $20\text{dB}/\text{Decade}$

High-Pass with Gain

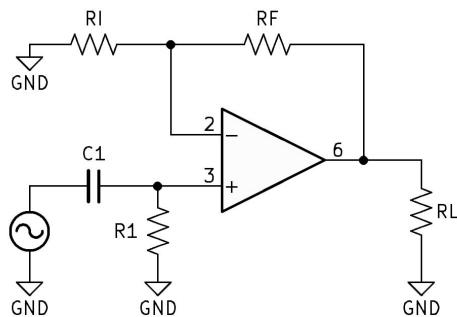


Figure 7.19: First Order High-Pass Active Filter with Gain Circuit

In figure 7.19 the Operational Amplifier is used to provide circuit isolation and signal gain.

- $\Delta V = \frac{RF}{RI} + 1$
- Frequency roll-off is $20\text{dB}/\text{Decade}$

Cascading Band-Pass Filter

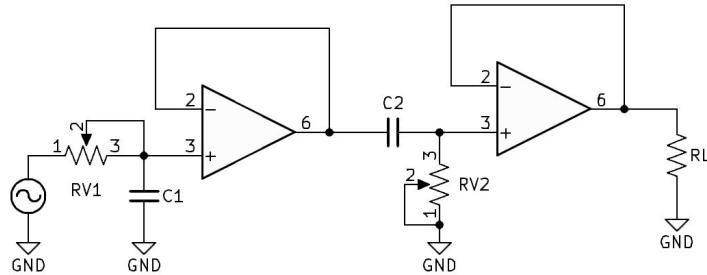


Figure 7.20: First Order Cascaded Band-Pass Active Filter

In figure 7.20 two first-order filters, a Low-Pass and a High-Pass are cascaded together to create a Band-Pass Filter.

- FC_{Low} is determined by RV_1 and C_1
- FC_{High} is determined by RV_2 and C_2
- Frequency roll-off is $20dB/Decade$

Single Stage Band-Pass Filter

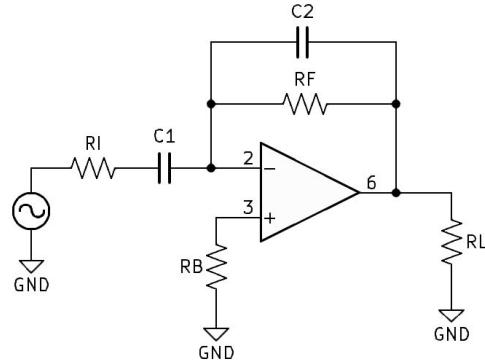


Figure 7.21: First Order Single Stage Band Pass Filter

In figure 7.21 a single-stage Operational amplifier is used to create a first-order band-pass filter.

- FC_{Low} is determined by R_1 and C_1 , $FC_{Low} = \frac{1}{2\pi R_1 C_1}$
- FC_{High} is determined by R_2 and C_2 , $FC_{High} = \frac{1}{2\pi R_2 C_2}$
- Frequency roll-off is $20dB/Decade$

7.7.2 Second Order Active Filtering

Second Order Low-Pass

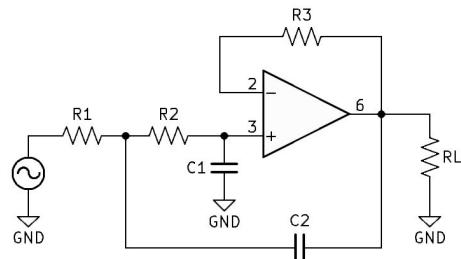


Figure 7.22: Second-Order Low Pass Active Filter

- Op-Amp is used as a buffer and active filtering
- $R1 = R2$
- $C2 = 2 \times C1$
- $FC_{High} = \frac{1}{2\pi\sqrt{R1 \times R2 \times C1 \times C2}}$
- Frequency roll-off is $40dB/Decade$

Second Order High-Pass

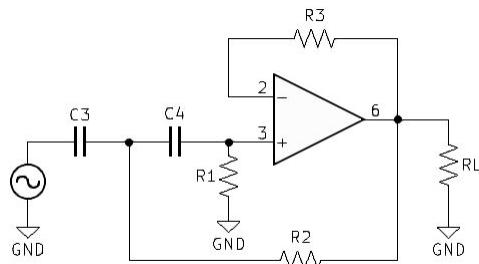


Figure 7.23: Second-Order High Pass Active Filter

- Op-Amp is used as a buffer and active filtering
- $C1 = C2$
- $R1 = 2 \times R2$
- $FC_{High} = \frac{1}{2\pi\sqrt{R1 \times R2 \times C1 \times C2}}$
- Frequency roll-off is $40dB/Decade$

Second-Order Cascading Band-Pass Filter

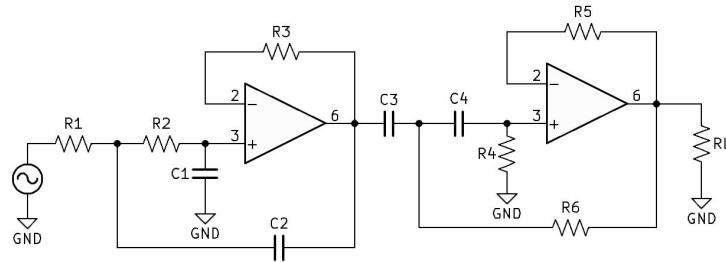


Figure 7.24: Second-Order Cascaded Band Pass Active Filter

- Two Second-Order Cascaded Op-Amp filters (Low-Pass to a High-Pass)
- Frequency roll-off is $40dB/Decade$

Second-Order Single Stage Band-Pass Filter

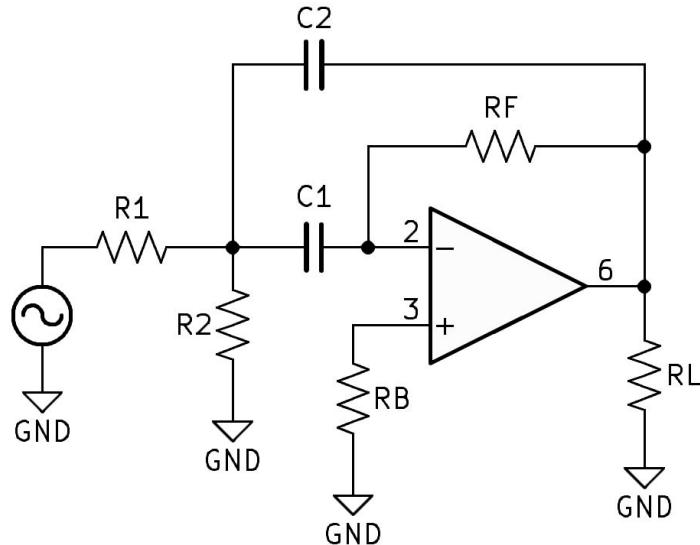
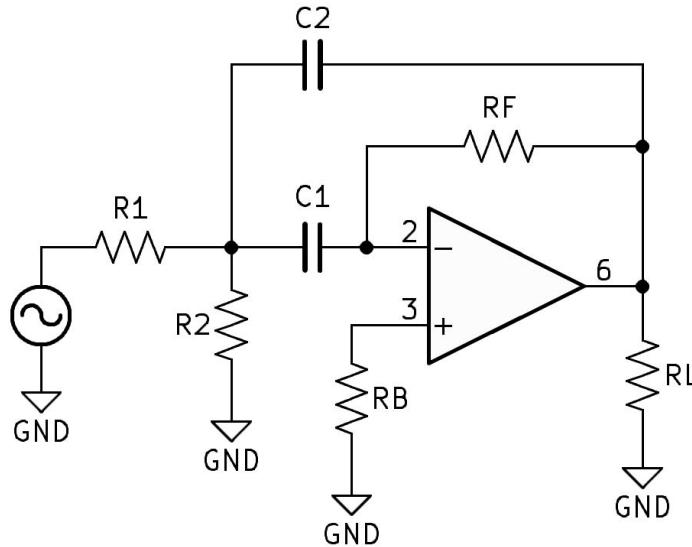


Figure 7.25: Second-Order Single Stage Band Pass Active Filter

- See Design Steps on next page

Second-Order Single Stage Band-Pass Filter Design Steps

**Figure 7.26:** Second-Order Single Stage Band Pass Active Filter

Second-Order Single Stage Band Pass Active Filter Design Steps:

- $Q = \frac{f_R}{BW}$
- Use small caps $\approx 0.001\mu F$

$$C1 = C2$$

- Pick:

Resonant Frequency

Bandwidth

Q^* (Q should be between 1 & 20 to prevent oscillations)

- Pick Δv at f_R *(make $\Delta v < 2Q^2$)

- $R1 = \frac{Q}{2\pi f_R C \Delta v}$

- $R2 = \frac{Q}{2\pi f_R C (2Q^2 - \Delta v)}$

- $RF = \frac{2Q}{2\pi f_R C}$

- $RB = RF$

7.8 Bessel, Butterworth, & Chebyshev Filters

7.8.1 Bessel Filter

- **Named after:** German Mathematician Friedrick Bessel
- **Notable features:** The Bessel filter has the gentlest response of the group. Even though it doesn't have a sharp cutoff, it offers superior phase shift (delay) compared to the other filters in the group. The Bessel filter requires the most stages (i.e. most components); however, it offers excellent characteristics: low sensitivity to component tolerance, superior step response.
- **Best used for:** The Bessel filter is ideal for applications that require minimal phase shift. Due to the gentle frequency response of the Bessel filter, it can only be used in applications where there is adequate space between the passband and stopband. - [Filter Topology Face Off: A closer look at the top 4 filter types \[10\]](#)

7.8.2 Butterworth Filter

- **Named after:** British Physicist Stephen Butterworth
- **Notable features:** The Butterworth filter is commonly referred to as the "maximally flat" option because the passband response offers the steepest roll-off without inducing a passband ripple. In addition to the flat passband response, the selectivity of the Butterworth filter is better than many other filter typologies such as the Bessel or Gaussian. The flip-side of this improved selectivity is greater delay and poorer phase linearity. Butterworth filters offer solid performance considering the number of components needed to implement the filter.
- **Best used for:** Butterworth filters are typically forgiving to part tolerances and values of discrete elements (capacitors, inductors, and resistors). For most bandpass designs, the (Voltage Standing Wave Ratio) VSWR at center frequency is extremely good. - [Filter Topology Face Off: A closer look at the top 4 filter types \[10\]](#)

7.8.3 Chebyshev Filter

- **Named after:** Russian mathematician Pafnuty Chebyshev
- **Notable features:** The Chebyshev filter is known for its ripple response. This ripple response can be designed to be present in the passband (Chebyshev Type 1) or in the stopband (Chebyshev Type 2). The amplitude of the ripple is directly proportional to steepness of the rolloff. That is, if you want a steeper response, you'll see a larger ripple response. These filters offer performance between that of Elliptic function filters and Butterworth

filters. The phase response of the Chebyshev filter is relatively non-linear, which ultimately wreaks havoc on demodulators because it tends to distort pulses because of the non-linear delays. The most common work-around for this phenomena is to increase the bandwidth of the Chebyshev filter to push this non-linear region further out. filter.

- **Best used for:** The Chebyshev filter is the workhorse of the common filter typologies. Its response is easily realised with few components and offers very good selectivity with one of the steepest roll-off responses of the group.

- [Filter Topology Face Off: A closer look at the top 4 filter types \[10\]](#)

7.8.4 Damping Factor

In filter design, the damping factor (ζ) is important for shaping the frequency response, controlling the bandwidth of the filter, and managing the transient response characteristics. For example, in a second-order low-pass filter, the damping factor directly affects the peak response at the cutoff frequency.

- **Overdamped** ($d > 1$) : The system returns to equilibrium without oscillating. It has a slower response but no overshoot.
- **Critically Damped** ($d = 0.707$): The system returns to equilibrium as quickly as possible without oscillating.
- **Underdamped** ($d < 1$): The system will start to oscillate especially as the gain is increased.

Most designs of second order filters are generally named after their inventor with the most common filter types being: Butterworth, Chebyshev, Bessel and Sallen-Key. All these types of filter designs are available as either: low pass filter, high pass filter, band pass filter and band stop (notch) filter configurations, and being second order filters, all have a 40-dB-per-decade roll-off.

In active second-order filters, the damping factor, ζ (zeta), which is the inverse of Q is normally used. Both Q and ζ are independently determined by the gain of the amplifier, A so as Q decreases the damping factor increases. In simple terms, a low pass filter will always be low pass in its nature but can exhibit a resonant peak in the vicinity of the cut-off frequency, that is the gain can increase rapidly due to resonance effects of the amplifiers gain.

Then Q, the quality factor, represents the “peakiness” of this resonance peak, that is its height and narrowness around the cut-off frequency point, f_C . But a filters gain also determines the amount of its feedback and therefore has a significant effect on the frequency response of the filter.

Generally to maintain stability, an active filters gain must not be more than 3.

Then somewhere in between, $\zeta = 0$ and $\zeta = 2.0$, there must be a point where the frequency response is of the correct value, and there is. This is when the filter is “critically damped” and occurs when $\zeta = 0.7071$. - [Second Order Filters\[11\]](#)

7.8.5 Second Order Low-Pass Test Circuit

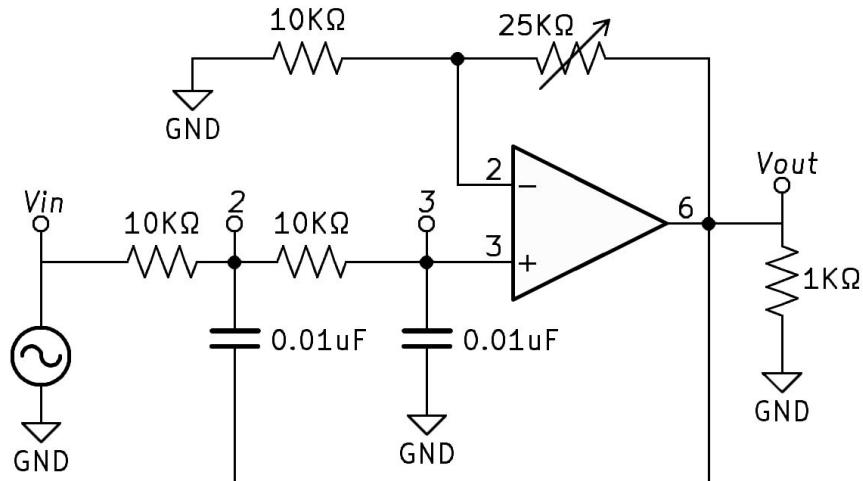


Figure 7.27: Bessel, Butterworth, & Chebyshev Test Circuit

Table 7.1: Bessel, Butterworth, & Chebyshev Test Circuit Data

	Vin	2	3	ζ	RV	ΔV	Vout
Bessel	2vpp	1.414vpp	1vpp	2	0.0Ω	1	1vpp
Bessel	1.73vpp	1.414vpp	1vpp	1.73	2.68KΩ	1.268	1.268vpp
Butterworth	1.414vpp	1.414vpp	1vpp	1.414	5.86KΩ	1.586	1.586vpp
Chebyshev	1vpp	1.414vpp	1vpp	1	10KΩ	2	2vpp
Chebyshev	0.5vpp	1.414vpp	1vpp	0.5	15KΩ	2.5	2.5vpp
Oscillator	0.0vpp	Undetermined		0	$\geq 20K\Omega$	≥ 3	OSC.

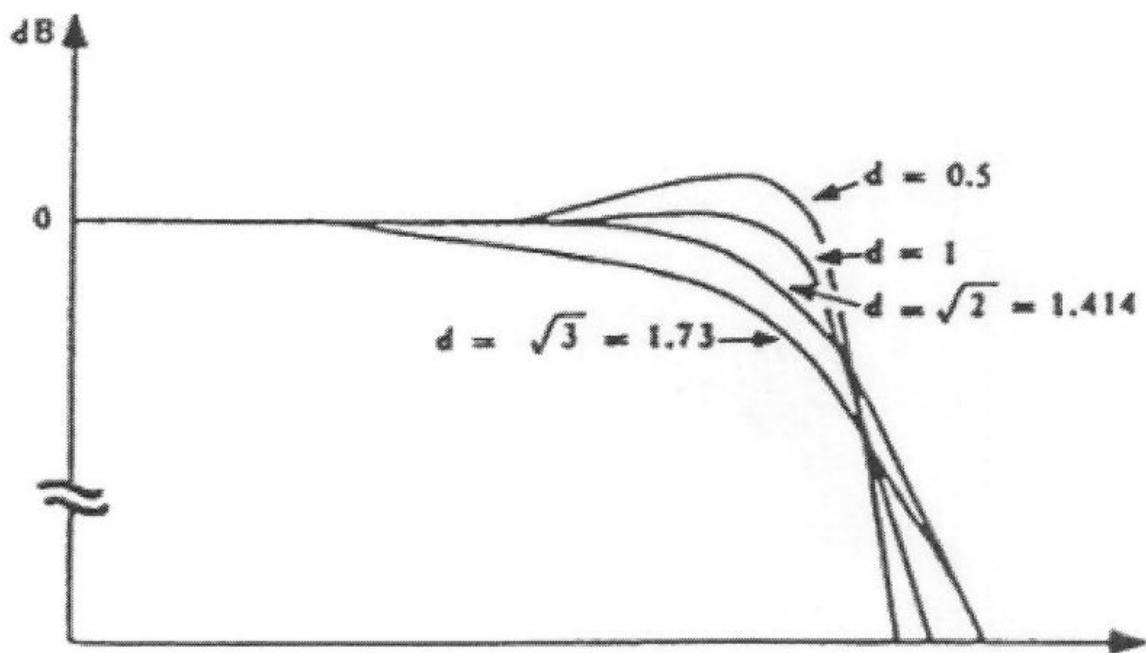
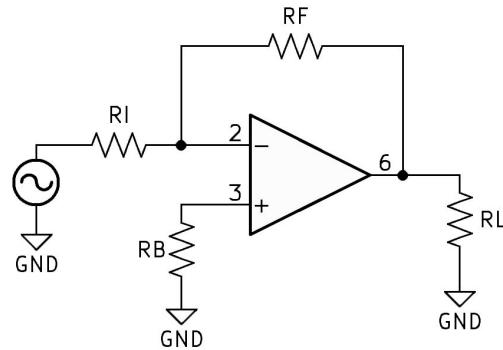


Figure 7.28: Filter Response Curves in terms of Damping, $d = \text{zeta}(\zeta)$

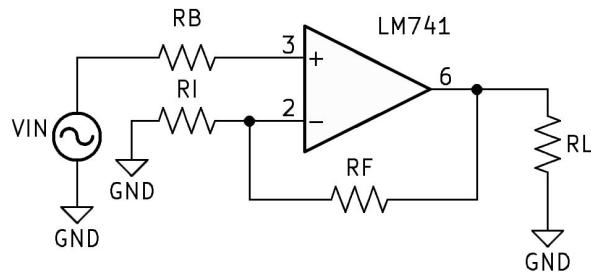
7.9 Operational Amplifier Practice Problems

1. Given: $RF = 10K\Omega$, $RI = 1K\Omega$, Slew Rate = $0.5V/\mu S$, $FAB = 1.5MHz$, & $VIN = 1vp$.
 Find: $Vout$, ΔV , RB , Z_{IN} , Z_{OUT} , and FC_{High} .



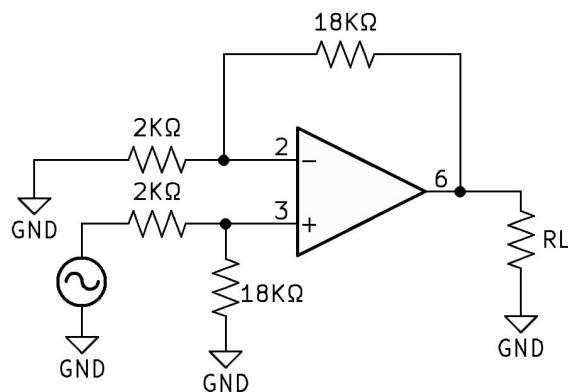
$Vout =$	$\Delta V =$	$RB =$
$Z_{IN} =$	$Z_{OUT} =$	$FC_{High} =$

2. Given: $RF = 10K\Omega$, $RI = 1K\Omega$, Slew Rate = $0.5V/\mu S$, $FAB = 1.5MHz$, & $VIN = 1vp$.
 Find: $Vout$, ΔV , RB , Z_{IN} , Z_{OUT} , and FC_{High} .



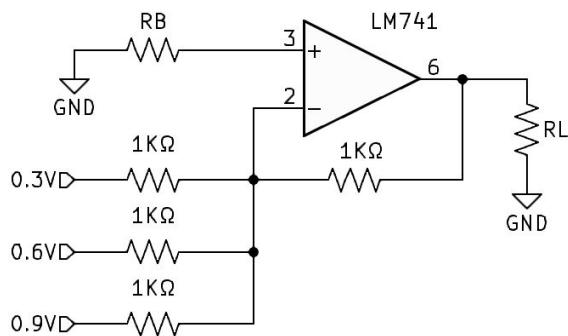
$Vout =$	$\Delta V =$	$RB =$
$Z_{IN} =$	$Z_{OUT} =$	$FC_{High} =$

3. Given: $V_{IN} = 250\text{mV}$.
 Find: V_{out} and ΔV .



$V_{out} =$	$\Delta V =$
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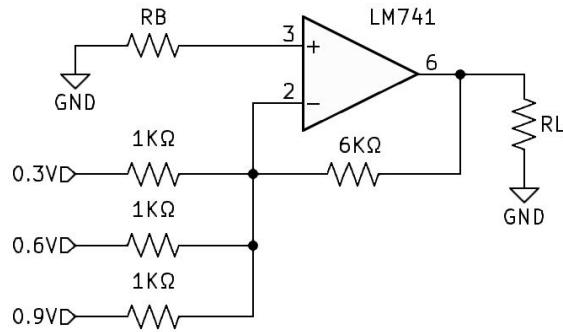
4. Given: See Circuit Schematic
 Find: V_{out} and R_B .



$V_{out} =$	$RB =$
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5. Given: See Circuit Schematic

Find: V_{out} and R_B .

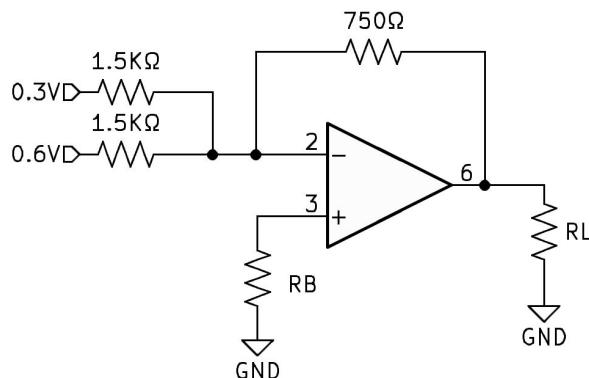


$$V_{out} =$$

$$RB =$$

6. Given: See Circuit Schematic

Find: V_{out} and R_B .

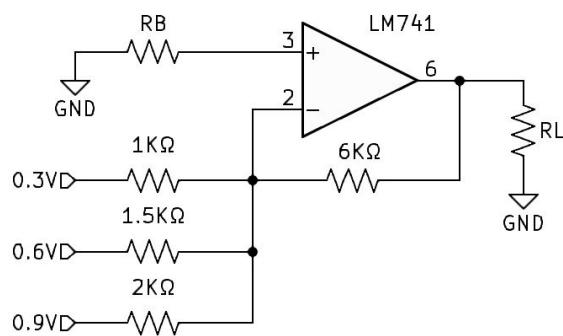


$$V_{out} =$$

$$RB =$$

7. Given: See Circuit Schematic

Find: V_{out} and R_B .

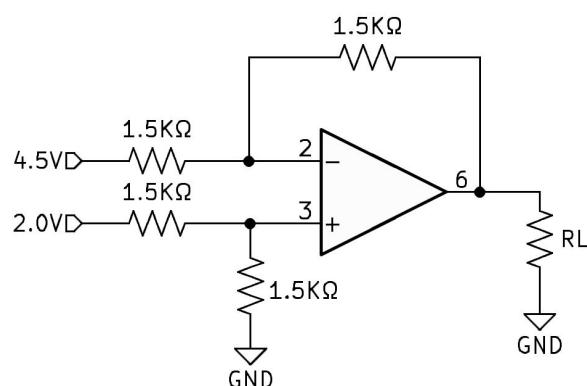


$$V_{out} =$$

$$R_B =$$

8. Given: See Circuit Schematic

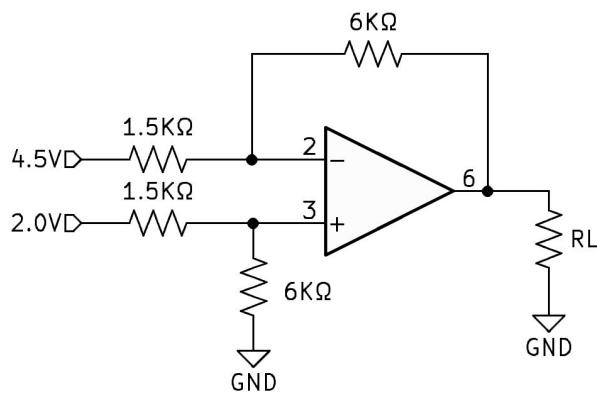
Find: V_{out} .



$$V_{out} =$$

9. Given: See Circuit Schematic

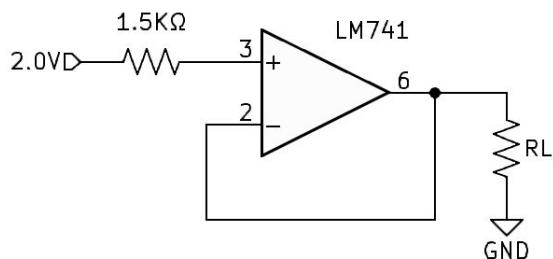
Find: V_{out} .



$$V_{out} =$$

10. Given: See Circuit Schematic

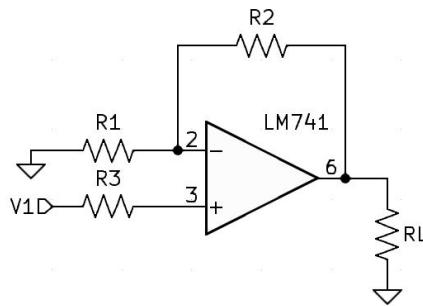
Find: V_{out} .



$$V_{out} =$$

11. Given: $V_{Supply} = \pm 15V$, $Z_{inDev} = 2M\Omega$, $Z_{outDev} = 75\Omega$, $SlewRate = 1.5V/\mu S$, $GBWP = 1.5MHz$, $R1 = 1K\Omega$, $R2 = 10K\Omega$, & $V1 = 600mV$

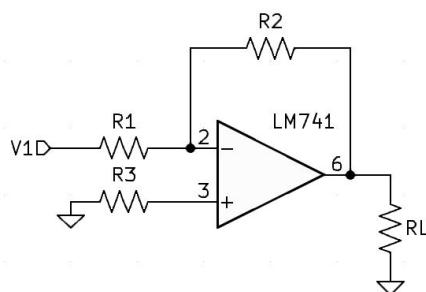
Find: $R3$, V_{RL} , ΔV , Z_{IN} , Z_{OUT} , & FC_{High}



$R3 =$	$V_{RL} =$	$\Delta V =$
$Z_{IN} =$	$Z_{OUT} =$	$FC_{High} =$

12. Given: $V_{Supply} = \pm 25V$, $Z_{inDev} = 2.5M\Omega$, $Z_{outDev} = 65\Omega$, $SlewRate = 0.5V/\mu S$, $GBWP = 1.0MHz$, $R1 = 4.5K\Omega$, $R2 = 7.4K\Omega$, & $V1 = 10V$

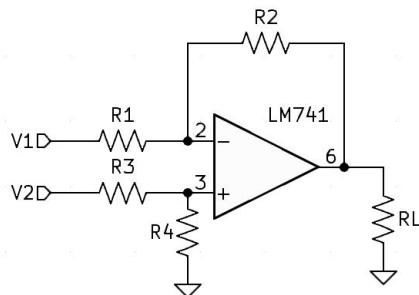
Find: $R3$, V_{RL} , ΔV , Z_{IN} , Z_{OUT} , & FC_{High}



$R3 =$	$V_{RL} =$	$\Delta V =$
$Z_{IN} =$	$Z_{OUT} =$	$FC_{High} =$

13. Given: $V_{Supply} = \pm 15V$, $R1 = 420\Omega$, $R2 = 4.2K\Omega$, $R3 = 420\Omega$, $R4 = 4.2K\Omega$, $V1 = 200mV$, & $V2 = 500mV$

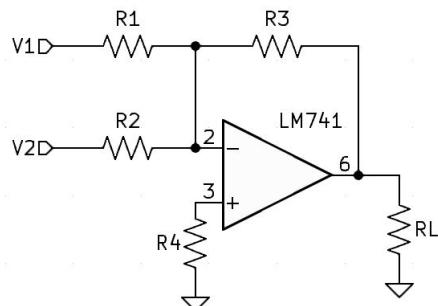
Find: V_{RL}



$$V_{RL} =$$

14. Given: $V_{Supply} = \pm 15V$, $R1 = 1K\Omega$, $R2 = 1K\Omega$, $R3 = 1K\Omega$, $V1 = 4V$, & $V2 = 4V$

Find: V_{RL} & $R4$

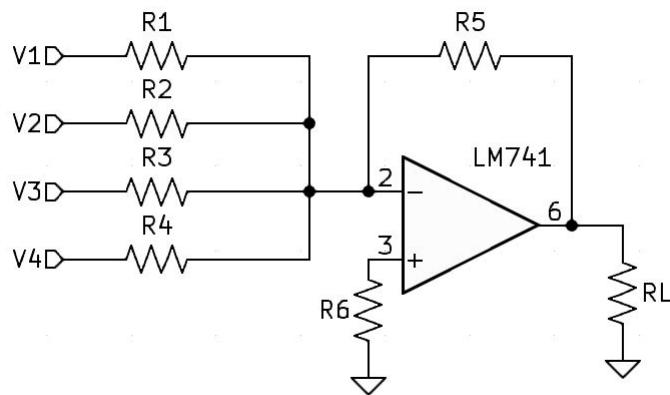


$$V_{RL} =$$

$$R4 =$$

15. Given: $V_{Supply} = \pm 18V$, $R1 = 50K\Omega$, $R2 = 25K\Omega$, $R3 = 12.5K\Omega$, $R4 = 6.25K\Omega$, $R5 = 10K\Omega$, & $V1, V2, V3$, & $V4 = 5V$

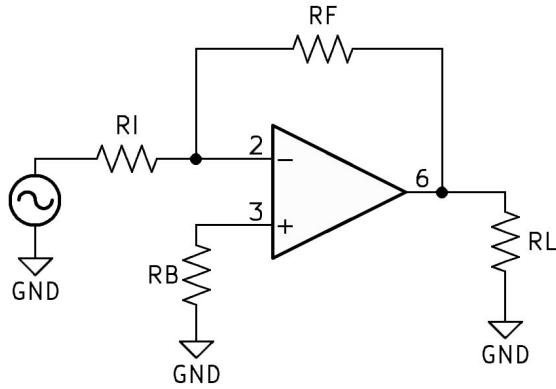
Find: V_{RL} & $R6$



$V_{RL} =$	$R6 =$
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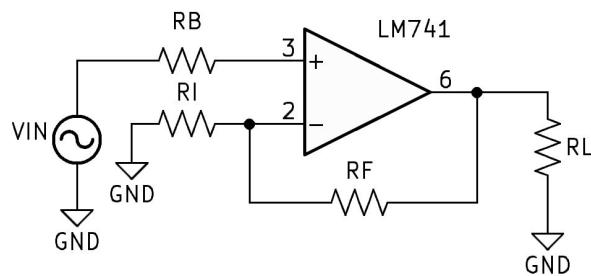
7.10 Operational Amplifier Practice Problem Answers

1. Given: $RF = 10K\Omega$, $RI = 1K\Omega$, Slew Rate = $0.5V/\mu S$, $FAB = 1.5MHz$, & $VIN = 1vp$.
 Find: $Vout$, ΔV , RB , Z_{IN} , Z_{OUT} , and FC_{High} .



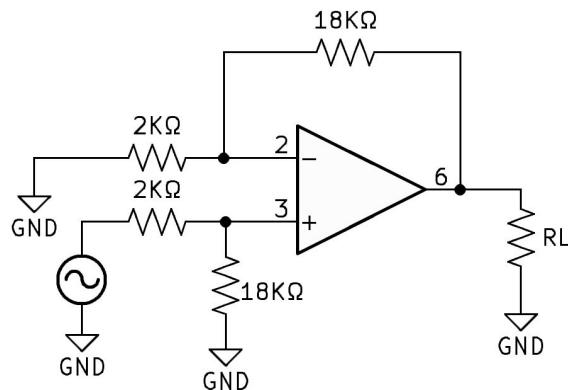
$Vout = 10v_P$	$\Delta V = -10$	$RB = 909.1\Omega$
$Z_{IN} = 1K\Omega$	$Z_{OUT} = 4.125m\Omega$	$FC_{High} = 7.958Khz$

2. Given: $RF = 10K\Omega$, $RI = 1K\Omega$, Slew Rate = $0.5V/\mu S$, $FAB = 1.5MHz$, & $VIN = 1vp$.
 Find: $Vout$, ΔV , RB , Z_{IN} , Z_{OUT} , and FC_{High} .



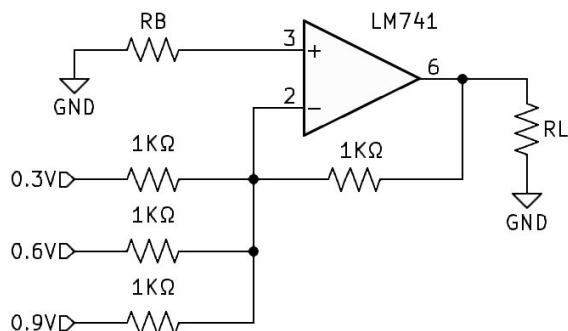
$Vout = 11v_P$	$\Delta V = 11$	$RB = 909.1\Omega$
$Z_{IN} = 36.364 \times 10^9 \Omega$	$Z_{OUT} = 4.125m\Omega$	$FC_{High} = 7.958Khz$

3. Given: $V_{IN} = 250\text{mV}$.
 Find: V_{out} and ΔV .



$V_{out} = 2.25\text{v}_P$	$\Delta V = 9$
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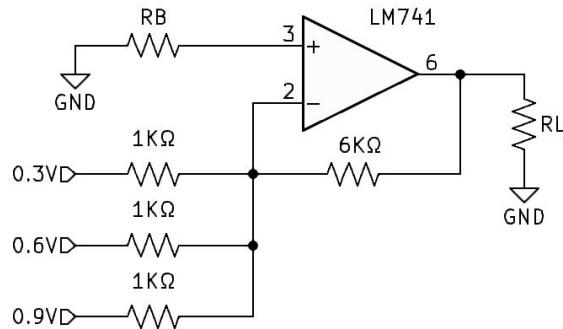
4. Given: See Circuit Schematic
 Find: V_{out} and R_B .



$V_{out} = -1.8V$	$RB = 250\Omega$
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5. Given: See Circuit Schematic

Find: V_{out} and RB .

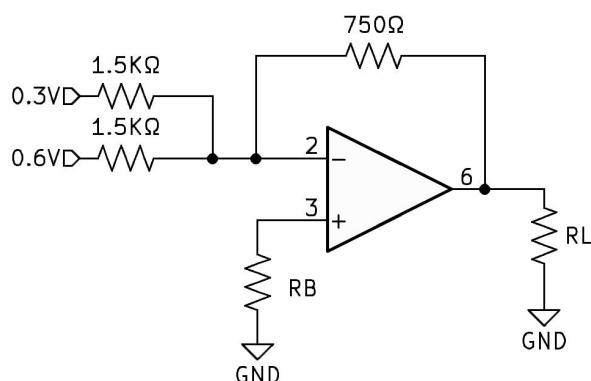


$$V_{out} = -10.8V$$

$$RB = 316.8\Omega$$

6. Given: See Circuit Schematic

Find: V_{out} and RB .

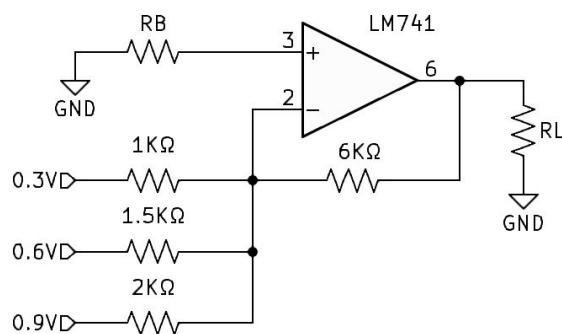


$$V_{out} = -450mV$$

$$RB = 375\Omega$$

7. Given: See Circuit Schematic

Find: V_{out} and R_B .

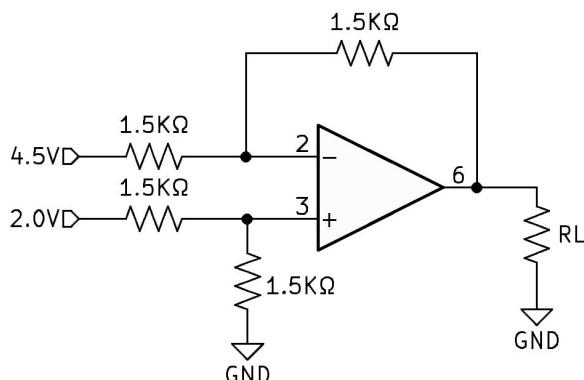


$$V_{out} = -6.9V$$

$$RB = 429\Omega$$

8. Given: See Circuit Schematic

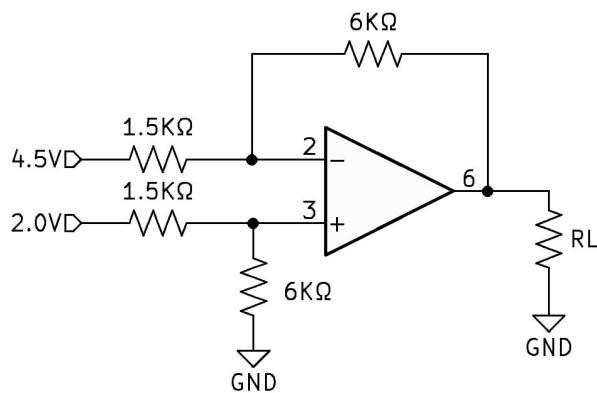
Find: V_{out} .



$$V_{out} = -2.5V$$

9. Given: See Circuit Schematic

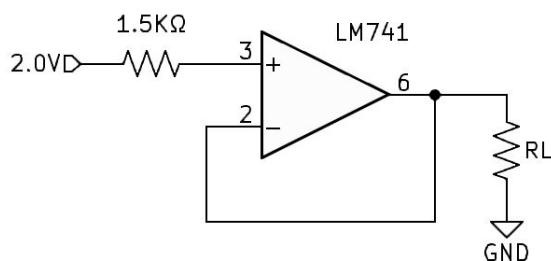
Find: V_{out} .



$$V_{out} = -10V$$

10. Given: See Circuit Schematic

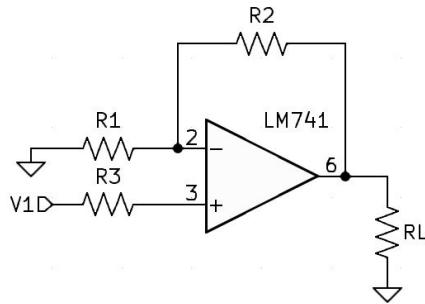
Find: V_{out} .



$$V_{out} = 2V$$

11. Given: $V_{Supply} = \pm 15V$, $Z_{inDev} = 2M\Omega$, $Z_{outDev} = 75\Omega$, $SlewRate = 1.5V/\mu S$, $GBWP = 1.5MHz$, $R1 = 1K\Omega$, $R2 = 10K\Omega$, & $V1 = 600mV$

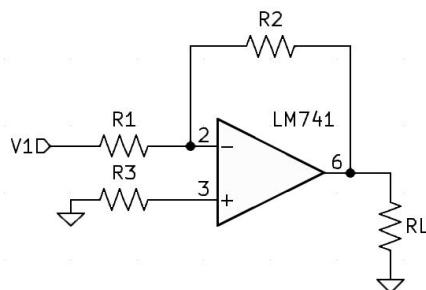
Find: $R3$, V_{RL} , ΔV , Z_{IN} , Z_{OUT} , & FC_{High}



$R3 = 909.9\Omega$	$V_{RL} = 6.6V$	$\Delta V = 11$
$Z_{IN} = 36.189G\Omega$	$Z_{OUT} = 4.125m\Omega$	$FC_{High} = 36.173KHz$

12. Given: $V_{Supply} = \pm 25V$, $Z_{inDev} = 2.5M\Omega$, $Z_{outDev} = 65\Omega$, $SlewRate = 0.5V/\mu S$, $GBWP = 1.0MHz$, $R1 = 4.5K\Omega$, $R2 = 7.4K\Omega$, & $V1 = 10V$

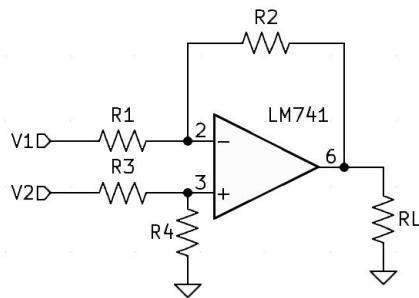
Find: $R3$, V_{RL} , ΔV , Z_{IN} , Z_{OUT} , & FC_{High}



$R3 = 2.798K\Omega$	$V_{RL} = -16.444V$	$\Delta V = -1.644$
$Z_{IN} = 4.5K\Omega$	$Z_{OUT} = 859.433\mu\Omega$	$FC_{High} = 4.839KHz$

13. Given: $V_{Supply} = \pm 15V$, $R1 = 420\Omega$, $R2 = 4.2K\Omega$, $R3 = 420\Omega$, $R4 = 4.2K\Omega$, $V1 = 200mV$, & $V2 = 500mV$

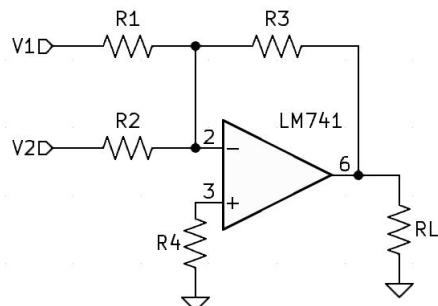
Find: V_{RL}



$V_{RL} = 3V$

14. Given: $V_{Supply} = \pm 15V$, $R1 = 1K\Omega$, $R2 = 1K\Omega$, $R3 = 1K\Omega$, $V1 = 4V$, & $V2 = 4V$

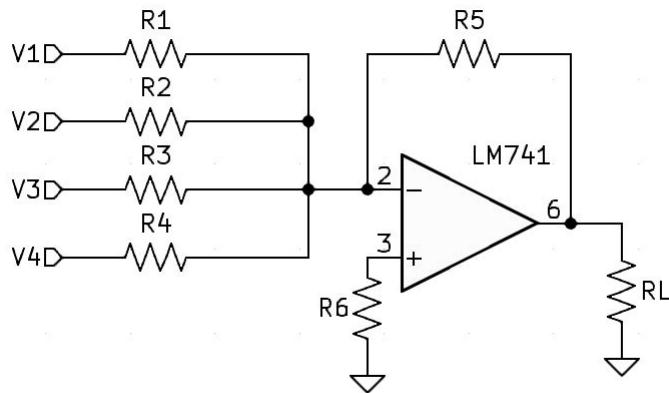
Find: V_{RL} & $R4$



$V_{RL} = -8V$	$R4 = 333.333\Omega$
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15. Given: $V_{Supply} = \pm 18V$, $R1 = 50K\Omega$, $R2 = 25K\Omega$, $R3 = 12.5K\Omega$, $R4 = 6.25K\Omega$, $R5 = 10K\Omega$, & $V1, V2, V3$, & $V4 = 5V$

Find: V_{RL} & $R6$



$$V_{RL} = -15V$$

$$R6 = 2.5K\Omega$$

Chapter 8

Digital to Analog & Analog to Digital Conversions

8.1 Objectives

8.1.1 Digital to Analog Conversion Objectives

Knowledge Objectives

1. **Understand DAC Fundamentals:** Explain the basic principles of digital-to-analog conversion, including key concepts such as resolution, sampling rate, and quantization.
2. **Types of DACs:** Describe the different types of DACs (e.g., R-2R ladder & binary-weighted) and their operating principles.
3. **DAC Specifications:** DAC Specifications: Understand and interpret specifications of DACs, including linearity, and settling time.

Design Objectives

1. **Design a Simple DAC Circuit:** Design and implement a basic DAC circuit using common components.
2. **Component Selection:** Select appropriate components for DAC circuits based on application requirements, such as resolution and speed.
3. **Circuit Pre-Calculations:** Use calculations to model DAC behavior and predict performance characteristics and output waveforms.

Troubleshooting Objectives

1. **Identify Common Issues:** Identify and diagnose common issues in DAC circuits, such as non-linearity, glitches, and noise.

2. **Testing and Measurement:** Use oscilloscopes, signal generators, and other test equipment to measure and analyze DAC output signals.
3. **Performance Optimization:** Implement techniques to optimize DAC performance, including filtering and error correction methods.

8.1.2 Analog to Digital Conversion Objectives

Knowledge Objectives

1. **Understand ADC Fundamentals:** Explain the basic principles of analog-to-digital conversion, including key concepts such as sampling theorem, Nyquist rate, and aliasing.
2. **Types of ADCs:** Describe the different types of ADCs (e.g., flash, successive approximation, delta-sigma) and their operating principles.
3. **ADC Specifications:** Understand and interpret specifications of ADCs, including resolution, signal-to-noise ratio (SNR), and effective number of bits (ENOB).

Design Objectives

1. **Design a Simple ADC Circuit:** Design and implement a basic ADC circuit using common components.
2. **Component Selection:** Select appropriate components for ADC circuits based on application requirements, such as sample rate.
3. **Circuit Pre-Calculations:** Use calculations to model ADC behavior and predict performance characteristics.

Troubleshooting Objectives

1. **Identify Common Issues:** Identify and diagnose common issues in ADC circuits, such as quantization noise, jitter, and distortion.
2. **Testing and Measurement:** Use oscilloscopes, signal generators, and other test equipment to measure and analyze ADC input signals and conversion accuracy.
3. **Performance Optimization:** Implement techniques to optimize ADC performance, including proper grounding, shielding, and anti-aliasing filtering.

8.1.3 Integrated Objectives

Practical Applications

1. **Real-world Applications:** Discuss and analyze real-world applications of DACs and ADCs in systems such as audio processing, instrumentation, and communication systems.
2. **Integration in Systems:** Understand the integration of DACs and ADCs within larger systems, including interfacing with microcontrollers and digital signal processors (DSPs).

Project-Based Learning

1. **Lab Project:** Design, implement, and troubleshoot a complete system that incorporates both DAC and ADC circuits, demonstrating an understanding of both digital-to-analog and analog-to-digital conversion processes.

8.2 Key Terms

Acquisition	Acquisition refers to the process of capturing and converting an analog signal into a digital form so it can be processed, analyzed, or stored by digital systems.
ADC	Analog-to-Digital Converter. This conversion is crucial in digital electronics because most modern electronic devices process and store data in digital form.
ADC Resolution	The resolution of an ADC is the number of distinct digital output values it can produce for a given analog input range. It is usually specified in bits. An n -bit ADC can represent 2^n discrete levels. For example, a 10-bit ADC can represent $2^{10} = 1024$ distinct levels.
	If an ADC has a 10-bit resolution and an input voltage range of 0 to 5 volts, each digital step represents $\frac{5V}{1024} \approx 4.88mV/step$.
Aliasing	Aliasing occurs when a signal is sampled at a rate that is too low to capture its variations accurately, leading to distortion and loss of information.
Anti-Aliasing Filter	A low-pass filter, applied to the analog signal before sampling, that removes frequency components higher than half the sampling rate. This ensures that the sampled signal accurately represents the original signal without high-frequency components that could cause aliasing.

DAC

Digital-to-Analog Converter. A DAC is a device that converts a digital signal, which is a discrete signal represented by binary numbers, into an analog signal, which is a continuous signal. This conversion is essential in various applications where digital data needs to be converted back into a form that can be perceived by human senses or processed by analog systems.

DAC Resolution

The resolution of a DAC is the number of discrete output levels it can produce from a given range of digital input values. It is also specified in bits.

An n -bit DAC can produce 2^n discrete output levels. For example, a 8-bit DAC can represent $2^8 = 256$ distinct levels.

If a DAC has an 8-bit resolution and an output voltage range of 0 to 10 volts, each step corresponds to $\frac{10V}{256} \approx 39.06mV/step$.

Delta-Sigma ADC

The Delta-Sigma ADC offers high-resolution performance while providing high stability. -[Texas Instruments \[12\]](#)

Encoding

The process of converting the quantized values into a binary code that can be processed by digital systems.

Filtering

Smoothing out the step-like output of the DAC to produce a more natural analog signal, often using a low-pass filter.

Latency

Latency refers to the time delay between the application of an analog input signal and the availability of the corresponding digital output. This delay encompasses all the internal processes of the ADC, including sampling, conversion, and any additional processing stages.

Nyquist theorem

also known as the Nyquist-Shannon sampling theorem, is a fundamental principle in the field of digital signal processing. It provides a criterion for the minimum sampling rate required to accurately capture and reconstruct a continuous signal from its samples without introducing aliasing.

Mathematical Expression: If f_{max} is the highest frequency component of the signal, the sampling rate f_s must satisfy:

$$f_s \geq 2 \times f_{max}$$

Pipeline ADC

Also known as subranging quantizers, pipeline ADCs consist of numerous consecutive stages, each containing a track/hold (T/H), a low-resolution ADC and DAC, and a summing circuit that includes an interstage amplifier to provide gain. -[Maxim Integrated \[12\]](#)

Quantization	The process of mapping the sampled values to a finite set of levels, which are represented by binary numbers.
Reconstruction	The process of converting discrete digital values into a continuous analog waveform.
Sampling	The process of measuring the amplitude of an analog signal at regular intervals is known as the sampling rate.
SAR ADC	The success of approximation register converter, or SAR ADC, is often considered the backbone of general-purpose mixed-signal circuits and is used in many data acquisition applications, including control loops, power monitoring, and low-to-medium frequency analysis. -Texas Instruments [12]
Settling time	in electronics refers to the time required for a circuit or system to reach a stable state after a perturbation, such as a change in input signal or conditions. It is particularly important in analog and digital systems where signals need to stabilize to ensure accurate and reliable operation.

8.3 Digital to Analog Conversion

8.3.1 Binary Weighted DAC

Binary weighted digital-to-analog converters are a type of data converter that converts a digital binary number into an equivalent analog output signal proportional to the value of the digital number - [Electronics Tutorials \[13\]](#)

8.3.2 BCD Binary Weighted DAC Design

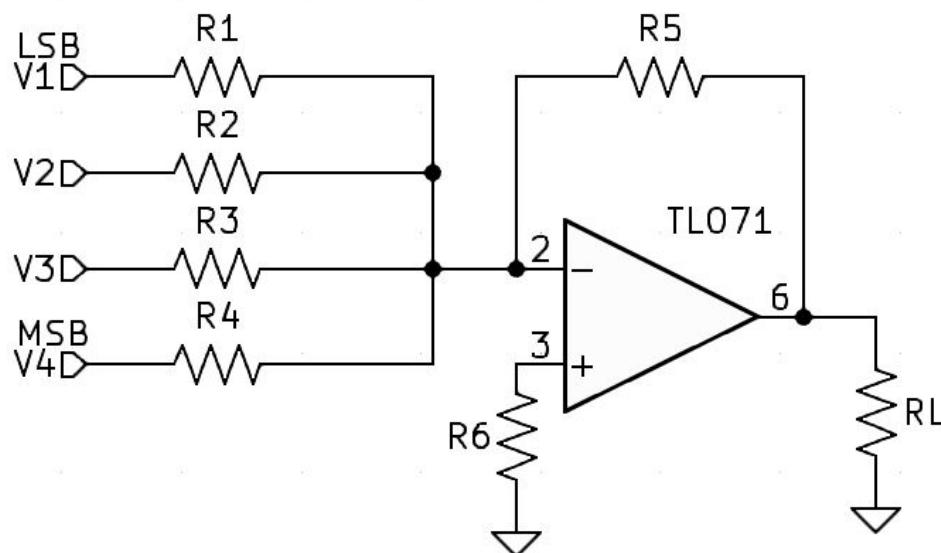


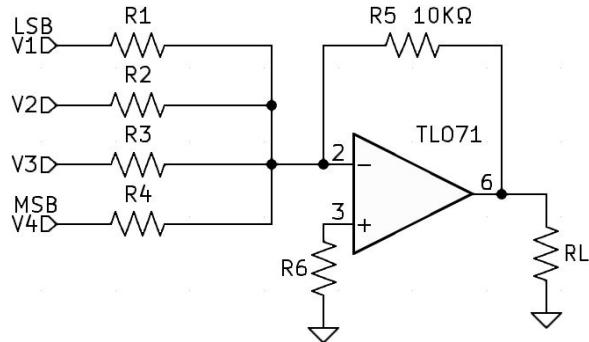
Figure 8.1: Binary Weighted Digital to Analog Converter

Table 8.1: Binary Weighted DAC Data

Digital				Analog
(MSB) 2^3	2^2	2^1	(LSB) 2^0	V_{RL}
0	0	0	0	0V
0	0	0	1	-1V
0	0	1	0	-2V
0	0	1	1	-3V
0	1	0	0	-4V
0	1	0	1	-5V
0	1	1	0	-6V
0	1	1	1	-7V
1	0	0	0	-8V
1	0	0	1	-9V

Steps:

1. See figure 8.1: Binary Weighted Digital to Analog Converter and choose a feedback resistor. For this example we will use $10K\Omega$.



2. Calculate R1:

Imagine the binary input is set to 0001_2 , the desired output will be $-1V$.

- (a) Find V_{R5} : Because the V+ Pin3 is at 0V, V- Pin 2 will also be at 0V (with feedback). This means that $V_{R5} = 1V$ with polarities left to right equal to + -.
- (b) Calculate I_{R5} :
 - $I_{R5} = \frac{V_{R5}}{R5} = \frac{1V}{10K\Omega} = 100\mu A$
- (c) Determine V1: A TTL high will be approximately 5V.
- (d) Determine V_{R1} : $V_{R1} = V1 = 5V$
- (e) Determine I_{R1} : $I_{R1} = I_{R5} = 100\mu A$
- (f) Calculate $R1$: $R1 = \frac{V_{R1}}{I_{R1}} = \frac{5V}{100\mu A} = 50K\Omega$

3. Calculate R2:

Imagine the binary input is set to 0010_2 , the desired output will be $-2V$.

- (a) Find V_{R5} : Because the V+ Pin3 is at 0V, V- Pin 2 will also be at 0V (with feedback). This means that $V_{R5} = 2V$ with polarities left to right equal to + -.
- (b) Calculate I_{R5} :
 - $I_{R5} = \frac{V_{R5}}{R5} = \frac{2V}{10K\Omega} = 200\mu A$
- (c) Determine V2: A TTL high will be approximately 5V.
- (d) Determine V_{R2} : $V_{R2} = V2 = 5V$
- (e) Determine I_{R2} : $I_{R2} = I_{R5} = 200\mu A$
- (f) Calculate $R2$: $R2 = \frac{V_{R2}}{I_{R2}} = \frac{5V}{200\mu A} = 25K\Omega$

4. Calculate R3:

Imagine the binary input is set to 0100_2 , the desired output will be $-4V$.

(a) Find V_{R5} : Because the V+ Pin3 is at 0V, V- Pin 2 will also be at 0V (with feedback). This means that $V_{R5} = 4V$ with polarities left to right equal to + -.

(b) Calculate I_{R5} :

$$\bullet I_{R5} = \frac{V_{R5}}{R5} = \frac{4V}{10K\Omega} = 400\mu A$$

(c) Determine V3: A TTL high will be approximately 5V.

(d) Determine V_{R3} : $V_{R3} = V3 = 5V$

(e) Determine I_{R3} : $I_{R3} = I_{R5} = 400\mu A$

$$(f) \text{ Calculate } R3: R3 = \frac{V_{R3}}{I_{R3}} = \frac{5V}{400\mu A} = 12.5K\Omega$$

5. Calculate R4:

Imagine the binary input is set to 1000_2 , the desired output will be $-8V$.

(a) Find V_{R5} : Because the V+ Pin3 is at 0V, V- Pin 2 will also be at 0V (with feedback). This means that $V_{R5} = 8V$ with polarities left to right equal to + -.

(b) Calculate I_{R5} :

$$\bullet I_{R5} = \frac{V_{R5}}{R5} = \frac{8V}{10K\Omega} = 800\mu A$$

(c) Determine V4: A TTL high will be approximately 5V.

(d) Determine V_{R4} : $V_{R4} = V4 = 5V$

(e) Determine I_{R4} : $I_{R4} = I_{R5} = 800\mu A$

$$(f) \text{ Calculate } R4: R4 = \frac{V_{R4}}{I_{R4}} = \frac{5V}{800\mu A} = 6.25K\Omega$$

6. Calculate R6:

$$(a) R6 = \frac{1}{\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3} + \frac{1}{R4} + \frac{1}{R5}} = \frac{1}{\frac{1}{50K\Omega} + \frac{1}{25K\Omega} + \frac{1}{12.5K\Omega} + \frac{1}{6.25K\Omega} + \frac{1}{10K\Omega}}$$

$$(b) R6 = 2.5K\Omega$$

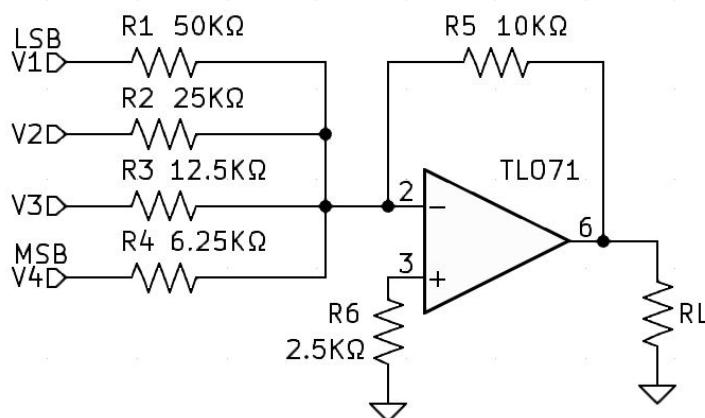


Figure 8.2: Designed Binary Weighted Digital to Analog Converter

8.3.3 R-2R DAC

R-2R Digital-to-Analogue Converter, or DAC, is a data converter which use two precision resistor to convert a digital binary number into an analogue output signal proportional to the value of the digital number - [Electronics Tutorials \[14\]](#)

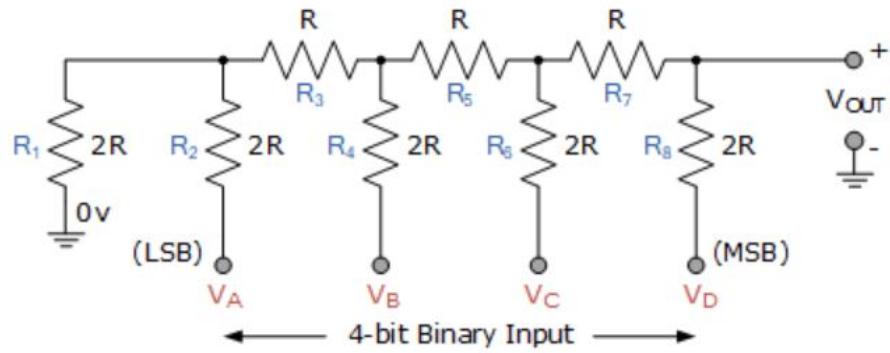


Figure 8.3: R-2R Digital to Analog Converter [14]

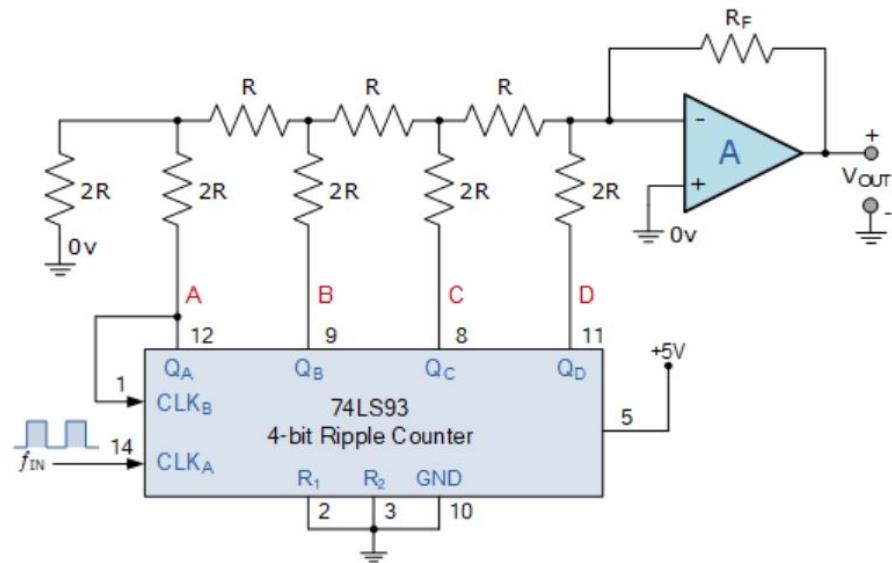


Figure 8.4: R-2R Digital to Analog Converter with 4-Bit Counter [14]

8.3.4 DAC0808

The DAC0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with $\pm 5V$ supplies. No reference current (IREF) trimming is required for most applications since the full scale output current is typically ± 1 LSB of 255 IREF/256. Relative accuracies of better than $\pm 0.19\%$ assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $IREF \geq 2$ mA. The power supply currents of the DAC0808 are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range. The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

- [DAC0808 Data Sheet \[14\]](#)

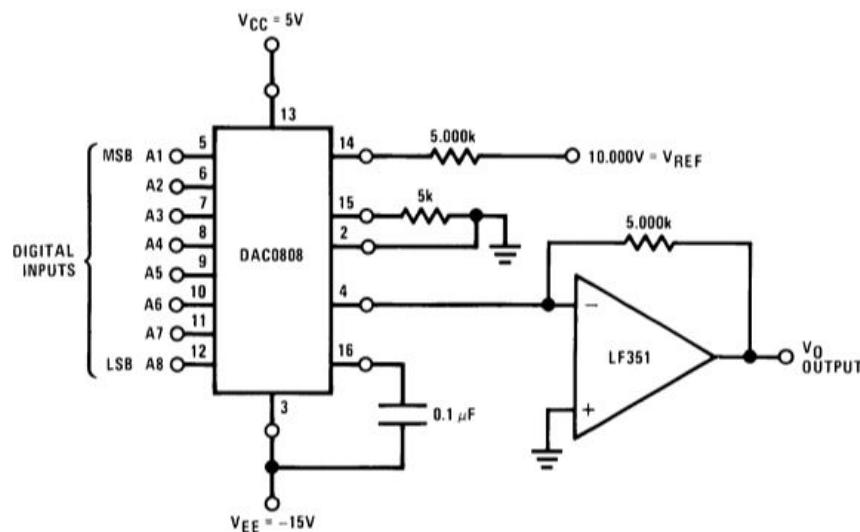


Figure 8.5: DAC0808 Typical Application [15]

8.4 Analog to Digital Conversion

8.4.1 Flash ADC (Direct Conversion ADC)

- **Principle:** Uses a bank of comparators, each one comparing the input signal to a unique reference voltage.
- **Advantages:** Very fast, as conversion happens in a single step.
- **Disadvantages:** Requires a large number of comparators, leading to high power consumption and complexity, especially for high resolutions.
- **Applications:** High-speed applications like digital oscilloscopes, radar, and high-speed data acquisition.

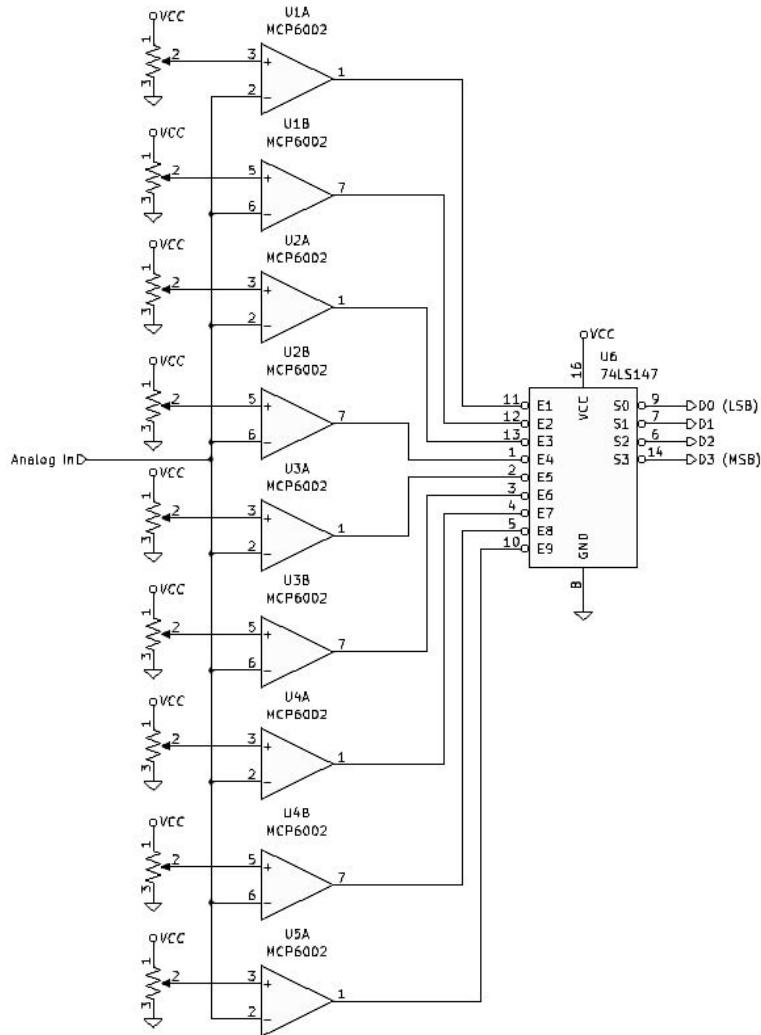


Figure 8.6: ADC Flash (Direct Conversion) 4-Bit

8.4.2 Additional Resources

- Flash ADC [16]
- Choosing the best ADC architecture [12]
- SAR and Delta-Sigma: Basic operation [17]
- Pipeline ADCs Come of Age [18]

8.5 DAC to ADC Circuit Integration

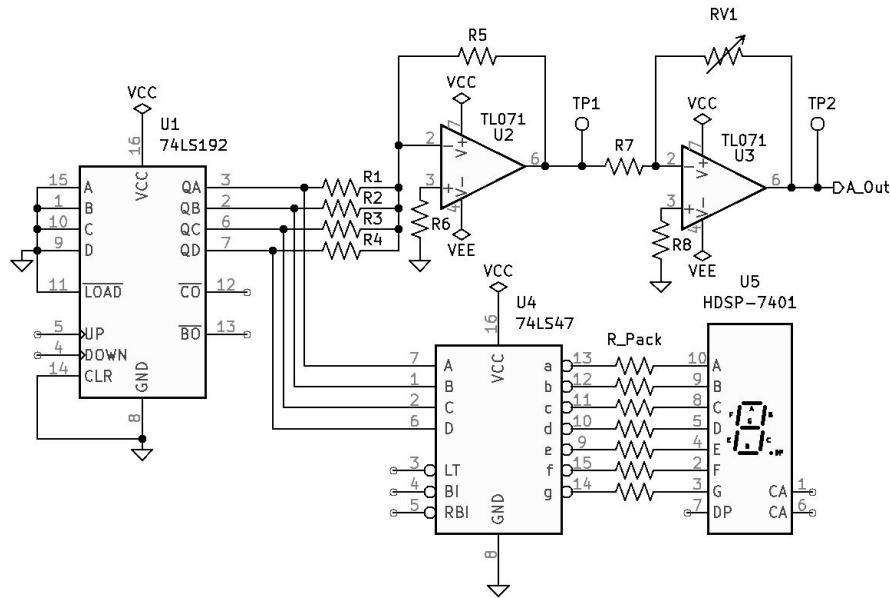


Figure 8.7: Design Test Circuit 1

Assignment:

1. Identify each IC used in Figure 8.7 Design Test Circuit 1 and include the following.
 - Part Description
 - Key Features
 - Key Applications
 - Important Specifications
2. Analyze the circuit and determine the overall function.
3. Verify that all wiring is correct.
4. Calculate the appropriate resistor values and the resistor current, voltage, and power.

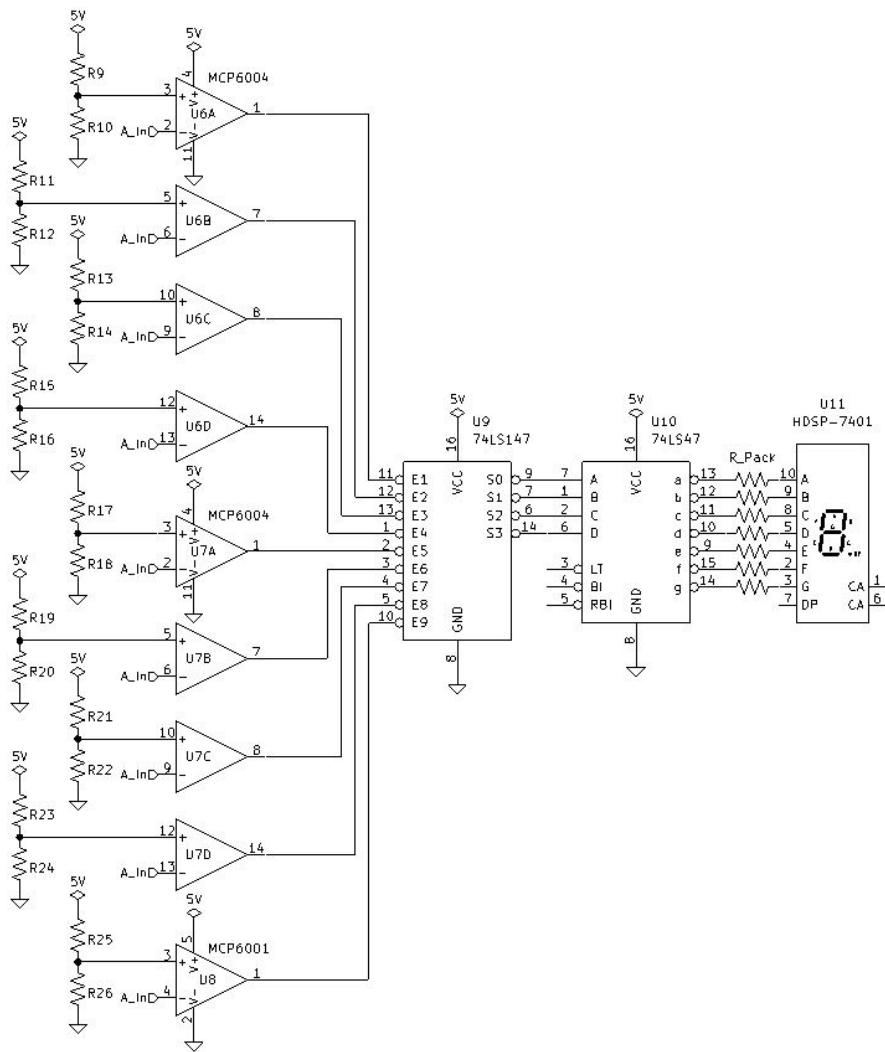


Figure 8.8: Design Test Circuit 2

Assignment:

1. Identify each IC used in Figure 8.8 Design Test Circuit 2 and include the following.
 - Part Description
 - Key Features
 - Key Applications
 - Important Specifications
2. Analyze the circuit and determine the overall function.
3. Verify that all wiring is correct.
4. Calculate the appropriate resistor values and the resistor current, voltage, and power.

Chapter 9

Switching Transistors

9.1 Objectives

1. Theory of Operation:

- Describe how a transistor operates in different regions (cutoff, active, and saturation).
- Explain the concept of a transistor as a switch.

2. Switching Characteristics:

- Analyze the switching behavior of transistors, including turn-on and turn-off times.
- Understand parameters such as rise-time, fall-time, delay-time, and storage-time.

3. Circuit Design and Analysis:

- Design simple switching circuits using transistors.
- Analyze and calculate the required component values for desired switching performance.
- Understand the term Overdrive in terms of Switching Transistors and its effect on Turn-On and Turn-Off times.
- Design an improved Switching Transistor circuit using a Commutating Capacitor.

9.2 Switching Transistors Identification

- The switching transistor circuit is NOT AN AMPLIFIER!! It is easily identified because it is missing a biasing circuit: No Base Bias, No Emitter Bias, No Universal Bias, No Collector Feedback Bias...

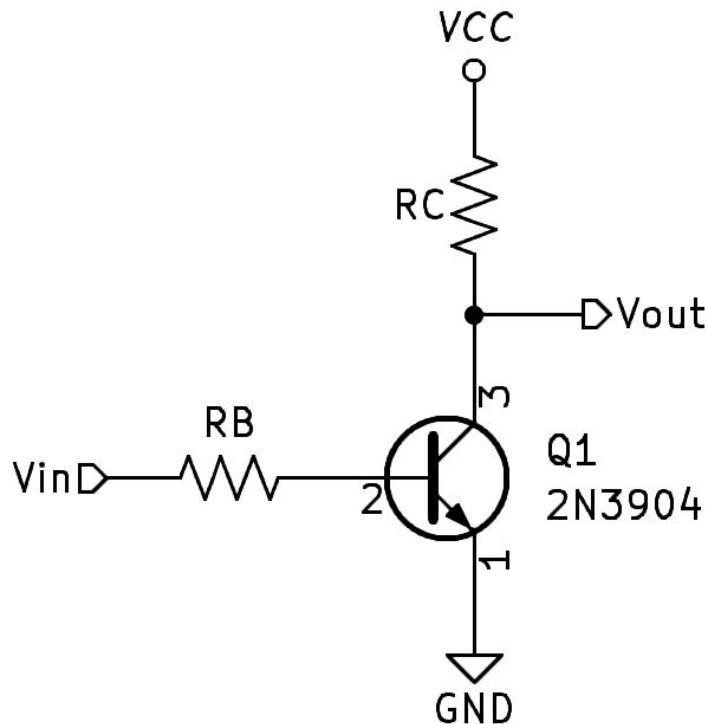


Figure 9.1: Switching Transistor Circuit

- The switching transistor circuit is designed to operate, not in the Active Region, but in Saturation and Cutoff.
- Switching transistor circuits operate much more efficiently than amplifier circuits because they operate in saturation and cutoff and not the active region.
 - In saturation, I_C is max and V_{CE} is theoretically 0V. $P_Q = 0w$
 - In cutoff, I_C is zero and V_{CE} is max. $P_Q = 0w$
- The Common Emitter switch configuration is an inverting switch.
 - A high V_{in} will equal low V_{out} . The transistor is in saturation.
 - A low V_{in} will equal high V_{out} . The transistor is in cutoff.

9.3 Switching Transistor Turn-On and Turn-Off Times

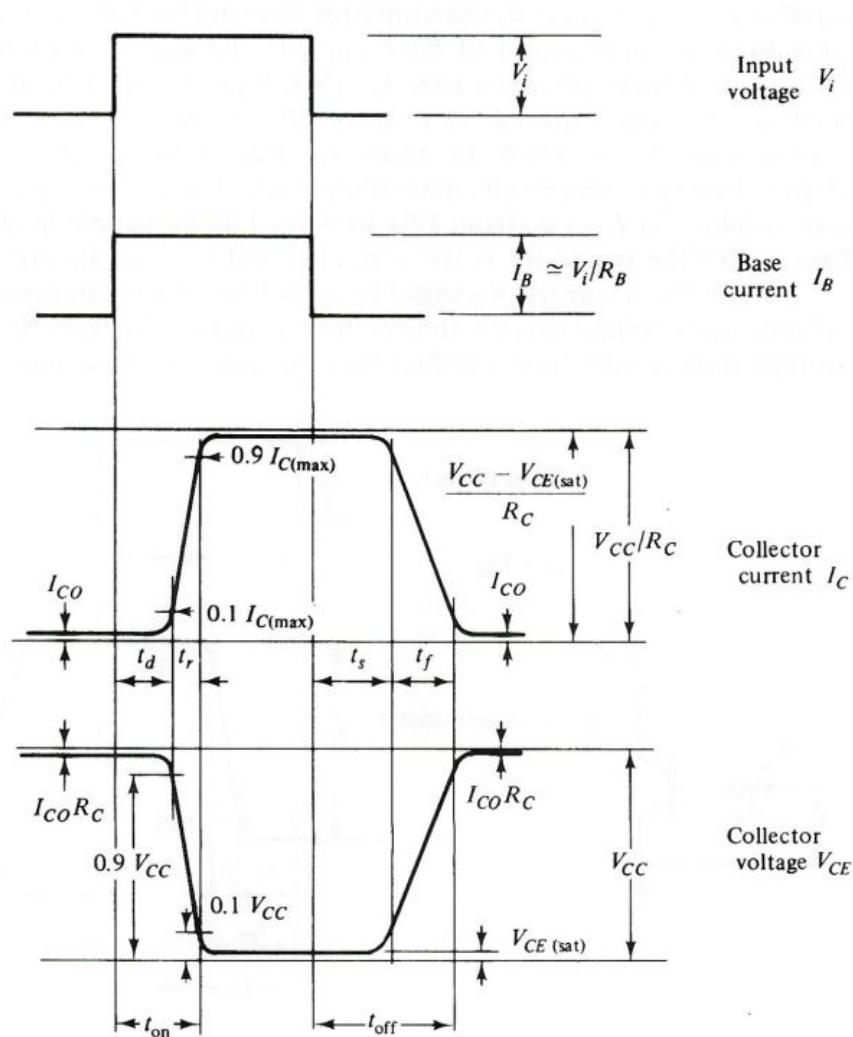


Figure 9.2: Switching Transistor Turn-On and Turn-Off Characteristics - Bell [19]

- t_d = Delay Time
- t_r = Rise Time. The transistor is turning on. Rise Time occurs when the input signal is transitioning from 10% to 90% of the signal voltage. The collector current will begin to flow from its 10% to 90% of $I_{C_{\text{sat}}}$ during the Rise Time.
- Turn-On Time = $t_d + t_r$
- t_f = Fall Time
- t_s = Storage Time
- Turn-Off Time = $t_s + t_f$

9.3.1 2N3904 Turn-On & Turn-Off Times

Switching Characteristics			
Delay Time	t_d	$V_{CC} = 3V, V_{EB} = 0.5V, I_C = 10mA, I_{B1} = 1mA$	- - 35 ns
Rise Time	t_r		- - 35 ns
Storage Time	t_s	$V_{CC} = 3V, I_C = 10mA, I_{B1} = I_{B2} = 1mA$	- - 200 ns
Fall Time	t_f		- - 50 ns

Figure 9.3: 2N3904 Switching Characteristics - NTE [20]

- 2N3904 Turn-On Time = $t_d + t_r$
 - 2N3904 Turn-On Time = $35nS + 35nS$
 - 2N3904 Turn-On Time = $70nS$
- 2N3904 Turn-On Time = $t_s + t_f$
 - 2N3904 Turn-Off Time = $200nS + 50nS$
 - 2N3904 Turn-Off Time = $250nS$

9.4 Switching Transistor Design

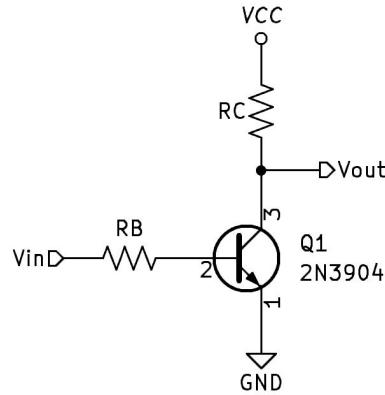


Figure 9.4: Switching Transistor Circuit

Calculation Steps:

- $I_{C_{Sat}} = \frac{V_{CC}}{RC}$
- $I_{B_{Sat}} = \frac{I_{C_{Sat}}}{Beta_{Q1}}$
- $RB_{Sat} = \frac{V_{in} - V_{beQ1}}{IB_{Sat}}$

9.5 Overdriving a Switching Transistor

Overdriving is achieved by increasing the switching transistors base current beyond IB_{Sat} . Overdriving the transistor switch will improve or decrease the Turn-On Time. However, the disadvantage is Overdriving will increase the Storage-Time which will increase the Turn-Off Time.

Overdrive by percentage

- To Overdrive by 10%, simply reduce RB_{Sat} by 10%. $RB_{10\%OD} = RB_{Sat} \times 0.9$
- To Overdrive by 20%, simply reduce RB_{Sat} by 20%. $RB_{20\%OD} = RB_{Sat} \times 0.8$
- Measure Turn-On and Turn-Off Times as Overdrive is being applied to the switching transistor. Repeat... until a decrease in RB no longer lowers the Turn-On Time.

9.6 Improved Turn-On and Turn-Off Times using a Commutating Capacitor

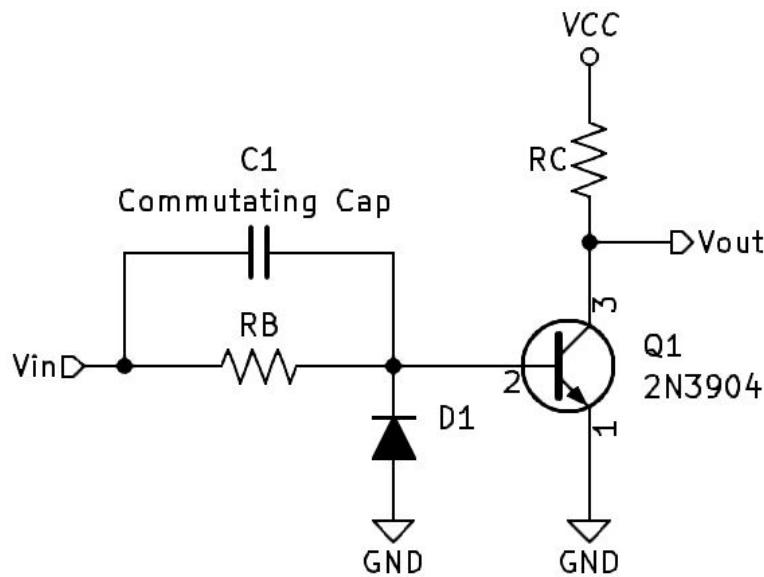


Figure 9.5: Improved Switching Transistor Circuit

Adding a Commutating Capacitor will improve both Turn-On and Turn-Off Times for the switching transistor circuit.

9.6.1 Commutating Capacitor Theory of Operation

- When V_{in} transitions from a low to a high, the Commutating Capacitor will initially act like a short causing the transistor to be overdriven and improving the Turn-On Time. Once the capacitor is charged ($V_{C1} = V_{in} - V_{beQ1}$) the current path is through R_B which is designed to keep the transistor in saturation and not in overdrive.
- When V_{in} transitions from a high to a low, (assuming there was previously enough time to fully charge the capacitor) the voltage across the commutating capacitor and R_B network is $V_{C1} = V_{in} - V_{beQ1}$ meaning that as V_{in} goes to 0V, the base of the transistor will see a negative voltage with respect to ground and its own emitter. This negative voltage at the base of the transistor will help turn off the transistor and because the transistor was previously in saturation and not in overdrive the Turn-Off Time is optimized.

Absolute Maximum Ratings:

Collector-Emitter Voltage, V_{CEO}	40V
Collector-Base Voltage, V_{CB}	60V
Emitter-Base Voltage, V_{EBO}	6V

Figure 9.6: 2N3904 V_{EB} Max - NTE [20]

- Observe in Figure 9.6 2N3904 V_{EB} Max - NTE [20] that the maximum negative voltage base to emitter is -6V ($V_{maxEB} = 6V$, $V_{maxBE} = -6V$). This means that if V_{in} is more than 6.7 volts the transistor could be damaged when V_{in} transitions to 0V due to the now negative voltage held by the capacitor. Diode D1 serves two functions, it is used to limit the negative voltage seen at V_{BE} to -0.7V; secondly, it removes R_B from the discharge path of the Commutating Capacitor allowing for a faster discharge. With diode D1 forward biased, via the discharging Commutating Capacitor, the discharge path is now through the diode and R_{Gen} of the input generator. This allows for a rapid discharge of the Commutating Capacitor, improving the Recovery Time.

9.6.2 Recovery Time and Maximum Frequency Calculations

1. Design a switching transistor circuit to operate in Saturation (do not overdrive).
2. Determine the Turn-On Time for the transistor the switching transistor used.
 - Turn-On Time = $t_d + t_r$
 - 2N3904 Turn-On Time = 35nS + 35nS
 - 2N3904 Turn-On Time = 70nS
3. Use the Turn-On Time to calculate the tau of the Commutating Capacitor.
 - $t_{on} = 0.1R_{Gen}C_C$
 - t_{on} = Turn-On Time

- making the tau one-tenth of the turn-on time allows for the capacitor to charge quickly
- R_{Gen} = Generator Resistance
- C_C = Commutating Capacitor

4. Initial Over-Drive Current Calculations:

- $IB(\max)_{\text{Instantaneous}} = \frac{V_{Gen} - V_{BE}}{R_{Gen}}$

5. Determine the Recovery Time t_{re} .

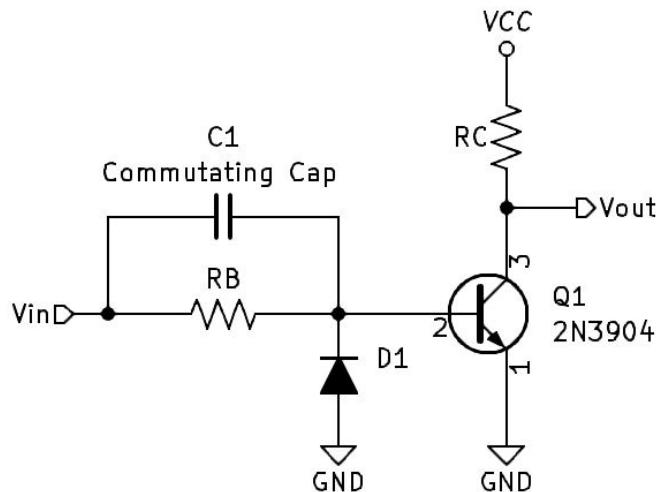
- The Recovery Time is the time needed for the capacitor to charge or discharge 90% of its final voltage.
- At 5tau the capacitor will be fully charged or fully discharged.
- Solve for the tau at 90%:
 - $V_C = V_{fin} - (V_{fin} - V_{in})e^{\frac{-t_{re}}{RC}}$
 - $0.9 = 1 - (1 - 0)e^{\frac{-t_{re}}{RC}}$
 - $0.9 - 1 = -(1 - 0)e^{\frac{-t}{RC}}$
 - $-0.1 = -(1 - 0)e^{\frac{-t_{re}}{RC}}$
 - $-0.1 = -(1)e^{\frac{-t_{re}}{RC}}$
 - $\frac{-0.1}{-1} = e^{\frac{-t_{re}}{RC}}$
 - $0.1 = e^{\frac{-t_{re}}{RC}}$
 - $LN(0.1) = \frac{-t_{re}}{RC}$
 - $\frac{-t_{re}}{RC} = -2.303$
 - $-t_{re} = -2.303(RC)$
 - With diode D1 in the circuit, R_{Gen} becomes the primary resistance in the discharge path of the Commutating Capacitor, you could add the dynamic resistance of the diode.
- ✓ $t_{re} = 2.303(RC)$

6. Determine the maximum square wave input frequency f_{MaxCC} for the Commutating Capacitor Switching Transistor circuit:

- $f_{MaxCC} \approx \frac{1}{2t_{re}}$

9.7 Practice Questions:

1. Design a Switching Circuit using a Commutating Capacitor to improve both Turn-On and Turn-Off Times.



Given: $V_{CC} = 9V$, $IC = 10mA$, $\text{Beta}_{min} = 50$, $V_{in} = 0$ to $5V$, $T_{On} = 50nS$, $R_{Gen} = 50\Omega$.

Find: RC , RB , & $C1$.

Solve:

$$RC = \underline{\hspace{2cm}}$$

$$RB = \underline{\hspace{2cm}}$$

$$C1 = \underline{\hspace{2cm}}$$

9.8 Answers:

1. $RC = \underline{880\Omega}$

$$RB = \underline{21.45K\Omega}$$

$$C1 = \underline{0.01\mu F}$$

Chapter 10

Multivibrators

10.1 Objectives:

1. Introduction to Multivibrators:

- Define what multivibrators are and their role in electronic circuits.
- Differentiate between the types of multivibrators: astable, monostable, and bistable.

2. Theory of Operation:

- Explain the basic principles and operation of each type of multivibrator.
- Discuss the conditions under which each type operates and their typical applications.

3. Astable Multivibrators:

- Describe the structure and function of an astable multivibrator.
- Analyze the waveform outputs and timing characteristics.
- Design and calculate component values for a given frequency and duty cycle.

4. Monostable Multivibrators

- Explain the operation of a monostable multivibrator.
- Discuss its use as a pulse generator.
- Design circuits to produce a specific pulse width.

5. Circuit Design and Analysis:

- Build and analyze multivibrator circuits using both discrete components and integrated circuits (ICs).

10.2 Introduction:

A multivibrator is a versatile electronic circuit used to implement simple yet essential functionalities in various applications. Comprising resistors, capacitors, and transistors or integrated circuits, multivibrators are categorized into three types: astable, monostable, and bistable. Each type serves a distinct purpose: astable multivibrators generate continuous oscillations without requiring an external trigger, monostable multivibrators produce a single output pulse in response to an input trigger, and bistable multivibrators, also known as flip-flops, toggle between two stable states based on input signals. These circuits play a crucial role in timing, waveform generation, and digital logic operations, making them foundational elements in the design of clocks, pulse generators, memory storage devices, and other critical electronic systems.

10.3 Schmitt Triggered Astable Multivibrator:

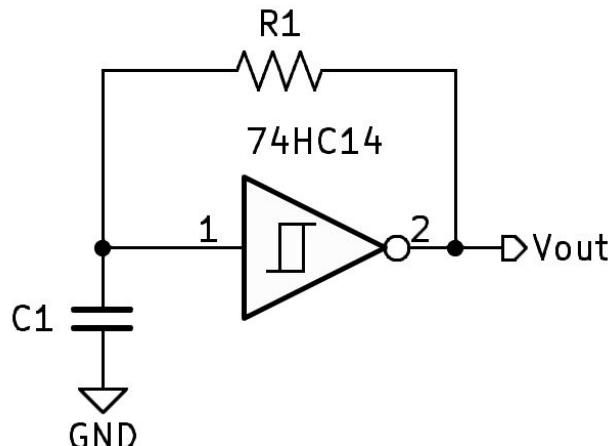


Figure 10.1: Schmitt Triggered Astable Multivibrator

10.3.1 SN74HC14 Specifications

- $V_{outH} \approx 5V$
- $V_{outL} \approx 0V$
- $V_{T+} \approx 2.5V$
- $V_{T-} \approx 1.6V$
- To get more accuracy use measured V_{outH} , V_{outL} , V_{T+} , and V_{T-} .

10.3.2 Pulse Width Calculations:

- $V_C = V_{fin} - (V_{fin} - V_{in})e^{\frac{-t}{RC}}$
- $V_{T+} = V_{out_H} - (V_{out_H} - V_{T-})e^{\frac{-PW}{RC}}$
- $2.5V = 5V - (5V - 1.6V)e^{\frac{-PW}{RC}}$
- $2.5V - 5V = -(5V - 1.6V)e^{\frac{-PW}{RC}}$
- $-2.5V = -(3.4V)e^{\frac{-PW}{RC}}$
- $\frac{2.5}{3.4} = e^{\frac{-PW}{RC}}$
- $LN(\frac{2.5}{3.4}) = \frac{-PW}{RC}$
- $-0.30748 = \frac{-PW}{RC}$
- ✓ $PW = RC \times 0.30748$
- The R value: The gate needs to have enough current I_{in_H} to allow the inverter to switch states. Generally speaking, we would want the capacitor current to be ten times larger than I_{in_H} at the time of the transition. This means that we may be instantaneously (for a short amount of time) exceeding the I_{out_H} specification. Because of this we need to keep the R1 value small enough to maintain oscillations but large enough to protect the output current specifications/limitations of the inverter. If the R1 value is too big the circuit will not oscillate.
- $R1 \approx \frac{V_{out_H} - V_{T+}}{2 \times I_{out_H}}$
 - $R1 \approx \frac{5V - 2.5V}{2 \times 400\mu A}$
 - $R1 \approx \frac{2.5V}{800\mu A}$
- ✓ $R1 \approx 3.125K\Omega$
- $C \approx \frac{PW}{R1 \times 0.30748}$
- ✓ $C \approx \frac{PW}{3.125K\Omega \times 0.30748}$

10.3.3 Pulse Space Calculations:

- $V_C = V_{fin} - (V_{fin} - V_{in})e^{\frac{-t}{RC}}$
- $V_{T-} = V_{out_L} - (V_{out_L} - V_{T+})e^{\frac{-PS}{RC}}$
- $1.6V = 0 - (0 - 2.5V)e^{\frac{-PS}{RC}}$
- $1.6V = -(-2.5V)e^{\frac{-PS}{RC}}$
- $1.6V = (2.5V)e^{\frac{-PS}{RC}}$
- $\frac{1.6V}{2.5V} = e^{\frac{-PS}{RC}}$

- o $LN\left(\frac{1.6V}{2.5V}\right) = \frac{-PS}{RC}$
- o $-0.446287 = \frac{-PS}{RC}$
- o $-0.446287 \times RC = -PS$
- ✓ $PS \approx 0.446287(3.125K\Omega \times C)$

- Build and measure, adjust the capacitor value to achieve the desired frequency.

10.4 BJT Astable Multivibrator:

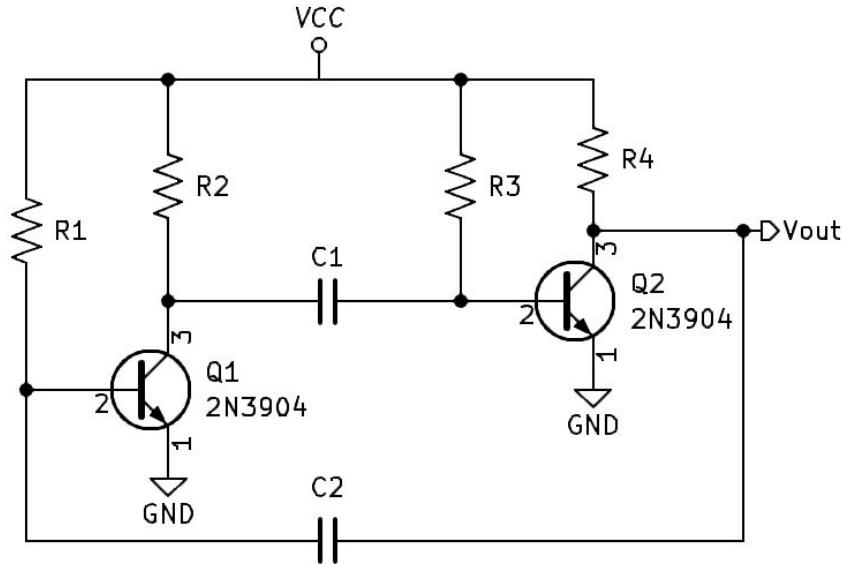


Figure 10.2: Bipolar Junction Transistor Astable Multivibrator

10.4.1 Introduction

The Bipolar Junction Transistor (BJT) Astable Multivibrator is a fundamental electronic circuit that generates a continuous square wave output, making it an essential component in timing and waveform generation applications. Unlike monostable or bistable multivibrators, an astable multivibrator has no stable states; it constantly switches between its two unstable states, producing a periodic oscillation without the need for an external trigger. Utilizing BJTs, capacitors, and resistors, this circuit operates by alternately driving the transistors into saturation and cutoff regions, resulting in a consistent toggling action. BJT astable multivibrators are widely used in applications such as clock pulse generation, LED flashers, and tone generators, providing a simple yet effective solution for generating periodic signals in various electronic devices.

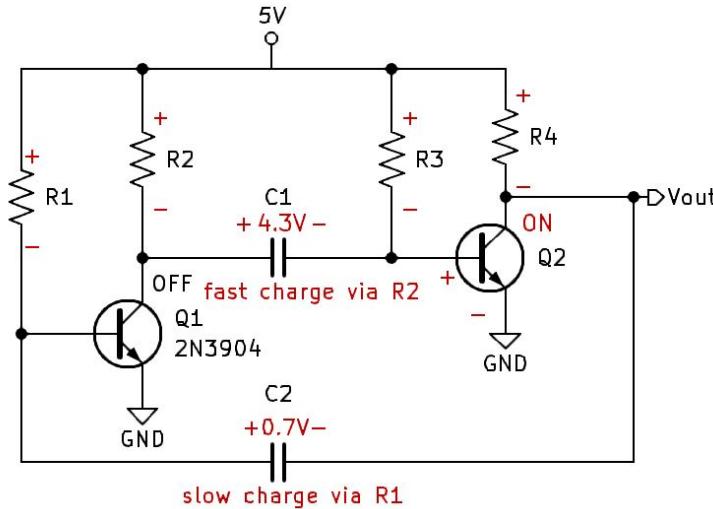
10.4.2 Calculation Steps

Calculating R values:

1. The transistors should act like switches operating in the Saturation and Cutoff Regions.
 - (a) Choose the saturation current IC_{Sat} .
 - (b) $R2 \& R4 = \frac{VCC}{IC_{Sat}}$
 - (c) $IB_{Sat} = \frac{IC_{Sat}}{\text{Beta}_{min}}$
 - (d) $R1 \& R3 = \frac{VCC - V_{BE}}{IB_{Sat}}$
 - (e) Example: $VCC = 5V$, $IC_{Sat} = 10mA$, and $\text{Beta}_{Q1\&Q2} = 100$:
 - i. $R2 \& R4 = 500\Omega$
 - ii. $R1 \& R3 = 43K\Omega$

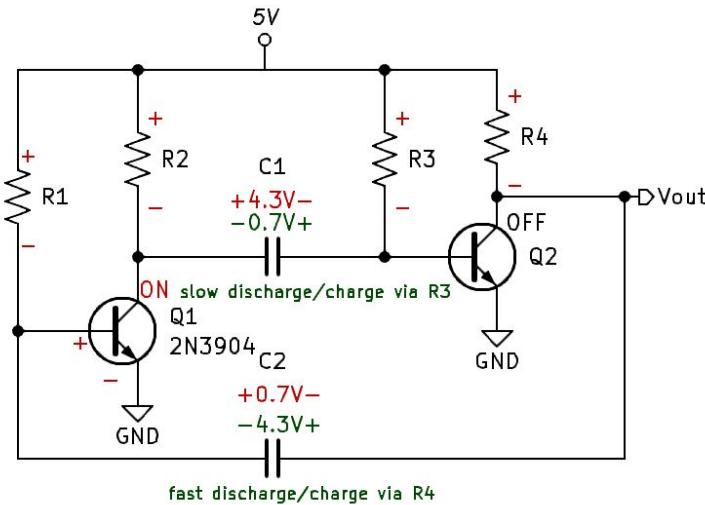
Calculating C values:

2. Notice $R2$ and $R4$ are relatively small compared to $R1$ and $R3$. Assuming $C1$ and $C2$ are equal and depending on which transistor is on, the capacitor with the charge path through $R2$ or $R4$ will change much faster than the other capacitor which will have either $R1$ or $R3$ to charge/discharge through.



Assuming that $VCC = 5V$ and $Q2$ is ON and $Q1$ is OFF.

- (a) $C1$ (relative to $C2$) will charge quickly through the smaller RC resistor $R2$.
- (b) $C2$ (relative to $C1$) will charge slower through the larger RB resistor $R1$.



- (c) At the moment C2 reaches 0.7V, Q1 will turn on. When Q1 turns on it provides a path to ground, the capacitor C1 has been charged to 4.3V and now the base of Q2 has -4.3V VBE which will immediately force Q2 Off.
- (d) Observe that the circuit will oscillate between these two states. Q1 and Q2 will oscillate between on and off opposite each other, and C1 constantly charge and discharge between 4.3V and -0.7V and C2 will charge and discharge between 0.7V and -4.3V. The timing of the circuit is always dependent on the RB resistor (the slower of the two discharge/charge cycles).

3. Pulse Width occurs when Q2 is off.

- (a) Analyzing the circuit, observe that when C1 charges to 0.7V through R3, Q2 will turn on. This means that C1 and R3 (the time it takes C1 to discharge from -4.3V and charge to 0.7V) will determine the Pulse Width or time off of Q2.

4. Pulse Space occurs when Q2 is on.

- (a) Analyzing the circuit, observe that when C2 charges to 0.7V through R1, Q1 will turn on which will force Q2 off. This means that C2 and R1 (the time it takes C2 to discharge from -4.3V and charge to 0.7V) will determine the Pulse Space or time off of Q2.

5. Capacitor Formulas Derived:

$$(a) VC = V_{fin} - (V_{fin} - V_{in})e^{\frac{-t}{RC}}$$

When V_{C1} reaches 0.7V, the output transitions from a high to a low.

- $0.7V = V_{Fin} - (V_{fin} - V_{in})e^{\frac{-t}{RC}}$

If the transistor could charge uninterrupted, it would charge to V_{CC} in this example 5V.

- $0.7V = 5V - (5V - V_{in})e^{\frac{-t}{RC}}$

The tricky part is that we must account for the changing polarity of the capacitor voltage, meaning the capacitor has to discharge down from -4.3V to 0 and up to 0.7V.

- $0.7V = 5V - (5V - (-4.3V))e^{\frac{-t}{RC}}$
 - $0.7V - 5V = -(5V - (-4.3V))e^{\frac{-t}{RC}}$
 - $-4.3V = -(5V + 4.3V)e^{\frac{-t}{RC}}$
 - $-4.3V = -(9.3V)e^{\frac{-t}{RC}}$
 - $\frac{-4.3V}{-9.3V} = e^{\frac{-t}{RC}}$
 - $\frac{4.3}{9.3} = e^{\frac{-t}{RC}}$
 - $LN\frac{4.3}{9.3} = \frac{-t}{RC}$
 - $-0.7714 = \frac{-t}{RC}$
 - $C = \frac{t}{0.7714R}$

In our example, $R = RB_{Q2} = R3$ and $C = C1$.

- $C1 = \frac{t}{0.7714(43K\Omega)}$

Select a time or desired frequency. For this example, we will use 1Khz.

- $t = \frac{1}{2f}$
 - $t = \frac{1}{2(1Khz)}$
 - $t = 500\mu S$

Solve for C1.

- $C1 = \frac{t}{0.7714(43K\Omega)}$
 - $C1 = \frac{500\mu S}{0.7714(43K\Omega)}$
 - ✓ $C1 = 15.074nF$

Assuming a desired 50% duty cycle if the two RBs (R1 and R3) are equal, C2 will be equal to C1.

- $C2 = C1 = 15.074nF$

10.4.3 Capacitor Value Approximation Method

The Approximation Method assumes that the discharge voltage is down to 0V and the charge voltage is VCC.

1. $VC = V_{fin} - (V_{fin} - V_{in})e^{\frac{-t}{RC}}$
 - $0V = VCC - (VCC - (-VCC))e^{\frac{-t}{RC}}$
 - $-VCC = -(VCC - (-VCC))e^{\frac{-t}{RC}}$
 - $-VCC = -(VCC + VCC)e^{\frac{-t}{RC}}$
 - $-VCC = -(2VCC)e^{\frac{-t}{RC}}$
 - $\frac{-VCC}{-2VCC} = e^{\frac{-t}{RC}}$

- $\frac{1}{2} = e^{\frac{-t}{RC}}$
- $LN\frac{1}{2} = \frac{-t}{RC}$
- $-0.693147 = \frac{-t}{RC}$
- $C = \frac{-t}{-0.693147R}$
- $C = \frac{t}{0.693147R}$
- ✓ $C = \frac{PW}{0.693147R}$ (Substitute desired Pulse Width for time)

Design for previous circuit at 1Khz:

- $C = \frac{500\mu S}{0.693147(43K\Omega)}$
- $C = \frac{500\mu S}{0.693147(43K\Omega)}$
- $C = 16.776nF$

$C1 \text{ & } C2 = 16.776nF$ (using the approximation method)

10.4.4 Improved Rise Time Astable Variant

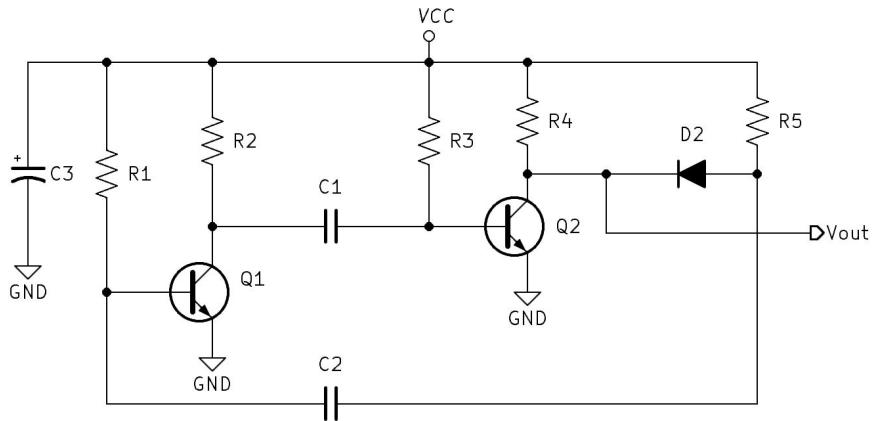


Figure 10.3: Improved Rise Time BJT Astable Variant

R5 Calculations for Improved Rise Time BJT Astable Variant

1. Pulse Width (PW) = 5τ
 - (a) $\tau = \frac{PW}{5}$
2. $\tau = RC$
3. Substitute the formulas in terms of τ .
 - (a) $RC = \frac{PW}{5}$
 - (b) $R5 \times C2 = \frac{PW}{5}$
 - ✓ $R5 = \frac{PW}{C2 \times 5}$

10.5 BJT Monostable Multivibrator:

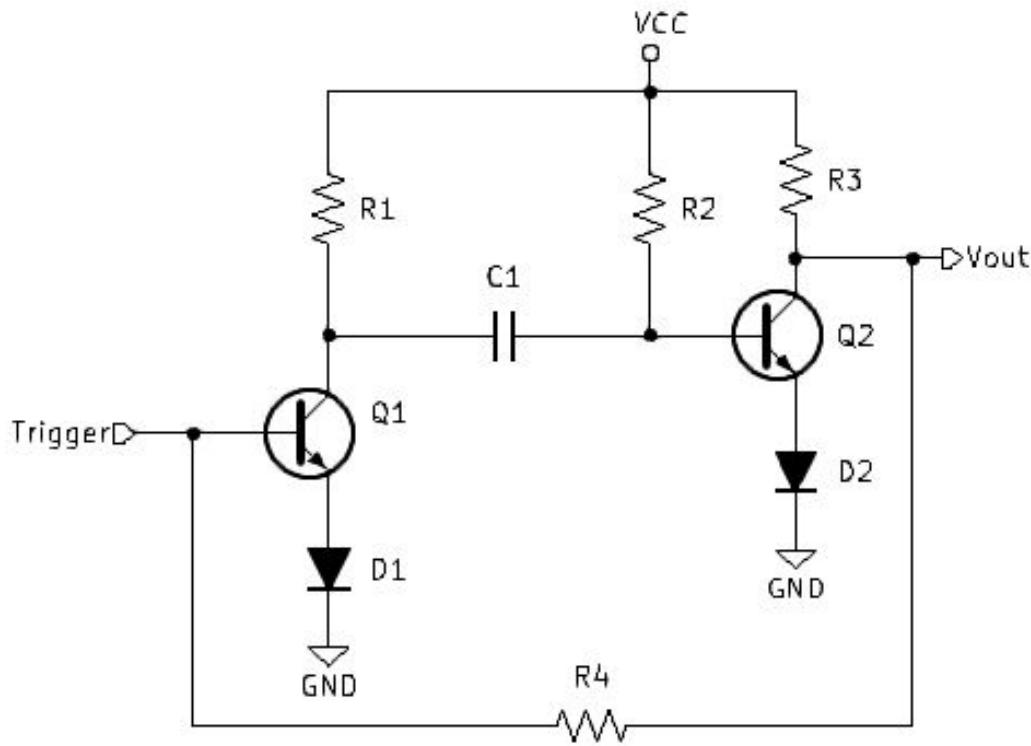


Figure 10.4: Bipolar Junction Transistor Monostable Multivibrator

10.5.1 Introduction

A Bipolar Junction Transistor (BJT) monostable multivibrator, also known as a one-shot multivibrator, is a pivotal circuit in electronics designed to generate a single output pulse of a specific duration in response to an external trigger. Unlike its astable counterpart, the BJT monostable multivibrator has one stable state and one unstable state. Upon receiving a triggering signal, the circuit temporarily shifts to its unstable state, producing a pulse before reverting to its stable state. This functionality is achieved using a combination of BJTs, resistors, and capacitors, which determine the pulse width. Monostable multivibrators are extensively used in applications such as pulse generation, timers, and debouncing switches, offering precise control over timing events in various electronic systems.

10.5.2 Calculating Resistor Values

1. The transistors will be like switches, designed to operate in the Saturation and Cutoff regions.
2. Choose a saturation current IC_{Sat} .
3. $R1 \& R3 = \frac{VCC - VF_{Diode}}{IC_{Sat}}$
4. $IB_{Sat} = \frac{IC_{Sat}}{\text{Beta}_{min}}$
5. $R2 \& R4 = \frac{VCC - (V_{BE} + VF_{Diode})}{IB_{Sat}}$
6. Example:
 - Given: $VCC = 5V$, $IC_{Sat} = 10mA$, and $\text{Beta}_{min} = 100$
 - $R1 \& R3 = 430\Omega$
 - $R2 \& R4 = 36K\Omega$

10.5.3 Calculating the Capacitor Value

- Diodes D1 and D2 serve two purposes. They raise the trigger threshold voltage which helps prevent false triggers and protect the transistors from negative over-voltage/current at the base to emitter junction.

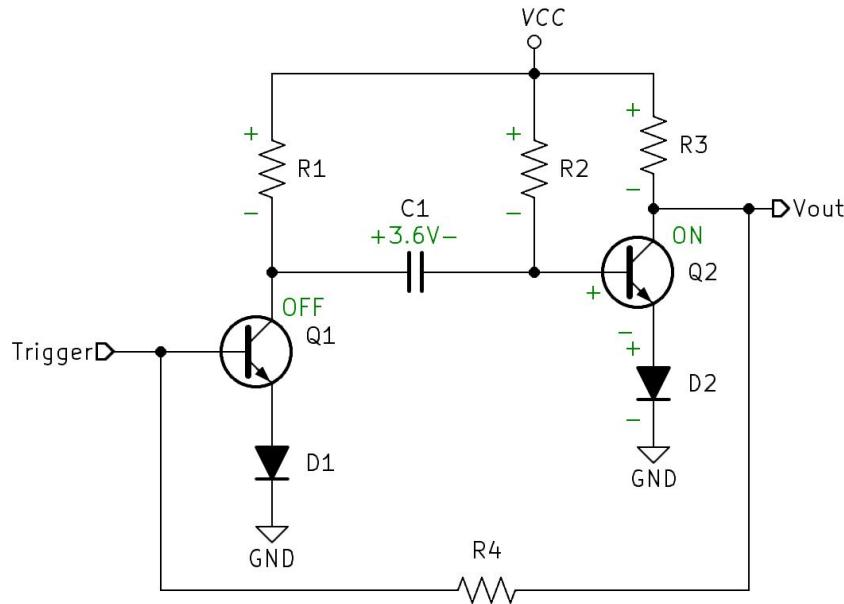


Figure 10.5: Bipolar Junction Transistor Monostable Multivibrator Stable State

- Stable State** Observe Figure 10.5. Q2 will immediately turn on due to the unrestricted base resistor R2. The current path for Q1 to turn on goes through R3 and R4. This means Q2 will turn on faster than Q1 and once Q1 is on it will take away VCC leaving only the 0.7 volts of D2 which will not be enough to bias on both Q1 and D1. This is the happy or stable state of the monostable and Vout is low.

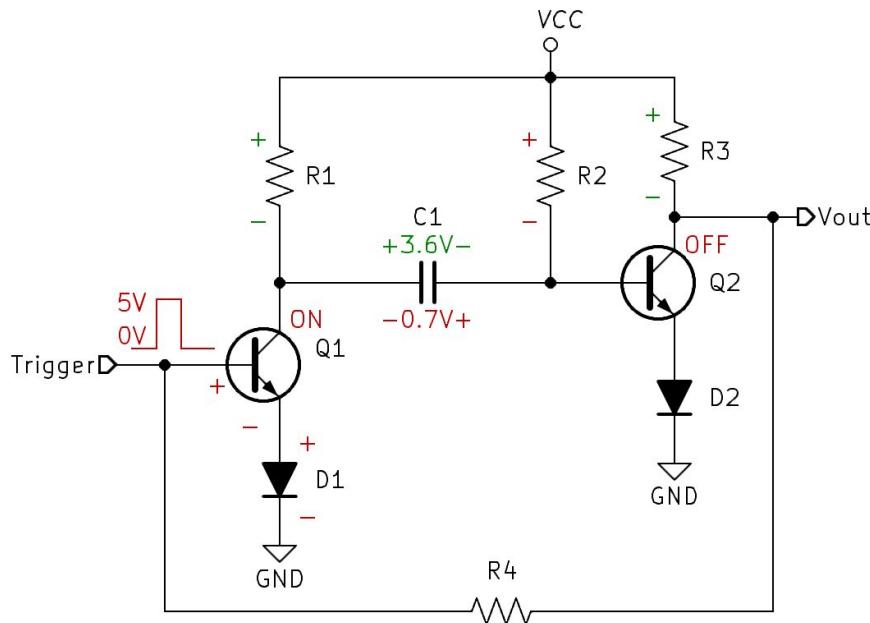


Figure 10.6: Bipolar Junction Transistor Monostable Multivibrator Un-Stable State

- To drive the monostable output high, a positive going trigger signal must be applied to the base of Q1. Ideally, the trigger pulse width is significantly less than the desired pulse width of the Monostable Multivibrator.
- Observe Figure 10.6. As Q1 is biased on from the Trigger signal, Q2 initially will see -3.6V at its base which will turn Q2 off. C1 will begin to discharge the -3.6V through the path of R2, Q1, and D1. Once discharged Q2 will begin to charge and once it reaches 0.7V, the base of Q2 will now have 1.4V ($V_{C1} + V_{D1}$) this will turn on Q2 which will then force Q1 back off returning the circuit to return to its stable state.

- $VC = V_{fin} - (V_{fin} - V_{in})e^{\frac{-t}{RC}}$

- $0.7V = VCC - (VCC - (VCC - 1.4V))e^{\frac{-PW}{R2C1}}$
- $0.7V = VCC - (VCC + VCC - 1.4V)e^{\frac{-PW}{R2C1}}$
- $0.7V = VCC - (2VCC - 1.4V)e^{\frac{-PW}{R2C1}}$
- $0.7V - VCC = -(2VCC - 1.4V)e^{\frac{-PW}{R2C1}}$
- $0.7V - VCC = (-2VCC + 1.4V)e^{\frac{-PW}{R2C1}}$
- $\frac{0.7V - VCC}{-2VCC + 1.4V} = e^{\frac{-PW}{R2C1}}$

- $\frac{VCC - 0.7V}{2VCC - 1.4V} = e^{\frac{-PW}{R2C1}}$
- $\frac{1(VCC - 0.7V)}{2(VCC - 0.7V)} = e^{\frac{-PW}{R2C1}}$
- $\frac{1}{2} = e^{\frac{-PW}{R2C1}}$
- $LN\frac{1}{2} = \frac{-PW}{R2C1}$
- $-0.693 = \frac{-PW}{R2C1}$
- $C1 = \frac{-PW}{R2 \times (-0.693)}$
- ✓ $C1 = \frac{PW}{R2 \times 0.693}$

Example:

Given: $VCC = 5V$, $IC_{Sat} = 10mA$, $Beta_{min} = 100$, $R1$ & $R3 = 500\Omega$, $R2$ & $R4 = 43K\Omega$, and $PW = 1\text{ Second}$.

Find: $C1$

- $C1 = \frac{PW}{R2 \times 0.693}$
- $C1 = \frac{-1\text{Sec}}{43K\Omega \times 0.693}$
- ✓ $C1 = 33.558\mu F$

10.5.4 Trigger Circuit

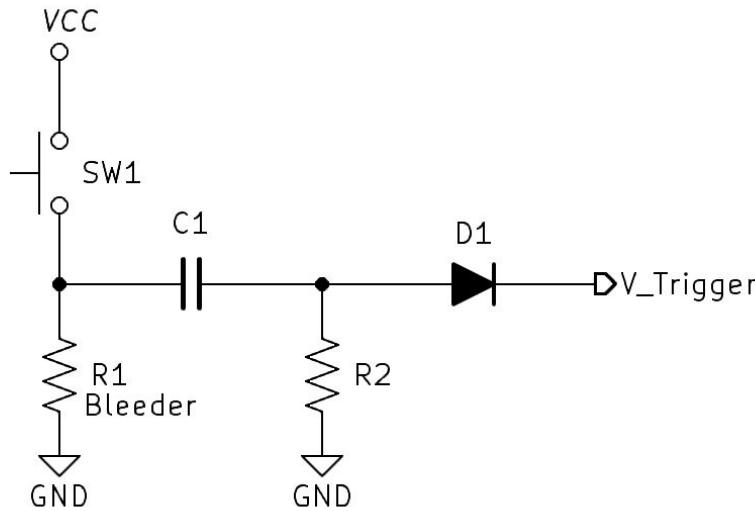


Figure 10.7: Trigger Circuit

The trigger signal's pulse width needs to be significantly less than the pulse width of the monostable multivibrator ideally, $PW_{Trigger} \leq \frac{PW_{MonoStable}}{10}$. A differentiated pulse signal in Figure 10.7. will eliminate switch bounce and will prevent unintended re-triggers of the Monostable Multivibrator.

Trigger Circuit Setup:

- Consider the desired Monostable Multivibrator output Pulse Width.
- Design an RC Differentiated circuit (C_1 and R_2) to produce a pulse that is ten times smaller than the desired Monostable Pulse Width, $PW_{Trigger} \leq \frac{PW_{MonoStable}}{10}$. Review RC Circuits Differentiators on page 61 if necessary.
- Make R_1 the bleeder resistor ten times larger than R_2 , $R_{Bleeder} \approx 10 \times R_2$.
- Diode D_1 clips the negative spike of the differentiated signal.
- Build and test. If the signal looks correct but the Monostable Multivibrator will not trigger, raise the resistance of R_2 until the Monostable is reliably triggered by switch SW1.

10.6 Extreme Duty Cycle Astable Multivibrator Circuit Variant

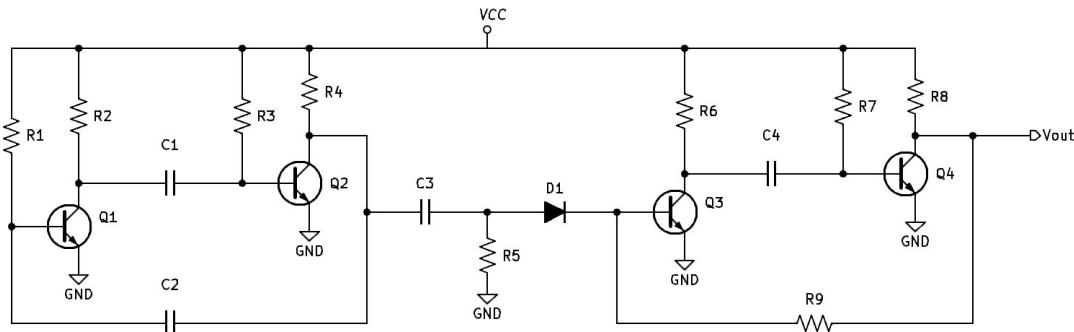


Figure 10.8: Astable Multivibrator Extreme Duty Cycle Circuit Variant

10.6.1 Introduction

An extreme duty cycle astable multivibrator circuit variant is a specialized form of the conventional astable multivibrator designed to generate output pulses with exceptionally high or low duty cycles. Unlike standard configurations, which typically aim for a 50% duty cycle or moderately skewed pulse widths, this variant uses tailored resistor and capacitor values to produce output signals where the on-time or off-time significantly dominates the cycle. Such circuits are particularly useful in applications requiring precise control over pulse duration relative to the overall period, such as in pulse-width modulation (PWM) for power control, specialized timing circuits, and signal modulation tasks. By leveraging components like Bipolar Junction Transistors (BJTs) or integrated circuits (ICs), these multivibrators

can achieve the desired extreme duty cycles while maintaining stability and reliability in various electronic systems.

- The standard Astable Multivibrator circuit likes to operate around 50% duty cycle.
- To produce an extreme duty cycle waveform, an a standard Astable circuit can be used to drive/trigger a standard Monostable circuit as seen in Figure 10.8.
- Design steps:
 1. Design a 50% duty cycle BJT Astable to operate at the desired frequency (Q1 & Q2).
 2. Design a BJT Monostable circuit to produce the desired pulse width (Q3 & Q4).
 3. Use an RC circuit to differentiate the output of the Astable to produce the trigger pulse for the Monostable circuit (C3 & R5) ensuring that the differentiated waveform's pulse width is significantly less than the desired output pulse width.
 4. The Diode D1 protects the base of Q3 from any negative voltage and keeps R6 isolated from the monostable biasing circuit.

10.7 555 Timer Astable Multivibrator:

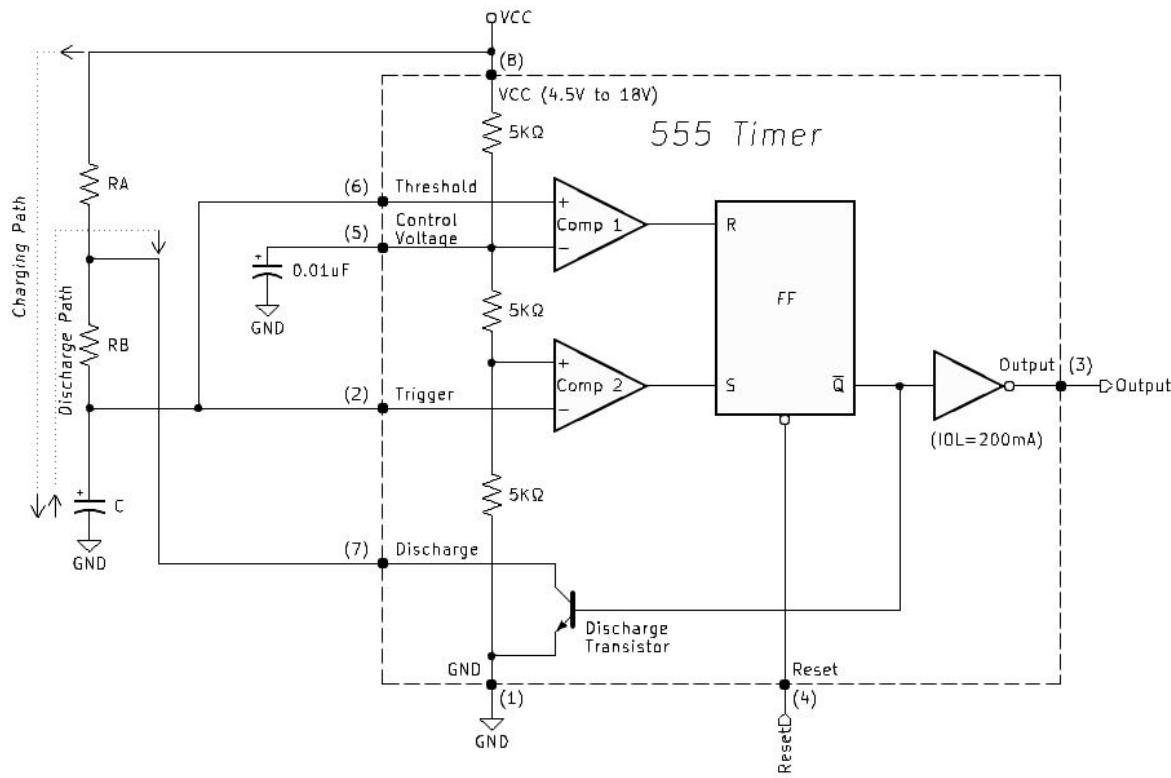


Figure 10.9: Simplified block diagram of a 555 timer with the external timer components to form an astable multivibrator - Kleitz [21]

10.7.1 Introduction

The 555 timer astable multivibrator is a versatile and widely-used electronic circuit configuration that generates a continuous square wave output. At the heart of this configuration is the 555 timer IC, a highly reliable and easy-to-use integrated circuit that has become a staple in electronics design. In its astable mode, the 555 timer operates without any stable states, constantly oscillating between high and low output levels to produce a periodic waveform. This oscillation is achieved by carefully selecting external resistors and capacitors, which determine the frequency and duty cycle of the output signal. The 555 timer astable multivibrator is commonly employed in applications such as clock pulse generation, LED flashers, and tone generators, offering a simple yet powerful solution for creating precise and adjustable timing signals in a variety of electronic projects.

10.7.2 Circuit Analysis

- Internally, VCC is divided across three $5\text{K}\Omega$ resistors. Comparator 1 will have $\frac{2VCC}{3}$ on its minus input. Comparator 2 will have $\frac{1VCC}{3}$ on its plus input.
- When power is initially turned on, the capacitor voltage VC , starting at zero volts will charge up through RA and RB. Starting off, Comparator 1 will rail negative, and Comparator 2 will rail positive. This will set the Flip Flop, \bar{Q} will equal a Low, the discharge transistor is off and the output, after the inverter, is High.
- As the capacitor voltage charges up through RA and RB, it will eventually cross the $\frac{1VCC}{3}$ threshold, this will cause Comparator 2 to rail negative which will cause the Flip Flop to enter a (0,0) Hold state (no change at the output).
- The capacitor voltage continues to charge through RA and RB and will eventually cross the $\frac{2VCC}{3}$ threshold. At this point, Comparator 1 will rail positive resulting in a reset for the Flip Flop, \bar{Q} will go high and turn on the discharge transistor. Additionally, the output will go low via the inverter.
- Once the discharge transistor is on, ground potential is essentially placed between RA and RB. This will cause the capacitor to start to discharge through RB.
- As VC discharges and falls below $\frac{2VCC}{3}$, Comparator 1 will rail low which will cause the Flip Flop to go into a hold state (0,0).
- As VC continues to discharge and falls below $\frac{1VCC}{3}$, Comparator 2 will rail high and cause the Flip Flop to go into a Set state. \bar{Q} will go low which will turn off the discharge transistor and the output will go high via the inverter.
- From the analysis, we can see that our Astable output will oscillate as VC discharges and charges between $\frac{2VCC}{3}$ and $\frac{1VCC}{3}$.

10.7.3 Pulse Width (Charge Time) Formula Derivation

During the charge cycle, we know that the output is high and the capacitor will charge through RA and RB from $\frac{1VCC}{3}$ to $\frac{2VCC}{3}$.

- $VC = V_{fin} - (V_{fin} - V_{in})e^{\frac{-t}{RC}}$
 - $\frac{2VCC}{3} = VCC - (VCC - \frac{1VCC}{3})e^{\frac{-PW}{(RA+RB)C}}$
 - $\frac{2VCC}{3} = \frac{3VCC}{3} - (\frac{3VCC}{3} - \frac{1VCC}{3})e^{\frac{-PW}{(RA+RB)C}}$
 - $\frac{2VCC}{3} = \frac{3VCC}{3} - (\frac{2VCC}{3})e^{\frac{-PW}{(RA+RB)C}}$
 - $\frac{2VCC}{3} - \frac{3VCC}{3} = -(\frac{2VCC}{3})e^{\frac{-PW}{(RA+RB)C}}$
 - $\frac{-1VCC}{3} = (-\frac{2VCC}{3})e^{\frac{-PW}{(RA+RB)C}}$

- $\frac{-1VCC}{3} \times \frac{-3}{2VCC} = e^{\frac{-PW}{(RA+RB)C}}$
- $\frac{3VCC}{6VCC} = e^{\frac{-PW}{(RA+RB)C}}$
- $\frac{1}{2} = e^{\frac{-PW}{(RA+RB)C}}$
- $LN\frac{1}{2} = \frac{-PW}{(RA+RB)C}$
- $-0.693147 = \frac{-PW}{(RA+RB)C}$
- ✓ $PW = 0.693147(RA + RB)C$

10.7.4 Pulse Space (Discharge Time) Formula Derivation

During the discharge cycle, we know that the output is low and the capacitor will discharge through RB from $\frac{2VCC}{3}$ to $\frac{1VCC}{3}$.

- $VC = V_{fin} - (V_{fin} - V_{in})e^{\frac{-t}{RC}}$
- $\frac{1VCC}{3} = 0 - (0 - \frac{2VCC}{3})e^{\frac{-PS}{(RB)C}}$
- $\frac{1VCC}{3} = -(-\frac{2VCC}{3})e^{\frac{-PS}{(RB)C}}$
- $\frac{1VCC}{3} = (\frac{2VCC}{3})e^{\frac{-PS}{(RB)C}}$
- $\frac{1VCC}{3} = (\frac{2VCC}{3})e^{\frac{-PS}{(RB)C}}$
- $\frac{1VCC}{3} \times \frac{3}{2VCC} = e^{\frac{-PS}{(RB)C}}$
- $\frac{3VCC}{6VCC} = e^{\frac{-PS}{(RB)C}}$
- $\frac{1}{2} = e^{\frac{-PS}{(RB)C}}$
- $LN\frac{1}{2} = \frac{-PS}{(RB)C}$
- $-0.693147 = \frac{-PS}{(RB)C}$
- ✓ $PS = 0.693147(RB)C$

10.7.5 Design Example

- Pick a desired frequency. For this example, we will use 1Khz.
- $Period = \frac{1}{frequency} = \frac{1}{1Khz} = 1mS$
- $Period = PW + PS$
 - * $Period = 0.693147(RA + RB)C + 0.693147(RB)C$
 - * $Period = 0.693147C[(RA + RB) + (RB)]$
 - * $Period = 0.693147C[RA + 2RB]$
 - * $\frac{Period}{0.693147C} = [RA + 2RB]$

- * $\frac{1mS}{0.693147C} = [RA + 2RB]$
Pick a capacitor value ($1\mu F$)
- * $\frac{1mS}{0.693147 \times 1\mu F} = RA + 2RB$
- * $1.443 \times 10^3 = RA + 2RB$
Make RA approximately $\frac{1}{3}$ of the total resistance.
- * $RA \approx \frac{1.443 \times 10^3}{3} \approx 480.898\Omega$
Round RA to a standard value
- ✓ $RA = 470\Omega$
Solve for RB
- * $2RB = 1.443K\Omega - 470\Omega$
- * $2RB = 972.695\Omega$
- * $RB = \frac{972.695\Omega}{2}$
- ✓ $RB = 486.348\Omega$ ($470\Omega + 18\Omega$)

10.7.6 Adjustable Duty Cycle Circuit

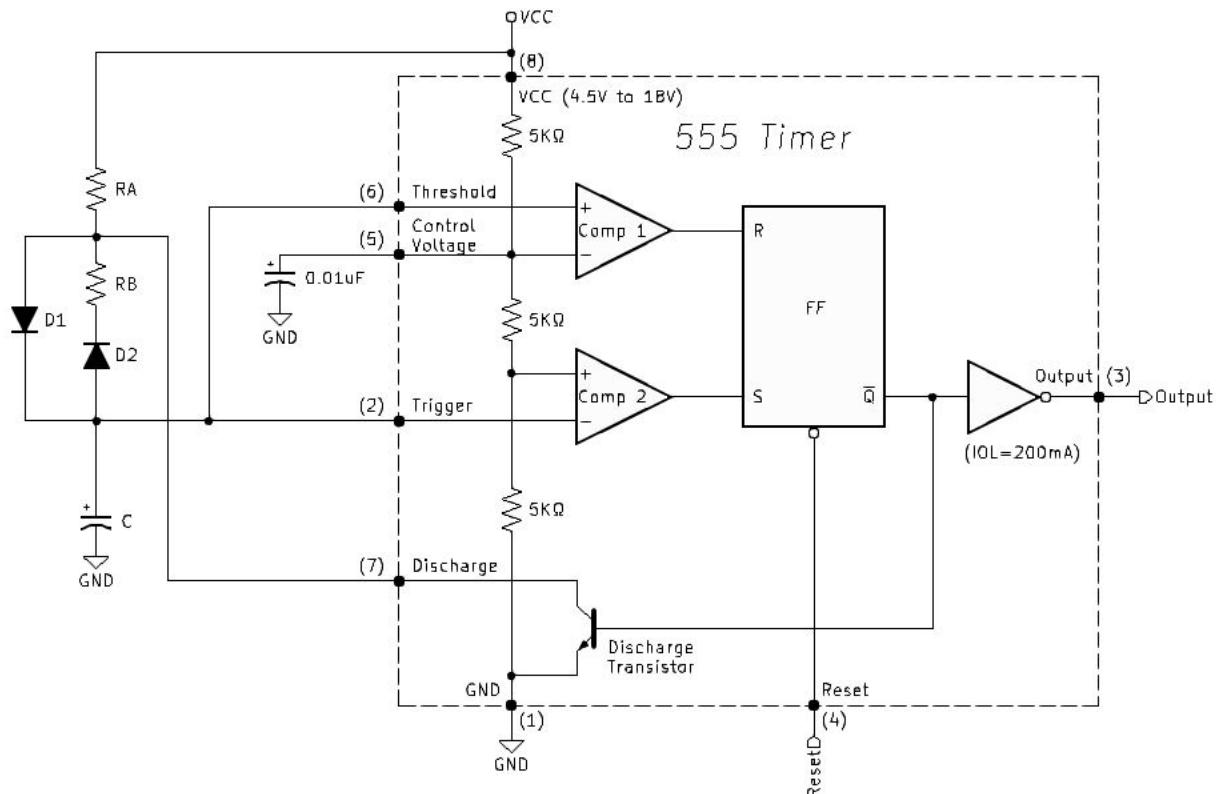


Figure 10.10: Adjustable Duty Cycle 555 Timer Astable Circuit

The Adjustable Duty Cycle Circuit of Figure 10.10 will operate similarly to the standard 555 Timer Astable Multivibrator circuit previously analyzed. The main difference is that

the charge path, which determines the Pulse Width of the output, is now through RA and D1 and the discharge path is through D2 and RB. Technically, D2 is not necessary however, it is useful when designing for 50% duty cycle outputs to balance the charge and discharge paths allowing for the RA and RB resistances to be equal value.

10.7.7 Pulse Width (Charge Time) Formula Derivation

During the charge cycle, we know that the output is high and the capacitor will charge through RA and D1 from $\frac{1VCC}{3}$ to $\frac{2VCC}{3}$.

- $VC = V_{fin} - (V_{fin} - V_{in})e^{\frac{-t}{RA \times C}}$
- $\frac{2VCC}{3} = (VCC - VD1) - ((VCC - VD1) - \frac{1VCC}{3})e^{\frac{-PW}{RA \times C}}$
- $\frac{2VCC}{3} - (VCC - VD1) = -((VCC - VD1) - \frac{1VCC}{3})e^{\frac{-PW}{RA \times C}}$
- $\frac{2VCC}{3} - (VCC - VD1) = -(VCC - VD1) + \frac{1VCC}{3}e^{\frac{-PW}{RA \times C}}$
- $\frac{2VCC}{3} - (VCC - VD1) = (-VCC + VD1 + \frac{1VCC}{3})e^{\frac{-PW}{RA \times C}}$
- $\frac{2VCC}{3} - (\frac{3VCC}{3} - \frac{3VD1}{3}) = (-\frac{3VCC}{3} + \frac{3VD1}{3} + \frac{1VCC}{3})e^{\frac{-PW}{RA \times C}}$
- $\frac{2VCC}{3} - \frac{3VCC}{3} + \frac{3VD1}{3} = (-\frac{3VCC}{3} + \frac{3VD1}{3} + \frac{1VCC}{3})e^{\frac{-PW}{RA \times C}}$
- $\frac{2VCC - 3VCC + 3VD1}{3} = (\frac{-3VCC + 3VD1 + 1VCC}{3})e^{\frac{-PW}{RA \times C}}$
- $\frac{-1VCC + 3VD1}{3} = (\frac{-2VCC + 3VD1}{3})e^{\frac{-PW}{RA \times C}}$
- $\frac{-1VCC + 3VD1}{3} \times \frac{3}{-2VCC + 3VD1} = e^{\frac{-PW}{RA \times C}}$
- $\frac{-1VCC + 3VD1}{-2VCC + 3VD1} = e^{\frac{-PW}{RA \times C}}$
- $\frac{-1VCC + 3(0.7)}{-2VCC + 3(0.7)} = e^{\frac{-PW}{RA \times C}}$
- $\frac{-1VCC + 2.1}{-2VCC + 2.1} = e^{\frac{-PW}{RA \times C}}$
- $\frac{1VCC - 2.1}{2VCC - 2.1} = e^{\frac{-PW}{RA \times C}}$
- $LN[\frac{1VCC - 2.1}{2VCC - 2.1}] = \frac{-PW}{RA \times C}$
- $LN[\frac{VCC - 2.1}{2VCC - 2.1}] \times (RA \times C) = -PW$
- ✓ $PW = -[(LN[\frac{VCC - 2.1}{2VCC - 2.1}]) \times (RA \times C)]$

10.7.8 Pulse Space (Discharge Time) Formula Derivation

During the discharge cycle, we know that the output is low and the capacitor will discharge through RB and D2 from $\frac{2VCC}{3}$ to $\frac{1VCC}{3}$.

- $VC = V_{fin} - (V_{fin} - V_{in})e^{\frac{-t}{RC}}$
- $\frac{1VCC}{3} = VD2 - (VD2 - \frac{2VCC}{3})e^{\frac{-PS}{(RB)C}}$
- $\frac{1VCC}{3} - VD2 = -(VD2 - \frac{2VCC}{3})e^{\frac{-PS}{(RB)C}}$
- $\frac{1VCC}{3} - \frac{3VD2}{3} = (-\frac{3VD2}{3} + \frac{2VCC}{3})e^{\frac{-PS}{(RB)C}}$
- $\frac{1VCC-3VD2}{3} = (\frac{-3VD2+2VCC}{3})e^{\frac{-PS}{(RB)C}}$
- $\frac{1VCC-3VD2}{3} \times \frac{3}{-3VD2+2VCC} = e^{\frac{-PS}{(RB)C}}$
- $\frac{1VCC-3VD2}{-3VD2+2VCC} = e^{\frac{-PS}{(RB)C}}$
- $\frac{1VCC-3VD2}{2VCC-3VD2} = e^{\frac{-PS}{(RB)C}}$
- $\frac{1VCC-3(0.7)}{2VCC-3(0.7)} = e^{\frac{-PS}{(RB)C}}$
- $\frac{1VCC-2.1}{2VCC-2.1} = e^{\frac{-PS}{(RB)C}}$
- $LN[\frac{1VCC-2.1}{2VCC-2.1}] = \frac{-PS}{(RB)C}$
- $LN[\frac{VCC-2.1}{2VCC-2.1}] \times (RB \times C) = -PS$

✓ $PS = -[(LN[\frac{VCC-2.1}{2VCC-2.1}]) \times (RB \times C)]$

* Notice the Pulse Space formula is the same formula as the Pulse Width formula the only difference is the substitution of RB for RA.

10.7.9 Design Example 1

Given:

Design an Adjustable Duty Cycle 555 Timer Astable Circuit to produce a 10Khz 50% Duty Cycle signal using 5 volts for VCC and a $0.1\mu F$ capacitor.

Find:

- RA
- RB

Solve:

- Solve for RA:

$$\begin{aligned} \circ & PW = -[(LN[\frac{VCC-2.1}{2VCC-2.1}]) \times (RA \times C)] \\ \circ & \frac{PW}{(LN[\frac{VCC-2.1}{2VCC-2.1}]) \times C} = -(RA) \\ \circ & RA = \frac{-PW}{(LN[\frac{VCC-2.1}{2VCC-2.1}]) \times C} \\ * & PW = \frac{1}{2F} \\ \circ & PW = \frac{1}{2 \times 10Khz} \\ \circ & PW = 50\mu S \\ \circ & RA = \frac{-50\mu S}{(LN[\frac{5-2.1}{2(5)-2.1}]) \times 0.1\mu F} \\ \circ & RA = \frac{-50\mu S}{(LN[\frac{2.9}{10-2.1}]) \times 0.1\mu F} \\ \circ & RA = \frac{-50\mu S}{(LN[\frac{2.9}{7.9}]) \times 0.1\mu F} \\ \circ & RA = \frac{-50\mu S}{(-1.00215) \times 0.1\mu F} \\ \circ & RA = \frac{-50\mu S}{-100.215 \times 10^{-9} S} \\ \checkmark & RA = 498.927\Omega \end{aligned}$$

- Solve for RB:

$$\begin{aligned} \circ & PS = -[(LN[\frac{VCC-2.1}{2VCC-2.1}]) \times (RB \times C)] \\ \circ & \frac{PS}{(LN[\frac{VCC-2.1}{2VCC-2.1}]) \times C} = -(RB) \\ \circ & RB = \frac{-PS}{(LN[\frac{VCC-2.1}{2VCC-2.1}]) \times C} \\ * & PS = \frac{1}{2F} \\ \circ & PS = \frac{1}{2 \times 10Khz} \\ \circ & PS = 50\mu S \end{aligned}$$

- $RB = \frac{-50\mu S}{(LN[\frac{5-2.1}{2(5)-2.1}]) \times 0.1\mu F}$
- $RB = \frac{-50\mu S}{(LN[\frac{2.9}{10-2.1}]) \times 0.1\mu F}$
- $RB = \frac{-50\mu S}{(LN[\frac{2.9}{7.9}]) \times 0.1\mu F}$
- $RB = \frac{-50\mu S}{(-1.00215) \times 0.1\mu F}$
- $RB = \frac{-50\mu S}{-100.215 \times 10^{-9} S}$
- ✓ $RB = 498.927\Omega$

10.7.10 Design Example 2

Given:

Design an Adjustable Duty Cycle 555 Timer Astable Circuit to produce an output waveform with a Pulse Space equal to 1.5mS and a Pulse Width of 20mS using 5 volts for VCC and a $10\mu F$ capacitor.

Find:

- RA
- RB

Solve:

- Solve for RA:

- $RA = \frac{-PW}{(LN[\frac{VCC-2.1}{2VCC-2.1}]) \times C}$
- $RA = \frac{-1.5mS}{(LN[\frac{5-2.1}{2(5)-2.1}]) \times 10\mu F}$
- $RA = \frac{-1.5mS}{(LN[\frac{2.9}{10-2.1}]) \times 10\mu F}$
- $RA = \frac{-1.5mS}{(LN[\frac{2.9}{7.9}]) \times 10\mu F}$
- $RA = \frac{-1.5mS}{(-1.00215) \times 10\mu F}$
- $RA = \frac{-1.5mS}{-10.0215 \times 10^{-6} S}$
- ✓ $RA = 149.678\Omega$

- Solve for RB:

- $RB = \frac{-PS}{(LN[\frac{VCC-2.1}{2VCC-2.1}]) \times C}$
- $RB = \frac{-20mS}{(LN[\frac{5-2.1}{2(5)-2.1}]) \times 10\mu F}$

- $RB = \frac{-20mS}{(LN[\frac{2.9}{10-2.1}]) \times 10\mu F}$
- $RB = \frac{-20mS}{(LN[\frac{2.9}{7.9}]) \times 10\mu F}$
- $RB = \frac{-20mS}{(-1.00215) \times 10\mu F}$
- $RB = \frac{-20mS}{-10.0215 \times 10^{-6} S}$
- ✓ $RA = 1.996 K\Omega$

10.8 555 Timer Monostable Multivibrator:

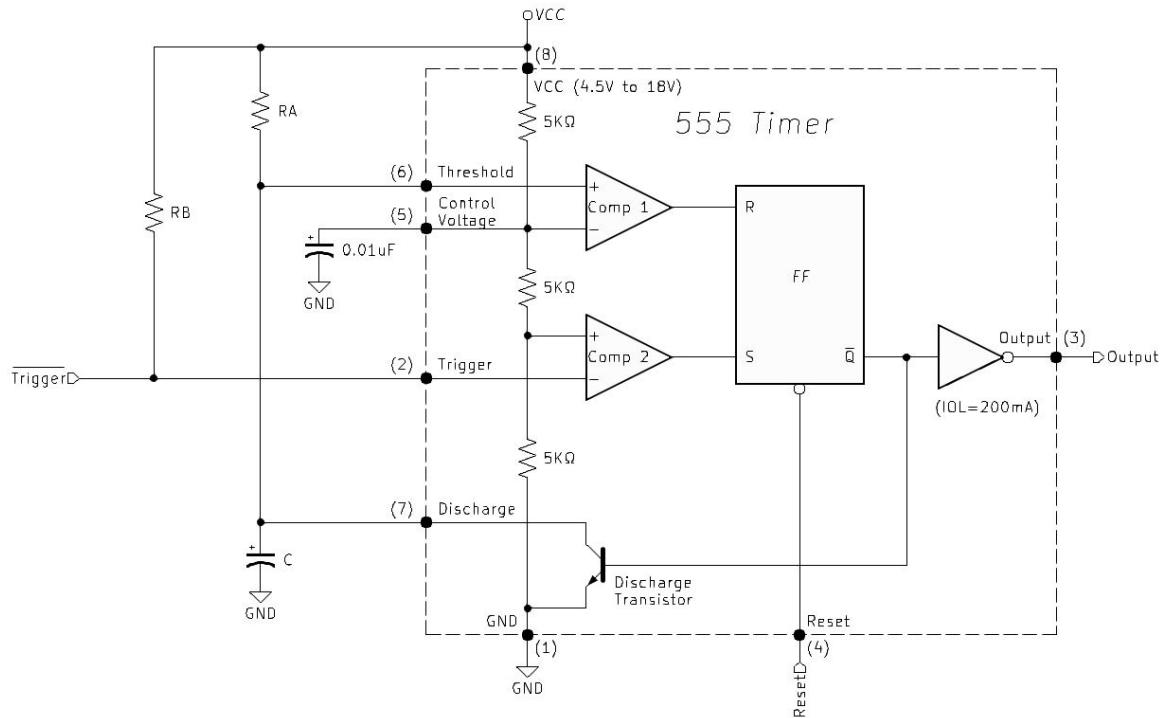


Figure 10.11: Monostable Multivibrator circuit using a 555 Timer

10.8.1 Introduction

The 555 timer monostable multivibrator is an essential electronic circuit configuration that generates a single, precise output pulse in response to an external trigger signal. Utilizing the versatile 555 timer IC, this monostable mode operation involves the circuit transitioning from its stable state to an unstable state upon receiving a trigger. The duration of the output pulse is determined by external components, typically a resistor and capacitor, allowing for adjustable and accurate timing. After the pulse is completed, the circuit automatically returns to its stable state, ready to be triggered again. The 555 timer monostable

multivibrator is widely used in applications such as pulse generation, timing delays, and debouncing switches, providing a reliable and straightforward solution for creating controlled timing events in various electronic systems.

10.8.2 Circuit Analysis

- Internally, VCC is divided across three $5\text{K}\Omega$ resistors. Comparator 1 will have $\frac{2VCC}{3}$ on its minus input. Comparator 2 will have $\frac{1VCC}{3}$ on its plus input.
- Assuming that the 555 timers internal Flip Flop power up in the Set condition, the output will be high, the Discharge Transistor will be off, and the Capacitor voltage will begin to charge through RA. Initially, Comparator 1 will rail negative and Comparator 2 will rail negative resulting in a Hold state for the Flip Flop.
- As the capacitor voltage charges, or increases, through RA it will eventually cross the $\frac{2VCC}{3}$ threshold. This will cause Comparator 1 to rail positive and will result in a Reset condition for the Flip Flop, \bar{Q} will go high turning on the Discharge Transistor and the Output will go low via the inverter.
- With the Discharge Transistor on, ground is placed across the capacitor. This will cause the capacitor to discharge rapidly to 0V. Comparator 1 will rail low with Comparator 2 already low, the Flip Flop to enter a Hold state.
- (Stable State) The output is now low and the only thing that will change the output is a *Trigger* signal on pin 2.
- Note, the *Trigger* pulse needs to be shorter, or faster, than the desired pulse width of the Monstables output.

10.8.3 Pulse Width Calculations

- $VC = V_{fin} - (V_{fin} - V_{in})e^{\frac{-t}{RC}}$
 - $VC = \frac{2VCC}{3}$
 - $V_{fin} = VCC$
 - $V_{in} = 0V$
 - $t = PW$
 - $R = RA$
 - $C = C$
- $\frac{2VCC}{3} = VCC - (VCC - 0)e^{\frac{-PW}{RA \times C}}$
 - $\frac{2VCC}{3} - VCC = -(VCC)e^{\frac{-PW}{RA \times C}}$
 - $\frac{2VCC}{3} - \frac{3VCC}{3} = (-VCC)e^{\frac{-PW}{RA \times C}}$

- $\frac{-1VCC}{3} = (-VCC)e^{\frac{-PW}{RA \times C}}$
- $\frac{-1VCC}{3(-VCC)} = e^{\frac{-PW}{RA \times C}}$
- $\frac{-1VCC}{-3VCC} = e^{\frac{-PW}{RA \times C}}$
- $\frac{1}{3} = e^{\frac{-PW}{RA \times C}}$
- $LN(\frac{1}{3}) = \frac{-PW}{RA \times C}$
- $-1.0986 = \frac{-PW}{RA \times C}$
- $-1.0986 \times (RA \times C) = -PW$
- ✓ $PW = 1.0986(RA \times C)$

10.8.4 Design Example 1

Design a Monostable Multivibrator Circuit using a 555 Timer to produce a 5-second pulse when triggered.

Given:

- $VCC = 5V$
- $RB = 10K\Omega$
- $C = 100\mu F$
- $PW = 5 \text{ seconds}$

Find:

- RA

Solve:

- $PW = 1.0986(RA \times C)$
 - $\frac{PW}{1.0986 \times C} = (RA)$
 - $RA = \frac{PW}{1.0986 \times C}$
- $RA = \frac{PW}{1.0986 \times C}$
 - $RA = \frac{5\text{sec}}{1.0986 \times 100\mu F}$
 - $RA = \frac{5\text{sec}}{1.0986 \times 10^{-6}}$
 - ✓ $RA = 45.512K\Omega$

10.8.5 Trigger Circuits

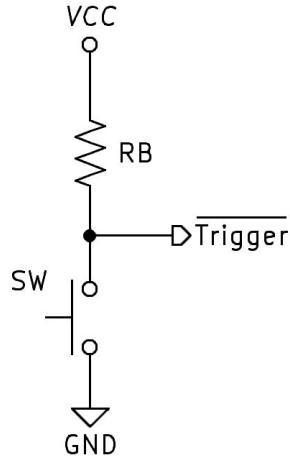


Figure 10.12: Monostable Multivibrator Trigger Circuit 1, the monostable will see the switch bounce.

The Trigger Circuit Figure 10.12. can be used to trigger a 555 Timer Monostable circuit with an output Pulse Width greater than or equal to ten times larger than the switch bounce.

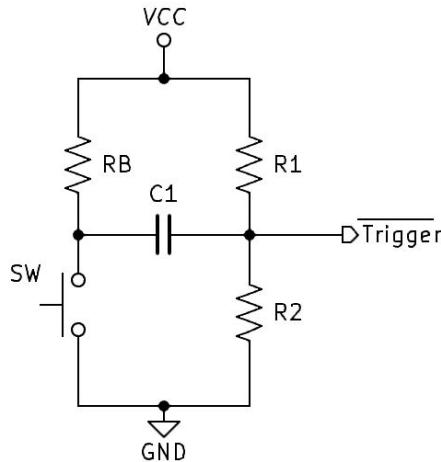
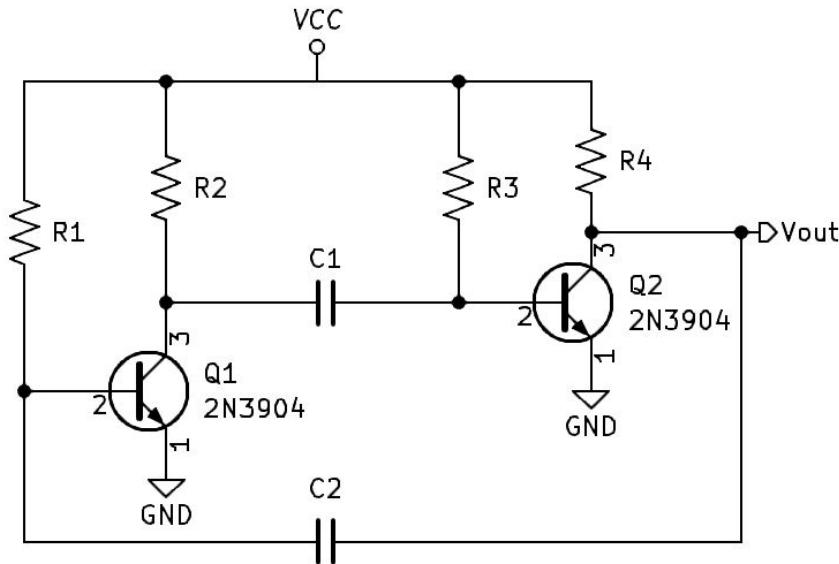


Figure 10.13: Monostable Multivibrator Trigger Circuit 2, no switch bounce and trigger pulse-width can be adjusted

The Trigger Circuit Figure 10.13. can be used to trigger a 555 Timer Monostable circuit with an output Pulse Width less than or equal to ten times larger than the switch bounce.

10.9 Practice Questions:

1. Design a BJT Astable Multivibrator.



Given: $V_{CC} = 18V$, $IC_{sat} = 30mA$, $PRF = 15Khz$, $DC = 58\%$, $Beta_{Q1} = 30$, $Beta_{Q2} = 50$.

Find: $R1$, $R2$, $R3$, $R4$, $C1$, $C2$.

Solve:

$$R1 = \underline{\hspace{2cm}}$$

$$R2 = \underline{\hspace{2cm}}$$

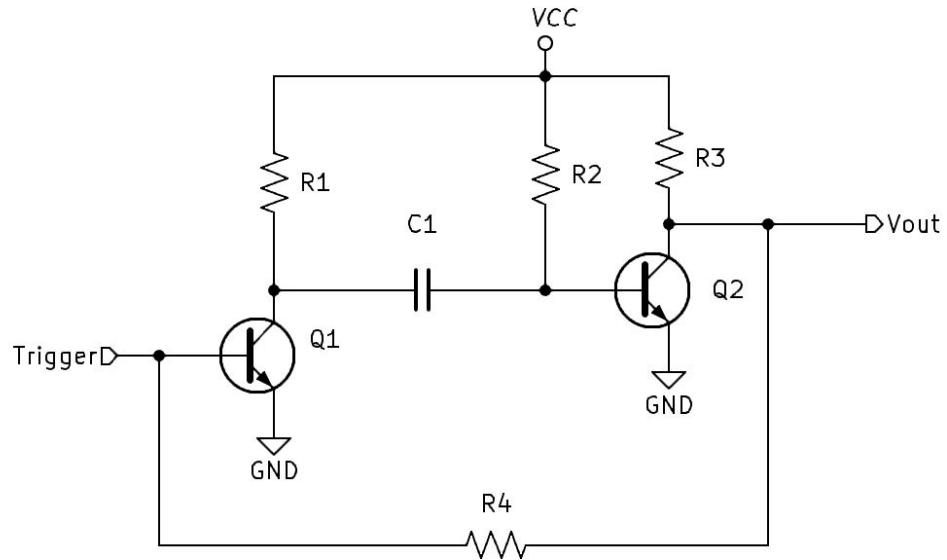
$$R3 = \underline{\hspace{2cm}}$$

$$R4 = \underline{\hspace{2cm}}$$

$$C1 = \underline{\hspace{2cm}}$$

$$C2 = \underline{\hspace{2cm}}$$

2. Design a BJT Monostable Multivibrator.



Given: $VCC = 10V$, $IC_{sat} = 10mA$, $PW = 2.00S$, $Beta_{Q1} = 120$, $Beta_{Q2} = 60$
(Make $IB = 2 \times IB_{min}$).

Find: $R1$, $R2$, $R3$, $R4$, $C1$, $C2$.

Solve:

$$R1 = \underline{\hspace{2cm}}$$

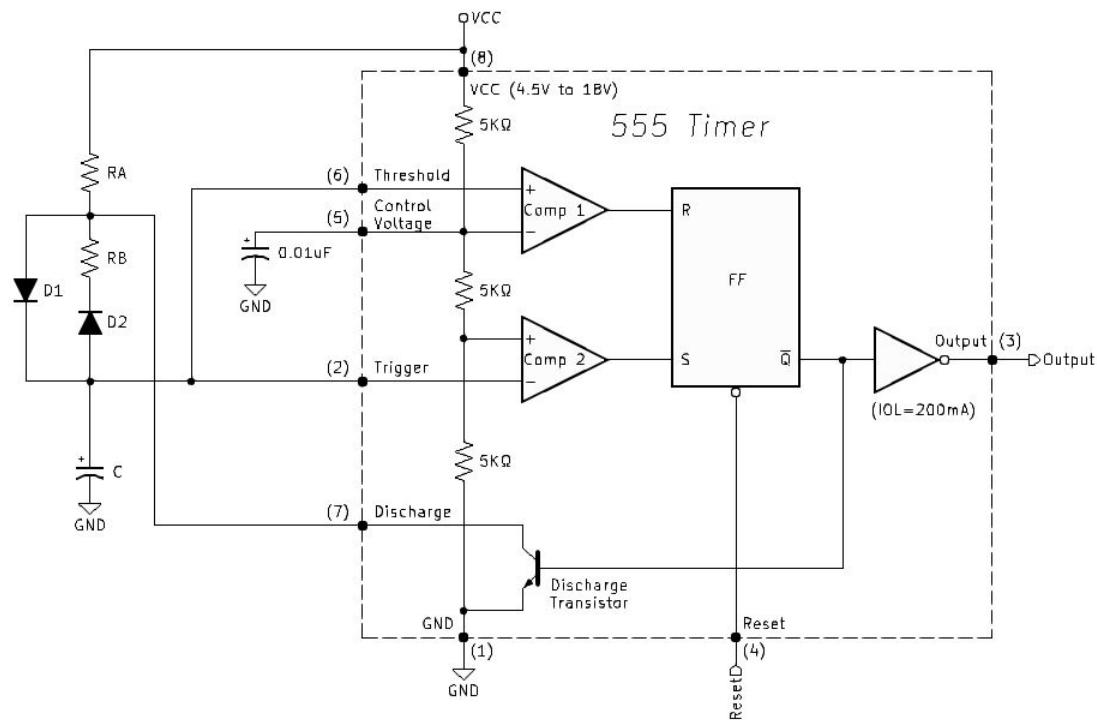
$$R2 = \underline{\hspace{2cm}}$$

$$R3 = \underline{\hspace{2cm}}$$

$$R4 = \underline{\hspace{2cm}}$$

$$C1 = \underline{\hspace{2cm}}$$

3. Design an Astable Multivibrator using a 555 Timer.



Given: $V_{CC} = 10V$, $PW = 38.443\mu S$, $PS = 1.636\mu S$. $C1 = 0.001\mu F$

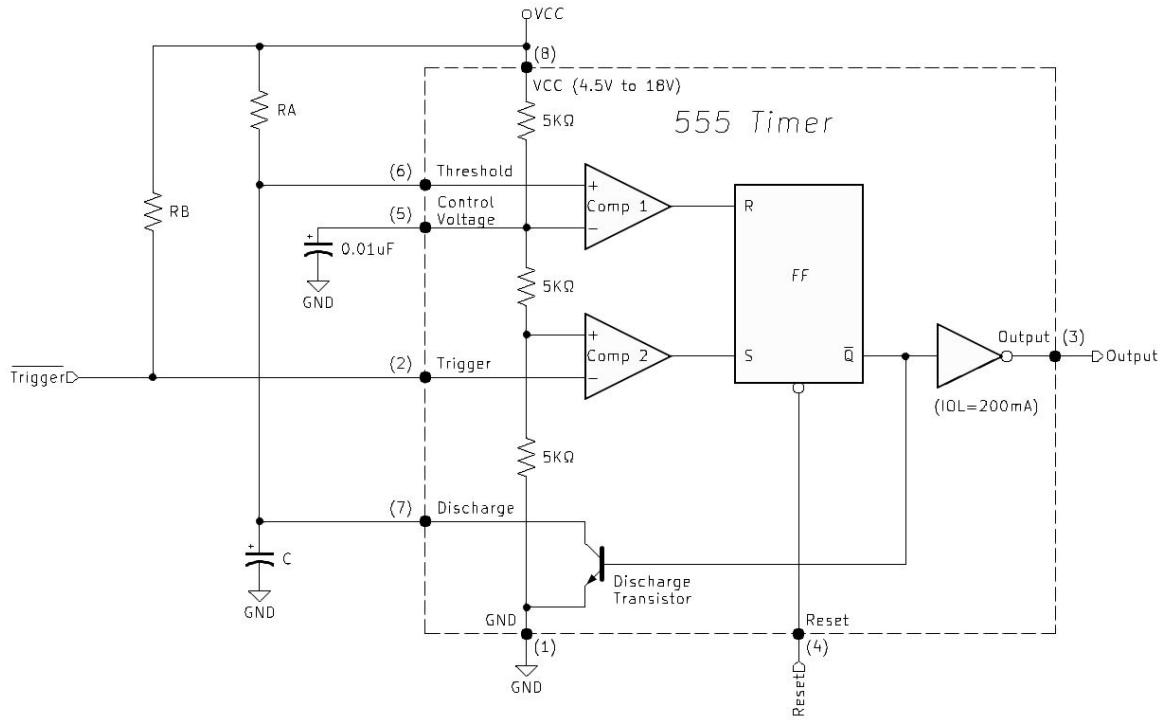
Find: $R1$, $R2$.

Solve:

$$R1 = \underline{\hspace{2cm}}$$

$$R2 = \underline{\hspace{2cm}}$$

4. Analyze a Monostable Multivibrator using a 555 Timer.



Given: $VCC = 15V$, $RA = 32K\Omega$, $RB = 10K\Omega$, $C = 10nF$, (Trigger pulse occurs every $500\mu S$).

Find: PW , DC .

Solve:

$$PW = \text{_____}$$

$$DC = \text{_____}$$

10.10 Answers:

$$1. \quad R1 = 17.3K\Omega$$

$$R2 = 600\Omega$$

$$R3 = 28.8K\Omega$$

$$R4 = 600\Omega$$

$$C1 = 1.9nF$$

$$C2 = 2.3nF$$

$$2. \quad R1 = 1K\Omega$$

$$R2 = 27K\Omega$$

$$R3 = 1K\Omega$$

$$R4 = 54.8K\Omega$$

$$C1 = 99.932\mu F$$

$$3. \quad R1 = 47K\Omega$$

$$R2 = 2K\Omega$$

$$4. \quad PW = 351.566\mu S$$

$$DC = 70.311\%$$

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