PCB

Board size: 90.0x27.0 mm (3.54x1.06 inches)

- This is the size of the rectangle that contains the board
- Thickness: 1.6 mm (63 mils)
- Material: FR4
- Finish: None
- Layers: 2
- Copper thickness: 35 µm

Solder mask: TOP / BOTTOM

- Color: Green

Silk screen: TOP / BOTTOM

- Color: White

Stackup:

Name	Type	Color	Thickness [µm]	Material	Er	Loss tan
F.SilkS	Top Silk Screen					
F.Paste	Top Solder Paste					
F.Mask	Top Solder Mask		10			
F.Cu	copper		35			
dielectric 1	core		1510	FR4	4.5	0.020
B.Cu	copper		35			
B.Mask	Bottom Solder Mask		10			
B.Paste	Bottom Solder Paste					
B.SilkS	Bottom Silk Screen					

Important sizes

Clearance: 0.2 mm (8 mils)

Track width: 0.7 mm (28 mils)

- By design rules: 0.6 mm (24 mils)

Drill: 0.9 mm (35 mils)

- Vias: N/A mm (N/A mils) [Design: 0.4 mm (16 mils)]
- Pads: 0.9 mm (35 mils)
- The above values are real drill sizes, they add 0.1 mm (4 mils) to plated holes (PTH)

Via: N/A/N/A mm (N/A/N/A mils)

- By design rules: 0.5/0.3 mm (20/12 mils)
- Micro via: yes [0.2/0.1 mm (8/4 mils)]
- Buried/blind via: yes
- Total: 0 (thru: 0 buried/blind: 0 micro: 0)

Outer Annular Ring: 0.2 mm (8 mils)

- By design rules: 0.2 mm (8 mils)

Eurocircuits class: 4A - Using min drill 0.9 mm for an OAR of 0.2 mm

General stats

Components count: (SMD/THT)

- Top: 12/3 (SMD + THT)
- Bottom: 12/6 (SMD + THT)

Defined tracks:

- 0.25 mm (10 mils)
- 0.6 mm (24 mils)
- 0.7 mm (28 mils)

Used tracks:

- 0.7 mm (28 mils) (132) defined: yes

Defined vias:

Used vias:

Holes (excluding vias):

- 0.8 mm (31 mils) (16)
- 1.0 mm (39 mils) (38)
- 2.5 mm (98 mils) (12)

Oval holes:

Drill tools (including vias and computing adjusts and rounding):

- 0.9 mm (35 mils) (16)
- 1.0 mm (39 mils) (6)
- 1.1 mm (43 mils) (32)

- 2.5 mm (98 mils) (12)

Solder paste stats:

Using a paste with 87.75 % alloy, that has an specific gravity for the alloy of 7.4 g/cm³ and 1.0 g/cm³ for the flux. This paste has an specific gravity of 4.15 g/cm³.

The stencil thickness is 0.12 mm.

Side	Pads with paste	Area [mm²]	Paste [g]
Top	24	48.68	0.24
Bottom	24	38.91	0.19
Total	48	87.59	0.44

Note: this is just an approximation to the theoretical value. Margins of the solder mask and waste aren't computed.

Schematic

Schematic in SVG format

PCB Layers

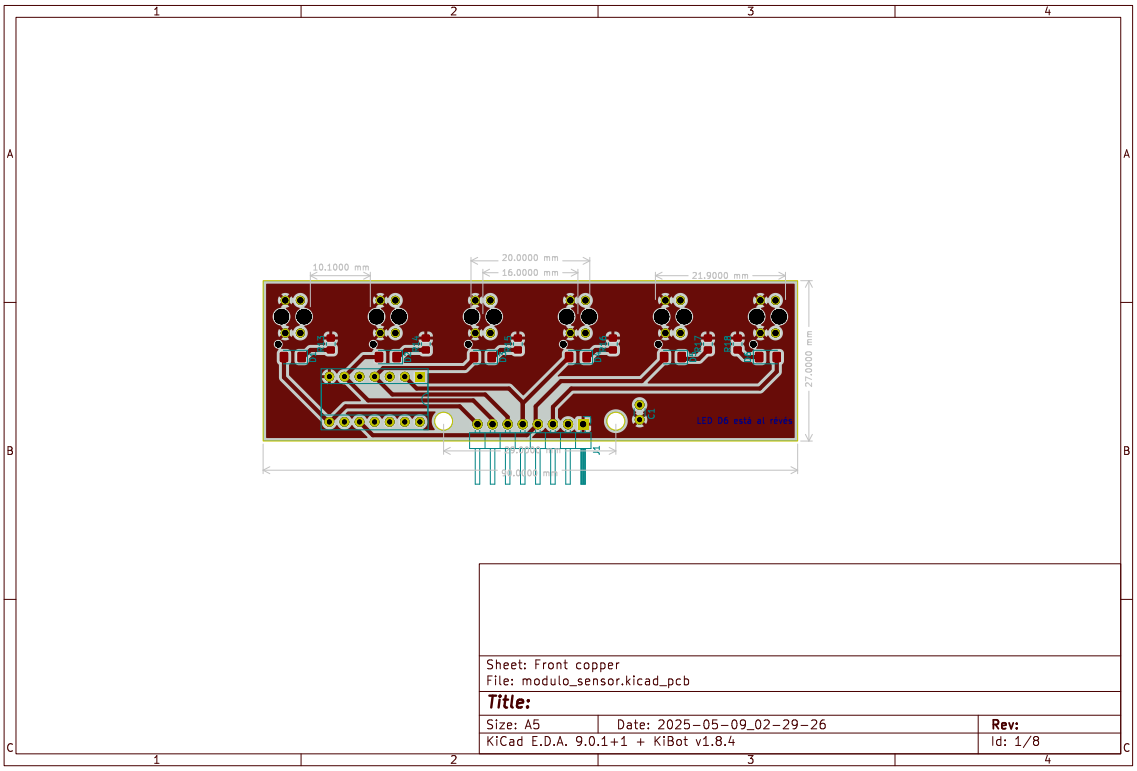

Figure 1: PCB Front copper

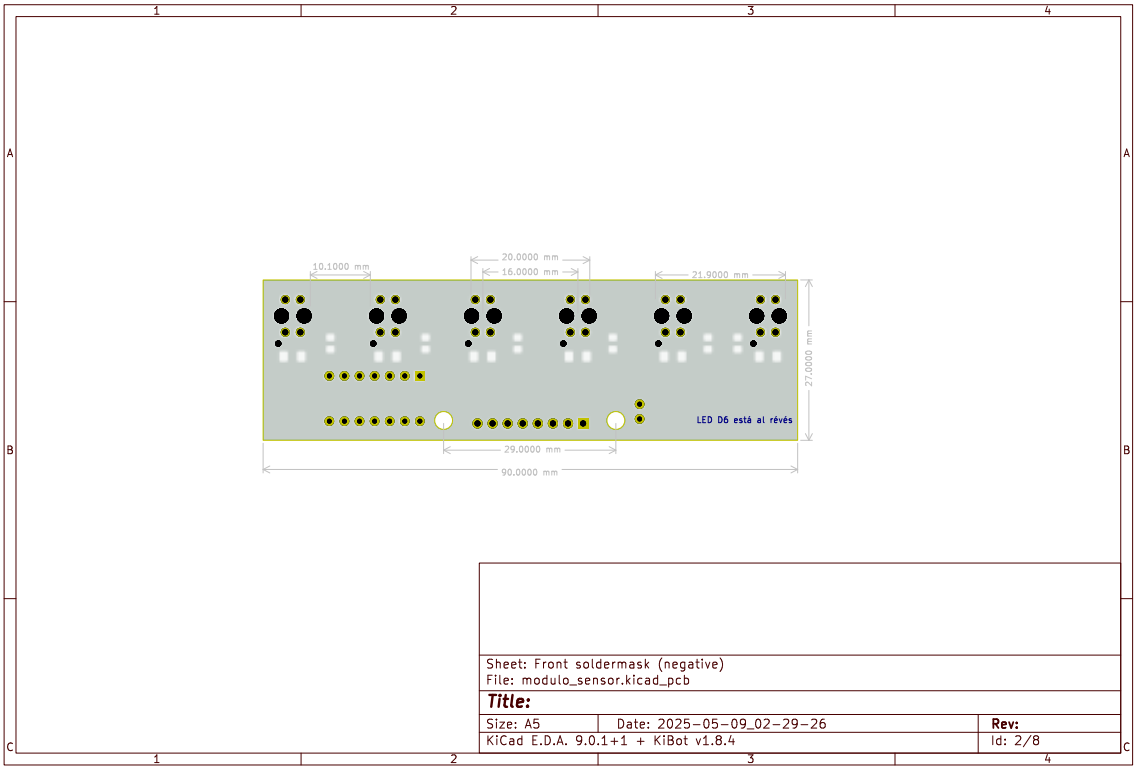

Figure 2: PCB Front soldermask (negative)

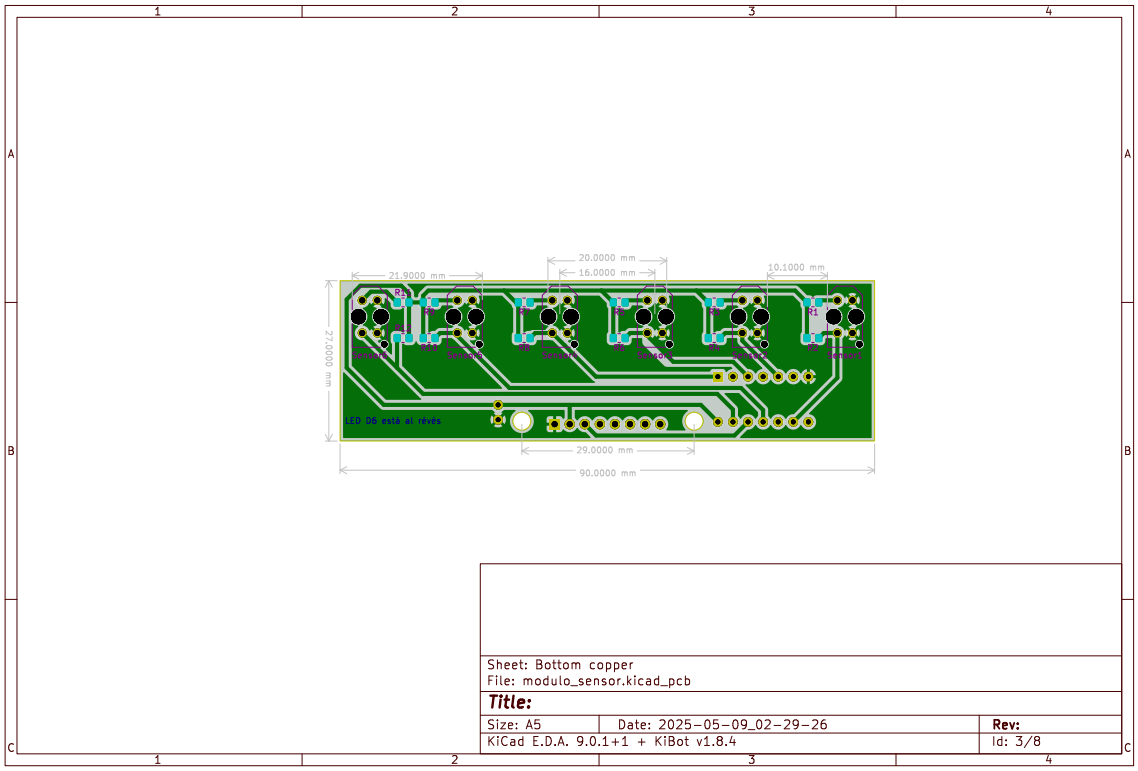

Figure 3: PCB Bottom copper

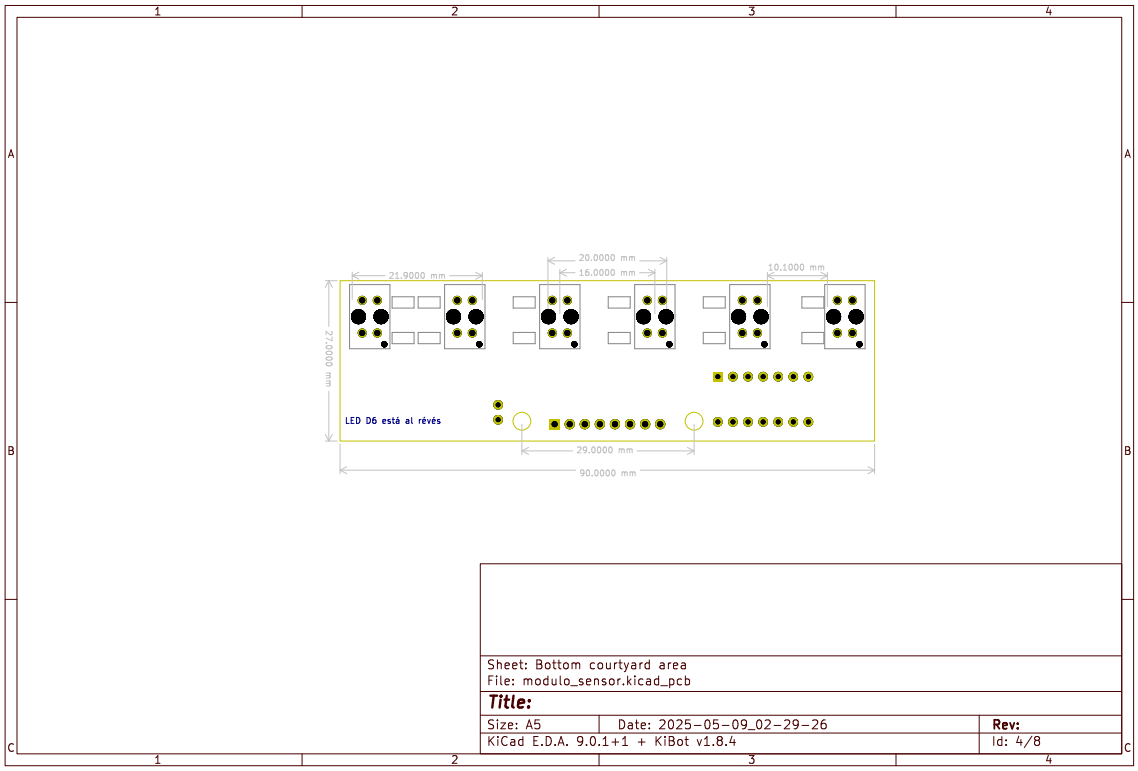

Figure 4: PCB Bottom courtyard area

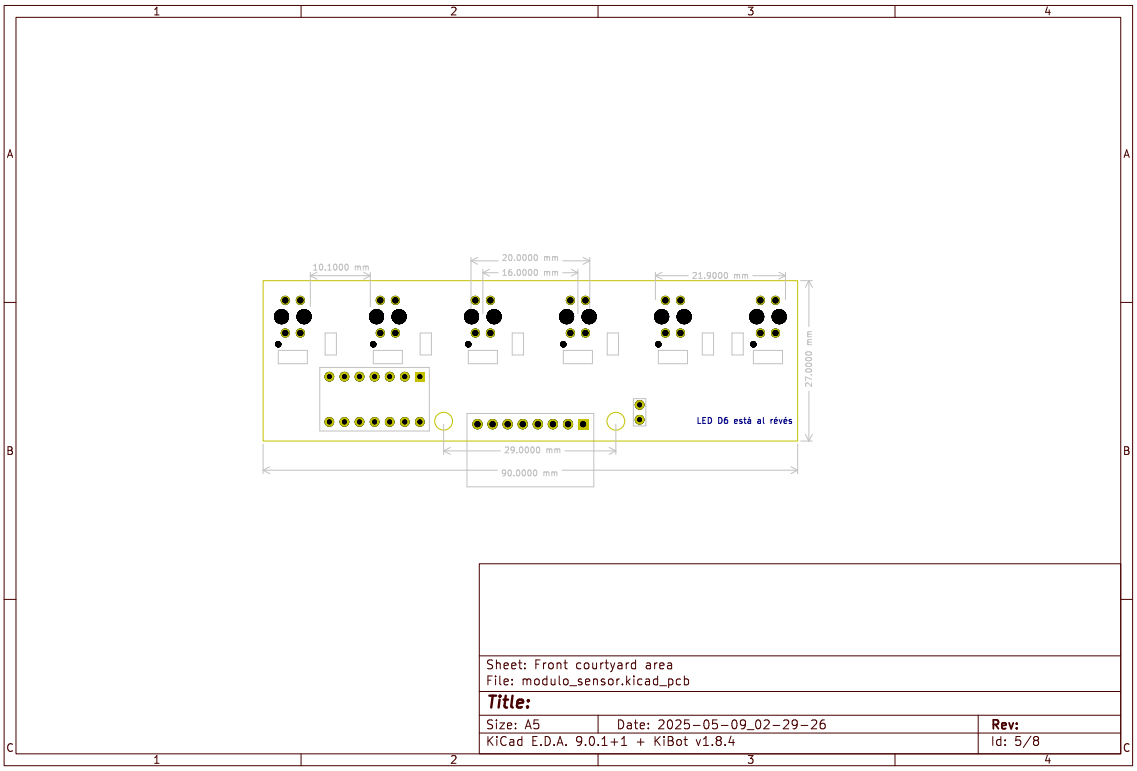

Figure 5: PCB Front courtyard area

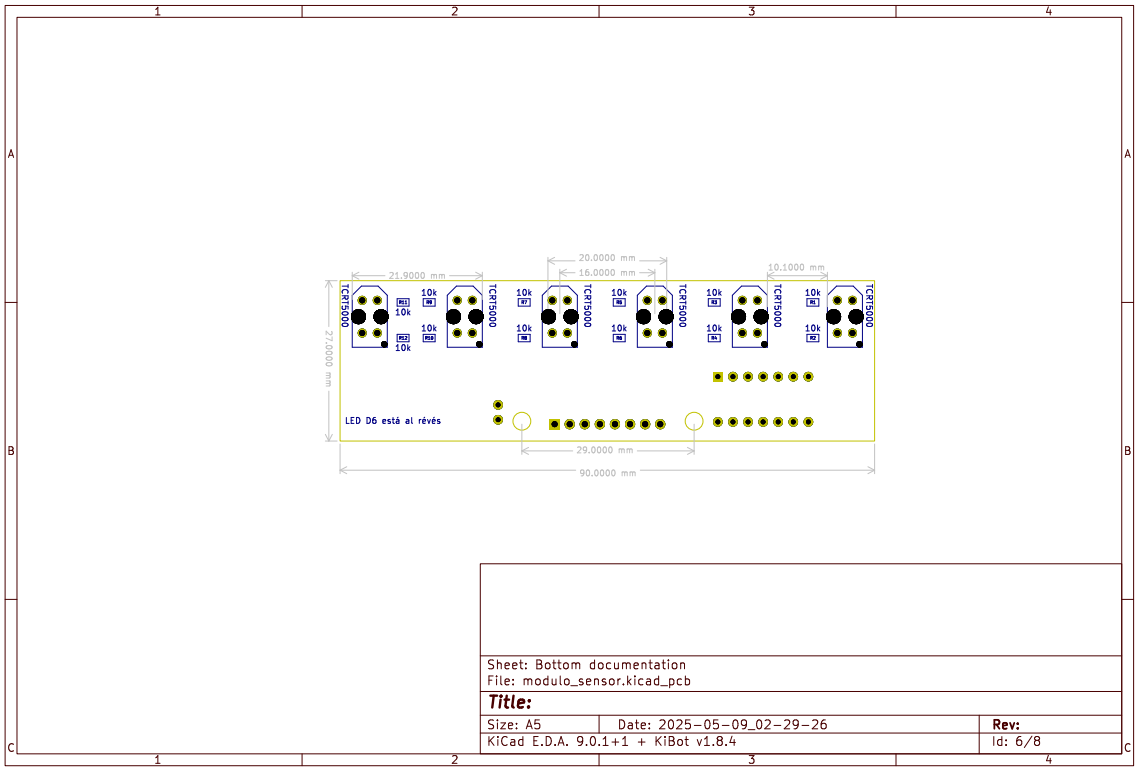

Figure 6: PCB Bottom documentation

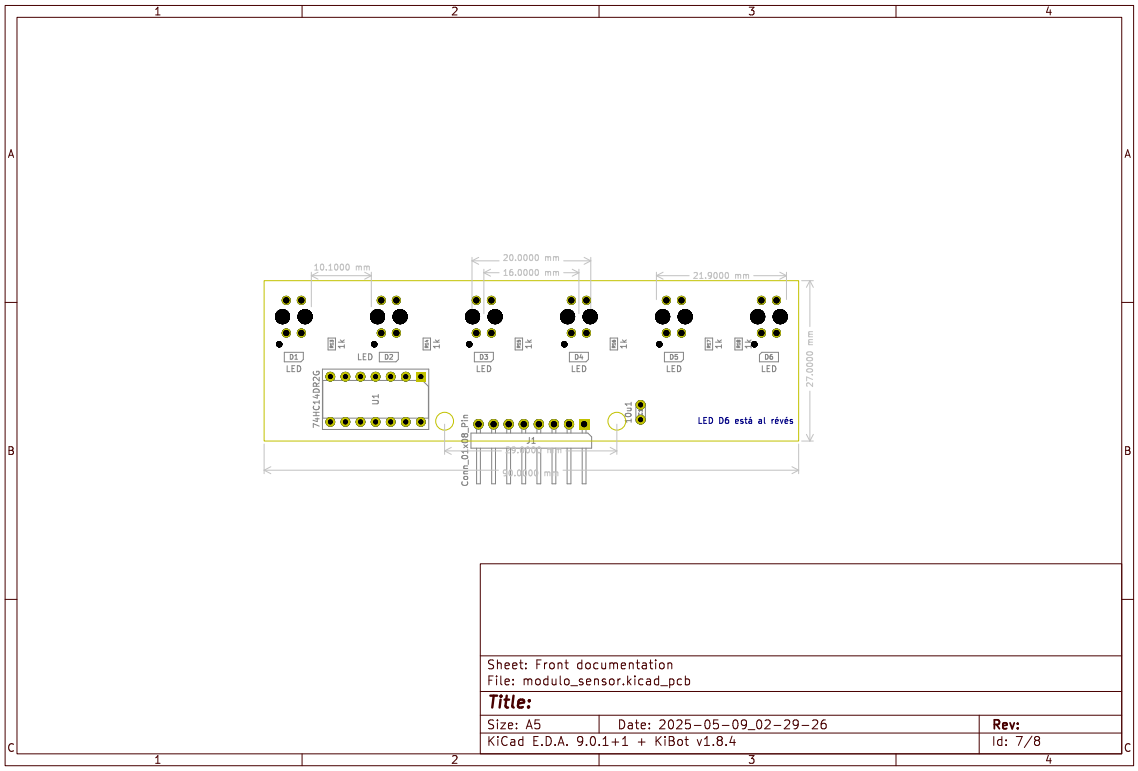

Figure 7: PCB Front documentation

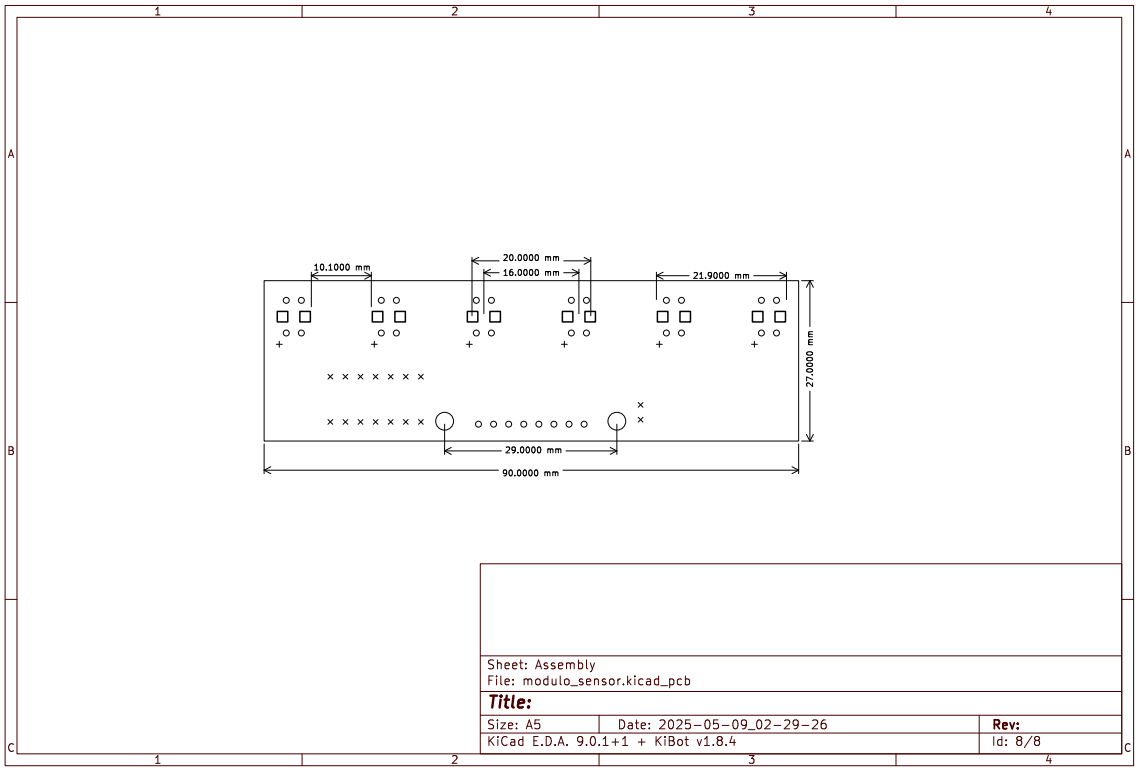

Figure 8: PCB Assembly