Topic: Computer System Architecture

Subtopic: Binary arithmetics

Q: In the floating-point IEEE 754 format:

A: there is more than one sign bit
B: the sign bit is 1 for positive numbers
C: the sign bit is either 1 or 0 depending on whether the mantissa is even or odd
D: the sign bit is 0 for positive numbers

Q: What happens to the binary representation of a number when it gets multiplied by 2?

A: The bits get shifted to the left
B: The bits are shuffled
C: The bits get flipped
D: The bits get shifted to the right

Q: An advantage of the floating-point system for representing fractional numbers is that:

A: the representable magnitude is very large
B: with the same encoding we can represent very large or very small numbers, depending on the
C: any number fits into 32 bits
D: the precision is very high

Q: Which is the two’s complement representation of the number -10, using 8 bits?

A: 11110110
B: 00001010
C: 10101010
D: 11100111

Q: Which is the two’s complement representation of the number -42, using 8 bits?

A: 11100111

B: 11010110
C: 10101010
D: 00101010

Q: In the two’s complement encoding for negative numbers:

A: very high precision is achieved
B: one needs two times the number of bits
C: there is only one representation of zero
D: even numbers are represented better

Q: An advantage of the two’s complement scheme for negative numbers is:

A: the set of representable numbers is very large
B: any number of bits can be used
C: the precision is very high
D: there is only one representation of zero

Q: Which is the result of the binary operation 001101 + 110010?

A: 000000
B: 111000
C: 111111
D: 10101

Q: Which is the two’s complement representation of the number -1, using 8 bits?

A: 11101111
B: 11100001
C: 11110000
D: 11111111

Q: Which is the result of the binary operation 111000 + 000111?

A: 000000

B: 111000

C: 010101

D: 111111

Q: What happens to a binary number when it is shifted to the left by one position? (for exa

A: the value is divided by 2

B: the value is raised to the power of 2

C: the value is multiplied by 2

D: the new value is unrelated

Q: Which is the result of the binary operation 111001 + 111001?

A: 1110010

B: 1110000

C: 0000001

D: 0101010

Q: In the floating-point IEEE 754 format:

A: the distance between two consecutive numbers is variable

B: there is no way to represent the concept of infinity

C: the distance between two consecutive numbers is constants

D: there is only one representation of the number zero

Subtopic: Logic gates and boolean algebra

Q: If A=0 e B=0, which is the result of the Boolean operations A AND B, A OR B, and A XO

A: 0, 0, 0

B: 0, 1, 0

C: 1, 1, 1

D: 1, 0, 1

Q: Which of these combinations of gates can be used to build a Set-Reset flip-flop?

A: two XOR gates
B: two AND gates
C: an OR gate and an AND gate
D: two NAND gates

Q: If A=0 e B=1, which is the result of the Boolean operations A NAND B, A NOR B, and A X

A: 0, 1, 0
B: 1, 1, 1
C: 1, 1, 0
D: 1, 0, 1

Q: In a Set-Reset flip-flop built with NOR gates, when S=0 and R=0, the circuit:

A: gives output 0
B: stays in the memory configuration
C: gives output 1
D: has unpredictable behavior

Subtopic: The BUS

Q: In the old PCI bus:

A: synchronization of devices happens automatically
B: all the devices were limited by the set 66MHz clock frequency
C: there are multiple clock signals that have to be synchronized together
D: devices do not have to synchronize their access to the bus

Q: With the interrupt I/O mechanism:

A: the CPU interrupts the control flow more frequently
B: the CPU interrupts the control flow at each instruction

C: the CPU waits for I/O operations
D: the CPU interrupts the control flow when I/O is ready

Q: In an asynchronous bus:

A: synchronization of devices happens without a central clock signal
B: there are multiple clock signals that have to be synchronized together
C: devices do not have to synchronize their access to the bus
D: the transitions of the clock signal synchronize all the operations

Q: In the PCI-Express bus:

A: there is no central clock signal
B: all the devices are limited to the same clock frequency
C: the clock frequency is chosen by the operating system
D: the data lines connecting the devices to the host are parallel

Subtopic: Sequential and Combinatorial circuits

Q: A shift register is:

A: a sequential circuit whose output shifts to the right or to the left at each clock cycle
B: a sequential circuit whose output is registered in different ways at each clock cycle
C: a combinatorial circuit that outputs a shifted version of the input
D: a combinatorial circuit that registers user inputs

Q: In a superscalar CPU architecture, performance increases when:

A: there are only few dependencies between the instructions
B: there are enough registers to keep all the needed temporary values
C: there are too many dependencies between the instructions
D: the instructions access memory very often

Q: A counter is:

A: a combinatorial circuit that counts the number of 1s in the inputs
B: a sequential circuit that counts the number of 1s in the inputs
C: a sequential circuit whose output increments at each clock cycle
D: a combinatorial circuit that counts the number of 0s in the inputs

Q: A dynamic memory is:

A: a memory made of capacitors, and it needs to be refreshed periodically
B: a memory used to store information that changes frequently
C: a memory that can be written many times
D: a memory made of flip flops, and it does not need to be refreshed

Q: The cache memory is very especially effective when:

A: nearby data are accessed together
B: the bandwidth of the bus is large enough
C: the CPU frequency is relatively low
D: main memory is built with similar technologies

Q: In a pipelined CPU architecture, performance increases when:

A: the jumps are correctly predicted
B: there are only a few instructions to execute at once
C: only a few registers are used
D: the ALU is given small numbers as inputs

Q: In a pipelined CPU architecture, performance can degrade if:

A: the registers are full
B: the jumps are not correctly predicted
C: there are too many instructions to execute at once
D: the ALU is given too large numbers as inputs

Q: The cache memory is very effective also because of:

A: synchronization of devices happens automatically
B: the transitions of the clock signal synchronize all the operations
C: devices do not have to synchronize their access to the bus
D: there are multiple clock signals that have to be synchronized together

Q: A Set-Reset flip-flop has the purpose of:

A: setting or resetting an external circuit
B: generating a clock signal
C: memorizing one bit of information
D: memorizing a word of N bits

Q: The direct memory access (DMA) mechanism:

A: allows peripherals to directly access main memory without the CPU
B: allows the CPU to directly access main memory without the bus
C: allows main memory to directly access peripherals
D: allows main memory to directly access the CPU registers

Q: In a superscalar CPU architecture, performance can degrade if:

A: there are not enough registers to keep all the needed temporary values
B: there are only a few dependencies between the instructions
C: the instructions do not access memory often enough
D: there are too many dependencies between the instructions