Topic: Computer System Architecture

Subtopic: Binary arithmetics

Q: In the floating-point IEEE 754 format:

A: the sign bit is either 1 or 0 depending on whether the mantissa is even or odd

B: there is more than one sign bit

C: the sign bit is 0 for positive numbers

D: the sign bit is 1 for positive numbers

Q: What happens to the binary representation of a number when it gets multiplied by 2?

A: The bits get shifted to the left

B: The bits get shifted to the right

C: The bits are shuffled

D: The bits get flipped

Q: An advantage of the floating-point system for representing fractional numbers is that:

A: any number fits into 32 bits

B: with the same encoding we can represent very large or very small numbers, depending on the applications

C: the precision is very high

D: the representable magnitude is very large

Q: Which is the two s complement representation of the number -10, using 8 bits?

A: 11100111

B: 11110110

C: 00001010

D: 10101010

Q: Which is the two s complement representation of the number -42, using 8 bits?

A: 00101010

B: 11100111

C: 10101010

D: 11010110

Q: In the two s complement encoding for negative numbers:

A: there is only one representation of zero

B: even numbers are represented better

C: very high precision is achieved

D: one needs two times the number of bits

Q: An advantage of the two s complement scheme for negative numbers is:

A: any number of bits can be used

B: the precision is very high

C: the set of representable numbers is very large

D: there is only one representation of zero

Q: Which is the result of the binary operation 001101 + 110010?

A: 000000

B: 111000

C: 10101

D: 111111

Q: Which is the two s complement representation of the number -1, using 8 bits?

A: 11101111

B: 11110000

C: 11100001

D: 11111111

Q: Which is the result of the binary operation 111000 + 000111?

A: 111111

B: 111000

C: 010101

D: 000000

Q: What happens to a binary number when it is shifted to the left by one position? (for example, from 111001 to 1110010)

A: the new value is unrelated

B: the value is multiplied by 2

C: the value is divided by 2

D: the value is raised to the power of 2

Q: Which is the result of the binary operation 111001 + 111001?

A: 1110010

B: 1110000

C: 0000001

D: 0101010

Q: In the floating-point IEEE 754 format:

A: there is no way to represent the concept of infinity

B: the distance between two consecutive numbers is variable

C: the distance between two consecutive numbers is constants

D: there is only one representation of the number zero

Subtopic: Logic gates and boolean algebra

Q: If A=0 e B=0, which is the result of the Boolean operations A AND B, A OR B, and A XOR B?

A: 1, 0, 1

B: 0, 0, 0

C: 1, 1, 1

D: 0, 1, 0

Q: Which of these combinations of gates can be used to build a Set-Reset flip-flop?

A: an OR gate and an AND gate

B: two AND gates

C: two NAND gates

D: two XOR gates

Q: If A=0 e B=1, which is the result of the Boolean operations A NAND B, A NOR B, and A XOR B?

A: 1, 1, 0

B: 0, 1, 0

C: 1, 0, 1

D: 1, 1, 1

Q: In a Set-Reset flip-flop built with NOR gates, when S=0 and R=0, the circuit:

A: has unpredictable behavior

B: gives output 1

C: stays in the memory configuration

D: gives output 0

Subtopic: The BUS

Q: In the old PCI bus:

A: all the devices were limited by the set 66MHz clock frequency

B: devices do not have to synchronize their access to the bus

C: synchronization of devices happens automatically

D: there are multiple clock signals that have to be synchronized together

Q: With the interrupt I/O mechanism:

A: the CPU interrupts the control flow when I/O is ready

B: the CPU waits for I/O operations

C: the CPU interrupts the control flow more frequently

D: the CPU interrupts the control flow at each instruction

Q: In an asynchronous bus:

A: devices do not have to synchronize their access to the bus

B: synchronization of devices happens without a central clock signal

C: there are multiple clock signals that have to be synchronized together

D: the transitions of the clock signal synchronize all the operations

Q: In the PCI-Express bus:

A: the clock frequency is chosen by the operating system

B: there is no central clock signal

C: the data lines connecting the devices to the host are parallel

D: all the devices are limited to the same clock frequency

Subtopic: Sequential and Combinatorial circuits

Q: A shift register is:

A: a sequential circuit whose output shifts to the right or to the left at each clock cycle

B: a combinatorial circuit that registers user inputs

C: a sequential circuit whose output is registered in different ways at each clock cycle

D: a combinatorial circuit that outputs a shifted version of the input

Q: In a superscalar CPU architecture, performance increases when:

A: there are too many dependencies between the instructions

B: there are only few dependencies between the instructions

C: there are enough registers to keep all the needed temporary values

D: the instructions access memory very often

Q: A counter is:

A: a combinatorial circuit that counts the number of 1s in the inputs

B: a combinatorial circuit that counts the number of 0s in the inputs

C: a sequential circuit whose output increments at each clock cycle

D: a sequential circuit that counts the number of 1s in the inputs

Q: A dynamic memory is:

A: a memory used to store information that changes frequently

B: a memory made of capacitors, and it needs to be refreshed periodically

C: a memory made of flip flops, and it does not need to be refreshed

D: a memory that can be written many times

Q: The cache memory is very especially effective when:

A: the bandwidth of the bus is large enough

B: nearby data are accessed together

C: main memory is built with similar technologies

D: the CPU frequency is relatively low

Q: In a pipelined CPU architecture, performance increases when:

A: the jumps are correctly predicted

B: the ALU is given small numbers as inputs

C: only a few registers are used

D: there are only a few instructions to execute at once

Q: In a pipelined CPU architecture, performance can degrade if:

A: there are too many instructions to execute at once

B: the registers are full

C: the ALU is given too large numbers as inputs

D: the jumps are not correctly predicted

Q: The cache memory is very effective also because of:

A: synchronization of devices happens automatically

B: there are multiple clock signals that have to be synchronized together

C: devices do not have to synchronize their access to the bus

D: the transitions of the clock signal synchronize all the operations

Q: A Set-Reset flip-flop has the purpose of:

A: setting or resetting an external circuit

B: generating a clock signal

C: memorizing one bit of information

D: memorizing a word of N bits

Q: The direct memory access (DMA) mechanism:

A: allows peripherals to directly access main memory without the CPU

B: allows the CPU to directly access main memory without the bus

C: allows main memory to directly access peripherals

D: allows main memory to directly access the CPU registers

Q: In a superscalar CPU architecture, performance can degrade if:

A: there are too many dependencies between the instructions

B: there are not enough registers to keep all the needed temporary values

C: the instructions do not access memory often enough

D: there are only a few dependencies between the instructions