Topic: Computer System Architecture

Subtopic: Binary arithmetics

Q: In the floating-point IEEE 754 format:

A: there is more than one sign bit

B: the sign bit is 0 for positive numbers

C: the sign bit is either 1 or 0 depending on whether the mantissa is even or odd

D: the sign bit is 1 for positive numbers

Q: What happens to the binary representation of a number when it gets multiplied by 2?

A: The bits get flipped

B: The bits get shifted to the right

C: The bits get shifted to the left

D: The bits are shuffled

Q: An advantage of the floating-point system for representing fractional numbers is that:

A: any number fits into 32 bits

B: the precision is very high

C: with the same encoding we can represent very large or very small numbers, depending on the applications

D: the representable magnitude is very large

Q: Which is the two s complement representation of the number -10, using 8 bits?

A: 00001010

B: 11110110

C: 11100111

D: 10101010

Q: Which is the two s complement representation of the number -42, using 8 bits?

A: 10101010

B: 11010110

C: 11100111

D: 00101010

Q: In the two s complement encoding for negative numbers:

A: there is only one representation of zero

B: even numbers are represented better

C: very high precision is achieved

D: one needs two times the number of bits

Q: An advantage of the two s complement scheme for negative numbers is:

A: there is only one representation of zero

B: the set of representable numbers is very large

C: the precision is very high

D: any number of bits can be used

Q: Which is the result of the binary operation 001101 + 110010?

A: 10101

B: 111111

C: 111000

D: 000000

Q: Which is the two s complement representation of the number -1, using 8 bits?

A: 11110000

B: 11111111

C: 11101111

D: 11100001

Q: Which is the result of the binary operation 111000 + 000111?

A: 000000

B: 111111

C: 111000

D: 010101

Q: What happens to a binary number when it is shifted to the left by one position? (for example, from 111001 to 1110010)

A: the new value is unrelated

B: the value is multiplied by 2

C: the value is divided by 2

D: the value is raised to the power of 2

Q: Which is the result of the binary operation 111001 + 111001?

A: 0000001

B: 0101010

C: 1110010

D: 1110000

Q: In the floating-point IEEE 754 format:

A: there is only one representation of the number zero

B: the distance between two consecutive numbers is variable

C: the distance between two consecutive numbers is constants

D: there is no way to represent the concept of infinity

Subtopic: Logic gates and boolean algebra

Q: If A=0 e B=0, which is the result of the Boolean operations A AND B, A OR B, and A XOR B?

A: 1, 0, 1

B: 0, 1, 0

C: 0, 0, 0

D: 1, 1, 1

Q: Which of these combinations of gates can be used to build a Set-Reset flip-flop?

A: two NAND gates

B: two AND gates

C: two XOR gates

D: an OR gate and an AND gate

Q: If A=0 e B=1, which is the result of the Boolean operations A NAND B, A NOR B, and A XOR B?

A: 1, 1, 0

B: 0, 1, 0

C: 1, 0, 1

D: 1, 1, 1

Q: In a Set-Reset flip-flop built with NOR gates, when S=0 and R=0, the circuit:

A: gives output 0

B: gives output 1

C: has unpredictable behavior

D: stays in the memory configuration

Subtopic: The BUS

Q: In the old PCI bus:

A: there are multiple clock signals that have to be synchronized together

B: devices do not have to synchronize their access to the bus

C: all the devices were limited by the set 66MHz clock frequency

D: synchronization of devices happens automatically

Q: With the interrupt I/O mechanism:

A: the CPU waits for I/O operations

B: the CPU interrupts the control flow when I/O is ready

C: the CPU interrupts the control flow at each instruction

D: the CPU interrupts the control flow more frequently

Q: In an asynchronous bus:

A: the transitions of the clock signal synchronize all the operations

B: there are multiple clock signals that have to be synchronized together

C: synchronization of devices happens without a central clock signal

D: devices do not have to synchronize their access to the bus

Q: In the PCI-Express bus:

A: all the devices are limited to the same clock frequency

B: there is no central clock signal

C: the data lines connecting the devices to the host are parallel

D: the clock frequency is chosen by the operating system

Subtopic: Sequential and Combinatorial circuits

Q: A shift register is:

A: a combinatorial circuit that registers user inputs

B: a combinatorial circuit that outputs a shifted version of the input

C: a sequential circuit whose output shifts to the right or to the left at each clock cycle

D: a sequential circuit whose output is registered in different ways at each clock cycle

Q: In a superscalar CPU architecture, performance increases when:

A: there are too many dependencies between the instructions

B: the instructions access memory very often

C: there are only few dependencies between the instructions

D: there are enough registers to keep all the needed temporary values

Q: A counter is:

A: a sequential circuit that counts the number of 1s in the inputs

B: a sequential circuit whose output increments at each clock cycle

C: a combinatorial circuit that counts the number of 1s in the inputs

D: a combinatorial circuit that counts the number of 0s in the inputs

Q: A dynamic memory is:

A: a memory used to store information that changes frequently

B: a memory made of capacitors, and it needs to be refreshed periodically

C: a memory made of flip flops, and it does not need to be refreshed

D: a memory that can be written many times

Q: The cache memory is very especially effective when:

A: the CPU frequency is relatively low

B: the bandwidth of the bus is large enough

C: main memory is built with similar technologies

D: nearby data are accessed together

Q: In a pipelined CPU architecture, performance increases when:

A: only a few registers are used

B: there are only a few instructions to execute at once

C: the ALU is given small numbers as inputs

D: the jumps are correctly predicted

Q: In a pipelined CPU architecture, performance can degrade if:

A: there are too many instructions to execute at once

B: the ALU is given too large numbers as inputs

C: the jumps are not correctly predicted

D: the registers are full

Q: The cache memory is very effective also because of:

A: devices do not have to synchronize their access to the bus

B: the transitions of the clock signal synchronize all the operations

C: there are multiple clock signals that have to be synchronized together

D: synchronization of devices happens automatically

Q: A Set-Reset flip-flop has the purpose of:

A: generating a clock signal

B: setting or resetting an external circuit

C: memorizing a word of N bits

D: memorizing one bit of information

Q: The direct memory access (DMA) mechanism:

A: allows the CPU to directly access main memory without the bus

B: allows peripherals to directly access main memory without the CPU

C: allows main memory to directly access the CPU registers

D: allows main memory to directly access peripherals

Q: In a superscalar CPU architecture, performance can degrade if:

A: there are only a few dependencies between the instructions

B: there are too many dependencies between the instructions

C: there are not enough registers to keep all the needed temporary values

D: the instructions do not access memory often enough