Doc. No.: TD-LO65-DR-2001	Doc. Title:	65nm Logic Salicide 1.2/1.8/2.5/3.3V Low Leakage and 1.0/1.8/2.5/3.3V Generic Design Rules	Doc.Rev: 14R	Tech Dev Rev: 1.9	Page No.: 1/223

Document Level: (For Engineering & Quality Document/工程暨品质文件专用)

☐ Level 1 - Manual ☑ Level 2 – Procedure/SPEC/Report ☐ Level 3 - Operation Instruction

Security Level:

☐ Security 1 - SMIC Confidential ☑ Security 2 - SMIC Restricted ☐ Security 3 - SMIC Internal

Document Change History

Doc. Rev.	Tech Dev. Rev.	Effective Date	Author	Change Description
0T	0.0	2004-09-01	Jay Ning	Initiate
1T	0.0	2004-12-22	Jay Ning	1) 7.4.4,, 2 and 3: Added native NMOS AA width for 1.0/1.8/2.5/3.3v transistors as 0.5um. Transistor length for 1.0, 1.8, 2.5/3.3 are 0.2,0.8 and 1.2um, respectively. 2) 7.4.5, 2a: Having AA width for 1.0v transistors to increase from 0.08 to 0.09um, while keep the AA interconnect at 0.08 and minimum pitch 0.18um. 3) 7.4.5, 2b: Added width of an AA to define the width of NMOS/PMOS for 1.8/2.5/3.3v transistors as 0.4um 4) 7.4.5, 4b:Added min space between AA width larger than 0.15um as 0.14um for photo process margin.. 5) 7.4.8, 2: Having GT width for 1.0/1.8/2.5/3.3v transistors as 0.08, 0.2, 0.28, 0.38, respectively. 6) 7.4.8, 4b: Added poly space between polys wider than 0.15um as 0.14um for photo process margin. 7) 7.4.9-7.4.14, 1 and 2: Increased LDD and N+, P+ min width and space from 0.15um to 0.18um for photo process margin. 8) 7.4.8, 7 to 9: Realigned some overlay numbers based on photo overlay budget input from photo (mean+3 are 35 and 28nm for 190nm photo 90nm and 65nm node, respectively). 9) 7.4.1 note and 4 10) 7.4.3: Some descriptions were added for Nwell and DNW resistors. 11) Update 7.1 User Guide
2T	0.0	2005-8-17	Jay Ning	Text and description change for all sections. Most of the numbers are changed based on ITRS and published papers.
3T	0.0	2006-12-19	Howard Ho	1. Modified Doc Title (to include 1.0V/G and 1.2V/LL). 2. Adding VTNH section and VTPH section (customer request). 3. Add LVN/LVP gds # (unify layout layer). 4. Modify DNW.5 from 4.1 to 4 (align 90nm). 5. Modify AA.2a from 0.09 to 0.12. AA.2b from 0.09 to 0.4 (from marketing). 6. Modify NW.6 and NW.7 descriptions (include 1.8.2.5/3.3V). 7. Modify PUB.8 to 0.31 (align 90nm). 8. Modify LVN.1/LVN.2/LVP.1/LVP.2 from 0.32 to 0.18

				(customer request). 9. Modify DG.1/DG.2/TG.1/TG.2 from 0.8 to 0.46. Modify DG.4/GD.6/TG.6 descriptions. Modify TG.7 from 0.8 to 0.46 (customer request). 10. Modify GT.1b/GT.1c/GT.1d to 0.2/0.28/0.38 (align 90nm). Modify GT.6 from 0.14 to 0.1 (0.8X90nm). Modify GT.9 description. 11. Modify NLL.6/PLL.6/NLH.6/NLHT.6/PLH.6/PLHT.6 from 0.3 to 0.26 (align 90nm). Modify NLL.7/PLL.7/NLH.7/NLHT.7/PLH.7/PLHT.7 and NLL.8/PLL.8/NLH.8/NLHT.8/PLH.8/PLHT.8 descriptions. 12. Modify SN.5/SN.6/SP.5/SP.6 from 0.3 to 0.26 (align 90nm). Modify SN.7/SN.8/SP.7/SP.8 descriptions. 13. M1.8 metal width limit change from 14 to 8um (CMP dishing too high). 14. Mn.8 metal width limit change from 15 to 8um (CMP dishing too high).
4T	0.0	2007-07-17	BRANDON LI	For update 0.065um Logic technology: 1. Modify item 7.4.2 AA.2b 0.4->0.3 2. Modify item 7.4.21 CT.4a 0.06->0.055 and CT.4b 0.08->0.11 3. Modify item 7.4.5 NC.1 0.32->0.28 and NC.2 0.32->0.28 4. Modify item 7.4.6 PC.1 0.32->0.28 and PC.2 0.32->0.28 5. Add note for 7.2 to identify LOTA number.
5R	1.0	2008-12-02	Emily Bei	1. Add Mask No. in the table of 7.2.1 2. Modify PA2 layer normal use from “drawn” to “generated” 3. Modify Alpa layer normal use from “drawn” to “generated” 4. Update 7.2.1 layer mapping table, add RDL via, RDL, RDL PA2, RESAA, RESP1, OVERPL, INST, HR and LOGO window layer 5. Update LOTA No in 7.2.1 note part 6. Modify 7.2.1 table “LVN” description from “Low Vt pMOS device” to “Low Vt NMOS device” 7. Modify 7.2.1 table “LVP” description from “Low Vt NMOS device” to “Low Vt PMOS device” 8. Modify 7.2.1 table “PLH” to “PLHT” 9. Modify 7.2.1 table “NLH” to “NLHT” 10. Add 7.2.3 device truth table 11. Modify AA.3b 0.14->0.13 12. Add AA.10 “AA density rule”

				13. Add AA.11 item for AA dummy rule 14. Add "AA resistor rules" as Part 7.3.3 15. Modify NW.2 NW width for NW resistor in Part 7.3.4 from 1.8 to 1.6 16. Add one note for "NW resistor guideline" in part 7.3.4 17. Modify PSUB.3c in Part 7.3.5 from 1.2 to 0.5 18. Modify VTNH.4 0.18->0.16 19. Modify VTNH.5 0.18->0.16 20. Modify VTNH.6 0.27->0.21 21. Modify VTNH.7 0.27->0.21 22. Modify VTPH.4 0.18->0.16 23. Modify VTPH.5 0.18->0.16 24. Modify VTPH.6 0.27->0.21 25. Modify VTPH.7 0.27->0.21 26. Modify LVN.4 0.18->0.16 27. Modify LVN.5 0.18->0.16 28. Modify LVP.4 0.18->0.16 29. Modify LVP.5 0.18->0.16 30. Modify LVP.6 0.27->0.21 31. Modify LVP.7 0.27->0.21 32. Modify LVN.6 0.27->0.21 33. Modify LVN.7 0.27->0.21 34. Modify NLL.6 0.26->0.24
				35. Modify PLL.6 0.26->0.24 36. Modify NLH.6 0.26->0.24 37. Modify PLH.6 0.26->0.24 38. Modify SN.5 0.26->0.24 39. Modify SN.6 0.26->0.24 40. Modify SP.5 0.26->0.24 41. Modify SP.6 0.26->0.24 42. Add GT.13 to add ploy dummy rule 43. Add GT.1e poly cd overdrive rule. 44. Add GT rule note 3. 45. Add 7.3.15 Poly resistor rule 46. Add E-fuse rule as Part 7.3.16 47. Update DG.4, DG.5, DG.6 description and DG.4 scheme 48. Update TG.4, TG.5, TG.6 description and TG.4 scheme. 49. Update GT.7 description and add density check window size 50. Update NLL.6, PLL.6, NLH.6, PLH.6, SN.5, SN.6, SP.5, SP.6 description. 51. Modify CT.3 number 0.1→0.07 52. Modify CT.8 in Part 7.3.24 from 0.04 to 0.025

				53. Modify M1.6 description and values: Max 82%→75%, Min 16%→30%. And add "density check window" 54. Modify M1.7 description from "Space between metal line and 45 degree bent metal line" to "Space between metal lines with one or both are 45 degree, and the bending metal length is larger than 0.5um (the area with 0.1um distance from bending point need not follow this rule)" 55. Modify M1.8 description to delete "metal slot rule" and then define maximum line width allowed 56. Modify M1 schematic picture 57. Modify note descriptions in Part 7.3.26 to add "and the intersection area is larger than 0.3um^2" 58. Modify "M1" to "Mn" in "Mn.6" 59. Modify Mn.6 description and values: Max 82%→75%, Min 16%→30%. And add "density check window"
				60. Modify Mn.7 description from "Space between metal line and 45 degree bent metal line" to "Space between metal lines with one or both is 45 degree and the bending length >=0.5um (the area with 0.1um distance from bending point need not follow this rule)" 61. Modify Mn.8 description to delete slot rule and then define the max. metal width allowed 62. Modify Mn schematic picture 63. Modify "V1" of Vn.7 and Vn.8 to "Vn" 64. Modify Vn.7 value from "0.01" to "0.04" 65. Modify Vn.8 value from "0.04" to "0.01" 66. Delete the original Vn.9 rule and change the content as "Note" part. Modify "Vn.10" to "Vn.9" because it is not a strict rule, but as a recommendation. 67. Modify Vn schematic picture 68. Modify TV1 description to include TV1 option (b) 69. Add TV1.7 and TV1.8 rules 70. Add TV1 option (b) rules 71. Add TM1 description to include TM1 option (b) 72. Modify TM1.4 value from "1" to "0.7" 73. Modify TM1.5 rule description to delete slot rule and then define the max. width allowed 74. Add TM1 metal density rule as rule TM1a.6 75. Add TM1 option (b) rules 76. Add TV2 rule descriptions 77. Add TV2.7 and TV2.8 parts 78. Add TV2 option (b) rules

				79. Add TM2 description to include TM2 option (b) 80. Modify TM2a.4 value from "1" to "0.7" and add the unit in the description 81. Modify TM2a.5 rule description to delete slot rule and then define the max. metal width allowed 82. Add TM2 metal density rule as TM2a.6 83. Add TM2 option (b) rules 84. Delete the part of "Metal slot rules" because it is not suitable as device dimension is decreased 85. Add MTT rules 86. Modify the old dummy size from MD.1 to MD.5 87. Modify MD.10 "dummy metal Boolean operation"
				88. Add MD.13 rule 89. Add MD.14 rule 90. Add "PA1 rules" 91. Add "RDL rules" 92. Add "RDL PA2" rules 93. Add "seal ring rules" 94. Add "Current density Rule" 95. Modify 7.3.2 add AA.10 & AA.11, Change AA3b Design minimum (um) to 0.13
6R	1.1	Zhao Xu Shen	2009-02-24	1.Delete Fuse layer in "SMIC mask layer name mapping table" of Part 7.2.1 because Fuse layer is not used for 65LG currently 2.Modify PSUB.3b value from 0.50 to 0.8 in item7.3.5. 3.Delete PSUB.3c description "/3.3"for add 3.3V of PSUB.3d and modify value from 0.50 to 1.0 in item7.3.5. 4.Add PSUB.3d for "3.3V NMOS channel length" rule in item7.3.5. 5.Delete old Note 2 in the 7.3.14 GT rule part to avoid confusion 6.Modify Note 2"RP184" to "125;4 layer" 7.Correct 7.3.22 graph "0.25um" to "0.22um" 8.Modify CT.2b rule description to define CT array in item 7.3.24. 9.Modify V1.2b rule description to define via array in item7.3.26. 10.Modify Vn.2b rule description to define Via array in item7.3.28. 11.Correct 7.3.31(b) "TM->TM1" and "Mn->TM2" in the graph 12.Correct MD.6a value from "0.5" to "2" and modify "metal" to "Mn"in item7.3.34. 13.Add MD.6b rule to define "Space between dummy pattern and the edge of TMx block layer"in item7.3.34. 14.Correct MD.7a value from "0.5" to "2"in item7.3.34.

				15.Add MD.7b rule to define "space between dummy pattern and the edge of TMn pattern"in item7.3.34. 16. Add MD.9a to define space between Mx dummy pattern and the edge of poly gate (AA*GT) in item7.3.34. 17. Add "TMx" to the description of MD.9b in item7.3.34. 18.Modify 7.3.35 rule PA1.2 description from "PA1 via size" to "PA1 length or width" 19.Modify 7.3.35 rule PA1.3 from "space between two PA1 VIAs" to "space between two PA1" 20.Modify 7.3.35 rule PA1.4 " PA1 VIA enclosure by RDL" to " RDL Via enclosure by RDL" 21. Modify 7.3.34 metal dummy rule number to distinguish the same rule No. for MD.1-MD.7,MD.9.
7R	1.2	Emily Bei	2009-05-08	1. Modify 7.2.1 107,163,108 layer, "RDL via", "RDL PA2" and "RDL" layer description, add dummy layer gds numbers 2. Add "fuse" and "MARKF" layer to 7.2.1; 3. Modify AA.2b 0.30->0.21; 4. Modify AA.3b 0.13->0.11; 5. Modify NW.6 0.6->0.47; 6. Modify NW.7 0.6->0.47; 7. Modify NW.4 0.5->0.47; 8. Modify Psub.5,Psub.6,NC.4,NC.5,NC.6,NC.7,PC.4,PC.5, PC.6,PC.7,VTNH.4,VTNH.5, VTNH.6, VTNH.7,VTPH., VTPH.5, VTPH.6, VTPH.7,LVN.4, LVN.5, LVN.6,LVP.4 and LVP.5 description; 9. Modify NC.4 0.18->0.12; 10. Modify NC.5 0.18->0.12; 11. Modify NC.6 0.27->0.20; 12. Modify NC.7 0.27->0.20; 13. Modify PC.6 0.27->0.20; 14. Modify PC.4 0.18->0.12; 15. Modify PC.5 0.18->0.12; 16. Modify PC.7 0.27->0.20; 17. Modify VTNH.4 0.16->0.12; 18. Modify VTNH.5 0.16->0.12; 19. Modify VTNH.6 0.21->0.20; 20. Modify VTNH.7 0.21->0.20; 21. Modify VTPH.4 0.16->0.12; 22. Modify VTPH.5 0.16->0.12; 23. Modify VTPH.6 0.21->0.20; 24. Modify VTPH.7 0.21->0.20; 25. Modify LVN.4 0.16->0.12; 26. Modify LVN.5 0.16->0.12; 27. Modify LVN.6 0.21->0.20;

				28. Modify LVN.7 description; 29. Modify LVN.7 0.21->0.20; 30. Modify LVP.4 0.16->0.12; 31. Modify LVP.5 0.16->0.12; 32. Modify LVP.6 description; 33. Modify LVP.6 0.21->0.20; 34. Modify LVP.7 description; 35. Modify LVP.7 0.21->0.20; 36. Modify DG.3 and DG.4 description;
				37. Modify DG.4 0.33->0.24; 38. Modify DG.5 description; 39. Modify DG.6 0.33->0.24; 40. Modify TG.3 description; 41. Modify TG.4 description; 42. Modify TG.4 0.33->0.24; 43. Modify TG.5 description; 44. Modify TG.6 0.33->0.24; 45. Modify GT.3b,NLL.7,NLL.8,PLL.7,PLL.8,NLH.7,NLH.8, PLH.7,PLH.8 ,SN.7 ,SN.8, SP.7,SP.8 description; 46. Modify SAB.9 0.28->0.20; 47. Modify CT.4b 0.11->0.09; 48. Modify E-fuse rule 7.3.16; 49. Modify M1.3a 0.14->0.11; 50. Modify M1.3b value 0.3->0.18; 51. Modify M1.3c description; 52. Modify 7.3.25 note item3; 53. Modify V1.4 value 0.04->0.03; 54. Modify V1.7 value 0.04->0.03; 55. Modify 7.3.27 rule number; 56. Modify 7.3.27 note item3 description; 57. Modify Mn.3a 0.15->0.12, Mn.3b 0.3->0.16; 58. Modify Vn.4 0.04->0.03; 59. Modify Vn.7 0.04->0.03; 60. Delete MD.10 because it is duplicated with other rules and modify MD.11~MD.15 rule numbers; 61. Modify MD.7b “TMn” to “TMx”; 62. Modify MD.9a; 63. Modify 7.3.30 descriptions; 64. Modify TM1a.1 0.42->0.40; 65. Modify TM1a.2a 0.42->0.40; 66. Modify TM1a.2b description; 67. Modify TM1a.3 0.42->0.40; 68. Modify TM1b.2b~TM1b.2d, 7.3.31 and 7.3.32 description; 69. Modify TM2a.1 0.42->0.40;

				70. Modify TM2a.2a 0.42->0.40;
				71. Modify TM2a.3 0.42->0.40; 72. Modify TM2a.2b description; 73. Modify 7.3.29 description “0.42”->”0.40”; 74. Modify 7.3.31 description “0.42”->”0.40”; 75. Modify TV1a.6 0.03->0.02; 76. Modify TV1a.5 0.03->0.02; 77. Modify TV2a.5 0.03->0.02; 78. Modify TM1b.2b~TM1b.2d descriptions; 79. Add TM2a.8 rule; 80. Modify TV2a.6 0.03->0.02; 81. Modify TM2b.2b~TM2b.2d descriptions; 82. Add TM2b.8 rule; 83. Modify MTT.2b description; 84. Delete MTT.2c rule because it is not necessary from Si data; 85. Add MTT.10 rule 86. Modify 7.3.36 notes; 87. Modify 7.3.37 rule title and 7.3.37 description; 88. Modify 7.3.37 rule numbers; 89. Modify 7.3.35 PA1 rules; 90. Modify 7.3.36 Notes; 91. Modify RDLPA2.1 and RDLPA2.2 rule descriptions; 92. Add Al fuse rule; 93. Add Part 7.3.41and Part 7.3.42; 94. Add “GTFUSE” layer to 7.2.1; 95. Modify 7.3.25, 7.3.27, 7.3.31, 7.3.32, 7.3.33 schematic picture; 96. Delete TM2a.6 and TM2b.6 because it is not necessary from Si data; 97. Modify TM2b.5 value from 20->30.00; 98. Modify M1.6 and Mn.6 value: min. 30%->20%, Max: 75%->80%; 99. Modify AA.11 and GT.13 descriptions; 100. Modify 7.3.38 Fig.1; 101. Modify 7.3.29~ 7.3.32 descriptions; 102. Modify RESAA.1 from “to be larger than 2.0m and Nsq>=5 for stable Rs” to “to be larger than 0.5um and Nsq>=1 for stable Rs”;
8R	1.3	Emily Bei	2009-08-31	1. Modify 7.2.1 layer mapping layer 107 “normal use” value drawn->drawn/generated 2. Modify 7.2.1 layer mapping table 108 descriptions 3. Modify7.2.1 layer mapping table 163 layer name and descriptions 4. Modify 7.2.1 layer mapping table layer name PODUM->GTDUM

				5. Modify Note 4 in 7.2.1 layer mapping table 6. Modify 7.2.2 Definition of terminology used in this design rules 7. Modify 7.2.4 Device layout truth table 8. Modify DNW.2 value 6.00->3.00 in 7.3.1 9. Delete VTNH.3, VTPH.3, LVN.3, LVP.3 unnecessary rules in 7.3.8~7.3.11 10. Modify VTNH.8, VTPH.8, LVN.8, LVP.8 numbers to LVN.3, LVP.3, VTNH.3 and VTPH.3 respectively in 7.3.8~7.3.11 11. Modify GT.3b rule description in 7.3.12 12. Modify GT.5 value 0.15->0.12 in 7.3.12 13. Modify GT.5, GT.6 descriptions in 7.3.12 14. Modify CT.3 value 0.07->0.065 in 7.3.24 15. Modify CT.4 value 0.055->0.05 in 7.3.24 16. Modify M1.3b value: 0.18->0.16 in 7.3.25 17. Modify M1.4 value: 0.036->0.027 in 7.3.25 18. Delete M1.3a because Si data showed it is unnecessary and modify M1.2, M1.3b, M1.3c rule numbers in 7.3.25 19. Change M1.8 rule number to M1.3 in 7.3.25 20. Modify V1.4 value:0.03->0.025 in 7.3.26 21. Modify V1.7 value: 0.03->0.025 in 7.3.26 22. Modify Mn.4 value 0.045->0.035 in 7.3.27 23. Delete Mn.3a because Si data showed it is unnecessary and modify Mn.2, Mn.3b, Mn.3c rule numbers in 7.3.27 24. Change Mn.8 rule number to Mn.3 in 7.3.27 25. Modify Vn.4 value 0.03->0.025 in 7.3.28 26. Modify Vn.7 value 0.03->0.025 in 7.3.28 27. Modify TM1a.4 value 0.70->0.60 in 7.3.30(a) 28. Modify TM2a.4 value 0.70->0.60 in 7.3.32(a) Change rule number to TM2a.8-> TM2a.6 in 7.3.32(a), TM2b.7-> TM2b.6 and TM2b.8->TM2b.7 in 7.3.32(b) 29. Modify the schematic pictures of 7.3.25, 7.3.27, 7.3.30(b), 7.3.32(b) 30. Modify MD.6a and MD.7a from 0.5 to 2 in 7.3.34
				31. Delete MD.9a&MD.9b in 7.3.34 because they are not a must 32. Add MTT dummy rule as MD.9 in 7.3.34 33. Modify PA.1 value 1.5->1 in 7.3.35.1 34. Modify RDV.4 value 1.5->1 in 7.3.35.2 35. Modify GR.3 and GR.9 decryptions and values from post-OPC numbers to pre-OPC numbers in 7.3.38 36. Modify GR13 and GR16 numbers to meet the changes of GR.3 and GT.9 in 7.3.38 37. Modify 7.3.37 descriptions 38. Modify 7.3.38 note description and add post-OPC numbers 39. Modify 7.3.38 Fig.3b

				40. Modify CDR.49 from "CDR.1 – CDR.36" to "CDR.1 – CDR.48" in 7.3.39 41. Modify PR.1 to define Pre-OPC and Post-OPC numbers in 7.3.40.3 42. Add note in 7.3.40.3 43. Delete DNW note 2. no need for this rule. 44. Modify TG.5 description. 45. Add layer "EXCLU" in 7.2.1 the mapping table 46. Add 7.2.1 note 5.
8.1R	1.3	2009-09-28	Jove Ding	Document title change from "0.065um Logic 1P10M Salicide 1.0(G) or 1.2(LL)/1.8/2.5.or 3.3V Design Rules" to "65nm Logic 1P10M Salicide 1.2/1.8/2.5/3.3V Low Leakage and 1.0/1.8/2.5V Generic Design Rules"
9R	1.4	2010-02-05	Emily Bei	1. Add reference file in part 5 2. Modify 7.2.1 NLH, PLH, NLHT, PLHT "normal use" value from "drawn" to "drawn/generated" 3. Modify 7.2.1 gds layer number of AA, GT and M1~TM2 to add data type 4. Add UNDERPL, OVERPL, LDBK, STIDMY layers in 7.2.1 5. Modify note 4 in 7.2.1 to deleted SMICLC65GE1 and SMICLC65LL1 and modified SMICLC65GE0 and SMICLC65LL0 description because TM2 dummy rule is updated 6. Add note 6 and note 7 in 7.2.1 for EXCLU and INST layer definition 7. Correct 7.2.2 MOS AA description 8. Add "2.5V underdrive to 1.8V" and LDMOS items into 7.2.4 9. Modify DNW.2 value 3.00→4.00 in 7.3.1 10. Modify DNW.3 value: 2.00→1.00 in 7.3.1 11. Modify DNW.4 value: 2.00→1.00 in 7.3.1 12. Modify DNW.5 value: 4.00→3.00 in 7.3.1 13. Modify 7.3.2 AA.10 description and define AA density high/low spec. 14. Add note 2 and note 3 into 7.3.2 15. Delete the old AA dummy rule and schematic pictures and then be replaced with new AA Dummy fill pattern guideline because of new dummy rule release 16. Add note 5 into 7.3.4 to explain NW.1 and NW.3 17. Add note.6 and update the schematic picture to explain note.6 18. Modify PSUB.3c descriptions 19. Add rule GT.1f in 7.3.14 20. Modify 7.3.14 GT.7 description and define poly density high/low spec.

				21. Add note3 and note 4 into 7.3.14 22. Delete 7.3.14.1 the old poly dummy rule and schematic picture and be replaced with new Poly Dummy fill pattern guideline because of new dummy rule release 23. Add LDMOS rule as Part 7.3.17 24. Re-arrange rule numbers because of 7.3.17 addition. Correct some incited part numbers in 7.3.30 description, 7.3.31 description and 7.3.33 description.
				25. Modify 7.3.25 CT.2b descriptions 26. Modify M1.6 and Mn.6 descriptions 27. Add note4 in 7.3.26 part 28. Modify 7.3.27 V1.2b description 29. Add note5 in 7.3.28 part 30. Modify 7.3.29 Vn.2b description 31. Modify 7.3.30 (b) TV1b.2b descriptions 32. Modify TM1a.6 and TM1b.6 descriptions 33. Add TV2b.2b rule and modify "TV2b.2" number to "TV2b.2a" 34. Add TM2a.7 rule and TM2b.8 35. Delete 7.3.34 MTT design rule details and refer the content to other file. 36. Delete old metal dummy rule and replaced with new rules because of new dummy rule release 37. Modify 7.3.38 incited part number in the descriptions 38. Modify 7.3.39 descriptions to change some Figure numbers 39. Delete old GR.1~2, GR.5 and then re-arrange rule numbers and then update schematic pictures to correct rule numbers. 40. Update GR1~6 numbers to mask size 41. Split old GR.4 into three rules from GR.7 to GR.9 42. Split old GR.13 into three rules from GR.22 to GR.24 and correct the numbers 43. Split old GR.14 into two rules: GR.25 and GR.26 44. Split old GR.15 into two rules: GR.27 and GR.28 45. Split old GR.16 into two rules: GR.29 and GR.30 and also correct the values. 46. Update GR 29, GR30 rule numbers 47. Modify old GR.10 (now GR 14) description
				48. Modify 7.3.39 note description and modify table 2 numbers to pre-OPC numbers. 49. Modify 7.3.39 Fig.1 description and correct rule numbers 50. Delete the old Fig.2, Fig.3.b 4 in 7.3.39 and replaced with new Fig.2～Fig.3 to make rules clear and consistent with real layout 51. Modify Fig.3a rule number as Fig.4 and update rule

				numbers 52. Update Fig.5 rule numbers 53. Add table 3 in 7.3.39 to make layout clear 54. Modify CDR.49 description 55. Modify 7.3.41 description to update the incited rule numbers 56. Modify PR.2 0.36→0.28 57. Modify Mark.11 description to update the incited rule numbers
10R	1.5	2010-03-09	Ellen Jin	1. Update layer mapping table 7.2.1, Add "HR" layer digitized area tone "C" and GDS layer number 34, update layer OVERPL & UNDEPL gds numbers and descriptions 2. Modify mapping table 7.2.1 "UNDERPL" to "UNDEPL" 3. Add SRAM cell identification layers STSRAM, DNSRAM, UDSRAM, DPSRAM, RFSRAM in to 7.2.1 4. Modify 7.3.2 AA.8 Design minimum from 0.054 to 0.038 5. Update 7.3.2 AA.9 description 6. Deleted 7.3.2 AA note.3 and put it to 7.3.2.1 note.2 7. Modify 7.3.2.1 title "AA dummy fill pattern guideline" to "AA dummy pattern design rules" 8. Add descriptions into 7.3.2.1 to define different dummy sets. 9. Modify AADUM.7~10, AADUM.17~22 and AADUM.24 descriptions. 10. Merge AADUM.25 and AADUM.26 as AADUM.25, then deleted AADUM.26 for new request 11. Modify 7.3.2.1 note part 12. Update 7.3.14 note 2 description 13. Deleted 7.3.14 note.4 and put it to 7.3.14.1 note.2 for new request 14. Modify 7.3.14.1 title from "poly dummy fill pattern guideline" to "poly dummy pattern design rules" 15. Add descriptions into 7.3.14.1 to define two sets of dummy patterns. 16. Modify PODUM.7~10, PODUM.17~22 and PODUM.28 descriptions 17. Merge PODUM.29 and PODUM.30 as PODUM.29, then deleted PODUM.30 for new request 18. Modify 7.3.14.1 note part 19. Modify 7.3.18 NLL.7, NLL.8, 7.3.19 PLL.7, PLL.8, 7.3.20 NLH.7, NLH.8, 7.3.21 PLH.7, PLH.8, 7.3.22 SN.7, SN.8, 7.3.23 SP.7, SP.8 descriptions and schematic descriptions. 20. Modify 7.3.18 NLL.8 Design min. from 0.20 to 0.17 21. Modify 7.3.19 PLL.8 Design min. from 0.20 to 0.17 22. Modify 7.3.20 NLH.8 Design min. from 0.20 to 0.17 23. Modify 7.3.21 PLH.8 Design min. from 0.20 to 0.17 24. Modify 7.3.22 SN.8 Design min. from 0.20 to 0.17

				25. Modify 7.3.23 SP.8 Design min. from 0.20 to 0.17 26. Modify 7.3.35, 7.3.35.1, 7.3.35.2, 7.3.35.3 title from guideline to “design rules” 27. Modify 7.3.35.1 MnDUM.6~8 descriptions 28. Modify 7.3.35.1 note.1 and note.2 29. Modify 7.3.35.2 TM1DUM.6~8 descriptions 30. Modify 7.3.35.2 note.1 and note.2 31. Modify 7.3.35.3 TM2DUM.6~8 descriptions 32. Modify 7.3.35.3 note.1 and note.2
11R	1.6	2010-07-16	Angela Ma	1. Re-arrange 7.2.1 mask layer mapping. The modified items please refer to 2~7. 2. Add PDRF, HRP, SM, HRPDMY, VARMOS, VARJUN, JVARDUM, EFUSE, NODMF, MxDUB (n=1~8), TM1DUB, TM2DUB, MOMDMY, MARKG, INDMY and DTDMY into 7.2.1 layer mapping table. And MOD PDRF, HR, LOGO layer normal use, HRPDMY layer Description, MOD AADUM, GTDUM layers Digitized Area Tone to “D”, MOD note5 descriptions. 3. DEL 7.2.1 note “A detailed rule…verified” because it is useless. 4. MOD 7.2.2 “width” and “space” definitions and add two pictures 5. Add DNW GDS# and mask ID in 7.2.3 and 7.2.4, add PDRF layer in 7.2.3, add AA, TG, DG, PDRF, GT and PSUB layers, MOD OVERPL and UNDERPL GDS# in 7.2.4 6. MOD implant step to layer name in 7.2.4 7. Add 7.2.5 and 7.2.6, 7.2.7 and 7.2.8 8. Add DNW.6 and DNW NOTE.2 and MOD schematic picture in 7.3.1 9. 7.3.2 AA.2a 0.12->0.11 10. Add NODMF into AADUM.7, AADUM.20, AADUM.23 and schematic picture 11. MOD 7.3.2.1 AADUM.25 AA, 7.3.16.1 PODUM.29 GT density check window size 12. Add Note.3 in 7.3.2.1. 13. NW.1 and NW.3 0.32 -> 0.36, NW.6 and NW.7 0.47 -> 0.72 14. DEL 7.3.4 NOTE.5 because of NW.1 and NW.3 rule changes 15. 7.3.5 PSUB.1 and PSUB.4 0.32 -> 0.36 16. Add “and AA in INDMY” in 7.3.5 PSUB NOTE.2 and add PSUB NOTE.3 & 4 in 7.3.5 17. VTNH.6, VTNH.7 0.20 -> 0.185 18. VTPH.6, VTPH.7 0.20 -> 0.185 19. LVN.6, LVN.7 0.20 -> 0.185 20. LVP.6, LVP.7 0.20 -> 0.185 21. Add VTNH.8, VTPH.8, LVN.8 and LVP.8 rules 22. MOD DG.2, DG.3, DG.4 and DG.5 Description in 7.3.12

				23. MOD DG.4 Description and values 0.25 -> 0.27 24. Add DG.7, DG.8, DG.9, DG.10, DG.11 and DG.12 rules in 7.3.12 and MOD schematic picture 25. MOD TG.2, TG.3, TG.4 and TG.5 Descriptions. 26. MOD TG.4 Description and value 0.25 -> 0.27. 27. Add TG.8, TG.9, TG.10, TG.11, TG.12 and TG.13 rules in 7.3.13 and MOD schematic picture. 28. Add 7.3.14 and 7.3.15 and rearrange the subsequent numbers. 29. GT.5 0.12 -> 0.115, GT.6 0.10 -> 0.14 30. MOD GT.11 Description and schematic. 31. Add GT.13 rule 32. Add NODMF layer into PODUM.8, PODUM.20, PODUM.23 and schematic. 33. Add Note.3 in 7.3.16.1. 34. MOD 7.3.17 RESP1.1 Description. 35. Add RESP1.8 and RESP1.9 in 7.3.17, and MOD schematic picture. 36. MOD EFU.9 and EFU.10 Description. 37. Add EFU.11 in 7.3.18 table. 38. MOD 7.3.18 Schematic layer description SP to EFUSE, and DEL "E-fuse block layer" because layer mapping table has defined GTFUSE function. 39. Add 7.3.19 LDAA.2 design maximum and MOD 0.10 -> 0.11. 40. MOD 7.3.19 schematic. 41. MOD NLL.8, PLL.8, NLH.8, PLH.8, SN.8 and SP.8 0.17 -> 0.16. 42. CT.5 0.03 -> 0.015, CT.6 0.02 -> 0.01 43. Add "Design maximum" in 7.3.28 and 7.3.30, 7.3.33(a). 44. MOD 7.3.28 note 3, note4 descriptions and add note5 and update schematic pictures. 45. MOD 7.3.29 note1 description and add schematics. 46. MOD V1.2b,Vn.2b description from "<=0.15" -> "<0.15". 47. MOD 7.3.30 note3 and note5 descriptions, and add note 6 and update schematic pictures. 48. MOD note 1 description in 7.3.31, add schematic and note2. 49. Add note in 7.3.33 (a). and update schematic picture. 50. MOD TM1b.5 description and update 7.3.33(b) schematic picture. 51. Add "design maximum" and notes in 7.3.35(a) and 7.3.35(b), 7.3.33(b). 52. Update 7.3.35(a),7.3.35(b) schematic picture. 53. DEL the old dummy rules 7.3.37.1 and be replaced with a new one. 54. MOD TM1DUM.11MOD PA.3, note.3 descriptions. 55. MOD 7.3.38.1 descriptions.

				56. Add RDV.5 rule and update the schematic. 57. RDL.1 1.5->3.0, RDL.2a 1.5->2.0. 58. Add RDL.4 into 7.3.39 and update schematic. 59. Add 7.3.40 and re-arrange sequent numbers. 60. MOD 7.3.42 title name, GR.22 0.1825 -> 0.183 and add GR.34 and add description into table 3. 61. MOD 7.3.42 table 3 and update the schematic Fig.1. 62. MOD 7.3.43 title and MOD note from "1.5" -> "10". 63. MOD CDR.28, CDR.34, CDR.41, CDR.45, CDR.49, CDR.52, CDR.54, CDR.58 descriptions, and add CDR.27, CDR.35, CDR.41, CDR.46, CDR.50, CDR.53, CDR.55, CDR.57 rules in 7.3.42. 64. DEL ALF.7 because it is unnecessary. 65. MOD SV.7 rule description 66. Add PR.10 rule 67. Add 7.3.46 and DEL 7.3.47 because it is not used 68. Add comment in 8. Attachment
12R	1.7	2010-10-07	Angela Ma	1. Modify Top Tier Doc. No in 7.2.1.1 and 7.2.1.2 2. Add NPR1 and BORDER in 7.2.1.1 and 7.2.1.2 3. Move LDBK from 7.2.1.3 to 7.2.1.1 and 7.2.1.2 4. Modify CT, PA, ALPA, MD, V1~TV2, DUMBM, RDL, BCB2, NODMF descriptions in tables of 7.2.1.1 and 7.2.1.2 5. Add EXDRC and NOSHR in 7.2.1.3 6. Add Note.8 & 9 in 7.2.1 7. Modify 7.3.1 DNW.2 4.00 -> 3.50 8. Modify 7.3.1 DNW.4 1.00 -> 0.40 9. Modify 7.3.1 DNW.5 3.00 -> 2.50 10. Modify 7.3.10 LVN and 7.3.11 LVP rule descriptions 11. Modify 7.3.12 DG.8, DG.9, DG.10 and DG.11 descriptions 12. Modify 7.3.13 TG.9, TG.10, TG.11 and TG.12 descriptions 13. Modify 7.3.16 GT.3a description 14. Modify 7.3.16 GT.6 description 15. Add Note. 4 in 7.3.16 16. Modify 7.3.16 schematic picture 17. Modify 7.3.19 LDMOS layout guidelines to LDMOS Design Rules 18. Modify 7.3.19 LDAA.7 1.5 -> 1.0 19. Modify 7.3.19 LDAA.12 description 20. Modify 7.3.19 schematic picture 21. Modify 7.3.26 SAB.1 and SAB.2 0.36 -> 0.40 22. Add M1.6b and M1.6c and density check schematic in 7.3.28 23. Modify 7.3.29 V1.4 0.025 -> 0.03 24. Modify 7.3.29 V1.6 0.01 ->0.02 25. Modify 7.3.29 V1.7 0.025->0.03 26. Modify 7.3.29 V1.8 0.01->0.02

				27. Add Mn.6b and Mn.6c and density check schematic in 7.3.30 28. Modify 7.3.31 Vn.4 0.025 -> 0.03 29. Modify 7.3.31 Vn.6 0.01 ->0.02 30. Modify 7.3.31 Vn.7 0.025->0.03 31. Modify 7.3.31 Vn.8 0.01->0.02 32. Modify item 8 Attachment Note.1 & 2 descriptions 33. Modify 11R -> 12R and 11RMIX -> 12RMIX in item 8 Attachment Note.2 table 34. Modify GT.6, DG.8, DG.9, DG.10, DG.11, TG.9, TG.10, TG.11 and TG.12 descriptions in item 8 Attachment Note.2 table
13R	1.8	2011-06-03	Amy Wong	1. 7.2.2 Modify space rule definition and related figures 2. Add SRAM part in 7.2.3 and 7.2.4 3. Modify BJT implant and layout truth tables in 7.2.5 and 7.2.6 4. Add varactor implant and layout truth tables as 7.2.9 and 7.2.10, respectively. 5. Delete 7.3.1 DNW.6 and update the schematic picture 6. Add RESAA.9 and RESAA.10 in 7.3.3 and update the schematic picture 7. Modify 7.3.2 AA.10 rule and note2, PSUB.5 description and add Note.5 in 7.3.5, 7.3.4 /7.3.2 Note； 7.312 DG.12 and 7.3.13 TG.13 rules, 7.3.16 Note3 and schematic picture 8. Add RESP1.10 in 7.3.17 and update the schematic picture 9. LDMOS rule update 10. Modify 7.3.21 description from LL to PLL 11. Modify CT.1 description 12. Modify Attachment Note.1 & 2 descriptions 13. Modify 12R -> 13R and 12RMIX -> 13RMIX in Attachment Note.2 table 14. Add DNW.3 and delete DNW.6 in Attachment Note.2 15. Delete NW.5 in section of 7.3.4. 16. 7.3.27 Optimize CT.7 figure 17. Modify M1.2b, M1.2c,M1.6a~M1.6c descriptions and the schematics，M1.6c rule value 30%->40%，Add M1.6d, Mn.6d rule，Modify M1.6a, Mn.6a 20% -->18%，Modify M1.3, Mn.3 8.00->12.00 18. Modify 7.3.28 Note 3~Note5 descriptions 19. Modify V1.1,Vn.1 descriptions 20. Modify Mn.2b, Mn.2c,Mn.6a~Mn.6c descriptions and the schematics，Modify Mn.6c rule value 30%->40%,Modify 7.3.30 note 3,note5, note6 descriptions 21. Modify TV1a.1, TV1b.1, TM1a.2b, TM1a.6, TM1b.2a~c, TM1b.6, TM2a.2b, TM2a.7, TM2b.2b~TM2b.2d, TM2b.8 descriptions and update the schematics

				22. Modify 7.3.29, V1.4a, V1.4b, V1.6a, V1.6b; add V1.10, 7.3.31, Vn.4a, Vn.4b, Vn.6a, Vn.6b; add Vn.10， TM1a.6, TM1b.6 30%->20%， 7.3.33(b), 7.3.35a, 7.3.35b note1.；MnDUM.6, 15，26，33，34.15 description，Add MnDUM.9,16，17，20，27，28，32，35-37 and update schematics 23. Modify MnDUM.10 0.30->0.16, MnDUM.12 0.30->0.17. MnDUM.13, MnDUM.23 0.30->0.25, MnDUM.14, 25 0.20->0.10, MnDUM.16, 27 0.30->0.17, 24. Modify 7.3.37.1 note2, TM1DUM.6, 11 descriptions and add TM1DUM.13, 15 and update schematics 25. Modify 7.3.37.2 note； TM1DUM.1, 2 2.5->1.6, TM1DUM.3, 4 1.5->0.8, TM1DUM..5 1.0->0.5， Delete TM1DUM.9, TM2DUM.9 because they are unnecessary 26. Modify TM2DUM.6, TM1DUM.11, TM2DUM.10, TM2DUM.11 descriptions 27. Add TM2DUM.13, TM1DUM.13 and update schematics，7.3.37.3 note， 7.3.38 description and schematics， RDV.1, RDV.2, RDV.4, RDV.5 descriptions，RDL.1, RDL.4 descriptions and update schematics，Delete RDL.2c because it is unnecessary and update schematics，Modify RDLPA2.2 10.0->5.0，7.3.42 seal ring descriptions and rule names, schematics， SR.3, SR.6, SR.24,SR.31, SR.34 descriptions 28. Delete SR.19, SR.20, and old Fig.4 and re-arrange figure numbers because they are not used in SMIC now. 29. Add SR.35 rule and Fig.5, Note.1 and update Note.2 table 30. Add MARKG, NODMF layer in 7.3.24 Table.3;Add 7.3.43 Chip edge border layer design rule，Modify 7.3.44 descriptions and ALF.6 and added ALF.7，Deleted old 7.3.44.3 and be replaced with 7.3.45.;Modify Mark.10~12 rule descriptions 31. Add 7.3.47 Logo layout guidelines and re-arrange rule numbers 32. Modify current density rule part numbers 33. Delete 7.3.49 AC current density rule 34. 7.3.41 add PA2 RDLPA2.4 and note. 35. Modify section 8 NW.3,5-7 rules 36. 7.3.37.1 add MnDUM.38 and update note2 37. 7.3.37.2/ 7.3.37.3 add TM1DUM.14/ TM2DUM.14 and update note 38. Remove 7.3.5 Psub.5，7.3.16 GT.3a and note4 for 55nm option 39. Delete section 8 content. 40. All of the DFM rules (including all priorities) become recommended rules. 41. Merge design rule TD-LO65-DR-2001v12R and DFM rule

				TD-LO65-DR-2002 (3TV0.4) into one document because of the need of system integration. Section 7.2 in original DFM rule document is copied to Section 7.4 in this document. We also made some modifications on the DFM rules as listed below. 42. Update 7.2.1.3 Accessorial layers table 43. Add DFM reference in item5
13.1R	1.8	2011-06-17	Amy Wong	1. Section 7.3.29 Via1 design minima: change V1.4b rule value from 0.005 to 0.00 2. Section 7.3.37.1 MnDUM.9, MnDUM.20: change the word of "MARK" to "MARKF"
14R	1.9	2012-03-20	Charles Yin	1. Title update: delete "1P10M", add "3.3V" for generic design rule. 2. Update 5.reference document, MOD 7.1 to User guideline. 3. 7.1: Add Grid size & Non-DRC checking guideline & DRC checking rule & Metalization options table. 4. Update layer mapping table & device truth table. 5. Correct 7.1.9 "B cover AA" figure and define "poly gate" forbidden drawing types. 6. Following design rule template format to add "Operation" and "Unit" column for all rule tables. 7. Adjust 7.2 rule No, because merge all guidelines to one section and combine all dummy insertion/check rule. 8. DNW: change Note1/2 as DNW.6/7[R]. 9. AA: change Note2 as AA.10c; MOD AA.10 ->AA.10a & .10b density rules. 10. NW:1) delete Note1-5 and MOD NW.3/5. 11. PSUB: 1) change Note1/2/3/5 as PSUB.9-12[R]; 2)MOD PSUB.3c. 12. delete NC/PC/HR/PDRF rules. 13. GT: 1)MOD GT.1-3b/6/7a10/11/13. 2) change GT.4a/4b to GT.4. 3) add GT.3c[R], GT.3d[R], GT.7c[R], MOD Note3 to GT.7b[R], 4)Change GT.6 "poly" to "gate poly." 14. NLL/PLL/ NLH-NLHT/ PLH-PLHT: 1) delete rule 5/9; 2) add rule 12. 15. SN: 1) MOD SN.2/9-11. 2) Add SN.12. 16. SP: 1)add SP.12; 2)MOD SP.13 to SP14[NC]. 17. CT: 1) update CT.1,7a,7b&10 2)add CT.7c, MOD schematics. 18. Merge TV1 and TM1 to 7.2.24 TV1/TM1 design rule and sperate to 4X and 2X(STV1/STM1) two options. 19. Merge TV2 and TM2 to 7.2.25 TV2/TM2 design rule and separate to 4X ,2X(STV2/STM2) and RF(UTV2/MTT2) 3 options. 20. M1: 1) MOD M1_Note as M1.6e[R], M1.8[NC], M1.9[NC], M1.10[R][NC]. 2)Add "MARKS" in pattern density check rules. 21. V1: 1)Change V1_note as rules: V1.3c[R][NC], V1.5c[R][NC],

				V1.11[R] & V1.12[R]. 2)MOD the schematics. 22. Mn, TM1,STM1, TM2, STM2, MTT2 do the same changes as M1. 23. Vn, TV1,STV1, TV2, STV2, UTV2 do the same changes as V1. 24. Add TV1.2b[R] ,TV2.2b[R],UTV2.2b[R] 25. Add UTV2/MTT2 design rules. 26. PA1: MOD Note.1~3 to [R] rule. 27. RDL Via: add "seal ring". 28. RDL: SMIC provides 14.5K and 28K RDL two process sharing the same design rule. 29. Add RDLPA2.5. 30. Add Passivation loop schematic 31. Merge AA/Poly and Mn, TM1, TM2 dummy pattern insertion and check rules into 7.2.32. 32. AA dummy: 1) AADUM.7, AADUM.20, AADUM.23 delete "DUMBP", add "MARKS". 2)MOD Note3 as AADUM.27 and Note2 as AADUMCK.1-3/5/6. 33. Poly dummy:1) PODUM.8, PODUM.20, PODUM.23 add MARKS. 2)MOD Note3 as PODUM.31and Note2 as GTDUMCK.1-3/5/6. 34. 7.2.32.5: 1)add MARKS in MnDUM.9, MnDUM.20, MnDUM32, MnDUM.35 2)add MnDUM.39, MnDUM.40 and MOD schematics. 35. Add AA/GT DUMCK.4, MnDUMCK.5 rules. 36. AA, GT DUMCK5/6, MnDUMCK.6 add MARKG/MARKF/MARKS. 37. TM1DUM/TM2DUM do the same change as Mn. 38. Add STM1/STM2/MTT2 dummy pattern insertion and check rules. 39. Add SRAM rules. 40. Merge all layout guidelines into 7.2.34. 41. MOD RESAA.1 and RESP1.1 min. width 0.5-> 0.4um and square number >5 -> ≥1; 42. MOD RESAA.9 and RESP1.9 ≥0.2 -> =0.2. 43. Add NW resistor guidelines, MOD RESNWAA.7 ≥0.2 -> =0.2and RESNWST.6 ≥0.2 -> =0.0, add RESNWST.11. 44. EFUSE: 1)update EFUSE.8 and delete EFUSE.9. 2) Add SP layer in schematics. 45. Add HRP rules. 46. LDMOS: 1)Change rules to guidelines. 2) delete LD.1b/LD.5b. 3)MOD LD.6/7/8. 4) add LD.8b/12/13 5 and schematics. 47. 7.2.34.7: Add DUP pad guidelines. 48. 7.2.34.8: 1). update SR15~18,SR33, delete SR34, SR35. 2) MOD Fig.5 MARKG->MARKS. 3) Add data type in Table.3.

				4) add seal ring check rules. 49. 7.2.34.9:update GR.1~20*, GR.18~20 delete “MARKS”. 50. 7.2.34.10:update ALFuse guidelines description. 51. 7.2.34.13:add SL.9. 52. Current Density Rule: add MTT2 and RDL 28K rules. 53. Add non-salicide poly resistors current density rule. 54. Add metal current density (AC) rules. 55. DFM: delete DFM22, MOD DFM95 rule and schematics, add DFM104 . 56. Attachment: update Seal ring GDS and add metallization Options Table. 57. Delete DTDMY layer information in 7.1.6. 58. DG/TG: update DG.5/7/12 to no use DTDMY, TG do same change. 59. 7.2.3:add NW.7a.

SEMICONDUCTOR MANUFACTURING INTERNATIONAL CORPORATION

65nm Logic Salicide 1.2/1.8/2.5/3.3V Low Leakage and 1.0/1.8/2.5/3.3V Generic Design Rules

Version 1.9

SMIC Confidential – Do Not Copy

Content

1. Title:

65nm Logic Salicide 1.2/1.8/2.5/3.3V Low Leakage and 1.0/1.8/2.5/3.3V Generic Design Rules

2. Purpose:

Patterns Design &DFM Guideline for 65nm Logic Process

3. Scope:

All SMIC Fabs

4. Nomenclature:

Pls refer detailed description in 7.1.9

5. Reference:

Items	Reference Documents
Reference Flows	TD-LO65-PF-2001
ESD and Latch up Guide Lines	TD-LO65-99-2002
Antenna Rules	TD-LO65-DR-2005

6. Responsibility:

Technology Development Center

7. Subject content

7.1 User guideline

7.1.1 Design requirements

- Design shape geometry: Polygons only
- Self-intersecting shape: Not allowed
- Shapes with acute angles: Not allowed
- Shape minimum width: Design minimum for corresponding design level
- Axes: 0 degree (X), 90 degree (Y), and 45 degree (diagonal)
- Letters and numbers: Polygons required and must satisfy design rules

- Logos: Must satisfy Logo layout guilelines 7.2.34.12

7.1.2 Grid size

Minimum Layout grid size is 0.001um.

7.1.3 Non-DRC checking guideline

1. No DRC for all layers on EXCLU (132:0) covered area.
2. No DRC for the design rules with the superscript of [NC].
3. No DRC for Notes which are below design rules tables.
4. EXDRC is used to block ROM array, no DRC for layers below M1 on EXDRC covered area.

7.1.4 DRC checking rule

1. The rules with the superscript of [R] are recommended rules which require performing DRC runset, but DRC checking is not gated for recommended rules. Pls consult with process integration engineer if customers have the doubt.
2. Pls follow guidelines for DRC checking as below:

Items	65nm
AA, NW and poly Resistor guidelines	V
Poly E-Fuse guidelines	V
HRP guidelines	V
LDMOS layout guidelines	V
DUP pad guidelines	
Seal ring layout guidelines	V
Guide ring layout guidelines	V
Al fuse guidelines	V
Fuse repairing alignment mark guidelines	V
Logo layout guidelines	
Metal slot guidelines	

7.1.5 SMIC mask layer name mapping table

7.1.5.1 65nm Logic Salicide 1.2/1.8/2.5/3.3V Low Leakage mask layer mapping table (Top Tier system Table ID LCMO65-V02)

Mask ID	Process Name	Dig. Area Tone	GDS No	Data type	Normal use	Mask Generation Formula	Description	Optional
120	AA	D	10	0	Drawn	SMICLC65LL0	Active Area	Must
292	DNW	C	19	0	Drawn	NA	Deep N well imp for substrate noise suppression	Optional
191	PW	C			Generated	SMICLC65LL0	P-Well / P-Tub	Must
491	PWH	C			Generated	SMICLC65LL0	P well I/O	Optional
494	PWHT	C			Generated	SMICLC65LL0	Pwell for triple gate IO	Optional
192	NW	C	14	0	Drawn	SMICLC65LL0	N-Well / N-Tub	Must
492	NWH	C			Generated	SMICLC65LL0	N well I/O	Optional
495	NWHT	C			Generated	SMICLC65LL0	Nwell for triple gate IO	Optional
396	VTNH	C	47	0	Drawn	NA	Layer to define N core high Vt device	Optional
596	LVN	C	219	0	Drawn	SMICLC65LL0	Layer t odefine N core low Vt device	Optional
395	VTPH	C	46	0	Drawn	NA	Layer to define P core high Vt device	Optional
595	LVP	C	218	0	Drawn	SMICLC65LL0	Layer to define P core low Vt device	Optional
193	NC	C			Generated	SMICLC65LL0	N-Cell Implant	Optional
194	PC	C			Generated	SMICLC65LL0	P-Cell Implant/NFILED	Optional
145	TG	D	125	0	Drawn	SMICLC65LL0	Triple gate	Optional
131	DG	D	29	0	Drawn	SMICLC65LL0	Dual Gate	Must
412	HR	C			Generated	SMICLC65LL0	For N+ poly Pre-doping and N+ poly resistor	Must
130	GT	D	30	0	Drawn	SMICLC65LL0	Poly Gate / Poly-1	Must
214	NLHT	C	114	0	Generated/ Drawn	SMICLC65LL0	NMOS LDD Implant for 2.5 or 3.3V IO, default generated	Optional
215	PLHT	C	115	0	Generated/ Drawn	SMICLC65LL0	PMOS LDD Implant for 2.5 or 3.3V IO, default generated	Optional

114	NLH	C	36	0	Generated/ Drawn	SMICLC65LL0	NMOS LDD Implant for 1.8V IO, default generated	Optional
115	PLH	C	37	0	Generated/ Drawn	SMICLC65LL0	PMOS LDD Implant for 1.8V IO, default generated	Optional
116	NLL	C	35	0	Generated/ Drawn	SMICLC65LL0	NMOS LDD Implant for 1.2V core, default generated	Must
113	PLL	C	38	0	Generated/ Drawn	SMICLC65LL0	PMOS LDD Implant for 1.2V core, default generated	Must
198	SN	C	40	0	Drawn	SMICLC65LL0	N+ S/D Implant	Must
197	SP	C	43	0	Drawn	NA	P+ S/D Implant	Must
416	NPR1	C	57	0	Drawn/ Generated	NA	For non-SMIC standard N+ Poly Resistor adjustment	Optional
413	HRP	C	39	0	Drawn	NA	High Resistant Poly Imp	Optional
110	ESD1	C	41	0	Drawn	SMICLC65LL0	ESD Implant	Optional
155	SAB	D	48	0	Drawn	NA	Resist Protect Oxide / Salicide Block	Must
156	CT	C	50	0	Drawn	NA	Contact Holes (Metal to Si/Poly) or slots (guard ring/seal ring use only)	Must
160	M1	C	61	0	Drawn	SMICLC65LL0	Metal-1	Must
178	V1	C	70	0	Drawn	NA	Via-1 Hole or slots (guard ring/seal ring use only)	Must
180	M2	C	62	0	Drawn	SMICLC65LL0	Metal-2	Must
179	V2	C	71	0	Drawn	NA	Via-2 Hole or slots (guard ring/seal ring use only)	Must
181	M3	C	63	0	Drawn	SMICLC65LL0	Metal-3	Must
144	TV2 (UTV2)	C	123	0	Drawn	NA	Second 4X Top Via or 4X top via connected to MTT2 or slots (guard ring/seal ring use only)	Must
143	TM2 (MTT2)	C	122	0	Drawn	SMICLC65LL0	Second 4X Top Metal, or MTT (RF production application)	Must
107	PA	C	80	0	Drawn/ Generated	SMICLC65LL0	Passivation openings for Al pads or connection holes/slots between RDL and TM2	Must
108	ALPA	D			Generated	SMICLC65LL0	AL Bonding Pads or Al lines, bumps	Must
163	MD	C			Generated	SMICLC65LL0	Passivation 2 openings for Al pads or bumps	Must

177	V3	C	72	0	Drawn	NA	Via-3 hole or slots (guard ring/seal ring use only)	Optional
182	M4	C	64	0	Drawn	SMICLC65LL0	Metal-4	Optional
176	V4	C	73	0	Drawn	NA	Via-4 holes or slots (guard ring/seal ring use only)	Optional
183	M5	C	65	0	Drawn	SMICLC65LL0	Metal-5	Optional
175	V5	C	74	0	Drawn	NA	Via-5 hole or slots (guard ring/seal ring use only)	Optional
184	M6	C	66	0	Drawn	SMICLC65LL0	Metal-6	Optional
174	V6	C	75	0	Drawn	NA	Via-6 hole or slots (guard ring/seal ring use only)	Optional
185	M7	C	67	0	Drawn	SMICLC65LL0	Metal-7	Optional
173	V7	C	76	0	Drawn	NA	Via-7 hole or slots (guard ring/seal ring use only)	Optional
186	M8	C	68	0	Drawn	SMICLC65LL0	Metal-8	Optional
142	TV1	C	121	0	Drawn	NA	4X design rule first Top Via or slots (guard ring/seal ring use only)	Optional
141	TM1	C	120	0	Drawn	SMICLC65LL0	First Top Metal for 4X design rule	Optional
442	STV1	C	243	0	Drawn	NA	First 2X Top Via or slots (guard ring/seal ring use only)	Optional
441	STM1	C	228	0	Drawn	SMICLC65LL0	First 2X Top Metal	Optional
444	STV2	C	244	0	Drawn	NA	Second 2X Top Via or slots (guard ring/seal ring use only)	Optional
443	STM2	C	229	0	Drawn	SMICLC65LL0	Second 2X Top Metal	Optional
106	FUSE	C	81	0	Drawn	NA	Fuse Window	Optional
	DUMBA		91	0	Drawn	NA	Block Layer for Dummy operation on AA (For dummy-fill utility only)	
	AADUM		10	1	Generated/ Drawn	NA	AA dummy patterns	
	DPSRAM		60	4	Drawn	NA	Marker shape to allow LVS to identity DP974 dualport SRAM cells	
	INST		60	0	Drawn	NA	cell or instance and strap outline for all SRAM only	
	PSUB		85	0	Drawn	NA	Psub area(NN)	

	DUMBP		92	0	Drawn	NA	Block Layer for Dummy operation on GT(For dummy-fill utility only)	
	GTDUM		30	1	Generated/ Drawn	NA	GT dummy patterns	
	OVERPL		125	4	Drawn	NA	Marking layer for poly overdrive from 2.5V to 3.3V and 4.1V	
	UNDEPL		125	5	Drawn	NA	Marking layer for poly underdrive from 2.5V to 1.8v	
	VARMOS		93	0	Drawn	NA	Block Layer to cover all MOS-type varactor	
	VARJUN		94	0	Drawn	NA	Block Layer to cover all Junction type varactor	
	RESAA		97	0	Drawn	NA	Dummy Pattern for AA Resistor	
	RESP1		96	0	Drawn	NA	Dummy Pattern for Poly-1 Resistor	
	RESNW		95	0	Drawn	NA	Blocking layer for NW resistor	
	LDBK		216	150	Drawn	NA	To identify LDMOS function area and do related logic operation in IMP layers	
	HRPDMY		210	0	Drawn	NA	Marking layer for LVS, DRC to define high resistance poly resistor region	
	EFUSE		81	2	Drawn	NA	Marking layer for an electrical fuse	
	DUMBM		90	0	Drawn	NA	Dummy block layers for all metal layers (For dummy-fill utility only)	
	M1DUM		61	1	Generated/ Drawn	NA	M1 dummy patterns	
	M2DUM		62	1	Generated/ Drawn	NA	M2 dummy patterns	
	M3DUM		63	1	Generated/ Drawn	NA	M3 dummy patterns	
	M4DUM		64	1	Generated/ Drawn	NA	M4 dummy patterns	
	M5DUM		65	1	Generated/ Drawn	NA	M5 dummy patterns	
	M6DUM		66	1	Generated/ Drawn	NA	M6 dummy patterns	

	M7DUM		67	1	Generated/ Drawn	NA	M7 dummy patterns	
	M8DUM		68	1	Generated/ Drawn	NA	M8 dummy patterns	
	TM1DUM		120	1	Generated/ Drawn	NA	TM1 dummy patterns	
	TM2DUM		122	1	Generated/ Drawn	NA	TM2 or MTT2 dummy patterns	
	STM1DM		228	1	Generated/ Drawn	NA	2X STM1 dummy patterns	
	STM2DM		229	1	Generated/ Drawn	NA	2X STM2 dummy patterns	
	BCB1 (RDL via)		165	0	Drawn	NA	Via under RDL connecting TM and RDL	
	RDL		166	0	Drawn	NA	Al redistributed lines, Al pads, Al bumps and Al fuse	
	BCB2 (RDL PA2)		167	0	Drawn	NA	Passivation 2 openings for RDL or Al bumps	
	NOSHR		180	150	Drawn	NA	non-shrink block layer (55nm application)	
	M1DUB		151	1	Drawn	NA	Block Layer for Dummy operation on M1 (For dummy-fill utility only)	
	M2DUB		152	1	Drawn	NA	Block Layer for Dummy operation on M2 (For dummy-fill utility only)	
	M3DUB		153	1	Drawn	NA	Block Layer for Dummy operation on M3 (For dummy-fill utility only)	
	M4DUB		154	1	Drawn	NA	Block Layer for Dummy operation on M4 (For dummy-fill utility only)	
	M5DUB		155	1	Drawn	NA	Block Layer for Dummy operation on M5 (For dummy-fill utility only)	
	M6DUB		156	1	Drawn	NA	Block Layer for Dummy operation on M6 (For dummy-fill utility only)	
	M7DUB		157	1	Drawn	NA	Block Layer for Dummy operation on M7 (For dummy-fill utility only)	
	M8DUB		158	1	Drawn	NA	Block Layer for Dummy operation on M8 (For dummy-fill utility only)	

	TM1DUB		193	1	Drawn	NA	Block Layer for Dummy operation on TM1 (For dummy-fill utility only)	
	TM2DUB		194	1	Drawn	NA	Block Layer for Dummy operation on TM2 or MTT2 (For dummy-fill utility only)	
	STM1DB		194	5	Drawn	NA	Block Layer for Dummy operation on STM1 (For dummy-fill utility only)	
	STM2DB		194	4	Drawn	NA	Block Layer for Dummy operation on STM2 (For dummy-fill utility only)	
	NODMF		180	0	Drawn	NA	AA/GT/Metal Dummy block layer (For dummy-fill utility only)	
	MARKG		189	0	Drawn	NA	Guard ring area mark layer for DRC and dummy insertion blockage for dummy fill utility	
	MARKF		190	0	Drawn	NA	Fuse area mark for Fuse DRC check and dummy insertion blockage for dummy fill utility	
	MARKS		189	151	Drawn	NA	Seal ring (chip level) marking layer for DRC and dummy auto-filling blockage for dummy fill utility	

7.1.5.2 65nm logic 1P10M salicide 1.0/1.8/2.5/3.3V generic mask layer mapping table (Top Tier system: Table ID. LCMO65-V03)

Mask ID	Process Name	Dig. Area Tone	GDS No	Data type	Normal use	Mask Generation Formula	Description	Optional
120	AA	D	10	0	Drawn	SMICLC65GE0	Active Area	Must
292	DNW	C	19	0	Drawn	NA	Deep N well imp for substrate noise suppression	Optional
191	PW	C			Generated	SMICLC65GE0	P-Well / P-Tub	Must
491	PWH	C			Generated	SMICLC65GE0	P well I/O	Optional
494	PWHT	C			Generated	SMICLC65GE0	Pwell for triple gate IO	Optional
192	NW	C	14	0	Drawn	SMICLC65GE0	N-Well / N-Tub	Must
492	NWH	C			Generated	SMICLC65GE0	N well I/O	Optional
495	NWHT	C			Generated	SMICLC65GE0	Nwell for triple gate IO	Optional
396	VTNH	C	47	0	Drawn	NA	Layer to define N core high Vt device	Optional
596	LVN	C	219	0	Drawn	SMICLC65GE0	Layer to define N core low Vt device	Optional
395	VTPH	C	46	0	Drawn	NA	Layer to define P core high Vt device	Optional
595	LVP	C	218	0	Drawn	SMICLC65GE0	Layer to define P core low Vt device	Optional
193	NC	C			Generated	SMICLC65GE0	N-Cell Implant	Optional
194	PC	C			Generated	SMICLC65GE0	P-Cell Implant/NFILED	Optional
145	TG	D	125	0	Drawn	SMICLC65GE0	Triple gate	Optional
131	DG	D	29	0	Drawn	SMICLC65GE0	Dual Gate	Must
412	HR	C			Generated	SMICLC65GE0	For N+ poly Pre-doping and N+ poly resistor	Must
148	PDRF	C			Generated	SMICLC65GE0	P+ Poly Pre-doping	Must
130	GT	D	30	0	Drawn	SMICLC65GE0	Poly Gate / Poly-1	Must
214	NLHT	C	114	0	Generated/ Drawn	SMICLC65GE0	NMOS LDD Implant for 2.5 or 3.3V IO, default generated	Optional
215	PLHT	C	115	0	Generated/ Drawn	SMICLC65GE0	PMOS LDD Implant for 2.5 or 3.3V IO, default generated	Optional

114	NLH	C	36	0	Generated/ Drawn	SMICLC65GE0	NMOS LDD Implant for 1.8V IO , default generated	Optional
115	PLH	C	37	0	Generated/ Drawn	SMICLC65GE0	PMOS LDD Implant for 1.8V IO, default generated	Optional
116	NLL	C	35	0	Generated/ Drawn	SMICLC65GE0	NMOS LDD Implant for 1.0V core, default generated	Must
113	PLL	C	38	0	Generated/ Drawn	SMICLC65GE0	PMOS LDD Implant for 1.0V core, default generated	Must
198	SN	C	40	0	Drawn	SMICLC65GE0	N+ S/D Implant	Must
197	SP	C	43	0	Drawn	NA	P+ S/D Implant	Must
416	NPR1	C	57	0	Drawn/ Generated	NA	For non-SMIC standard N+ Poly Resistor adjustment	Optional
413	HRP	C	39	0	Drawn	NA	High Resistant Poly Imp	Optional
110	ESD1	C	41	0	Drawn	SMICLC65GE0	ESD Implant	Optional
155	SAB	D	48	0	Drawn	NA	Resist Protect Oxide / Salicide Block	Must
301	SM	C			Generated	SMICLC65GE0	Area open to the removal of stress nitride	Must
156	CT	C	50	0	Drawn	NA	Contact Holes (Metal to Si/Poly) or slots (guard ring/seal ring use only)	Must
160	M1	C	61	0	Drawn	SMICLC65GE0	Metal-1	Must
178	V1	C	70	0	Drawn	NA	Via-1 Hole or slots (guard ring/seal ring use only)	Must
180	M2	C	62	0	Drawn	SMICLC65GE0	Metal-2	Must
179	V2	C	71	0	Drawn	NA	Via-2 Hole or slots (guard ring/seal ring use only)	Must
181	M3	C	63	0	Drawn	SMICLC65GE0	Metal-3	Must
144	TV2 (UTV2)	C	123	0	Drawn	NA	Second 4X Top Via or 4X top via connected to MTT2 or slots (guard ring /seal ring use only)	Must
143	TM2 (MTT2)	C	122	0	Drawn	SMICLC65GE0	Second 4X Top Metal, or MTT (RF production application)	Must
107	PA	C	80	0	Drawn/Gen erated	SMICLC65GE0	Passivation openings for Al pads or connection holes/slots between RDL and TM2	Must
108	ALPA	D			Generated	SMICLC65GE0	AL Bonding Pads or Al lines, bumps	Must

163	MD	C			Generated	SMICLC65GE0	Passivation 2 openings for Al pads or bumps	Must
177	V3	C	72	0	Drawn	NA	Via-3 hole or slots (guard ring/seal ring use only)	Optional
182	M4	C	64	0	Drawn	SMICLC65GE0	Metal-4	Optional
176	V4	C	73	0	Drawn	NA	Via-4 holes or slots (guard ring/seal ring use only)	Optional
183	M5	C	65	0	Drawn	SMICLC65GE0	Metal-5	Optional
175	V5	C	74	0	Drawn	NA	Via-5 hole or slots (guard ring/seal ring use only)	Optional
184	M6	C	66	0	Drawn	SMICLC65GE0	Metal-6	Optional
174	V6	C	75	0	Drawn	NA	Via-6 hole or slots (guard ring/seal ring use only)	Optional
185	M7	C	67	0	Drawn	SMICLC65GE0	Metal-7	Optional
173	V7	C	76	0	Drawn	NA	Via-7 hole or slots (guard ring/seal ring use only)	Optional
186	M8	C	68	0	Drawn	SMICLC65GE0	Metal-8	Optional
142	TV1	C	121	0	Drawn	NA	First Top Via or slots for 4X design rule (guard ring/seal ring use only)	Optional
141	TM1	C	120	0	Drawn	SMICLC65GE0	First Top Metal for 4X design rule	Optional
442	STV1	C	243	0	Drawn	NA	First 2X Top Via or slots (guard ring/seal ring use only)	Optional
441	STM1	C	228	0	Drawn	SMICLC65GE0	First 2X Top Metal	Optional
444	STV2	C	244	0	Drawn	NA	Second 2X Top Via or slots (guard ring/seal ring use only)	Optional
443	STM2	C	229	0	Drawn	SMICLC65GE0	Second 2X Top Metal	Optional
106	FUSE	C	81	0	Drawn	NA	Fuse Window	Optional
	DUMBA		91	0	Drawn	NA	Block Layer for Dummy operation on AA (For dummy-fill utility only)	
	AADUM		10	1	Generated/ Drawn	NA	AA dummy patterns	
	DPSRAM		60	4	Drawn	NA	Marker shape to allow LVS to identity DP974 dualport SRAM cells	

	INST		60	0	Drawn	NA	cell or instance outline for all SRAM	
	PSUB		85	0	Drawn	NA	Psub area(NN)	
	RESP1		96	0	Drawn	NA	Dummy Pattern for Poly-1 Resistor	
	RESAA		97	0	Drawn	NA	Dummy Pattern for AA Resistor	
	RESNW		95	0	Drawn	NA	Blocking layer for NW resistor	
	DUMBP		92	0	Drawn	NA	Block Layer for Dummy operation on GT (For dummy-fill utility only)	
	GTDUM		30	1	Generated/ Drawn	NA	GT dummy patterns	
	OVERPL		125	4	Drawn	NA	Marking layer for poly overdrive from 2.5V to 3.3V and 4.1V	
	UNDEPL		125	5	Drawn	NA	Marking layer for poly underdrive from 2.5V to 1.8v	
	HRPDMY		210	0	Drawn	NA	Marking layer for LVS, DRC to define high resistance poly resistor region	
	VARMOS		93	0	Drawn	NA	Block Layer to cover all MOS-type varactor	
	VARJUN		94	0	Drawn	NA	Block Layer to cover all Junction type varactor	
	DUMBM		90	0	Drawn	NA	Dummy block layers for all metal layers (For dummy-fill utility only)	
	M1DUM		61	1	Generated/ Drawn	NA	M1 dummy patterns	
	M2DUM		62	1	Generated/ Drawn	NA	M2 dummy patterns	
	M3DUM		63	1	Generated/ Drawn	NA	M3 dummy patterns	
	M4DUM		64	1	Generated/ Drawn	NA	M4 dummy patterns	
	M5DUM		65	1	Generated/ Drawn	NA	M5 dummy patterns	
	M6DUM		66	1	Generated/ Drawn	NA	M6 dummy patterns	
	M7DUM		67	1	Generated/ Drawn	NA	M7 dummy patterns	

	M8DUM		68	1	Generated/ Drawn	NA	M8 dummy patterns	
	TM1DUM		120	1	Generated/ Drawn	NA	TM1 dummy patterns	
	TM2DUM		122	1	Generated/ Drawn	NA	TM2 or MTT2 dummy patterns	
	STM1DM		228	1	Generated/ Drawn	NA	2X STM1 dummy patterns	
	STM2DM		229	1	Generated/ Drawn	NA	2X STM2 dummy patterns	
	BCB1 (RDL via)		165	0	Drawn	NA	Via under RDL connecting TM and RDL	
	RDL		166	0	Drawn	NA	Al redistributed lines, Al pads, Al bumps and Al fuse	
	BCB2 (RDL PA2)		167	0	Drawn	NA	Passivation 2 openings for RDL or Al bumps	
	NODMF		180	0	Drawn	NA	AA/GT/Metal Dummy block layer (For dummy-fill utility only)	
	EFUSE		81	2	Drawn	NA	Marking layer for an electrical fuse	
	LDBK		216	150	Drawn	NA	To identify LDMOS function area and do related logic operation in IMP layers	
	M1DUB		151	1	Drawn	NA	Block Layer for Dummy operation on M1 (For dummy-fill utility only)	
	M2DUB		152	1	Drawn	NA	Block Layer for Dummy operation on M2 (For dummy-fill utility only)	
	M3DUB		153	1	Drawn	NA	Block Layer for Dummy operation on M3 (For dummy-fill utility only)	
	M4DUB		154	1	Drawn	NA	Block Layer for Dummy operation on M4 (For dummy-fill utility only)	
	M5DUB		155	1	Drawn	NA	Block Layer for Dummy operation on M5 (For dummy-fill utility only)	
	M6DUB		156	1	Drawn	NA	Block Layer for Dummy operation on M6 (For dummy-fill utility only)	
	M7DUB		157	1	Drawn	NA	Block Layer for Dummy operation on M7 (For dummy-fill utility only)	

	M8DUB		158	1	Drawn	NA	Block Layer for Dummy operation on M8 (For dummy-fill utility only)	
	TM1DUB		193	1	Drawn	NA	Block Layer for Dummy operation on TM1 (For dummy-fill utility only)	
	TM2DUB		194	1	Drawn	NA	Block Layer for Dummy operation on TM2 or MTT2 (For dummy-fill utility only)	
	STM1DB		194	5	Drawn	NA	Block Layer for Dummy operation on STM1 (For dummy-fill utility only)	
	STM2DB		194	4	Drawn	NA	Block Layer for Dummy operation on STM2 (For dummy-fill utility only)	
	MARKG		189	0	Drawn	NA	Guard ring-area mark layer for DRC and dummy insertion blockage for dummy-fill utility	
	MARKF		190	0	Drawn	NA	Fuse area mark for Fuse DRC check and dummy insertion blockage for dummy-fill utility	
	MARKS		189	151	Drawn	NA	Seal ring (chip level) marking layer for DRC and dummy auto-filling blockage for dummy-fill utility	

7.1.6 Accessorial layers

Design layer name	GDS layer number	Data type	Description
JVARDUM	183	0	Junction varactor recognition layer for DRC/LVS
LOGO	26	0	LOGO;L mark area
EXCLU	132	0	DRC block layer
STIDMY	215	0	Dummy layer for LDMOS drain side STI plate DRC check
STSRAM	60	1	Marker layer to allow LVS to identity Q525 SRAM cells
DNSRAM	60	2	Marker layer to allow LVS to identity Q62 SRAM cells
UDSRAM	60	3	Marker layer to allow LVS to identity Q499 SRAM cells
RFSRAM	60	9	Marker layer to allow LVS to identity F1158 SRAM cells
INDMY	212	0	Dummy layer for MTT2 in inductor applications
EXDRC	239	0	Dummy layer for unDRC area in SRAM and ROM array
EXDFM	239	1	Dummy layer to identify DFM error waiver areas (must be approved by SMIC DFM group)
GTFUSE	81	1	Poly E-Fuse block layer for function area
MOMDMY	211	1	MOM recogonization layer
BORDER	127	0	Top Structure's Border
M1R	171	0	M1 resistor layer
M2R	172	0	M2 resistor layer
M3R	173	0	M3 resistor layer
M4R	174	0	M4 resistor layer
M5R	175	0	M5 resistor layer
M6R	176	0	M6 resistor layer
M7R	177	0	M7 resistor layer

M8R	178	0	M8 resistor layer
TM1R	201	0	TM1 resistor layer
TM2R	202	0	TM2 resistor layer
ALPAR	83	1	ALPA resistor layer
DNWTR	19	2	LVS six terminal DNW MOS
DPSRAM	60	4	Marker shape to allow LVS to identity DP974 dualport SRAM cells
RESP3T	96	1	Dummy layer for Poly-1 Resistor with 3 terminal
MOSCKT	131	2	LVS dummy layer to distinguish bsim mos and subckt mos
RESCKT	131	3	LVS dummy layer for subckt resistor
SUBD	131	1	LVS substrate separation layer
ESD5V	133	1	Dummy layer for 5V tolerant I/O device identification
ESDIO1	133	0	Dummy layer for SMIC Internal ESD devices and protection circuits
ESDIO2	133	3	Dummy layer for SMIC external ESD devices and protection circuits
DMPNP	134	0	Parasitic PNP
CAPBP	137	0	Capacitor Bottom Plate
DSTR	138	0	Diode Marker (identifies a diode, for LVS only)
DCTY	139	0	Area with no Extraction for LVS
RFDEV	181	0	DRC/LVS mark layer for RF device
RFDN6T	181	4	6-terminal RF MOS in deep NWELL for LVS,the sixth terminal is psub.
RFSD	181	3	RF MOS of even finger with S/D permute for LVS
RFMOSD	182	0	DRC/LVS mark layer for RF mos drain terminal
RF3T	183	2	DRC/LVS mark layer for RF 3 terminal devices and 3 terminal MOM

Note:

1. Mask NWH/NWHT, PWH/PWHT and PW are generated from NW, DG, TG, AA, SP/SN and (or) PSUB patterns. There is no need for customers to draw these layers specifically.
2. The LDD patterns are generated by logic operations. Dummy block layer is used to block AA and poly resistors. The logic operation will NOT add LDD patterns onto poly and AA resistor.

3. The HR and PDRF patterns are generated by logic operations. Dummy block layer is used to block AA and poly resistors. The logic operation will ADD HR patterns onto N+ poly resistor. The logic operation will NOT ADD PDRF patterns onto P+ poly resistor.
4. Please refer the below table for LOTA file No.:

File No.	Description
SMICLC65GE0	For Generic flow
SMICLC65LL0	For LL flow

5. EXCLU layer boundary should not cut through the function patterns.
6. INST is used to block all SRAM cell. Please follow SRAM rules for M2 and lower layers on INST covered area.
7. EXDFM layer can be applied to exclude DFM rule check at M2 layer and below upon approval from SMIC DFM group.

7.1.7 Metallization Options Table

Metal options definition scheme is denoted in this section for metal layer, and is limited only to those options present in the table.

The scheme uses the following naming: xPyM_(y-v-z-w)Ic_vSTMc_zTMc_wMTTc_ALPAu

Where:

P = poly layers,

M = total metal layers excluding AL pad/Al RDL,

Ic= Cu inter metal layers,

TMc= Cu top metal layers,

MTTc=Cu Ultra thick metal,

STMc=Cu 2X top metal layers (0.2um design)

ALPA = AL pad/AI RDL

x = number of poly layers,

y = number of total metal layers,

z = number of top metal layers,

w = number of Ultra thick metal layers.

v = number of 2X top metal layers.

u = type of AL, 1 type AL14.5k, 2 type AL28k .

For (y-1)=0 or z=0 or w =0 or v=0 process , the naming of metallization table don't include C or TM or MTT or TMB.

65nm LG metal option.xls

7.1.8 Device truth table

7.1.8.1 Device implant truth table

SMIC		1.2v NMOS			1.2v PMOS			1.8V IO		2.5V/3.3V IO		Native			HVT SRAM		SVT SRAM	
implant step	mask ID	SVT	HVT	LVT	SVT	HVT	LVT	N	P	N	P	Core	1.8V IO	2.5V/ 3.3V IO	PU	PD, PG	PU	PD, PG
PW	191	V	V	V												V		V
PWH	491							V										
PWHT	494									V								
NW	192				V	V	V								V		V	
NWH	492								V									
NWHT	495										V							
VTNH	396		V													V		
VTPH	395					V									V			
LVN	596	V	V													V		v
LVP	595				V	V									v		V	
NC	193																	V
HR	412	V	V	V				V		V		V	V	V		V		V
PDRF (for G only)	148				V	V	V		V		V				V		V	
NLL	116	V	V	V								V				V		V
NLH	114							V					V					
NLHT	214									V				V				
PLL	113				V	V	V								V		V	
PLH	115								V									
PLHT	215										V							
SN	198	V	V	V				V		V		V	V	V		V		V
SP	197				V	V	V		V		V				V		V	

7.1.8.2 Device layout truth table

SMIC				1.2v NMOS			1.2v PMOS			1.8V IO		2.5V /3.3 V IO		2.5V overdrive to 3.3V(4.1 V)		2.5V underdrive to 1.8V		LDMOS (Drain5V, Gate2.5V)		Native					Efuse	HVT SRAM		SVT SRAM	
Layer name	GDS #	Data type	mask ID	SVT	HVT	LVT	SVT	HVT	LVT	N	P	N	P	N	P	N	P	N	P	Core 1.8V IO	2.5V/3.3V IO	2.5V overdrive to 3.3V	2.5V underdrive to 1.8V			PU	PD, PG	PU	PD, PG
AA	10	0	120	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V		V	V	V	V
NW	14	0	192				V	V	V		V		V		V		V	V	V							V		V	
VTNH	47	0	396		V																						V		
VTPH	46	0	395					V																		V			
LVN	219	0	596			V																							
LVP	218	0	595						V																				
TG	125	0	145									V	V	V	V	V	V	V	V			V	V	V					
DG	29	0	131							V	V										V								
GT	30	0	130	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
SN	40	0	198	V	V	V				V		V		V		V		V		V	V	V	V	V			V		V
SP	43	0	197				V	V	V		V		V		V		V		V						V	V		V	
PSUB	85	0																		V	V	V	V	V					
OVERPL	125	4												V	V								V						
UNDERPL	125	5														V	V							V					
LDBK	216	150																V	V										
STIDMY	215	0																V	V										
EFUSE	81	2																							V				
GTFUSE	81	1																							V				

7.1.8.3 Bipolar Junction Transistor (BJT) implant truth table

SMIC		BJT Core		BJT 1.8V		BJT 2.5V	
implant step	mask ID	NPN	PNP	NPN	PNP	NPN	PNP
DNW	292	V		V		V	
PW	191	V	V				
PWH	491			V	V		
PWHT	494					V	V
NW	192	V	V				
NWH	492			V	V		
NWHT	495					V	V
NLL	116	V (only into N+ emitter)					
NLH	114			V (only into N+ emitter)			
NLHT	214					V (only into N+ emitter)	
PLL	113		V (only into P+ emitter)				
PLH	115				V (only into P+ emitter)		
PLHT	215						V (only into P+ emitter)
SN	198	V(into N+ emitter and Nwell pickup)	V(into Nwell pickup)	V(into N+ emitter and Nwell pickup)	V(into Nwell pickup)	V(into N+ emitter and Nwell pickup)	V(into Nwell pickup)
SP	197	V (into Pwell pickup)	V (into P+ emitter and Pwell pickup)	V (into Pwell pickup)	V (into P+ emitter and Pwell pickup)	V (into Pwell pickup)	V (into P+ emitter and Pwell pickup)

7.1.8.4 Bipolar Junction Transistor (BJT) layout truth table

SMIC			BJT Core		BJT 1.8V		BJT 2.5V	
Layer Name	GDS #	mask ID	NPN	PNP	NPN	PNP	NPN	PNP
AA	10	120	V	V	V	V	V	V
DNW	19	292	V		V		V	
NW	14	192	V	V	V	V	V	V
TG	125	145					V	V
DG	29	131			V	V		
SN	40	198	V(emitter and Nwell pickup)	V(Nwell pickup)	V(N+ emitter and Nwell pickup)	V(Nwell pickup)	V(N+ emitter and Nwell pickup)	V(Nwell pickup)
SP	43	197	V (Pwell pickup)	V (P+ emitter and Pwell pickup)	V (Pwell pickup)	V (P+ emitter and Pwell pickup)	V (Pwell pickup)	V (P+ emitter and Pwell pickup)

7.1.8.5 Resistor implant truth table

SMIC		N+ Poly Resistor	P+ Poly Resistor	AA Resistor		NW Resistor		High Poly Resistor
implant step	mask ID	normal (HR +SN)	normal (SP)	N+ AA (SN)	P+ AA (SP)	under AA (NW)	under STI (NW)	
PW	191			V				
NW	192				V	V	V	
LVN	596			V				
LVP	595				V	V	V	
HR	412	V						
PDRF(for G only)	148							
SN	198	V		V	V(for Nwell pickup only)	v	v	
SP	197		V	V(for psub pickup only)	V	V(for psub pickup only)	V(for psub pickup only)	V(for pickup only)
HRP	413							V

7.1.8.6 Resistor layout truth table

SMIC			N+ Poly Resistor	P+ Poly Resistor	AA Resistor		NW Resistor		High Poly Resistor
layer name	GDS #	mask ID	normal (HR +SN)	normal (SP)	N+ AA (SN)	P+ AA (SP)	Under AA (NW)	under STI (NW)	
AA	10	120			V	V	V		
NW	14	192				V	V	V	
GT	30	130	V	V					V
SN	40	198	V		V	V(for Nwell pickup only)	v	v	
SP	43	197		V	V (for psub pickup only	V	V (for psub pickup only)	V (for psub pickup only)	V(for pick up only)
SAB	48	155	V	V	V	V	**V**		V
NPR1	57	416							
RESP1	96		V	V					
RESAA	97				V	V			
RESNW	95						V	V	
HRP	39	413							V
HRPDMY	210								V

7.1.8.7 Varactor implant truth table

SMIC		PFET in PW MOSVAR			NFET in NW MOSVAR			P+/NW JUNVAR	N+/PW JUNVAR
implant step	mask ID	1.2V	1.8V	2.5V/3.3V	1.2V	1.8V	2.5V/3.3V		
DNW	292	V (optional)	V (optional)	V (optional)	V (optional)	V (optional)	V (optional)		
PW	191	V							V
PWH	491		V						
PWHT	494			V					
NW	192				V			V	
NWH	492					V			
NWHT	495						V		
LVN	596				V				V
LVP	595	V						V	
HR	412				V	V	V		
PDRF (for G only)	148	V	V	V					
NLL	116								V
PLL	113							V	
SN	198	V (only at pickup area)	V (only at pickup area)	V (only at pickup area)	V	V	V	V (only at pickup area)	V
SP	197	V	V	V	V (only at pickup area)	V (only at pickup area)	V (only at pickup area)	V	V (only at pickup area)

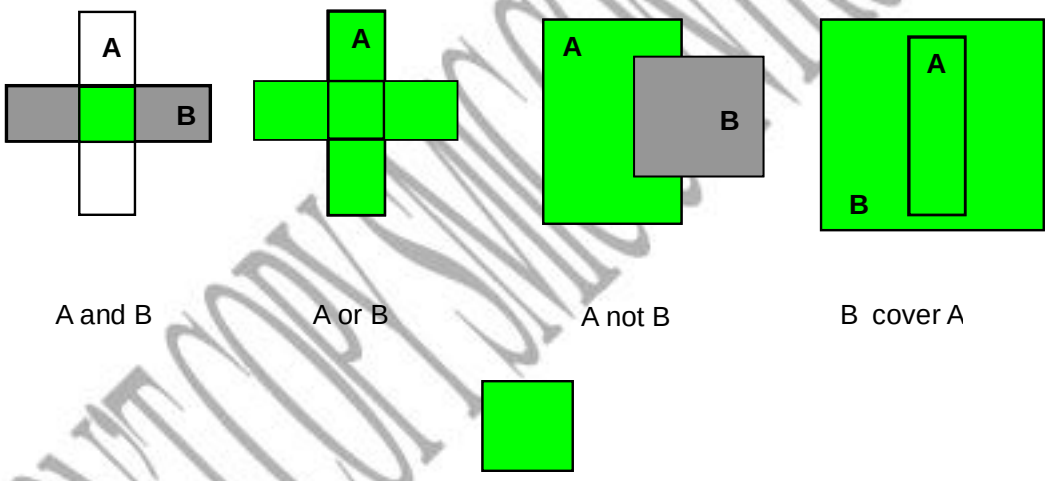
7.1.8.8 Varactor layout truth table

SMIC			PFET in PW MOSVAR			NFET in NW MOSVAR			P+/NW JUNVAR	N+/PW JUNVAR
implant step	GDS #	mask ID	1.2V	1.8V	2.5V/3.3V	1.2V	1.8V	2.5V/3.3V		
AA	10	120	V	V	V	V	V	V	V	V
DNW	19	292	V (optional)	V (optional)	V (optional)	V (optional)	V (optional)	V (optional)		
NW	14	192	V (only at pickup area)	V (only at pickup area)	V (only at pickup area)	V	V	V	V	
TG	125	145			V			V		
DG	29	131		V			V			
GT	30	130	V	V	V	V	V	V		
SN	40	198	V (for NW pickup)	V (for NW pickup)	V (for NW pickup)	V	V	V	V (only at pickup area)	V
SP	43	197	V	V	V	V (for PW pickup)	V (for PW pickup)	V (for PW pickup)	V	V (only at pickup area)
VARMOS	93		V	V	V	V	V	V		
VARJUN	94								V	V

7.1.9 Design Rules Nomenclatures and Abbreviations

(A) Logic Function Definitions

Logic Function	Definition
A and B	Define the intersection area of A and B
A or B	Define the union area of A and B
A not B	Define the area of A excluding the common area of A and B
B cover A	Define the B area where there is A inside B.



(B) Nomenclatures and Abbreviations

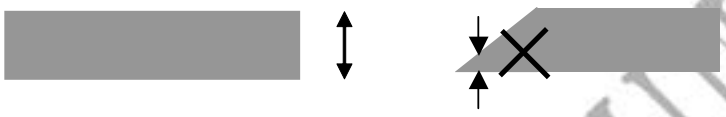
Name	Definitions
PW	Not (NW or PSUB).
Gate	A poly pattern used as transistor gate is defined as a gate poly, which can be produced by the overlap of an AA layer (excluding dummy AA) and a Poly layer (excluding dummy poly).
Channel Length	The dimension (from GT edge to GT edge) over AA.
Channel Width	The dimension (from AA edge to AA edge) over GT.

MOS AA	MOS AA refers to an AA that is part of a transistor active area. When a poly pattern is on top of an AA, the AA is treated as MOS AA. If there is no poly pattern on top of an AA, the AA is not a MOS AA. Dummy AA is not a MOS AA.
N+AA	(AA and SN) not GT.
P+AA	(AA and SP) not GT.
N+ pick-up AA	SN and AA island or stick in n-type area, used as a connection point for electric stress.
P+ pick-up AA	SP and AA island or stick in p-type area, used as a connection point for electric stress.
Field oxide	Not (AA or AADUM)
STI	Not (AA or AADUM)
Different or same net	Electrically based connectivity using all conducting layers (unless otherwise noted), including diffusion, poly, and all back-end-of-line (BEOL) metal and via layers in the stack (M1 through last metal). It also includes connectivity through the substrate, through n-wells and p-wells and between n-wells through the deep n-well (for triple-well designs).

7.1.10 Definition of terminology used in these design rules

1. Width

- Distance from one inside edge to a parallel inside edge within a shape along the shorter dimension of the shape.



2. Length

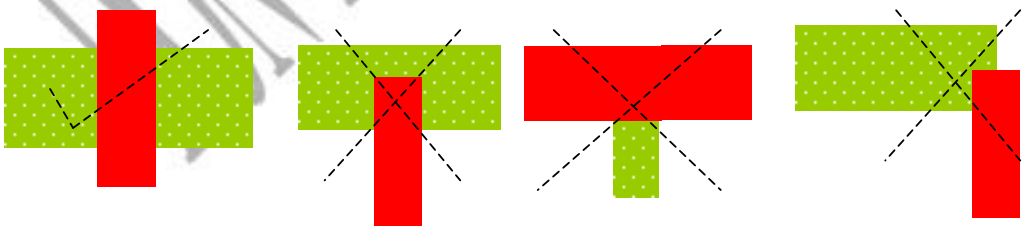
- Distance from one inside edge to a parallel inside edge within a same rectangular shape along the longer dimension of the shape.

3. Space

- Distance between the outside edge of a shape to a parallel outside edge of another shape on the same layer.
- The word "space" is also generally used to denote separation of shapes, whether or not they are on the same layer.
- On the same layer, when runlength=<0, only VTNH,VTPH,LVN,LVP,NC,PC, SN, SP layers can skip space check.

4. Gate poly:

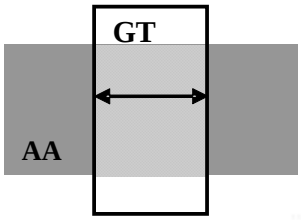
- If designers draw the gate poly, type (b) (c) and (d) is forbidden.



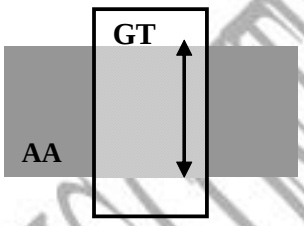
(a) **(b)** **(c)** **(d)**

Poly **AA**

- Channel Length: The dimension from GT edge to GT edge over AA.

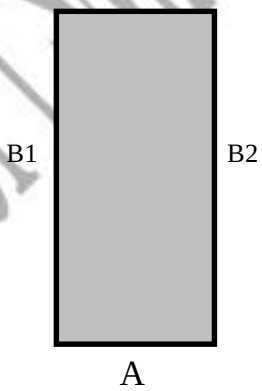


- Channel Width: The dimension from AA edge to AA edge over GT.



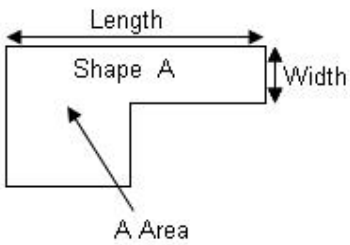
5. Poly End

- The edge A when A ≤ 0.14um, and B1,B2 >0.14um



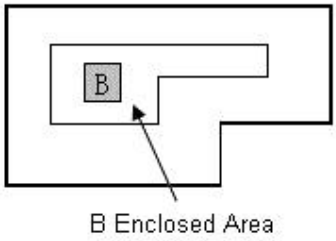
6. Area

- The area of the shape



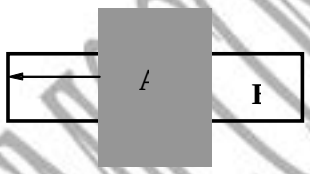
7. Enclosed Area

- The space between the outside edges of one or more shapes.



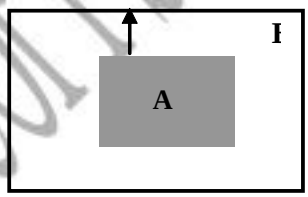
8. Extension

- Layer B shape extends outside layer A shape in one direction, with no restriction on the other directions.
- The minimum distance from the outside edge of the layer A shape to the inside edge of the layer B shape.



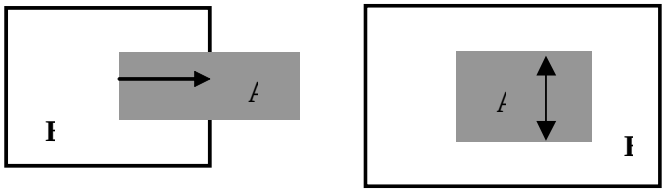
9. Enclosure

- A enclosed by B: The layer A shape is completely within the layer B shape.
- The minimum distance from the outside edge of A to the inside edge of B in all directions.
- The layer A shape can not extend past the layer B shape in any direction.



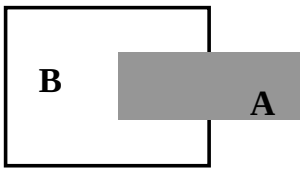
10. Overlap

- The layer A shape crosses a boundary of the layer B shape, or the layer A shape is completely enclosed by the layer B shape.
- The distance:
- (1) This distance from the inside edge of the layer A shape to the inside edge of the layer B shape.
- (2) The distance is also the width of the layer A shape for enclosed A.



11. Straddle

- When the layer A shape crosses a boundary of the layer B shape.

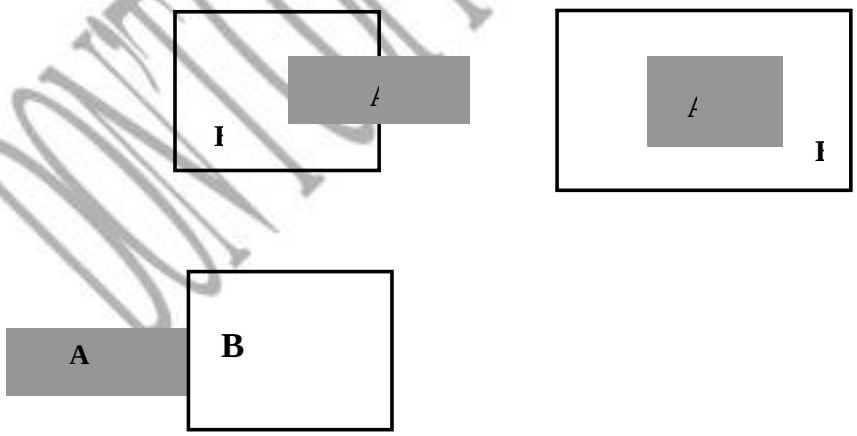


12. Butted

- When the layer A shape meets without going beyond a boundary of the layer B shape.

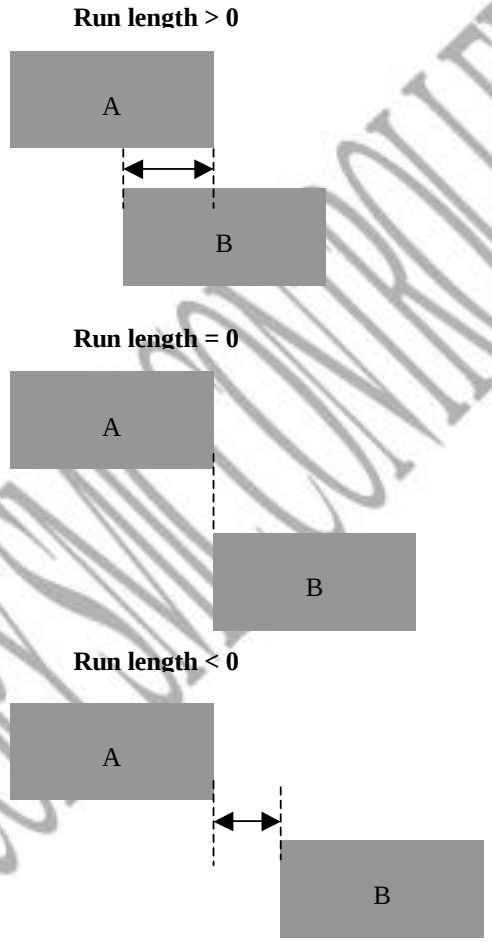
13. Interact with

- When the layer A shape overlaps or crosses or meets the layer B shape, interact with include overlap, straddle, butted three condition.



14. Run length

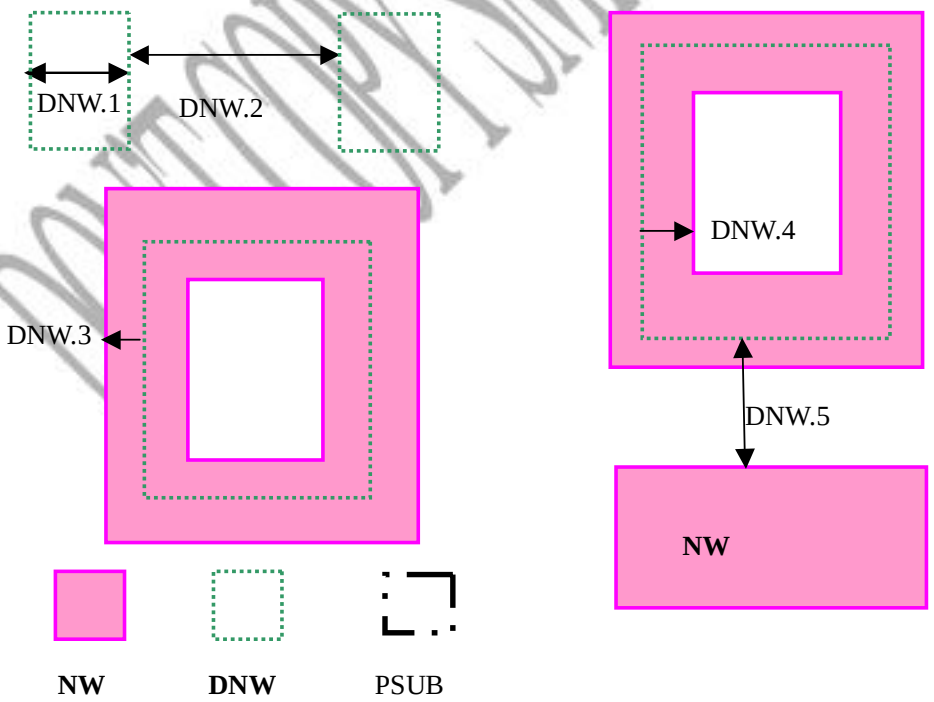
- The distance in which two lines continuously run alongside one another.



7.2 Layout Rule Description

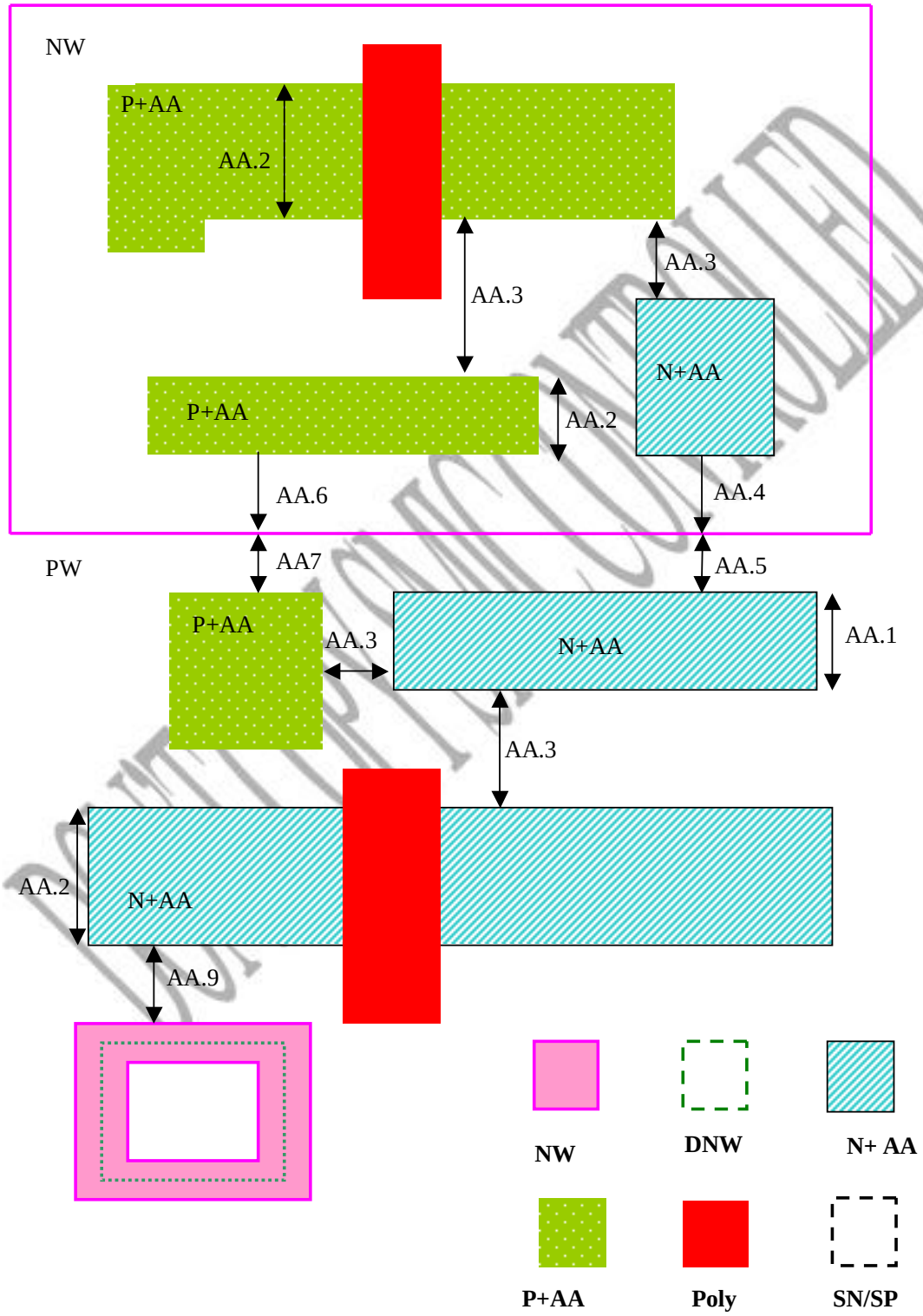
7.2.1 DNW: Deep N-Well design rules

Rules number	Description	Operation	Design Value	Unit
DNW.1	DNW width	≥	3.00	um
DNW.2	Space between two DNWs	≥	3.50	um
DNW.3	NW Enclosure of DNW	≥	1.00	um
DNW.4	Overlap of NW and DNW	≥	0.40	um
DNW.5	Space between DNW and NW	≥	2.50	um
DNW.6[R]	DNW is enclosed by NW			
DNW.7[R]	DNW is not allowed in native device region.			



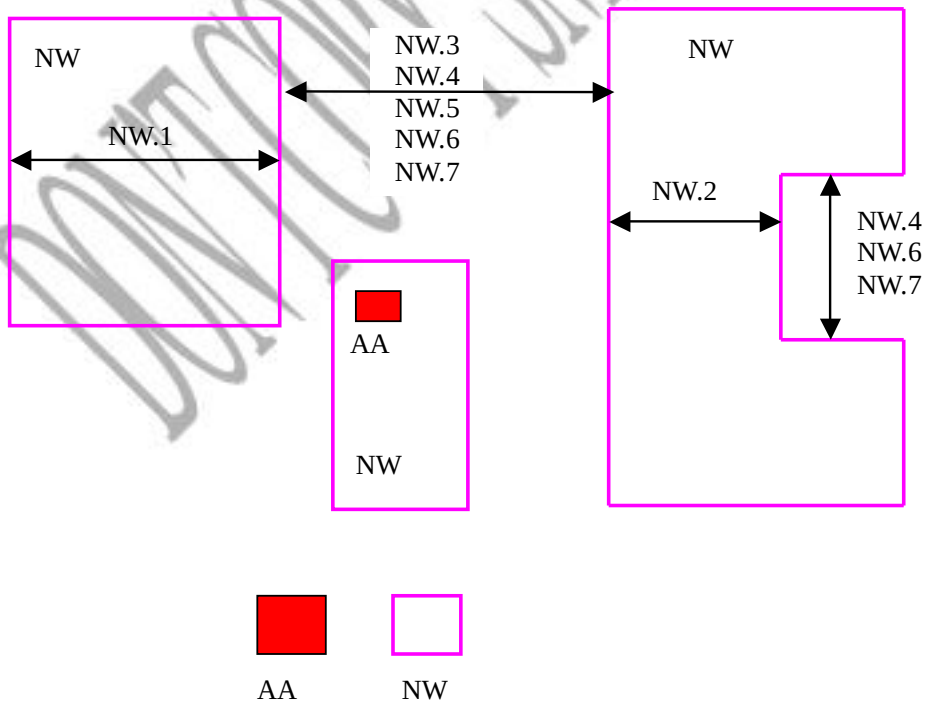
7.2.2 AA: Active area design rules

Rules number	Description	Operation	Design Value	Unit
AA.1	Width of interconnect AA	≥	0.08	um
AA.2a	Channel width for 1.0/1.2V NMOS/PMOS transistors	≥	0.11	um
AA.2b	Channel width for 1.8/2.5/3.3V NMOS/PMOS transistors	≥	0.21	um
AA.3a	Space between two AAs in the same well	≥	0.10	um
AA.3b	Space between AAs when one or both AA width greater than 0.15um in the same well	≥	0.11	um
AA.4	N+AA enclosed by NW	≥	0.12	um
AA.5	Space between NW and N+AA inside PW	≥	0.15	um
AA.6	P+AA enclosed by NW	≥	0.15	um
AA.7	Space between NW and P+AA inside PW	≥	0.12	um
AA.8	AA area	≥	0.038	um^2
AA.9	Space between N+AA, which is not enclosed by DNW, and NW which encloses a DNW	≥	0.32	um
AA.10a	Local AA density (including dummy AA) in 200umX200um window with step size 100um	≥	19%	
		≤	90%	
AA.10b[R]	Global AA density for fully chip (including dummy AA)	≥	23%	
		≤	75%	
AA.10c[R]	AA density inside of dummy block area,while the area of dummy block layer is larger than 2500um^2 (50umX50um)	≥	23%	



7.2.3 NW: N-Well rule

Rules number	Description	Operation	Design Value	Unit
NW.1	NW width	≥	0. 36	um
NW.2	NW width for NW resistor	≥	1.60	um
NW.3	Space between 1.0/1.2V NWs at the same nets	≥	0. 36	um
NW.4	Space between 1.0/1.2V NWs at different nets	≥	0.47	um
NW.5	Space between 1.0/1.2V and 1.8/2.5/3.3V NWs at the same nets.	≥	0.47	um
NW.6	Space between 1.0/1.2V NW and 1.8/2.5/3.3V NW at different nets.	≥	0.72	um
NW.7a	Space between 1.8/2.5/3.3V NWs at same nets.	≥	0.47	um
NW.7b	Space between 1.8/2.5/3.3V NWs at different nets.	≥	0.72	um
NW.8	NW area	≥	0.30	um^2

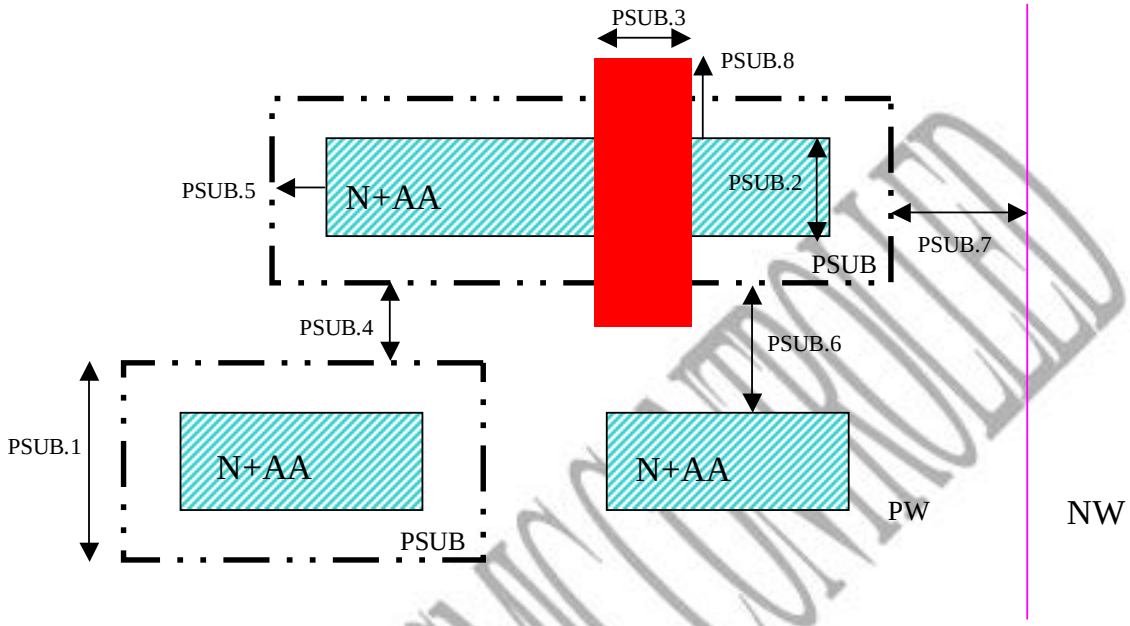


7.2.4 PSUB design rules for layer to define native NMOS

Rules number	Description	Operation	Design Value	Unit
PSUB.1	PSUB width	≥	0.36	um
PSUB.2	1.0/1.2/1.8/2.5/3.3V native NMOS channel width	≥	0.50	um
PSUB.3a	1.0/1.2V NMOS channel length	≥	0.20	um
PSUB.3b	1.8V NMOS channel length	≥	0.8	um
PSUB.3c	2.5V (or overdrive to 3.3V and underdrive to 1.8V) NMOS channel length	≥	1.0	um
PSUB.3d	3.3V NMOS channel length	≥	1.2	um
PSUB.4	Space between two PSUBs	≥	0.36	um
PSUB.5	Native NMOS AA enclosure by PSUB	=	0.26	um
PSUB.6	Space between PSUB and MOS AA	≥	0.37	um
PSUB.7	Space between PSUB and NW	≥	1.20	um
PSUB.8	Extension of native NMOS poly gate outside of AA	≥	0.31	um
PSUB.9[R]	PSUB inside, overlapping with, or crossing over a DNW area is not allowed			
PSUB.10[R]	PSUB must not overlap NW or PW .			
PSUB.11[R]	Only one AA pattern is allowed in one PSUB region, except for NMOS capacitors and AAs in INDMY.			
PSUB.12[R]	SP is not allowed to exist in a PSUB region			

Note:

It is recommended that PSUB is shaped conforming to AA edges. For example, in the case of dog-bone AA as shown in Fig. 1, PSUB should be drawn in a similar shape as also shown in Fig. 1 and avoid non-conforming PSUB shapes as shown in Fig.2. When the distance X between AA, as shown in Fig.2, is too short (so that PSUB.4 is violated), it is recommended to increase X so that PSUB shapes can conform to AA edges.



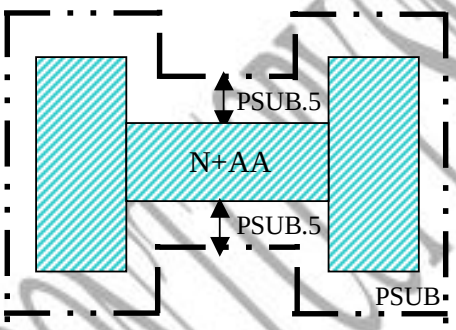


Fig. 1 Recommended

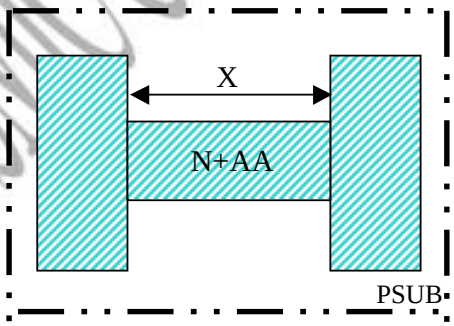
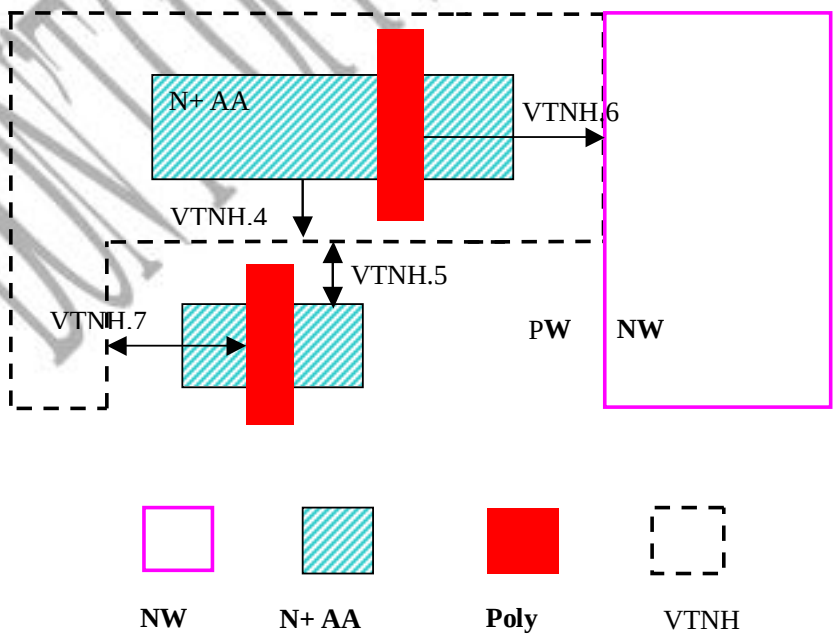


Fig. 2 Not Recommended

7.2.5 VTNH: High Vt NMOS design rules(optional)

VTNH is a drawn layer for Vt implant of high Vt MOS. VTNH is for 1.0/1.2V core high Vt device only.

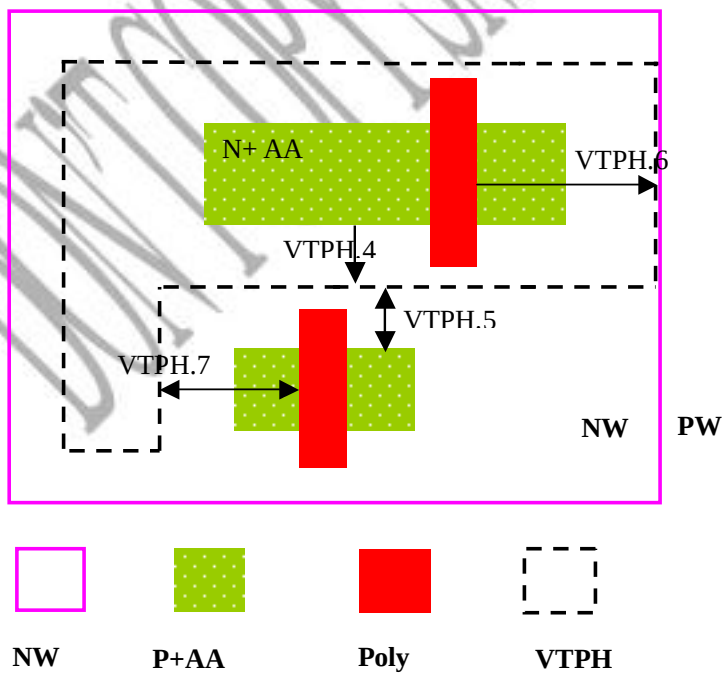
Rules number	Description	Operation	Design Value	Unit
VTNH.1	VTNH width	≥	0.18	um
VTNH.2	Space between two VTNHs	≥	0.18	um
VTNH.3	VTNH and PSUB overlap isn't allowed			
VTNH.4	VTNH extension outside of MOS AA along gate poly length direction.	≥	0.12	um
VTNH.5	Space between VTNH and MOS AA of other device along other device's gate poly length direction	≥	0.12	um
VTNH.6	VTNH extension outside of gate along source/drain direction	≥	0.185	um
VTNH.7	Space between VTNH and gate of other device along other device's source/drain direction	≥	0.185	um
VTNH.8	VTNH area	≥	0.18	um^2



7.2.6 VTPH: High Vt PMOS design rules (optional)

VTPH is a drawn layer for VT implant of high Vt PMOS. VTPH is for 1.0/1.2V core high Vt device only.

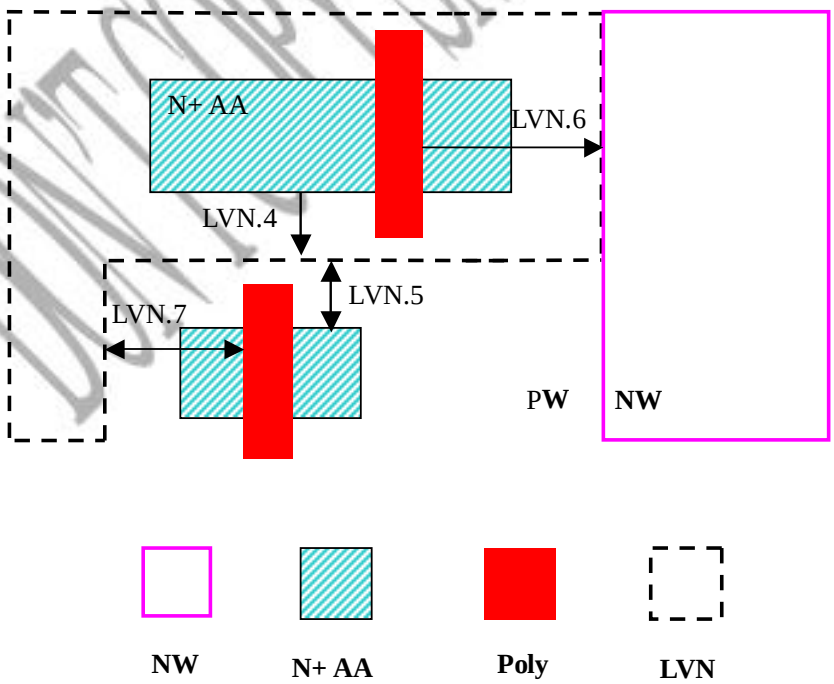
Rules number	Description	Operation	Design Value	Unit
VTPH.1	VTPH width	≥	0.18	um
VTPH.2	Space between two VTPHs	≥	0.18	um
VTPH.3	VTPH and PSUB overlap isn't allowed			
VTPH.4	VTPH extension outside of MOS AA along gate poly length direction.	≥	0.12	um
VTPH.5	Space between VTPH and MOS AA of other device along other device's gate poly length direction.	≥	0.12	um
VTPH.6	VTPH extension outside of gate along source/drain direction	≥	0.185	um
VTPH.7	Space between VTPH and gate of other device along other device's source/drain direction	≥	0.185	um
VTPH.8	VTPH area	≥	0.18	um^2



7.2.7 LVN : Low Vt NMOS design rules (optional)

LVN is a drawn LVN layer to define low Vt NMOS devices. LVN is to block 1.0/1.2V core low Vt device only.

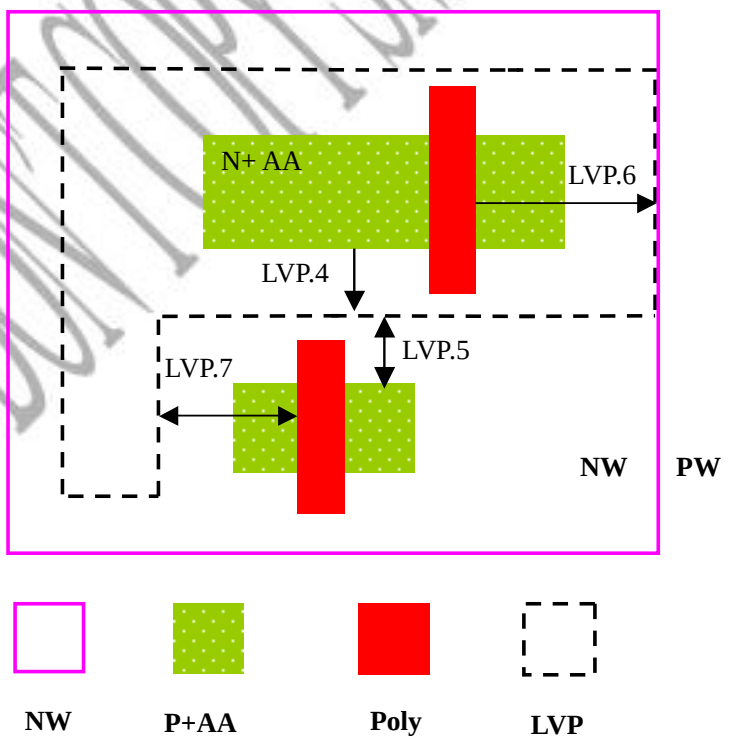
Rules number	Description	Operation	Design Value	Unit
LVN.1	LVN width	≥	0.18	um
LVN.2	Space between two LVNs	≥	0.18	um
LVN.3	LVN and PSUB overlap isn't allowed			
LVN.4	LVN extension outside of MOS AA along gate poly length direction.	≥	0.12	um
LVN.5	Space between LVN and MOS AA of other device along other device's gate poly length direction.	≥	0.12	um
LVN.6	LVN extension outside of gate along source/drain direction	≥	0.185	um
LVN.7	Space between LVN and gate of other device along other device's source/drain direction	≥	0.185	um
LVN.8	LVN area	≥	0.18	um^2



7.2.8 LVP : Low Vt PMOS design rules (optional)

LVP is a drawn layer to define low Vt PMOS devices. LVP is to block 1.0/1.2V core low Vt device only.

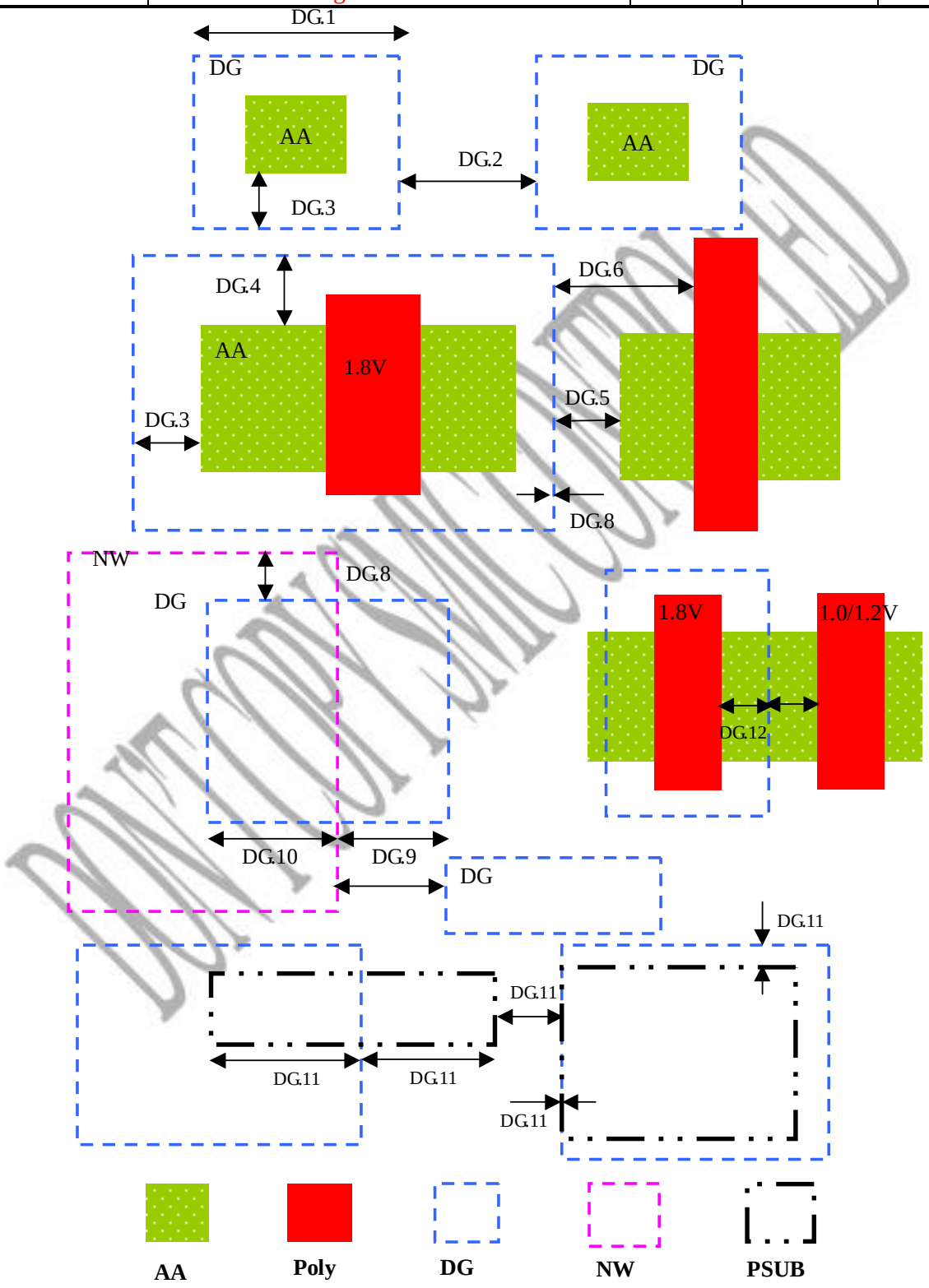
Rules number	Description	Operation	Design Value	Unit
LVP.1	LVP width	≥	0.18	um
LVP.2	Space between two LVPs	≥	0.18	um
LVP.3	LVP and PSUB overlap isn't allowed			
LVP.4	LVP extension outside of MOS AA along gate poly length direction.	≥	0.12	um
LVP.5	Space between LVP and MOS AA of other device along other device's gate poly length direction.	≥	0.12	um
LVP.6	LVP extension outside of gate along source/drain direction	≥	0.185	um
LVP.7	Space between LVP and gate of other device along other device's source/drain direction	≥	0.185	um
LVP.8	LVP area	≥	0.18	um^2



7.2.9 DG: Dual gate design rules to define 1.8V transistor region

Rules number	Description	Operation	Design Value	Unit
DG.1	DG width	≥	0.46	um
DG.2	Space between two DGs, merge if the space is less than 0.46um	≥	0.46	um
DG.3	Enclosure of AA by DG(Except pick-up AA)	≥	0.25	um
DG.4	Enclosure of MOS AA by DG along gate poly direction	≥	0.27	um
DG.5	Space between DG and MOS AA	≥	0.25	um
DG.6	Space between DG and 1.2/2.5/3.3 gate along source/drain direction.	≥	0.24	um
DG.7[NC]	Overlap between DG and other voltage MOS AA is allowed			
DG.8	Enclosure of NW beyond DG, set the value to 0 if the enclosure is less than 0.46um	≥	0.46	um
DG.9	Space or extension of DG to NW, set the value to 0 if it is smaller than 0.46um	≥	0.46	um
DG.10	Overlap of DG and NW, set the value to 0 if it is smaller than 0.46um	≥	0.46	um
DG.11	Enclosure of DG beyond PSUB, space or extension of PSUB to DG, overlap of PSUB and DG, set the value to 0 if it is smaller than 0.32um	≥	0.32	um
DG.12	Enclosure of gate by DG, along source/drain direction	≥	0.33	um
DG.13	Space between DG and 1.0/1.2V gate along source/drain direction	≥	0.33	um

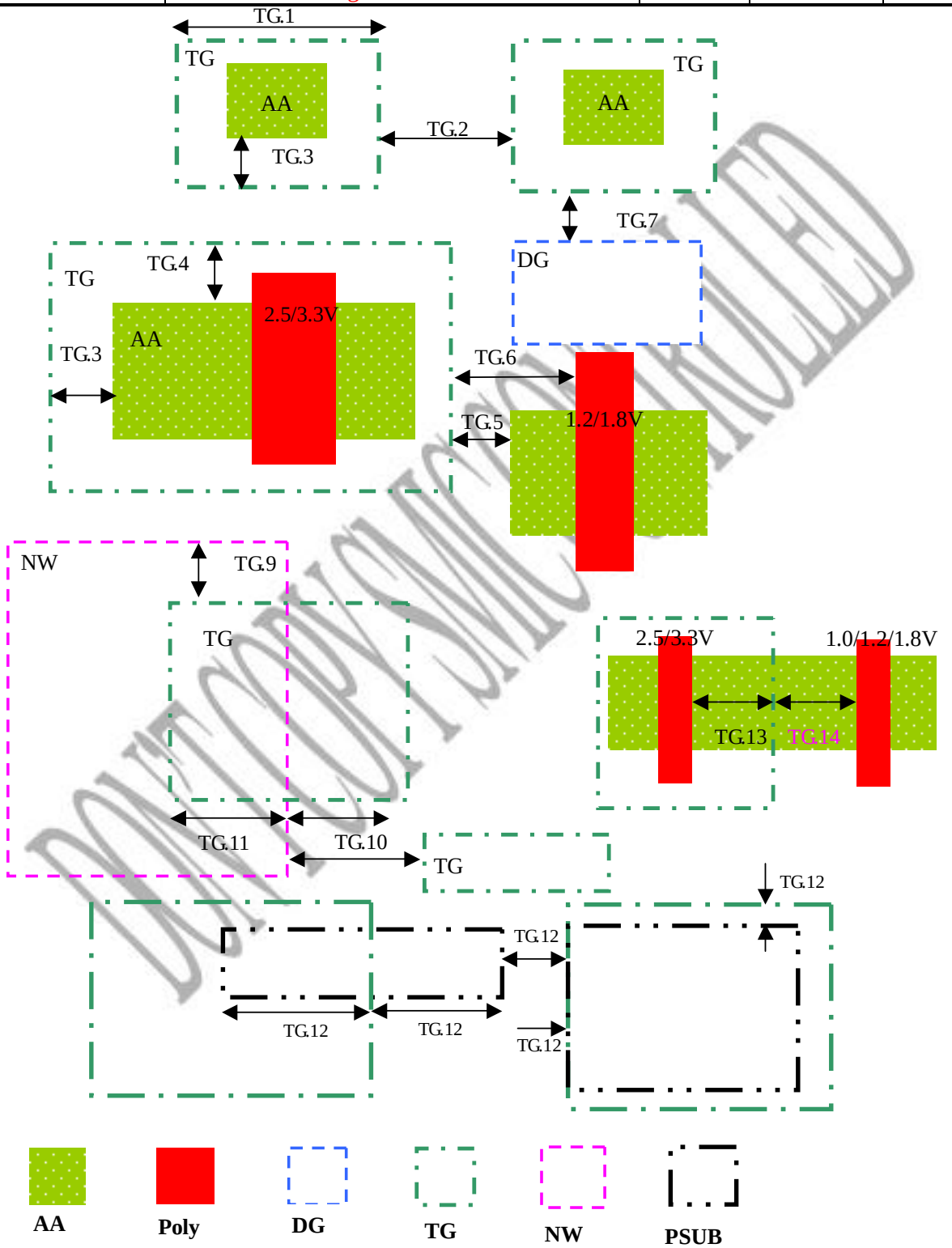
Note: NWH is generated by NW * DG.



7.2.10 TG: Triple gate design rules to define 2.5/3.3V transistor for AA

Rules number	Description	Operation	Design Value	Unit
TG.1	TG width	≥	0.46	um
TG.2	Space between two TGs, merge if the space is less than 0.46um	≥	0.46	um
TG.3	Enclosure of AA by TG(except pickup AA)	≥	0.25	um
TG.4	Enclosure of MOS AA by TG along gate poly direction	≥	0.27	um
TG.5	Space between TG and MOS AA	≥	0.25	um
TG.6	Space between TG and 1.2/1.8V gate along source/drain direction.	≥	0.24	um
TG.7	Space between TG and DG	≥	0.46	um
TG.8[NC]	Overlap between TG and other voltage MOS AA is allowed			
TG.9	Enclosure of NW beyond TG, set the value to 0 if the enclosure is less than 0.46um	≥	0.46	um
TG.10	Space or extension of TG to NW, set the value to 0 if it is smaller than 0.46um	≥	0.46	um
TG.11	Overlap of TG and NW, set the value to 0 if it is smaller than 0.46um	≥	0.46	um
TG.12	Enclosure of TG beyond PUB, space or extension of PSUB to TG, overlap of PSUB and TG, set the value to 0 if it is smaller than 0.32um	≥	0.32	um
TG.13	Enclosure of gate by TG, along source/drain direction	≥	0.33	um
TG.14	Space between TG and 1.0/1.2/1.8V gate along source/drain direction	≥	0.33	um

Note: NWHT is generated by NW * TG



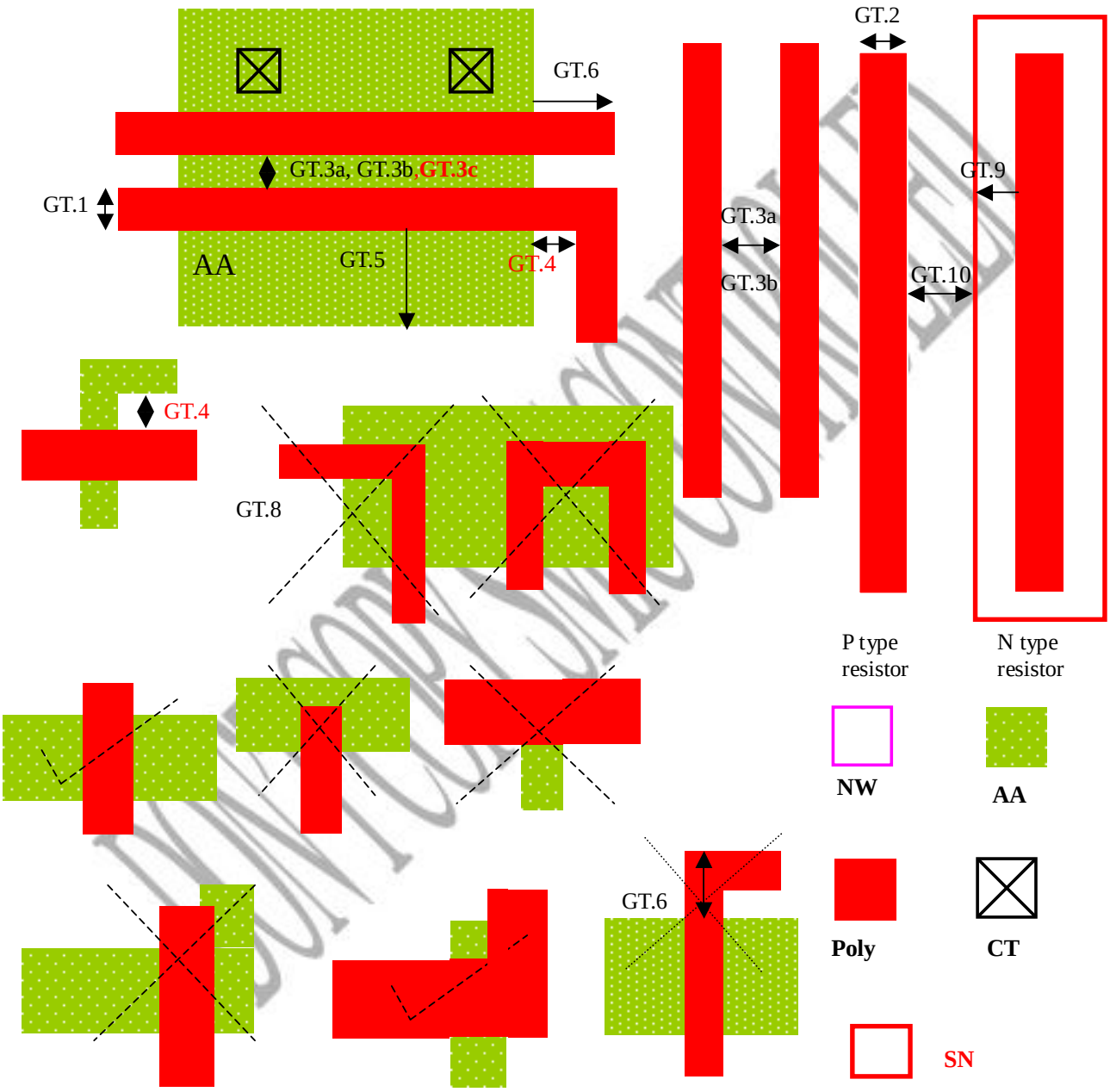
7.2.11 GT: Poly design rules

Rules number	Description	Operation	Design Value	Unit
GT.1a	Channel length for 1.0/1.2V NMOS /PMOS transistors	≥	0.06	um
GT.1b	Channel length for 1.8V NMOS/PMOS transistors	≥	0.20	um
GT.1c	Channel length for 2.5V NMOS/PMOS transistors	≥	0.28	um
GT.1d	Channel length for 3.3V NMOS/PMOS transistors	≥	0.38	um
GT.1e	Channel length for 2.5V NMOS/PMOS transistors (over drive to 3.3V and 4.1V)	≥	0.50(NMOS)	um
		≥	0.40(PMOS)	um
GT.1f	Channel length for 2.5V NMOS/PMOS transistors (under drive to 1.8V)	≥	0.22	um
GT.2	Width of interconnect poly	≥	0.06	um
GT.3a	Space between two GTs	≥	0.12	um
GT.3b	Space between two GTs when one or both GT width is >= 0.4um,and the run length of two GTs is >=0.5um.	≥	0.16	um
GT.3c[R]	Recommended space between GTs on the same AA	≥	0.19	um
GT.3d[R]	Recommended space between GTs on the same AA inside TG	≥	0.24	um
GT.4	Space between AA and GT on field oxide	≥	0.05	um
GT.5	Extension of AA outside of GT(not include dummy AA and dummy Poly)	≥	0.115	um
GT.6	Extension of gate poly end-cap outside of AA (not including dummy AA and dummy poly)	≥	0.14	um
GT.7a	Local GT density (including dummy) in 200um*200um window with step size: 100um	≥	7%	
		≤	70%	
GT.7b[R]	Global GT density for fully chip (including dummy)	≥	10%	
		≤	45%	
GT.7c[R]	GT density inside of dummy block area, while the area of	≥	10%	

	dummy block layer is larger than 2500um^2 (50X50um).			
GT.8	No bent GT on AA are allowed. All GT patterns on AA have to be orthogonal to AA edge.			
GT.9	SN and SP extension outside of poly resistor. Poly resistor enclosed by SN/SP	≥	0.16	um
GT. 10	Space between NLL, NLH, SN and P type poly resistor; Space between PLL,PLH, SP to N type poly resistor	≥	0.16	um
GT. 11	GT is enclosed by SN and/or SP, except MOM and HRPDMY area (when checking the rule, size down the HRPDMY by 0.3um along the current direction).			
GT. 12	SN and SP overlap on GT is not allowed			
GT.13	GT area	≥	0.038	um^2

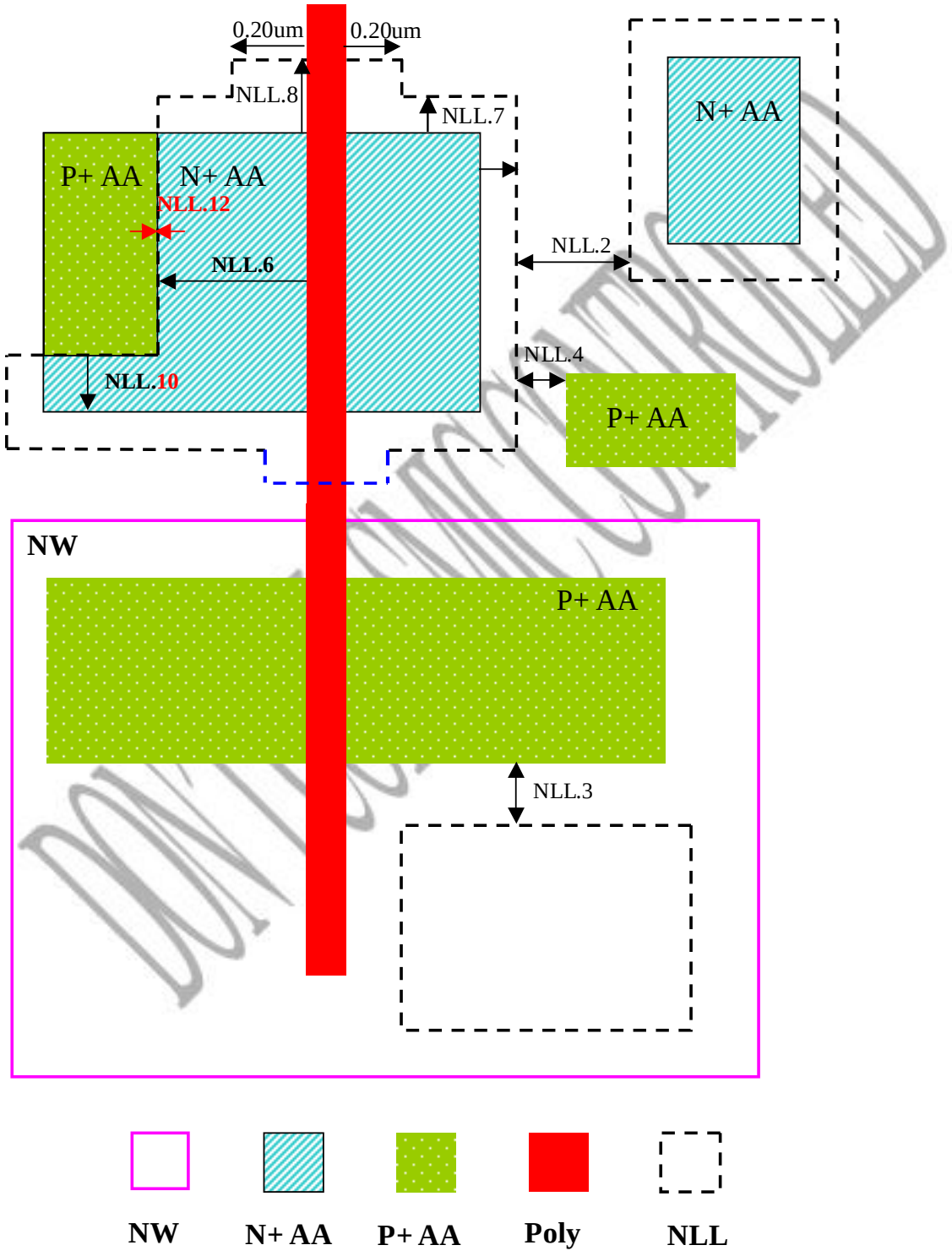
Note:

1. Please use 125;4 layer to block over drive poly from 2.5V to 3.3V and 4.1V, and use 125;5 layer to block under drive poly from 2.5V to 1.8V, and layer 125:4 and layer 125;5 must be drawn within layer 125:0.



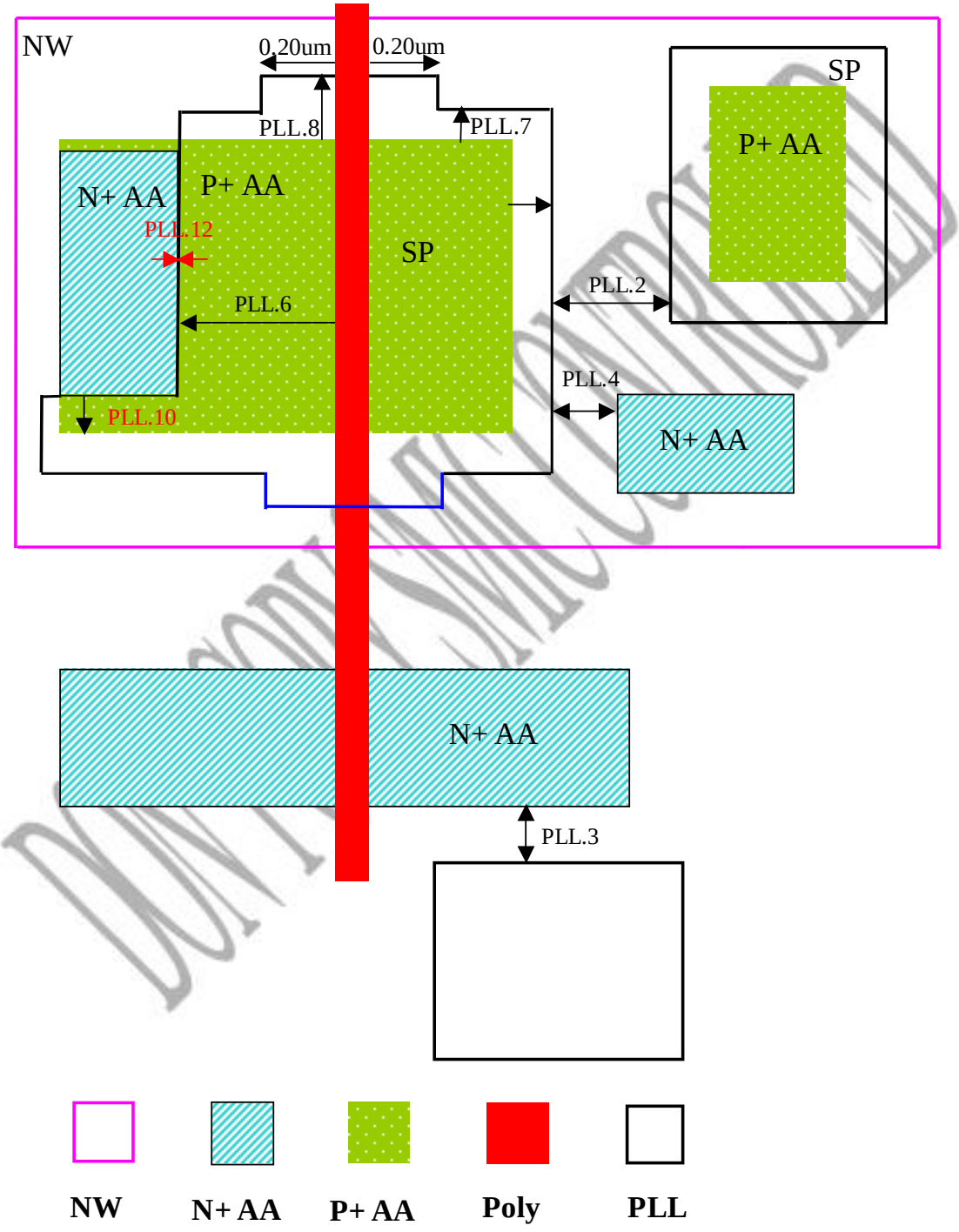
7.2.12 NLL: 1.0/1.2V NLDD implantation design rules

Rules number	Description	Operation	Design Value	Unit
NLL.1	NLL width	≥	0.18	um
NLL.2	Space between two NLLs.	≥	0.18	um
NLL.3	Space between NLL and P+ AA inside N well	≥	0.10	um
NLL.4	Space between NLL and P+ AA inside P well	≥	0.02	um
NLL.5	(Purposely blank)			
NLL.6	NLL extension outside of NMOS gate along source/drain direction.	≥	0.24	um
NLL.7	NLL extension outside of NMOS AA along gate poly length direction, if distance to the related poly is larger than 0.20um	≥	0.12	um
NLL.8	NLL extension outside of NMOS AA along gate poly length direction, if distance to the related poly is less than or equal to 0.20um	≥	0.16	um
NLL.9	(Purposely blank)			
NLL.10	Overlap of NLL and AA	≥	0.09	um
NLL.11	NLL area	≥	0.10	um^2
NLL.12	Space between NLL and butted P+AA (except SRAM area).	≥	0.00	um



7.2.13 PLL: 1.0/1.2V PLDD implantation design rules

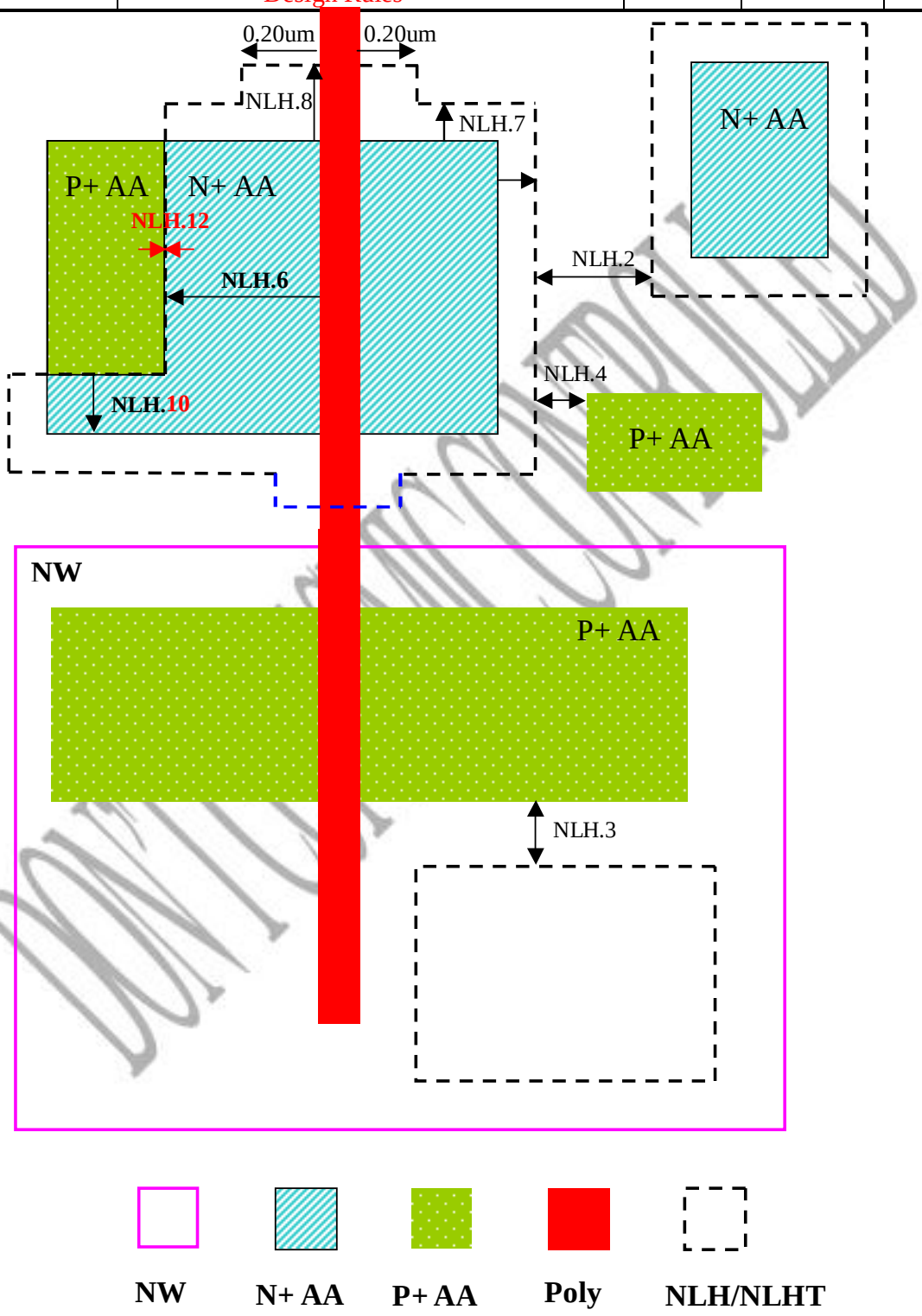
Rules number	Description	Operation	Design Value	Unit
PLL.1	PLL width	≥	0.18	um
PLL.2	Space between two PLLs	≥	0.18	um
PLL.3	Space between PLL and N+ AA inside P well	≥	0.10	um
PLL.4	Space between PLL and N+ AA inside N well	≥	0.02	um
PLL.5	(Purposely blank)			
PLL.6	PLL extension outside of PMOS gate along source/drain direction.	≥	0.24	um
PLL.7	PLL extension outside of PMOS AA along gate poly length direction, if distance to the related poly is larger than 0.20um	≥	0.12	um
PLL.8	PLL extension outside of PMOS AA along gate poly length direction, if distance to the related poly is less than or equal to 0.20um	≥	0.16	um
PLL.9	(Purposely blank)			
PLL.10	Overlap of PLL and AA	≥	0.09	um
PLL.11	PLL area	≥	0.10	um^2
PLL.12	Space between PLL and butted N+AA (except SRAM area).	≥	0.00	um



7.2.14 NLH-NLHT: 1.8V-2.5/3.3V NLDD implantation design rules

In dual gate process use NLH only. In triple gate process both NLH and NLHT are used.

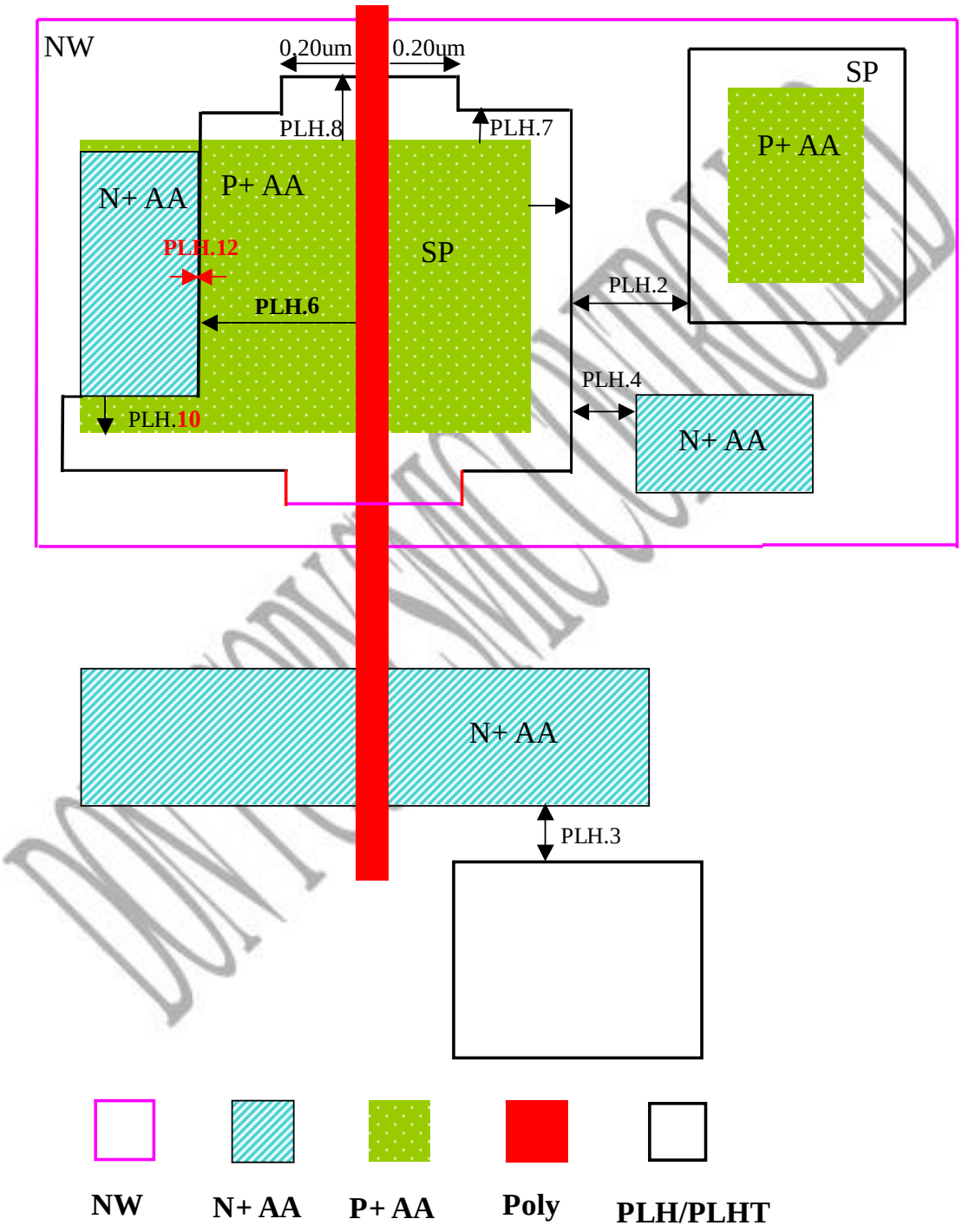
Rules number	Description	Operation	Design Value	Unit
NLH.1	NLH/NLHT width	≥	0.18	um
NLH.2	Space between two NLH/NLHTs.	≥	0.18	um
NLH.3	Space between NLH/NLHT and P+ AA inside NW	≥	0.10	um
NLH.4	Space between NLH/NLHT and P+ AA inside PW	≥	0.02	um
NLH.5	(Purposely blank)			
NLH.6	NLH/NLHT extension outside of NMOS gate along source/drain direction.	≥	0.24	um
NLH.7	NLH/NLHT extension outside of NMOS AA along gate poly length direction, if distance to the related poly is larger than 0.20um	≥	0.12	um
NLH.8	NLH/NLHT extension outside of NMOS AA along gate poly length direction, if distance to the related poly is less than or equal to 0.20um	≥	0.16	um
NLH.9	(Purposely blank)			
NLH.10	Overlap of NLH/NLHT and AA	≥	0.09	um
NLH.11	NLH/NLHT area	≥	0.10	um^2
NLH.12	Space between NLH/NLHT and butted P+AA(except SRAM area).	≥	0.00	um



7.2.15 PLH-PLHT: 1.8V-2.5/3.3V PLDD implantation design rules

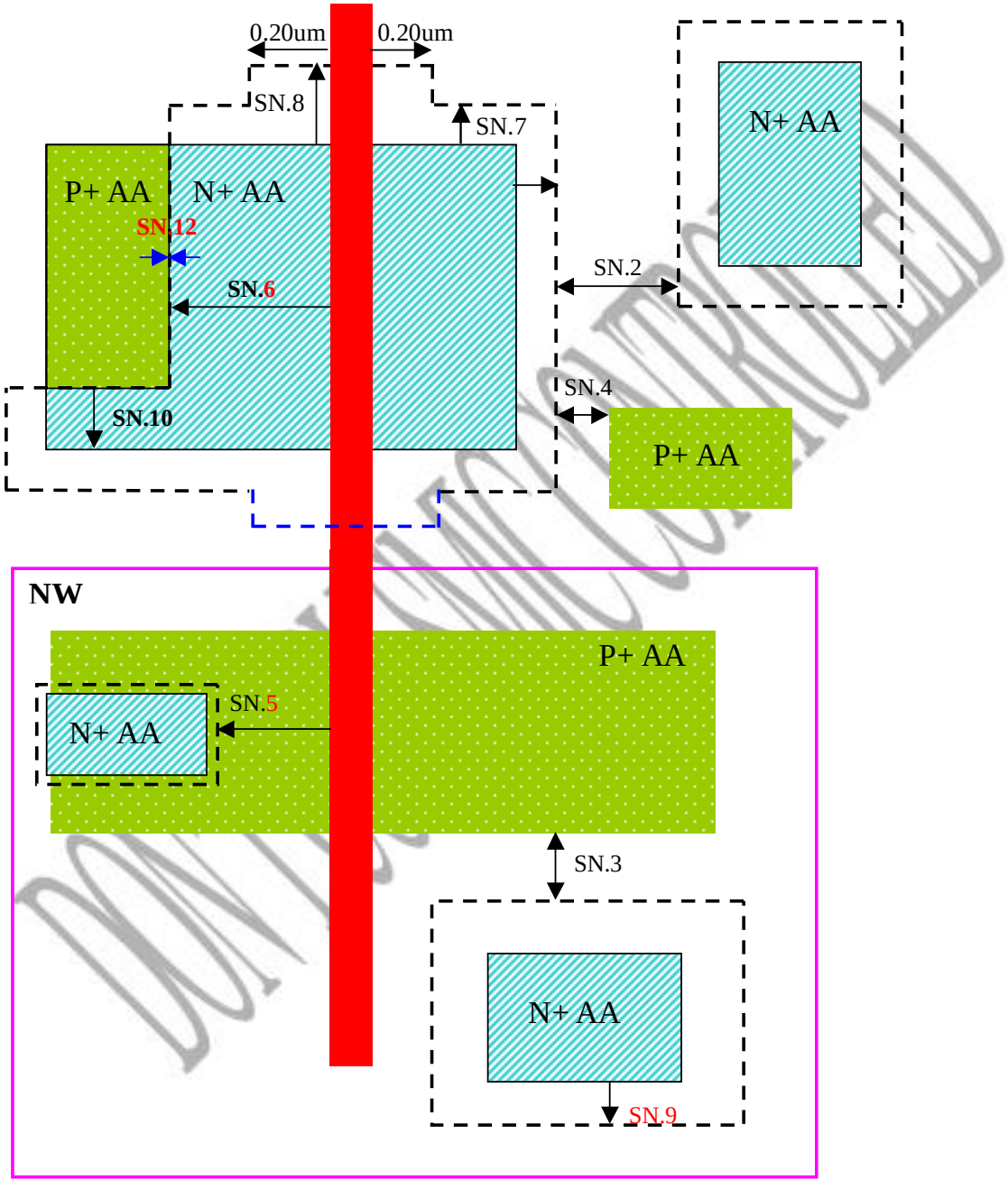
In dual gate process use PLH only. In triple gate process both PLH and PLHT are used)

Rules number	Description	Operation	Design Value	Unit
PLH.1	PLH/PLHT width	≥	0.18	um
PLH.2	Space between two PLH/PLHT s	≥	0.18	um
PLH.3	Space between PLH/PLHT and N+ AA inside P well	≥	0.10	um
PLH.4	Space between PLH/PLHT and N+ AA inside N well	≥	0.02	um
PLH.5	(Purposely blank)			
PLH.6	PLH/PLHT extension outside of PMOS gate along source/drain direction.	≥	0.24	um
PLH.7	PLH/PLHT extension outside of PMOS AA along gate poly length direction, if distance to the related poly is larger than 0.20um	≥	0.12	um
PLH.8	PLH/PLHT extension outside of PMOS AA along gate poly length direction, if distance to the related poly is less than or equal to 0.20um	≥	0.16	um
PLH.9	(Purposely blank)			
PLH.10	Overlap of PLH/PLHT and AA	≥	0.09	um
PLH.11	PLH/PLHT area	≥	0.10	um^2
PLH.12	Space between PLH/PLHT and butted N+AA (except SRAM area).	≥	0.00	um



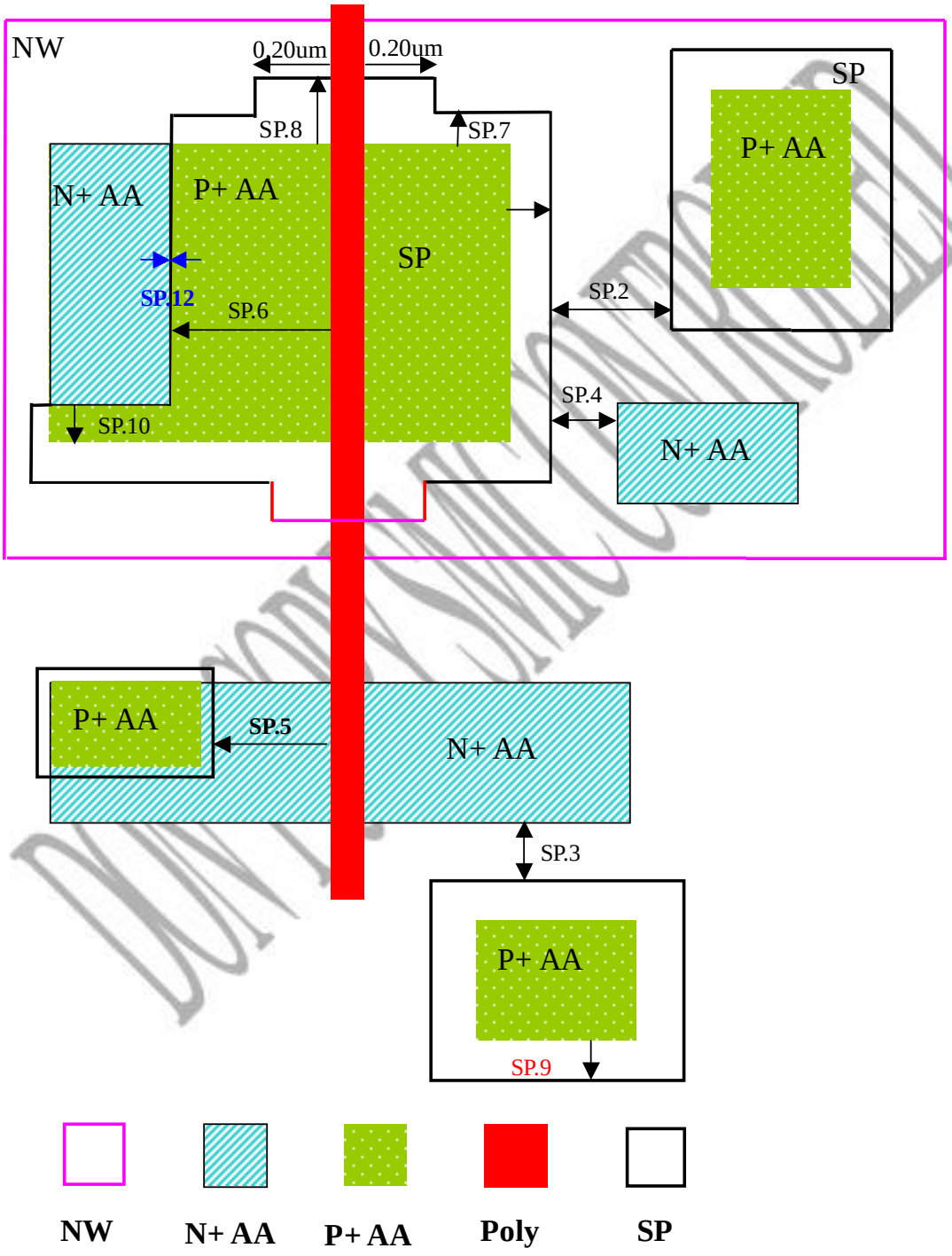
7.2.16 SN: N+ S/D implantation design rules

Rules number	Description	Operation	Design Value	Unit
SN.1	SN width	≥	0.18	um
SN.2	Space between two SNs.	≥	0.18	um
SN.3	Space between SN and P+ AA inside NW	≥	0.10	um
SN.4	Space between SN and P+ pick-up AA inside PW	≥	0.02	um
SN.5	Space between SN and PMOS gate along source/drain direction.	≥	0.24	um
SN.6	SN extension outside of NMOS gate along source/drain direction..	≥	0.24	um
SN.7	SN extension outside of NMOS AA along gate poly length direction, if the distance to the related poly is larger than 0.20um	≥	0.12	um
SN.8	SN extension outside of NMOS AA along gate poly length direction, if the distance to the related poly is less than or equal to 0.20um	≥	0.16	um
SN.9	N+AA enclosured by by SN in NW.	≥	0.02	um
SN.10	Overlap of SN and AA	≥	0.09	um
SN.11	SN area	≥	0.10	um^2
SN.12	Space between SN and butted P+AA (except SRAM area).	≥	0.00	um



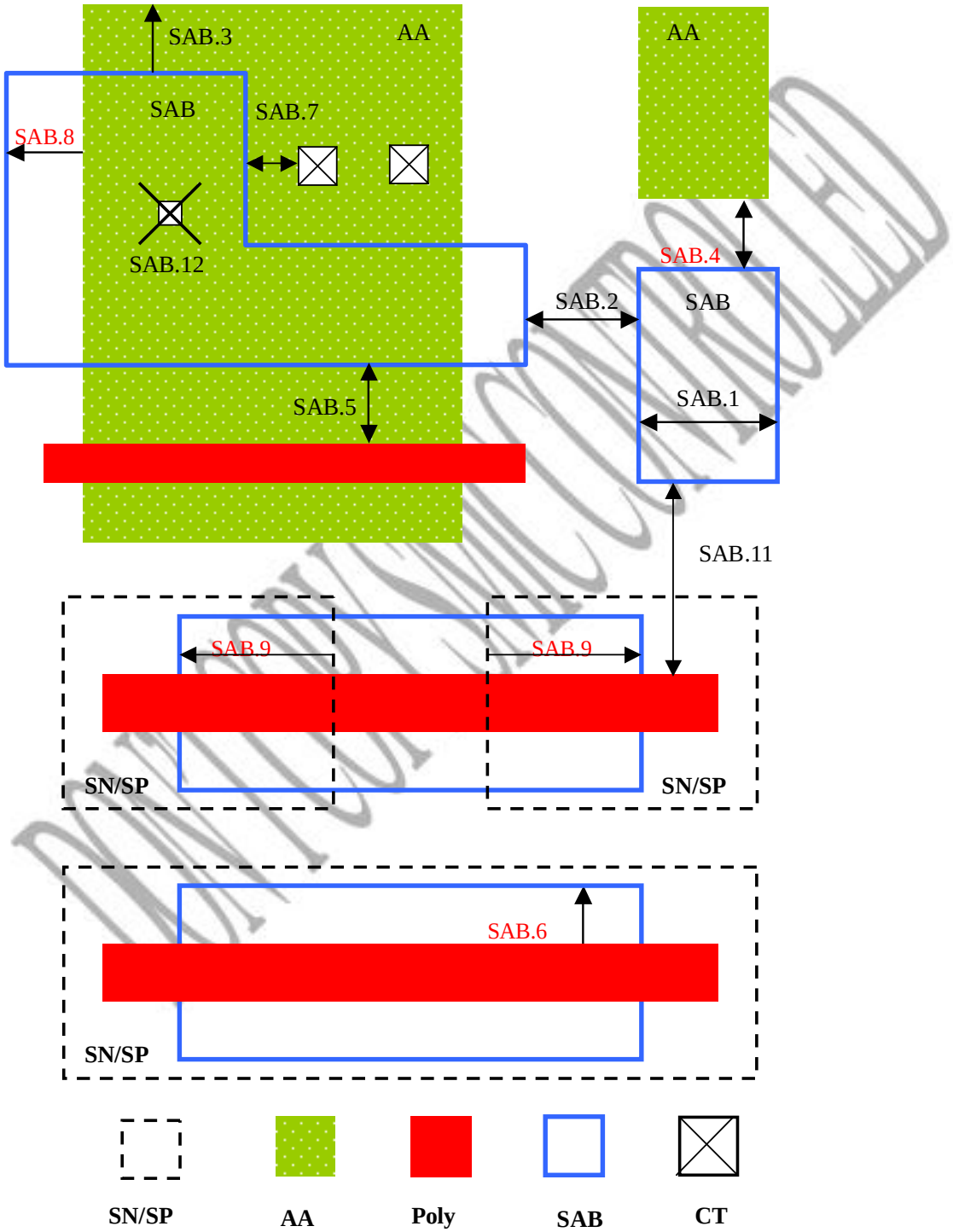
7.2.17 SP+ S/D implantation design rules

Rules number	Description	Operation	Design Value	Unit
SP.1	SP width	≥	0.18	um
SP.2	Space between two SPs.	≥	0.18	um
SP.3	Space between SP and N+ AA inside P well	≥	0.10	um
SP.4	Space between SP and N+ AA inside N well	≥	0.02	um
SP.5	Space between SP and NMOS gate along source/drain direction.	≥	0.24	um
SP.6	SP extension outside of PMOS gate along source/drain direction.	≥	0.24	um
SP.7	SP extension outside of PMOS AA along gate poly length direction, if the distance to the related poly is larger than 0.20um	≥	0.12	um
SP.8	SP extension outside of PMOS AA along gate poly length direction, if the distance to the related poly is less than or equal to 0.20um	≥	0.16	um
SP.9	P+ AA enclosure by SP in PW	≥	0.02	um
SP.10	Overlap of SP and AA	≥	0.09	um
SP.11	SP area	≥	0.10	um^2
SP.12	Space between SP and butted N+AA (except SRAM area).	≥	0.00	um
SP.13	No SP and SN overlap is allowed			
SP.14[NC]	SP can not be generated by the reverse tone of SN.			



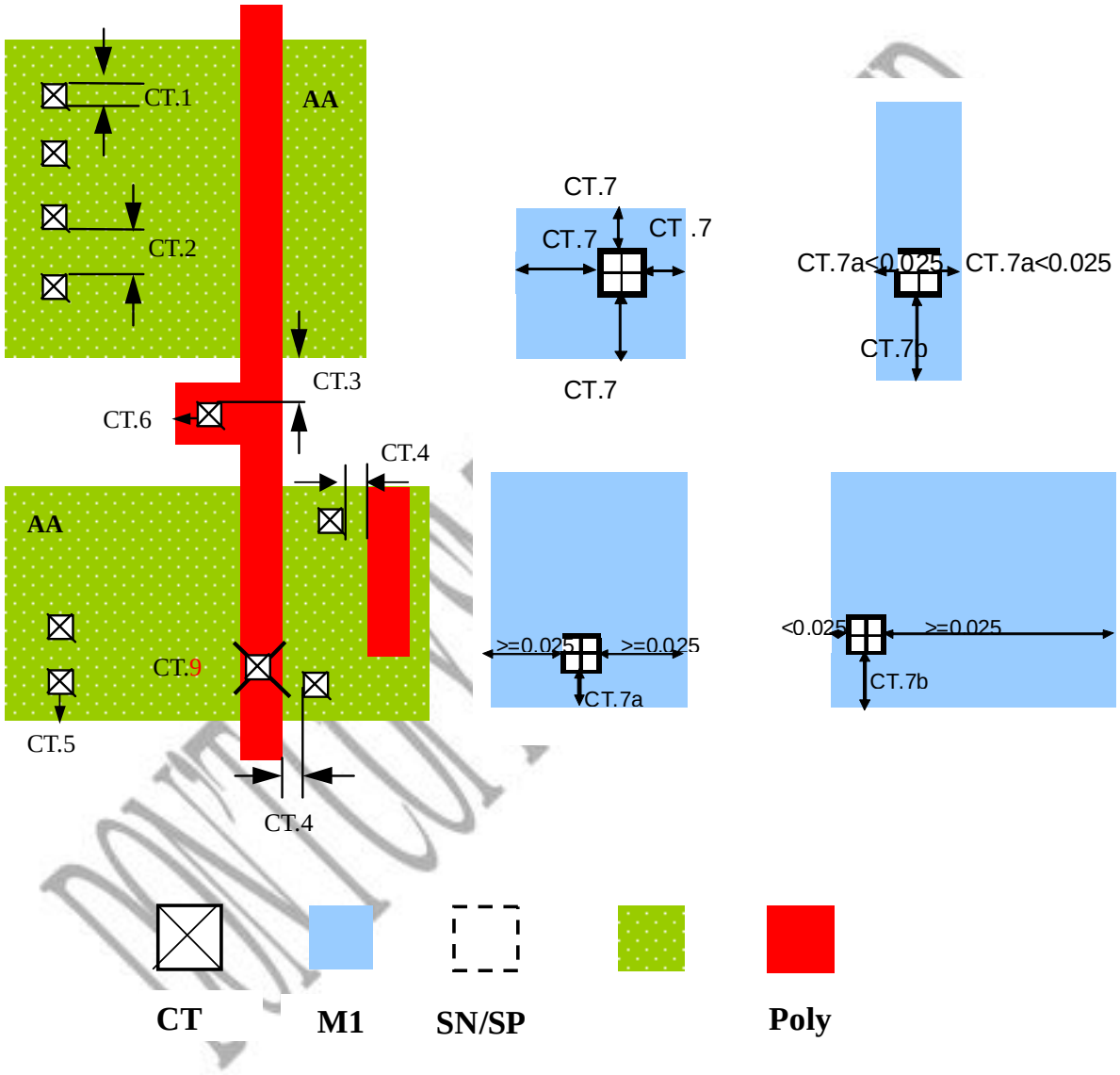
7.2.18 SAB: Salicide block design rules

Rules number	Description	Operation	Design Value	Unit
SAB.1	SAB width	≥	0.40	um
SAB.2	Space between two SABs	≥	0.40	um
SAB.3	Extension of AA outside of SAB	≥	0.20	um
SAB.4	Space between SAB and AA	≥	0.20	um
SAB.5	Space between SAB and GT ,while the GT is on AA	≥	0.36	um
SAB.6	Extension of SAB outside of poly on field oxide	≥	0.20	um
SAB.7	Space between SAB and CT	≥	0.20	um
SAB.8	Extension of SAB outside of AA	≥	0.20	um
SAB.9	SAB overlap with SN or SP	≥	0.20	um
SAB.10	SAB area	≥	0.50	um^2
SAB.11	Space between SAB and poly on field oxide.	≥	0.28	um



7.2.19 CT: Contact design rules

Rule number	Description	Operation	Design Value	Unit
CT.1	Fixed contact size (square shape except rectangular CT in SRAM and EFUSE area)	=	0.09	um
CT.2a	Space between two contacts	≥	0.11	um
CT.2b	Space between two contacts in case contact array is larger or equal to 4x4. Two contact regions whose space is <=0.15um are considered to be in the same array.	≥	0.13	um
CT.3	Space between AA and contact on poly	≥	0.065	um
CT.4a	Space between poly and contact on AA for 1.0V/1.2V	≥	0.05	um
CT.4b	Space between poly and contact on AA for 1.8/2.5/3.3V	≥	0.09	um
CT.5	CT enclosure by AA for CT landed on AA	≥	0.015	um
CT.6	CT enclosure by poly for CT landed on poly	≥	0.01	um
CT.7a	M1 enclosure of CT	≥	0.00	um
CT.7b	M1 enclosure of CT when M1 enclosure on one or both perpendicular directions < 0.025um	≥	0.025	um
CT.7c[NC]	M1 enclosure of CT should be as large as layout allowed			
CT.8	(Purposely blank)			
CT.9	CT is not allowed to land on gate			
CT.10	CT should land on salicided surface (except MARKG/MARKS covered areas)			

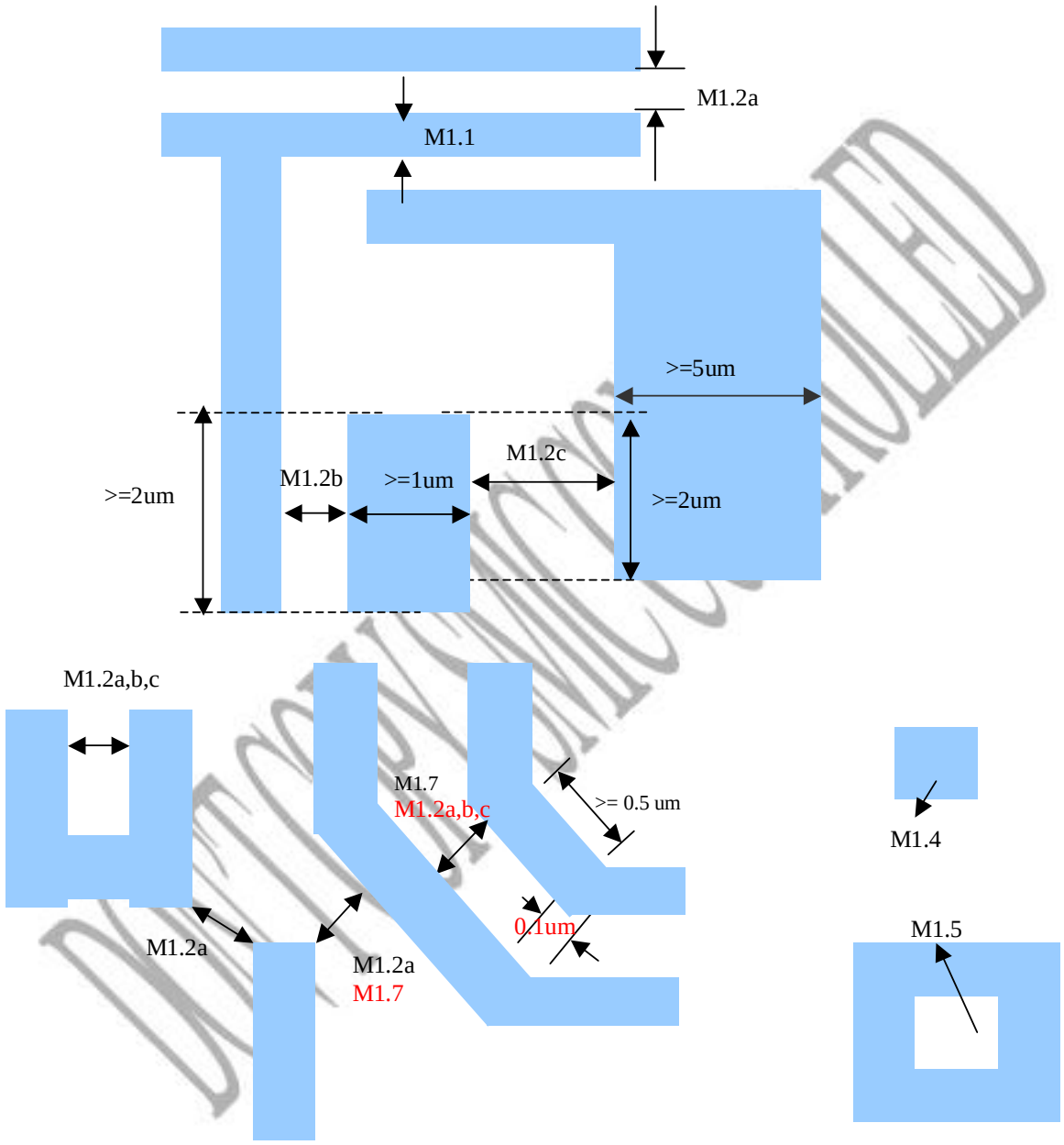


7.2.20 Metal 1 design rules

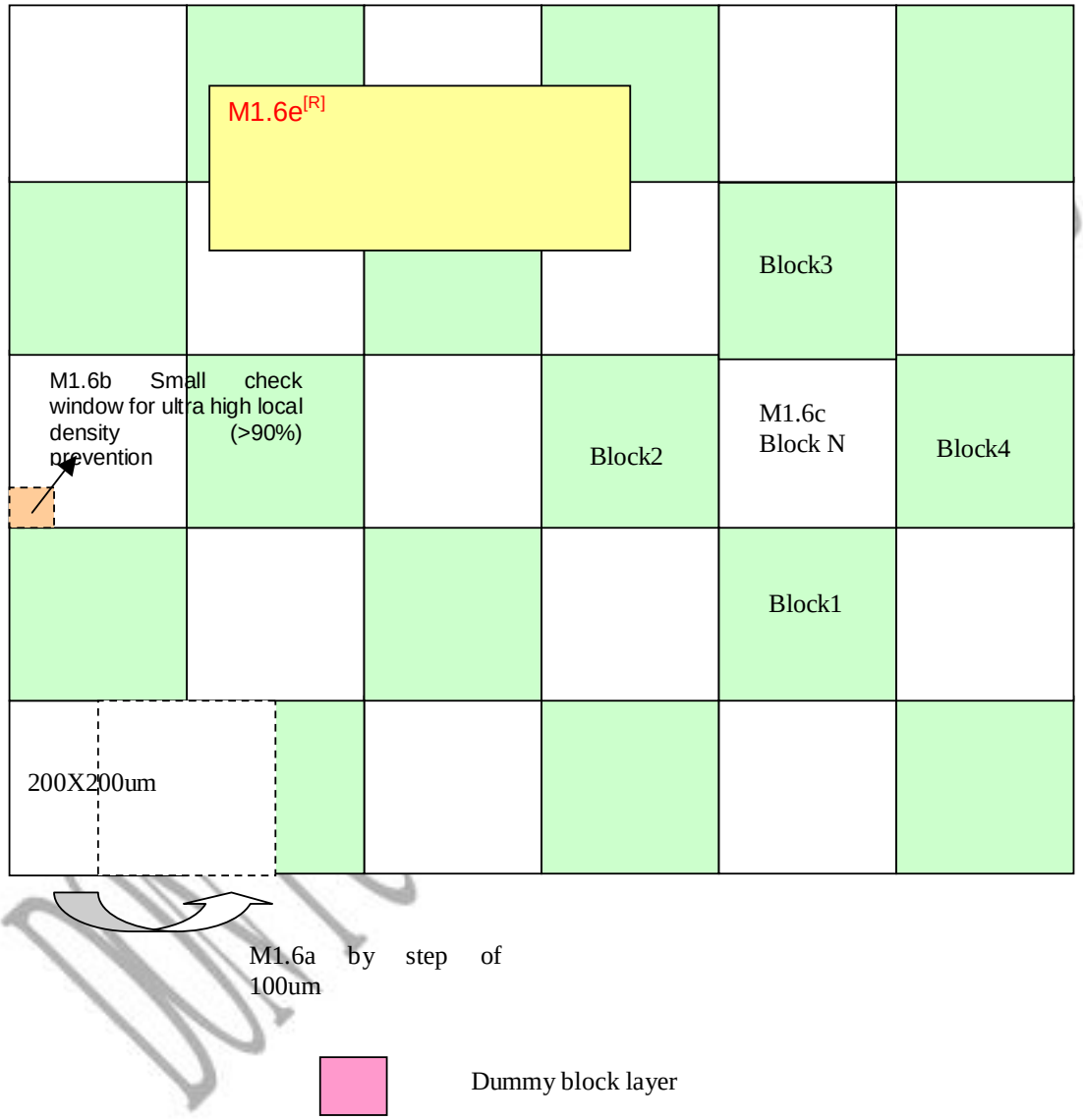
Rule number	Description	Operation	Design Value	Unit
M1.1	M1 width	≥	0.09	um
M1.2a	Space between two M1s	≥	0.09	um
M1.2b	Space between two M1s when one or both M1 width or length ≥1um, and the run length of two M1s is ≥2um	≥	0.16	um
M1.2c	Space between two M1s when one or both M1 width or length ≥5um, and run length of two M1s is ≥2um	≥	0.50	um
M1.3	M1 width	≤	12.00	um
M1.4	M1 area	≥	0.027	um^2
M1.5	Enclosed dielectric area by M1	≥	0.13	um^2
M1.6a	M1 density (including dummy) in 200umX200um window with step size 100um. INDMY/MARKF/MARKG/MARKS covered areas are excluded for this rule checking	≥	18%	
		≤	80%	
M1.6b	M1 density (including dummy) in 50umX50um window with step size 25um.	≤	90%	
M1.6c	The difference between M1 density in 200umX200um with step size 200um and those of the adjacent checking windows (including dummy). INDMY/MARKG/MARKF/MARKS covered areas are excluded for this rule checking	≤	40%	
M1.6d	M1 density (including dummy) in 25umX25um window with step size 12.5um. INDMY/MARKG/MARKS covered areas are excluded for this rule checking	≥	12%	
M1.6e[R]	M1 average density inside the dummy block area in 25umX25um window with step size 12.5um when the dummy block area ≥ 25umX25um. INDMY/MARKF/MARKG/MARKS covered areas are excluded for this rule checking. Device sensitive areas can be waived.	≥	12%	
		≤	90%	

M1.7	Space between metal lines with one or both are 45 degree, and the bending metal length>=0.5um (the area with 0.1um distance from bending point need not follow this rule)	≥	0.105	um
M1.8[NC]	If designer needs to design metals wider than M1.3, please comply with metal slot rules in section 7.2.34.13.			
M1.9[NC]	Dummy insertion rules refer to section 7.2.32.5			
M1.10[R] [NC]	Recommend that the length of M1 lines is orthogonal to the length of metal lines on neighboring layers.			

Note: M1.2b, M1.2c width or length checked by DRC is perpendicular to run length.

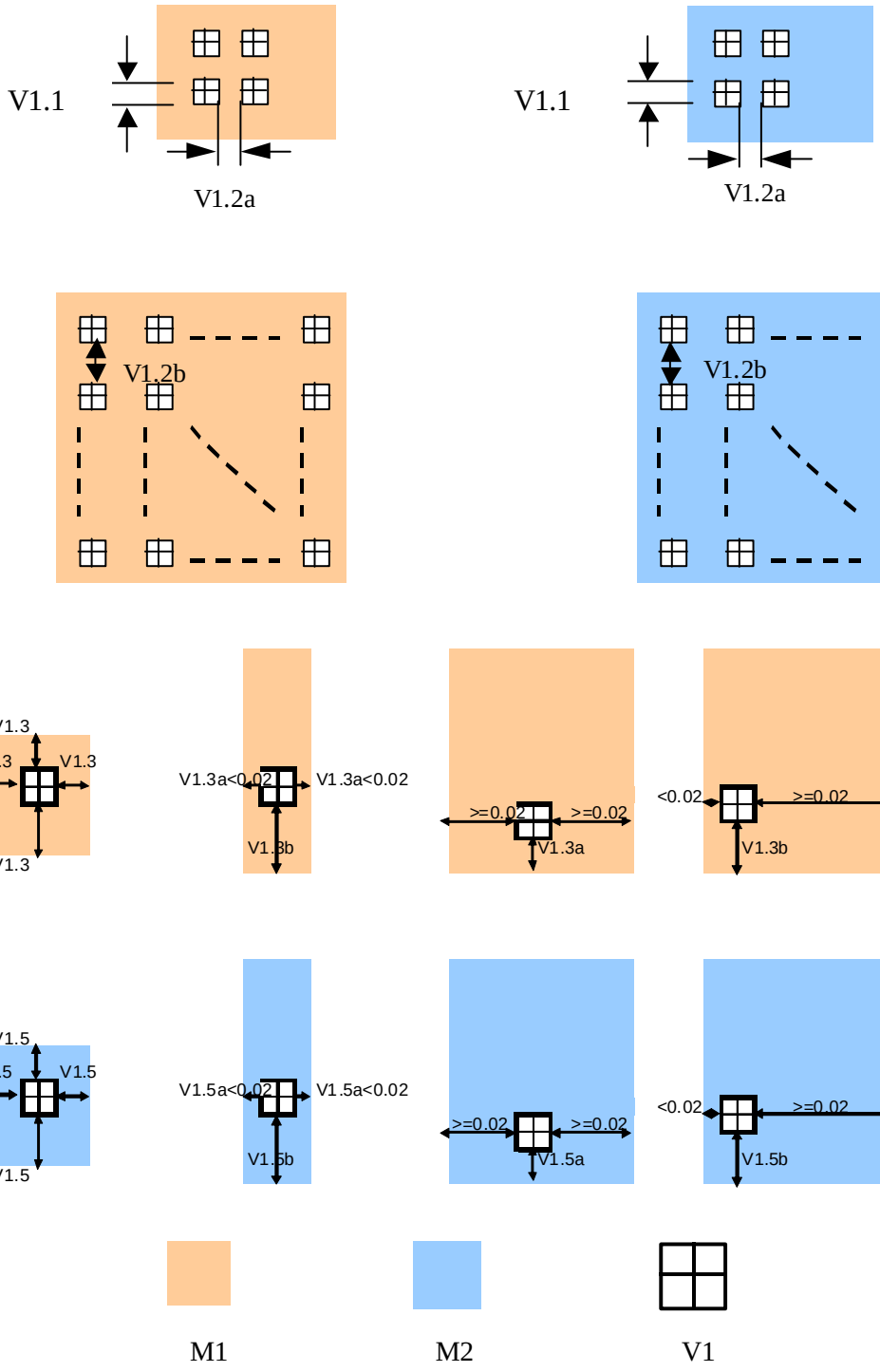


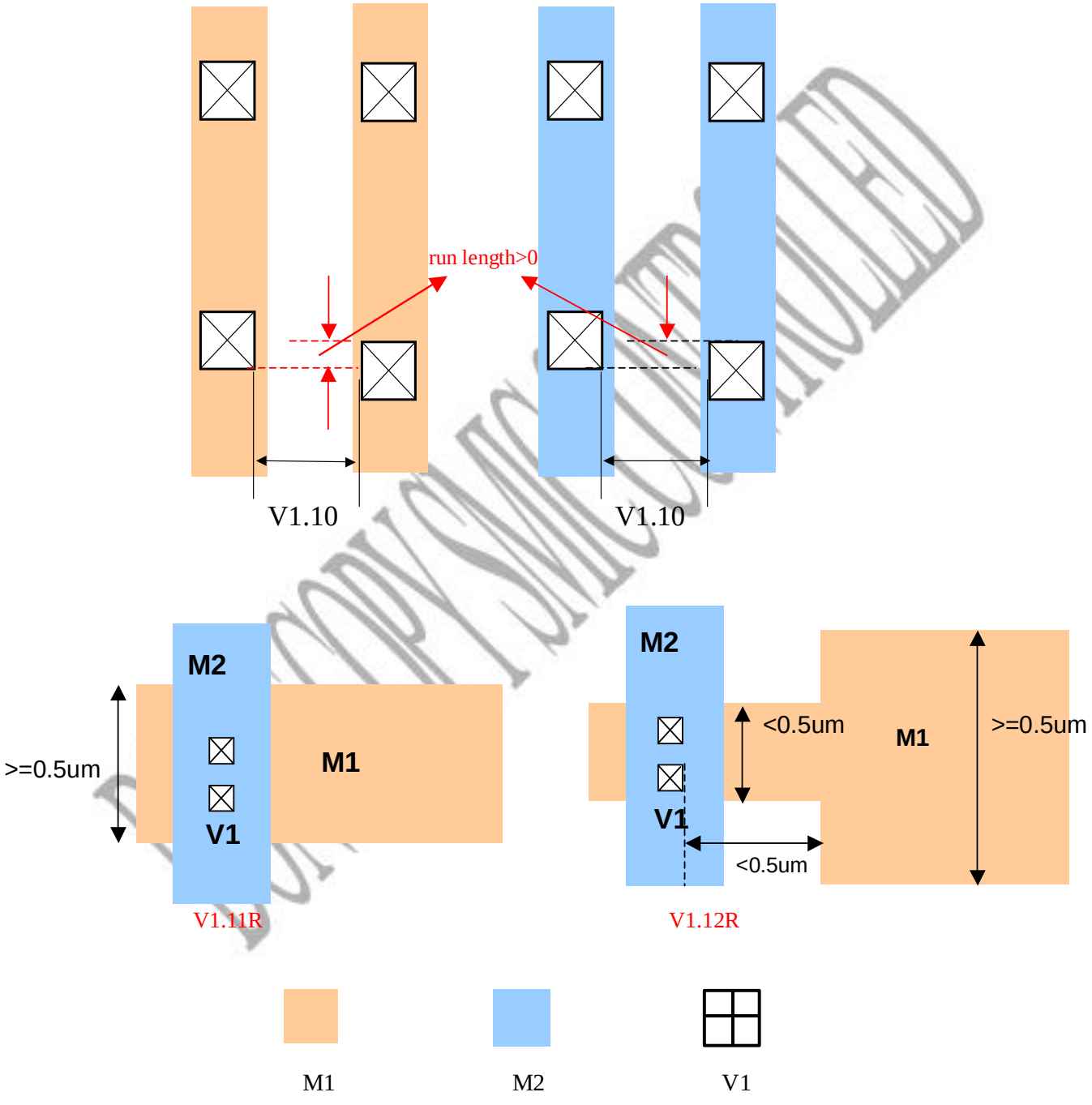
Whole chip view



7.2.21 Via1 design rules

Rule number	Description	Operation	Design Value	Unit
V1.1	Fixed V1 size (square shape)	=	0.09	um
V1.2a	Space between two V1s	≥	0.11	um
V1.2b	Space between V1s, when array equal to or greater than 4x4. Two vias whose space is within 0.15um are considered to be in the same array.	≥	0.13	um
V1.3a	M1 enclosure of V1	≥	0.00	um
V1.3b	M1 enclosure of V1 when M1 enclosure on one or both perpendicular directions<0.03um	≥	0.03	um
V1.3c[R][NC]	V1 must be enclosed by M1 and the enclosure should be as large as layout allowed.			
V1.4	(Purposely blank)			
V1.5a	M2 enclosure of V1	≥	0.005	um
V1.5b	M2 Enclosure of V1 when M2 enclosure on one or both perpendicular directions < 0.02um	≥	0.02	um
V1.5c[R][NC]	V1 must be enclosed by M2 and the enclosure should be as large as layout allowed.			
V1.6	(Purposely blank)			
V1.7	(Purposely blank)			
V1.8	(Purposely blank)			
V1.9	(Purposely blank)			
V1.10	Space between two neighbor V1s (different net and run length>0)	≥	0.13	um
V1.11[R]	There should be at least two V1s in the M1and M2 intersection area when either or both M1 and M2 width >= 0.5um			
V1.12[R]	There should be at least two V1s in the M1and M2 intersection area when either or both M1 and M2 is connected with metal line of width>=0.5um and space between V1 and wider metal edge <0.5um			



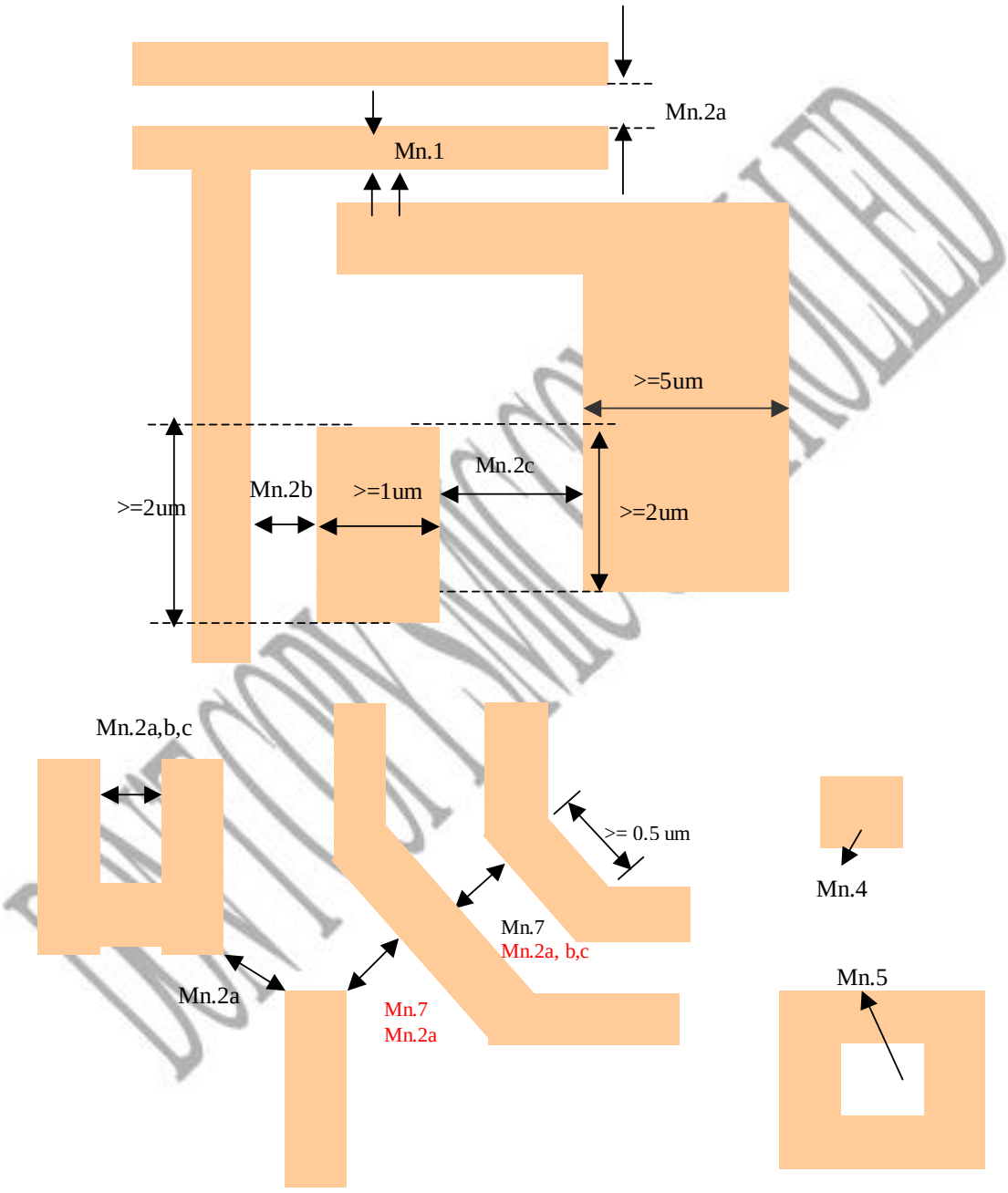


7.2.22 Mn: Metal n (n=2~8) design rules

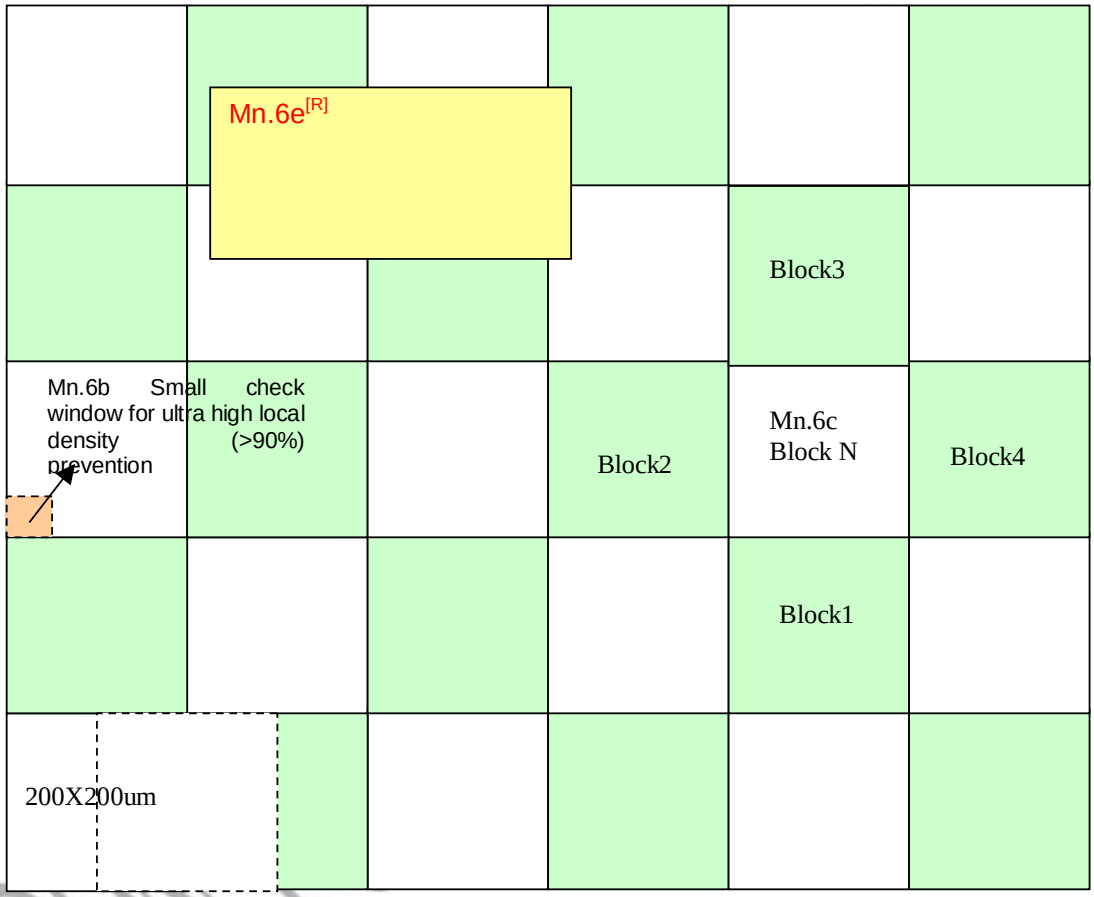
Rule number	Description	Operation	Design Value	Unit
Mn.1	Mn width	≥	0.10	um
Mn.2a	Space between two Mns	≥	0.10	um
Mn.2b	Space between two Mns when one or both Mn width or length≥1um, and the run length of two Mns is ≥2um	≥	0.16	um
Mn.2c	Space between two Mns when one or both Mn width or length ≥5um, and the run length of two Mns is ≥2um	≥	0.50	um
Mn.3	Mn width	≤	12.00	um
Mn.4	Mn area	≥	0.035	um^2
Mn.5	Enclosed dielectric area by Mn	≥	0.12	um^2
Mn.6a	Mn density (including dummy) in 200umX200um window with step size 100um. INDMY/MARKF/MARKG/MARKS covered areas are excluded for this rule checking	≥	18%	
		≤	80%	
Mn.6b	Mn density (including dummy) in 50umX50um window with step size 25um.	≤	90%	
Mn.6c	The difference between Mn density in 200umX200um with step size 200um and those of the adjacent checking windows (including dummy). INDMY/MARKG/MARKF/MARKS covered areas are excluded for this rule checking	≤	40%	
Mn.6d	Mn density (including dummy) in 25umX25um window with step size 12.5um. INDMY/MARKG/MARKS covered areas are excluded for this rule checking	≥	12%	
Mn.6e[R]	Average density for Mn inside the dummy block area in 25umX25um window with step size 12.5um when the dummy block area ≥ 25umX25um. INDMY/MARKF/MARKG/MARKS covered areas are excluded from this rule checking. Device sensitive areas can be waived.	≥	12%	
		≤	90%	

Mn.6f[R] [NC]	High metal density area (>70%) on consecutive layers is not recommended.			
Mn.7	Space between metal lines with one or both is 45 degree and the bending length >=0.5um (the area with 0.1um distance from bending point need not follow this rule)	≥	0.115	um
Mn.8[NC]	If designer needs to design metals wider than Mn.3, please comply with metal slot rules in section 7.2.34.13.			
Mn.9[NC]	Dummy filling rules refer to section 7.2.32.5			
Mn.10[R] [NC]	Recommend that the length of metal lines is perpendicular to the length of metal lines on neighboring layers.			

Note：Mn.2b, Mn.2c width or length checked by DRC is perpendicular to run length.



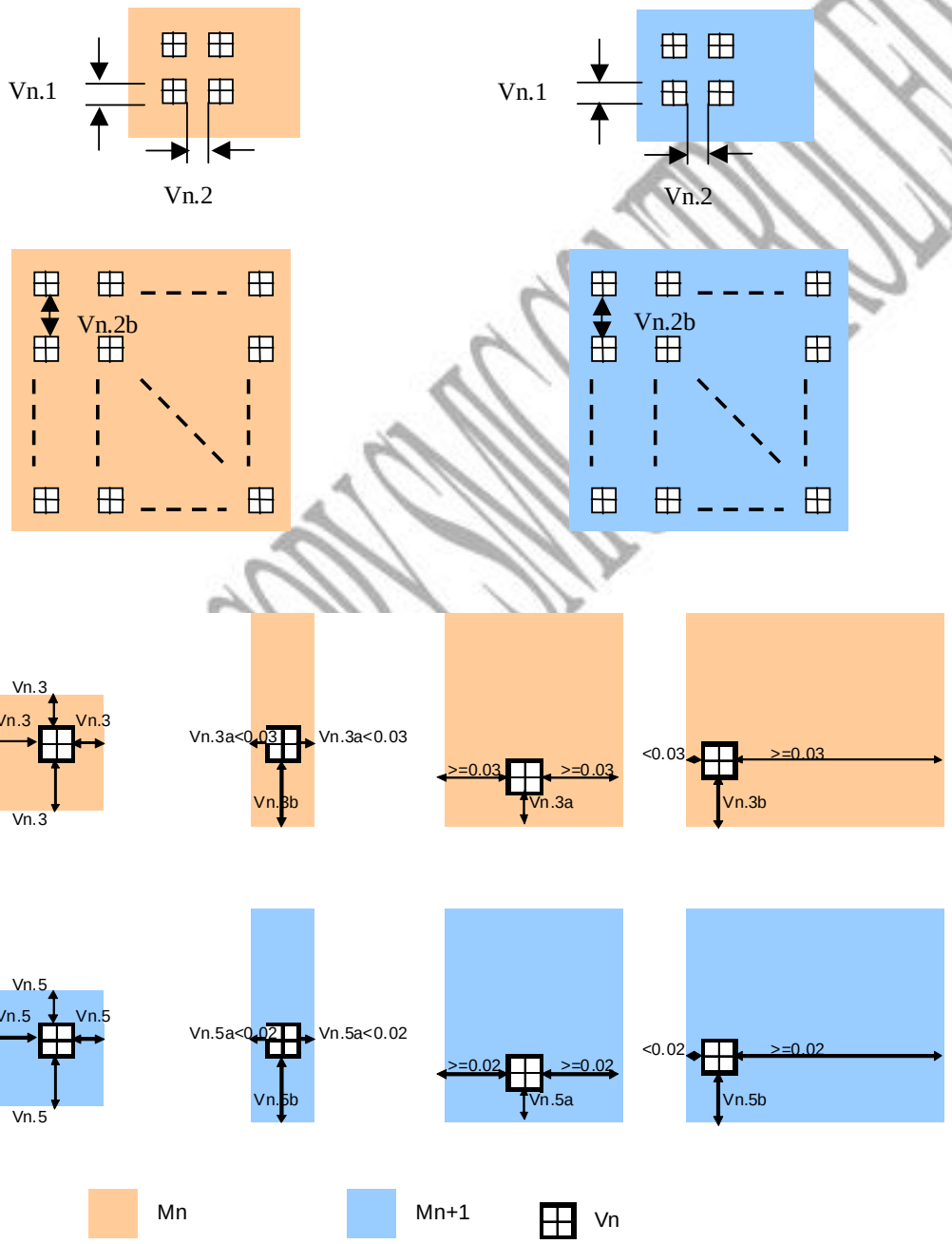
Whole chip vie

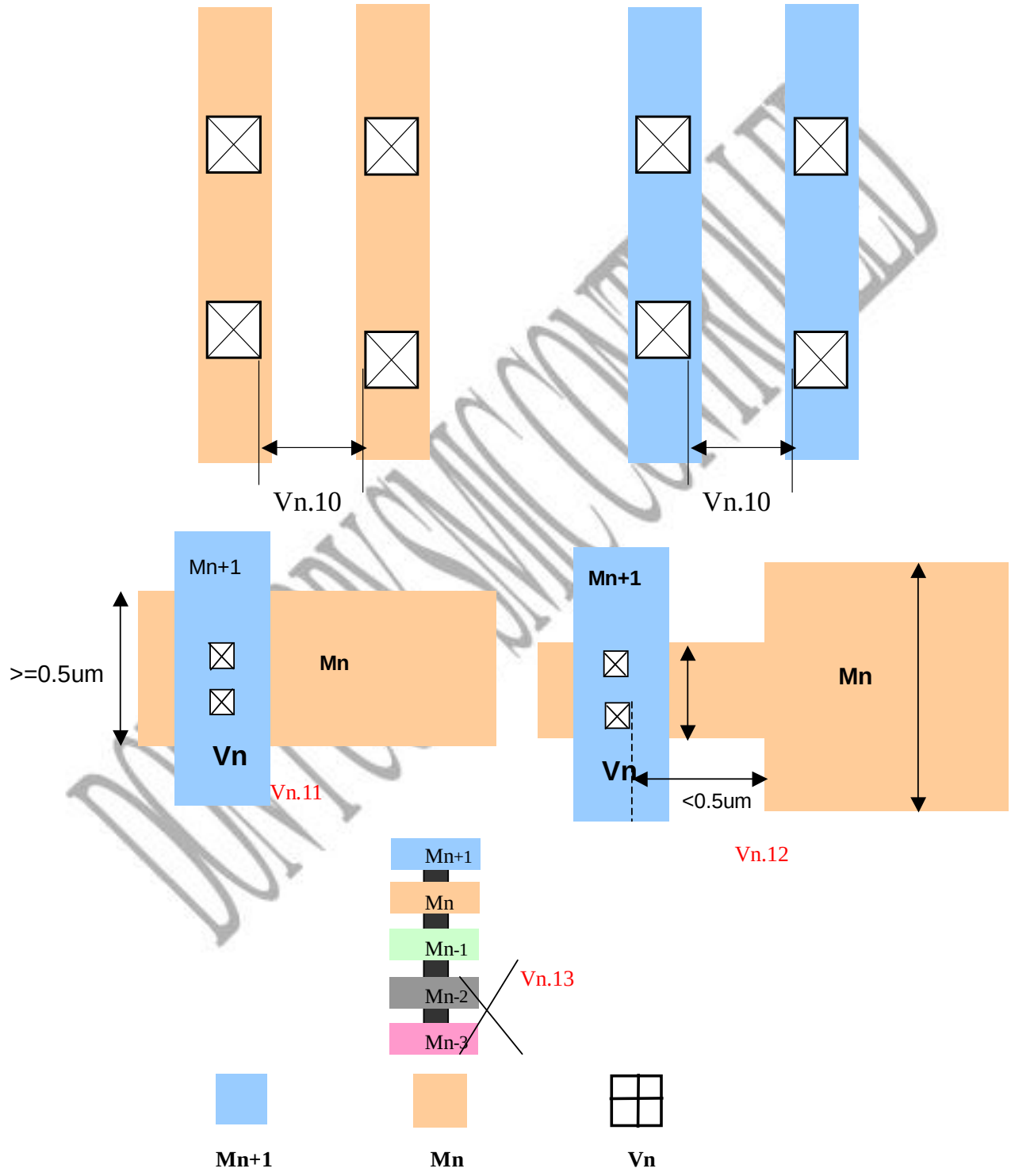


7.2.23 Vn: Via n (n=2,3,4,5,6,7) design rules

Rule number	Description	Operation	Design Value	Unit
Vn.1	Fixed Vn size (square shape)	=	0.09	um
Vn.2a	Space between two Vns	≥	0.11	um
Vn.2b	Space between Vns, when array equal to or greater than 4x4. Two via regions whose space is <0.15um are considered to be in the same array.	≥	0.13	um
Vn.3a	Mn enclosure of Vn	≥	0.005	um
Vn.3b	Mn enclosure of Vn when Mn enclosure on one or both perpendicular directions<0.03um	≥	0.03	um
Vn.3c[R][NC]	Vn must be enclosed by Mn and the enclosure should be as large as layout allowed			
Vn.4	(Purposely blank)			
Vn.5a	Mn+1 enclsoure of Vn	≥	0.005	um
Vn.5b	Mn+1 enclosure of Vn when Mn enclosure on one or both perpendicular directions<0.02um	≥	0.02	um
Vn.5c[R][NC]	Vn must be enclosed by Mn+1 and the enclosure should be as large as layout allowed.			
Vn.6	(Purposely blank)			
Vn.7	(Purposely blank)			
Vn.8	(Purposely blank)			
Vn.9	(Purposely blank)			
Vn.10	Space between two neighbor Vns (different net and run length>0)	≥	0.13	um
Vn.11[R]	There should be at least two Vns in the Mn and Mn+1 intersection area when either or both Mn and Mn+1 with width >= 0.5um			
Vn.12[R]	There should be at least two Vns in the Mn and Mn+1 intersection area when either or both Mn and Mn+1 connected with metal line of width>=0.5um and space between Vn and			

	wider metal edge <0.5um			
Vn.13R[R][NC]	Single vias stacked by more than 3 layers are not allowed.			



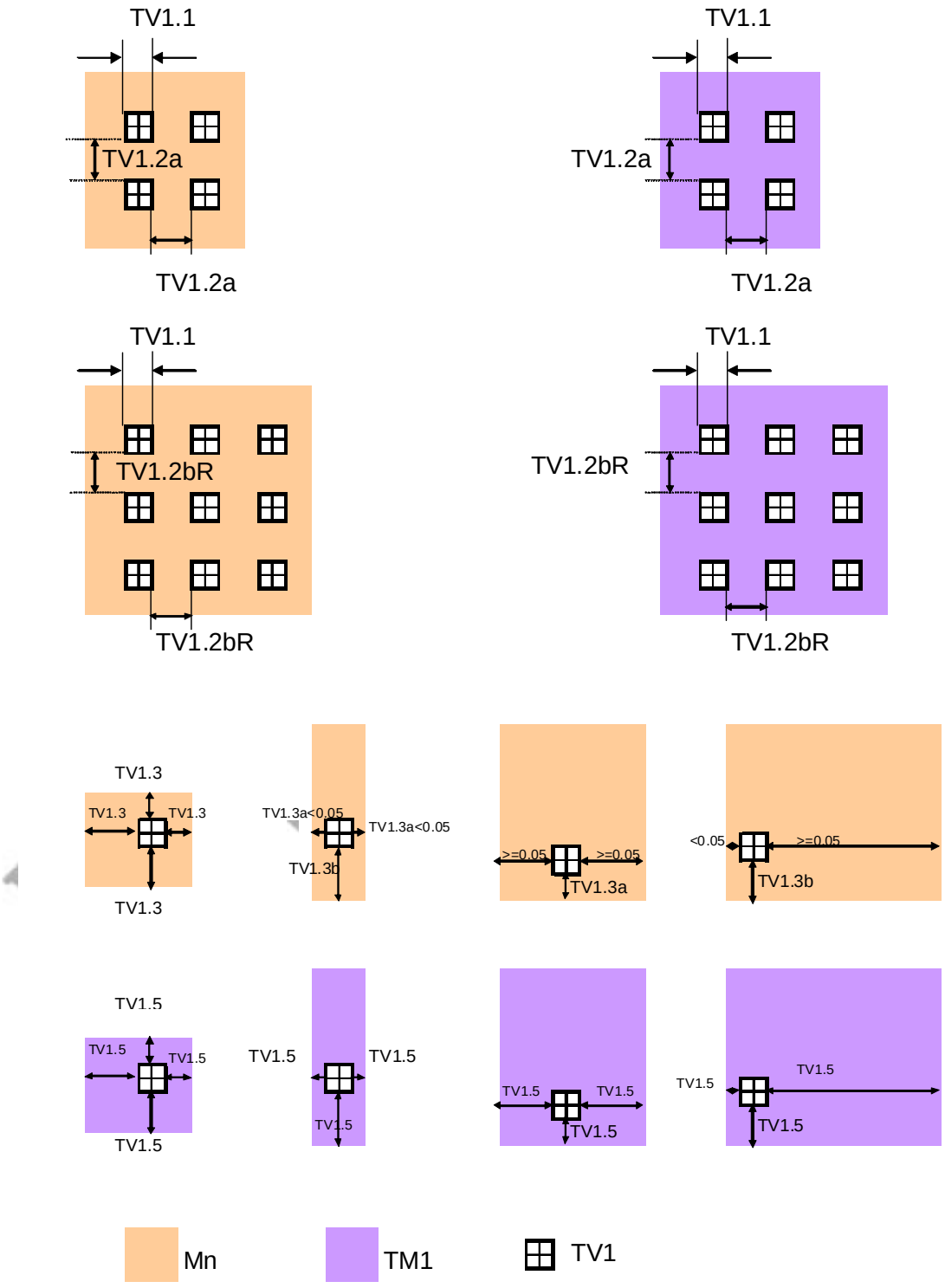


7.2.24 TV1/TM1: Top Via1/TM1 design rules

SMIC can provide two options for top via one/ top metal one loop. Both options use oxide as dielectric film, but the minimum design rule and Cu thickness are different. Please find the below tables for details.

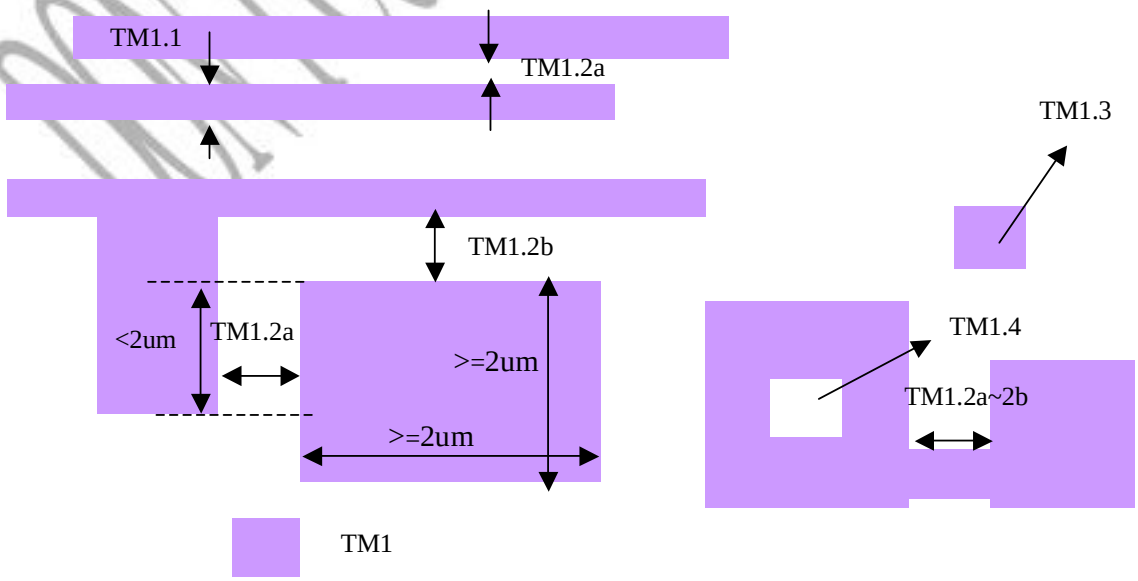
7.2.24.1 Standard offering for 4X design rule TV1-TM1

Rule number	Description	Operation	Design Value	Unit
TV1.1	Fixed TV1 size (square shape)	=	0.36	um
TV1.2a	Space between two TV1s	≥	0.34	um
TV1.2b[R]	Space between TV1s within array greater or equal to 3x3 （Two via regions whose space is ≤0.56um are considered to be in the same array）	≥	0.5	um
TV1.3a	Mn enclosure of TV1 (Mn is Metal layer directly underneath TV1)	≥	0.01	um
TV1.3b	Mn enclosure of TV1 when Mn enclosure on one or both perpendicular directions< 0.05um (Mn is Metal layer directly underneath TV1)	≥	0.05	um
TV1.4	(Purposely blank)			
TV1.5	TM1 enclosure of TV1 (four directions)	≥	0.02	um
TV1.6	(Purposely blank)			
TV1.7	(Purposely blank)			
TV1.8	(Purposely blank)			



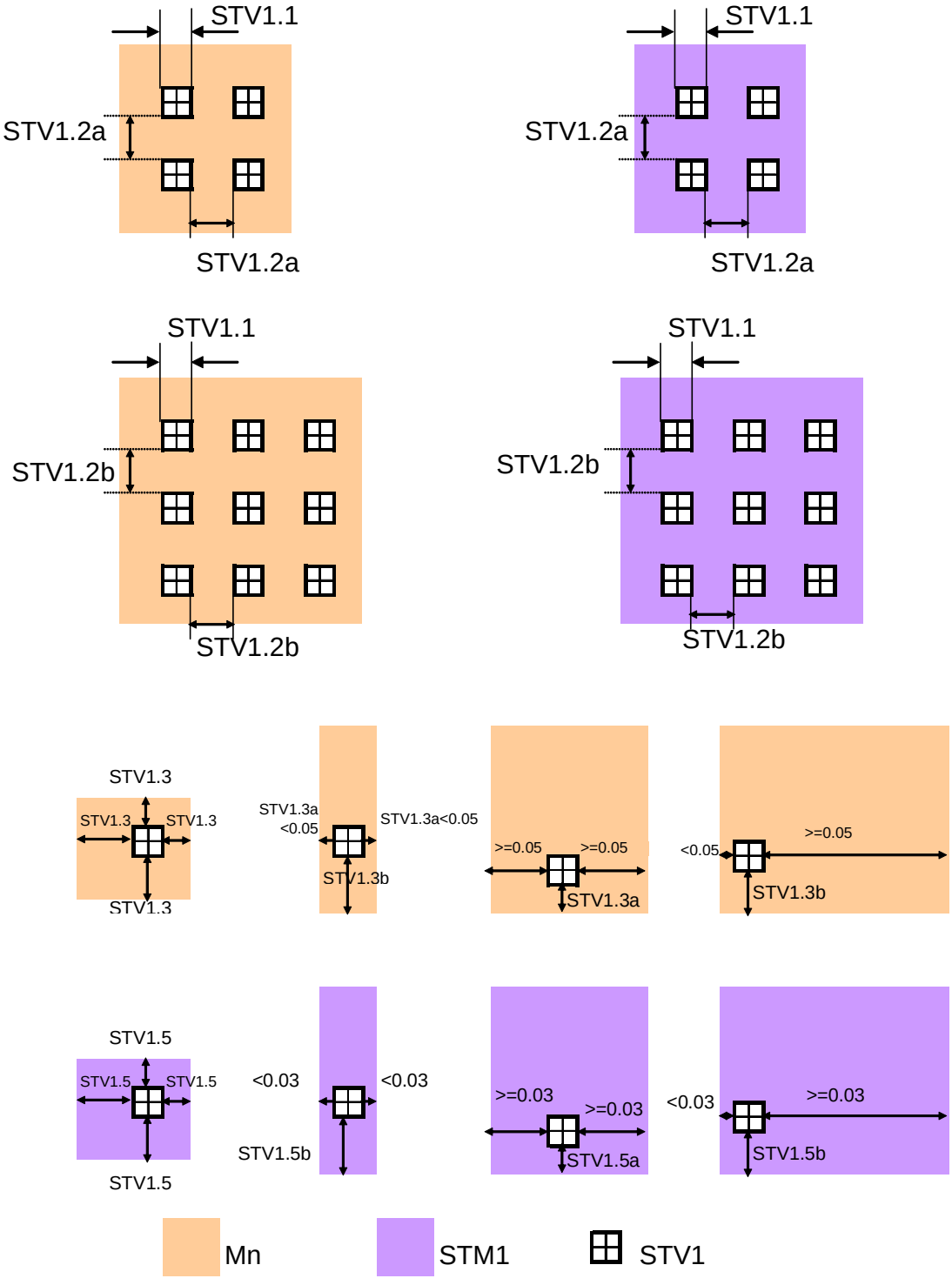
Rule number	Description	Operation	Design Value	Unit
TM1.1	TM1 width	≥	0.40	um
TM1.2a	Space between two TM1s	≥	0.40	um
TM1.2b	Space between two TM1s when one or both TM1 width or length ≥2um, and the run length of two TM1s is ≥2um	≥	0.50	um
TM1.3	TM1 area	≥	0.40	um^2
TM1.4	Enclosed dielectic area by TM1	≥	0.60	um^2
TM1.5	TM1 width (Top metal bond pad application can be waived.)	≤	20.00	um
TM1.6	TM1 density (including dummy) in 200umX200um window with step size 100um. INDMY/MARKF/MARKG/MARKS covered areas are excluded for this rule checking. (Top metal bond pad areas can be waived.)	≥ ≤	20% 85%	
TM1.7[NC]	If customers need to design wide metal lager than TM1.5, please comply with metal slot rules in section 7.2.34.13 (Top metal bond application can be waived.)			
TM1.8[NC]	Dummy filling rules refer to section 7.2.32.7			

Note: TM1.2b width or length checked by DRC is perpendicular to run length.



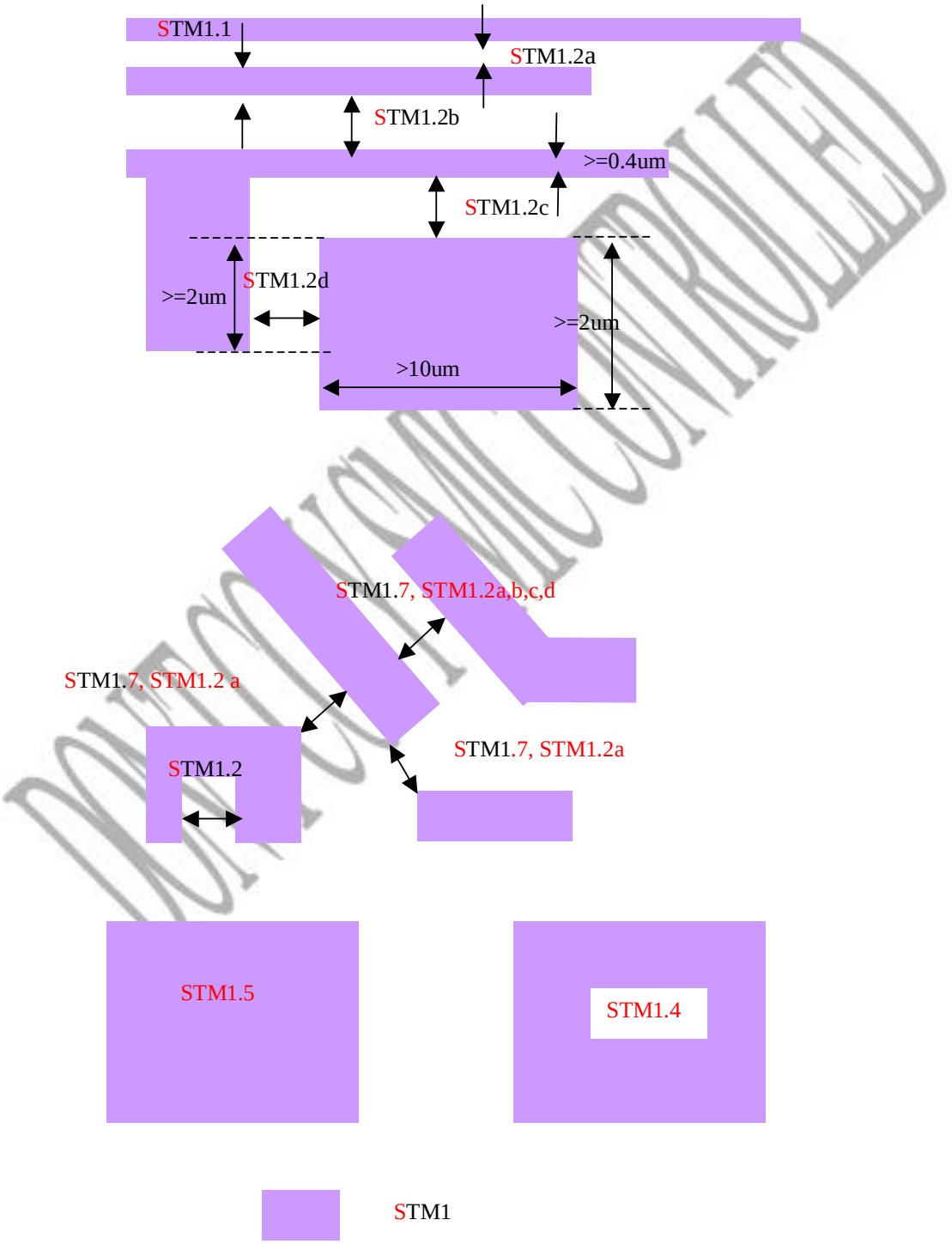
7.2.24.2 Special offering for 2X design rule STV1-STM1

Rule number	Description	Operation	Design Value	Unit
Rule number	**Description**	**Operation**	**Design Value**	**Unit**
STV1.1	Fixed STV1 size (square shape)	=	0.20	um
STV1.2a	Space between two STV1s	≥	0.20	um
STV1.2b	Space between STV1s within array greater or equal to 3x3 （Two via regions whose space is ≤0.30um are considered to be in the same array）	≥	0.25	um
STV1.3a	Mn enclosure of STV1 (Mn is Metal layer directly underneath STV1)	≥	0.00	um
STV1.3b	Mn Enclosure of STV1 when Mn enclosure on one or both perpendicular directions< 0.05um (Mn is Metal layer directly underneath STV1)	≥	0.05	um
STV1.4	(Purposely blank)			
STV1.5a	STM1 enclosure of STV1	≥	0.02	um
STV1.5b	STM1 Enclosure of STV1 when STM1 enclosure on one or both perpendicular directions< 0.03um	≥	0.03	um
STV1.6	(Purposely blank)			
STV1.7	(Purposely blank)			
STV1.8	(Purposely blank)			
STV1.9	There should be at least two STV1s in this Mn and STM1 intersection area when either or both Mn (Mn is Metal layer directly underneath STV1) and STM1 width is > 0.9um.			



Rule number	Description	Operation	Design Value	Unit
STM1.1	STM1 width	≥	0.20	um
STM1.2a	Space between STM1s	≥	0.20	um
STM1.2b	Space between two STM1s when one or both STM1 width or length ≥0.4um, and the run length of two STM1s is ≥0.4um	≥	0.25	um
STM1.2c	Space between two STM1s when one or both STM1 width or length≥2um, and the run length of two STM1s is ≥2um	≥	0.40	um
STM1.2d	Space between two STM1s when one or both STM1 width or length≥10um, and the run length of two STM1s is ≥2um	≥	0.50	um
STM1.3	STM1 area	≥	0.12	um^2
STM1.4	Enclosed dielectric area by STM1	≥	0.26	um^2
STM1.5	STM1 width	≤	20.00	um
STM1.6	STM1 density (including dummy) in 200umX200um window with step size 100um. INDMY/MARKF/MARKG/MARKS covered areas are excluded for this rule checking. Top metal bond pad areas can be waived	≥	20%	
		≤	85%	
STM1.7	Space between STM1 metal lines with one or both are 45 degree bent metal lines	≥	0.22	um
STM1.8[NC]	If customers need to design wide metal lager than STM1.5, please comply with metal slot rule 7.2.34.13.			
STM1.9[NC]	Dummy filling rules refer to 7.2.32.7.			

Note: STM1.2b, STM1.2c, STM1.2d width or length checked by DRC is perpendicular to run length.

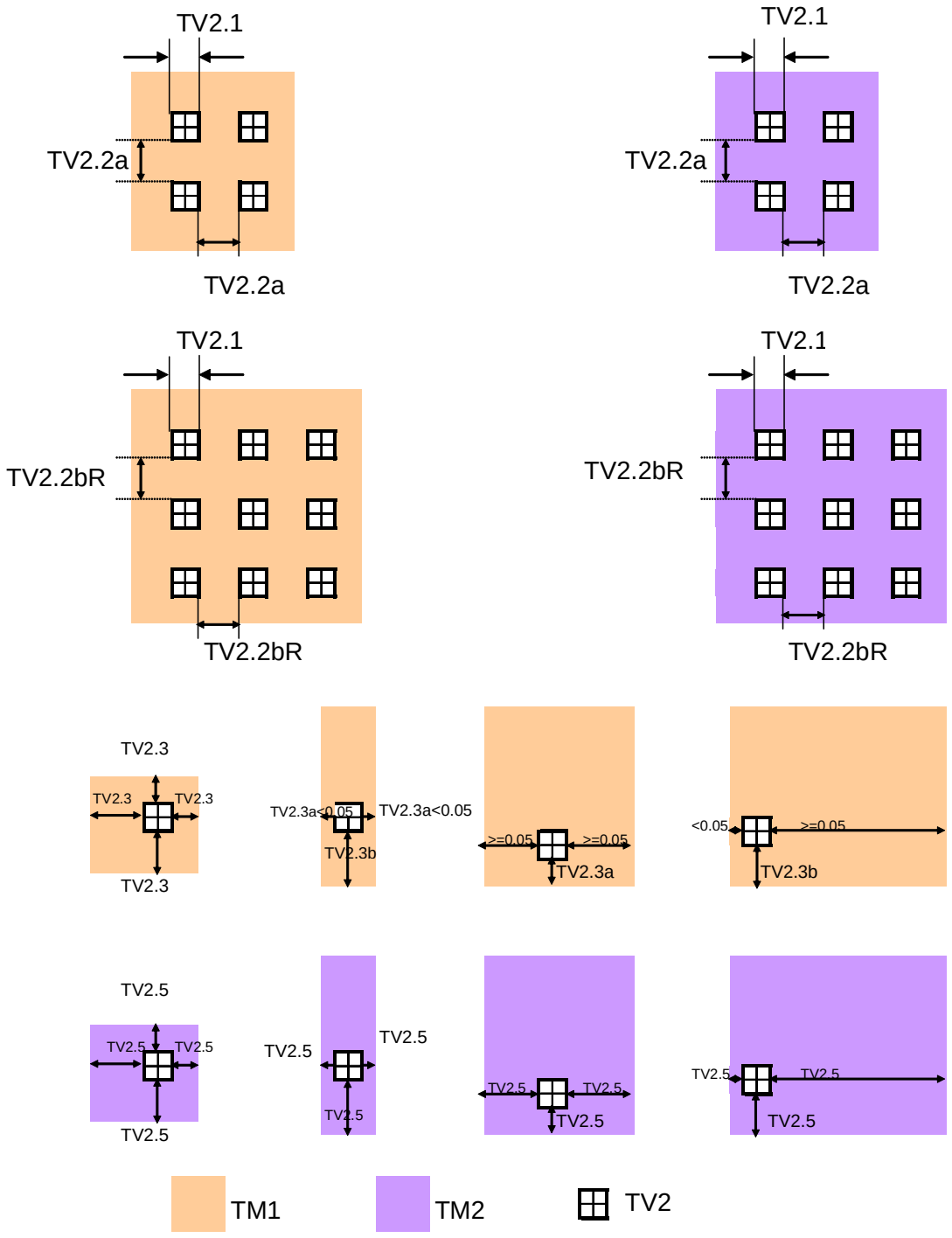


7.2.25 TV2/TM2: Top Via2 /Top Metal2 design rules

SMIC can provide three options for top via two (TV2) to top metal two (TM2) loop. Three options use oxide as dielectric film, but the minimum design rule and Cu thickness are different. Please find the below table for details.

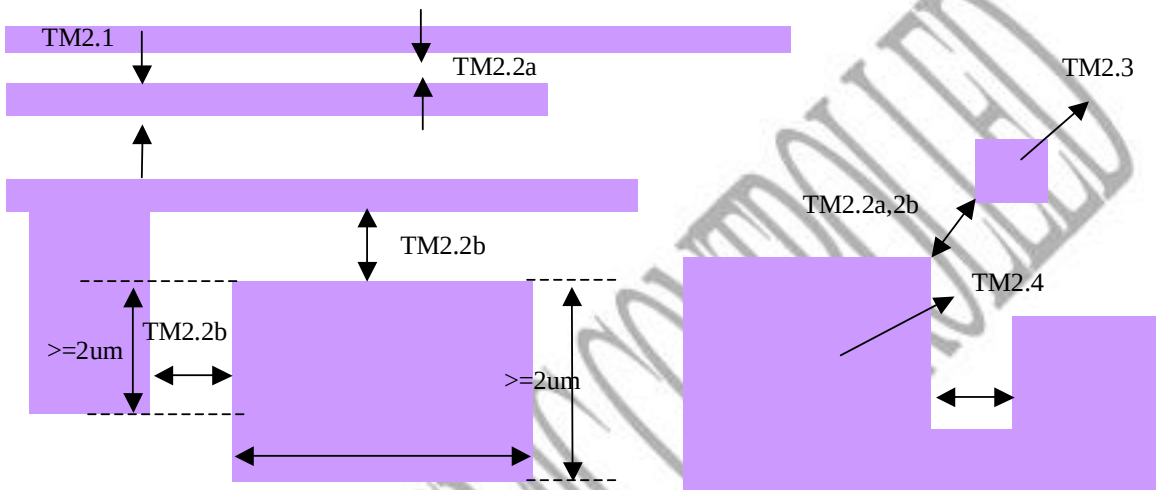
7.2.25.1 Standard offering for 4X design rule TV2-TM2

Rule number	Description	Operation	Design Value	Unit
TV2.1	Fixed TV2 size (square shape)	=	0.36	um
TV2.2a	Space between two TV2s	≥	0.34	um
TV2.2b[R]	Recommended space between TV2s within array greater or equal to 3x3 （Two via regions whose space is ≤0.56um are considered to be in the same array）	≥	0.5	um
TV2.3a	TM1 enclosure of TV2	≥	0.01	um
TV2.3b	TM1 enclosure of TV2 when TM1 enclosure on one or both perpendicular directions < 0.05um	≥	0.05	um
TV2.4	(Purposely blank)			
TV2.5	TV2 enclosure by TM2 (four directions)	≥	0.02	um
TV2.6	(Purposely blank)			
TV2.7	(Purposely blank)			
TV2.8	(Purposely blank)			
TV2.9[NC]	For the case that only one top metal layer is needed, TV2/TM2 should be used. TM1 in this page will be replaced by Mn underneath TV2.			



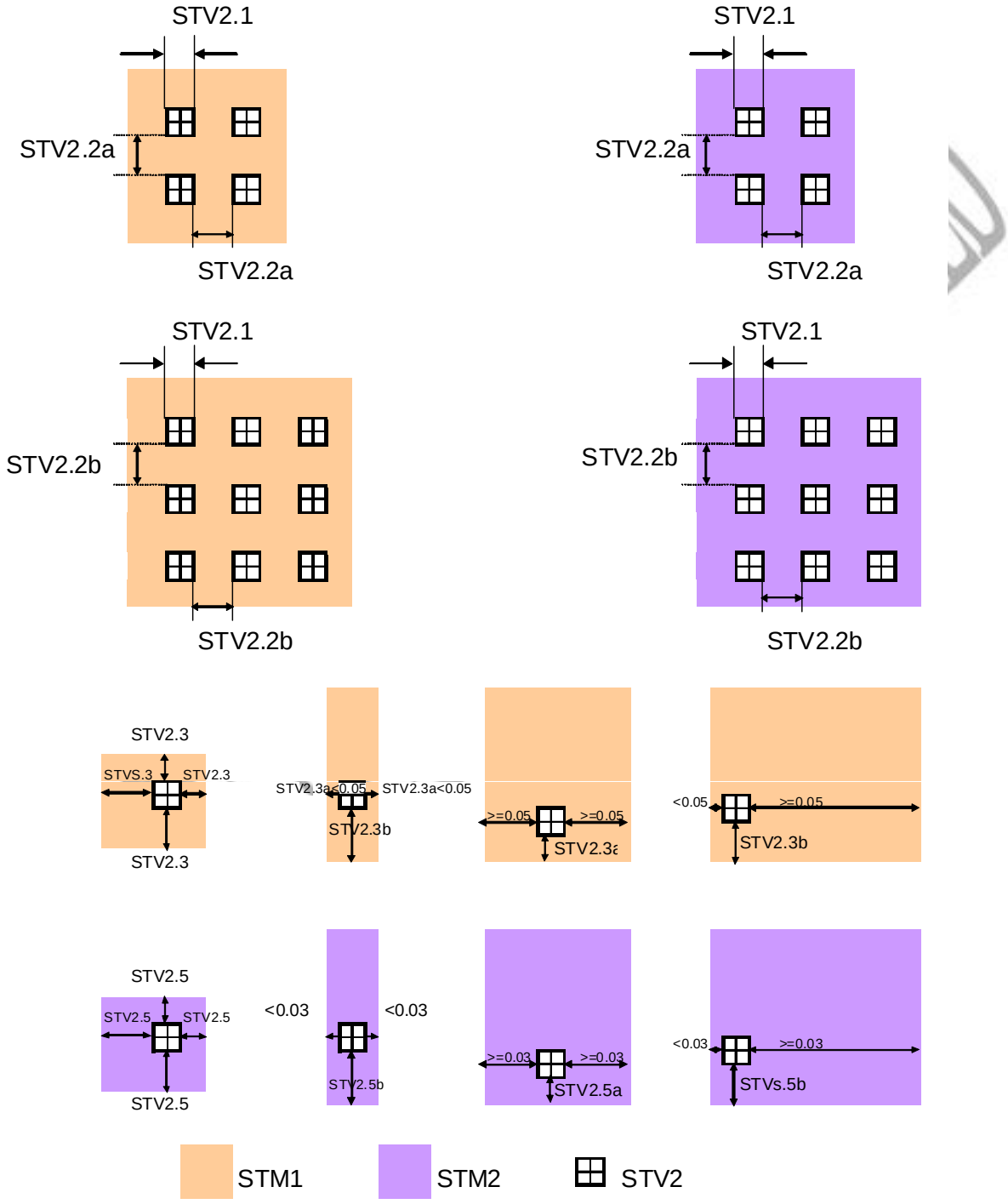
Rule number	Description	Operation	Design Value	Unit
TM2.1	TM2 width	≥	0.40	um
TM2.2a	Space between TM2s	≥	0.40	um
TM2.2b	Space between two TM2s when one or both TM2 width or length≥2um, and the run length of two TM2s is ≥2um	≥	0.50	um
TM2.3	TM2 area	≥	0.40	um^2
TM2.4	Enclosed dielectic area by TM2	≥	0.60	um^2
TM2.5	TM2 width Top metal bondpads can be waived.	≤	30.00	um
TM2.6	(Purposely blank)			
TM2.7	TM2 density (including dummy) in 400umX400um window with step size 200um. INDMY/MARKF/MARKG/MARKS covered areas are excluded for this rule checking. Top metal bond pad areas can be waived.	≥	20%	
		≤	85%	
TM2.8[NC]	If customers need to design wide metal lager than TM2.5, please comply with metal slot rule 7.2.34.13. Top metal bondpad application can be waived.			
TM2.9[NC]	Dummy insertion rules refer to section 7.2.32.9.			

Note: TM2.2b width or length checked by DRC is perpendicular to run length.



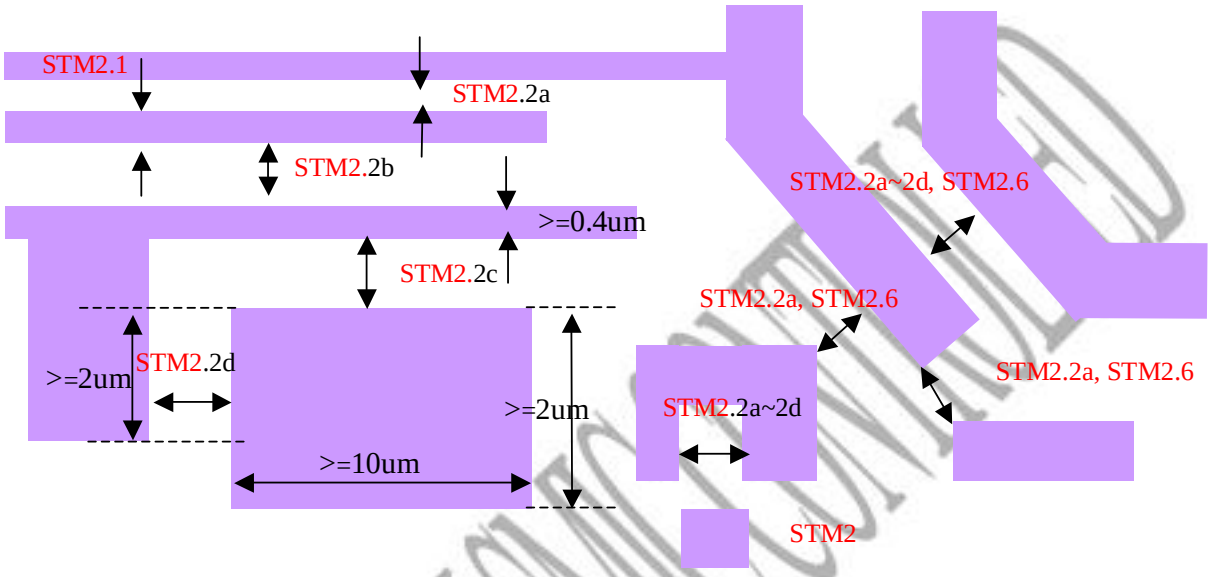
7.2.25.2 2X design rules for STV2-STM2

Rule number	Description	Operation	Design Value	Unit
STV2.1	Fixed STV2 size (square shape)	=	0.20	um
STV2.2a	Space between two STV2s	≥	0.20	um
STV2.2b	Space between STV2s, when array equal to or greater than 4x4. Two via regions whose space is <=0.30um are considered to be in the same array.	≥	0.25	um
STV2.3a	STM1 enclosure of STV2	≥	0.00	um
STV2.3b	STM1 enclosure of STV2 when STM1 enclosure on one or both perpendicular directions < 0.05um	≥	0.05	um
STV2.4	(Purposely blank)			
STV2.5a	STM2 enclosure of STV2	≥	0.00	um
STV2.5b	STM2 enclosure of STV2 when STM2 enclosure on one or both perpendicular directions <0.03um	≥	0.03	um
STV2.6	(Purposely blank)			
STV2.7	(Purposely blank)			
STV2.8	(Purposely blank)			
STV2.9	There should be at least two STV2s in the STM1 and STM2 intersection area, when either or both STM1 and STM2 width > 0.9um.			
STV2.10[NC]	For the case that only one top metal layer is needed, STV2 and STM2 should be used. STM1 in this page will be replaced by Mn underneath STV2.			



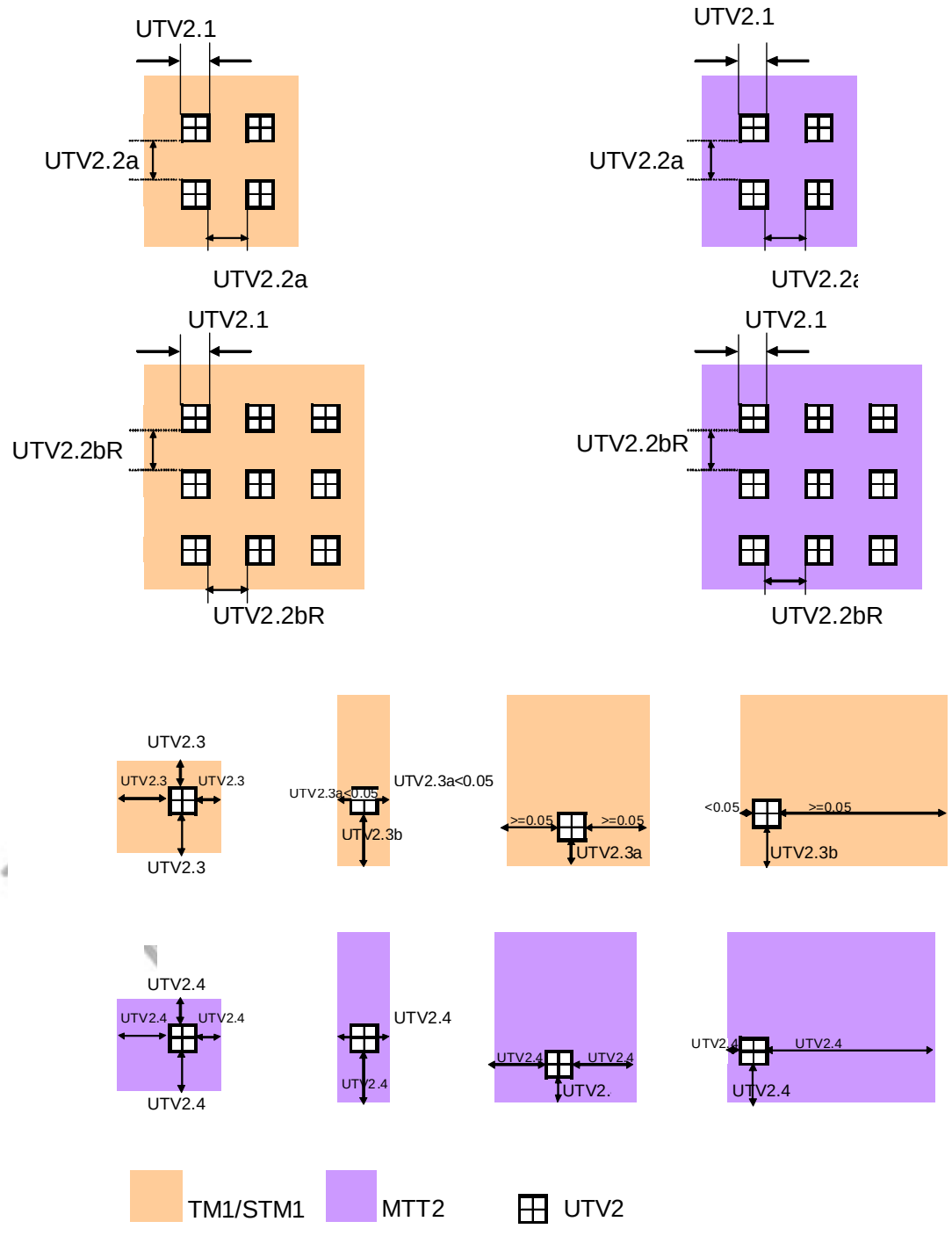
Rule number	Description	Operation	Design Value	Unit
STM2.1	STM2 width	≥	0.20	um
STM2.2a	Space between STM2s	≥	0.20	um
STM2.2b	Space between two STM2s when one or both STM2 width or length≥0.4um, and the run length of two STM2s ≥0.4um	≥	0.25	um
STM2.2c	Space between two STM2s when one or both STM2 width or length≥2um, and the run length of two STM2s ≥2um	≥	0.40	um
STM2.2d	Space between two STM2s when one or both STM2 width or length≥10um, and the run length of two STM2s≥2um	≥	0.50	um
STM2.3	STM2 area	≥	0.12	um^2
STM2.4	Enclosed dielectric area by STM2	≥	0.26	um^2
STM2.5	STM2 width Top metal bondpad application can be waived.	≤	30.00	um
STM2.6	Space between metal lines with one or both are 45 degree bent metal lines	≥	0.22	um
STM2.7	(Purposely blank)			
STM2.8	STM2 density (including dummy) in 400umX400um window with step size 200um.	≥	20%	
	INDMY/MARKF/MARKG/MARKS covered areas are excluded for this rule checking.	≤	85%	
STM2.9[NC]	If customers need to design wide metal lager than STM2.5, please comply with metal slot rule 7.2.34.13. Top metal bondpad application can be waived.			
STM2.10[NC]	Dummy filling rule refer to section 7.2.32.9.			

Note: STM2.2b~2d width or length checked by DRC is perpendicular to run length.



7.2.25.3 For RF product application: UTV2-MTT2

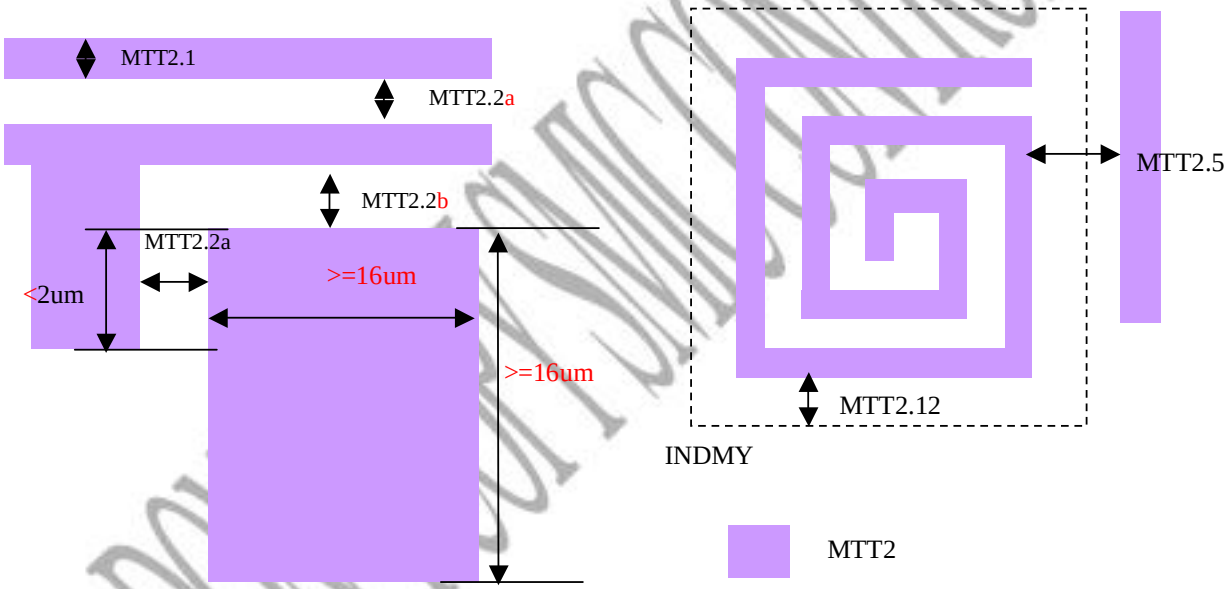
Rule number	Description	Operation	Design Value	Unit
UTV2.1	Fixed UTV2 size (square shape)	=	0.36	um
UTV2.2a	Space between two UTV2s	≥	0.34	um
UTV2.2b[R]	Recommended space between UTV2s, when array equal to or greater than 4x4. (Two via regions whose space is <=0.56um are considered to be in the same array.)	≥	0.5	um
UTV2.3	TM1 enclosure of UTV2 (TM1 is replaced with STM1 if 2X STM1 is used under UTV2)	≥	0.01	um
UTV2.4	TM1enclosure of UTV2 when TM1 enclosure on one or both perpendicular directions < 0.05um (TM1 is replaced with STM1 if 2X STM1 is used under UTV2)	≥	0.05	um
UTV2.5	MTT2 enclosure of UTV2 (four directions)	≥	0.30	um
UTV2.6[NC]	For the case that only one top metal layer is needed, TM1/STM1 in this page will be replaced by Mn underneath UTV2.			



Rule number	Description	Operation	Design Value	Unit
MTT2.1	MTT2 metal width	≥	1.50	um
MTT2.2a	Space between MTT2s	≥	1.50	um
MTT2.2b	Space between two MTT2s when one or both MTT2 width or length ≥16um, and the run length of two MTT2s >2um	≥	2.00	um
MTT2.3	(Purposely blank)			
MTT2.4	(Purposely blank)			
MTT2.5	Space between an Inductor MTT2 and other MTT2	≥	30	
MTT2.6	MTT2 area	≥	8	um^2
MTT2.7	Enclosed dielectic area by MTT2s	≥	6	um^2
MTT2.8	MTT2 width	≤	50	um
MTT2.9a	MTT2 density (including dummy) in 400umX400um window with step size 200um.	≤	70%	
MTT2.9b	MTT2 pattern density on the whole chip (including dummy patterns)	≤	55%	
MTT2.9c[R]	Recommend the average MTT2 density of whole chip is larger than 20% (including dummy patterns), otherwise SMIC would help to add dummy patterns.	≥	20%	
MTT2.10	Both active and passive devices inside Inductor area are not allowed.			
MTT2.11	(Purposely blank)			
MTT2.12	MTT2 Inductor area must by covered by “INDMY” and the enclosure by “INDMY”	≥	15	um
MTT2.13[NC]	No Via and metal patterns inside “INDMY” area are allowed, except for components of inductors including inductor connection, guard ring, dummy metal or patterned ground shielding.			
MTT2.14	(Purposely blank)			

MTT2.15	(Purposely blank)			
MTT2.16[NC]	If customers need to design wide metal lager than MTT2.8, please comply with metal slot rule section 7.2.34.13. Top metal bondpad application can be waived.			
MTT2.17[NC]	Dummy filling rule refer to section 7.2.32.9.			

Note: MTT2 width or length checked by DRC is perpendicular to run length.



7.2.26 Passivation one (PA1) design rules

Passivation 1 patterns can be formed by PA or/and RDL VIA layers.

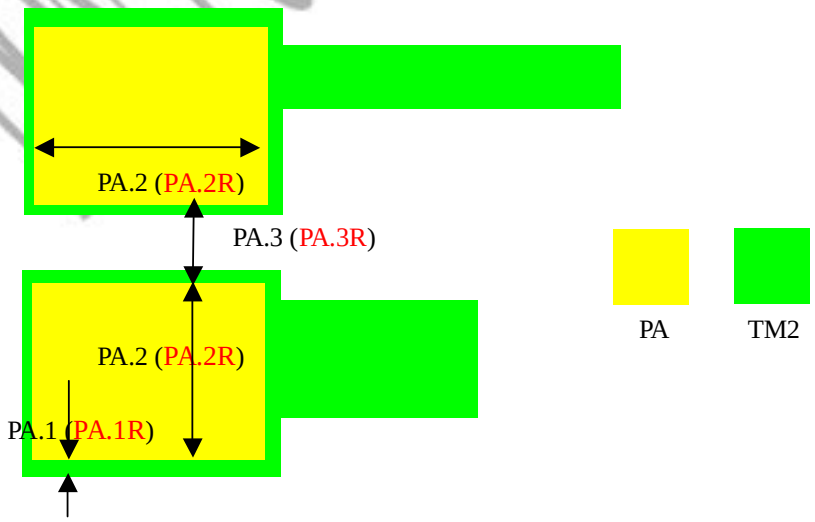
7.2.26.1 PA rule

"PA" gds layer can be used to draw pad openings that connect top Cu (TM2 or MTT) pads to AL pads. The below table is for process minimum concern, but not for package rules.

Rule number	Description	Operation	Design Value	Unit
PA.1	PA enclosure by TM2 or other metal layer directly underneath PA	≥	1.0	um
PA.2	PA width and length	≥	3.0	um
PA.3	Space between two PAs	≥	3.0	um

For general application of AL wire bonding pads, below minimum dimensions are recommended. Please consult the packaging house for the pad requirements. Al wire bonding pads can be generated from PA layer.

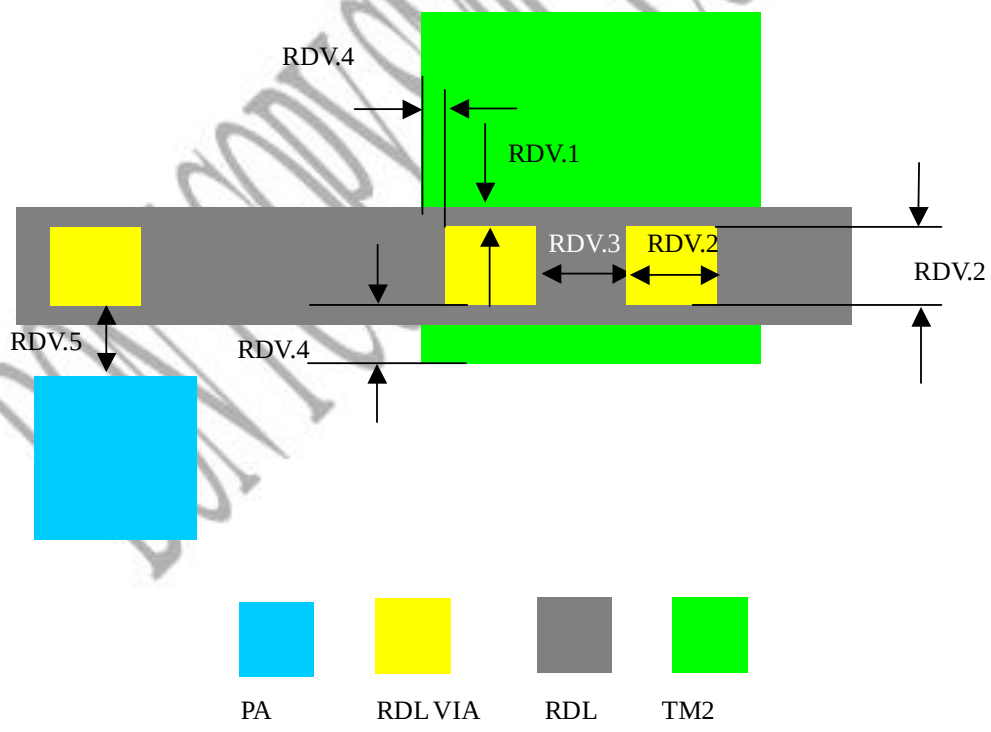
Rule number	Description	Operation	Design Value	Unit
PA.1[R]	PA enclosure by TM2 or other metal layer directly underneath PA	≥	1.5	um
PA.2[R]	PA width and length	≥	55	um
PA.3[R]	Space between two PAs	≥	5.0	um



7.2.26.2 RDL via design rules

"RDL via" gds layer is normally used to draw AL RDL via openings that connect RDL and TM patterns.

Rule Number	Description	Operation	Design Value	Unit
RDV.1	RDL via enclosure by RDL (except fuse, seal ring and guard ring design)	≥	1.5	um
RDV.2	RDL Via width and length (except fuse, seal ring and guard ring design)	≥	3.0	um
RDV.3	Space between two RDL vias	≥	3.0	um
RDV.4	RDL via enclosure by TM2 or other metal layer directly underneath PA1 (except seal ring and guard ring design)	≥	1.0	um
RDV.5	Space between RDL via and PA	≥	5.0	um



7.2.27 RDL (AL re-distribution layer) design rules

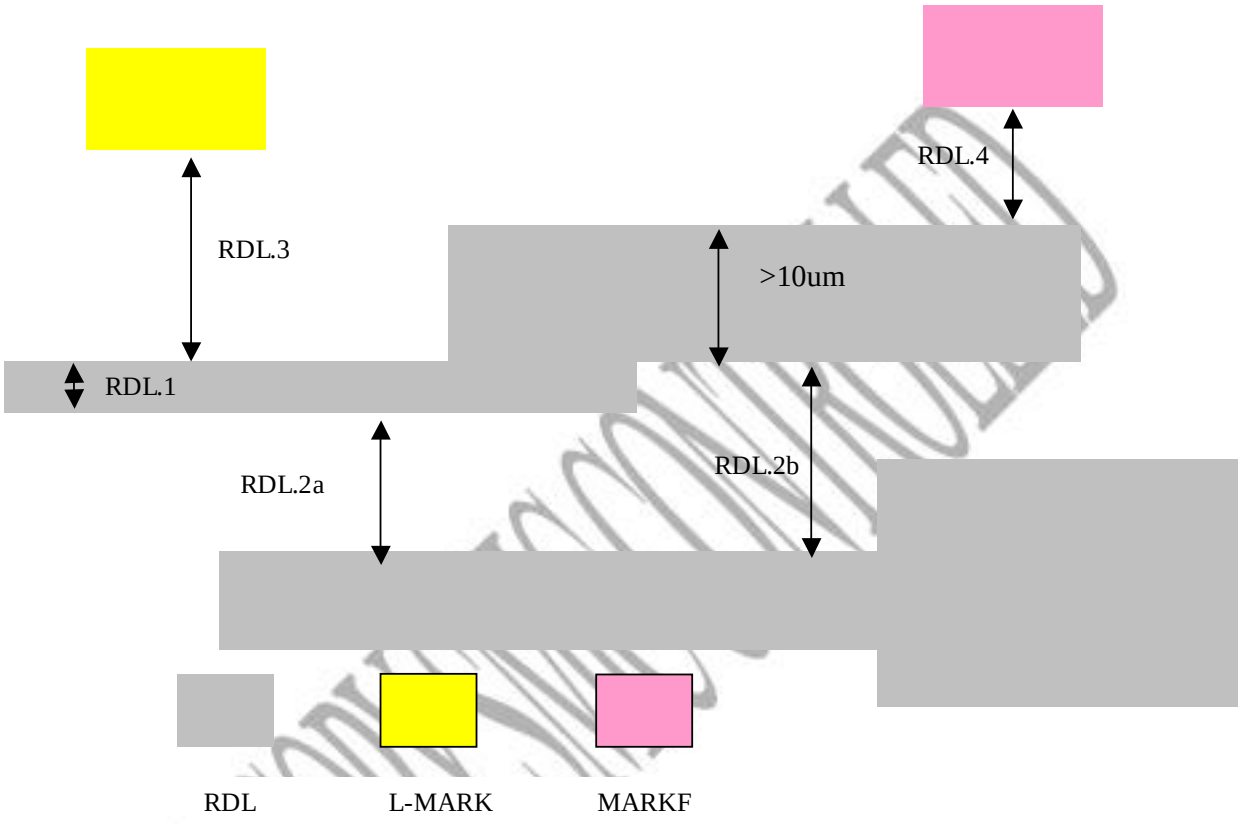
SMIC can support two options for RDL layer, one is standard 14.5K RDL thickness and the other is for 28K RDL thickness. Both options could share the same design rules.

RDL layer can be used to draw AL inter-connect lines, Al fuse metal line, AL bumping pads and re-distribution AL pads.

Rule Number	Description	Operation	Design Value	Unit
RDL.1	RDL Width (except fuse design)	≥	3.0	um
RDL.2a	Space between two RDLs	≥	2.0	um
RDL.2b	Space between two RDLs with one or both RDL width larger than 10um	≥	3.0	um
RDL.3	Space between RDL and L mark window	≥	10.0	um
RDL.4	Space between RDL and fuse area (marked by MARKF)	≥	10.0	um

Notes:

1. If RDL is used for AL bumping or re-distributed AL pads, suggest consulting with package vendors for the dimension.



7.2.28 ALPA rules

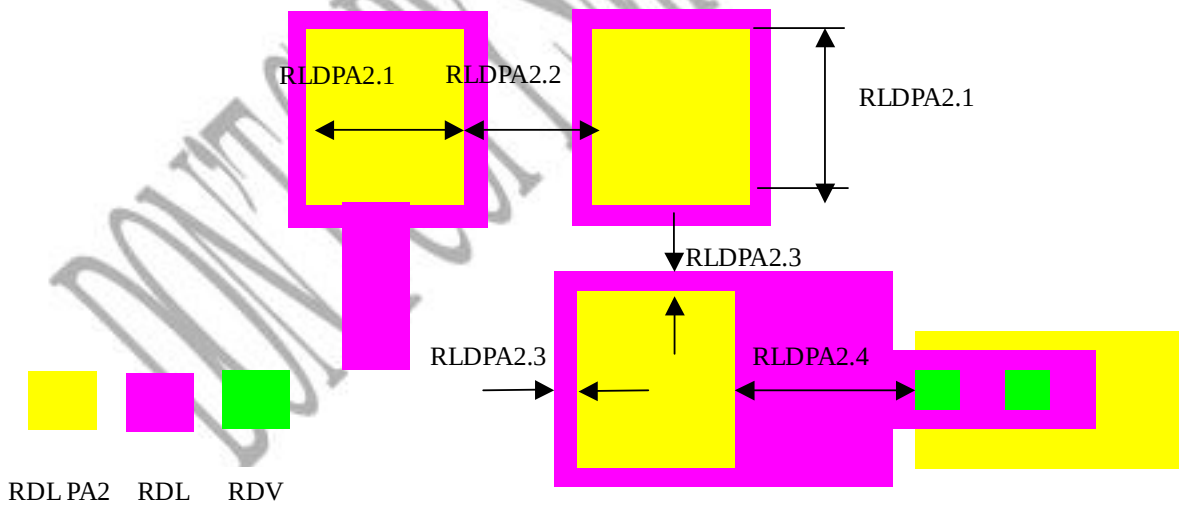
ALPA patterns include Al pads generated by PA logic generation and RDL patterns. Please check below rules after logic operation.

Rule Number	Description	Operation	Design Value	Unit
ALPA.1	PA opening without ALPA patterns above landed on TM2 is not allowed. ALPA patterns enclosure of PA	≥	1.5	um
ALPA.2	Space between ALPA patterns	≥	2	um
ALPA.3	Space between Al patterns of width larger than 35um and Fuse window edge	≥	50	um

7.2.29 Passivation 2 design rules

Passivation 2 patterns can be generated by PA or/and RDL PA2 layers. Regular pad openings are normally generated by PA (see 7.2.26.1). RDL PA2 can be used for openings of AL redistributed patterns, such as bumping pads. RDL PA2 should follow the below rules.

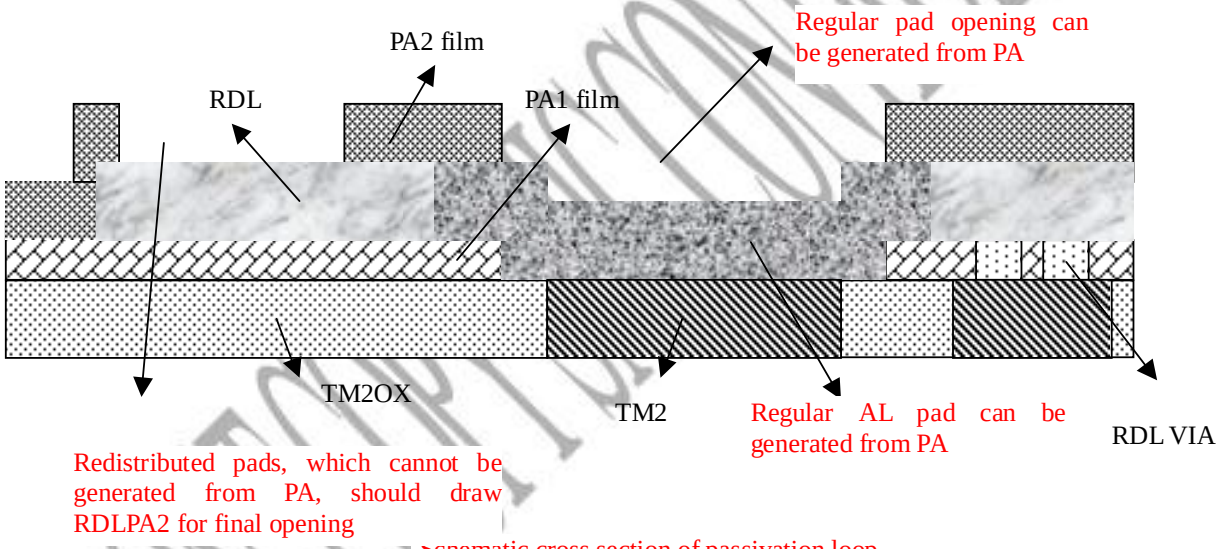
Rule Number	Description	Operation	Design Value	Unit
RDLPA2.1	RDL PA2 width (suggest to consult with package vendor)	≥	10.0	um
RDLPA2.2	Space between two RDL PA2 (suggest to consult with package vendor)	≥	5.0	um
RDLPA2.3	RDL enclosure of PA2	≥	1.5	um
RDLPA2.4	Space between RDLPA2 and RDL via (except fuse and guard ring/seal ring design)	≥	1.0	um
RDLPA2.5	RDL Via is not allowed to be overlapped with RDLPA2			



7.2.30 Passivation loop schematic

Designer should follow below table and cross section schematic for passivation loop and RDL design.

SMIC drawing layer	GDS #	Data type	With RDL application	Without RDL application
PA	80	0	V	V
BCB1 (RDL via)	165	0	V	X
RDL	166	0	V	X
BCB2 (RDL PA2)	167	0	V	X



Schematic cross section of passivation loop and RDL/RDL via

7.2.31 Chip edge BORDER layer design rule

This section is used only for the designs on which designer does not put seal rings. Chip edge BORDER layer and layout pattern rules are defined to avoid any layout pattern extending out to the scribe lane regions. Designer must draw border layer if they do not put the seal ring in the design.

For the designs of seal ring, please refer to Section 7.2.34.8 Seal ring and chip edge definition.

Border rule is only applied for chip level, IP level doesn't need to follow it.

Items	Description	Operation	Design Value	Unit
BD.1	Border layer enclosure of layout patterns (all chip design)	≥	0.37	um
BD.2	Border layer enclosure of DNW	≥	6	um
BD.3	BORDER layer must enclose all chip layout pattern			

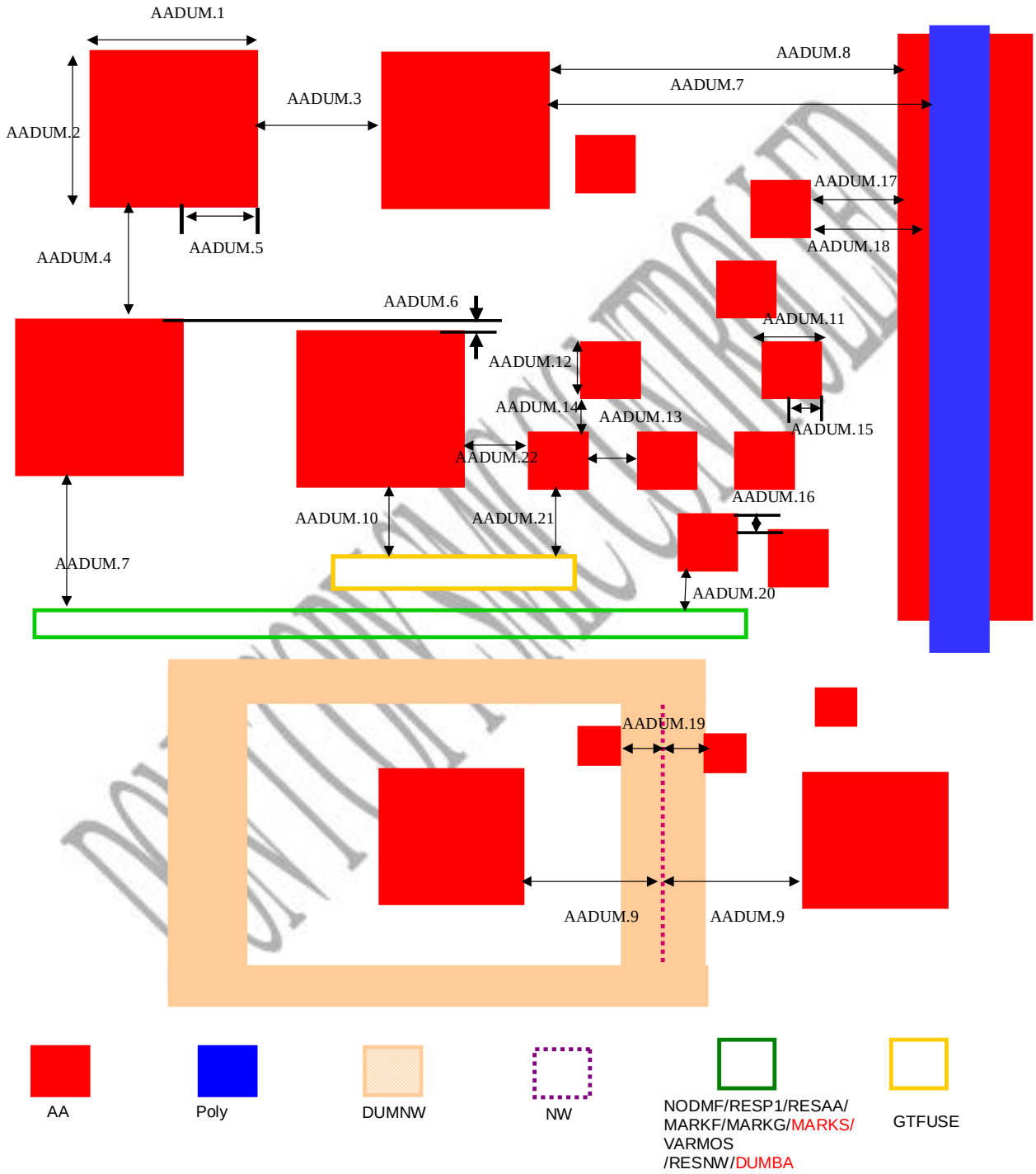
7.2.32 Dummy Insertion Rules and Checking Rules

7.2.32.1 AA Dummy pattern insertion rules

There are two sets of dummy patterns, set-1 with larger pattern dimension to fill open areas, while set-2 having smaller pattern dimension and spaces to fill narrow areas.

Rules number	Description	Operation	Design Value	Unit
AADUM rule (for Set-1):				
AADUM.1	Dummy AA1 width	=	3.5	um
AADUM.2	Dummy AA1 height	=	3.00	um
AADUM.3	Horizontal space between two Dummy AA1s	=	2.40	um
AADUM.4	Vertical space between two Dummy AA1s	=	2.00	um
AADUM.5	Displacement between adjacent dummy AA1 in horizontal direction	=	1.75	um
AADUM.6	Displacement between adjacent dummy AA1 in vertical direction	=	0.00	um
AADUM.7	Space between dummy AA1 and active AA/ DUMBA/ NODMF/ RESAA/ RESNW/ RESP1/ MARKF/ MARKG/ MARKS/ VARMOS	≥	7.00	um
AADUM.8	Space between dummy AA1 and poly	≥	7.00	um
AADUM.9	Space between dummy AA1 and NW edge (DUMNW)	≥	7.00	um
AADUM.10	Space between dummy AA1 and GTFUSE	≥	7.00	um
AADum rule (for Set-2):				
AADUM.11	Dummy AA2 width	=	0.42	um
AADUM.12	Dummy AA2 height	=	0.46	um
AADUM.13	Horizontal space between two Dummy AA2s	=	0.33	um
AADUM.14	Vertical space between two Dummy AA2s	=	0.37	um
AADUM.15	Displacement between adjacent dummy AA2 in horizontal direction	=	0.21	um
AADUM.16	Displacement between adjacent dummy AA2 in vertical direction	=	0.00	um

AADUM.17	Space between dummy AA2 and active AA	≥	1.50	um
AADUM.18	Space between dummy AA2 and poly	≥	1.50	um
AADUM.19	Space between dummy AA2 and NW edge (DUMNW)	≥	0.30	um
AADUM.20	Space between dummy AA2 and DUMBA/NODMF/ RESAA/RESNW/RESP1/MARKF/MARKG/MARKS/ VARMOS layers	≥	0.40	um
AADUM.21	Space between dummy AA2 and GTFUSE	≥	3.20	um
AADUM.22	Space between dummy AA2 and Dummy AA1	≥	0.40	um
General Rules				
AADUM.23	No dummy pattern insertion is allowed inside an area that is covered by DUMBA/ NODMF/RESAA/ RESNW /RESP1//MARKF/MARKG/MARKS/VARMOS layers			
AADUM.24	Space between dummy AA and chip edge	≥	1.50	um
AADUM.25	To check AA density with window size 50umX50um with step 25um before filling dummy AA. Not need to fill dummy AA, if AA pattern density is > 60% in each 50umX50um area.			
AADUM.26	No dummy AA is allowed to straddle on a boundary of NW			
AADUM.27	If dummy AA auto-filling is not needed in the inductor or other sensitive areas, designer need use DUMBA layer for dummy block.			



7.2.32.2 AA Dummy pattern check rules

Suggest following SMIC AA dummy insertion rules for dummy filling. Dummy AA1 pattern density is 35.6%, Dummy AA2 pattern density is 31%.
For non-SMIC AA dummy patterns (data type 1), SMIC data process will follow below table for DRC checking.

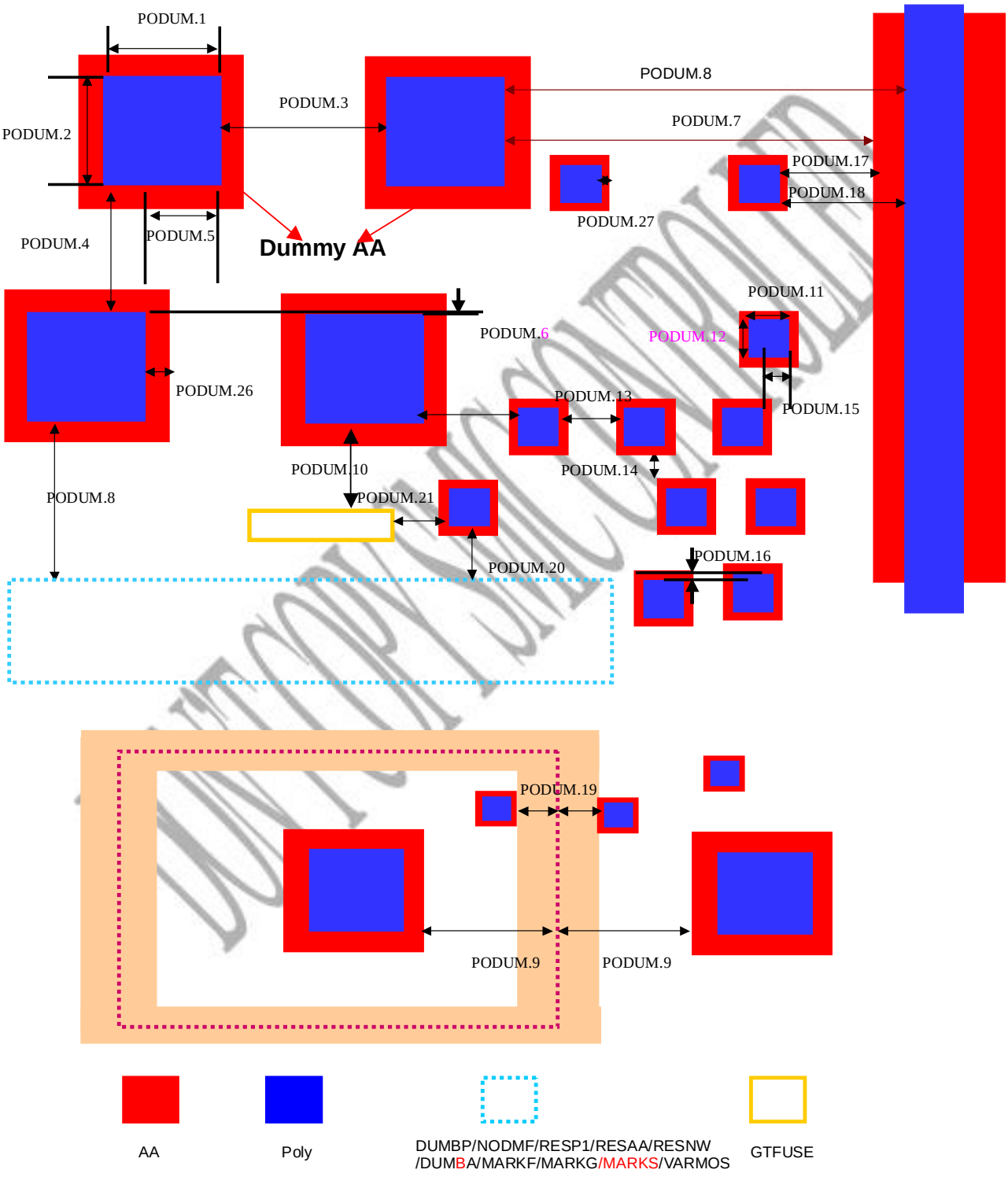
Rules number	Description	Operation	Design Value	Unit
AADUMCK.1	AA dummy can not violate AA.1, AA.3a, AA.3b, AA.8, AADUM.19, AADUM.21 and AADUM.26			
AADUMCK.2	Space between AA dummy and AA main patterns can not violate AA.3a and AA.3b.			
AADUMCK.3	Space between AA dummy and poly main pattern can not violate GT.4.			
AADUMCK.4	AA dummy patterns cannot touch AA main patterns.			
AADUMCK.5	No AA dummy patterns are allowed inside RESAA/RESNW/RESP1/VARMOS/MARKG/MARKF/MARKS covered areas.			
AADUMCK.6	Space between dummy AA and RESAA/RESNW/ RESP1/VARMOS/MARKG/MARKF/MARKS layers	≥	0.4	um

7.2.32.3 Poly Dummy pattern insertion rules

There are two sets of poly dummy patterns, set-1 with larger pattern dimension to fill open areas, while set-2 having smaller pattern dimension and spaces to fill narrow areas.

Rule numbers	Description	Operation	Design Value	Unit
PODUM rule (for set1):				
PODUM.1	Dummy poly1 width	=	3.10	um
PODUM.2	Dummy poly1 height	=	2.60	um
PODUM.3	Horizontal space between two Dummy poly1s	=	2.80	um
PODUM.4	Vertical space between two Dummy poly1s	=	2.40	um
PODUM.5	Displacement between adjacent dummy poly1 in horizontal direction.	=	1.75	um
PODUM.6	Displacement between adjacent dummy poly1 in vertical direction	=	0.00	um
PODUM.7	Space between dummy poly1 and active AA	≥	7.00	um
PODUM.8	Space between dummy poly1 and poly/ DUMBA/ DUMBP/ NODMF/RESP1/RESAA/RESNW/MARKF/MARKG/ MARKS/VARMOS	≥	7.00	um
PODUM.9	Space between dummy poly1 and NW edge (DUMNW).	≥	7.00	um
PODUM.10	Space between dummy poly1 and GTFUSE	≥	7.00	um
PODUM rule (for set2):				
PODUM.11	Dummy poly2 width	=	0.34	um
PODUM.12	Dummy poly2 height	=	0.38	um
PODUM.13	Horizontal space between two Dummy poly2s	=	0.41	um
PODUM.14	Vertical space between two Dummy poly2s	=	0.45	um
PODUM.15	Displacement between adjacent dummy poly2 in horizontal direction.	=	0.21	um
PODUM.16	Displacement between adjacent dummy poly2 in vertical direction	=	0.00	um

PODUM.17	Space between dummy poly2 and active AA	≥	0.50	um
PODUM.18	Space between dummy poly2 and poly	≥	0.50	um
PODUM.19	Space between dummy poly2 and NW edge (DUMNW).	≥	0.34	um
PODUM.20	Space between dummy poly2 and DUMBA/ DUMBP/ NODMF/ RESP1/ RESAA/ RESNW/MARKF/MARKG/ MARKS/VARMOS	≥	0.44	um
PODUM.21	Space between dummy poly2 and GTFUSE	≥	3.24	um
PODUM.22	Space between poly2 and poly1	≥	0.64	um
General Rules				
PODUM.23	No dummy pattern insertion is allowed inside the area that is covered by DUMBA/ DUMBP/ NODMF/ RESAA/ RESNW/ RESP1/MARKF/MARKG/MARKS/VARMOS layers			
PODUM.24	No dummy poly pattern is allowed to exist above AA circuit pattern (not include dummy AA)			
PODUM.25	Poly dummy (poly1, poly2) is either adding overlap with AA dummy (AA1, AA2) or on STI			
PODUM.26	AA1 extension of poly1	=	0.20	um
PODUM.27	AA2 extension of poly2	=	0.04	um
PODUM.28	Space between dummy poly and chip edge	≥	1.5	um
PODUM.29	To check Poly density with window size 50umX50um with step 25um before filling dummy Poly. If Poly pattern density is > 50% in each 50umX50um area, it doesn't need to fill dummy Poly.			
PODUM.30	No dummy poly is allowed to straddle on a boundary of NW			
PODUM.31	If dummy GT auto-filling is not needed in an inductor or other sensitive areas, designer needs use DUMBP layer for dummy blockage.			



7.2.32.4 Poly Dummy pattern check rules

Suggest following SMIC poly dummy insertion rules for dummy filling. Dummy Poly1 pattern density is 27.3%, Dummy Poly2 pattern density is 20.7%.
For non-SMIC poly dummy patterns (data type 1), SMIC data process will follow below table for DRC checking.

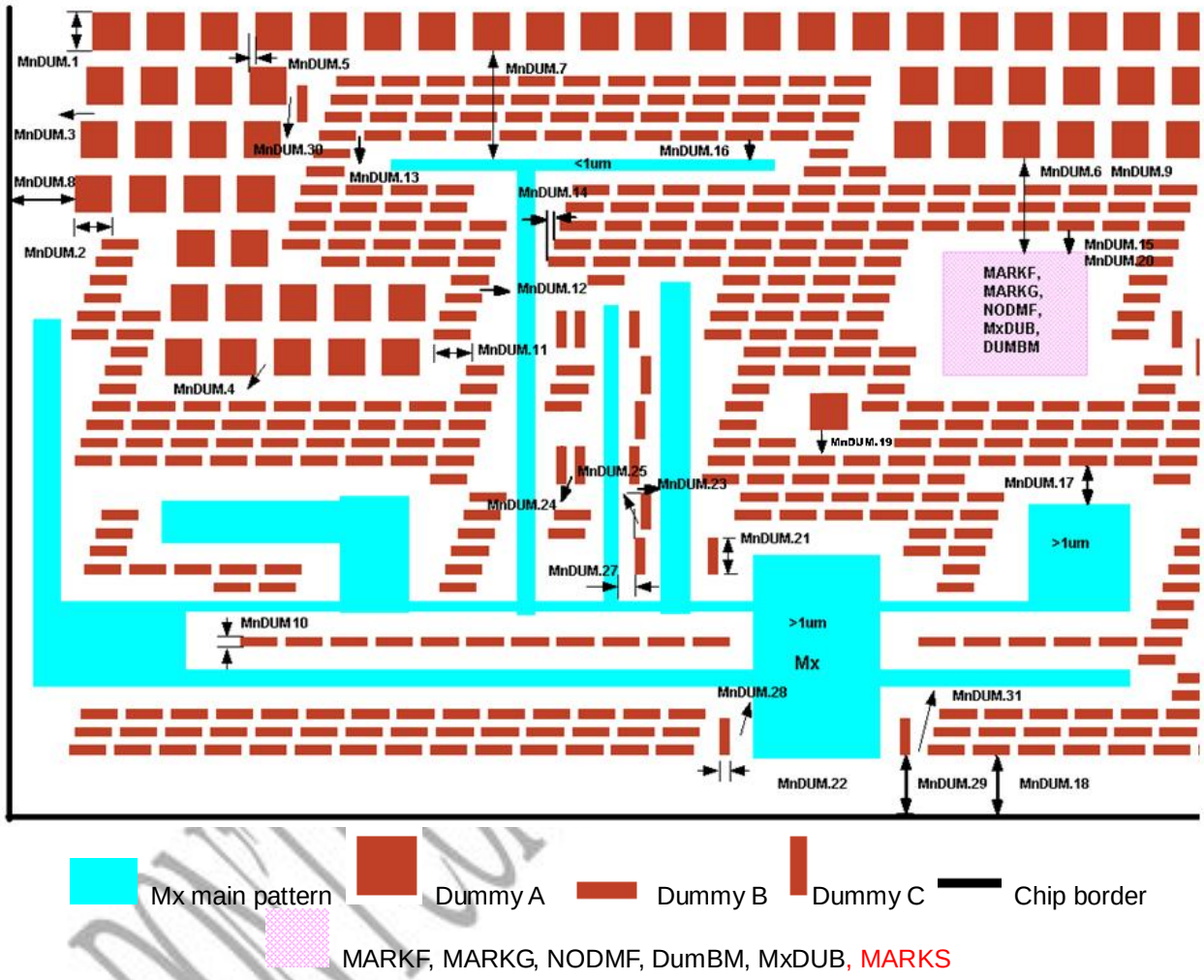
Rule numbers	Description	Operation	Design Value	Unit
GTDUMCK.1	Poly dummy can not violate GT.2, GT.3a, GT.3b, PODUM.21, PODUM.24 and PODUM.25			
GTDUMCK.2	Space between poly dummy and poly main pattern can not violate GT.3a and GT.3b.			
GTDUMCK.3	Space between poly dummy and AA main pattern can not violate GT.4.			
GTDUMCK.4	Poly dummy patterns cannot touch GT main patterns.			
GTDUMCK.5	No dummy patterns are allowed inside RESAA/RESNW/RESP1/VARMOS/MARKG/ MARKF/MARKS covered areas.			
GTDUMCK.6	Space between dummy poly and RESP1/ RESAA/ RESNW/VARMOS/MARKG/MARKF/MARKS	≥	0.44	um

7.2.32.5 Mn (n=1~8) Metal dummy pattern insertion rules

RULE No.	Descriptions	Operation	Design Value	Unit
DUMMY A: DATA TYPE 1 (dummy density: 44%)				
MnDUM.1	MnDUM line width	=	1.20	um
MnDUM.2	MnDUM line length	=	1.20	um
MnDUM.3	Vertical space between MnDUM patterns	=	0.60	um
MnDUM.4	Horizontal space between MnDUM patterns	=	0.60	um
MnDUM.5	Displacement between adjacent MnDUM lines	=	0.20	um
MnDUM.6	Space between dummy pattern and the edge of Mn block layers （MxDUB, DUMBM, NODMF）	≥	3.00	um
MnDUM.7	Space between dummy pattern and the edge of Mn pattern	≥	3.00	um
MnDUM.8	Chip border enclosure of dummy pattern	≥	2.00	um
MnDUM.9	Space between dummy pattern and MARKF/ MARKG/MARKS	≥	0.50	um
DUMMY B: DATA TYPE 1 (Dummy density: 40%)				
MnDUM.10	MnDUM line width	=	0.16	um
MnDUM.11	MnDUM line length	=	1.20	um
MnDUM.12	Vertical space between MnDUM patterns	=	0.17	um
MnDUM.13	Horizontal space between MnDUM patterns	=	0.25	um
MnDUM.14	Displacement between adjacent MnDUM lines	=	0.10	um
MnDUM.15	Space between dummy pattern and the edge of Mn block layers （MxDUB, DUMBM, NODMF）	≥	0.70	um
MnDUM.16	Space between dummy pattern and Mn pattern with width <=1um	≥	0.17	um
MnDUM.17	Space between dummy pattern and Mn pattern with width >1um	≥	0.70	um
MnDUM.18	Chip border enclosure of dummy pattern	≥	2.00	um

MnDUM.19	Space between dummy A and dummy B	≥	0.30	um
MnDUM.20	Space between dummy pattern and MARKF/MARKG /MARKS	≥	0.5	um
DUMMY C: DATA TYPE 1 (Dummy density: 40%)				
MnDUM.21	MnDUM line width	=	1.2	um
MnDUM.22	MnDUM line length	=	0.16	um
MnDUM.23	Vertical space between MnDUM patterns	=	0.25	um
MnDUM.24	Horizontal space between MnDUM patterns	=	0.17	um
MnDUM.25	Displacement between adjacent MnDUM lines	=	0.10	um
MnDUM.26	Space between dummy pattern and the edge of Mn dummy block layers（MxDUB, DUMBM, NODMF）	≥	0.70	um
MnDUM.27	Space between dummy pattern and Mn line with width <=1um	≥	0.17	Um
MnDUM.28	Space between dummy pattern and Mn line with width >1um	≥	0.7	Um
MnDUM.29	Chip border enclosure of dummy pattern	≥	2.0	Um
MnDUM.30	Space between dummy A and dummy C	≥	0.3	Um
MnDUM.31	Space between dummy B and dummy C	≥	0.3	Um
MnDUM.32	Space between dummy pattern and MARKF/MARKG/MARKS	≥	0.5	Um
General rules				
MnDUM.33	Need check metal density first before dummy filling. No additional dummy filling is needed if Mn density in 25umX25um window with step size 25um is greater than 65%.			
MnDUM.34	A, B and C types of dummy patterns are considered along with main patterns for OPC engineering			
MnDUM.35	MARKF, MARKG, MARKS covered areas will be automatically excluded for dummy filling. For other design specific areas (LOGO, INDMY, MOMDMY covered areas etc.), where designer would not like to place dummy patterns automatically, he or she should draw dummy block layers accordingly.			

MnDUM.36	Mn+1DUM patterns need to be on perpendicular directions from the adjacent dummy layer MnDUM			
MnDUM.37	The set of the above metal dummy rules (DUMMY A type, DUMMY B, and DUMMY C type) can be applied to chip area. However, only DUMMY A type is applied to scribe lane area			
MnDUM.38	Mn dummy metal can not be interacted with Mn metal design patterns.			
MnDUM.39	No metal dummy pattern insertions are allowed inside dummy block layers covered areas, including DUMBM, NODMF.			
MnDUM.40	No Mn (n=1~8) dummy pattern insertions are allowed inside MnDUB (n=1~10) covered areas			



7.2.32.6 Mn (n=1~8) Metal Dummy pattern check rules

Please follow SMIC's Mn dummy insertion rules for dummy insertion. If designers use their own dummy insertion patterns or methods, all metals (effective circuits plus dummy) must pass SMIC DRC.

All non-SMIC dummy patterns will be considered along with main patterns for OPC engineering.

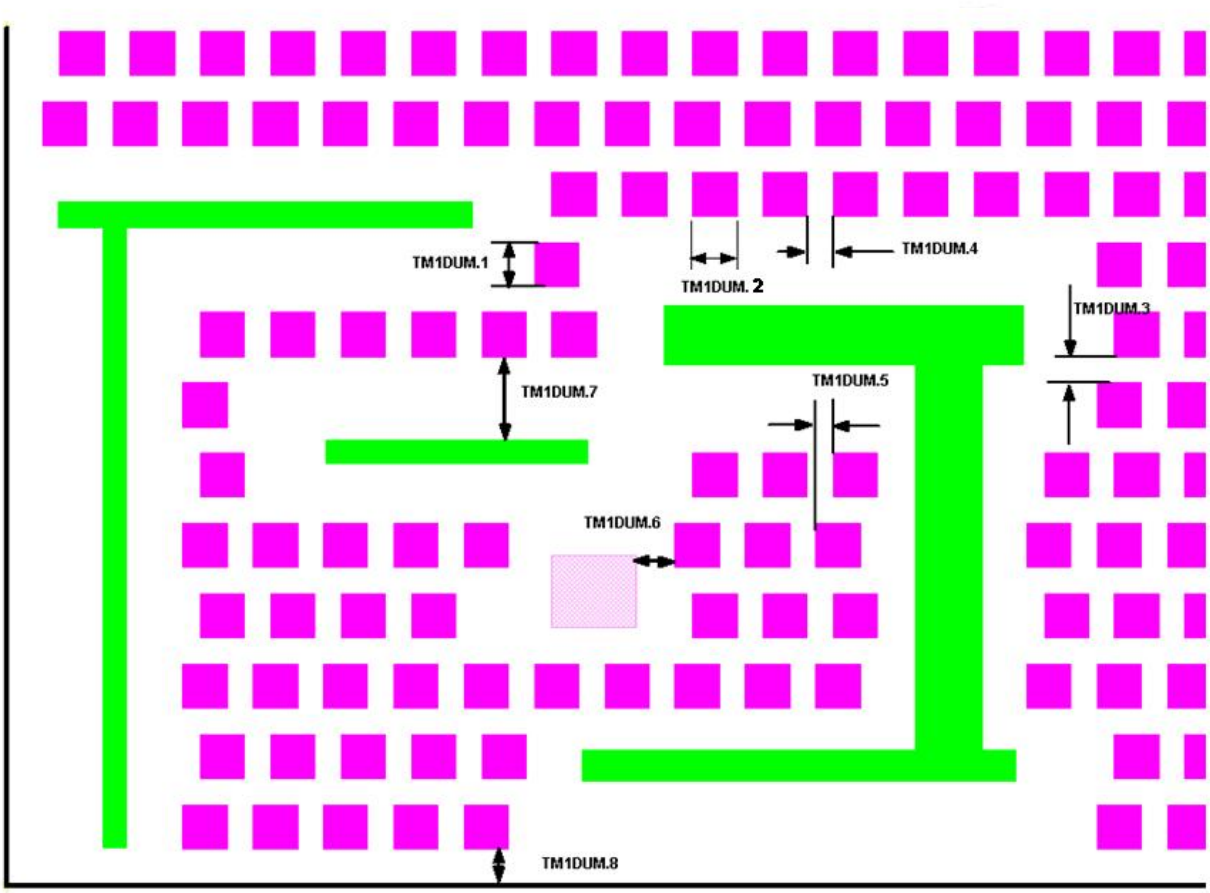
Rule numbers	Description
MnDUMCK.1	M1 dummy patterns must not violate M1.1, M1.2a,M1.2b,M1.2c M1.3, M1.4, M1.5
MnDUMCK.2	Space between M1 dummy patterns and M1 main patterns must not violate M1.2a, M1.2b and M1.2c.
MnDUMCK.3	Mn dummy patterns must not violate Mn.1, Mn.2a, Mn.2b, Mn.2c, Mn.3, Mn.4, Mn.5 (n=2~8)
MnDUMCK.4	Space between Mn dummy patterns and Mn main patterns must not violate Mn.2a, Mn.2b and Mn.2c. (n=2~8)
MnDUMCK.5	Mn dummy metal can not be interacted with Mn metal design patterns. (n=1~8)
MnDUMCK.6	Mn (n=1~8) dummy patterns are not allowed inside MARKF, MARKG and MARKS covered areas.

7.2.32.7 TM1/STM1 Dummy pattern insertion rules

RULE NO.	Description	Operation	Design Value	Unit
For TM1DUM (4X option):				
TM1DUM.1	TM1DUM line width	=	1.6	um
TM1DUM.2	TM1DUM line length	=	1.6	um
TM1DUM.3	Vertical space between TM1DUM patterns	=	0.8	um
TM1DUM.4	Horizontal space between TM1DUM patterns	=	0.8	um
TM1DUM.5	Displacement between adjacent TM1DUM lines	=	0.5	um
TM1DUM.6	Space between dummy pattern and the edge of TM1 dummy block layers (TM1DUB, DUMBM and NODMF)	≥	2.0	um
TM1DUM.7	Space between dummy pattern and the edge of TM1 pattern	≥	2.0	um
TM1DUM.8	Chip border enclosure of dummy patterns	≥	2.0	um
TM1DUM.9	Space between dummy pattern and MARKF/ MARKG/MARKS	≥	2.0	um
TM1DUM.10	This metal dummy rule also applies to chip area and empty scribe lane area.			
TM1DUM.11	Need check metal density first before dummy insertion. No additional dummy insertion is needed if Mn density in 25umX25um window with step size 25um is larger than 65%.			
TM1DUM.12	All dummy pattern need not OPC			
TM1DUM.13	MARKF, MARKG, MARKS covered areas will be automatically excluded for dummy insertion. For other design specific areas (LOGO, INDMY, MOMDMY covered areas etc.), where designer would not like place dummy automatically, he or she should draw dummy block layer.			
TM1DUM.14	TM1 dummy metal can not interact with TM1 metal design patterns.			

TM1DUM.15	TM1 dummy pattern insertion is not allowed inside dummy block layers (TM1DUB, DUMBM and NODMF)			
For STM1DUM (2X option):				
STM1DUM.1	STM1DUM line width	=	1.6	um
STM1DUM.2	STM1DUM line length	=	1.6	um
STM1DUM.3	Vertical space between STM1DUM patterns	=	0.8	um
STM1DUM.4	Horizontal space between STM1DUM patterns	=	0.8	um
STM1DUM.5	Displacement between adjacent STM1DUM lines	=	0.5	um
STM1DUM.6	Space between dummy pattern and the edge of STM1 dummy block layers (STM1DUB, DUMBM and NODMF)	≥	2.0	um
STM1DUM.7	Space between dummy pattern and the edge of STM1 pattern	≥	2.0	um
STM1DUM.8	Chip border enclosure of dummy pattern	≥	2.0	um
STM1DUM.9	Space between dummy pattern and MARKF/ MARKG/MARKS	≥	2.0	um
STM1DUM.10	This metal dummy rule also applies to chip area and empty scribe lane area.			
STM1DUM.11	Need check metal density first before dummy insertion. No additional dummy insertion is needed if Mn density in 25umX25um window with step size 25um is greater than 65%.			
STM1DUM.12	All dummy pattern need not OPC			
STM1DUM.13	MARKF, MARKG, MARKS covered areas will be automatically excluded for dummy insertion. For other design specific areas (LOGO, INDMY, MOMDMY covered areas etc.), where designer would not like place dummy automatically, he or she should draw dummy block layer.			
STM1DUM.14	STM1 dummy metal can not interact with STM1 metal design patterns.			
STM1DUM.15	STM1 dummy pattern insertion is not allowed inside			

	dummy block layers (STM1DUB, DUMBM and NODMF)			



TM1/STM1 main patterns

TM1DUM/ STM1DUM

Chip border

MARKF, MARKG, MARKS, NODMF, TM1DUB/STM1DUB, DUMBM

7.2.32.8 TM1/STM1 Dummy pattern check rules

Please follow SMIC's TM1/STM1 dummy pattern insertion rules for dummy filling. If designers use their own dummy fill patterns or methods, all TM1s patterns (effective circuits plus dummy) must pass SMIC DRC.

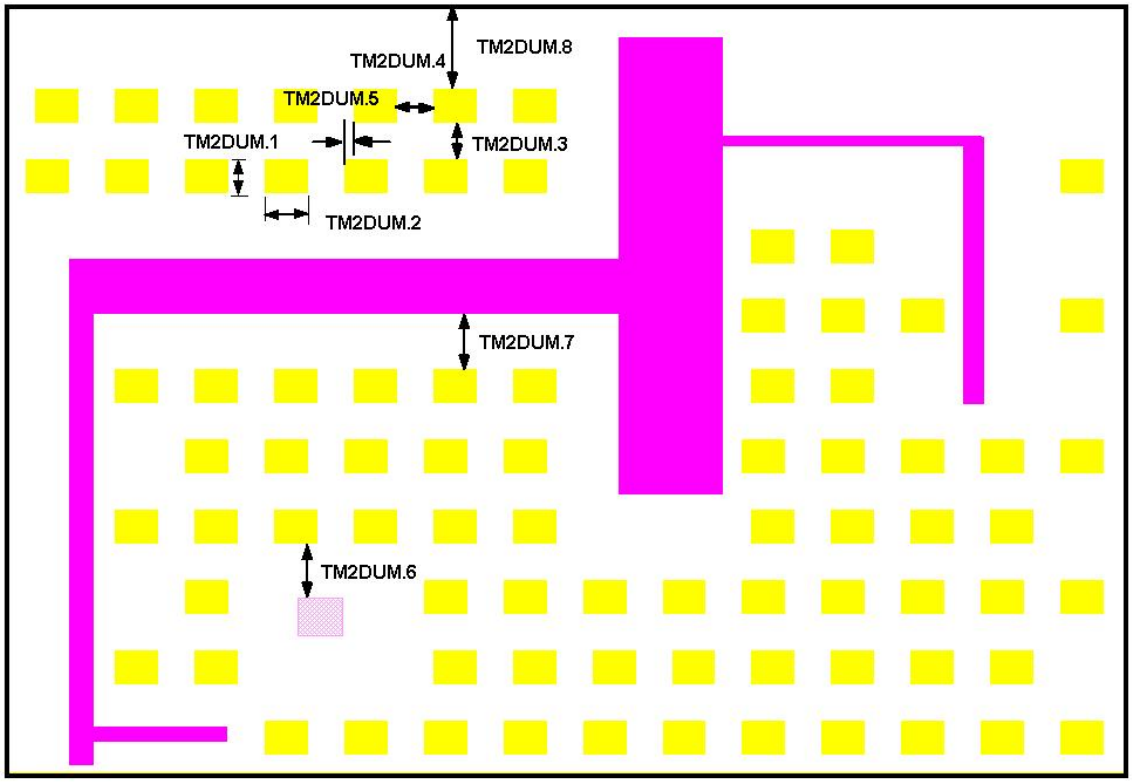
SMIC will consider non-SMIC TM1 dummy patterns (data type 1) as main patterns and follow below tables for DRC.

Rule numbers	Description
For TM1 (4X option)	
TM1DUMCK.1	TM1 dummy patterns must not violate TM1.1, TM1.2a, TM1.2b, TM1.3, TM1.4, TM1.5
TM1DUMCK.2	Space between TM1 dummy patterns and TM1 main patterns must not violate TM1.2a and TM1.2b.
TM1DUMCK.3	TM1 dummy metal can not interact with TM1 metal design patterns.
TM1DUMCK.4	No TM1 dummy patterns are allowed inside MARKG, MARKF and MARKS covered areas
For STM1 (2X option)	
STM1DUMCK.1	STM1 dummy patterns must not violate STM1.1, STM1.2a, STM1.2b, STM1.2c, STM1.2d, STM1.3, STM1.4, STM1.5 and STM1.7.
STM1DUMCK.2	Space between STM1 dummy patterns and STM1 main patterns must not violate STM1.2a, STM1.2b STM1.2c, STM1.2d and STM1.7.
STM1DUMCK.3	STM1 dummy metal can not interact with STM1 metal design patterns.
STM1DUMCK.4	No STM1 dummy patterns are allowed inside MARKG, MARKF and MARKS covered areas

7.2.32.9 TM2/MTT2/STM2 Dummy pattern insertion rules

Rule number	Description	Operation	Design Value	Unit
For TM2DUM (4X option TM2 and MMT2 option)				
TM2DUM.1	TM2DUM line width	=	3.5	um
TM2DUM.2	TM2DUM line length	=	3.5	um
TM2DUM.3	Vertical space between TM2DUM patterns	=	3.0	um
TM2DUM.4	Horizontal space between TM2DUM patterns	=	3.0	um
TM2DUM.5	Displacement between adjacent TM2DUM lines	=	1.0	um
TM2DUM.6	Space between dummy pattern and the edge of TM2 dummy block layers (TM2DUB, DUMBM and NODMF)	≥	2.0	um
TM2DUM.7	Space between dummy pattern and the edge of TM2/MTT2 pattern	≥	2.0	um
TM2DUM.8	Chip border enclosure of dummy pattern	≥	2.0	um
TM2DUM.9	Space between dummy pattern and MARKF/ MARKG/MARKS	≥	2.0	um
TM2DUM.10	For TM2 (4X option) design, this metal dummy rule also applies to chip area and empty scribe lane area. But if MTT2 is used as TM2, no dummy pattern insertion is allowed on the scribe lane area.			
TM2DUM.11	Need check metal density first before dummy insertion. No additional dummy insertion is needed if TM2/MTT2 density in 100um X 100um window with step size 100um is greater than 35%.			
TM2DUM.12	All dummy pattern need not OPC			
TM2DUM.13	MARKF, MARKG, MARKS covered areas will be automatically excluded for dummy insertion. For other design specific areas (LOGO, INDMY, MOMDMY covered areas etc.), where designer would not like place dummy automatically, he or she should draw dummy block layer.			
TM2DUM.14	TM2 dummy metal can not interact with TM2 metal design patterns.			

TM2DUM.15	No TM2/MTT2 dummy pattern insertion is allowed inside DUMBM, NODMF and TM2DUB covered areas.			
For STM2DUM (2X option STM2):				
STM2DUM.1	STM2DUM line width	=	1.6	um
STM2DUM.2	STM2DUM line length	=	1.6	um
STM2DUM.3	Vertical space between STM2DUM patterns	=	0.8	um
STM2DUM.4	Horizontal space between STM2DUM patterns	=	0.8	um
STM2DUM.5	Displacement between adjacent STM2DUM lines	=	0.5	um
STM2DUM.6	Space between dummy pattern and the edge of STM2 dummy block layers (STM2DUB, DUMBM and NODMF)	≥	2.0	um
STM2DUM.7	Space between dummy pattern and the edge of STM2 pattern	≥	2.0	um
STM2DUM.8	Chip border enclosure of dummy pattern	≥	2.0	um
STM2DUM.9	Space between dummy pattern and MARKF/ MARKG/MARKS	≥	2.0	um
STM2DUM.20	This metal dummy rule also applies to chip area and empty scribe lane area.			
STM2DUM.22	Need check metal density first before dummy insertion. No additional dummy insertion is needed if Mn density in 25umX25um window with step size 25um is greater than 65%.			
STM2DUM.22	All dummy pattern need not OPC			
STM2DUM.23	MARKF, MARKG/MARKS covered areas will be automatically excluded for dummy filling. For other design specific areas (LOGO, INDMY, MOMDMY covered areas etc.), where designer would not like place dummy automatically, he or she should draw dummy block layer.			
STM2DUM.24	STM2 dummy metal can not interact with STM2 metal design patterns.			
STM2DUM.15	No STM2 dummy pattern insertion is allowed inside DUMBM, NODMF and STM2DUB covered areas.			



TM2 main patterns TM2DUM Chip border

NODMF, MARKF, MARKG, MARKS, DUMBM, TM2DUB

7.2.32.10 TM2/MTT2/STM2 Dummy pattern check rules

Please follow SMIC's TM2/STM2 dummy pattern insertion rules for dummy filling. SMIC TM2DUM density is designed as ~24.7% for both TM2 and MTT2 application and STM2DUM density is ~44% for 2X STM2. If designers use their own dummy fill patterns or methods, all TM2/STM2s patterns (effective circuits plus dummy) must pass SMIC DRC.

SMIC will consider non-SMIC TM2/STM2 dummy patterns (data type 1) as main patterns and follow below tables for DRC.

Rule number	Description
For TM2DUM (for 4X TM2 option)	
TM2DUMCK.1	TM2 dummy patterns must not violate TM2.1, TM2.2a, TM2.2b,TM2.3, TM2.4, TM2.5
TM2DUMCK.2	Space between TM2 dummy patterns and TM2 main patterns must not violate TM2.2a and TM2.2b.
TM2DUMCK.3	TM2 dummy metal can not interact with TM2 metal design patterns.
TM2DUMCK.4	No TM2 dummy patterns are allowed inside MARKG, MARKF and MARKS covered areas
For TM2DUM (for MTT2 option)	
TM2DUMCK.1	TM2 dummy patterns must not violate MTT2.1, MTT2.2a, MTT2.2b, MTT2.5, MTT2.6, MTT2.7, MTT2.8
TM2DUMCK.2	Space between TM2DUM patterns and MTT2 main patterns must not violate MTT2.2a and MTT2.2b
TM2DUMCK.3	TM2DUM metal can not interact with MTT2 metal design patterns.
TM2DUMCK.4	No TM2DUM patterns are allowed inside MARKG, MARKF and MARKS covered areas
For STM2DUM (for 2X STM2 option)	
STM2DUMCK.1	STM2 dummy patterns must not violate STM2.1, STM2.2a, STM2.2b, STM2.2c, STM2.2d, STM2.3, STM2.4, STM2.5, STM2.6
STM2DUMCK.2	Space between STM2 dummy patterns and STM2 main patterns must not violate STM2.2a, STM2.2b, STM2.2c and STM2.2d.
STM2DUMCK.3	STM2 dummy metal can not interact with STM2 metal design patterns.
STM2DUMCK.4	No STM2 dummy patterns are allowed inside MARKG, MARKF and MARKS covered areas

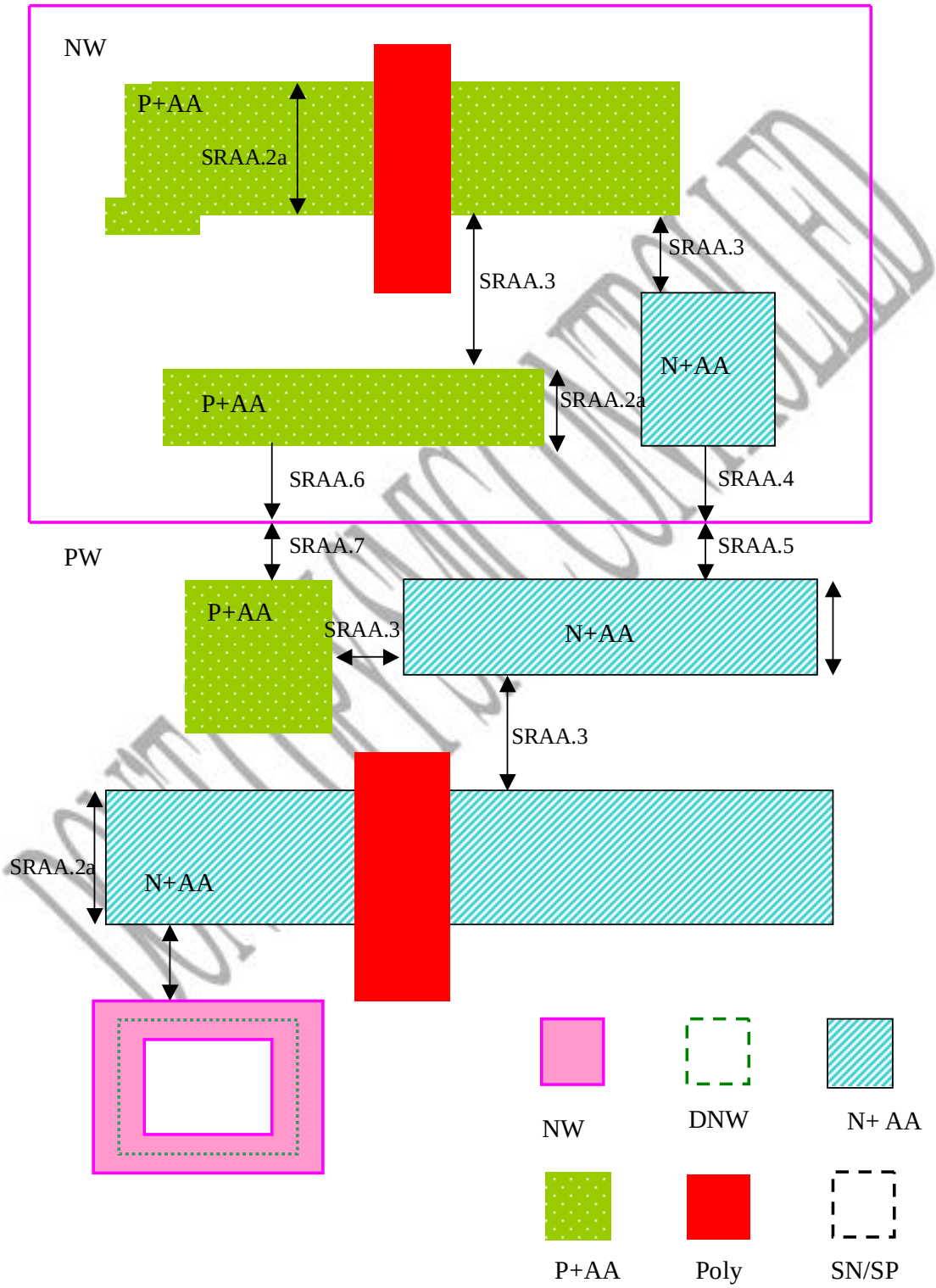
7.2.33 SRAM Rules Description

It is strongly recommended to use SMIC standard SRAM cells. If custom-designed SRAM cells are used, those SRAM cells must be enclosed by the INST layer (60;0). Edges of INST layer must be aligned with the boundary of SRAM cell arrays, which include bit cells, strap cells, edge cells and dummy cells of SRAM.
The area covered by INST should follow SRAM rule if these rule is redefined in SRAM rule.
The area covered by INST should follow the general rule also if this rule is not redefined in SRAM rule.

7.2.33.1 AA: Active area design rules

Besides the rules listed in below table, SRAM AA follow general rule 7.2.2 except AA.2a, AA.2b, AA.4, AA.5, AA.6, AA.7, AA.8.

Rules number	Description	Operation	General Rule Value	SRAM Design Value	Unit
SRAA.2a	Channel width for 1.0/1.2V NMOS/PMOS transistors	≥	0.11	0.085	um
SRAA.4	N+AA enclosed by NW	≥	0.12	0.055	um
SRAA.5	Space between NW and N+AA inside PW	≥	0.15	0.06	um
SRAA.6	P+AA enclosed by NW	≥	0.15	0.06	um
SRAA.7	Space between NW and P+AA inside PW	≥	0.12	0.11	um
SRAA.8	AA area	≥	0.038	0.029	um^2

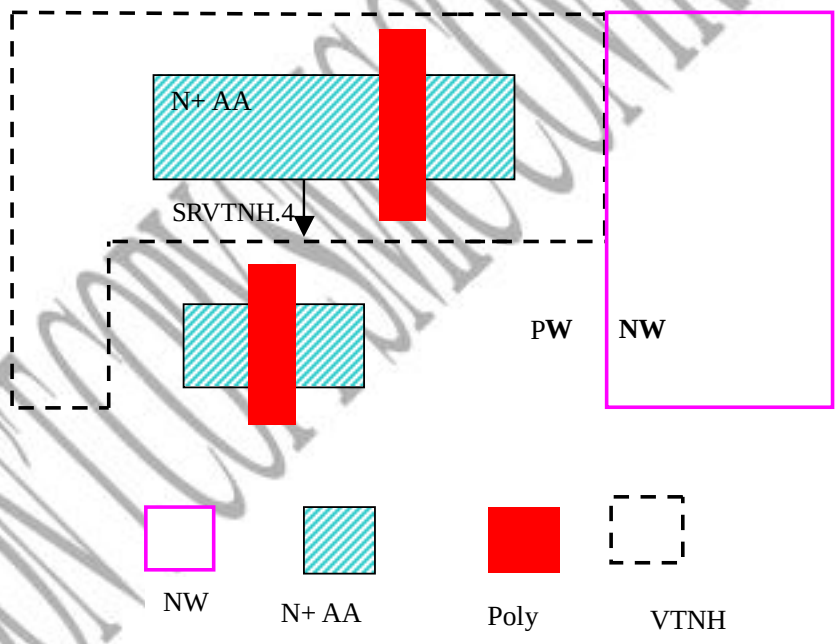


7.2.33.2 VTNH: High Vt NMOS design rules(optional)

VTNH is a drawn layer for Vt implant of high Vt MOS. VTNH is for 1.0/1.2V core high Vt device only.

Besides the rules listed in below table, SRAM VTNH follow general rule 7.2.5 except VTNH.4, VTNH.8.

Rules number	Description	Operation	General Rule Value	SRAM Design Value	Unit
SRVTNH.4	VTNH extension outside of NMOS AA along gate poly length direction.	≥	0.12	0.065	um
SRVTNH.8	VTNH area	≥	0.18	0.11	um^2

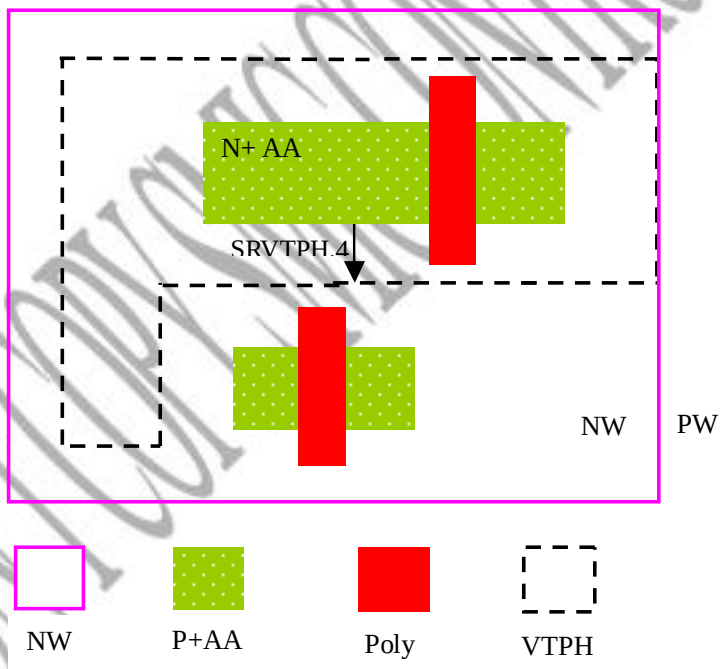


7.2.33.3 VTPH: High Vt PMOS design rules (optional)

VTPH is a drawn layer for VT implant of high Vt PMOS. VTPH is for 1.0/1.2V core high Vt device only.

Besides the rules listed in below table, SRAM VTPH follow general rule 7.2.5 except VTPH.4,VTPH.8.

Rules number	Description	Operation	General Rule Value	SRAM Design Value	Unit
SRVTPH.4	VTPH extension outside of PMOS AA along gate poly length direction.	≥	0.12	0.065	um
SRVTPH.8	VTPH area	≥	0.18	0.11	um^2



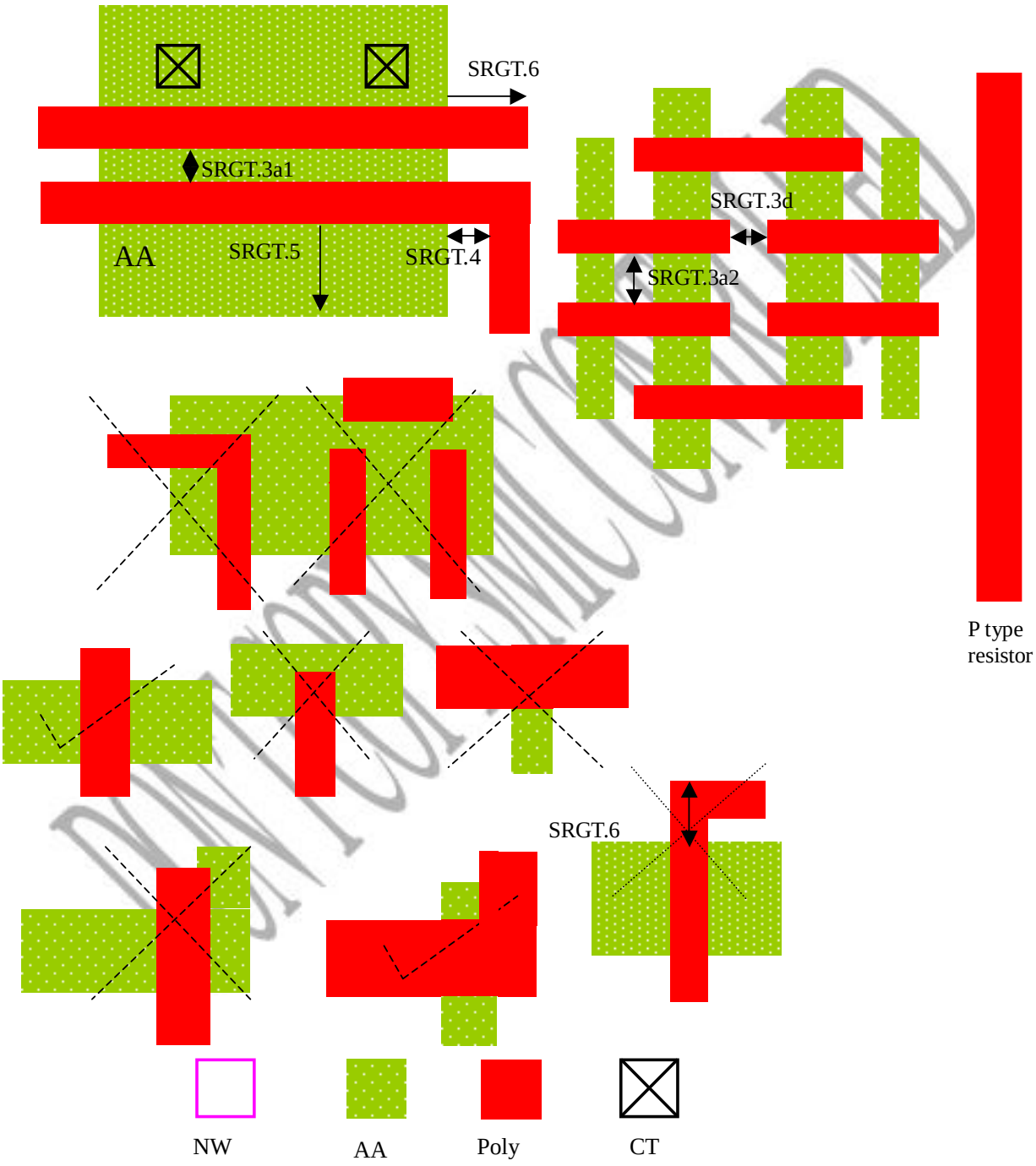
7.2.33.4 GT: Poly design rules

Besides the rules listed in below table, SRAM GT follow general rule 7.2.11 except GT.1b-1f, GT.3a, GT.3c, GT.3d, GT.4, GT.5, GT.6, GT.9-11.

Rules number	Description	Operation	General Rule Value	SRAM Design Value	Unit
SRGT.3a1	Space between GTs with the run length >0.12um	≥	0.12	0.12	um
SRGT.3a2	Space between GTs with the run length>0.025 and <=0.12um	≥	0.12	0.107	um
SRGT.3a3	Space between GTs with the run length <=0.025um	≥	0.12	0.06	um
SRGT.3c	Space between GTs on the same AA	≥	0.19	0.12	um
SRGT.3d	Space between poly line end to end	≥	N/A	0.105	um
SRGT.4a	Space between AA and GT on field oxide with the run length>0.04um	≥	0.05	0.05	um
SRGT.4b	Space between AA and GT on field oxide with the run length<=0.04um	≥	0.05	0.032	um
SRGT.5a	Extension of AA outside of GT with the run length >0.15um (not include dummy AA and dummy Poly)	≥	0.115	0.095	um
SRGT.5b	Extension of AA outside of GT with the run length>0.015um and <=0.04um (not include dummy AA and dummy Poly)	≥	0.115	0.077	um
SRGT.5c	Extension of AA outside of GT with the run length >0.04um and <=0.15um (not include dummy AA and dummy Poly)	≥	0.115	0.077	um
SRGT.6	Extension of gate poly end-cap outside of AA (not including dummy AA and dummy poly)	≥	0.14	0.068	um

Note:

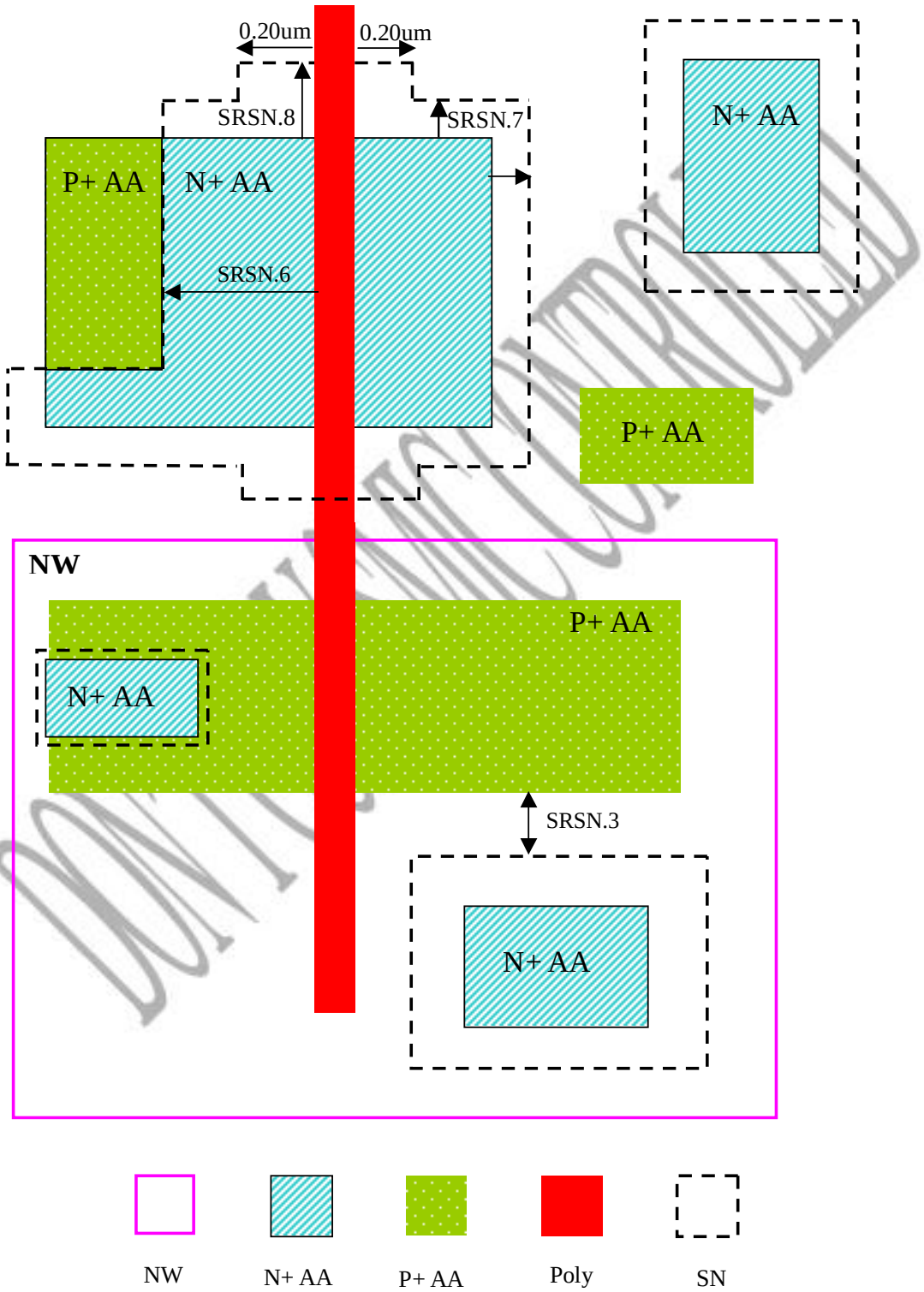
1. Poly line end to end pattern is excluded to check the rules with " run length".
2. Minimum space between GTs on AA is 0.13um, if the chip design is planned for 55nm technology.



7.2.33.5 SN: N+ S/D implantation design rules

Besides the rules listed in below table, SRAM SN follow general rule 7.2.16 except SN.3, SN.5,SN.6, SN.7, SN.8, SN.12.

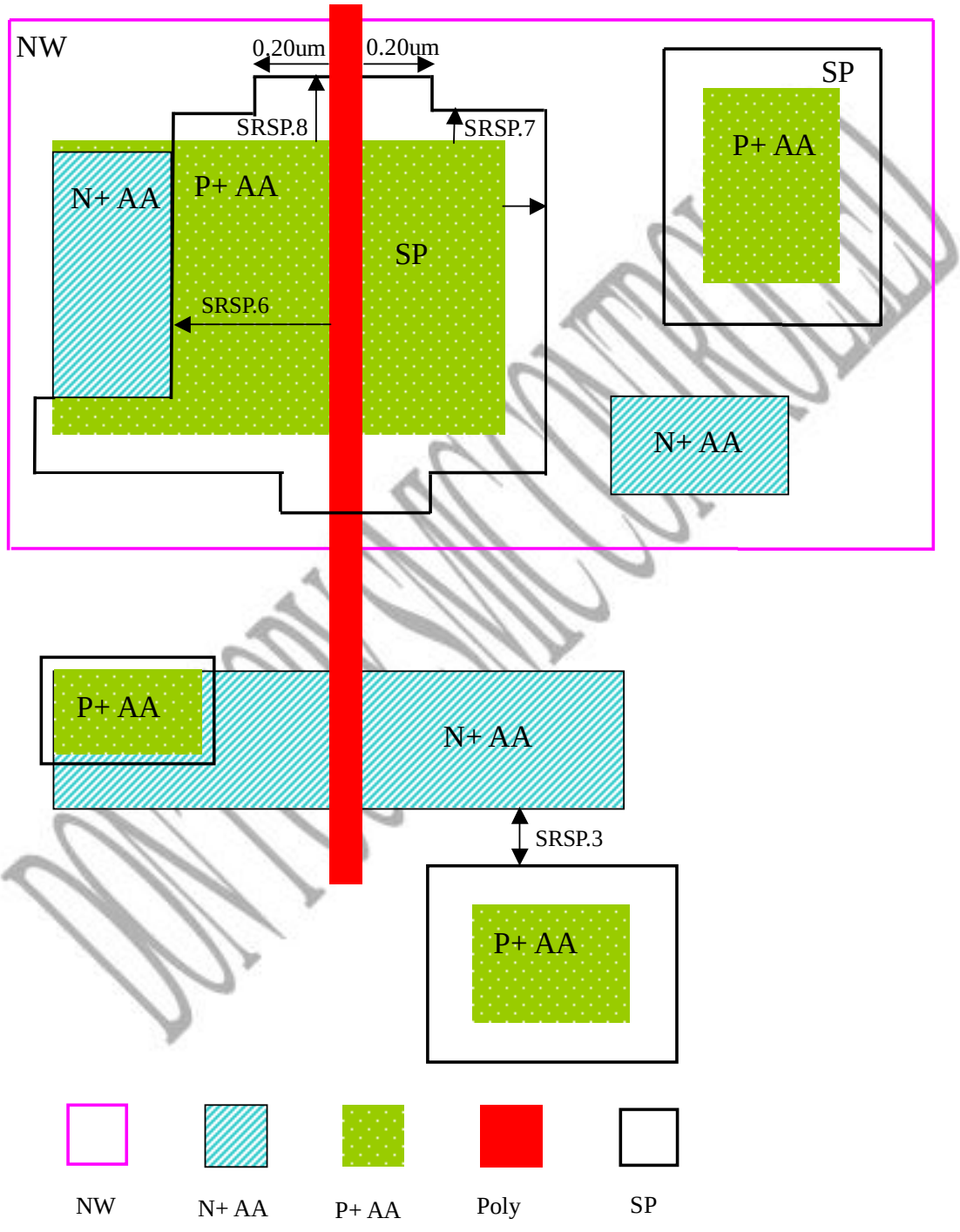
Rules number	Description	Operation	General Rule Value	SRAM Design Value	Unit
SRSN.3a	Space between SN and P+ AA inside NW with the run length >0.055um	≥	0.10	0.065	um
SRSN.3b	Space between SN and P+ AA inside NW with the run length<=0.055um	≥	0.10	0.06	um
SRSN.5	Space between SN and PMOS gate along source/drain direction.	≥	0.24	0.219	um
SRSN.6	SN extension outside of NMOS gate along source/drain direction..	≥	0.24	0.214	um
SRSN.7a	SN extension outside of NMOS AA along gate poly length direction with the run length >0.055um, if the distance to the related poly is > 0.20um	≥	0.12	0.065	um
SRSN.7b	SN extension outside of NMOS AA along gate poly length direction with the run length <=0.055um, if the distance to the related poly is > 0.20um	≥	0.12	0.06	um
SRSN.8a	SN extension outside of NMOS AA along gate poly length direction with the run length >0.055um, if the distance to the related poly is <= 0.20um	≥	0.16	0.065	um
SRSN.8b	SN extension outside of NMOS AA along gate poly length direction with the run length <=0.055um, if the distance to the related poly is <= 0.20um	≥	0.16	0.06	um



7.2.33.6 SP: P+ S/D implantation design rules

Besides the rules listed in below table, SRAM SP follow general rule 7.2.17 except SP.3, SP.5, SP.6, SP.7, SP.8,SP.12.

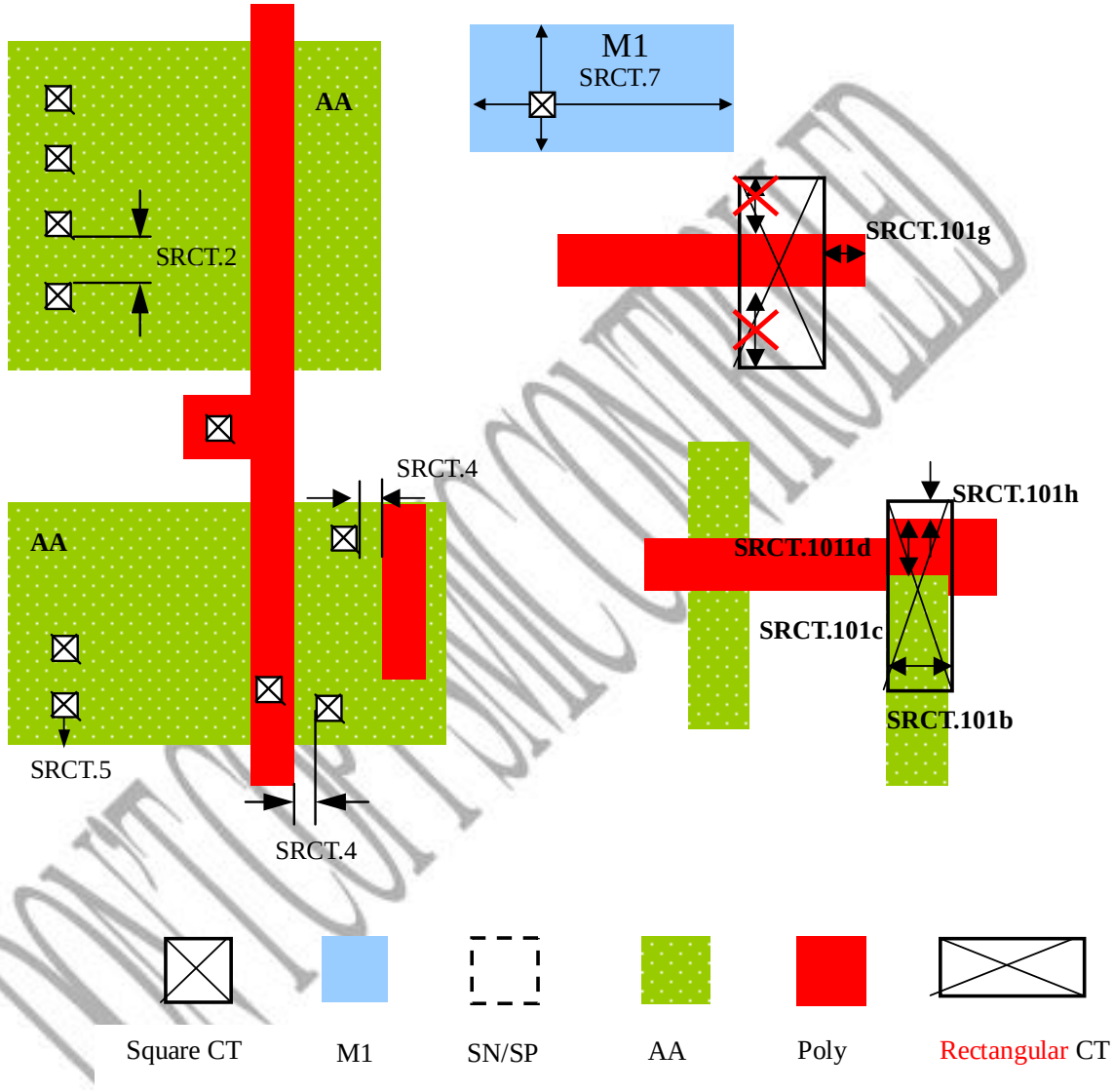
Rules number	Description	Operation	General Rule Value	SRAM Design Value	Unit
SRSP.3a	Space between SP and N+ AA inside PW with the run length>0.055um	≥	0.10	0.065	um
SRSP.3b	Space between SP and N+ AA inside PW with the run length<=0.055um	≥	0.10	0.06	um
SRSP.5	Space between SP and NMOS gate along source/drain direction.	≥	0.24	0.219	um
SRSP.6	SP extension outside of PMOS gate along source/drain direction.	≥	0.24	0.214	um
SRSP.7a	SP extension outside of PMOS AA along gate poly length direction with the run length >0.055μm, if the distance to the related poly is > 0.20um	≥	0.12	0.065	um
SRSP.7b	SP extension outside of PMOS AA along gate poly length direction with the run length <=0.055um, if the distance to the related poly is > 0.20μm	≥	0.12	0.06	um
SRSP.8a	SP extension outside of PMOA AA along gate poly length direction with the run length >0.055um, if the distance to the related poly is <=0.20um	≥	0.16	0.065	um
SRSP.8b	SP extension outside of PMOS AA along gate poly length direction with the run length <=0.055um, if the distance to the related poly is <= 0.20um	≥	0.16	0.06	um



7.2.33.7 CT: Contact design rules

Besides the rules listed in below table, SRAM CT follow general rule 7.2.19 except CT.2a, CT.4a, CT.4b, CT.5, CT.6, CT.7a, CT.7b, CT.9.

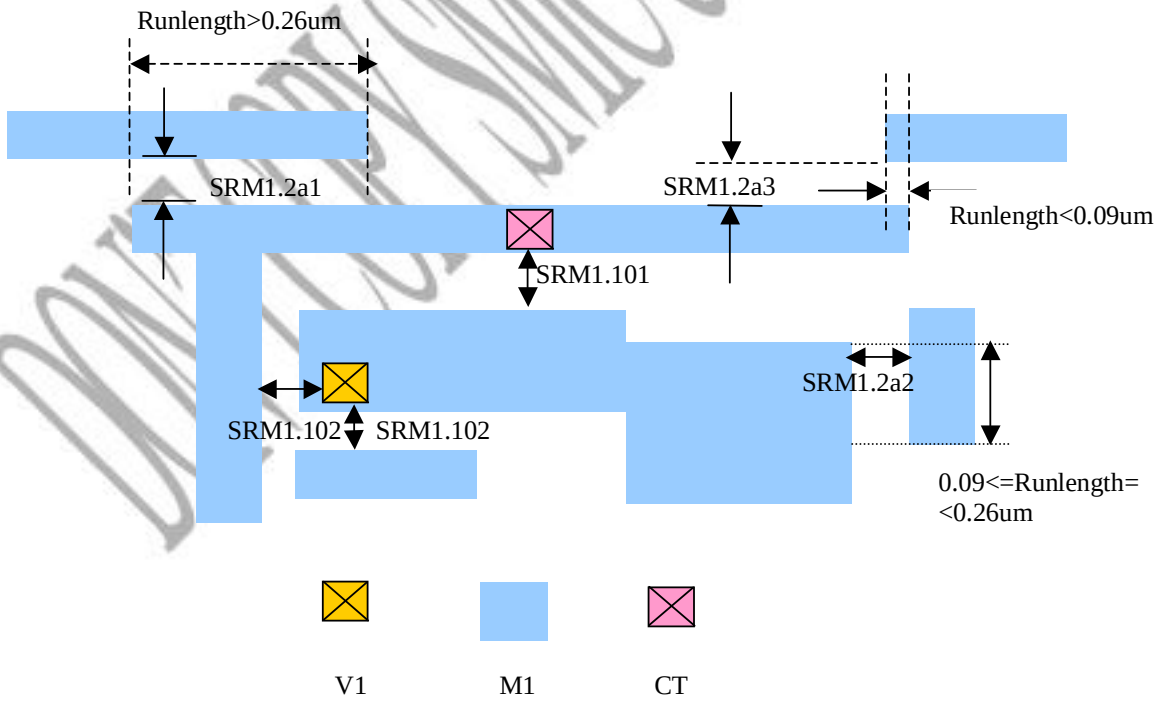
Rule number	Description	Operation	General Rule Value	SRAM Design Value	Unit
SRCT.2a1	Space between contacts(runlength>0.02µm)	≥	0.11	0.11	um
SRCT.2a2	Space between contacts(runlength<=0.02µm)	≥	0.11	0.09	um
SRCT.4a	Space between poly and contact on AA for 1.0V/1.2V	≥	0.05	0.038	um
SRCT.5	Square CT area enclosed by AA for CT landed on AA	≥	N/A	87%	
SRCT.6	CT enclosure by poly for CT landed on poly (exclude rectangular CT)	≥	0.01	0.00	um
SRCT.7	M1 enclosure of CT (four directions, exclude rectangular CT)	≥	N/A	0.00	um
SRCT.9	Square CT is not allowed to land on gate		N/A		
SRCT.101a[NC]	Rectangular CT connect AA and poly, and length is larger than width, which is in INST layer				
SRCT.101b	Rectangular CT width	≥	N/A	0.08	um
SRCT.101c	Rectangular CT overlap AA area	≥	N/A	0.01	um^2
SRCT.101d	Rectangular CT overlap poly	≥	N/A	0.073	um
SRCT.101e	Rectangular CT overlap poly area	≥	N/A	0.006	um^2
SRCT.101f	Rectangular CT overlap M1 area	≥	N/A	0.017	um^2
SRCT.101g	Poly extension outside of rectangular CT	≥	N/A	-0.008	um
SRCT.101h	Rectangular CT extension outside of poly (without AA overlap)	≤	N/A	0.02	um
SRCT.101i	M1 enclosure of rectangular CT	≥	N/A	-0.032	um



7.2.33.8 Metal 1 design rules

Besides the rules listed in below table, SRAM M1 should follow general rule 7.2.20 except M1.2a and M1.4.

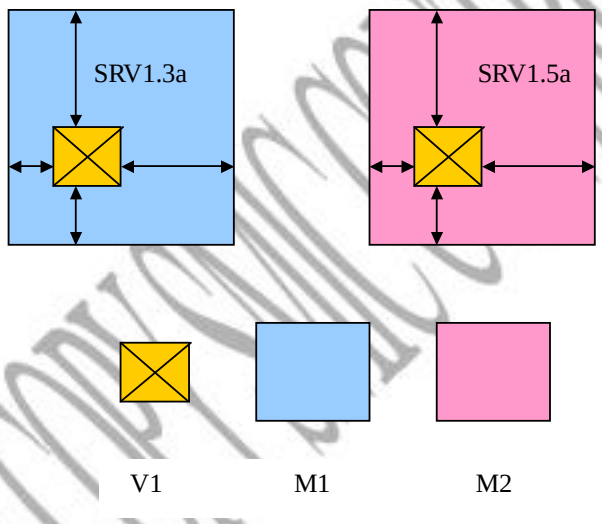
Rule Number	Description	Operation	General Rule Value	SRAM Design Value	Unit
SRM1.2a1	Space between M1s with the run length>0.26um	≥	0.09	0.09	um
SRM1.2a2	Space between two M1s with the run length >=0.09um and <=0.26um	≥	0.09	0.08	um
SRM1.2a3	Space between two M1s with the run length <0.09um	≥	0.09	0.075	um
SRM1.4	M1 area	≥	0.027	0.019	um^2
SRM1.101	Space between M1 and adjacent CT with run length>0	≥	N/A	0.082	um
SRM1.102	Space between M1 and adjacent V1 with run length>0.03um	≥	N/A	0.087	um



7.2.33.9 Via1 design rules

Besides the rules listed in below table, SRAM V1 should follow general rule 7.2.21 except V1.3a,V1.3b, V1.5a,V1.5b.

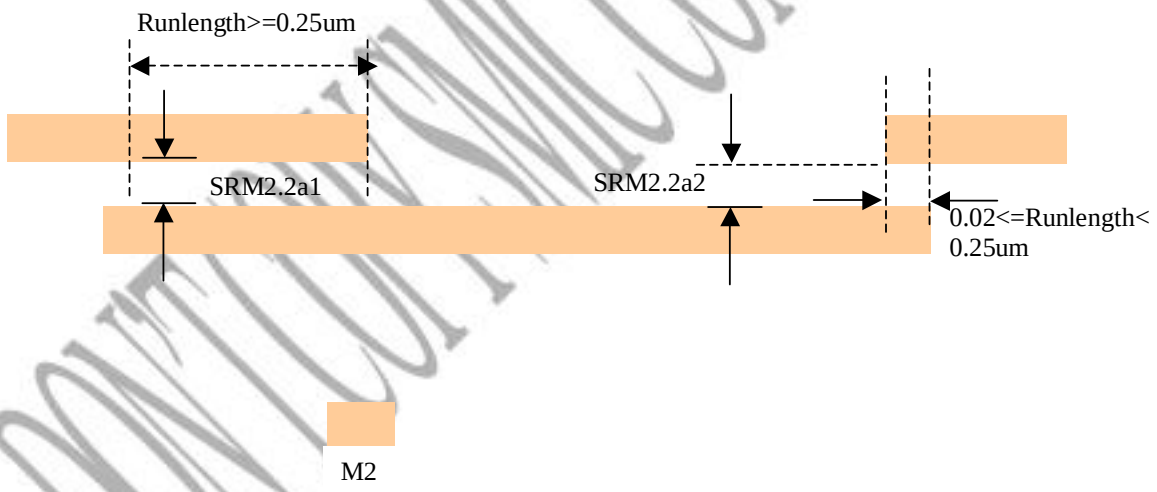
Rule number	Description	Operation	General Rule Value	SRAM Design Value	Unit
SRV1.3a	M1 enclosure of V1 (four directions)	≥	N/A	0.00	um
SRV1.5a	M2 enclosure of V1 (four directions)	≥	N/A	0.00	um



7.2.33.10 M2: Metal2 design rules

Besides the rules listed in below table, SRAM M2 should follow general rule 7.2.22 except Mn.2a, Mn.4.

Rule number	Description	Operation	General Rule Value	SRAM Design Value	Unit
SRM2.2a1	Space between two M2s with the run length >=0.25um	≥	0.10	0.10	um
SRM2.2a2	Space between two M2s with the run length>=0.02um and <0.25um	≥	0.10	0.095	um
SRM2.2a3	Space between two M2s with the run length<0.02um	≥	0.10	0.09	um
SRM2.4	M2 area	≥	0.035	0.03	um^2



7.2.34 Layout guidelines

It's stongly recommended to follow layout guidelines for design. And the guidelines require performing DRC runset, but DRC checking is not gated for them.Pls consult with integration engineers if customer has the problem.

SMIC spice model and PDK is based on SMIC design rule guidelines.

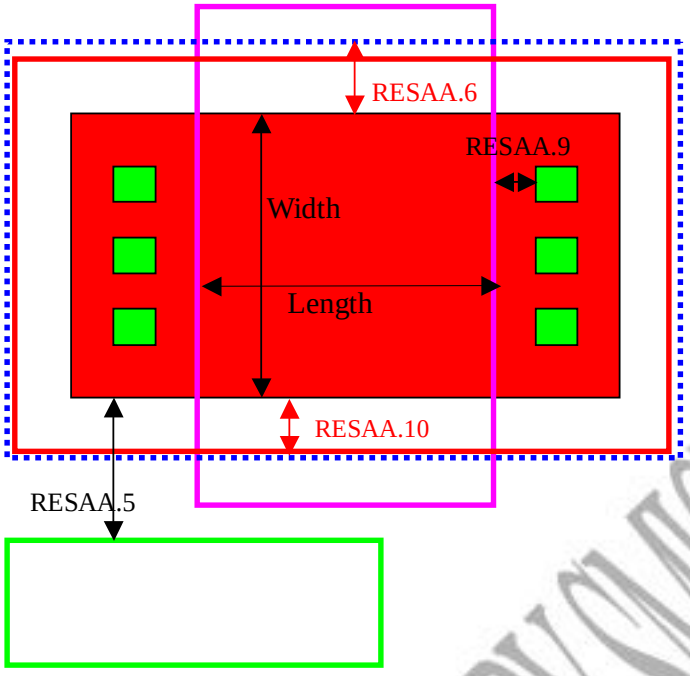
7.2.34.1 AA resistor guidelines

RESAA is blocking layer for AA resistor. AA resistor is the overlapped area of AA and RESAA, AA resistor must within RESAA layer.

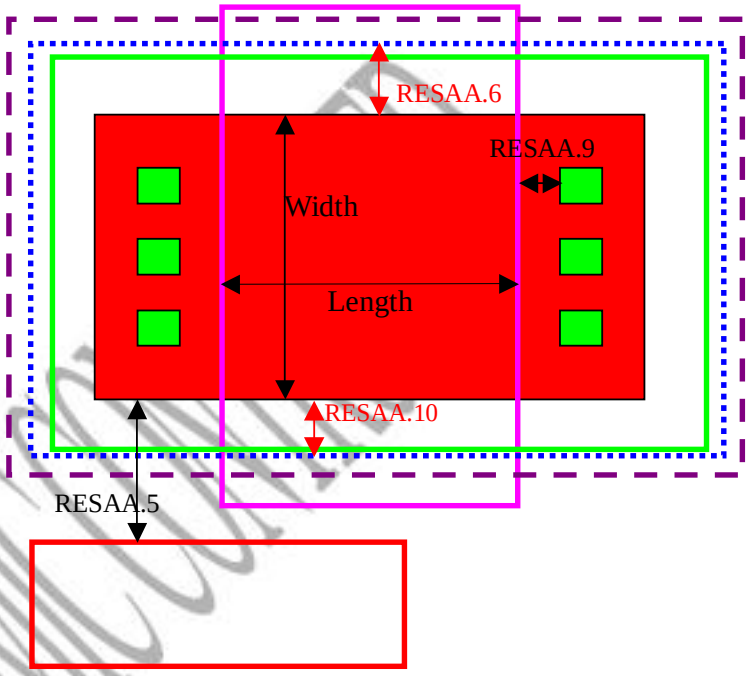
Note:RESAA.n (n=1 – 7) is for SAB resistor. RESAA.8 is for non-SAB resistor.

Rules number	Description	Operation	Design Value	Unit
RESAA.1	Width of AA resistor, and is suggested AA resistor square number(length/width ratio) ≥1 for stable Rs	≥	0.4	um
RESAA.2.	For AA resistor, make sure the AA be covered by SAB and implanted by SN or SP.			
RESAA.3.	Dummy layer RESAA is drawn to block LDD implant in the resistor area according to LOTA table.			
RESAA.4.	Dog-bone design at the end of AA resistor for contact pick-up is not suggested.			
RESAA.5.	Space between AA resistors area and other implant region	≥	0.2	um
RESAA.6.	Extension of RESAA outside of AA resistor area	≥	0.2	um
RESAA.7.	AA SAB resistor with SP must be inside NW			
RESAA.8.	For Non-SAB resistor, two sides of RESAA must be along the CT edge.			
RESAA.9	Space between SAB and CT	=	0.2	um
RESAA.10	SP/SN enclosure of AA resistor	≥	0.16	um

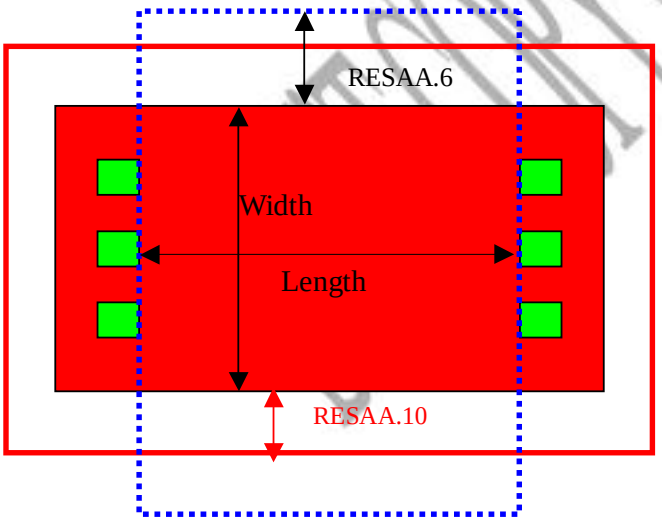
N+AA SAB resistor (non-salicide resistor)



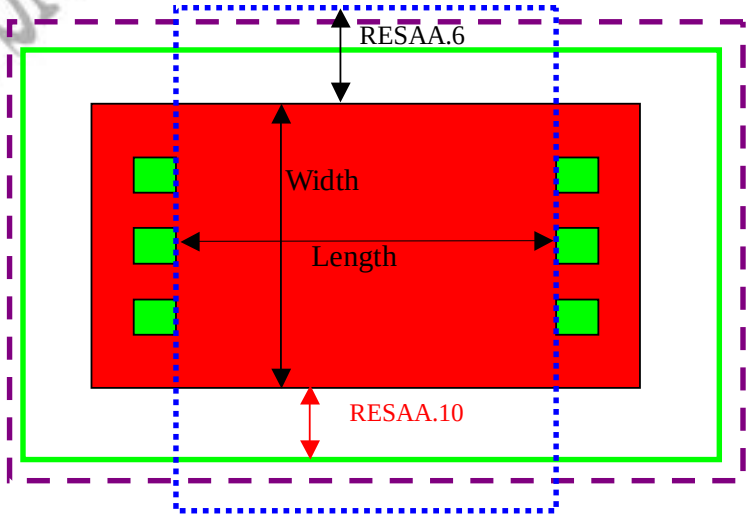
P+AA SAB resistor (non-salicide resistor)



N+AA Non-SAB resistor



P+AA Non-SAB resistor

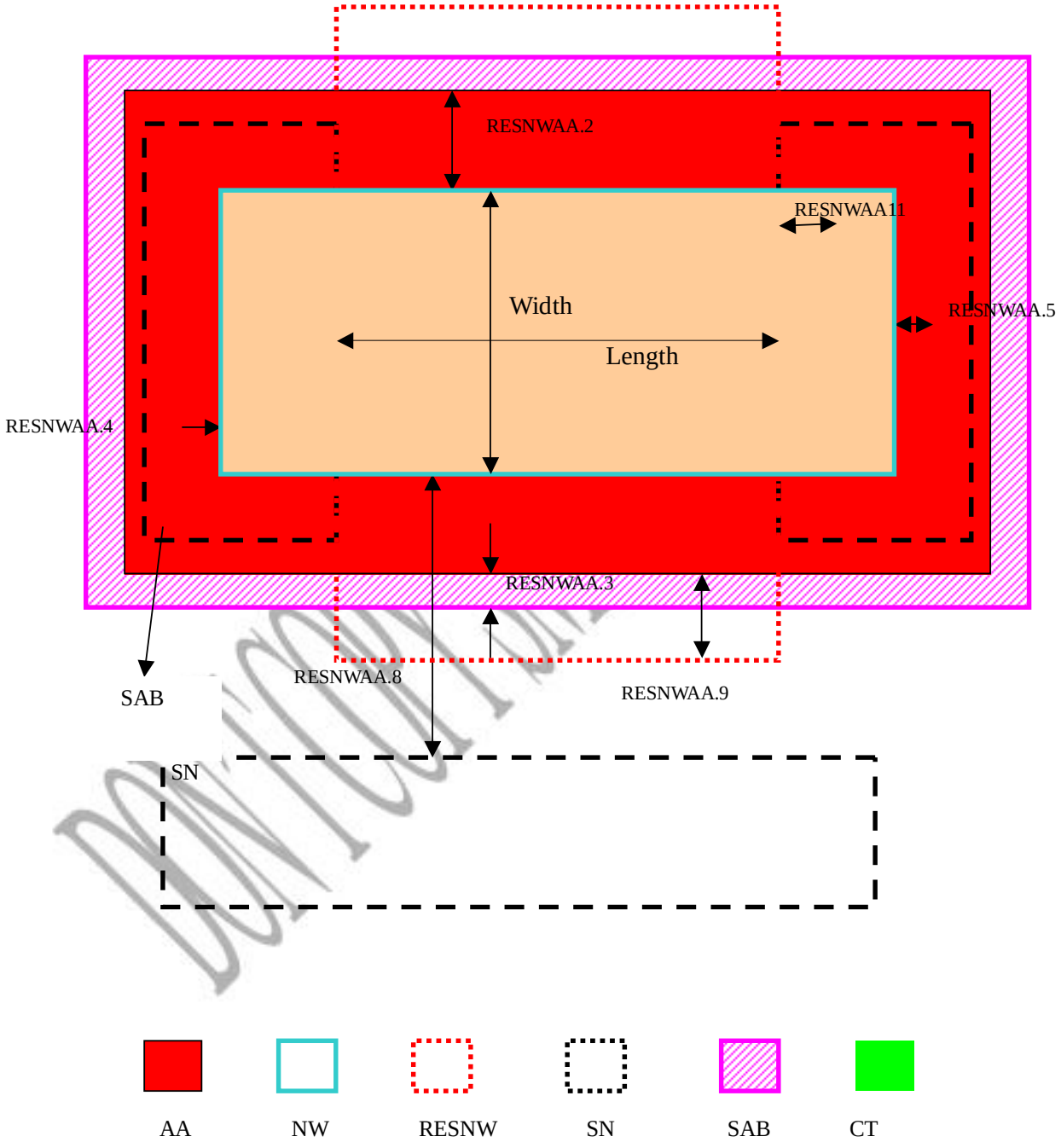


7.2.34.2 NW resistor guidelines

RESNW layer is to define the NW resistor area where no other implantation layer except for NW, NW resistors is the overlapped area of NW and RESNW, NW resistor must within RESNW layer.

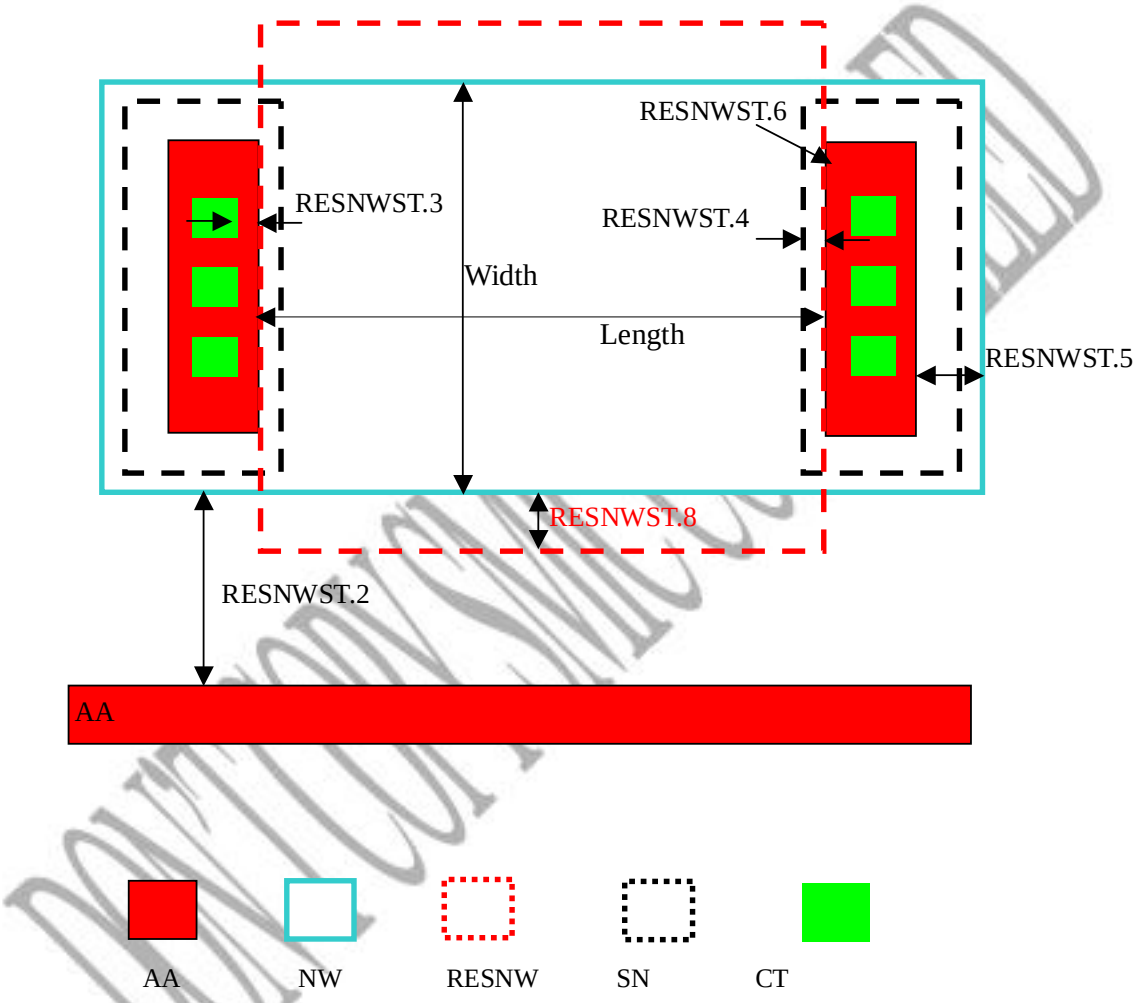
7.2.34.2.1 NW resistor under AA guidelines

Rules number	Description	Operation	Design Value	Unit
RESNWAA.1	NW-Resistor width	≥	1.6	um
RESNWAA.2	AA enclosure of NW-Resistor	≥	0.30	um
RESNWAA.3	SAB enclosure of AA	≥	0.20	um
RESNWAA.4	NW enclosure of CT	≥	0.20	um
RESNWAA.5	Enclosure of SAB and related NW	≥	0.20	um
RESNWAA.6	RESNW must not overlap with other implant layers(except NW) in the resistor area.			
RESNWAA.7	Space between RESNW and silicided CT area	=	0.20	um
RESNWAA.8	Space between NW of NW resistors and un-related implant region	≥	0.60	um
RESNWAA.9	Extension of RESNW outside of AA	≥	0.20	um
RESNWAA.10	SAB must cover NW resistor except CT area			
RESNWAA.11	Space between RESNW and CT	=	0.4	um



7.2.34.2.2 NW resistor under STI guidelines

Rules number	Description	Operation	Design Value	Unit
RESNWST.1	NW-Resistor width	≥	1.6	um
RESNWST.2	Space between NW resistor and adjacent AA	≥	0.50	um
RESNWST.3	CT enclosed by silicided AA	≥	0.20	um
RESNWST.4	SN implant area enclosure of silicided AA	≥	0.15	um
RESNWST.5	NW enclosure of silicided AA area	≥	0.20	um
RESNWST.6	Space between RESNW to silicided AA area	=	0.00	um
RESNWST.7	RESNW(ineract with SN) must not overlap with dummy pattern and other implant layers(except NW) in the resistor area			
RESNWST.8	Extension of RESNW outside of NW	≥	0.20	um
RESNWST.9	No silicide is allowed on NW Resistor except for CT area			



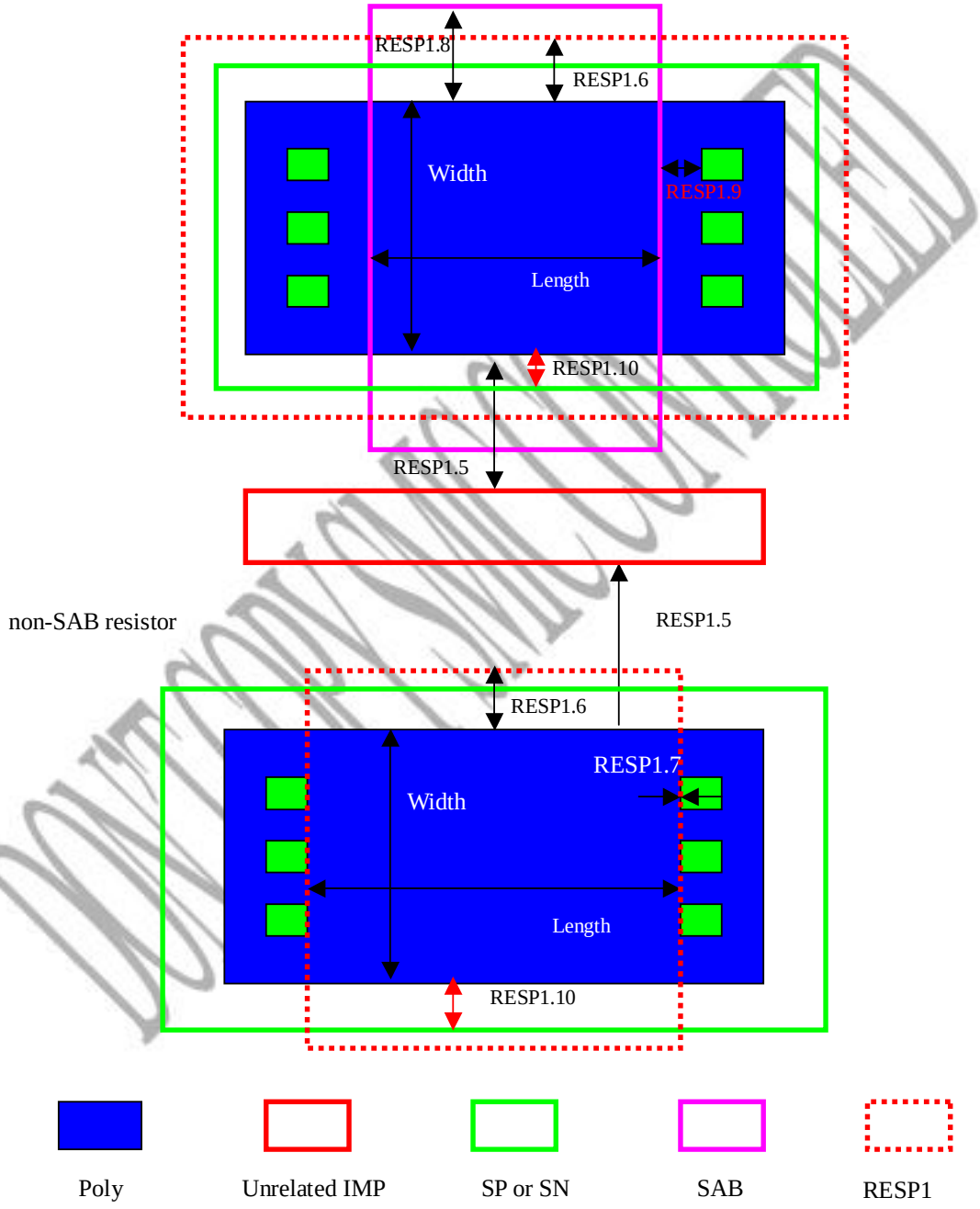
7.2.34.3 Poly resistor layout guidelines

RESP1 is blocking layer for poly resistor. Poly resistor is the overlapped area of poly and RESP1, poly resistor must within RESP1 layer. Suggest to use P-poly resistors where is possible.

Rules number	Description	Operation	Design Value	Unit
RESP1.1	Width of poly resistor, and is suggested poly resistor square number(length/width ratio) ≥1 for stable Rs.	≥	0.4	um
RESP1.2.	For poly resistor, make sure the poly be covered by SAB and implanted by either SN or SP.			
RESP1.3.	Dummy layer RESP1 is drawn to block LDD implant in the resistor area according to LOTA table.			
RESP1.4	Dog-bone design at the end of poly resistor for contact pick-up is not suggested.			
RESP1.5.	Space between poly resistors and un-related implant region (follow GT.10 rule)	≥	0.16	um
RESP1.6	Extension of RESP1outside of Poly resistor area	≥	0.2	um
RESP1.7	For Non-SAB Poly resistor, two sides of RESP1 must be along the CT edge.			
RESP1.8	Extension of SAB outside of poly resistor area(follow SAB.6 rule)	≥	0.2	um
RESP1.9	Space between SAB and CT	=	0.2	um
RESP1.10	Enclosure of SP/SN outside of a Poly resistor area (following GT.9 rule)	≥	0.16	um

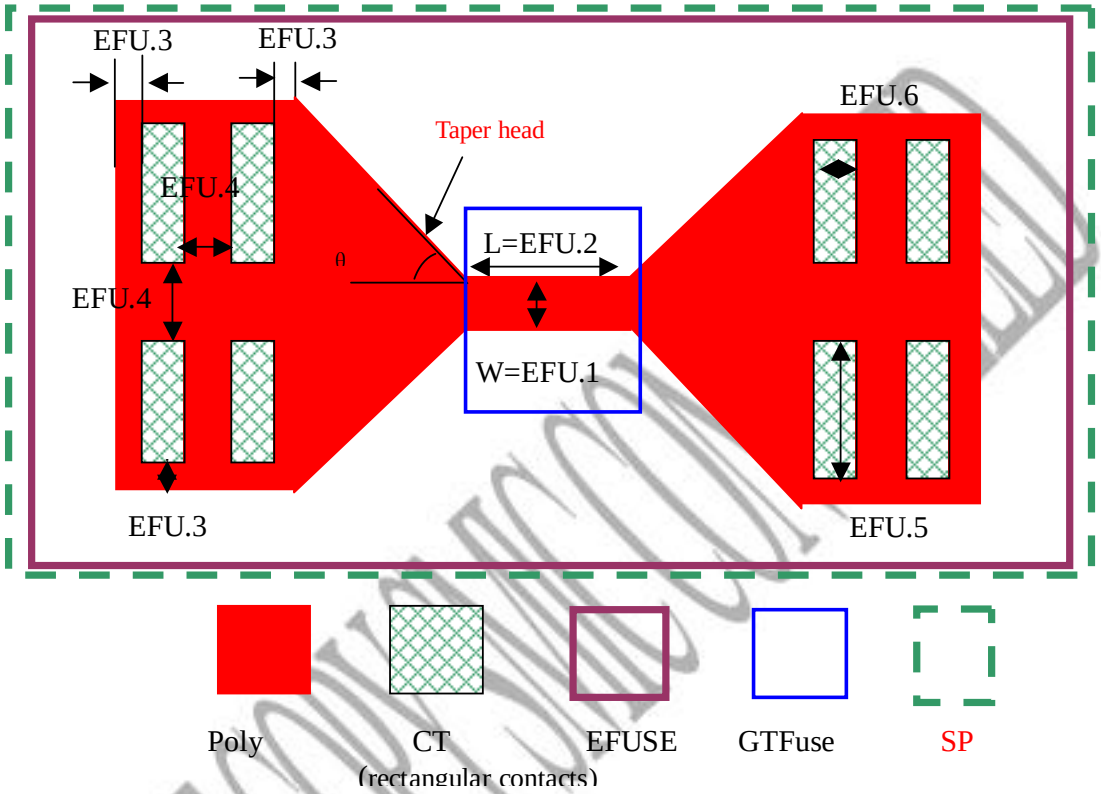
Note:RESP1.n(n=1 – 6) is for SAB poly resistor, RESP1.7 is for non-SAB poly resistor.

SAB Resistor (non-silicided)



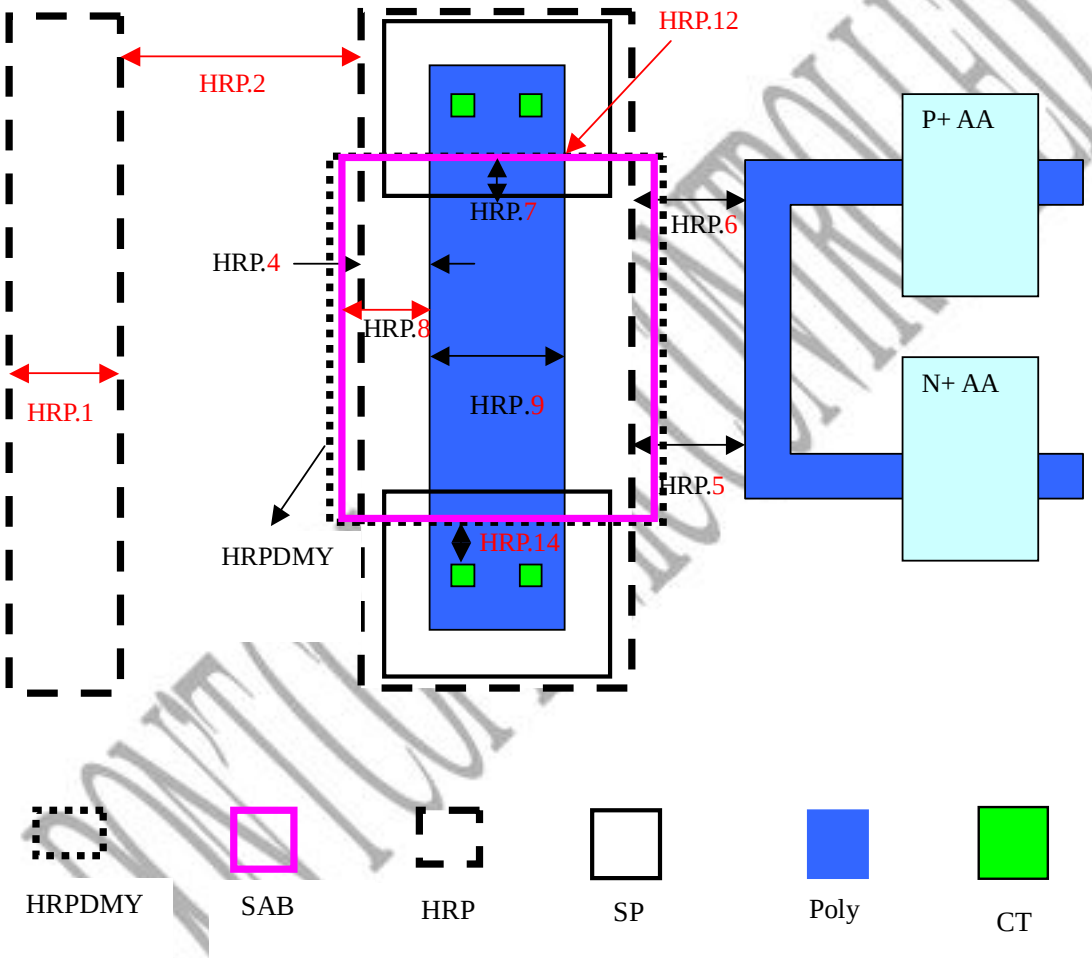
7.2.34.4 Poly E-Fuse layout guidelines

Rules number	Description	Operation	Design Value	Unit
EFU.1	E-Fuse Width (perpendicular to current flow)	=	0.06	um
EFU.2	E-Fuse Length (parallel to current flow)	=	0.24	um
EFU.3	CT enclosure by poly	=	0.05	um
EFU.4	Space between two rectangular contacts (RCT)	=	0.16	um
EFU.5	Length of RCT (rectangular contacts)	=	0.30	um
EFU.6	Width of RCT (rectangular contacts)	=	0.09	um
EFU.7	Use 2x2 RCT array for E-Fuse poly contact			
EFU.8	Angle of poly taper head (degree)	=	45	degree
EFU.9	(Purposely blank)			
EFU.10	GTFUSE is used to identify E-Fuse function area			
EFU.11	EFUSE is used to identify E-Fuse area			



7.2.34.5 HRP (High resistance poly) guidelines

Rules number	Description	Operation	Design Value	Unit
HRP.1	Width of HRP	≥	0.21	um
HRP.2	Space between two HRP	≥	0.21	um
HRP.3[NC]	It is strongly suggested that the resistor square number (length/width ratio) ≥ 1 for precise Rs.			
HRP.4	HRP enclosure of high resistance poly	≥	0.20	um
HRP.5	Space between HRP region and NMOS poly	≥	0.16	um
HRP.6	Space between HRP region and PMOS poly	≥	0.16	um
HRP.7	SP overlap with SAB	=	0.30	um
HRP.8	SAB extension outside of high resistance poly	≥	0.22	um
HRP.9	Poly width for high resistance poly	≥	2.00	um
HRP.10	Dummy layer "HRPDMY" is marker layer for LVS/ DRC to define high resistance poly resistor region.			
HRP.11	(SN, SP) layers are not allowed in the HRPDMY region (when checking the rule, size down the HRPDMY by 0.3um along the current direction).			
HRP.12	HRPDMY edge should align with SAB edge.			
HRP.13[NC]	For contact rule in HRP region, please follow CT main rule.			
HRP.14	Space between SAB and CT in HRP region	=	0.2	um

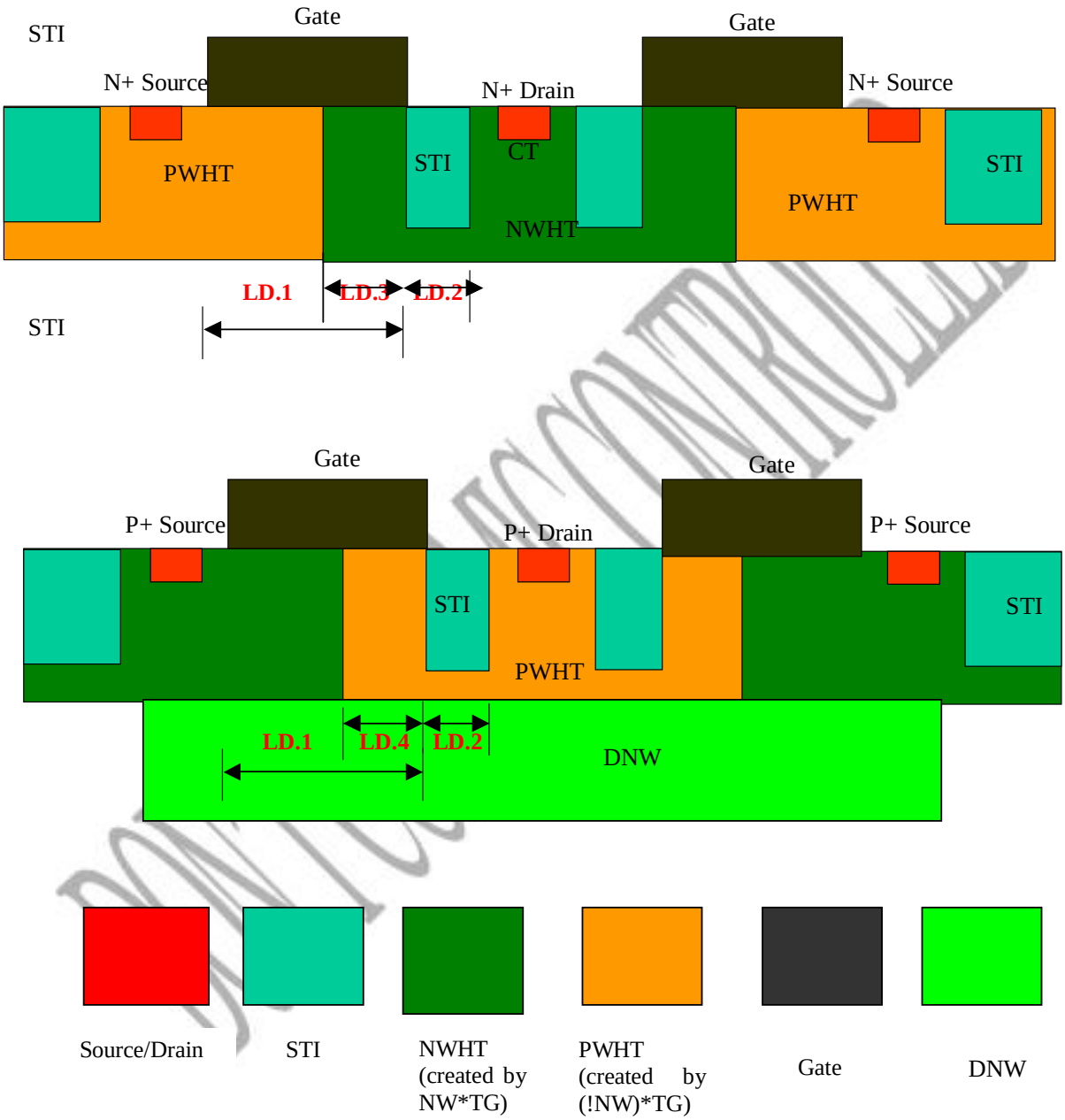


7.2.34.6 LDMOS layout guidelines

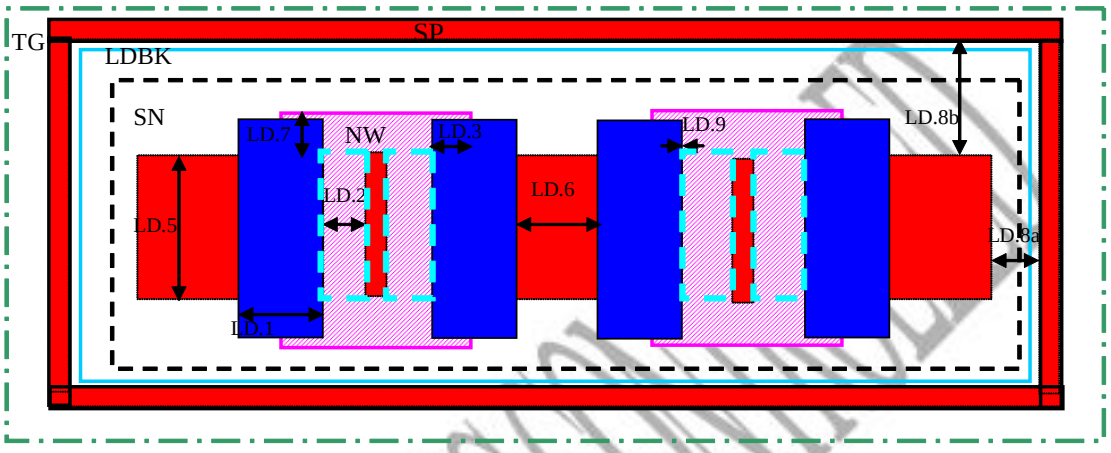
The asymmetric LDMOS is parasitical device to 2.5V IO; So, LDMOS area must be covered by TG layer and follow 2.5V IO general design rule besides below special LDMOS rule.

Only drain side with field plate for high voltage 5V operation; Gate side with 2.5V operation voltage; Source side connect to ground.

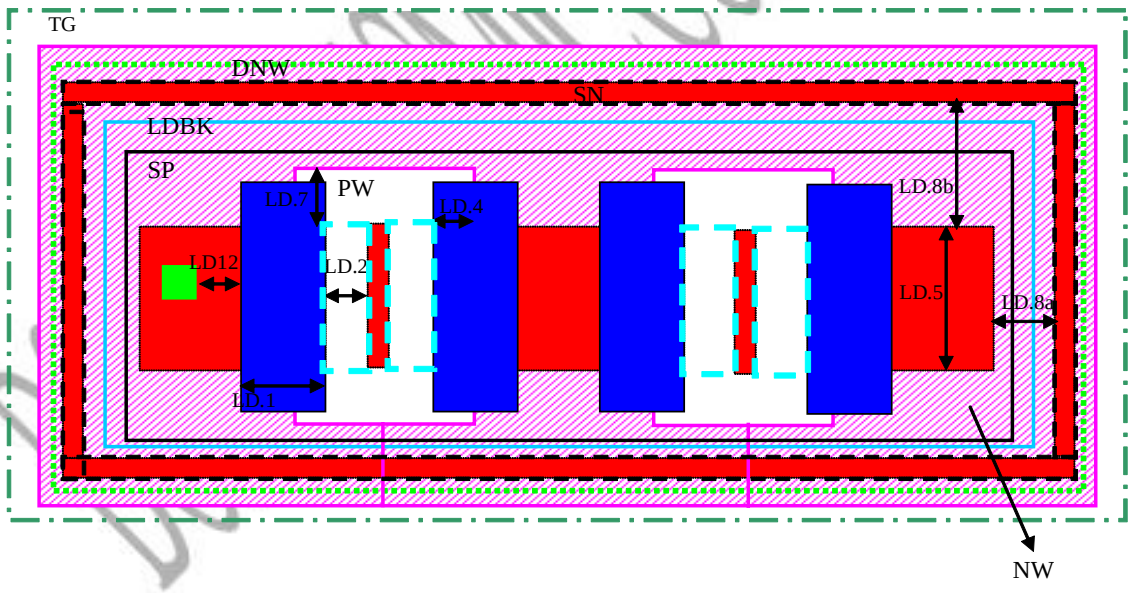
Rules number	Description	Operation	Design Value	Unit
LD.1a	LDMOS gate length	≥	0.48	um
LD.2	Dummy layer STIDMY is required for LDMOS transistor field plate area. STI width for LDMOS transistor drain side field plate	=	0.11	um
LD.3	Overlap of NW and LDNMOS gate	=	0.20	um
LD.4	Overlap of PW and LDPMOS gate	=	0.20	um
LD.5a	Channel width for LDMOS transistors	≥	2	um
LD.6	Space between one LDMOS gate poly to another LDMOS gate poly on source side	≥	0.27	um
LD.7	NW or PW extension outside of LDMOS AA along gate poly length direction	≥	0.25	um
LD.8a	Space between LDMOS source side AA and pickup AA along source/drain direction	≥	0.6	um
LD.8b	Space between LDMOS source side AA and pickup AA along gate poly direction	≥	0.9	um
LD.9	GT to STI drain side field plate overlap	=	0	um
LD.10	LDMOS block layer (LDBK) is used to identify LDMOS function area. LDBK extension outside of MOSAA	≥	0.4	um
LD.11	STIDMY enclosure LDMOS drain side filed plate	=	0	um
LD.12	CT to GT space on LDMOS at source side	≥	0.11	um
LD.13[NC]	A LDMOS unit structure has two poly and a common drain. Common source or single poly structure is not suggested.			

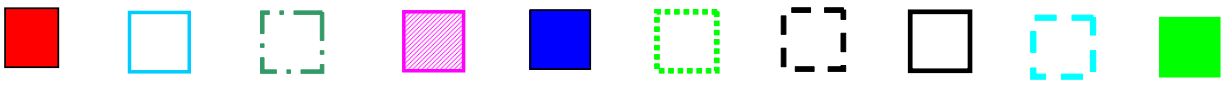


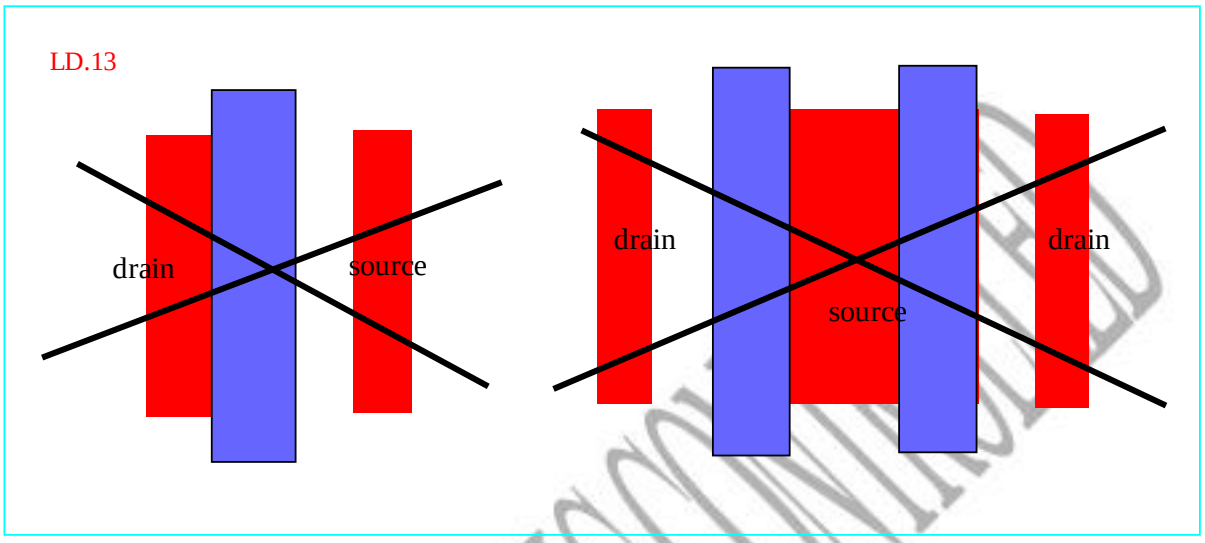
LDNMOS Platform



LDPMOS Platform



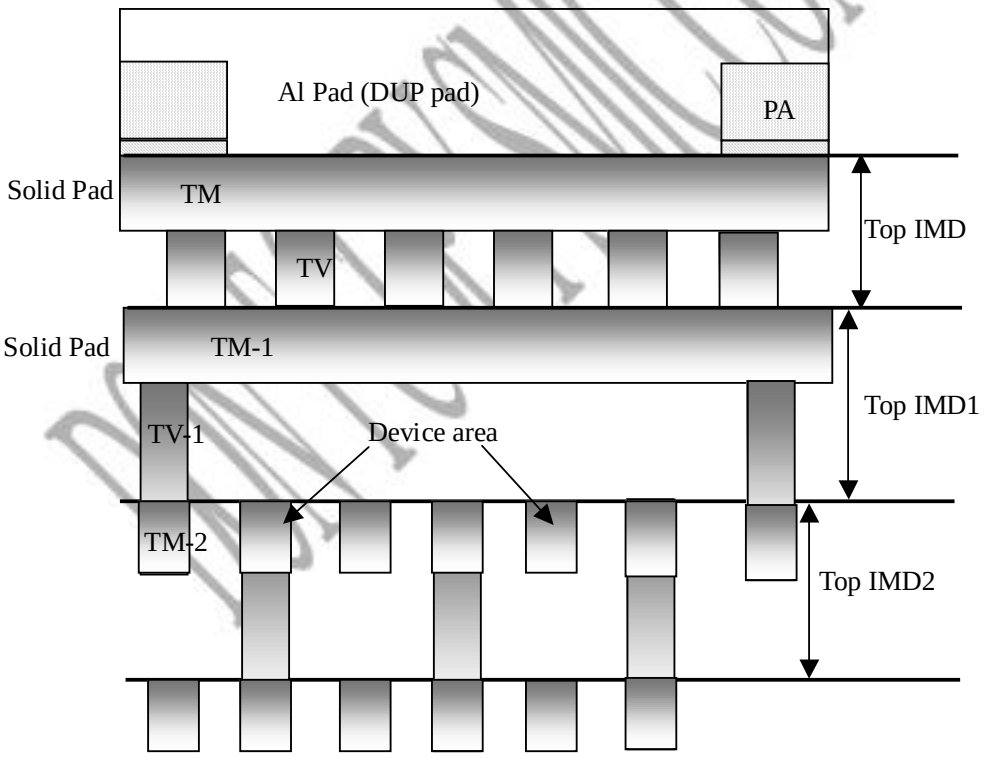




7.2.34.7 DUP (Device under pad) pad guidelines

Rules Number	DESCRIPTION
DUP.1[NC]	Two metal layers (TM and TM-1) are needed between DUP pad and device, where the metal design must be solid.
DUP.2[NC]	For one top metal process: TV-1 pattern is not allowed under the DUP pad opening area. For two top metal process: TV1 or STV1 patterns are not allowed under the DUP pad opening area.
DUP.3[NC]	TV array must be drawn between TM and TM-1 layer under the DUP pad opening area.
DUP.4[NC]	It's not allowed to add metal slots for TM and TM-1 under the DUP pad opening area.

Notes:
1. TM is TM2 or STM2 or MTT2.
2. TM-1 is directly underneath TM layer, it can be inter-metal (Mn) or TM1 or STM1.
3. TV is TV2 or STV2 or UTV2. TV-1 is directly underneath TV layer, it can be inter-via (Vn) or TV1 or STV1.



Cross section of DUP pad

7.2.34.8 Seal Ring layout guidelines

Use of the scribe line seal ring to protect test chip is recommended. A completed seal ring structure includes metal guard rings, die corner stress relief patterns and assembly isolation areas.

7.2.34.8.1 SMIC Seal Ring layout dimension

The dimensions given in Figs. 1-5 and in the tables of this section are used by SMIC. The numbers in the table are mask size, which OPC and mask bias operation have taken into consideration.

A. Typical structure of metal rings

Continuous metal rings are required on all sides of a chip that is intended for dicing and packaging. A 45 degree bending is expected around every die corner. Multiple stacked via/metal trench patterns are used to suppress crack risk during dicing saw operation in assembly. Refer to Fig.1 and Fig.2 for the schematics. For products having less than 10 metal layers, please skip the metal and via layers those are not used.

B. Die corner stress relief pattern layout

The seal ring corner layout is recommended to manage local stress at each die corner. The dimension of each segment of the corner layout is given in Fig. 3~4. Same as metal ring parts, there are only AA/SP layers needed under contact layer on die corner stress relief areas.

For those who wish SMIC to apply seal rings for the customers, a separate seal ring corner will be used, since SMIC is not going to change the corner part of customer's original layout. Please refer to Fig. 4.

Items	Description	Operation	Design Value	Unit
SR 1	Contact slot width	=	0.14	um
SR 2	V1-V7 slot width	=	0.11	um
SR 3	TV1, TV2 slot width (for 4X option)	=	0.28	um
SR 4	Square CT size	=	0.135	um
SR 5	Square V1-V7 size	=	0.130	um
SR 6	Square TV1, TV2 size (for 4X option)	=	0.39	um
SR 7	Space between square CT along the direction of seal ring	=	0.705	um
SR 8	Space between square Vn (n=1~7) along the direction of seal ring	=	0.71	um
SR 9	Space between square TVn (n=1~2) along the direction of seal ring	=	0.45	um
SR 10	Metal width of inner ring	=	5.00	um
SR 11	Metal width of outer ring	=	1.50	um

SR 12	Space between inner and outer metal ring	=	1.50	um
SR 13	Space between inner metal ring and layout edge	=	0.00	um
SR 14	Space between outer metal ring and window edge	=	2.00	um
SR 15	Passivation slot(RDL via) width	=	2.20	um
SR 16	Space between passivation slot(RDL via) and layout edge	=	2.50	um
SR 17	Al ring (RDL) width	=	7.20	um
SR 18	Space between AL ring (RDL) and layout edge	=	0.00	um
SR 19	(purposely blank)			
SR 20	(purposely blank)			
SR 21	Distance from window edges to the point that inner ring start to bend 45 degree at corners. This rule is for SMIC to apply seal rings for customer.	=	28.00	um
SR 22	Space between square contact and M1 edge in the die corner dummy relief area	=	0.183	um
SR 23	Space between square via1~via7 and Mx (x=1~8) metal edge in the die corner dummy relief area	=	0.185	um
SR24	Space between square TV and TM dummy metal edge in the die corner dummy relief area (for 4X option)	=	0.805	um
SR 25	Metal width of die corner dummy pattern for M1 to M8	=	0.50	um
SR 26	TM1/TM2 metal width of die corner dummy pattern	=	2.00	um
SR 27	Space between metal of die corner dummy pattern for M1 to M8	=	0.50	um
SR 28	Space between metal of die corner dummy pattern for TM1/TM2	=	2.00	um
SR 29	Contact distance from each other in die corner dummy area	=	0.865	um
SR 30	Vn (n=1~7) distance from each other in die corner dummy area	=	0.87	um
SR 31	TV1/TV2 (for 4X option) distance from each other in die corner dummy area	=	0.61	um
SR 32	Total seal ring width	=	10.00	um

SR 33	Assembly isolation between active AA/GT/METAL/AL RDL patterns and internal metal ring edge	=	10.00	um

Note: Top via size in the above tables is for TV 4X option, which can be shared with MTT2/UTV2 option. If TV1/2 layout follows top via 2X design rule, TV1/2 slot size in seal ring is fixed at 0.19um, and TV1/2 square hole size is fixed at 0.20um. Other dimensions should be adjusted accordingly.

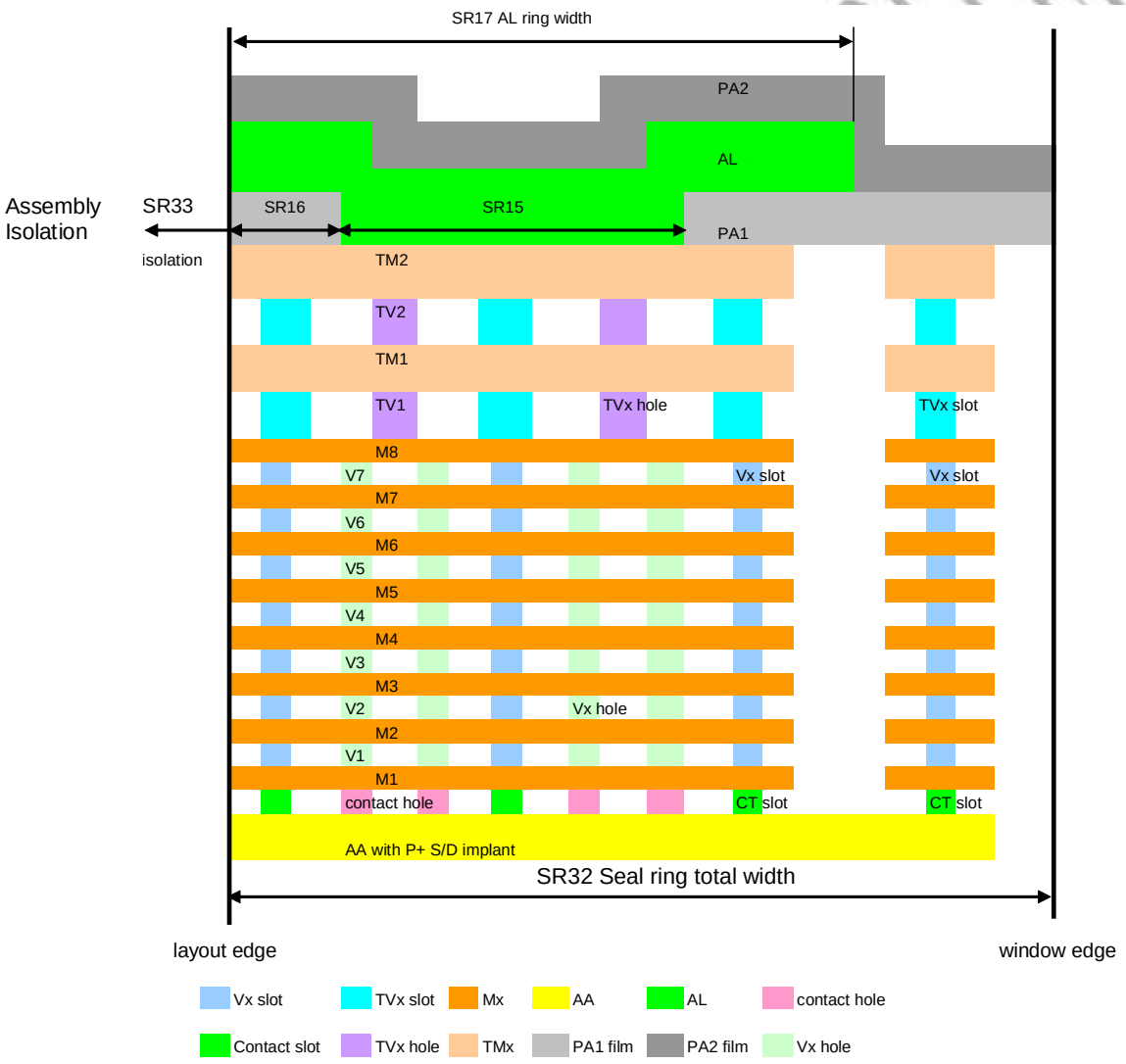
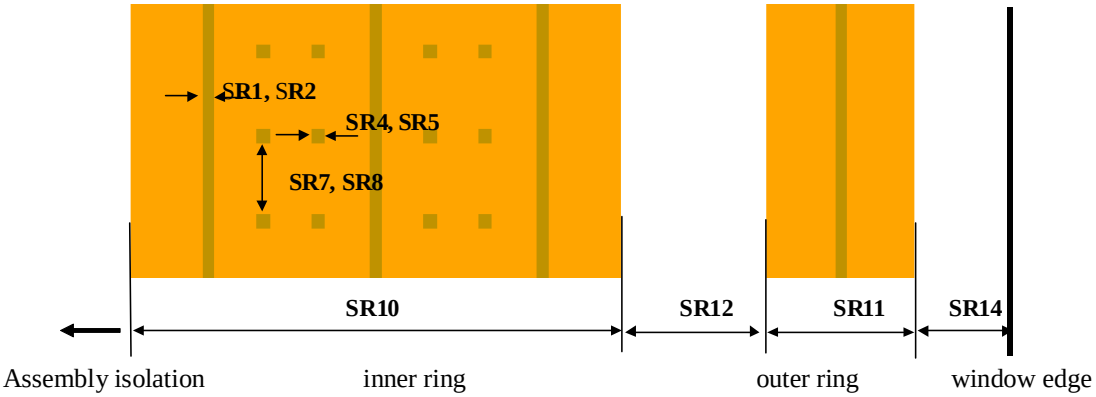
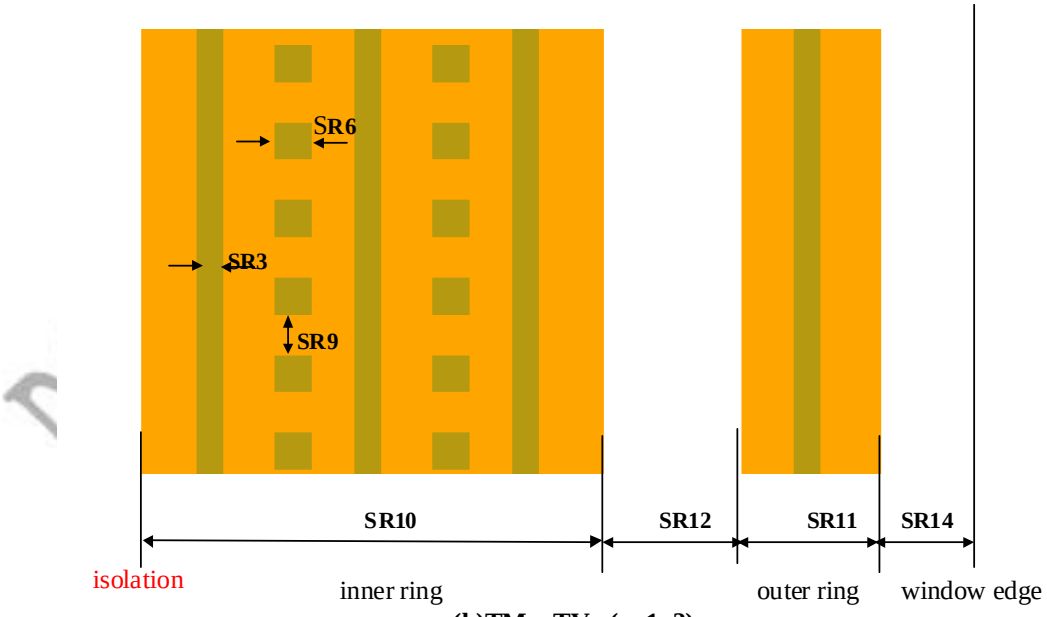


Fig.1 Cross section schematic of 10 metal seal ring structure



(a) For CT, M1~M8, V1~V7



(b)TMx, TVx (x=1, 2)

Fig. 2 Schematic top view of the seal ring structure

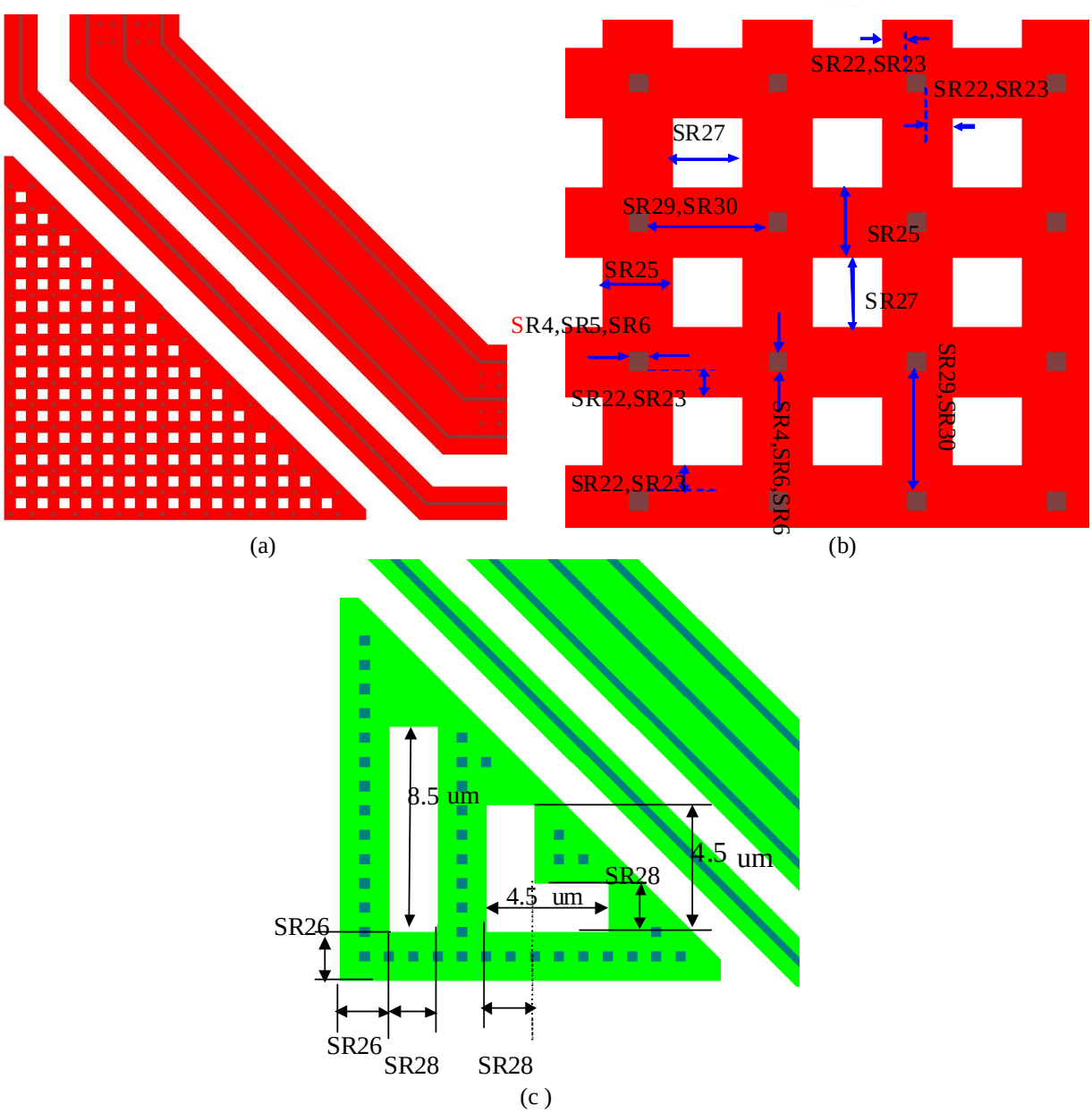
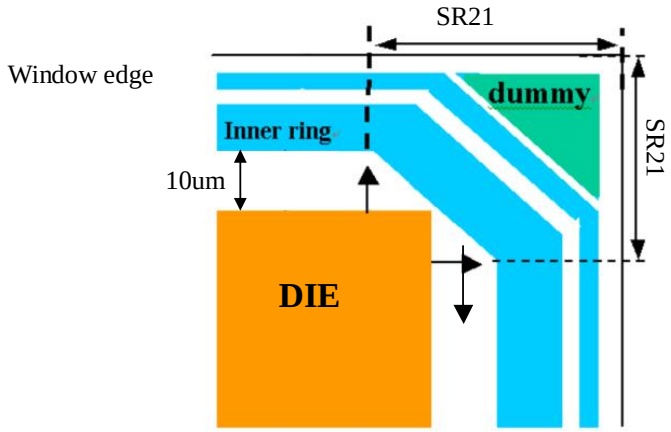


Fig. 3. Die corner stress relief structure layout (a) for M1~M8, CT, V1~V7 (b) zoom in images for the corner area of (a) (c) design for TV1~2, TM1~2



Assembly Isolation area

Fig.4 Seal ring corner if applied at SMIC

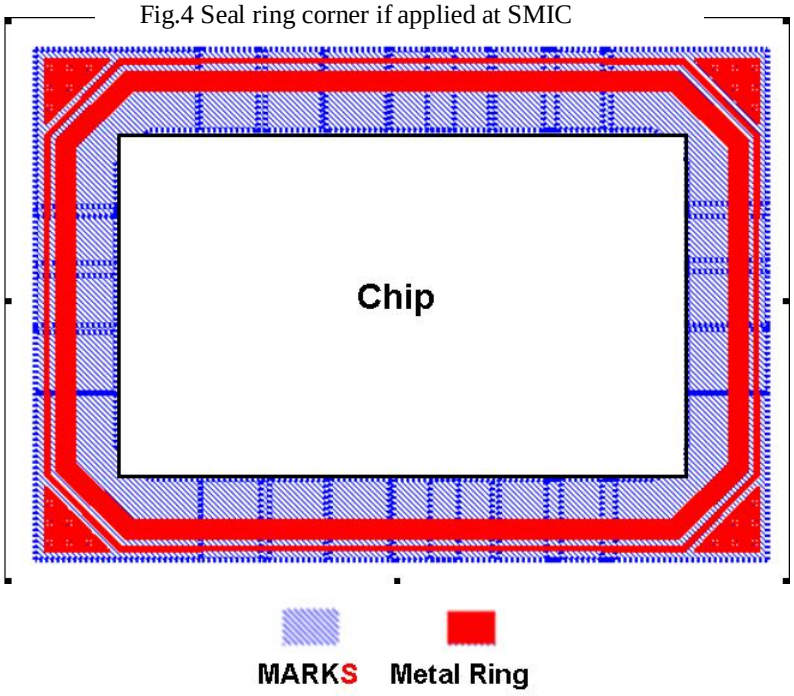


Fig.5 MARKS covered seal ring area

Table 3 Layout Coordinate of Seal ring structure

"C" represents no PR areas and "D" represents PR covered areas.

Layer	GDS No.	Data type	Assemble Isolation Tone	Starting Coordinate	Ending Coordinate	Size (um)	Pattern Tone
DNW	19	0	D	0	10	10	D
AA	10	0	C	0	8	8	D
PW	20	0	D	0	10	10	D
VTNH	47	0	D	0	10	10	D
PWH	105	0	D	0	10	10	D
PWHT	109	0	D	0	10	10	D
NW	14	0	D	0	10	10	D
NWH	106	0	D	0	10	10	D
NWHT	110	0	D	0	10	10	D
NC	21	0	D	0	10	10	D
PC	16	0	D	0	10	10	D
VTPH	46	0	D	0	10	10	D
DG	29	0	C	0	10	10	C
GT	30	0	C	0	10	10	C
NLL	35	0	D	0	10	10	D
PLL	38	0	D	0	10	10	D
PLH	37	0	D	0	10	10	D
NLH	36	0	D	0	10	10	D
SN	40	0	D	0	10	10	D
LVN	219	0	D	0	10	10	D
LVP	218	0	D	0	10	10	D
TG	125	0	D	0	10	10	D
PLHT	115	0	D	0	10	10	D
NLHT	114	0	D	0	10	10	D
SP	43	0	D	0	8	8	C
ESD1	41	0	D	0	10	10	D
SAB	48	0	D	0	10	10	D
CT (slot)	50	0	D	0.705	0.845	0.14	C
CT	50	0	D	1.283	1.418	0.135	C
CT	50	0	D	1.843	1.978	0.135	C
CT (slot)	50	0	D	2.415	2.555	0.14	C
CT	50	0	D	2.993	3.128	0.135	C
CT	50	0	D	3.553	3.688	0.135	C
CT (slot)	50	0	D	4.125	4.265	0.14	C

CT (slot)	50	0	D	7.175	7.315	0.14	C
Metal 1	61	0	D	0	5	5	C
Metal 1	61	0	D	6.5	8	1.5	C
Via 1 (slot)	70	0	D	0.735	0.845	0.11	C
Via 1	70	0	D	1.285	1.415	0.13	C
Via 1	70	0	D	1.845	1.975	0.13	C
Via 1 (slot)	70	0	D	2.445	2.555	0.11	C
Via 1	70	0	D	2.995	3.125	0.13	C
Via 1	70	0	D	3.555	3.685	0.13	C
Via 1 (slot)	70	0	D	4.155	4.265	0.11	C
Via 1 (slot)	70	0	D	7.205	7.315	0.11	C
Metal 2	62	0	D	0	5	5	C
Metal 2	62	0	D	6.5	8	1.5	C
Via 2 (slot)	71	0	D	0.735	0.845	0.11	C
Via 2	71	0	D	1.285	1.415	0.13	C
Via 2	71	0	D	1.845	1.975	0.13	C
Via 2 (slot)	71	0	D	2.445	2.555	0.11	C
Via 2	71	0	D	2.995	3.125	0.13	C
Via 2	71	0	D	3.555	3.685	0.13	C
Via 2 (slot)	71	0	D	4.155	4.265	0.11	C
Via 2 (slot)	71	0	D	7.205	7.315	0.11	C
Metal 3	63	0	D	0	5	5	C
Metal 3	63	0	D	6.5	8	1.5	C
Via 3 (slot)	72	0	D	0.735	0.845	0.11	C
Via 3	72	0	D	1.285	1.415	0.13	C
Via 3	72	0	D	1.845	1.975	0.13	C
Via 3 (slot)	72	0	D	2.445	2.555	0.11	C
Via 3	72	0	D	2.995	3.125	0.13	C
Via 3	72	0	D	3.555	3.685	0.13	C
Via 3 (slot)	72	0	D	4.155	4.265	0.11	C
Via 3 (slot)	72	0	D	7.205	7.315	0.11	C
Metal 4	64	0	D	0	5	5	C
Metal 4	64	0	D	6.5	8	1.5	C
Via 4 (slot)	73	0	D	0.735	0.845	0.11	C
Via 4	73	0	D	1.285	1.415	0.13	C
Via 4	73	0	D	1.845	1.975	0.13	C
Via 4 (slot)	73	0	D	2.445	2.555	0.11	C
Via 4	73	0	D	2.995	3.125	0.13	C

Via 4	73	0	D	3.555	3.685	0.13	C
Via 4 (slot)	73	0	D	4.155	4.265	0.11	C
Via 4 (slot)	73	0	D	7.205	7.315	0.11	C
Metal 5	65	0	D	0	5	5	C
Metal 5	65	0	D	6.5	8	1.5	C
Via 5 (slot)	74	0	D	0.735	0.845	0.11	C
Via 5	74	0	D	1.285	1.415	0.13	C
Via 5	74	0	D	1.845	1.975	0.13	C
Via 5 (slot)	74	0	D	2.445	2.555	0.11	C
Via 5	74	0	D	2.995	3.125	0.13	C
Via 5	74	0	D	3.555	3.685	0.13	C
Via 5 (slot)	74	0	D	4.155	4.265	0.11	C
Via 5 (slot)	74	0	D	7.205	7.315	0.11	C
Metal 6	66	0	D	0	5	5	C
Metal 6	66	0	D	6.5	8	1.5	C
Via 6 (slot)	75	0	D	0.735	0.845	0.11	C
Via 6	75	0	D	1.285	1.415	0.13	C
Via 6	75	0	D	1.845	1.975	0.13	C
Via 6 (slot)	75	0	D	2.445	2.555	0.11	C
Via 6	75	0	D	2.995	3.125	0.13	C
Via 6	75	0	D	3.555	3.685	0.13	C
Via 6 (slot)	75	0	D	4.155	4.265	0.11	C
Via 6 (slot)	75	0	D	7.205	7.315	0.11	C
Metal 7	67	0	D	0	5	5	C
Metal 7	67	0	D	6.5	8	1.5	C
Via 7 (slot)	76	0	D	0.735	0.845	0.11	C
Via 7	76	0	D	1.285	1.415	0.13	C
Via 7	76	0	D	1.845	1.975	0.13	C
Via 7 (slot)	76	0	D	2.445	2.555	0.11	C
Via 7	76	0	D	2.995	3.125	0.13	C
Via 7	76	0	D	3.555	3.685	0.13	C
Via 7 (slot)	76	0	D	4.155	4.265	0.11	C
Via 7 (slot)	76	0	D	7.205	7.315	0.11	C
Metal 8	68	0	D	0	5	5	C
Metal 8	68	0	D	6.5	8	1.5	C
TV1 (slot)	121	0	D	0.595	0.875	0.28	C
TV1	121	0	D	1.44	1.83	0.39	C
TV1 (slot)	121	0	D	2.305	2.585	0.28	C

TV1	121	0	D	3.15	3.54	0.39	C
TV1 (slot)	121	0	D	4.015	4.295	0.28	C
TV1 (slot)	121	0	D	7.065	7.345	0.28	C
TM1	120	0	D	0	5	5	C
TM1	120	0	D	6.5	8	1.5	C
TV2 (slot)	123	0	D	0.595	0.875	0.28	C
TV2	123	0	D	1.44	1.83	0.39	C
TV2 (slot)	123	0	D	2.305	2.585	0.28	C
TV2	123	0	D	3.15	3.54	0.39	C
TV2 (slot)	123	0	D	4.015	4.295	0.28	C
TV2 (slot)	123	0	D	7.065	7.345	0.28	C
TM2	122	0	D	0	5	5	C
TM2	122	0	D	6.5	8	1.5	C
BCB1(PA1 slot)	165	0	D	2.5	4.7	2.2	C
RDL	166	0	C	0	7.2	7.2	D
BCB2 (RDLPA2)	167	0	D	0	10	10	D
MARKS	189	151	NA	-10	10	20	NA
NODMF	180	0	NA	-10	10	20	NA

7.2.34.8.2 SMIC Seal Ring check rules

SMIC maskshop can help to add seal ring structure upon customer's request. If customers draw seal ring by themselves and combine it with main chip, the seal ring layout should not violate general design rules except special notices.

Rule No.	Description	Operation	Design Value	Unit
SRCK.1	Fixed CT slot width	=	0.09	um
SRCK.2	Fixed Vn slot width (n=1~7)	=	0.09	um
SRCK.3	TVn(n=1~2) slot width (for 4X option and UTV2)	≥	0.25	um
		≤	0.36	um
SRCK.4	STVn(n=1~2) slot width (for 2X option)	≥	0.19	um
		≤	0.20	um
SRCK.5	Space between two contact slots	≥	1.20	um
SRCK.6	Space between two Vn (n=1~7) slots	≥	1.20	um

SRCK.7	Space between two TVn/STVn/UTV2 (n=1~2) slots	≥	1.20	um
SRCK.8	Space between square contact and contact slot	≥	0.40	um
SRCK.9	Space between square Vn and Vn (n=1~7)slot	≥	0.40	um
SRCK.10	Space between square TVn (STVn/UTV2) and TVn (STVn/UTV2) slot(n=1~2)	≥	0.38	um
SRCK.11	M1 enclosure of V1 (both square via and slot patterns) in MARKS covered areas	≥	0.09	um
SRCK.12	Mn enclosure of Vn (both square via and slot patterns) in MARKS covered areas (n=2~7)	≥	0.09	um
SRCK.13	Mn+1 enclosure of Vn (both square via and slot patterns) in MARKS covered areas (n=2~7)	≥	0.09	um
SRCK.14	TM1/TM2 (STM1/STM2/MTT2) enclosure of TV1/TV2 (STV1/STV2/UTV2, both square via and slot patterns) in MARKS covered areas	≥	0.09	um
SRCK.15	Mn enclosure of TV1/TV2 (or STV1/STV2/UTV2, both square via and slot patterns) in MARKS covered areas. (Mn is the metal layer underneath of TV1/TV2/STV1/STV2/UTV2.)	≥	0.09	um
SRCK.16[NC]	Seal ring areas (including metal rings, die corner stress relief areas and assembly isolation areas) should be covered by MARKS layer for DRC and dummy automatic filling blockage (refer to Fig.5)			
SRCK.17	Assembly isolation between active AA/GT/METAL/AL RDL patterns and internal metal ring edge	≥	10.00	um
SRCK.18	No patterns (AA/GT/METAL/RDL) are allowed inside assembly isolation areas			
SRCK.19	No AA/GT/Metal dummy patterns are allowed inside MARKS covered areas.			
SRCK.20	Designers should refer to the seal ring layout (Fig. 1), which should include AA, CT, Mn(n=1~8), TM1(STM1), TM2(STM2/MTT2), Vn(n=1~7), TV1/STV1, TV2/STV2, to provide a low resistance path to ground for surge currents			

SRCK.21*	Passivation slot width ("RDL via" is recommended as drawn layer) in MARKS covered areas	≥	2.00	um
SRCK.22*	Al pattern (AL RDL) enclosure of passivation slot (RDL via) in MARKS covered areas	≥	1.00	um
SRCK.23*	TM2(STM2/MTT2) enclosure of passivation slot (RDL via) in MARKS covered areas	≥	0.50	um

Notes:

1. * The numbers are different from general rules, which can only be used in MARKS covered areas.
2. Contact, via and TV/UTV2/STV slots are not permitted for main chip design except MARKS/MARKG covered areas. (CT/via patterns, with the width/length ratio larger than 3, should be taken as Contact/via slots.)

7.2.34.9 Guard ring layout guidelines

Guard ring (which can be identified by MARKG marking layer) is used to protect inside circuits from damage, which should follow the rules as below.

Rule Number	DESCRIPTION	Operation	Design Value	Unit
GR.1	Fixed CT slot width in guard ring	=	0.09	um
GR.2	Fixed Vn slot width in guard ring (n=1~7)	=	0.09	um
GR.3a	TVn(n=1~2) slot (for 4X option and UTV option) width in guard ring	≥	0.25	um
		≤	0.36	um
GR.3b	STVn(n=1~2) slot (for 2X option) width in guard ring	≥	0.19	um
		≤	0.20	um
GR.4	Space between contact slots in guard ring	≥	1.20	um
GR.5	Space between via slots in guard ring	≥	1.20	um
GR.6	Space between TVn/STVn (n=1~2) slots in guard ring	≥	1.20	um
GR.7	Space between square contact and contact slot in guard ring	≥	0.40	um
GR.8	Space between square Vn and Vn slot in guard ring (n=1~7)	≥	0.40	um
GR.9	Space between square TVn/STVn/UTV2 and TVn/STVn/UTV2 slot in guard ring	≥	0.38	um
GR.10	M1 enclosure of V1 (both square via and slot patterns) in guard ring	≥	0.09	um
GR.11	Mn enclosure of Vn (both square via and slot patterns) in guard ring (n=2~7)	≥	0.09	um
GR.12	Mn+1 enclosure of Vn (both square via and slot patterns) in guard ring (n=2~7)	≥	0.09	um
GR.13	TM1/TM2 (or STM1/STM2/MTT2) enclosure of TV1/TV2 (or STV1/STV2/UTV2) (both square via and slot patterns) in guard ring	≥	0.09	um
GR.14	Mn enclosure of TV1/TV2 (STV1/STV2/UTV2) (both square via and slot patterns) in guard ring (Mn is the metal layer underneath of TV1/TV2/STV1/STV2/UTV2）	≥	0.09	um

GR.15[NC]	Guard ring areas (including metal rings, and isolation areas from active areas) should be covered by MARKG layer for DRC and dummy automatic filling blockage			
GR.16	Isolation between active AA/GT/METAL/AL patterns and internal metal ring edge	≥	1.00	um
GR.17	No dummy patterns (AA/GT/METAL/RDL) are allowed inside isolation areas			
GR.18*	Passivation slot width ("RDL via" is recommended as drawn layer) in guard ring	≥	2.00	um
GR.19*	Al pattern (RDL) enclosure of passivation slot (RDL via) by in guard ring	≥	1.00	um
GR.20*	TM2/STM2/MTT2 enclosure of passivation slot (RDL via) in guard ring	≥	0.50	um

Notes:

1. * The numbers are different from main rules, and only applied for MARKG covered areas.
2. Contact, via and TV/UTV2/STV slots are not permitted for main chip design except MARKS/MARKG covered areas. (CT/via patterns, with the width/length ratio larger than 3, should be taken as Contact/via slots.)

7.2.34.10 Al fuse guidelines

AL laser fuse consists of AL fuse element that is blown by laser (7.2.34.10.1), via that connect AL fuse elements to the circuits (7.2.34.10.2), guard ring(7.2.34.9) that surrounds the AL fuse array, and a fuse window which defines an area etched into passivation 2 where AL fuse array reside (7.2.34.10.3). Only AL14.5K option can be used for AL-fuse application. Al 28K option is not allowed for this purpose.

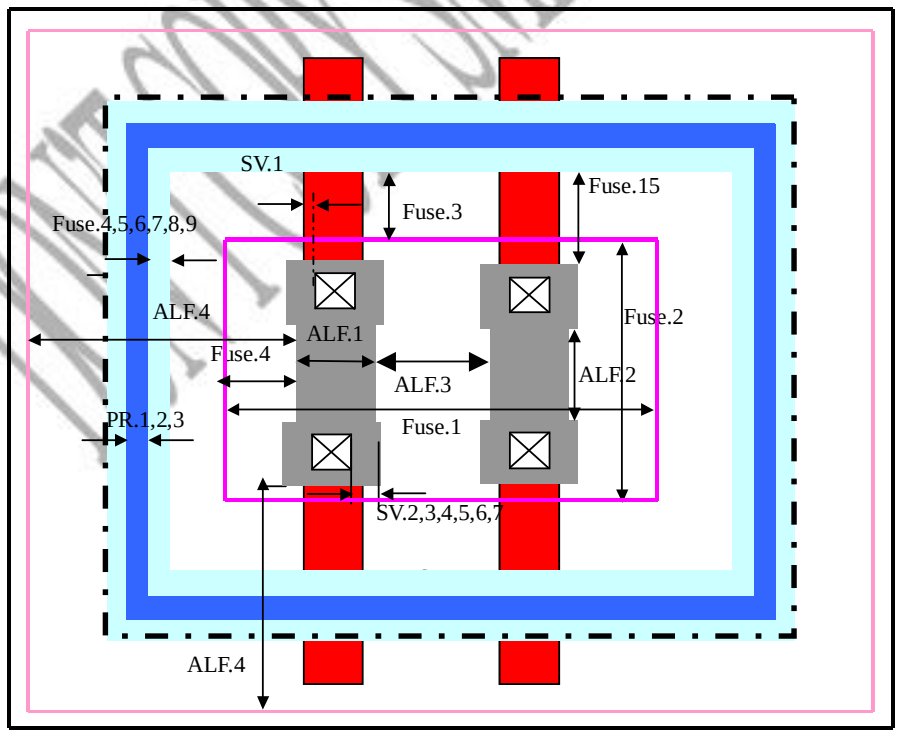
7.2.34.10.1 Al fuse element rule (to use RDL as drawing layer)

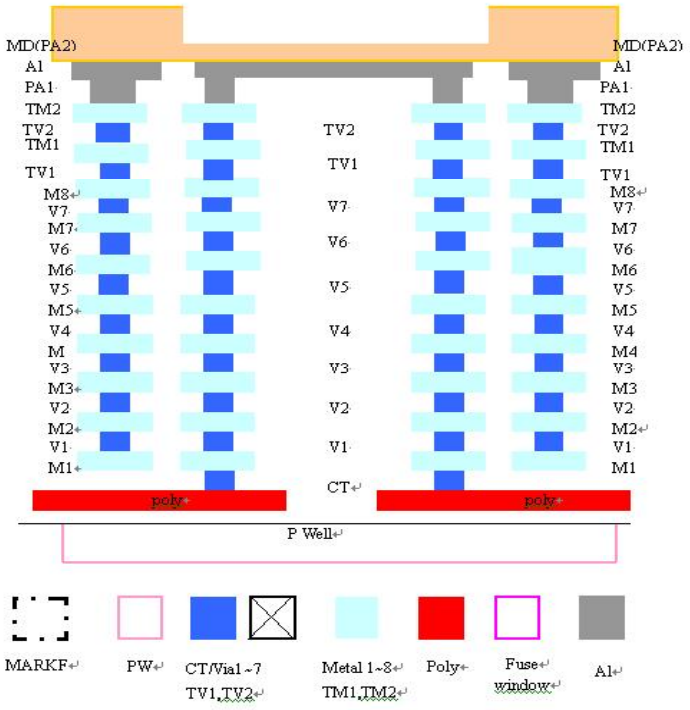
Rule No.	DESCRIPTION	Operation	Design Value	Unit
ALF.1	AL fuse element width	≥	0.80	um
ALF.2	AL fuse element length	≥	4.00	um
ALF.3	Space between AL fuse elements	≥	4.00	um
ALF.4	Space between fuse edge and p-well edge	≥	8.00	um
ALF.5	AL fuse must be connected to GT through stacked via/contact			
ALF.6[NC]	MARKF layer is needed for Fuse DRC check and automatic dummy filling blockage. The recommended size is same as the guard ring edge			
ALF.7	No AA/Poly/Metal dummy patterns are allowed in Fuse area covered by MARKF			

7.2.34.10.2 Stack via/CT connection to Al fuse

Stacked via/contact structures are needed to connect AL fuse elements to the circuits, which should follow below table. "RDL via" layer is used as drawing layer for vias that connect TM2/STM2 and AL fuse elements.

Rule No.	DESCRIPTION	Operation	Design Value	Unit
SV.1	CT enclosure by GT	≥	0.145	um
SV.2	CT enclosure by M1	≥	0.145	um
SV.3	Vn enclosure by Mn or Mn+1 for stacked via (n=1~8)	≥	0.145	um
SV.4	TV1/TV2 (STV1/STV2) enclosure by TM1/TM2 (STM1/STM2) for stacked via	≥	0.10	um
SV.5	TV1/STV1 enclosure by Mn for stack via	≥	0.10	um
SV.6	RDL via enclosure by TM2/STM2 for stack via	≥	0.60	um
SV.7	RDL via enclosure by RDL for stacked via	≥	0.60	um
SV.8	RDL via width and length	≥	1.50	um





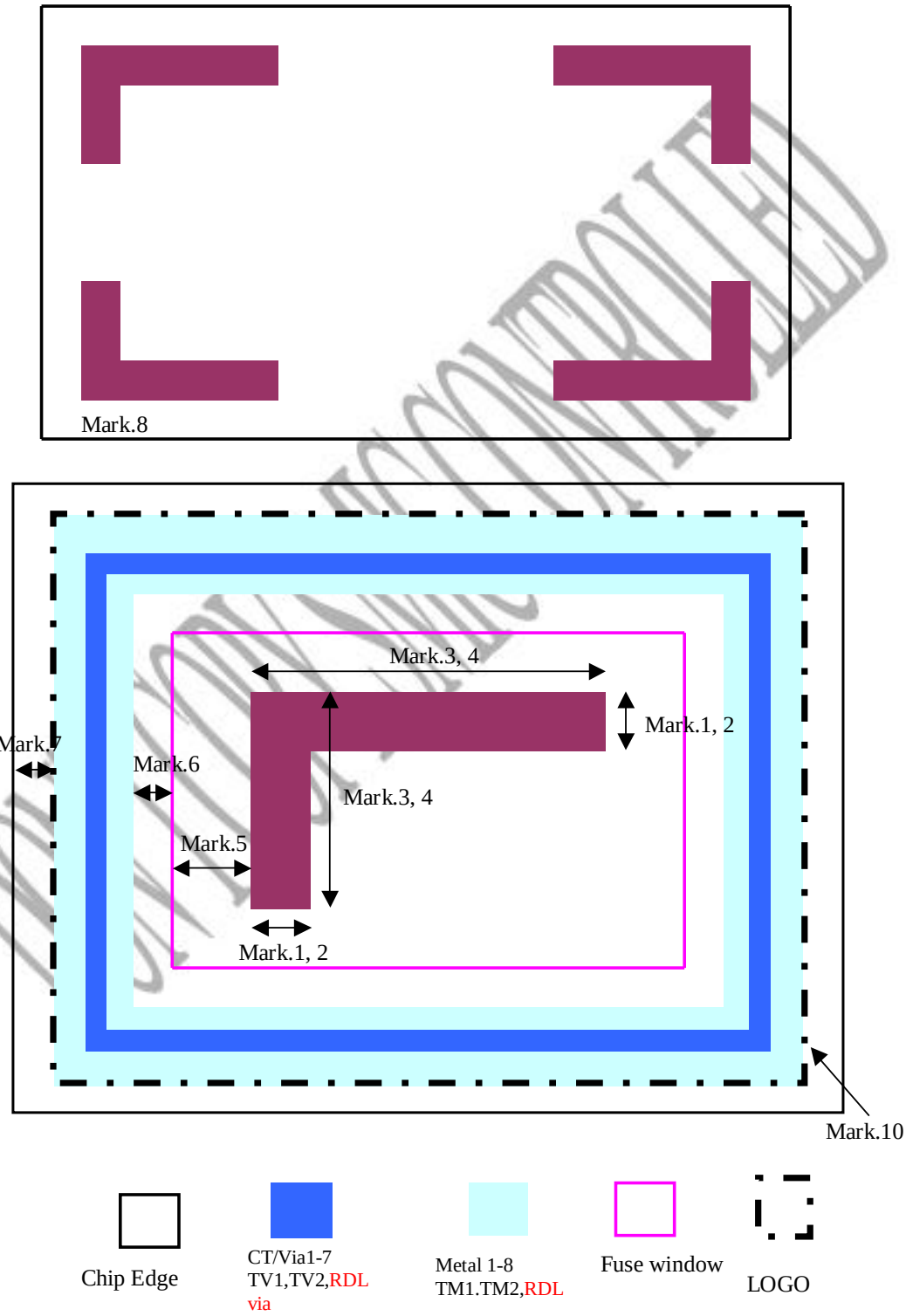
7.2.34.10.3 Fuse window design rules

"Fuse" layer is recommended as drawing layer for Fuse window definition.

Rules number	Description	Operation	Design Value	Unit
Fuse.1	Fuse window width	≥	5.00	um
Fuse.2	Fuse window length	≥	20.00	um
Fuse.3	Space between fuse window and guard ring	≥	1.50	um
Fuse.4	Space between fuse edge and fuse window	≥	3.50	um

7.2.34.11 Fuse repairing alignment mark guidelines

Items	DESCRIPTION	Operation	Design Value	Unit
Mark.1	L mark minimum width	≥	10.00	um
Mark.2	L mark maximum width	≤	20.00	um
Mark.3[NC]	L mark minimum length	≥	30.00	um
Mark.4	L mark maximum length	≤	50.00	um
Mark.5	Space between L mark and FUSE window	≥	10.00	um
Mark.6	Space between FUSE window and guard ring	≥	1.50	um
Mark.7[NC]	Space between guard ring and chip edge	≥	7.00	um
Mark.8[NC]	L mark should be on each corner of a chip			
Mark.9[NC]	L mark metal layer is fuse metal (RDL layer is recommended as drawing layer if Al fuse is used.)			
Mark.10[NC]	LOGO layer is needed for Lmark area definition, the recommended size is same as guard ring edge			
Mark.11[NC]	Guard ring rule refer to 7.2.34.9			
Mark.12[NC]	No AA/ploy/metal dummy patterns are allowed in "L mark" area. Please use "dummy block" layer for this area. The dummy block layer size is same as guard ring edge			



7.2.34.12 Logo layout guidelines[NC]

Logo patterns include company logo, numbers, mask names and other similar labels. Minimum fix-sized squares are recommended for logo pattern formation at contact/via layers. CT and via polygons are not allowed for logo formation. Dummy block layers are recommended to be drawn around logo areas if designer does not hope to have automatic dummy insertion on those areas.

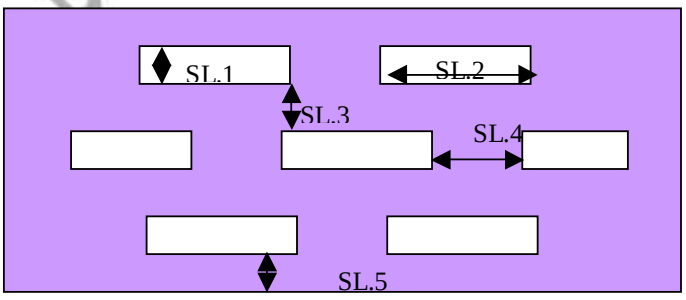
7.2.34.13 Metal slot rules guidelines[NC]

All metal layer slot insertion must follow these rules except top metal bonding area. Consult SMIC process integration for risk assessment if device layout needs design rule violation waiver.

The metal slots must be placed for wide metal lines greater than maximum width allowed at each layer. Top metal bondpads can be waived.

Items	Descriptions	Operation	Design Value	Unit
SL.1	Slot width	≥	1	um
SL.2	Slot length	≥	0.8	um
SL.3	Space between two parallel open slots	≤	5.0	um
SL.4	Space between two open slots in a coaxial line	≤	2.0	um
SL.5	Distance between any open slot to the metal edge	≥	2.0	um
SL.6	Distance between open slot edge and contact or vias	≥	0.5	um
SL.7	The length of the slot should be parallel to current flow direction at this layer			
SL.8	Slot density of wide metal	≥	10%	
SL.9	Metal slots should be drawn with the GDS No. of corresponding metal layers (61;0, 62;0 …).			

Notes: uniform slot pattern is recommended. Please try to avoid irregular pattern to slot metal.



7.2.35 Current Density Rule

7.2.35.1 Current density rule for non-salicide poly resistor

The table below listed Jmax: DC current allowed per μm of poly line at 110℃

non salicide resistor	Operation	Jmax (DC)	Unit
N+ non-salicide Poly resistor	≤	0.3	mA/um
P+ non-salicide Poly resistor	≤	0.3	mA/um

Note: Non-salicide poly current density is not sensitive to temperature.

7.2.35.2 Current density rule for Cu metal

The table below listed Jmax:DC current allowed per μm of metal line at 110℃

Mx layer	Operation	Jmax (DC)	Unit
M1	≤	1.6	mA/um
M2	≤	1.9	mA/um
M3	≤	1.9	mA/um
M4	≤	1.9	mA/um
M5	≤	1.9	mA/um
M6	≤	1.9	mA/um
M7	≤	1.9	mA/um
M8	≤	1.9	mA/um
TM1(4X TM)	≤	8.1	mA/um
STM1(2X TM)	≤	2.8	mA/um
TM2 (4X TM)	≤	8.1	mA/um
STM2 (2X TM)	≤	2.8	mA/um
TM2 for MTT2	≤	27	mA/um

7.2.35.3 Current density rule (DC) for contact/via

The table below listed Jmax: DC current allowed per contact or via at 110℃. UTV2 will share the same current density rule as 4X TV2.

Contact or Via layers	Operation	Jmax (DC)	Unit
Contact	≤	0.3	mA/Count
Via1	≤	0.16	mA/Count
Via2	≤	0.16	mA/Count
Via3	≤	0.16	mA/Count
Via4	≤	0.16	mA/Count
Via5	≤	0.16	mA/Count
Via6	≤	0.16	mA/Count
Via7	≤	0.16	mA/Count
TV1 (for 4X TV1)	≤	3.2	mA/Count
STV1 (for 2X STV1)	≤	0.99	mA/Count
TV2(for 4X TV2 or UTV)	≤	3.2	mA/Count
STV2(for 2X STV2)	≤	0.99	mA/Count

7.2.35.4 Current density rule (DC) for stacked contact/via

The table below listed Jmax:DC current allowed per stacked contact or via at 110℃. UTV2 will share the same current density rule as 4X TV2.

Stacked Via layers	Operation	Jmax(DC)	Unit
Stacked V1/V2	≤	0.16	mA/Count
Stacked V1/V2/V3	≤	0.16	mA/Count
Stacked V1/V2/V3/V4	≤	0.16	mA/Count
Stacked V1/V2/V3/V4/V5	≤	0.16	mA/Count
Stacked V1/V2/V3/V4/V5/V6	≤	0.16	mA/Count
Stacked V1/V2/V3/V4/V5/V6/V7	≤	0.16	mA/Count
Stacked V1/V2/V3/V4/V5/V6/V7/TV1 or V1/V2/V3/V4/V5/V6/V7/STV1	≤	0.16	mA/Count
Stacked V1/V2/V3/V4/V5/V6/V7/TV1/TV2 or V1/V2/V3/V4/V5/V6/V7/STV1/STV2	≤	0.16	mA/Count
Stacked V2/V3	≤	0.16	mA/Count
Stacked V2/V3/V4	≤	0.16	mA/Count
Stacked V2/V3/V4/V5	≤	0.16	mA/Count
Stacked V2/V3/V4/V5/V6	≤	0.16	mA/Count
Stacked V2/V3/V4/V5/V6/V7	≤	0.16	mA/Count
Stacked V2/V3/V4/V5/V6/V7/TV1 or V2/V3/V4/V5/V6/V7/STV1	≤	0.16	mA/Count
Stacked V2/V3/V4/V5/V6/V7/TV1/TV2 or V2/V3/V4/V5/V6/V7/STV1/STV2	≤	0.16	mA/Count
Stacked V3/V4	≤	0.16	mA/Count
Stacked V3/V4/V5	≤	0.16	mA/Count
Stacked V3/V4/V5/V6	≤	0.16	mA/Count
Stacked V3/V4/V5/V6/V7	≤	0.16	mA/Count
Stacked V3/V4/V5/V6/V7/TV1 or	≤	0.16	mA/Count

V3/V4/V5/V6/V7/STV1			
Stacked V3/V4/V5/V6/V7/TV1/TV2 or V3/V4/V5/V6/V7/STV1/STV2	≤	0.16	mA/Count
Stacked V4/V5	≤	0.16	mA/Count
Stacked V4/V5/V6	≤	0.16	mA/Count
Stacked V4/V5/V6/V7	≤	0.16	mA/Count
Stacked V4/V5/V6/V7 /TV1 or V4/V5/V6/V7 /STV1	≤	0.16	mA/Count
Stacked V4/V5/V6/V7 /TV1/TV2 or V4/V5/V6/V7 /STV1/STV2	≤	0.16	mA/Count
Stacked V5/V6 at 110℃	≤	0.16	mA/Count
Stacked V5/V6/V7 at 110℃	≤	0.16	mA/Count
Stacked V5/V6/V7/TV1 or V5/V6/V7/STV1	≤	0.16	mA/Count
Stacked V5/V6/V7/TV1/TV2 or V5/V6/V7/STV1/STV2	≤	0.16	mA/Count
Stacked V6/V7	≤	0.16	mA/Count
Stacked V6/V7/TV1 or V6/V7/STV1	≤	0.16	mA/Count
Stacked V6/V7/TV1/TV2 or V6/V7/STV1/STV2	≤	0.16	mA/Count
Stacked V7/TV1 or V7/STV1	≤	0.16	mA/Count
Stacked V7/TV1/TV2 or V7/STV1/STV2	≤	0.16	mA/Count
Stacked TV1/TV2	≤	3.2	mA/Count
Stacked STV1/STV2	≤	0.99	mA/Count
Stacked STV1/TV2	≤	0.99	mA/Count

7.2.35.5 Maximum DC current under different temperatures for Cu metal and via/contact:

The below table includes Jmax: DC current under different temperature for metal and via/contact:

70℃: 8.54 x (corresponding value under 110℃)
85℃: 5.20 x (corresponding value under 110℃)
100℃: 2.14 x (corresponding value under 110℃)
125℃: 0.547 x (corresponding value under 110℃)

7.2.35.6 Current density rules (DC) for RDL and RDL Via

Below table lists Jmax: DC current of RDL (both 14.5K and 28K options) per um and RDL via per via number at 110℃.

RDL/RDL via	Operation	Jmax (DC)	Unit
RDL (14.5K)	≤	2.74	mA/um
RDL (28K)	≤	5.2	mA/um
RDL via(3umX3um)	≤	8	mA/Count

Below table lists maximum DC current under different temperature for RDL (both 14.5K and 28K options) and RDL via.

70℃: 3.4 x (corresponding value under 110℃)
85℃: 2.1 x (corresponding value under 110℃)
100℃: 1.3 x (corresponding value under 110℃)
125℃: 0.67 x (corresponding value under 110℃)

7.2.35.6 Current density rule (AC) for Cu metal layers

The below table lists the maximum Irms allowed for each of the metal lines of 1P8M (2TM)at 110℃. If designer would like to use M7 and M8, please refer to M6 layer.
W (in μm) : the width of the metal line
ΔT (℃): the temperature rise due to Joule heating

Mx layer	Operation	Jmax(AC)	Unit
M1	≤	SQRT[ΔT*(11.69*w^2+22.79*w]	mA
M2	≤	SQRT[ΔT*(5.63*w^2+5.79*w]	mA
M3	≤	SQRT[ΔT*(3.94*w^2+8.10*w]	mA
M4	≤	SQRT[ΔT*(3.01*w^2+4.04*w]	mA
M5	≤	SQRT[ΔT*(2.39*w^2+6.25*w]	mA
M6	≤	SQRT[ΔT*(1.86*w^2+6.60*w]	mA
TM1(for 4X TM)	≤	SQRT[ΔT*(4.95*w^2+37.79*w]	mA
TM2 (for 4X TM)	≤	SQRT[ΔT*(4.44*w^2+25.34*w]	mA
TM2 (for MTT2)	≤	SQRT[ΔT*(7.71*w^2+113.53*w]	mA

7.2.36 SMIC DFM rules

Introduction:
Notice that not every design rule has its DFM rule. Also note that there are DFM rules standing out on their own and do not pair with any design rules
This document has DFM rules based on silicon data. We have used the following methods to generate the rules:
(1) Characterization of dimension rules based on SMIC's utilities that generate shapes, contours, and patterns that match silicon process variations of our fabs;
(2) Device performance variability analysis based on the results in (1);
(3) Reliability variability analysis based on the results in (1);
(4) Timing analysis including signal integrity based on the results in (1).

We have also put the DFM rules in different priority levels. Higher priority indicates higher risk of manufacturability and yield damages when the rule is not obeyed. The "DFM Rules Description" section states how to execute DFM rule checking according to the priority levels.
SMIC recommends that all of the DFM rules in this section are followed. If designers decide to follow the recommendation and run DRC checks on the DFM rules, they should follow the Priority 1 rules requirements.

Rule No.	Enhanced Rule Description	Priority	Affected	DFM Rule (um)	Design Rule (um)	Design Rule Number
DFM1a	Space between L-shape AA to GT in the same MOS (channel width>=0.16)	1	device	≥0.07	0.05	GT.4
DFM1b	Space between L-shape AA to GT in the same MOS (channel width<0.16)	1	device	>=0.1	0.05	GT.4
DFM2a	Space between L-shape GT to AA in the same MOS(channel width>=0.16)	1	device	≥0.07	0.05	GT.4
DFM2b	Space between L-shape GT to AA in the same MOS (channel width<0.16)	1	device	>=0.1	0.05	GT.4
DFM3	(Purposely blank)					
DFM4	Via (Vn, TV1) insertion, n=1~7	1	Process, reliability	Insert one Vn if single Vn and (Wn>=5Wn+1, or Wn+1>=5Wn) at enclosure	N/A	N/A
DFM5	Maximum length of parallel metal (Mn, n=1~7) lines with	1	Signal integrity	25	N/A	N/A

	metal (Mn, n=1~7) lines with minimum spacing Designer can waive the violations if design passes sign-off-level signal integrity check.		integrity			
DFM6	Single CT enclosure by M1	2	process	≥0.005	0	CT.7a
DFM7	(Purposely blank)					
DFM8	(Purposely blank)					
DFM9	Single Vn enclosure by Mn n = 2,3,4,5,6,7	2	process	≥0.025	0.005	Vn.3a
DFM10	Mn line-end extension outside of Vn n = 1,2,3,4,5,6,7	2	process	≥0.04	0.03	Vn.3b
DFM11	Single Vn enclosure by Mn+1 n = 1,2,3,4,5,6,7	2	process	≥0.025	0.005	Vn.5a
DFM12	Mn+1 line-end extension outside of Vn n = 1,2,3,4,5,6,7	2	process	≥0.03	0.02	Vn.5b
DFM13	Mn, TM1 jog/notch size n=1~8	2	Process, OPC	Notch size>=min width of the layer	N/A	N/A
DFM14	(Purposely blank)					
DFM15	See below attached picture	2				
DFM16	(Purposely blank)					
DFM17	(Purposely blank)					
DFM18	See below attached picture	2				
DFM19	Local AA density (including dummy): Density check window size 200um*200um, step size: 100um	1	Process	Min 30% Max 70%	Min 23% Max 75%	AA.10a
DFM20	Local GT density (including dummy): Density check window	1	Process	Min 15%	Min 7%	GT.7a

	size 200um*200um, step size 100um			Max 65%	Max 70%	
DFM.21	For parallel long NW (length > 50um), must make NW width larger than 1.07um or NW to NW space larger than 1.07um	1	Process	≥1.07	N/A	N/A
DFM22	(purposely blank)					
DFM23	Space between 1.0/1.2V NWs at different nets	2	Device	1.0	0.47	NW.4
DFM24	Space between 1.0/1.2V NW and 1.8/2.5/3.3V NW at different nets	2	Device	1.2	0.72	NW.6
DFM25	Space between 1.8/2.5/3.3V NWs at different nets.	2	Device	1.2	0.72	NW.7
DFM26a	Channel width for 1.0/1.2V NMOS/PMOS transistors	2	Device	0.12	0.11	AA.2a
DFM26b	Channel width for 1.8/2.5/3.3V NMOS/PMOS transistors	2	Device	0.4	0.21	AA.2b
DFM27a	Space between AAs that are on the same well	2	Device	0.11	0.1	AA.3a
DFM27b	Space between AAs with one or both AA width greater than 0.15um that are on the same well	2	Device	0.13	0.11	AA.3b
DFM28	N+AA enclosure by NW	2	Device	0.16	0.12	AA.4
DFM29	Space between NW and N+AA	2	Device	0.16	0.15	AA.5
DFM30	P+AA enclosure by NW	2	Device	0.16	0.15	AA.6
DFM31	Space between NW to P+AA inside PW	2	Device	0.16	0.12	AA.7
DFM32	AA area (in um^2)	2	Process	0.054	0.038	AA.8
DFM33	NW width	2	Process	0.47	0. 36	NW.1
DFM34	Space between 1.0/1.2V NWs at same potential	2	Device	0.47	0. 36	NW.3
DFM35	Space between 1.0/1.2V NWs at	2	Device	1	0.47	NW.4

	different potential.					
DFM36	Space between 1.0/1.2V NW and 1.8/2.5/3.3V NW	2	Device	1.2	0.72	NW.6
DFM37	Space between 1.8/2.5/3.3V NWs	2	Device	1.2	0.72	NW.7
DFM38	NW area (um^2)	2	Process	1.2	0.3	NW.8
DFM39	PSUB width	2	Process	0.47	0.36	PSUB.1
DFM40a	2.5V (or overdrive to 3.3V) NMOS channel length	2	Device	1.2	1	PSUB.3c
DFM40b	3.3V NMOS channel length	2	Device	?	1.2	PSUB.3d
DFM41	Space between PSUBs with same potential	2	Device	0.47	0.36	PSUB.4
DFM42	MOS AA enclosure by PSUB	2	Device	=0.26	0.26 (fixed)	PSUB.5
DFM43	Extension of native NMOS poly gate outside of AA	2	Device	0.35	0.31	PSUB.8
DFM44	VTNH extension outside of MOS AA along gate poly length direction.	2	Process	0.16	0.12	VTNH.4
DFM45	Space between VTNH and MOS AA of other device along other device's gate poly length direction	2	Device	0.16	0.12	VTNH.5
DFM46	VTNH area	2	Process	0.27	0.18	VTNH.8
DFM47	VTPH extension outside of MOS AA along gate poly length direction.	2	Process	0.16	0.12	VTPH.4
DFM48	Space between VTPH and MOS AA of other device along other device's gate poly length direction	2	Device	0.16	0.12	VTPH.5
DFM49	VTPH area	2	Process	0.27	0.18	VTPH.8
DFM50	LVN extension outside of MOS AA along gate poly length direction.	2	Process	0.16	0.12	LVN.4

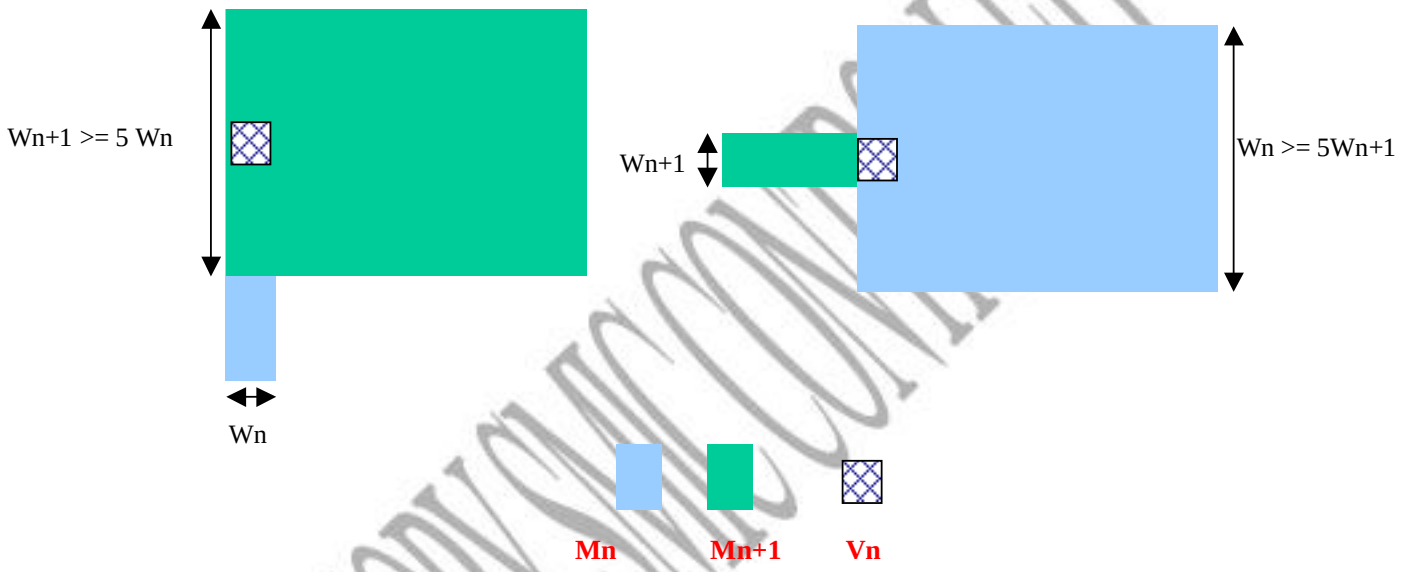
DFM51	Space between LVN and MOS AA of other device along other device's gate poly length direction	2	Device	0.16	0.12	LVN.5
DFM52	LVN area	2	Process	0.27	0.18	LVN.8
DFM53	Space between DG and MOS AA	2	Device	0.27	0.25	DG.5
DFM54	Space between DG and transistor gate poly (1.2/2.5/3.3) along source/drain direction.	2	Device	0.27	0.24	DG.6
DFM55	(purpose blank)					
DFM56	Space between TG and MOS AA	2	Device	0.27	0.25	TG.5
DFM57	Space between TG and 1.2/1.8V transistor gate poly along source/drain direction.	2	Device	0.27	0.24	TG.6
DFM58	(purpose blank)					
DFM59	Space between GTs	2	Device	G: 0.13, Recm 0.2 G1: CD>0.09, 0.15 H: IO=0.25	0.12	GT.3a
DFM60	Space between AA and GT on field oxide	2	Process	K: 0.1 for w<0.15 xtor	0.05	GT.4
DFM61	Extension of AA outside of GT(not include dummy AA and dummy Poly)	2	Process	P: 0.115 recom 0.18	0.115	GT.5
DFM62	Min. GT island area	2	Process	0.042	0.038	GT.13
DFM63	LDMOS gate length	2	Device	0.48	0.48	LD.1a
DFM64	STI width for LDMOS transistor drain side field plate	2	Device	0.11	0.11	LD.2
DFM65	Overlap of NW and LDNMOS gate	2	Device	0.2	0.2	LD.3
DFM66	Overlap of PW and LDPMOS gate	2	Device	0.2	0.2	LD.4

DFM67	GT to STI drain side field plate overlap	2	Device	0	0	LD.9
DFM68	Dummy layer STIDMY is required for LDMOS transistor field plate area; STIDMY enclosure LDMOS drain side filed plate	2	Process	0	0	LD.11
DFM69	Space between SN and P+ AA inside NW	2	Device	0.13	0.1	SN.3
DFM70	SN extension outside of Poly gate for NMOS along source/drain direction.	2	Device	0.32	0.24	SN.6
DFM71	Space between SN and poly gate for PMOS along source/drain direction.	2	Device	0.32	0.24	SN.5
DFM72	SN extension outside of NMOS AA along gate poly length direction, if the distance to the related poly is larger than 0.20um	2	Process	0.13	0.12	SN.7
DFM73	SN and AA overlap	2	Device	0.13	0.09	SN.10
DFM74	SN area (um^2)	2	Process	0.122	0.1	SN.11
DFM75	Space between SP and N+ AA inside P well	2	Device	0.13	0.1	SP.3
DFM76	Space between SP and N-channel poly gate along source/drain direction.	2	Device	0.32	0.24	SP.5
DFM77	SP extension outside of PMOS poly gate along source/drain direction..	2	Device	0.32	0.24	SP.6
DFM78	SP extension outside of PMOS AA along gate poly length direction, if the distance to the related poly is larger than 0.20µm	2	Process	0.13	0.12	SP.7
DFM79	SP and AA overlap	2	Device	0.13	0.09	SP.10
DFM80	SP area (um^2)	2	Process	0.122	0.1	SP.11

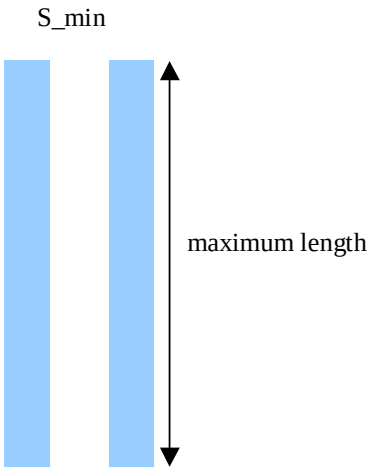
DFM81	SAB width	2	Process	0.43	0.4	SAB.1
DFM82	Space between SABs	2	Process	0.43	0.4	SAB.2
DFM83	Extension of related AA outside of SAB	2	Process	0.22	0.2	SAB.3
DFM84	Space between SAB and AA	2	Device	0.22	0.2	SAB.4
DFM85	Space between SAB and GT on AA	2	Device	0.38	0.36	SAB.5
DFM86	Extension of SAB outside of poly on field oxide	2	Process	0.22	0.2	SAB.6
DFM87	Space between SAB and CT	2	Device	0.22	0.2	SAB.7
DFM88a	Extension of SAB outside of AA	2	Process	0.22	0.2	SAB.8
DFM88b	Extension of SAB outside of AA when AA width>10um	2	Process	0.3	0.2	SAB.8
DFM89	SAB area (um^2)	2	Device	1	0.5	SAB.10
DFM90	Space between SAB and poly on field oxide.	2	Device	0.3	0.28	SAB.11
DFM91	Space between two contacts in case contact array is larger or equal to 4x4. Two contact regions whose space is <=0.15µm are considered to be in the same array.	2	Device	0.12/0.14	0.13	CT.2b
DFM92	Space between AA and contact on poly	2	Device	0.07	0.065	CT.3
DFM93a	Space between poly and contact on AA for 1.0V/1.2V	2	Device	0.055	0.05	CT.4a
DFM93b	Space between poly and contact on AA for 1.8/2.5/3.3V	2	Device	0.11	0.09	CT.4b
DFM94	CT enclosure by AA for CT landed on AA	2	Process	AA w>0.2=0.015 AA w<0.2=0.03 Recomm=0.06	0.015	CT.5

DFM95	M1 enclosure of CT when the M1 length along CT is >=0.3um	2	Process	>=0.035	0.025	CT.7b
DFM96	Space between two M1s having parallel segment >0.5um with one or both M1 width>0.2um	2	Process	>0.11um		
DFM97	Space between two M1s having parallel segment >0.5um with one or both M1 width>0.5um	2	Process	>0.13um		
DFM98	Space between two Mns having parallel segment >0.5um with one or both Mn width>0.2um	2	Process	>0.11um		
DFM99	Space between two Mns having parallel segment >0.5um with one or both Mn width>0.5um	2	Process	>0.13um		
DFM100	Vn enclosure by Mn+1 or Mn-1 if Mn+1/Mn-1 length along via is >= 0.3um	2	Process	0.035	0.02	Vn.5b
DFM101	Maximum parallel metal line width allowed without slot	2	Process	4	12	M1.3
DFM102	Slot density of wide metals Density check window size: 100um* 100um, step size:50um	2	Process	>=15%	>=10%	SL.8
DFM103	Space between Vn and unconnected Mn+1(two metal lines are perpendicular to one another)	2	process	>=0.12um		
DFM104	M1 enclosure of CT when M1 enclosure on one or both perpendicular directions<0.035um	1	Process	>=0.035	0.025	CT.7b

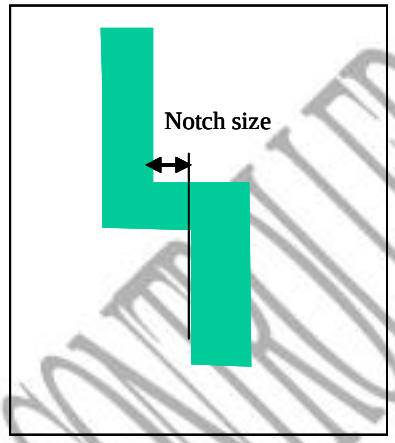
DFM4 Via (Vn, TV1) insertion,
n=1~7



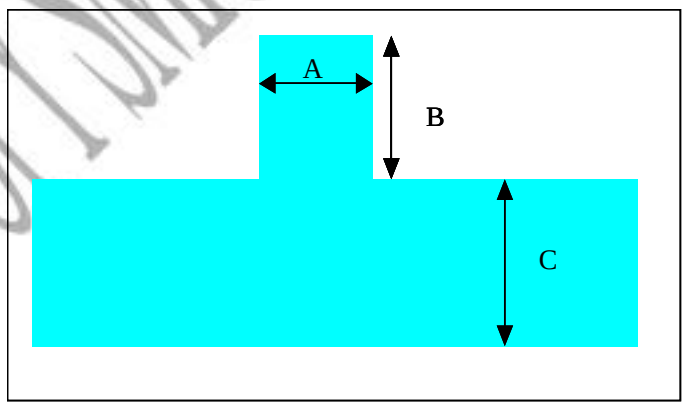
DFM5 Maximum length of parallel metal
(Mn, n=1~7) lines with minimum spacing



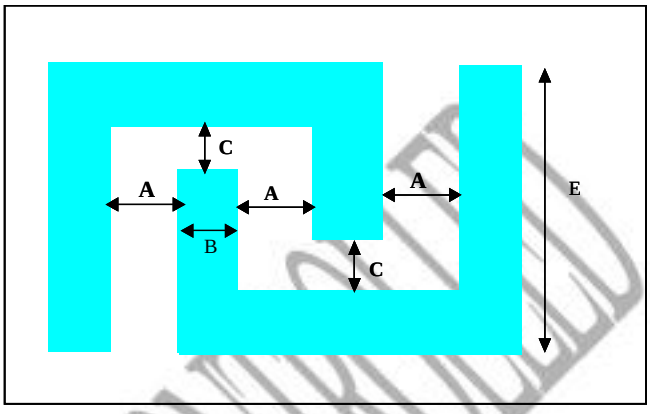
DFM13 Mn, TM1 jog/notch size (n=1~8)



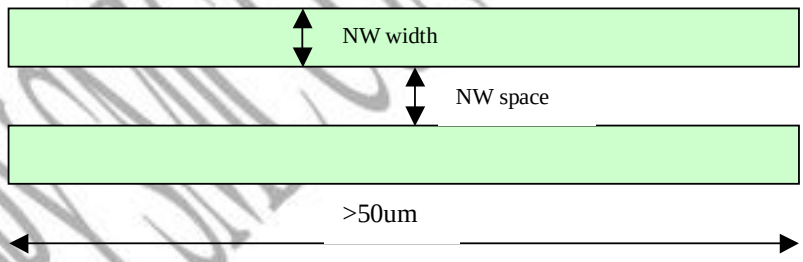
DFM15 (Priority 2) M1
Nubs
When B>=0.1, A should >=0.16



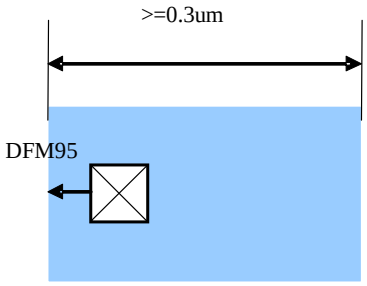
DFM18 (Priority 2) M1
Horse shoe
A=C>=120 when B>=120



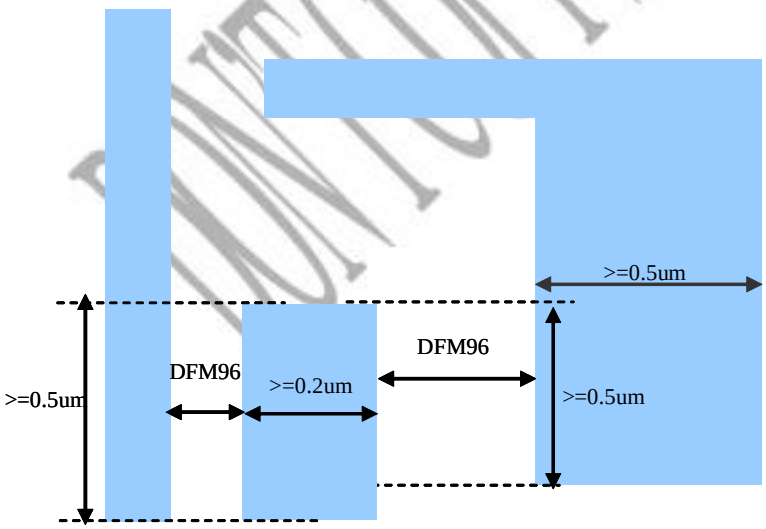
DFM21 (priority 1) For parallel long NW (length > 50um), must make NW width larger than 1.07um or NW to NW space larger than 1.07um



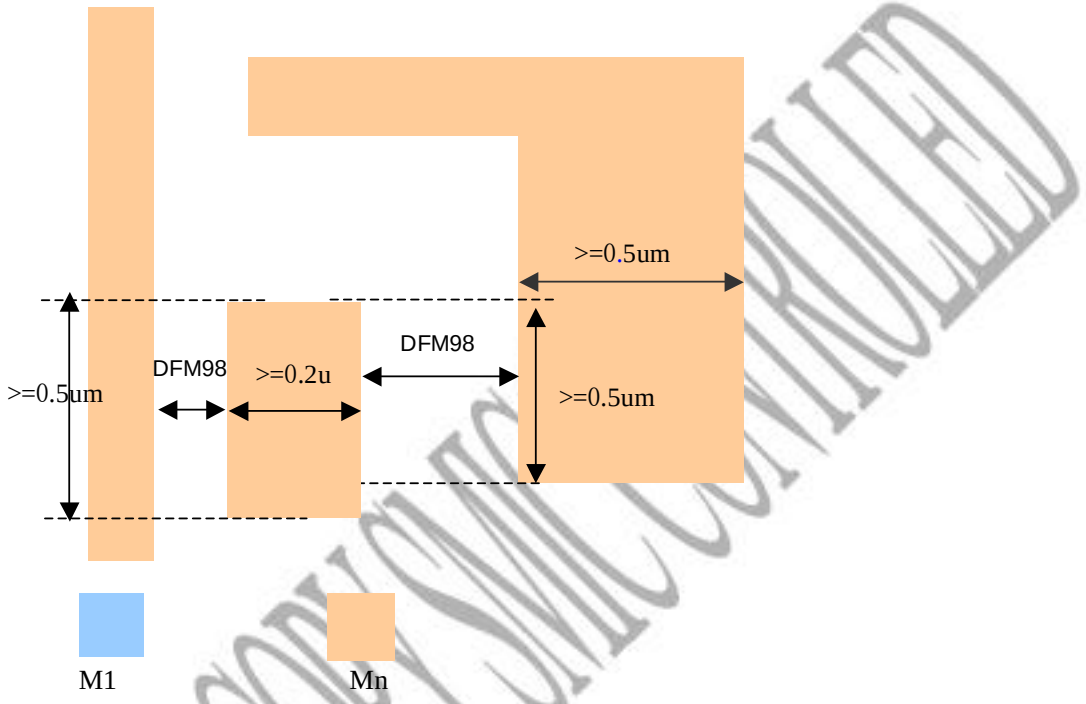
DFM95: M1 enclosure of CT should be larger than or equal to 0.035um whenM1 length along CT is >= 0.3um.



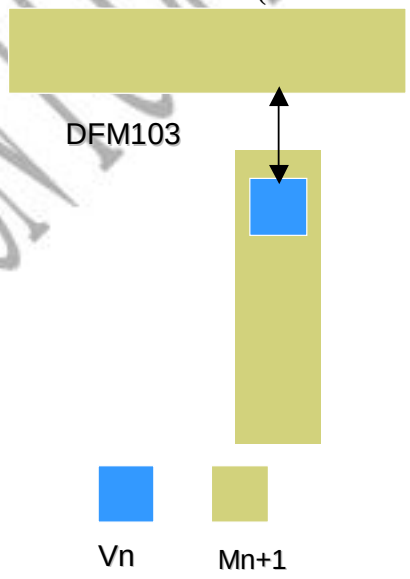
DFM96: Space between two M1s having parallel segment >0.5um with one or both M1 width>0.2um is larger than 0.13um



DFM98: Space between two Mns having parallel segment >0.5um with one or both Mn width>0.2um is larger than 0.11um



DFM103: Space between Vn and unconnected Mn+1(two metal lines are perpendicular to one another)>=0.12um



8.Attachment

1. SealRing_SMIC_20120210.gds
2. 65nm Metallization Options Table Excel for 7.1.7