SC8, SC9, and SC12 Standard Cell Libraries User Guide

Revision: 2008q3v1.0

For 45nm and Smaller Process Nodes

Released on: **September 2008**

ARM®

SC8, SC9, and SC12 Standard Cell Libraries User Guide
For 45nm and Smaller Process Nodes

Release Information

The following changes have been made to this book.

Release History

Part Number	Release Number	Date of Release	Updates
SC-UG-BASE-45nm	2008q3v1.0	September 2008	Initial release

Proprietary Notice

Confidentiality Status

This document is Non-Confidential. The right to use, copy and disclose this document may be subject to license restrictions in accordance with the terms of the agreement entered into by ARM and the party that ARM delivered this document to.

Product Status

The information in this document is final, that is for a developed product.

Web Address

`http://www.arm.com`

Contents
SC8, SC9, and SC12 Standard Cell Libraries User Guide
For 45nm and Smaller Process Nodes

Preface

ARM welcomes feedback on both the Standard Cell Library and its documentation.

Feedback

Please use the following sections to provide feedback.

Feedback on this book

If you have any comments on this book, please provide the following information:

- the document title
- the document number
- the document revision
- the page number(s) to which your comments apply
- a concise explanation of your comments.

General suggestions for additions and improvements are also welcome.

Feedback on the Standard Cell Library

If you have any problems with the Standard Cell Library, please provide the following information:

- a clear explanation of what is expected and what is observed
- the commands you used, including any command-line options
- sample output illustrating the problem
- version of EDA tool that is showing the problem with the actual error message.

Contact Information

For general questions related to ARM Physical IP product availability and their licensing requirements, customers can go to http://access.arm.com. Log in and click on the "Products and Services > New Business Request" link to enter a request.

Customers with active Support contracts can obtain support for ARM Physical IP products by going to http://access.arm.com and clicking on "Products and Services > New Technical Request." Support contract options are available for review at www.arm.com/products/physicalip/support.html.

You may also contact ARM by email: support-artisan@arm.com.

Introduction

This document outlines cells contained in multiple libraries. Descriptions are provided for cells that may not be included in your library. For details specific to your library, see the Technical Overview section of your databook.

ARM 45nm and smaller standard cell libraries build upon years of experience with multiple standard cell architectures. The cell line for each is derived from extensive customer design, synthesis, and place-and-route benchmark analysis. Library optimization is achieved by carefully matching the library functions and drive strengths to leading synthesis and place-and-route tools, producing superior RTL-to-GDSII results. SC9 libraries offer an optimal mix of performance, power, and area, ideal for mainstream applications. The ARM SC12 are high speed libraries targeting performance-critical designs while still optimizing power. SC8 libraries are optimized for high density, low-power applications. This user guide presents information for SC8, SC9, and SC12 libraries.

ARM also makes available a family of Multi-Channel libraries. ARM Multi-Channel (MC) libraries are an advanced solution for leakage power reduction of complex SoC designs. The libraries provide a family of cell sets that use transistors with different channel lengths and enable an optimization between leakage power and performance. By using gates that are built from transistors with long channels, leakage of of the gates is drastically reduced. All gates with longer channels have a reduced speed compared to gates with minimum channel lengths. The actual channel lengths are indicated in the library name with “Cxx”; larger “xx” numbers indicate larger channel length transistors with reduced leakage and performance. Different channel lengths can be combined with different Vt options, enabling either an additional leakage reduction compared to HVt devices or the replacement of HVt devices.

All MC libraries for a given process node and standard cell track height are footprint compatible; this enables a design flow for leakage – performance optimization similar to a mixed Vt design flow. MC libraries can be combined with the ARM MC Power Management Kit (PMK) for further active dynamic and leakage reduction.

1.1 How This Book is Organized

This user guide is organized into three sections:

- *Global Parameters* provides an overview of parameters that may be included with your library. Refer to the Technical Overview provided in the accompanying databook for values specific to your library.
- *Special Cells* details the types of special cells that may be included in your library. Descriptions of cells not included with your library are additional options available from ARM.
- *Library Naming Conventions* outlines the naming conventions used in the standard cell library.

1.2 Global Parameters

This section discusses global parameters that may be included with this library. Refer to the Technical Overview in your databook for values specific to your library. Descriptions of cells not included with your product are additional options available from ARM.

Note

For any shrink processes, *all* area numbers in the library and documentation are ***pre-shrink***. All performance numbers in the library and documentation are post-shrink.

1.2.1 Propagation Delays

The propagation delay through a cell is the sum of the intrinsic delay, the load-dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the rising time percentage of Vdd and the output crossing the falling time percentage of Vdd. Libraries are usually characterized with delays at either 50% rising time/50% falling time or 40% rising time/60% falling time. For comparison, illustrations are provided for both 50/50 and 40/60. Refer to the Technical Overview in your databook for values specific to your library.

Figure 1 illustrates the propagation delay at 50/50.

Figure 1 Propagation Delays at 50/50

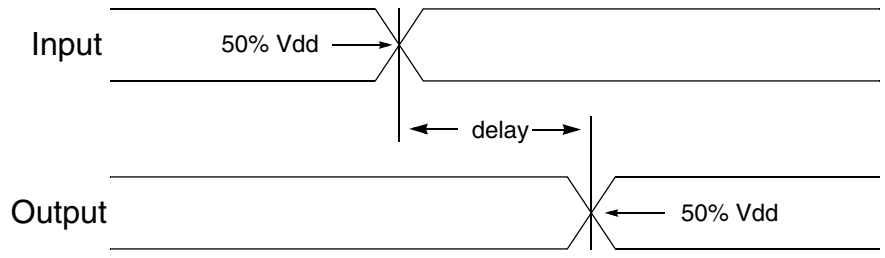
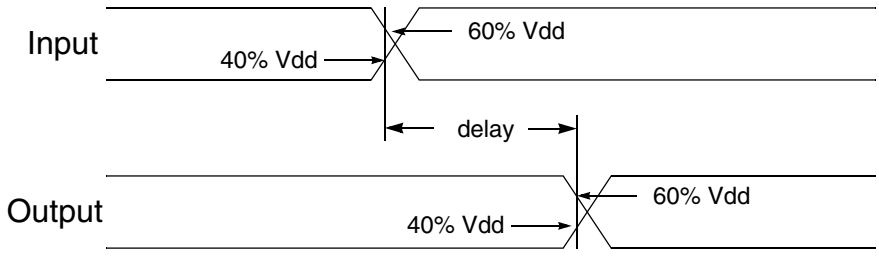


Figure 2 illustrates the propagation delay at 40/60.

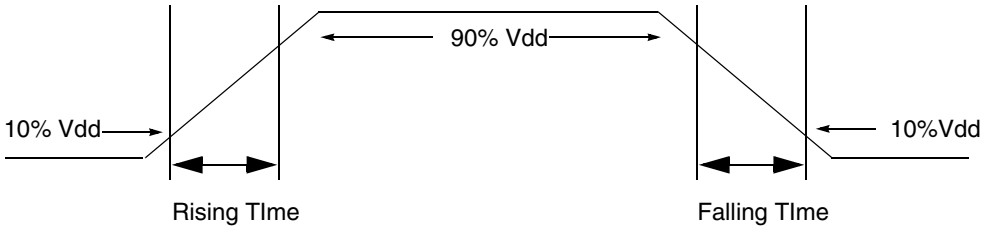
Figure 2 Propagation Delays at 40/60



The transition times (slews) on input and output pins are defined as the time interval between the signal crossing 10% of Vdd and 90% of Vdd.

Figure 3 illustrates transition time measurements for rising and falling signals.

Figure 3 Transition Time



Factors that affect propagation delays and transition time include: temperature, supply voltage, process variations, fanout loading, interconnect loading, input-transition time, input-signal polarity, and timing constraints. The timing models provided with this library include the effects of input-transition time on propagation delays. Also, NLDM timing models use a table lookup method to calculate accurate timing. The standard cell datasheets provide all timing numbers for the input slew specified in the Technical Overview accompanying your datasheets. All cells have been characterized with a physical overlay to more closely resemble a cell placed in a block for accurate characterization. Refer to the Technical Overview in your databook for values specific to your library.

The library may contain negative propagation delays. Although most third-party verification tools can handle negative propagation delays, some tools will turn negative delays into a zero value.

1.2.2 Timing Constraints

Timing constraints define minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing constraints include: setup time, hold time, recovery time, removal time, and minimum pulse width. The sequential-cell timing models provided with the library include the effects of input-transition time and data-signal and clock-signal polarity on timing constraints. Factors that affect timing constraints include temperature, supply voltage, slew rates, horizontal and vertical pitch, and process case variations. All cells have been characterized with a physical overlay to more closely resemble a cell placed in a block for accurate characterization. Refer to the Technical Overview in your databook for values specific to your library. Timing constraints can affect propagation delays. The intrinsic delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, and pulse widths). The use of shorter timing constraint intervals may increase delay. Each cell is considered functional as long as the actual delay does not exceed the delay given in the datasheets by more than 10%.

1.2.3 Setup Time

The setup time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%. Setup-constraint values are measured as the interval between the data signal crossing rising time% of Vdd for rising data (or falling time% of Vdd for falling data) and the clock signal crossing rising time% of Vdd for rising clocks (or falling time% of Vdd for falling clocks). Libraries are usually characterized with delays at either 50% rising time/50% falling time or 40% rising time/60% falling time. Refer to the Technical Overview in your databook for values specific to your library. For comparison, illustrations are provided for both 50/50 and 40/60 delays. For the measurement of setup time, the data input signal is kept stable after the active clock edge for an infinite hold time.

Figure 4 illustrates setup time for a positive-edge-triggered sequential cell with delays at 50/50.

Figure 4 Setup Time with Delays at 50/50

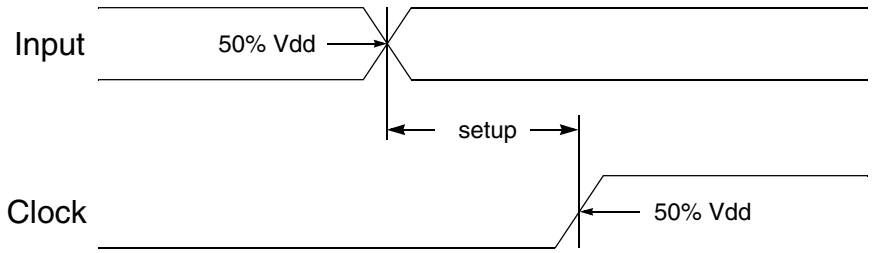
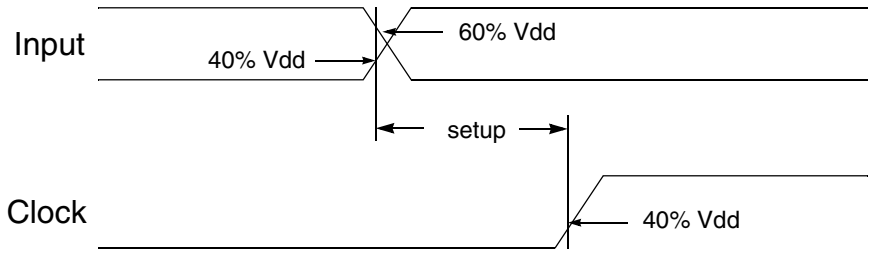


Figure 5 illustrates setup time for a positive-edge-triggered sequential cell with delays at 40/60.

Figure 5 Setup Time with Delays at 40/60



1.2.4 Hold Time

The hold time for a sequential cell is the minimum length of time the data-input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%. Hold-constraint values are measured as the interval between the data signal crossing rising time% of Vdd for rising data (or falling time% of Vdd for falling data) and the clock signal crossing rising time% of Vdd for rising clocks (or falling time% of Vdd for falling clocks). Libraries are usually characterized with delays at either 50% rising time/50% falling time or 40% rising time/60% falling time. Refer to the Technical Overview in your databook for values specific to your library. For comparison, illustrations are provided for both 50/50 and 40/60 delays. For the measurement of hold time, the data input signal is held stable before the active clock edge for an infinite setup time.

Note

ARM does not incorporate any hold time margins in the timing models. Chip designers should develop a timing methodology to account for chip-level timing inaccuracies inherent to extraction and timing analysis tools.

Figure 6 illustrates hold time with delays at 50/50.

Figure 6 Hold Time with Delays at 50/50

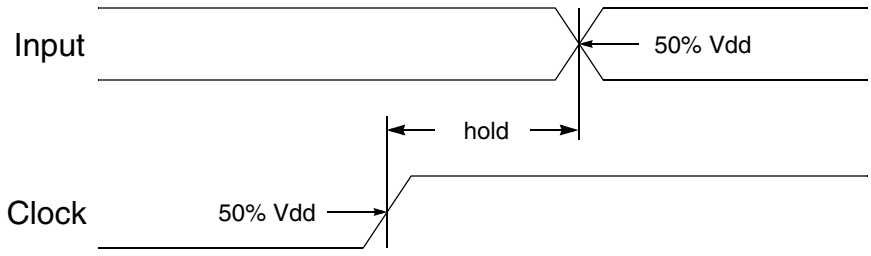
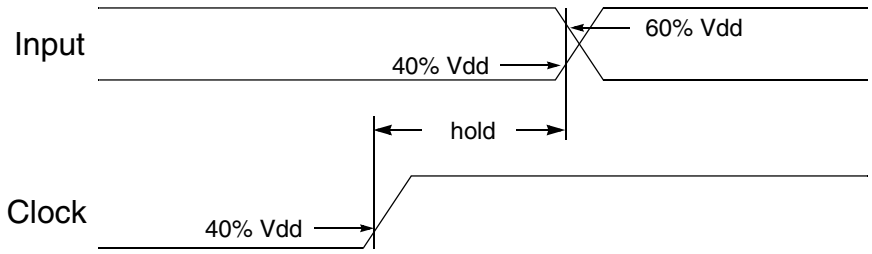


Figure 7 illustrates setup time with delays at 40/60.

Figure 7 Hold Time with Delays at 40/60



1.2.5 Recovery Time

Recovery time for sequential cells is the minimum length of time at which the set or reset signal must remain disabled before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%. Recovery constraint values are measured as the interval between the set or reset signal crossing rising time% of Vdd for active-low set or reset signals (or falling time% of VDD for active-high set or reset signals), and the clock signal crossing rising time% of Vdd for rising clocks (or falling time% of Vdd for falling clocks). Libraries are usually characterized with delays at either 50% rising time/50% falling time or 40% rising time/60% falling time. Refer to the Technical Overview in your databook for values specific to your library. For comparison, illustrations are provided for both 50/50 and 40/60 delays. For the measurement of recovery time, the set or reset signal is held stable after the active clock edge for an infinite hold time.

Figure 8 illustrates recovery time with delays at 50/50.

Figure 8 Recovery Time with Delays at 50/50

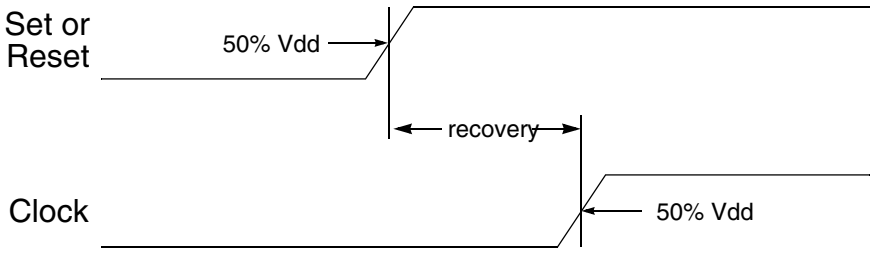
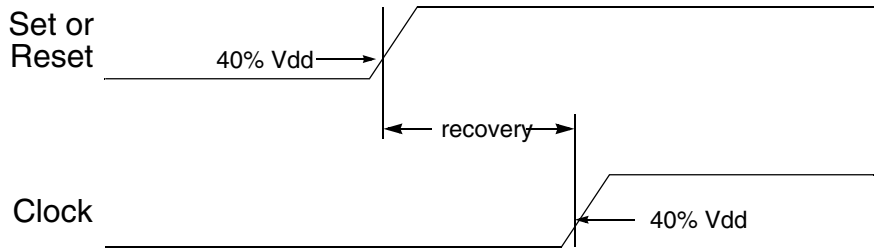


Figure 9 illustrates recovery time with delays at 40/60.

Figure 9 Recovery Time with Delays at 40/60



1.2.6 Removal Time

Removal time for sequential cells is the minimum length of time at which the set or reset signal must remain after the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the active clock edge does not latch in a new data value from that programmed by the asynchronous set or reset signal. Removal constraint values are measured as the interval between the set or reset signal crossing rising time% of Vdd for active-low set or reset signals (or falling time% of VDD for active-high set or reset signals), and the clock signal crossing rising time% of Vdd for rising clocks (or falling time% of Vdd for falling clocks). Libraries are usually characterized with delays at either 50% rising time/50% falling time or 40% rising time/60% falling time. Refer to the Technical Overview in your databook for values specific to your library. For comparison, illustrations are provided for both 50/50 and 40/60 delays. For the measurement of removal time, the set or reset signal is held stable before the active clock edge for an infinite setup time.

Figure 10 illustrates removal time with delays at 50/50.

Figure 10 Removal Time with Delays at 50/50

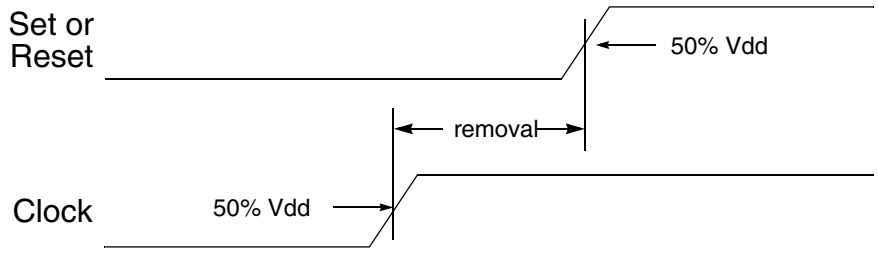
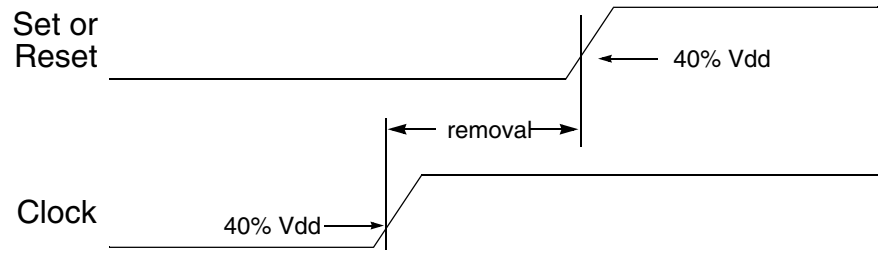


Figure 11 illustrates removal time with delays at 40/60.

Figure 11 Removal Time with Delays at 40/60



1.2.7 Minimum Pulse Width

Minimum pulse width is the minimum length of time between the leading and trailing edges of a pulse waveform. Minimum pulse width high (minpwh) is measured as the interval between the rising edge of the signal crossing rising time% of Vdd and the falling edge of the signal crossing falling time% of Vdd. Minimum pulse width low (minpwl) is measured as the interval between the falling edge of the signal crossing falling time% of Vdd and the rising edge of the signal crossing rising time% of Vdd. Libraries are usually characterized with delays at either 50% rising time/50% falling time or 40% rising time/60% falling time. Refer to the Technical Overview in your databook for values specific to your library. For comparison, illustrations are provided for both 50/50 and 40/60 delays.

Figure 12 illustrates minimum pulse width with delays at 50/50.

Figure 12 Minimum Pulse Width with Delays at 50/50.

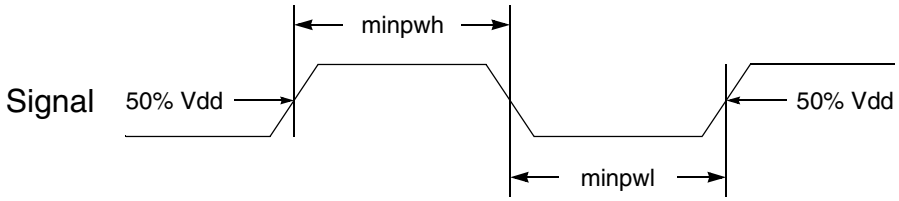
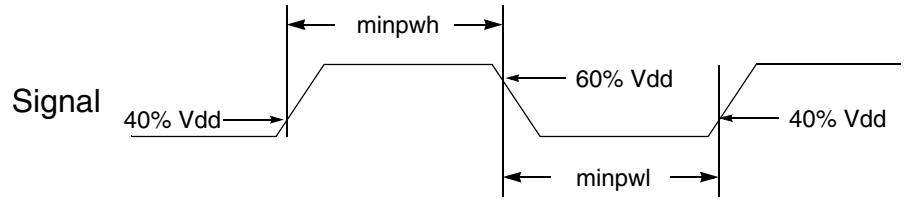


Figure 13 illustrates minimum pulse width with delays at 40/60.

Figure 13 Minimum Pulse Width with Delays at 40/60.



1.2.8 Electromigration

ARM standard cell libraries are designed to meet foundry electromigration guidelines for normal chip design usage; however, it is the chip designer's responsibility to ensure that electromigration guidelines are met at the chip level with regard to foundry guidelines as well as ARM guidelines for how the library will be used. The following three electromigration guidelines must be met in order to ensure safe use of the standard cell library within the electromigration guidelines of the foundry.

- The width of the metal2 Vdd and Vss power buses in the standard cells has been sized to provide adequate current to the cells. Vertical power straps must be placed with sufficient frequency to provide adequate current distribution to the standard cell power buses. For more details, see the section entitled *Routing* on page 13.
- The output pin metal for each standard cell has been sized to accommodate multiple vias when necessary (for worst case electromigration conditions) to meet via electromigration guidelines, although oversized metal output pins do not necessarily require multiple vias. The number of vias required to meet electromigration guidelines is design dependent, and you must use an appropriate number of vias and wire widths when routing from an output pin.
- The internal layouts of the standard cells have been designed and verified to comply with the manufacturer's electromigration guidelines under normal usage. Normal usage is defined as follows:

  1. The current required by the cell does not exceed the maximum current that can be supplied by the metal2 power buses.
  2. The output transition times (measured using 10% and 90% thresholds), for a cell outside the clock tree network, must be no greater than 20% of the total cycle time, or must be no greater than 10% of the cycle time for any of the output pins of that particular cell. Limiting the output transition time has the effect of limiting the load driven by the cell which will reduce the cell's current draw, making it comply with electromigration guidelines. Ratios larger than 20% are not appropriate for commonly used design flows and are unlikely to be encountered in normal designs.
  3. For a cell in the clock tree network, transition times must not exceed 10% of the total cycle time for that cell.

4. Some high drive clock cells need more stringent transition time requirements because they can potentially drive large capacitive loads at high frequencies. As a result, special care must be exercised when using these high drive clock cells.

1.2.9 Power Dissipation

The library is designed to dissipate only AC power, except for the small reverse-bias leakage currents which are normally present in all CMOS circuits. The power dissipation internal to a cell when a given input switches is primarily dependent upon the cell design itself. The power dissipation of a complete design, or part of a design, using cells from the library is primarily a function of the switching frequency of the design's internal nets. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

This library's datasheets contain both an AC power table which documents the internal energy consumption of each cell and a pin capacitance table which gives input pin capacitance data used to compute output loading. This information, coupled with design-specific information, can be used to estimate the total power dissipation of a cell within a design. The AC power tables specify the amount of energy consumed within a cell (uW/MHz) when the corresponding pin changes state at typical temperature, typical voltage, and typical process. The energy data in the tables were measured for the library's input slew and no loading at the outputs. For combinatorial cells, energy values are provided for only input pins. The energy value for each input pin is the average of energies associated with the input transitions which result in an output transition.

For sequential cells, the energy associated with each input pin is the average energy of those input transitions which do not result in an output transition. The energy associated with the output pin of a sequential cell is the average energy of all cases where an output transition is the result of a clock-input transition, minus the energy associated with the clock input pin. In the event that a sequential cell has multiple outputs, all output energy data will be associated with only one output pin.

1.2.10 Power Calculation

Power dissipation is dependent upon the power-supply voltage, frequency of operation, internal capacitance, and output load. The power dissipated by each cell is:

$$P_{avg} = \sum_{n=1}^{x} (E_{in} \bullet f_{in}) + \sum_{n=1}^{y} \left(C_{on} \bullet Vdd^2 \bullet \frac{1}{2} f_{on} \right) + E_{os} \bullet f_{o1} + L$$

where:

P_{avg} = average power (uW);

x = number of input pins;

E_{in} = energy associated with the nth input pin (uW/MHz);

f_{in} = frequency at which the nth input pin changes state during the normal operation of the design (MHz);

y = number of output pins;

C_{on} = external capacitive loading on the nth output pin, including the capacitance of each input pin connected to the output driver, plus the route wire capacitance, actual or estimated (pF);

V_{dd} = operating voltage = typical voltage;

f_{on}= frequency at which the nth output pin changes state during the normal operation of the design (MHz);

E_{os}= energy associated with the output pin for sequential cells only (uW/MHz);

L = leakage power (uW) for the cell.

The switching frequency of inputs and outputs of a particular cell in a design can be obtained from a gate-level logic simulator (e.g. Verilog) by applying typical input stimuli and measuring the activity on each node of interest. The total average power for the design can be computed by adding the average power for each cell.

EXAMPLE: Calculating Power for a DFFQXL Cell

For this exercise, assume that a DFFQXL cell has clock switching at 133MHz (clock frequency = 66.5MHz), input and output pins switching at 20MHz, cell leakage power of 0.001uW, and an external capacitance loading on the output pin of 0.02pF. Using the AC Power table, the power dissipated by the DFFQXL can be calculated by using the following equation:

$$P_{avg} = \sum_{n=1}^{x} (E_{in} \bullet f_{in}) + \sum_{n=1}^{y} \left(C_{on} \bullet Vdd^2 \bullet \frac{1}{2} f_{on} \right) + E_{os} \bullet f_{o1} + L$$

Given:

x= 2;

E_{i1} = 0.0056 uW/MHz;

E_{i2} = 0.0063 uW/MHz;

f_{i1} = 20 MHz;

f_{i2}= 133 MHz;

y= 2;

C_{o1}=0.02 pF;

C_{o2} = 0.02 pF;

V_{dd}=1.0V;

f_{o1}= 20 MHz;

f_{o2} =20 MHz;

E_{os}= 0.0060 uW/MHz,

we have:

$$P_{avg} = \sum_{n=1}^{2} (E_{in} \bullet f_{in}) + \sum_{n=1}^{2} \left(C_{on} \bullet Vdd^2 \bullet \frac{1}{2} f_{on} \right) + E_{os} \bullet f_{o1} + L$$

P_{avg} =

$$(E_{i1} \bullet f_{i1}) + (E_{i2} \bullet f_{i2})$$

$$+ \quad \left(C_{o1} \bullet VDD^2 \bullet \frac{1}{2} f_{o1}\right) + \left(C_{o2} \bullet VDD^2 \bullet \frac{1}{2} f_{o2}\right)$$

$$+ \quad (E_{os} \bullet f_{o1})$$

$$+ \quad L$$

P_{avg} =

$$(0.0056 \bullet 20) + (0.0063 \bullet 133)$$

$$+ \quad \left(0.02 \bullet 1.0 \bullet \frac{1}{2}(20)\right) + \left(0.02 \bullet 1.0 \bullet \frac{1}{2}(20)\right)$$

$$+ \quad (0.0060 \bullet 20)$$

$$+ 0.001$$

P_{avg} = 1.4709uW

1.2.11 Power Rail Strapping

The guidelines below provide a rough estimate with many simplifying assumptions. For a given module design, you can estimate the amount of vertical power-rail strapping that is required to fulfill electromigration requirements.

Note

Vss/Vdd rails are on metal2 for 45nm and smaller standard cell products, therefore strapping should be performed with vertical metal3 in 45nm and smaller libraries.

Given:

I_{avg} = total average current for the module, calculated from previous section (mA);

w_{m2} = Vss/Vdd metal2 wire width (um), refer to the Technical Overview provided with your datasheets for values specific to your library;

r = number of rows in module;

d_{m2} = maximum metal2 current density allowed for the process (mA/um);

d_{m3} = maximum metal3 current density allowed for the process (mA/um);

I_{m2} = maximum current that can be supported by all horizontal metal2 wires (mA);

I_{strap} = total current that must be supported by the vertical metal3 strapping (mA);

w_{m3} = metal3 wire width required for vertical strapping (um);

c = minimum number of metal3 straps;

we have:

$I_{m2} = w_{m2} \bullet r \bullet 2 \bullet d_{m2}$,

where multiplying by 2 assumes metal2 wires are supplied from both ends;

$$I_{strap} = \frac{(I_{avg} - I_{m2})}{2},$$

where dividing by 2 assumes the metal3 vertical strap wires are supplied from both ends;

$$w_{m3} = \frac{I_{strap}}{d_{m3}},$$

The metal3 wire width, w_{m3}, should be divided into a minumum of c equal portions which are spaced equidistant across the module, where

$c = \frac{I_{avg}}{I_{m2}}$, rounded up to the next integer.

It is recommended that the metal3 wire width, w_{m3}, be distributed evenly such that individual m3 straps have the same width as the m2 power rails. The same consideration must be given to the number of vias used to connect the metal2 and metal3 straps.

1.2.12 Routing

The guidelines below provide a rough estimate with many simplifying assumptions. For a given module design, you can estimate the amount of vertical power-rail strapping that is required to fulfill electromigration requirements.

As process geometries shrink, design rules become more complex and often more restrictive. Partly in conjunction with these design rules, and partly to enhance the performance of libraries, new cell architectures have been developed. As a result of these new design rules and architectures, routing often presents new challenges. This section addresses some of these challenges, specifically those created by the library architecture during the placement and routing phase.

The ARM Standard Cell Libraries at 40nm and 45nm process nodes are architected with metal2 power rails and a specific poly pitch. The following sections provide details on how these architectural selections impact routing are contained within this document.

The two primary factors to optimize routing results with these ARM libraries are:

- Enable smaller track pitches and denser cell design
- Decreased power rail resistance

1.2.12.1 Essential Library Information

Metal 2 (m2) power rails have several advantages:

- Decreased power rail resistance
  > m2 rail can be sized to optimize power versus signal routing
  > Improved IR drop for greater stride between m3 supply straps as a result
  > Better di/dt characteristics because of 2-D supply grid on m2 and m3
- Improved pin access by avoiding stretched pins (advantage over certain architectures)

The 12-track standard cell library (SC12) is architected with inset m2 rails. These inset rails do not abut when the cells are placed in a block. When the cells are flipped and abutted – the standard placement in blocks – the power rails remain separate. This allows for wide power rails without violating or being impacted by wide metal rules.

Metal2 power rails do impact routing and the power structure of the block; however this impact is primarily in the routing setup and power structure architecture. Using m2 for power rails implies that m2 is routed in the horizontal direction. In ARM standard cells, m1 is vertical, along with all odd-numbered metal layers. All even-numbered metal layers are horizontal. Routing test cases demonstrate fewer vias per pin, indicating a better utilization of lower metal planes.

The fixed poly pitch has a larger impact on routing. Because the poly pitch is fixed, this effectively dictates the cell width. The cell width "grid" is a multiple of the poly pitch – for example, the poly pitch is 140nm. However, the minimum routing pitch could be 120nm. Whatever the values, it is likely that the grid for the poly pitch is larger than the grid for the routing pitch. This is how the ARM Standard Cell Libraries at 40nm and 45nm process nodes are architected and used – a placement grid with a value that is ***not equal*** to the routing grid.

From a backend user's perspective, the net result of this architecture and the design rules is that the majority of pins will be on-grid with respect to metal2 (m2), but not always on the metal 3 (m3) grid. ARM refers to this style of pin implementation as "horizontally gridded pins."

Using a standard cell library with different placement and routing grids will become more and more common as geometries continue to shrink. The following is a list of general library information to address the library architecture and design rules. Understanding this information is essential to successfully and optimally implementing a design with the ARM Standard Cell Libraries at process nodes of 45nm and smaller.

- The libraries have placement grids and routing grids that are not the same
- The actual minimum m2 pitch, per the design rules, should be used for ALL and routing.

  Synopsys: The Milkyway database for the library will have the proper placement grid stored within the database. It will not reference the unit tile in the routing tech file.

  Cadence: Encounter will place based on the SITE definition in the LEF (example: "SIZE 0.140 BY 1.440.")

  Magma: You need to define your placement grid using "rule grid placement."
- The libraries are designed to be routed with the minimum m2 pitch contained in the design rules. They are NOT designed to be routed with an m2 pitch equal to the poly pitch (typically a larger value).

- The standard cell pins are “horizontally gridded” pins, meaning that the pins are neither completely “on-grid,” nor are they “off-grid.” There is always a valid on-grid pin access point in the m2 direction. The router must allow off-grid pins, including allowing horizontally gridded pins. You should finish routes off-grid.
- Routing horizontally gridded pins takes longer. Be aware that run times can be longer than routing a library that has all pins on-grid.

1.2.12.2 Routing with Horizontally Gridded Pins

The pins in the 45nm and smaller ARM Standard Cell Libraries are “horizontally gridded”. This means the pin can always be accessed by on-grid m2 but will usually require off-grid m1.

It is difficult to make generalizations about which router settings to change. Not all tools will have the same default settings, and default settings may change between versions of the same tool. However, the default settings of the router usually allow for off-grid routing and settings should be used that direct the router to place v1 within the m1 pin.

The latest place and route tools are recommended to achieve optimal results. For most tools, the latest versions are required in order to fully support certain design rules and smaller than 45nm nodes. Most EDA tool vendors have application notes specific to this size routing details available on-line.

1.2.12.3 Power Strapping

You should add vertical metal3 (m3) power buses. These buses should be distributed evenly, including between power and ground. M3 width should match the width of the m2 power rails, but at every intersection, flare these rails to permit a 2x2 via structure. This takes some effort within the routing tools, but the effort should not be significant. For the 12-track library (SC12), the power rails do not overlap with flipped and abutted rows, however, it is not DRC legal to place all the cells in every row with the same orientation; the cells are still designed to have every other row flipped.

It is expected that the design will have two upper metal layers as a second power grid. Whatever the design details, for the purposes of this document, upper layers that distribute power will be designated m(top) and m(top-1). These upper layers are not necessarily the top layers of the process, but the top layers for power distribution.

Vias between the two grids (lower power grid, m(top-1), and upper power grid, m(top)) have the following recommendations.

- Only m3 should have a via up to the m(top-1) layer. If m(top-1) is vertical, a horizontal m4 layer should be added, and only m4 should have a via up to m(top-1).
- There should be no vias between m(top) and m3 layer (or m4 if m(top-1) is vertical).
- The m2 rail is slightly narrower than which will fit a 2x2 via structure, but a careful designer can still get the supply routing to this style of structure without blocking more that two channels of m2 routing resources.

Some routers may not be capable of automatically providing the above. You may need to place an m2 strap centered on the current rail locations. Then via2s can be added to m3. Finally, the m2 strap can be removed and replaced with an m2 that is the same width as the rail (it may be possible to remove the strap completely). Although this is likely to be a manual step, it is the optimal way to add the most number of vias without blocking unnecessary routing channels.

A similar approach can be used for m3, such that m3 is the same width as the m2 rails but still has 2x2 via arrays attaching to it. This way, the design can take advantage of the parallel run length escape on the fat metal rules.

Details on metal usage targets are a strong function of the power density of the design. It is not possible for ARM to determine whether having these two grids (upper and lower) relates to previous designs that only distributed power on the upper metal layers. In general, however, these guidelines will achieve an electrically solid power grid and excellent routing results.

- Always evenly distribute your VDD and VSS routes on any given layer. Don't pair these networks and then have a large offset to the next pair.
- You should favor supply widths that block two or at most three tracks of 1x metal route resources. These widths avoid excessive local routing congestion and support 2x2 via structures which are an excellent balance between electrically solid power structures and route blockages. You must take the time to carefully size the width and offset of these supply routes, but the extra routing resource is worth the time to calculate this.

1.2.12.4 IR-Drop, L*Di/Dt and Edge Rates

In general, the di/dt response of any supply grid should be designed considering the fundamental frequencies of the edge rates and not clock period. Note that throughout the industry, this is atypical for supply design, though ARM strongly recommends consideration of the edge rates, not the clock.

The IR drop is a strong function of clock frequency because average current is a strong function of clock frequency. Also, cell delay is very non-linear with voltage as little as a 10% reduction from the nominal supply. You can not simply seek to average the impact of di/dt out over the cycle and get a simple averaging of cell delay. You need to insure that the average delta V below the nominal supply is higher than the 10% supply collapse used for characterization to insure the performance indicated by that voltage.

These supply recommendations have the underlying assumption that the top level thick metals are doing most of the work to minimize the IR drop, while the m2/m3 grid is doing most of the work to minimize the di/dt impact.

Note also that further discussion on this topic often proceeds to a discussion of margining and process variation, for which there are different philosophies and many books written

1.3 Special Cells

This section discusses special cells that may be included in your library. Descriptions of cells not included with your product are additional options available from ARM.

1.3.1 Antenna Fix Cells

The library contains an antenna-fix cell which must be inserted manually. However, most place and route tools will indicate which nets require the antenna-fix cell. Refer to the foundry's antenna effect prevention guideline, specified in your library's README, for maximum wire width. During place and route, the router may connect wires to the input gates of cells that are longer than the maximum length allowable by the guideline. The antenna cell can be used in this case to add an optional diode on the net close to the input gates which do not meet the guideline.

Pin A on the antenna cell connects to a diode, reverse biased to ground.

1.3.2 Delay Cells

The library contains delay cell, or families of delay cells, that have the same width. These delay cells allow you to adjust a given delay path with a simple cell substitution after place and route.

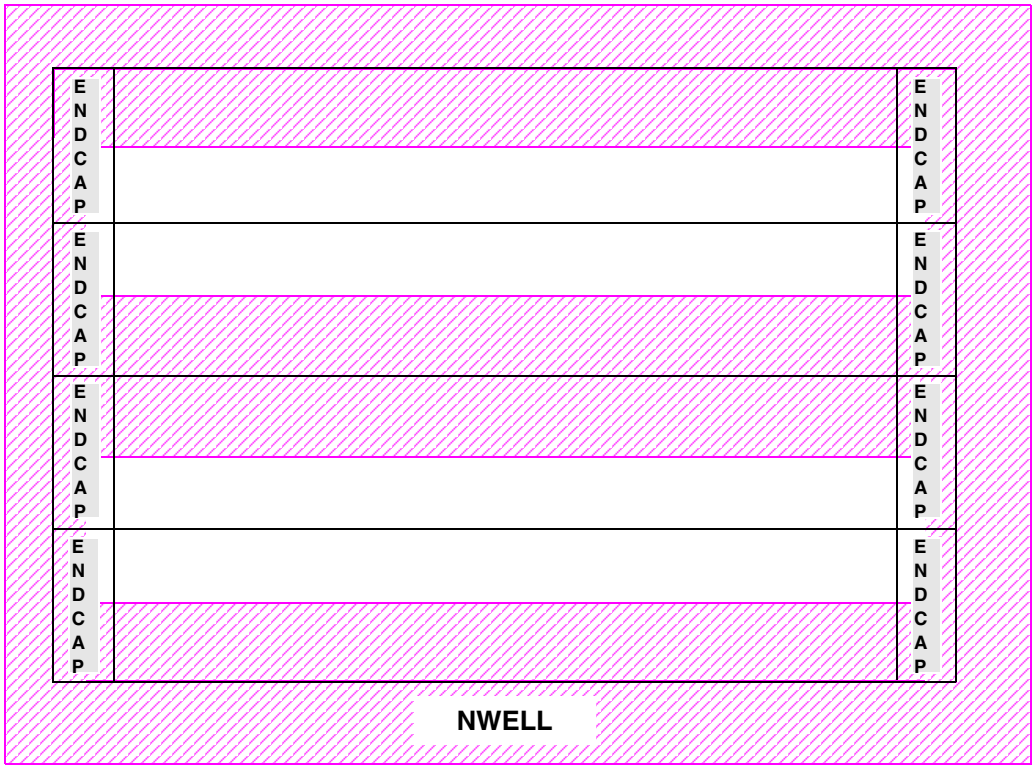
1.3.3 ENDCAP and ENDCAPTIE

If your library supports triple well design it is required to be NWELL-enclosed. The cell used to terminate a standard cell row and fulfill the NWELL antenna requirement is shown in the Twin/Triple Well Support table in the Technical Overview section of your databook. Additionally, a double-cell row is also required to ensure that the top and bottom rows, together with the terminus cell, form an enclosed NWELL. The wells are left floating in the case of ENDCAP cells, and are tied to power rails in the case of ENDCAPTIE cells.

If your library contains a FILLTIESB cell and you are designing for triple-well, then you must also place the FILLTIESB cell outside the ENDCAP cells. Consider the FILLTIESB as an endcap to the ENDCAP cell. It is only needed for triple-well designs, in order to fulfill the well antenna requirement for connecting to substrate.

Figure 14 illustrates the NWELL with ENDCAP cells.

Figure 14 NWELL with ENDCAP/ENDCAPTIE cells



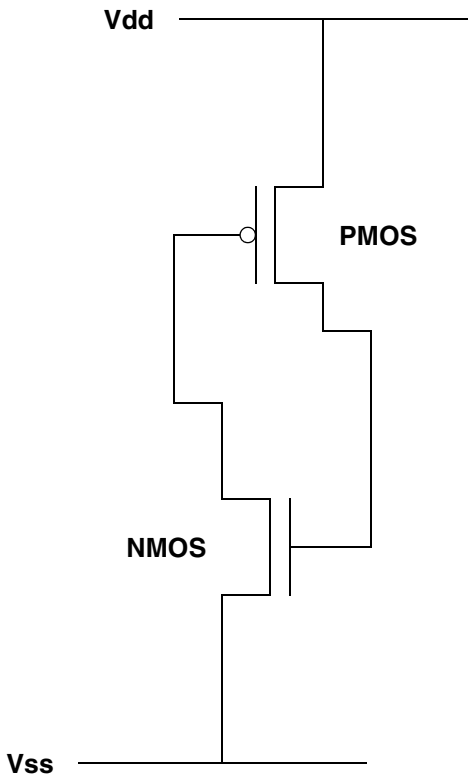
The ENDCAP cell extends the NWELL in east/west cell orientation directions to reduce well proximity effects and for OD to OD space mitigation. It is not for triple well support, nor does it include well antennas. The GDS2 for FILLTIE3 and ENDCAP3 is identical.

1.3.4 FILL*CAP and FILL*CAPTIE Cells

FILL*CAP and FILL*CAPTIE cells function as FILL cells with decoupling capacitors. Inside the FILL*CAP and FILL*CAPTIE, PMOS and NMOS devices form decoupling capacitors between the Vdd and Vss rails, reducing ground bounce in the power grids. The wells are left floating in the case of FILL*CAP cells, and are tied to power rails in the case of FILL*CAPTIE cells.

Figure 15 illustrates the FILL*CAP functional schematic.

Figure 15 FILL*CAP/FILL*CAPTIE Functional Schematic

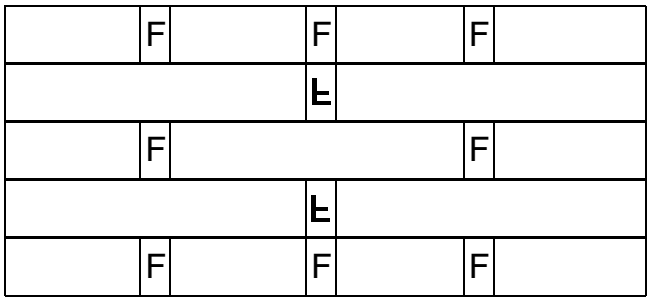


1.3.5 FILL*TIE-NWELL and Substrate Tie Cell

SC8, SC9, and SC12 libraries do not have well or substrate ties inside the cells. You are required to tie the NWELLs to Vdd and the substrate to Vss before place-and-route using the FILL*TIE cell. Before place-and-route, pre-place the FILL*TIE cell periodically in every placement row. You must place the FILL*TIE cell as frequently as the design requires. For example, if the design rules require a well or substrate connection every 20um, then the FILL*TIE cell must be pre-placed every 20um.

See Figure 16 for sample placement.

Figure 16 Sample Placement of FILLTIE Cells for 20um NWELL and Substrate Tie Design Rule



Note

The letter "F" indicates a FILL*TIE cell placed in normal orientation, and the letter "F" flipped upside down indicates a FILL*TIE cell placed in MY orientation.

In all rows except for the top and bottom rows, the NWELL and substrate are shared by two adjacent placement rows. This allows you to place the FILL*TIE cell only half as frequently as the design rules require. Remember to stagger the placement in the adjacent rows by an amount equal to the design row.

Assuming that the rule is every 20um, you need to place FILL*TIE cells every 20um in the top and bottom rows. If you stagger the placement by 20um between adjacent rows, you can place FILL*TIE cells every 40um for all rows between the top and bottom rows. This method allows every row to have well and substrate ties every 20um.

It is also possible to place the FILL*TIE cells in columns, skipping alternate rows. The distance betweek the FILL*TIE cells in this configuration is half the distance of the staggered configuration. For example, the closer together cells are placed 10um apart in the example, but every other row is free of FILL*TIE cells. Alternatively, you could place FILL*TIE cells 20um apart in every other row. The remaining rows would not require any FILL*TIE cells.

1.3.6 MX2 Cells

The MX2 cell is designed with a classic NAND2-NAND2 multiplexer circuit design. It is optimized for speed, area, and power, and maintains stable timing characteristics as process varies over time and across changes in device threshold. However, The output pin Y has the potential to glitch low during a high-to-low transition on the S0 input, when A=B=1. Use this cell with caution when driving clock or other control signals in your design.

1.3.7 Register File Cells

Register file cells (RF*) may be provided to support creating very small memories from standard cells. The register file bit cells (RF1R1W, RF2R1W, RF1R2W, RF2R2W) have tri-state outputs. You must tie these tri-state outputs together on a bit line and have this bit line drive function as an output buffer. The library contains a number of inverting and non-inverting buffers (INV*, BUF*, BUFZ*) that can buffer the bit lines.

It is possible to make a memory that has a non-power-of-two word depth. If this is employed, it is possible to input an address to the memory such that none of the bit cells are addressed and nothing is driving the bit line. A floating bit line can cause the logic following it to go into a high power state, therefore, users must take special care when designing a memory with a

non-power-of-two word depth. Users must guarantee that the bit line is never allowed to float by ensuring that at least one bit cell is always driving the bit line, or that a floating bit line does not cause subsequent logic to go into a high power state. One way to achieve the latter is to use an output buffer with an enable. NAND or AND gates or tri-state output buffers (NAND*, AND*, BUFZ*) can be used for this purpose. Whichever is used, be sure to generate an enable signal that only enables the output buffer when the bit line is not floating.

1.3.8 TIEHI/LO Cells

The library may contain a TIEHI cell and a TIELO cell. The outputs of the TIEHI and TIELO cells are driven through diffusion to provide isolation from the power and ground rails for better ESD protection. The standard cell abstract methodology assumes that the TIEHI and TIELO cells are used to tie off any inputs to power and ground. If these cells are not used and the router is allowed to drop vias on the power rail, DRC errors or shorts may result.

1.3.9 Well Antenna Cells

If your library contains the WELLANTENNA cell, this process requires that, for any standard cell row with a device in it, the NWELL must be tied down to the substrate and triple-wells must be tied to the enclosing NWELL. Any connection between the wells is usually sufficient. In a triple-well design, the connection happens automatically when you place the ENDCAPTIE cells at the ends of the standard cell rows. In triple-well and twin-well designs, any CMOS standard cell (such as an inverter) placed in a standard cell row will also make the connection; however, in a twin-well design, if a pair of standard cell rows, sharing an NWELL, or a single standard cell row is populated by nothing but FILL cells and/or ANTENNA cells and at least one FILLCAP cell, the associated NWELL will be in violation of the well antenna rule. In this scenario, the NWELL must be tied down to the substrate by inserting a WELLANTENNA cell into the standard cell row in violation.

1.4 Library Naming Conventions

The following naming conventions apply to ARM standard cell libraries.

1.4.1 Power, Voltage, and Timing

The Liberty files have a specific nomenclature that clearly identifies the PVT and other information used in extracting and characterizing the library.

The general syntax for an ARM Standard Cell Liberty file (both .lib and .db, in the lib/ and db/ directories, respectively) is:

[product]_[process corner]_[extraction]_[overlay]_[voltage]_{voltage2}_[temp]

The “product” field contains several fields as follows:

sc[cell height]{mc}_[process node name]_[toolkit name]_[threshold voltage]{_c[channel length]}

with the "product" field expanded, the complete syntax is:

sc[cell height]{mc}_[process node name]_[toolkit name]_[threshold voltage]{_c[channel length]}_[process corner]_[extraction]_[overlay]_[voltage]_{voltage2}_[temp]

where the following table describes each field.

Table 1 LIberty File Syntax

Field	Description	Example
“sc”	Standard Cell (represents all logic products); not a variable	sc
cell height	Track height of the library	12
“mc”	Optional. If not present, the library is minimum channel length. If present, the library is a multi-channel length library	mc
process node name	Process name as defined by the foundry	cln65gp, cmos10lp
toolkit name	Describes type of library	base for a base standard cell library pmk for a Power Management Kit, eco for an ECO kit, etc.
threshold voltage	Vt used in the library	rvt, hvt, etc
“c”	“channel” (required if “mc” field is present identifies that the next value indicates the channel length)	c
channel length	Required if "mc" field is present; defines channel length used in library	40
process corner	N and P transistor process corner used for characterization	ft for a fast n-channel corner and a typical p-channel corner

Table 1 LIberty File Syntax (Continued)

Field	Description	Example
extraction	Parasitic extraction corner used	typical nominal
overlay	Amount of overlay used for extraction	min max ave
voltage	Characterization voltage of form #p##v,	1p20v (= 1.20V)
voltage2	Optional: second characterization voltage used for cells with multiple voltage supplies such as level shifters	1p20v (= 1.20V)
temp	Temperature used for characterization	85c

1.4.2 Cell Name Fields

The library cell name has four separate fields. They are the root, drive strength, library identifier, and threshold voltage identifier. These four components are concatenated together in the following order:

[root]_[drive strength]_[library identifier][threshold voltage]

For Example:

SDFFQ_X1M_A12TR

SDFFQ : root field (mux-d scan flop with non-inverting output)

X1M : drive strength field (1 fold output stage with an M beta ratio)

A12 : library identifier field (ARM library at a 12 track pitch)

TR : threshold voltage field (Regular or nominal threshold voltage cell)

BUFH_X2P5B_A10TL or BUFH_Y2MK_A10TL

BUFH : root field (high speed buffer)

X2P5B : drive strength field (2.5 fold output stage with a B beta ratio)

X2ML: drive strength field (2 fold output stage with an M beta ratio, “L” indicates a strain optimized cell)

A10 : library identifier field (ARM library at a 10 track pitch)

TL : threshold voltage field (low threshold voltage cell

1.4.3 Root

This portion of the cell name defines the logical function of the cell. There is a large degree of variation in this field. A full definition of the root names are provided in later sections, broken out by major function. Some examples of what this field includes are NAND2, AOI21, INV, SDFF, etc.

1.4.4 Drive Strength

The library may contain multiple beta ratios for some of the topologies. This requires a naming convention be adopted which indicates the different beta ratios. The convention is: X[number][beta ratio letter];The "X" plus the number field indicates how many folds are present. One fold is indicated by "X1" while "X4" indicates four folds. Think of the "X" as a mnemonic for "multiplied by." The library also makes use of non-integer folds. This is useful for improving performance as well as reducing power consumption. When a non-integer fold is present, a "P" indicates the decimal place. For example, a cell that contains 1.4 folds is indicated with "X1P4." If the fold size is less than one, a zero prefixes the "P." Currently, only one significant digit is used after the decimal place as it is believed this provides enough granularity.

There are many potentially useful beta ratios. Table 2 lists all the beta ratios currently defined. Note that since the most recent SC9 and SC12 libraries are flood-filled and no letter was used in the their naming convention, ARM adopted the convention of null or no character for sindicating flood-filled.

Table 2 Beta Ratio Letter Definition

Letter	Description
null	Devices are drawn at the maximum size possible regardless of topology
A	Tuned to minimize the average delay between the input edges
B	The delay for both edges are equal when the input driver is a balanced inverter
E	The output rising and falling edge rates are equal assuming the input driver has equal rising and falling edge rates
M	Tuned to minimize the maximize delay between the input edges
F	tuned so that the input to output delay of a falling output is improved

With the addition of the beta ratio indicator to the drive strength field the "CLK" prefix has been dropped since this prefix was really just indicating a "B" type beta ratio in previous SAGE-X libraries.

1.4.5 Library Identifier

In order to support the mixing of different libraries on a single die, all ARM libraries have a unique library identifier field. The field has two parts. The first is the library letter and the second is a number indicating the library's cell pitch in tracks. The letter "A" denotes an ARM library and the number “12” denotes an SC12 (12-track) library. A twelve-track ARM library’s identifier is "A12." For a multi-channel library, the library identifier will end with the channel length. “A1240” indicates an ARM 12-track multi-channel library with a channel length of 40nm.

1.4.6 Threshold Voltage

This field differentiates the different threshold voltages versions of a cell. The syntax is:

T[threshold letter]

The defined threshold letters and their meaning are provided in Table 3.

Table 3 Threshold Voltage Letter Definition

Letter	Description
H	High Threshold Voltage
L	Low Threshold Voltage
R	Regular (Nominal) Threshold Voltage
S	Super High Threshold Voltage

For a cell containing low threshold voltage devices, this field would be "TL."

1.4.7 Root Name

Flops

[logic][root][clock][async][scanout][output][ppa]

logic : null, An, AOmn, On, OAmn, Mn, E

null : No logic integration

An : n-input AND (can be used for synchronous reset)

AOmn : AOI style input (can be used for synchronous set and reset with set dominant)

On : n-input OR (can be used for asynchronous set)

OAmn : OAI style input (can be used for synchronous reset and set with reset dominant)

Mn : n-input encoded mux

E : mux-hold flop (enable)

root : DFF, DRFF, SDFF, SDRFF

DFF : basic master slave flop

DRFF : basic master slave flop with retention

SDFF : mux-d flop

SDRFF: mux-d flop with retention

clock : null, N

null : positive edge clock and base setup verses clock->q relationship

N : negative edge clock and base setup verses clock->q relationship

async : null, S, R, RS, SR, P

null : no async inputs

S : async set

R : async reset

RS : async reset and set with reset dominant

SR : async set and reset with set dominant

P : active high

output : null, Q, QN

null : dual output flop

Q : non-inverting output flop (q)

QN : inverting output flop (qn)

ppa : null

null : base flop design point with regards to power, delay, and area

Integrated Clock Gate

[logic][testovrd]ICG[clock][ppa]

logic : null

null : no logic integration

test ovrd : FR, POST, PRE

FR : free running version with no enable desinged to match PRE and POST delay

POST : test over-ride input is asynchronous

PRE : test over-ride input is synchronous

clock : null

null : ICG produces an active high output

ppa : null

null : base flop design point with regard to power, delay, and area

Latches

The naming convention for latches is basically the same as the flops convention for consistency.[logic][root][clock][async][scanout][output][ppa]

logic : null

null : No logic integration

root : LAT

LAT : basic transparent latch

clock : null, N

null : latch is transparent while clock is high

N : latch is transparent while clock is low

async : null, S, R, P

null : no async inputs

S : async set

R : async reset

P : active high

scanout : null

null : no dedicated SO pin

output : Q, QN

Q : non-inverting output flop (q)

QN : inverting output flop (qn)

ppa : null

null : base flop design point with regards to power, delay, and area