



**CSMC 0.153um
CMOS EN Process 9Track
5V High Density Standard Cell Library**

User's Guide

Version 2.0

2019

CSMC TECHNOLOGIES CORPORATION

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Revision History

Document Version	Date	Notes
1.0	Jan.10 th , 2019	Production Build
2.0	Aug.10 th ,2019	Adding 35k top metal tf file

Introduction

This user's guide is intended to give users a general overview of the current CSMC 0.153um CMOS EN Process 1 POLY 6 METAL core cell library details for the production release contents and structure.

Product Description

The 5V CSMC 0.153um CMOS EN process High Density StandardCell library represents the most comprehensive set of Optimum Silicon™ standard core cells. The libraries are being certified by the CSMC and support Synopsys and Cadence EDA tools.

Library Feature

- CSMC 0.153um CMOS EN Process
- CSMC 0.153um CMOS EN Process #9C07 version DRC and LVS rule [LVS property margin = 0%](#)
- Support CSMC 0.153um CMOS EN process **hc1513x50v012.lib** spice model
- 368 standard core cell.
- Cell high : 4.284um.
- Accurate timing characterization
- Support most of the EDA tools
- Optimized for Cadence and Synopsys place&route tools.
- High density, routability, less area
- Routable for 3, 4, 5 or 6 metal
- Support 25K/35K thick top metal and 12K thin top metal
- Notice: 5V MOS library have worse performance when working on worst Corner ss 1.8V/2.7V

Library Package Content

- Optimum Silicon™ standard core cell library : CSMC0153

EDA Tool Environment

The library has been designed under Cadence and Synopsys software environment that consists of the following tools :

- Cadence Verilog_LDV5.1-QSR3
- Cadence Silicon Ensemble 5.4
- Cadence Abstract 5.4
- Cadence IC 51/IC61
- Synopsys VCS 7.1.1R1
- Synopsys PrimeTime 2008.06

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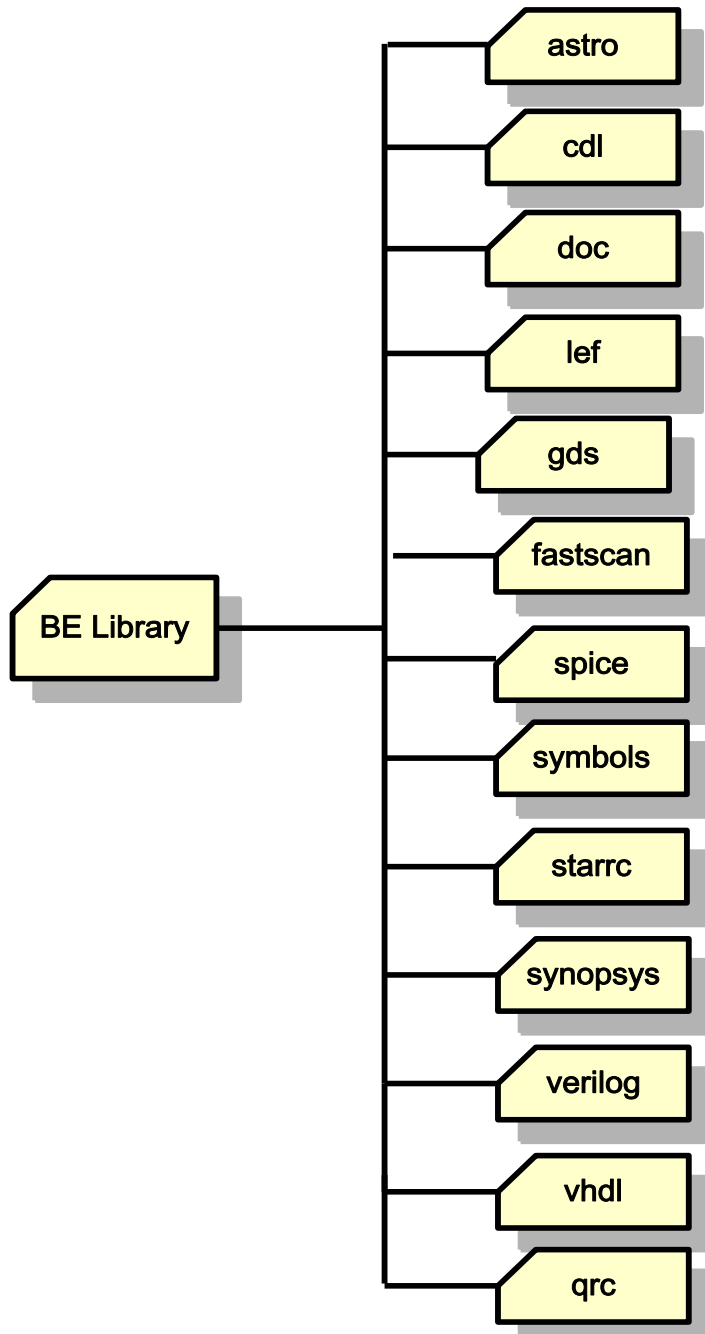
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-
- Synopsys DesignCompiler B-2008.09-SP5
 - Synopsys Astro 2007.03
 - Synopsys HSPICE 2017.03-2

Library Shipping Database

- CSMC0153MCU1P6M5V9Tlib_BE --- Include GDSII and corresponding database.

What is CSMC BE Library Installation Directory



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Figure 1 BE directory structure of CSMC library

BE Directory Major Structure Introduction

1. astro (12K/25K/35K)

Content	Description
Milkyway	<i>CSMC 0.153um CMOS EN process 5V standard CORE cells' FRAM, CELL, TIM, PWR</i>
tf	<i>CSMC 0.153um CMOS EN process 5V Apollo and Astro technology file</i>
clf	<i>CSMC 0.153um CMOS EN process 5V standard CORE cells' TT, FF, SS three corner case timing model, including, time, power, antenna information</i>

2. cdl

Content	Description
csmc0153.cdl	<i>CSMC 0.153um CMOS EN process 5V standard CORE cells' cdl netlist.It can be included to do lvs checking.</i>

3. doc

Content	Description
Library datasheet	<i>CSMC 0.153um CMOS EN process 5V process standard CORE cells' datasheet.</i>
Library user's guide	<i>CSMC 0.153um CMOS EN process 5V library user's guide</i>
libcelldatasheet	<i>Including cell list and cell datasheet summary</i>

4. fastscan

Content	Description
csmc0153.atpglib	<i>CSMC 0.153um CMOS EN process 5V process standard CORE cells' ATPG library for Mentor EDA tools</i>

5. lef :thick/thin:25k/12k

Content	Description
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csmc0153_3lm_tech_12k/25k/35k.lef	CSMC 0.153um CMOS EN process 5V process 3 metal technology lef file
csmc0153_4lm_tech_12k/25k/35k.lef	CSMC 0.153um CMOS EN process 5V process 4 metal technology lef file
csmc0153_5lm_tech_12k/25k/35k.lef	CSMC 0.153um CMOS EN process 5V 5 metal technology lef file
csmc0153_6lm_tech_12k/25k/35k.lef	CSMC 0.153um CMOS EN process 5V 6 metal technology lef file
csmc0153.lef	CSMC 0.153um CMOS EN process 5V standard core cells' lef library

6. gds

Content	Description
csmc0153.gds	CSMC 0.153um CMOS EN process 5V standard core cells' gds2 database

7. symbols(IC51/IC61)

Content	Description
csmc0153	CSMC 0.153um CMOS EN process standard core cells' cadence symbol library
csmc0153_without_PG	CSMC 0.153um CMOS EN process standard core cells' cadence symbol library without the VDD/GND PIN
csmc0153.edif	CSMC 0.153um CMOS EN process standard core cells'edif library
csmc0153_without_PG.edif	CSMC 0.153um CMOS EN process standard core cells'edif library without the VDD/GND PIN
csmc0153.sdb csmc0153_without_PG.sdb csmc0153.slib csmc0153_without_PG.slib	Synopsys symbol library

8. spice

Content	Description
*.pex.netlist *.pex.netlist*.pxi *.pex.netlist.pex	CSMC 0.153um CMOS EN process 5V standard core cells' spice netlist transistor level extraction

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9. starrc: thick/thin:35k/25k/12k

Content	Description
a3/t3_gt_cell_12k/25k/35k_max.itf a3/t3_gt_cell_12k/25k/35k_min.itf a3/t3_gt_cell_12k/25k/35k_typ.itf a3/t3_gt_cell_12k/25k/35k_max.nxtgrd a3/t3_gt_cell_12k/25k/35k_min.nxtgrd a3/t3_gt_cell_12k/25k/35k_typ.nxtgrd a3/t3_gt_cell_12k/25k/35k_max.tluplus a3/t3_gt_cell_12k/25k/35k_min.tluplus a3/t3_gt_cell_12k/25k/35k_typ.tluplus	CSMC 0.153um CMOS EN process 5V 3 metal Star_RCXT gate level extraction files
a4/t4_gt_cell_12k/25k/35k_max.itf a4/t4_gt_cell_12k/25k/35k_min.itf a4/t4_gt_cell_12k/25k/35k_typ.itf a4/t4_gt_cell_12k/25k/35k_max.nxtgrd a4/t4_gt_cell_12k/25k/35k_min.nxtgrd a4/t4_gt_cell_12k/25k/35k_typ.nxtgrd a4/t4_gt_cell_12k/25k/35k_max.tluplus a4/t4_gt_cell_12k/25k/35k_min.tluplus a4/t4_gt_cell_12k/25k/35k_typ.tluplus	CSMC 0.153um CMOS EN process 5V 4 metal Star_RCXT gate level extraction files
a5/t5_gt_cell_12k/25k/35k_max.itf a5/t5_gt_cell_12k/25k/35k_min.itf a5/t5_gt_cell_12k/25k/35k_typ.itf a5/t5_gt_cell_12k/25k/35k_max.nxtgrd a5/t5_gt_cell_12k/25k/35k_min.nxtgrd a5/t5_gt_cell_12k/25k/35k_typ.nxtgrd a5/t5_gt_cell_12k/25k/35k_max.tluplus a5/t5_gt_cell_12k/25k/35k_min.tluplus a5/t5_gt_cell_12k/25k/35k_typ.tluplus	CSMC 0.153um CMOS EN process 5V 5 metal Star_RCXT gate level extraction files
a6/t6_gt_cell_12k/25k/35k_max.itf a6/t6_gt_cell_12k/25k/35k_min.itf a6/t6_gt_cell_12k/25k/35k_typ.itf a6/t6_gt_cell_12k/25k/35k_max.nxtgrd a6/t6_gt_cell_12k/25k/35k_min.nxtgrd a6/t6_gt_cell_12k/25k/35k_typ.nxtgrd a6/t6_gt_cell_12k/25k/35k_max.tluplus a6/t6_gt_cell_12k/25k/35k_min.tluplus a6/t6_gt_cell_12k/25k/35k_typ.tluplus	CSMC 0.153um CMOS EN process 5V 6 metal Star_RCXT gate level extraction files

10. synopsys

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Content	Description
csmc0153_max.db csmc0153_max.lib csmc0153_max_2d7V.db csmc0153_max_2d7V.lib csmc0153_max_1d8V.db csmc0153_max_1d8V.lib csmc0153_min0c.db csmc0153_min0c.lib csmc0153_min40c.db csmc0153_min40c.lib csmc0153_typ.db csmc0153_typ.lib	<i>CSMC 0.153um CMOS EN 5V standard core cells' synopsys timing models on TT,SS,FF corner, tempratures were -40°C(5.5V), 0°C(5.5V), 25°C(5V), 125°C(1.8V/2.7V/4.5V)</i>

11. verilog

Content	Description
csmc0153.v	<i>CSMC 0.153um CMOS EN 5V standard core cells' verilog format behavior model for Version 2.1</i>
csmc0153_V3p0.v	<i>CSMC 0.153um CMOS EN 5V standard core cells' verilog format behavior model for Version 3.0</i>

12. vhd1

Content	Description
csmc0153_max_1d8V_VITAL.vhd csmc0153_max_1d8V_Vcomponents.vhd csmc0153_max_1d8V_Vtables.vhd	<i>CSMC 0.153um CMOS EN process standard core cells' VHDL format behavior model timing models on SS 1.8V corner, temprature was 125°C</i>
csmc0153_max_2d7V_VITAL.vhd csmc0153_max_2d7V_Vcomponents.vhd csmc0153_max_2d7V_Vtables.vhd	<i>CSMC 0.153um CMOS EN process standard core cells' VHDL format behavior model timing models on SS 2.7V corner, temprature was 125°C</i>
csmc0153_max_VITAL.vhd csmc0153_max_Vcomponents.vhd csmc0153_max_Vtables.vhd	<i>CSMC 0.153um CMOS EN process standard core cells' VHDL format behavior model timing models on SS 4.5V corner, temprature was 125°C</i>
csmc0153_min0c_VITAL.vhd csmc0153_min0c_Vcomponents.vhd csmc0153_min0c_Vtables.vhd	<i>CSMC 0.153um CMOS EN process standard core cells' VHDL format behavior model timing models on FF 5.5V corner, temprature was 0°C</i>

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csmc0153_min40c_VITAL.vhd csmc0153_min40c_Vcomponents.vhd csmc0153_min40c_Vtables.vhd	<i>CSMC 0.153um CMOS EN process standard core cells' VHDL format behavior model timing models on FF 5.5Vcorner, temprature was -40°C</i>
csmc0153_typ_VITAL.vhd csmc0153_typ_Vcomponents.vhd csmc0153_typ_Vtables.vhd	<i>CSMC 0.153um CMOS EN process standard core cells' VHDL format behavior model timing models on TT 5V corner, temprature was 25°C</i>

13. qrc

Content	Description
a3/t3_gt_cell_12k/25k/35k_max.ict a3/t3_gt_cell_12k/25k/35k_min.ict a3/t3_gt_cell_12k/25k/35k_typ.ict a3/t3_gt_cell_12k/25k/35k_max_captbl a3/t3_gt_cell_12k/25k/35k_min_captbl a3/t3_gt_cell_12k/25k/35k_typ_captbl qrcTechFile	<i>CSMC 0.153um CMOS EN process 3 metal qrc gate level extraction files for Cadence Tools</i>
a4/t4_gt_cell_12k/25k/35k_max.ict a4/t4_gt_cell_12k/25k/35k_min.ict a4/t4_gt_cell_12k/25k/35k_typ.ict a4/t4_gt_cell_12k/25k/35k_max_captbl a4/t4_gt_cell_12k/25k/35k_min_captbl a4/t4_gt_cell_12k/25k/35k_typ_captbl qrcTechFile	<i>CSMC 0.153um CMOS EN process 4 metal qrc gate level extraction files Cadence Tools</i>
a5/t5_gt_cell_12k/25k/35k_max.ict a5/t5_gt_cell_12k/25k/35k_min.ict a5/t5_gt_cell_12k/25k/35k_typ.ict a5/t5_gt_cell_12k/25k/35k_max_captbl a5/t5_gt_cell_12k/25k/35k_min_captbl a5/t5_gt_cell_12k/25k/35k_typ_captbl qrcTechFile	<i>CSMC0.153um CMOS EN process 5 metal qrc gate level extraction files Cadence Tools</i>
a6/t6_gt_cell_12k/25k/35k_max.ict a6/t6_gt_cell_12k/25k/35k_min.ict a6/t6_gt_cell_12k/25k/35k_typ.ict a6/t6_gt_cell_12k/25k/35k_max_captbl a6/t6_gt_cell_12k/25k/35k_min_captbl a6/t6_gt_cell_12k/25k/35k_typ_captbl qrcTechFile	<i>CSMC 0.153um CMOS EN process 6 metal qrc gate level extraction files Cadence Tools</i>

Library Cell List

The **csmc0153 CMOS EN process 5V** internal library supports a rich set of variable functions. It includes the following types of function cells:

ad Full Adder GATES
ah Half Adder GATES
aoi AND-NOR GATES
aor..... AND-OR GATES
an.....AND GATES
buff.....Buffer GATES
buft.....TRI-STATE BUFFER
df.....D Flip-Flop
dl.....Delay GATES
filler Filler CELL GATES
inv.....INVERTER GATES
la.....LATCH GATES
mi.....Inverting MUX GATES
mx.....MUX GATES
nd.....NAND GATES
nr.....NOR GATES
oai.....OR-NAND GATES
or.....OR GATES
sd.....Scan D Flip-Flop
tla.....Clock Gating
xn.....XNOR GATES
xr.....XOR GATES

Cells listed below:

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Arithmetic Gates	
ad01dN	1-bit FULL ADDER (0,1,2)
ah01dN	1-bit Half Adder (0,1,2)

Buffers Gates

buffdN	Non Inverting(0,1,2,3,4,5,6,8,10)
buftdN	Non-inverting 3-state Buffer with active low enable (0,1,2)
buftldN	Non-inverting 3-state Buffer with active high enable (0,1,2)
inv0dN	Inverter (0,1,2,3,4,5,6,8,10)
invtdN	Inverter 3-state Buffer with active low enable (0,1,2)
invtldN	Inverter 3-state Buffer with active high enable (0,1,2)
dl01dN	Delay Gate(0,1,2)
dl02dN	Delay Gate(0,1,2)

COMPLEX Gates

aoi21dN	AND-NOR 2,1 (0,1,2)
aoi31dN	AND-NOR 3,1 (0,1,2)
aoi32dN	AND-NOR 3,2 (0,1,2)
aoi33dN	AND-NOR 3,3 (0,1,2)
aoi22dN	AND-NOR2,2 (0,1,2)
aoi211dN	AND-NOR 2,1,1 (0,1,2)
aoi221dN	AND-NOR 2,2,1 (0,1,2)
aoim21dN	AND-NOR2,1 2 invt (0,1,2)
aoim22dN	AND-NOR2,2 2 invt (0,1,2)
aoim31dN	AND-NOR3,3 1invt (0,1,2)
oai21dN	OR-NAND2,1 (0,1,2)
oai31dN	OR-NAND3,1 (0,1,2)
oai32dN	OR-NAND3,2 (0,1,2)
oai33dN	OR-NAND3,3 (0,1,2)
oai22dN	OR-NAND2,2 (0,1,2)
oai211dN	OR-NAND2,1,1 (0,1,2)
oai221dN	OR-NAND2,2,1 (0,1,2)
oai222dN	OR-NAND2,2,2 (0,1,2)
oai311dN	OR-NAND3,1,1 (0,1,2)
oai321dN	OR-NAND3,2,1 (0,1,2)
oai322dN	OR-NAND3,2,2 (0,1,2)
oaim21dN	OR-NAND2,1 2 invt (0,1,2)
oaim22dN	OR-NAND2,2 2 invt (0,1,2)
oaim211dN	OR-NAND2,1,1 2 invt (0,1,2)
oaim2m11dN	OR-NAND2,1 1 3 invt (0,1,2)

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oaim31dN	OR-NAND3,1 3 invt (0,1,2)
aor21dN	AND-OR 2,1 (0,1,2)
aor22dN	AND-OR 2,2 (0,1,2)
aor211dN	AND-OR 2,1,1(0,1,2)
aor221dN	AND-OR 2,2,1 (0,1,2)
aor31dN	AND-OR 3,1 (0,1,2)
aor311dN	AND-OR 3,1,1 (0,1,2)
ora211dN	OR -AND 2,1,1 (0,1,2)
ora21dN	OR -AND 2,1 (0,1,2)
ora311dN	OR -AND 3,1,1 (1,2)
ora31dN	OR -AND 3,1 (0,1,2)

Gates

an02dN	AND 2 input (0,1,2)
an03dN	AND 3 input (0,1,2)
an04dN	AND 4 input (0,1,2)
an12dN	AND 2 input 1 invt (0,1,2)
an13dN	AND 3 input 1 invt (0,1,2)
an23dN	AND 3 input 2 invt (0,1,2)
nd02dN	NAND 2 input (0,1,2)
nd12dN	NAND 2 input 1 invt (0,1,2)
nd03dN	NAND 3 input (0,1,2)
nd13dN	NAND 3 input 1 invt (0,1,2)
nd04dN	NAND 4 input (0,1,2)
nd14dN	NAND 4 input 1 invt (0,1,2)
nd23dN	NAND 3 input 2 invt (0,1,2)
nd24dN	NAND 4 input 2 invt (0,1,2)
nr02dN	NOR 2 input (0,1,2)
nr12dN	NOR 2 input 1 inv (0,1,2)
nr03dN	NOR 3 input (0,1,2)
nr13dN	NOR 3 input 1 inv (0,1,2)
nr04dN	NOR 4 input (0,1,2)
nr14dN	NOR 4 input 1 inv (0,1,2)
nr23dN	NOR 3 input 2 inv (0,1,2)
nr24dN	NOR 4 input 2 inv (0,1,2)
or02dN	OR 2 input (0,1,2)
or03dN	OR 3 input (0,1,2)
or04dN	OR 4 input (0,1,2)
or12dN	OR 2 input 1 inv (0,1,2)
or13dN	OR 3 input 1 inv (0,1,2)
or23dN	OR 3 input 1 inv (0,1,2)

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xn02dN	Excl-NOR 2 input (0,1,2)
xn03dN	Excl-NOR 3 input (0,1,2)
xr02dN	Excl-OR 2 input (0,1,2)
xr03dN	Excl-OR 3 input (0,1,2)

MULTIPLEXERS

mx02dN	Mux 2-to-1 (0,1,2)
mi02dN	Inverting Mux 2-to-1 (0,1,2)
mx04dN	Mux 4-to-1 (0,1,2)
mi04dN	Inverting Mux 4-to-1 (0,1,2)

FLIP FLOPS

dfbfbN	Neg. Edge DFF, preset & clear (1,2)
dfbrbN	Pos. Edge DFF, preset & clear (1,2)
dfbrqN	Pos. Edge DFF, preset & clear, Q only (1,2)
dfcfbN	Neg. Edge DFF, clear (1,2)
dfcfqN	Neg. Edge DFF, clear, Q only (1,2)
dfcrbN	Pos. Edge DFF, clear (1,2)
dfcrnN	Pos. Edge DFF, clear, QN only (1,2)
dfcrqN	Pos. Edge DFF, clear, Q only (1,2)
dfnfbN	Neg. Edge DFF (1,2)
dfnrbN	Pos. Edge DFF (1,2)
dfnrrnN	Pos. Edge DFF, QN only (1,2)
dfnrqN	Pos. Edge DFF, Q only (1,2)
dfpfbN	Neg. Edge DFF, active-low preset (1,2)
dfprbN	Pos. Edge DFF, active-low preset (1,2)
dfprqN	Pos. Edge DFF, active-low preset, Q only (1,2)

LATCHES

labhbN	D latch, active-high enable, preset & clear (1,2)
lablbN	D latch, active-low enable, preset & clear (1,2)
lanhbN	D latch, active-high enable (1,2)
lanlbN	D latch, active-low enable (1,2)
lachbN	D latch, active-high enable, clear (1,2)
lachqN	D latch, active-high enable, clear , Q only (1,2)
laclbN	D latch, active-low enable, clear (1,2)
laclqN	D latch, active-low enable, clear , Q only (1,2)
laphbN	D latch, active-high enable, preset (1,2)
laplbN	D latch, active-low enable, preset (1,2)
lanhnN	D latch, active- high enable, QN only (1,2)

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lanhqN	D latch, active- high enable, Q only (1,2)
lanlnN	D latch, active-low enable , QN only (1,2)
lanlqN	D latch, active-low enable , Q only (1,2)
lanhtN	D latch, active-high enable ,three tristate ,Q only (1,2)

SCAN FLIP FLOPS

sdbrbN	Pos.Edge Scan DFF, active-low set and clear (1,2)
sdbfbN	Neg.Edge Scan DFF, active-low set and clear (1,2)
sdbrqN	Pos.Edge Scan DFF, active-low set and clear, Q only (1,2)
sdcfbN	Neg.Edge Scan DFF, active-low clear (1,2)
sdcfqN	Neg.Edge Scan DFF, active-low clear, Q only (1,2)
sdcrbN	Pos.Edge Scan DFF, active-low clear (1,2)
sdcrqN	Pos.Edge Scan DFF, active-low clear, Q only (1,2)
sdcrnN	Pos.Edge Scan DFF, active-low clear, QN only (1,2)
sdnfbN	Neg.Edge Scan DFF (1,2)
sdnrbN	Pos.Edge Scan DFF (1,2)
sdnrnN	Pos.Edge Scan DFF, QN only (1,2)
sdnrqN	Pos.Edge Scan DFF, Q only (1,2)
sdpfbN	Neg.Edge Scan DFF, active-low preset (1,2)
sdprbN	Pos.Edge Scan DFF, active-low preset (1,2)
sdprqN	Pos.Edge Scan DFF, active-low preset ,Q only(1,2)

CLOCK GATE

tlatncadN	Clock gating(1,2,4)
tlatntscadN	Clock enable gating(1,2,4)

MISCELLANEOUS

antenna	Antenna Diode
fillercap	Filler cap cell(4,8,16,32,64)
filler	Filler cell(1,2,4,8,16,32)
fillersub	fillersub
tiehi	Logic High
tielo	Logic Low