SC8, SC9, and SC12 Standard Cell Libraries for 65nm and Larger Process Nodes

Revision: r0p0

User Guide

Confidential

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SC8, SC9, and SC12 Standard Cell Libraries for 65nm and Larger Process Nodes
User Guide

Release Information

The following changes have been made to this book.

Change history

Date	Issue	Confidentiality	Change
04 December 2012	A	Confidential	First release for r0p0

Proprietary Notice

Confidentiality Status

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Product Status

The information in this document is final, that is for a developed product.

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SC8, SC9, and SC12 Standard Cell Libraries for 65nm and Larger Process Nodes User Guide

Preface

This preface introduces the *SC8, SC9, and SC12 Standard Cell Libraries for 65nm and Larger Process Nodes*. It contains the following sections:

About this book

This book is for the *4SC8, SC9, and SC12 Standard Cell Libraries for 65nm and Larger Process Nodes*.

Product revision status

The r*n*p*n* identifier indicates the revision status of the product described in this book, where:

r*n* Identifies the major revision of the product.

p*n* Identifies the minor revision or modification status of the product.

Intended audience

This book is written for experienced designers who are using this product in a design. The intended audience requires no knowledge or experience of ARM products.

Using this book

This book is organized into the following chapters:

Chapter 1 *Introduction*

Read this for the description of ARM Multi-channel libraries and overview of the parameters.

Chapter 2 *Global Parameters*

Read this for timing and power parameters and two metal layer implementation.

Chapter 3 *Special Cells*

Read this for the description of the special cells in this library.

Read this for information on naming conventions followed in this library.

Appendix A *Revisions*

Read this for the technical differences between the different releases.

Glossary

The *ARM Glossary* is a list of terms used in ARM documentation, together with definitions for those terms. The *ARM Glossary* does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See *ARM Glossary*, `http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html`.

Conventions

This book uses the conventions that are described in:

- *Typographical conventions* on page vii.
- *Timing diagrams* on page vii.
- *Signals* on page viii.

Typographical conventions

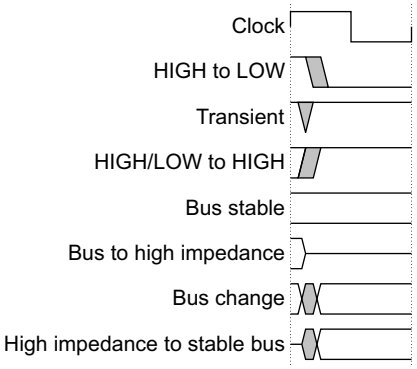
The following table describes the typographical conventions:

Style	Purpose
italic	Introduces special terminology, denotes cross-references, and citations.
bold	Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.
`monospace`	Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.
`monospace`	Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
`monospace` *`italic`*	Denotes arguments to monospace text where the argument is to be replaced by a specific value.
`monospace bold`	Denotes language keywords when used outside example code.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0 <Rd>, <CRn>, <CRm>, <Opcode_2>`
SMALL CAPITALS	Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The figure named *Key to timing diagram conventions* explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Key to timing diagram conventions

Timing diagrams sometimes show single-bit signals as HIGH and LOW at the same time and they look similar to the bus change shown in *Key to timing diagram conventions*. If a timing diagram shows a single-bit signal in this way then its value does not affect the accompanying description.

Signals

The signal conventions are:

Signal level The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals
- LOW for active-LOW signals.

Lower-case n At the start or end of a signal name denotes an active-LOW signal.

Additional reading

See ARM Information Center, http://infocenter.arm.com, for access to ARM documentation.

Feedback

ARM welcomes feedback on this product and its documentation.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to `errata@arm.com`. Give:

- the title
- the number, DUI0702A
- the page numbers to which your comments apply
- a concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

Customer support

If you have an active support contract then go to *DesignStart - Online Access to ARM IP*, http://www.arm.com/support/designstart.php and then login to obtain prompt attention to issues and questions about your ARM Physical Intellectual Property product.

Go to *Support and Maintenance*, http://www.arm.com/support/services/support-maintenance.php and select the **Physical IP** tab for information about support contract options.

If you cannot contact ARM through the web support channel then send an e-mail to `support-pipd@arm.com`.

Chapter 1
Introduction

This chapter introduces the ARM Multi-Channel library. It contains the following sections:

- *ARM standard cell libraries* on page 1-2.

1.1 ARM standard cell libraries

ARM 65nm and larger standard cell libraries build upon years of experience with multiple standard cell architectures. The cell line for each is derived from extensive customer design, synthesis, and place-and-route benchmark analysis. Library optimization is achieved by carefully matching the library functions and drive strengths to leading synthesis and place-and-route tools, producing superior RTL-to-GDSII results. SC9 libraries offer an optimal mix of performance, power, and area, ideal for mainstream applications. The ARM SC12 are high speed libraries targeting performance-critical designs while still optimizing power. SC8 libraries are optimized for high density, low-power applications. This user guide presents information for SC12 libraries.

Chapter 2
Global Parameters

This chapter describes the global parameters of this library. See *Technical Overview* in your databook for values specific to your library.

Note

For any shrink processes, all area numbers in the library and documentation are pre-shrink. All performance numbers in the library and documentation are post-shrink.

This chapter contains:

2.1 Propagation delays

The propagation delay through a cell is the sum of the intrinsic delay, the load-dependent delay, and the input-slew dependent delay. Delays are defined as the time interval between the input stimulus crossing the rising time percentage of **Vdd** and the output crossing the falling time percentage of **Vdd**. Libraries are usually characterized with delays at either 50% rising time or 50% falling time. See *Technical Overview* in your databook for values specific to your library. See Figure 2-1.

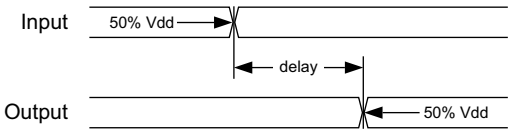


Figure 2-1 Propagation Delays at 50/50

The transition times (slews) on input and output pins are defined as the time interval between the signal crossing 10% of **Vdd** and 90% of **Vdd**. See Figure 2-2.

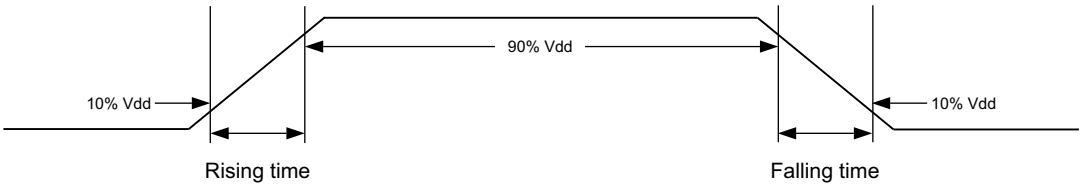


Figure 2-2 Transition Time

Factors that affect propagation delays and transition time include:

- Temperature.
- Supply voltage.
- Process variations.
- Fanout loading.
- Interconnect loading.
- Input transition time.
- Input signal polarity.
- Timing constraints.

The timing models provided with this library include the effects of input-transition time on propagation delays. Also, NLDM timing models use a table lookup method to calculate accurate timing. The standard cell datasheets provide all timing numbers for the input slew specified in the *Technical Overview* accompanying your datasheets. All cells have been characterized with a physical overlay to more closely resemble a cell placed in a block for accurate characterization. See *Technical Overview* in your databook for values specific to your library.

The library might contain negative propagation delays. Although most third-party verification tools can handle negative propagation delays, some tools turn negative delays into a zero value.

2.2 Timing constraints

Timing constraints define minimum time intervals during which specific signals must be held steady to ensure the correct functioning of any given cell. Timing constraints include:

- Setup time.
- Hold time.
- Recovery time.
- Removal time.
- Minimum pulse width.

The sequential cell timing models provided with this library include the effects of input transition time, data signal and clock signal polarity on timing constraints. Factors that affect timing constraints include:

- Temperature.
- Supply voltage.
- Slew rates.
- Process variations.

All cells have been characterized with a physical overlay to more closely resemble a cell placed in a block for accurate characterization. See *Technical Overview* in your databook for values specific to your library. Timing constraints can affect propagation delays. The intrinsic delays given in the datasheets are measured with relaxed timing constraints longer than necessary setup times, hold times, recovery times, and pulse widths. The use of shorter timing constraint intervals might increase delay. Each cell is considered functional as long as the actual delay does not exceed the delay given in the datasheets by more than 10%.

2.3 Setup time

The setup time for a sequential cell is the minimum length of time the data input signal must remain stable before the active edge of the clock or other specified signal to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output to reach its expected value does not exceed the reference delay measured with a large setup time by more than 10%. Setup constraint values are measured as:

- The interval between the data signal crossing rising time percentage of **Vdd** for rising data or the interval between the data signal crossing falling time percentage of **Vdd** for falling data.
- The clock signal crossing rising time percentage of **Vdd** for rising clocks or the clock signal crossing falling time percentage of **Vdd** for falling clocks.

Libraries are usually characterized with delays at 50% rising time or 50% falling time. See *Technical Overview* in your databook for values specific to your library. For the measurement of setup time, the data input signal is kept stable after the active clock edge for an infinite hold time. See Figure 2-3 for setup time for a positive-edge-triggered sequential cell with delays at 50/50.

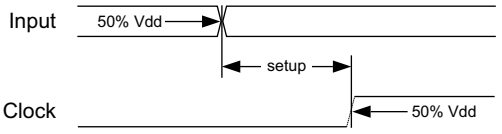


Figure 2-3 Setup Time with Delays at 50/50

2.4 Hold time

The hold time for a sequential cell is the minimum length of time the data input signal must remain stable after the active edge of the clock or other specified signal, to ensure proper functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay, measured with a large hold time, by more than 10%. Hold constraint values are measured as:

- The interval between the data signal crossing rising time percentage of **Vdd** for rising data or falling time percentage of **Vdd** for falling data.
- The clock signal crossing rising time percentage of **Vdd** for rising clocks or falling time percentage of **Vdd** for falling clocks.

Libraries are usually characterized with delays at either 50% rising time or 50% falling time. See *Technical Overview* in your databook for values specific to your library. For the measurement of hold time, the data input signal is held stable before the active clock edge for an infinite setup time. See Figure 2-4.

Note

ARM does not incorporate any hold time margins in the timing models. Chip designers must develop a timing methodology to account for chip-level timing inaccuracies inherent to extraction and timing analysis tools.

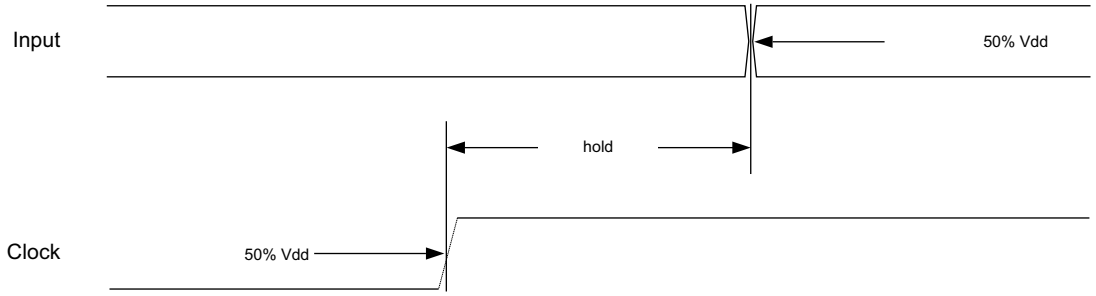


Figure 2-4 Hold Time with Delays at 50/50

2.5 Recovery time

Recovery time for sequential cells is the minimum length of time that the active-LOW set or reset signal must remain HIGH before the active edge of the clock to ensure proper functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay, measured with a large recovery time, by more than 10%.

Recovery constraint values are measured as:

- The interval between the set or reset signal crossing rising time percentage of **Vdd** for active-LOW or falling time percentage of **Vdd** for active-HIGH set or reset signals.
- The clock signal crossing rising time percentage of **Vdd** for rising clocks, or falling time percentage of **Vdd** for falling clocks.

Libraries are usually characterized with delays at either 50% rising time or 50% falling time. See *Technical Overview* in your databook for values specific to your library. For the measurement of recovery time, the set or reset signal is held stable after the active clock edge for an infinite hold time. See Figure 2-5.

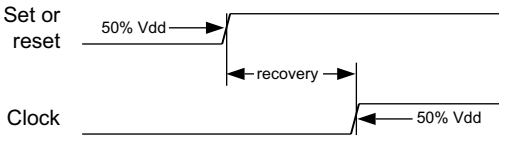


Figure 2-5 Recovery Time with Delays at 50/50

2.6 Removal time

Removal time for sequential cells is the minimum length of time that the active-LOW set or reset signal must remain LOW after the active edge of the clock to ensure proper functioning of the cell. The cell is considered functional as long as the active clock edge does not latch in a new data value from that programmed by the asynchronous set or reset signal.

Removal constraint values are measured as:

- The interval between the set or reset signal crossing rising time percentage of **Vdd** for active-LOW or falling time percentage of **Vdd** for active-HIGH set or reset signals.
- The clock signal crossing rising time percentage of **Vdd** for rising clocks or falling time percentage of **Vdd** for falling clocks.

Libraries are usually characterized with delays at either 50% rising time or 50% falling time. See *Technical Overview* in your databook for values specific to your library. For the measurement of removal time, the set or reset signal is held stable before the active clock edge for an infinite setup time. See Figure 2-6.

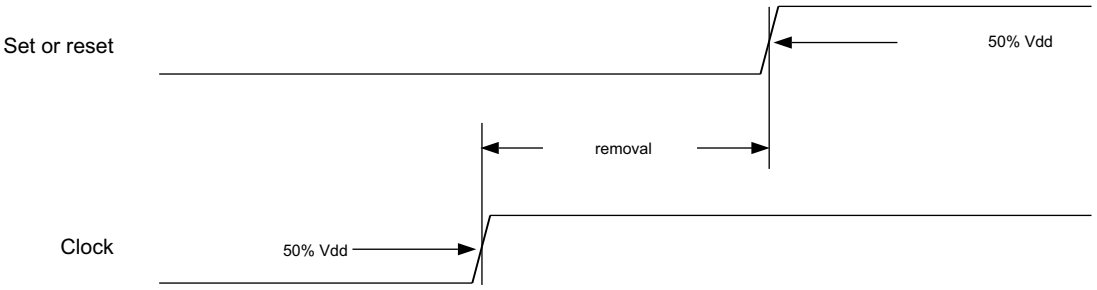


Figure 2-6 Removal Time with Delays at 50/50

2.7 Minimum pulse width

Minimum pulse width is the minimum length of time between the leading and trailing edges of a pulse waveform.

- *Minimum pulse width HIGH* (minpwh) is measured as the interval between the rising edge of the signal crossing rising time percentage of **Vdd** and the falling edge of the signal crossing falling time percentage of **Vdd**.
- *Minimum pulse width LOW* (minpwl) is measured as the interval between the falling edge of the signal crossing falling time% of **Vdd** and the rising edge of the signal crossing rising time% of **Vdd**.

Libraries are usually characterized with delays at either 50% rising time or 50% falling time. See *Technical Overview* in your databook for values specific to your library. See Figure 2-7.

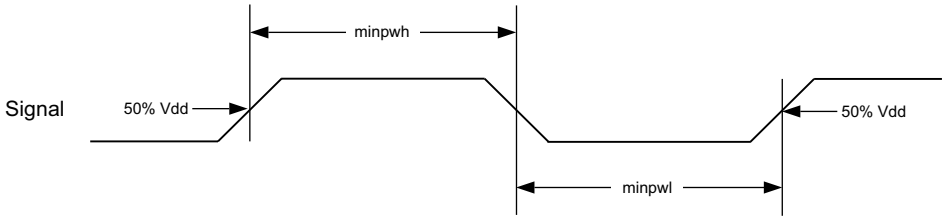


Figure 2-7 Minimum Pulse Width with Delays at 50/50

2.8 Electromigration

ARM standard cell libraries are designed to meet foundry *ElectroMigration (EM)* guidelines for normal chip design usage. However, you must ensure that the design meets:

- Electromigration guidelines are met at the chip level to foundry guidelines.
- ARM guidelines for library use.

You must meet the following EM guidelines to ensure safe use of the standard cell library within the electromigration guidelines of the foundry.

- The metal2 **Vdd** and **Vss** power buses in the standard cells must be wide enough to provide adequate current to the cells.
- The output pin metal for each standard cell must be wide enough to accommodate multiple vias when necessary to meet via EM guidelines. However, oversized metal output pins do not require multiple vias. The number of vias required to meet EM guidelines depends on the design. You must use an appropriate number of vias and wire widths when routing from an output pin.
- You must design and verify that the connections between the standard cells comply with the EM guidelines of the foundry under normal usage. Normal usage is defined as follows:
  - Clock nets are assumed to have an activity factor of 200%, because clock signals switch twice for every cycle in the design. Data nets are assumed to have an activity factor of 100% on average over time. Data signals are assumed to switch no more than ten times for every ten clock cycles on average over time.
  - The current required by the cell does not exceed the maximum current and can be supplied by the metal2 power buses.
  - For a cell outside the clock tree network, the output transition times for any of the output pins of the cell, measured using 10% and 90% thresholds, must not be higher than 20% of the total cycle time, or must not be greater than 10% of the cycle time. Limiting the output transition time limits the load driven by the cell. This reduces the current of that cell to comply with the EM guidelines. Ratios larger than 20% are not appropriate for commonly used design flows and are unlikely to be encountered in normal designs.
  - For a cell in the clock tree network, transition times must not exceed 10% of the total cycle time for that cell.
  - Some high drive clock cells require more stringent transition time requirements because they can potentially drive large capacitive loads at higher frequencies. You must take extra care when using these high drive clock cells.

See *Maximum transition time and Maximum Wire Length* in your library databook for more information on setting constraints to address EM considerations.

2.9 Power dissipation

The library is designed to dissipate only AC power, except for the small reverse-bias leakage currents that are normally present in all CMOS circuits. The internal power dissipation of a cell when an input switches is primarily a function of the cell topology. The power dissipation of a complete design, or part of a design using cells from the library, is primarily a function of the switching frequency of the internal nets for the design. These nets include the inputs and outputs of each cell and the capacitive load associated with the outputs of each cell.

The library datasheet provides the following tables:

- A power table that documents the internal energy consumption of each cell
- A pin capacitance table that gives input pin capacitance data used to compute output loading.

You can use this information, along with design-specific information to estimate the total power dissipation of a cell within a design. The power tables specify the amount of energy consumed within a cell (µW/MHz) when the corresponding pin changes state at typical temperature, typical voltage, and typical process. The energy data in the tables are measured for the input slew and no loading at the outputs of the library. For combinatorial cells, energy values are provided for only input pins. The energy value for each input pin is the average of energies associated with the input transitions that result in an output transition.

For sequential cells, the energy associated with each input pin is the average energy of those input transitions that do not result in an output transition. The energy associated with the output pin of a sequential cell is the average energy of all cases where an output transition is the result of a clock input transition, minus the energy associated with the clock input pin. In the event that a sequential cell has multiple outputs, all output energy data is associated with only one output pin.

2.10 Power calculation

Power dissipation depends on the power-supply voltage, frequency of the operation, internal capacitance, and output load. The power dissipated by each cell is:

$$P_{avg} = \sum_{n=1}^{x} (E_{in} \times f_{in}) + \sum_{n=1}^{y} (C_{on} \times Vdd^2 \times \frac{1}{2} f_{on}) + E_{os} \times f_{o1} + L$$

where:

P_{avg} average power (µW)

x number of input pins

E_{in} energy associated with the nth input pin (µW/MHz)

f_{in} frequency at which the n^{th} input pin changes state during the normal operation of the design (MHz)

y number of output pins

C_{on} external capacitive loading on the n^{th}h output pin, including the capacitance of each input pin connected to the output driver, plus the route wire capacitance, actual or estimated (pF)

V_{dd} operating voltage = typical voltage

f_{on} frequency at which the n^{th} output pin changes state during the normal operation of the design (MHz)

E_{os} energy associated with the output pin for sequential cells only (µW/MHz)

L leakage power (µW) for the cell

You can obtain the switching frequency of inputs and outputs of a particular cell in a design from a gate-level logic simulator, for example Verilog by applying typical input stimuli and measuring the activity on each node of interest. The total average power for the design is computed by adding the average power for each cell. Example 2-1 shows how to calculate the power for a DFFQ_X0P5M cell.

Example 2-1 Calculating power for a DFFQ_X0P5M cell:

For this example, assume the DFFQ_X0P5M cell has

- clock switching at 133MHz, clock frequency = 66.5MHz
- input and output pins switching at 20MHz
- cell leakage power of 0.001µW
- an external capacitance loading on the output pin of 0.02pF.

Using the AC Power table, the power dissipated by the DFFQ_X0P5M cell can be calculated by using the following equation:

$$P_{avg} = \sum_{n=1}^{x} (E_{in} \times f_{in}) + \sum_{n=1}^{y} (C_{on} \times Vdd^2 \times \frac{1}{2} f_{on}) + E_{os} \times f_{o1} + L$$

Given:

x	2
E_{i1}	0.0056 µW/MHz
E_{i2}	0.0063 µW/MHz
f_{i1}	20 MHz
f_{i2}	133 MHz
y	2
C_{o1}	0.02
C_{o2}	0.02
V_{dd}	1.0V
f_{o1}	20 MHz
f_{o2}	20 MHz
E_{os}	0.0060 µW/MHz

we have:

$$P_{avg} = \sum_{n=1}^{2} (E_{in} \times f_{in}) + \sum_{n=1}^{2} (C_{on} \times Vdd^2 \times \frac{1}{2} f_{on}) + E_{os} \times f_{o1} + L$$

$$P_{avg} = (E_{i1} \times f_{i1}) + (E_{i2} \times f_{i2}) + (C_{o1} \times Vdd^2 \times \frac{1}{2} f_{o1}) + (C_{o2} \times Vdd^2 \times \frac{1}{2} f_{o2}) + (E_{os} \times f_{o1}) + L$$

$P_{avg} = (0.0056 \times 20) + (0.0063 \times 133) + (0.02 \times 1.0 \times 1/2\ (20)) + (0.02 \times 1.0 \times 1/2\ (20)) + (0.0060 \times 2.0) + 0.001)$

$P_{avg} = 1.4709\mu W$

2.11 Power rail and network requirements and settings

This section describes the requirements and settings for power rail and network, and it has the following subsections:

- *Power strapping*
- *Estimating power strapping on metal3*
- *IR-drop, L*Di/Dt and edge rates* on page 2-14.

2.11.1 Power strapping

Metal2 rails and connecting V1s are built into the standard cell layouts. ARM recommends using metal3 power straps to supplement the metal2 rails. You must add vertical metal3 power buses and distribute these buses evenly, between power and ground. Metal3 width must match the width of the metal2 power rails.

2.11.2 Estimating power strapping on metal3

This section provides a rough estimate with many simplifying assumptions. For a given module design, you can estimate the amount of vertical power-rail strapping that is required to fulfill electromigration requirements.

Note

Vss or **Vdd** rails are on metal1 or metal2 for 45nm and smaller standard cell products. Therefore strapping must be performed with vertical metal3.

Given,

$\mathbf{I_{avg}}$	total average current for the module calculated. See *Power calculation* on page 2-11
$\mathbf{w_{m2}}$	**Vss** or **Vdd** metal2 wire width (µm). See *Technical Overview* in your databook for values specific to your library.
r	number of rows in the module
$\mathbf{d_{m2}}$	maximum metal2 current density allowed for the process (mA/µm)
$\mathbf{d_{m3}}$	maximum metal3 current density allowed for the process (mA/µm)
$\mathbf{I_{m2}}$	maximum current that is supported by all horizontal metal2 wires (mA)
$\mathbf{I_{strap}}$	total current that must be supported by the vertical metal3 strapping (mA)
$\mathbf{w_{m3}}$	metal3 wire width required for vertical strapping (µm)
c	minimum number of metal3 straps

We have:

$I_{m2} = w_{m2} \times r \times 2 \times d_{m2}$

where multiplying by 2 means the metal2 wires are supplied from both ends

$I_{strap} = (I_{avg} - I_{m2})/2,$

where dividing by 2 means the metal3 vertical strap wires are supplied from both ends

$w_{m3} = I_{strap}/d_{m3}$

The metal3 wire width, w_{m3}, must be divided into a minimum of c equal portions that are spaced equidistant across the module, where rounded up to the next integer.

$c = I_{avg}/I_{m2}$

ARM recommends that the metal3 wire width, w_{m3}, be distributed evenly so that individual m3 straps have the same width as the m2 power rails. You must give the same consideration to the number of vias used to connect the metal2 and metal3 straps.

2.11.3 IR-drop, L*Di/Dt and edge rates

In general, the Di/Dt response of any supply grid must be designed with consideration to the fundamental frequencies of the edge rates and not the clock period.

The IR drop is a strong function of clock frequency because average current is a strong function of clock frequency. Also, cell delay is very non-linear with voltage as little as a 10% reduction from the nominal supply. You must not seek average impact of Di/Dt out over the cycle and get a simple averaging of cell delay. You must ensure that the average delta V below the nominal supply is higher than the 10% supply collapse used for characterization to ensure the performance that voltage indicates.These supply recommendations have the underlying assumption that the top level thick metals are doing most of the work to minimize the IR drop, while the m2 and m3 grid is doing most of the work to minimize the Di/Dt impact.

Chapter 3
Special Cells

This library has following special cells.

3.1 Special cells

This section discusses special cells that may be included in your library. Descriptions of cells not included with your product are additional options available from ARM.

3.1.1 Antenna Fix cells

The library contains an antenna-fix cell which must be inserted manually. However, most place and route tools indicates which nets require the antenna-fix cell. Refer to the antenna effect prevention guideline of the foundry specified in your library README, for maximum wire width. During place and route, the router might connect wires to the input gates of cells that are longer than the maximum length allowable by the guideline. The antenna cell can be used in this case to add an optional diode on the net close to the input gates which do not meet the guideline.

Pin A on the antenna cell connects to a diode, reverse biased to ground.

3.1.2 Delay cells

The library contains delay cell, or families of delay cells, that have the same width. These delay cells allow you to adjust a given delay path with a simple cell substitution after place and route.

3.1.3 ENDCAP and ENDCAPTIE cells

If your library supports triple well design it is required to be NWELL-enclosed. The cell used to terminate a standard cell row and fulfill the NWELL antenna requirement is shown in the Twin/Triple Well Support table in the Technical Overview section of your databook. Additionally, a double-cell row is also required to ensure that the top and bottom rows, together with the terminus cell, form an enclosed NWELL. The wells are left floating in the case of ENDCAP cells, and are tied to power rails in the case of ENDCAPTIE cells.

If your library contains a FILLTIESB cell and you are designing for triple-well, then you must also place the FILLTIESB cell outside the ENDCAP cells. Consider the FILLTIESB as an endcap to the ENDCAP cell. It is only needed for triple-well designs, in order to fulfill the well antenna requirement for connecting to substrate.

Figure 3-1 on page 3-3 illustrates the NWELL with ENDCAP cells.

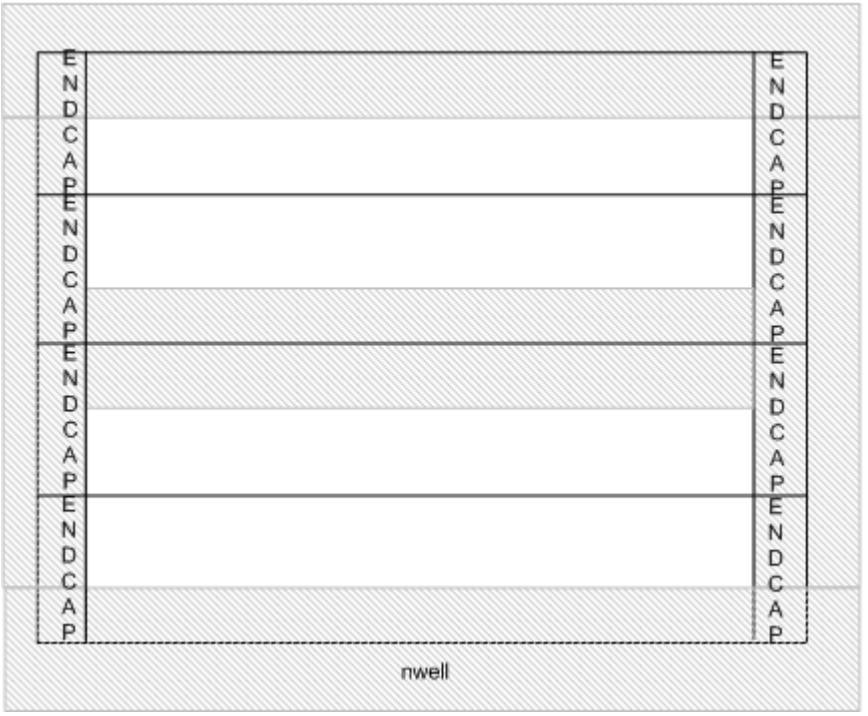


Figure 3-1 NWELL with ENDCAP/ENDCAPTIE cells

The ENDCAP cell extends the NWELL in east/west cell orientation directions to reduce well proximity effects and for OD to OD space mitigation. It is not for triple well support, nor does it include well antennas. The GDS2 for FILLTIE3 and ENDCAP3 is identical.

3.1.4 FILLCAP cells

The FILLCAP cells can have either of the following topologies:

1. *Gate connected to supply*.
2. *Cross-coupled structure* on page 3-4.

Gate connected to supply

The FILLCAP cells function as FILL cells with decoupling capacitors. In this topology, the cells connect gate inputs directly to the power or ground rail. This might violate the foundry *Electrical Rules Checker (ERC)*. However, if the FILLCAPs are used in a block that is power gated then the gate input is not directly connected to the power rail. Instead, the gate input connection goes through the power gate. ARM recommends using of these cells in power gated blocks.

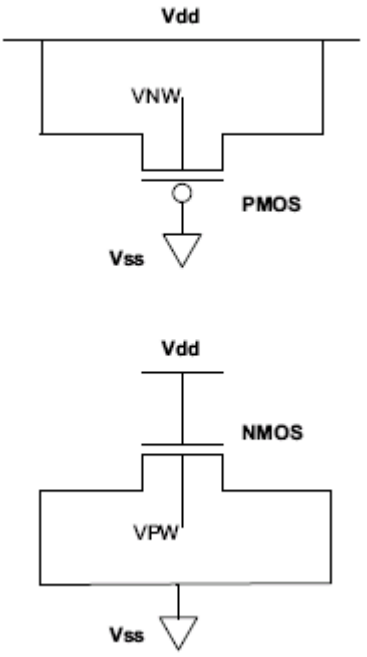


Figure 3-2 Gate conneted to supply

Cross-coupled structure

FILLCAP cells function as FILL cells with decoupling capacitors. Inside the FILLCAP, PMOS and NMOS devices form decoupling capacitors between the Vdd and Vss rails, reducing ground bounce in the power grids. The wells are left floating in the case of FILLCAP cells.

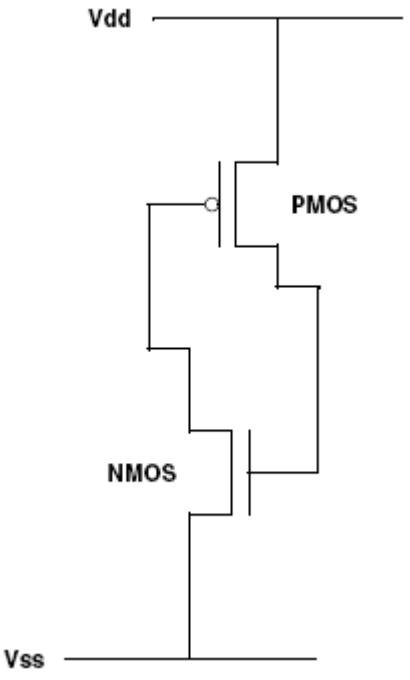


Figure 3-3 Cross-coupled structure

3.1.5 FILLCAPTIE Cells

FILLCAPTIE cells function as FILL cells. Inside the FILLCAPTIE, PMOS and NMOS devices form decoupling capacitors between the Vdd and Vss rails, reducing ground bounce in the power grids. The wells are tied to power rails in the FILLCAPTIE cells.

Figure 3-4 shows the FILLCAPTIE functional schematic.

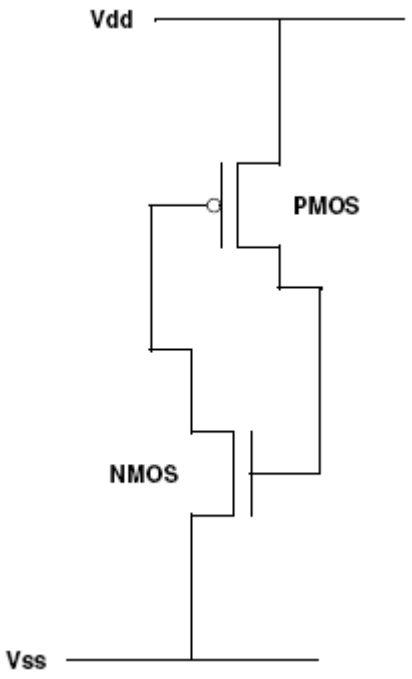


Figure 3-4 FILLCAPTIE functional schematic

3.1.6 Low-Power (XL) Cells

The library may contain a wide variety of cells, denoted by an "XL" suffix in the cell name, that are designed specifically for low-power applications. Input capacitance for the XL cells is much lower than that for corresponding X1 (1x drive strength) cells. Because XL cells have been designed for the sole purpose of reducing power consumption, output rise and fall times for these cells may not be equal, and due to the low-drive capability of the XL cells, these cells are not intended for use in critical timing paths, or to drive heavily loaded nets.

3.1.7 FILL*TIE-NWELL and Substrate Tie cell

SC8, SC9, and SC12 libraries do not have well or substrate ties inside the cells. You are required to tie the NWELLs to Vdd and the substrate to Vss before place-and-route using the FILL*TIE cell. Before place-and-route, pre-place the FILL*TIE cell periodically in every placement row. You must place the FILL*TIE cell as frequently as the design requires. For example, if the design rules require a well or substrate connection every 20um, then the FILL*TIE cell must be pre-placed every 20um. See Figure 3-5 on page 3-6 for sample placement.

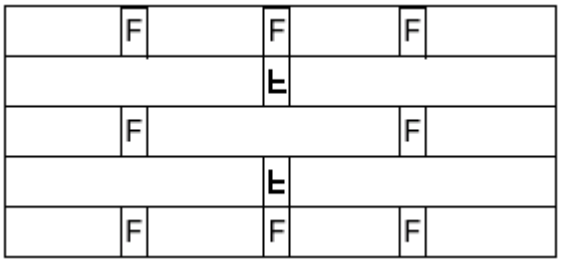


Figure 3-5 Sample Placement of FILLTIE Cells for 20um NWELL and Substrate Tie Design Rule

Note

The letter "F" indicates a FILL*TIE cell placed in normal orientation, and the letter "F" flipped upside down indicates a FILL*TIE cell placed in MY orientation.

In all rows except for the top and bottom rows, the NWELL and substrate are shared by two adjacent placement rows. This allows you to place the FILL*TIE cell only half as frequently as the design rules require. Remember to stagger the placement in the adjacent rows by an amount equal to the design row.

Assuming that the rule is every 20um, you need to place FILL*TIE cells every 20um in the top and bottom rows. If you stagger the placement by 20um between adjacent rows, you can place FILL*TIE cells every 40um for all rows between the top and bottom rows. This method allows every row to have well and substrate ties every 20um.

It is also possible to place the FILL*TIE cells in columns, skipping alternate rows. The distance betweek the FILL*TIE cells in this configuration is half the distance of the staggered configuration. For example, the closer together cells are placed 10um apart in the example, but every other row is free of FILL*TIE cells. Alternatively, you could place FILL*TIE cells 20um apart in every other row. The remaining rows would not require any FILL*TIE cells.

3.1.8 Register File cells

Register file cells (RF*) may be provided to support creating very small memories from standard cells. The register file bit cells (RF1R1W, RF2R1W, RF1R2W, RF2R2W) have tri-state outputs. You must tie these tri-state outputs together on a bit line and have this bit line drive function as an output buffer. The library contains a number of inverting and non-inverting buffers (INV*, BUF*, BUFZ*) that can buffer the bit lines.

It is possible to make a memory that has a non-power-of-two word depth. If this is employed, it is possible to input an address to the memory such that none of the bit cells are addressed and nothing is driving the bit line. A floating bit line can cause the logic following it to go into a high power state, therefore, users must take special care when designing a memory with a non-power-of-two word depth. Users must guarantee that the bit line is never allowed to float by ensuring that at least one bit cell is always driving the bit line, or that a floating bit line does not cause subsequent logic to go into a high power state. One way to achieve the latter is to use an output buffer with an enable. NAND or AND gates or tri-state output buffers (NAND*, AND*, BUFZ*) can be used for this purpose. Whichever is used, be sure to generate an enable signal that only enables the output buffer when the bit line is not floating.

3.1.9 TIEHI and TIELO cells

The library may contain a TIEHI cell and a TIELO cell. The outputs of the TIEHI and TIELO cells are driven through diffusion to provide isolation from the power and ground rails for better ESD protection. The standard cell abstract methodology assumes that the TIEHI and TIELO cells are used to tie off any inputs to power and ground. If these cells are not used and the router is allowed to drop vias on the power rail, DRC errors or shorts may result.

3.1.10 Well Antenna cells

If your library contains the WELLANTENNA cell, this process requires that, for any standard cell row with a device in it, the NWELL must be tied down to the substrate and triple-wells must be tied to the enclosing NWELL. Any connection between the wells is usually sufficient. In a triple-well design, the connection happens automatically when you place the ENDCAPTIE cells at the ends of the standard cell rows. In triple-well and twin-well designs, any CMOS standard cell (such as an inverter) placed in a standard cell row will also make the connection; however, in a twin-well design, if a pair of standard cell rows, sharing an NWELL, or a single standard cell row is populated by nothing but FILL cells and/or ANTENNA cells and at least one FILLCAP cell, the associated NWELL will be in violation of the well antenna rule. In this scenario, the NWELL must be tied down to the substrate by inserting a WELLANTENNA cell into the standard cell row in violation.

3.1.11 Well Antenna Tie Cells

WELLANTENNATIEPW is a well antenna cell that ties one or more wells to a supply rail. If your library contains the WELLANTENNATIEPW cell, then this process requires that, for any standard cell row with a device in it, the NWELL must be tied down to the substrate and triple-wells must be tied to the enclosing NWELL. Any connection between the wells is usually sufficient. In a triple-well design, the connection will happen automatically when you place the ENDCAP cells at the ends of the standard cell rows. In triple-well and twin-well designs, any CMOS standard cell (such as an inverter) placed in a standard cell row will also make the connection; however, in a twin-well design, if a pair of standard cell rows, sharing an NWELL, or a single standard cell row is populated by nothing but FILL cells and/or ANTENNA cells and at least one FILLCAP cell, then the associated NWELL will be in violation of the well antenna rule. In this scenario, the NWELL must be tied down to the substrate by inserting a WELLANTENNATIEPW cell into the standard cell row in violation.

Chapter 4
Library Naming Conventions

The following naming conventions apply to ARM standard cell libraries:

4.1 Process, Voltage, and Temperature (PVT)

The Liberty files have a specific nomenclature that clearly identifies the PVT and other information used in extracting and characterizing the library. The general syntax for an ARM Standard Cell Liberty file that is both `.lib` and `.db`, in the lib/ and db/ directories, respectively is:

```
[product]_[process corner]_[extraction]_[overlay]_[voltage]_{voltage2}_[temp]
```

The `product` field contains several fields as follows:

```
sc[cell height]{mc}{architecture type}_[process node name]_[toolkit name]_[primary
threshold voltage]{_[secondary threshold voltage]}{_c[primary channel
length]}{_c[secondary channel length]}{_w3}
```

With the `product` field expanded, the complete syntax is:

```
sc[cell height]{mc}{architecture type}_[process node name]_[toolkit name]_[primary
threshold voltage]{_[secondary threshold voltage]}{_c[primary channel
length]}{_c[secondary channel length]}{_w3}_[process
corner]_[extraction]_[overlay]_[voltage]_{voltage2}_[temp]
```

Table 4-1 describes the fields in the file syntax.

Table 4-1 LIberty file syntax

Field	Description	Example
`sc`	Standard Cell represents all logic products; not a variable	`sc`
`cell height`	Track height of the library	12
`mc`	Optional. Used to indicate compatibility with other libraries in a given process. If present, the library is a multi-channel length library. If not, the library is a minimum channel length library.	`mc`
`architecture type`	Optional. Used if needed to distinguish compatibility with other libraries. All libraries with the same architecture type are compatible.	`p`
`process node name`	Process name as defined by the foundry	cln40lp
`toolkit name`	Describes type of library	base for a base standard cell library, PMK for a *Power Management Kit*, eco for an ECO kit, *High Density Low Power Kit* for HDLPK.
`primary threshold voltage`	Predominant implant threshold (Vt) used in the library	`rvt, hvt`
`secondary threshold voltage`	Optional. Defines a secondary implant threshold used in the library.	`rvt, hvt`
`c`	Channel. Required if `mc` field is present, identifies that the next value indicates the channel length in the library	`c`
`primary channel length`	Required if `mc` field is present; defines predominant channel length used in library	30
`secondary channel length`	Optional. Defines a secondary channel length used in the library.	34

Table 4-1 LIberty file syntax (continued)

Field	Description	Example
`triple well`	Triple well indicator. Optional. A library with full support of a triple-well process is indicated by a `_w3` at the end of the product name. This is used to differentiate it from a dual-well library of the same process.	`w3`
`process corner`	N and P transistor process corner used for characterization	ft for a fast n-channel corner and a typical p-channel corner
`extraction`	Parasitic extraction corner used	typical, nominal
`overlay`	Amount of overlay used for extraction	min max avg
`voltage`	Characterization voltage of form #p##v	1p20v (= 1.20V)
`voltage2`	Optional. Second characterization voltage used for cells with multiple voltage supplies such as level shifters	1p20v (= 1.20V)
`temp`	Temperature used for characterization	85c

4.2 Cell name fields

The library cell name has three separate fields. They are the root, drive strength, and library identifier. These three components are concatenated together in the following order:

```
[root]_[drive strength]_[library identifier]
```

For Example:

In the cell name, `SDFFQ_X1M_A12TR`

`SDFFQ`	Root field. Multiplexer-d scan flop with non-inverting output.
`X1M`	Drive strength field. 1 fold output stage with an M beta ratio.
`A12`	Library identifier field. ARM library at a 12 track pitch.
`TR`	Threshold voltage field. Regular or nominal threshold voltage cell.

In the cell name, `BUFH_X2P5B_A9TL`

`BUFH`	Root field. High speed buffer.
`X2P5B`	Drive strength field. 2.5 fold output stage with a B beta ratio.
`A9`	Library identifier field. ARM library at a 9 track pitch.
`TL`	Threshold voltage field. Low threshold voltage cell.

4.3 Root

This portion of the cell name defines the logical function of the cell. There is a large degree of variation in this field. A full definition of the root names are provided in *Root name* on page 4-9.

4.4 Drive strength

The library contains multiple beta ratios for some of the topologies. This requires that the naming convention indicates the different beta ratios. The convention is `X[number][beta ratio letter]`. The `X` plus the number field indicates how many folds are present. For example, one fold is indicated by `X1` and `X4` indicates four folds. The library also makes use of non-integer folds. This is useful for improving performance in addition to reducing power consumption. When a non-integer fold is present, a `P` indicates the decimal place. For example, a cell that contains 1.4 folds is indicated as `X1P4`. If the fold size is less than one, a zero prefixes the `P`. Currently, only one significant digit is used after the decimal place as this provides enough granularity.

There are many useful beta ratios. Table 4-2 lists all the beta ratios currently defined. ARM adopted the convention of null or no character to indicate flood-filled in its SC9 and SC12 libraries.

Table 4-2 Beta ratio letter definition

Letter	Description
null	Devices are drawn at the maximum size possible, regardless of topology
A	Tuned to minimize the average delay between the input edges
B	The delay for both edges are equal when the input driver is a balanced inverter
E	The output rising and falling edge rates are equal, assuming the input driver has equal rising and falling edge rates
M	Tuned to minimize the maximum delay between the input edges
F	Tuned so that the input to output delay of a falling output is improved

With the addition of the beta ratio indicator to the drive strength field the `CLK` prefix is dropped because this prefix indicated a `B` type beta ratio in previous SAGE-X libraries.

4.5 Library identifier

To support mixing different libraries on a single die, all ARM libraries have a unique library identifier field. This field is comprised of twelve subfields as follows. See Table 4-3.

```
A[cell height]T[primary threshold identifier]{T[secondary threshold
identifier]}{_C[primary channel length]}{C[secondary channel length]}{_W3[triple well
identifier]}
```

Table 4-3 Library identifier fields

Field	Description
`A`	Indicates this is an ARM library
`cell height`	Indicates the cell height of the library in tracks
`T`	Indicates the abbreviation for threshold.
`primary threshold identifier`	Indicates the primary threshold voltage of the library
`secondary threshold identifier`	Indicates the secondary threshold voltage of the library
`_C`	Indicates non-minimum channel length libraries
`primary channel length`	Indicates the drawn channel length in units of nanometers
`C`	Indicates if the product contains more than one channel length in one or more cells
`secondary channel length`	Optional. Defines a secondary channel length used in the library.
`triple well identifier`	Optional. Indicates triple well.
`_W3`	A library with full support of a triple-well process is indicated by a `_W3` at the end of the product name.

Table 4-4 on page 4-8 defines the legal values for this subfield and their meaning.

For example:

- `A12TL` identifies a twelve-track low threshold voltage minimum channel only library.
- `A9TH34` identifies a nine-track high threshold voltage 34nm channel length multi-channel compatible library.
- `A9TLTH_C30C34_W3` identifies a library with 9 track high cells with LVt as the primary Vt and 30nm as the primary channel length, HVt as the secondary Vt and 34nm as the secondary channel length, and fully supporting triple well.

Table 4-4 shows threshold voltage letter definitions.

Table 4-4 Threshold voltage letter definition

Letter	Description
H	HIGH threshold voltage
L	LOW threshold voltage
R	Regular threshold voltage
S	Super high threshold voltage
UL	Ultra low threshold voltage

4.6 Root name

For *Flops*, the root name has the following format:

[*logic*][*root*][*clock*][*async*][*scanout*][*output*][*ppa*]

Table 4-5 shows the possible values for these elements.

Table 4-5 Root name for flops

Element	Value	Description
logic	null	No logic integration
	An	n-input AND, can be used for synchronous reset
	AOmn	AOI style input, can be used for synchronous set and reset with set dominant
	On	n-input OR, can be used for asynchronous set
	OAmn	OAI style input, can be used for synchronous reset and set with reset dominant
	Mn	n-input encoded multiplexer
	E	multiplexer-hold flop enable
root	DFF	basic master slave flop
	DRFF	basic master slave flop with retention
	SDFF	multiplexer-d flop
	SDRFF	multiplexer-d flop with retention
clock	null	positive edge clock and base setup versus clock->q relationship
	N	negative edge clock and base setup versus clock->q relationship
async	null	no async inputs
	S	async set
	R	async reset
	RS	async reset and set with reset dominant
	SR	async set and reset with set dominant
	P	active HIGH
scanout	null	no dedicated SO pin
output	null	dual output flop
	Q	non-inverting output flop (q)
	QN	inverting output flop (qn)
ppa	null	base design point with regards to power, delay, and area
	L	base design point with regards to power and area.

For *Integrated Clock Gates*, the root name has the following format:

[*logic*][*testovrd*]ICG[*clock*][*ppa*]

Table 4-6 shows the possible values for these elements.

Table 4-6 Root name for integrated clock gates

Element	Value	Description
logic	null	no logic integration
testovrd	FR	free running version with no enable designed to match PRE and POST delay
	POST	test over-ride input is asynchronous
	PRE	test over-ride input is synchronous
clock	null	ICG produces an active HIGH output
ppa	null	base flop design point with respect to power, delay, and area
	L	base design point with regards to power and area.

For *Latches*, the root name has the following format similar to flops naming convention:

`[logic][root][clock][async][scanout][output][ppa]`

Table 4-7 shows the possible values for these elements.

Table 4-7 Root name for latches

Element	Value	Description
logic	null	no logic integration
LAT	LAT	basic transparent latch
clock	null	ICG produces an active HIGH output
	N	latch is transparent while clock is LOW
async	null	no async inputs
	S	async set
	R	async reset
	P	active HIGH
scanout	null	no dedicated SO pin
output	Q	non-inverting output flop (q)
	QN	inverting output flop (qn)
ppa	null	base design point with respect to power, delay, and area
	L	base design point with regard to power and area.

Appendix A
Revisions

This appendix describes the technical changes between released issues of this book.

Table A-1 Issue A

Change	Location	Affects
First release	-	-