Doc. No.: TD-LO13-DR-2001	Doc. Title: 0.11um/0.13um Logic & Mix-Signal 1.2/2.5/3.3v generic and 1.5/3.3v low leakage Design Rule	Doc.Rev: 21	Tech Dev. Rev: 1.25

Document Level: (For Engineering & Quality Document/工程暨品质文件专用)

☐ Level 1 - Manual ☑ Level 2 - Procedure/SPEC/Report ☐ Level 3 - Operation Instruction

Security Level: ☐Security A - Top Secret ☐ Security B - SMIC Confidential

☑ Security C - SMIC Restricted ☐ Security D - SMIC Internal

Document Change History

Doc. Rev.	Tech Dev. Rev.	Effective Date	Author	Change Description
18	1.23	2013-07-17	Pretty Chen	Old Tech Version: 1.23 1.7.1.7 Update “space” definition for MVN, MVP, NC, PC, SN, SP layers. Add “runlength” definition. 2.7.2.5~7.2.8: Add note for NC, PC MVN, MVP. 3.7.2.10: Add GT.13 recommended rule. 4.7.2.20/7.2.22 Add V1.11[R]/ Vn.10[R] recommended rule, delete note rule. 5.7.2.18 Update CT.5 and CT.5a rule description. 6.Add 1.5v device into DR. Update Title (1) / Purpose (2) / Technology Feature (7.1.1) description. Add 1.5V device into 7.2.3/7.2.4/7.2.9/7.2.10/7.2.18 (NW.4/NW.4a/PSUB.2a/DG.6/GT.1a). 7.7.2.19/7.2.21 Add [R] for M1.3a/ Mn.3a/M1.3b/ Mn.3b rule number. Optimize M1.3a/ Mn.3a rule description. 8.Add user guideline: 2/3/4/5/6/7 into 7 subject content. 9.7.1.2 /7.1.3:update all the tables’ format (SMIC drawing, mask layer mapping table, device truth table, CAD layer mapping table). Update 7.1.2.1 Note. Add note under each mask layer mapping table. 10.7.1.4: update metal option table format and add note2. 11.7.2.11/7.2.12/7.2.23/7.2.24 Update NLL/PLL/TV/TM title description. 12.7.2.2: add AA density rule: AA.11/AA.12. Modify AA note 1 description. Add AA note 2. 13.Update 7.2.30 ALRDL/ 7.2.31 PA section design rules/sketch map. 14.Delete original 7.2.26 PI/ 7.2.25 ALPad design rule due to don’t provide this process. 15.Delete 7.2.10 GT note 3 due to this note is not reasonable. 16.Update reference document and format for 5 Reference section. 17.7.2.9 Optimized DG.4 rule description. Add DG.4b to cover 0.11um design. Delete DG.7 and DG note. 18.7.2.3/7.2.24/7.2.32: Add NW.7[G] /TM.9[G] /MD design guideline. 19.7.2.16 Add [NC] for SP.13.

				20.7.2.2/7.2.4/7.2.10/7.2.18/7.2.19~7.2.23 Optimized AA.3/ PSUB.4/ PSUB.7/ GT.3/ GT.4/GT.5/GT.8/ CT.9/PSUB.3/GT. 11/CT.10/M1.3a and Mn.3a/Mn.8/ TM.8/Vn.11/V1.1/Vn.1/TV.1 rule description. 21.Original 7.2.27 change to 7.2.25: Optimize metal slot section design rule. 22.Add 7.2.27.2 non-salicide poly current density rule resistor and 7.2.40 dummy check rule. 23.Add 7.2.27.1 Current Density Rule (DC/AC) title. 24.7.2.39 update whole border layer design rule. 25.Add 7.2.33~7.2.38.Merge Mix-signal & RF sub-ECN design rule(TD1302050002) into this document and update below items: a. Update HRP.12/P2.5/P2.7/MTT.5/MTT.2b/MIM.1/MIM.5/SMIM.1 /SMIM.5/ BMIM.6 rule description. b. Add [NC] for HRP.10/MTT.10 rule number. c. Modify P2.7/ MIMDMY.2[G] rule value. d. Add Bottom plate and active MIM definition above each MIM design rule table. e. Update BMiM.1 rule description and rule value. 26.Update document title. 27.Update 7.1.2/7.1.3 all the tables' format. 28.7.2.27 Add [NC] for all current density rule number. 29.Add 7.3: 0.11um design guideline. 30.Add 7.2.40 DUP Pad guideline. 31.Add CT.11.
19	1.23	2014-10-31	Kelpy Pan	Old Tech Version: 1.23 1. Modify Tech Ver to 1.23 follow DR version naming rule. (when latest Tech. Dev. Rev ≥ 1, the new value should be aligned to "1.xx" [xx = (10 + N - 1)] in next version if the accumulative total count of existing Tech. Dev. Rev ≥ 1 is N)2. Update page 10 file title to "0.11um/0.13um Logic & Mix-Signal 1.2/2.5/3.3v generic and 0.13um 1.5/3.3v low leakage Design Rule"3. 7.2.19 Update M1.8 description to "Maximum line width allowed. Metal slot rule will apply for a metal with line width greater than this value. DRC skip to check (M1 interact with PA pattern)." follow special release notice.4. 7.2.21 Update Mn.8 description to "Maximum line width. Metal line greater than this width will comply metal slot design rule (DRC waive: Mn interact with PA pattern, (TM-1 AND DUPMK1) region for one top metal design, MIM bottom plate and MIM shield under MIM design)."follow TECN TD130900025. 7.2.30 Add "ALPA.10a (for 0.11um design)", "ALPA.10b (for 0.11um design)" for

				0.11um DRC, add Note5 “For 0.11um, Al bump Pad is defined as ALPA layer width larger than 35μm and interact with PA (PA width> 35um).” for 0.11um DRC follow TECN TD130900026. 7.2.34 add “0.13um” for each section title7. 7.2.35 Add “MTT.2b (for 0.11um design)” for 0.11um DRC, follow TECN TD130900028. 7.2.36 add “0.13um” for each section title9. 7.2.37 add “0.13um” for each section title10. 7.2.38 add “0.13um” for each section title11. 7.3.4 update flow chart shape follow template12. Add 7.3.8 section to define DRC check rules switch setting for 0.11um and 0.13um DRCAdd 7.3.9; 7.3.10; 7.3.11; 7.3.12 sections for 0.11um MIM DRC check
20	1.24	2015-12-22	Amy Wang	1) Update rule 1.Title/2.Purpose to remove “0.13um” in “0.13um 1.5/3.3v”. 2) Update 5.Reference table to remove ESD/Antenna (Merged into main rule) 3) Update 7.1.1 Technology feature, rearrange P15 User guideline to 7.1.2/7.1.4 4) Add 7.1.3 Non-DRC checking guideline 5) Update 7.1.5.1/2 layer mapping table, 7.1.5.3 table update MD layer and add note2. 6) Update 7.1.6.1/2/3/4 Device truth tables, optimize the notes above the table, update ESD1/SAB setting to “0/*” for MOS, SP form “0” to “*” for poly e-Fuse, DNW to “0” for NW/Psub diode, NW to “*’ for DNW/Psub diode. 7) Add 7.1.7 Device table for dummy insertion 8) Update 7.1.9 Design Rule Nome. and Abbr. 9) Add 7.1.10 DRC methodology of Connectivity definition 10) Update 7.1.11 Definition of terminology 11) Update 7.1.12 Design requirements 12) Add 7.2.1 DNW.6 (lesson learn driven), update DNW.3, delete Notes1/2 (covered in main rule). 13) Update 7.2.2 AA.4/9/10/11 rule description 14) Update 7.2.3 NW.6, delete Notes1/2/3 (NW resistor rule covered). 15) Update 7.2.4 PSUB.4 “≥” to “=”, add PSUB.9[R]/ PSUB.10[NC], delete Notes1/2 (covered in main rule). 16) Update 7.2.5/6 NC.4/5/6/7/PC.4/5/6/7 rule description 17) Update 7.2.7/8 MVN.4/5/6/7/MVP.4/5/6/7 rule description 18) Update 7.2.9 DG.4/.4b rule to add 0.11/0.13 DRC switch 19) Add 7.2.10 GT.14[R]/GT.15[R] (rule completeness), delete notes2 to add as GT.16[R].

				20) Add 7.2.11-14 NLL.4b/PLL/4b/NLH.4b/PLH.4b, update NLL.6/PLL.6/NLH.6 /PLH.6 (Rule optimize for DR/DRC match) 21) Update 7.2.15 SN.7/8/9 to exclude NW resistor region. 22) Add 7.2.17 SAB.2a/10a[R], tighten SAB.10 rule value from 0.5 to 1.0um2 (Lesson learnt driven) 23) Update 7.2.18 CT.4a to add "1.5V", add CT.4c rule. 24) Delete 7.2.19/21 note1 to add as M1/Mn.19[NC] rules. 25) Add CT.15/V1.12/Vn.12/TV.11(Lesson learn driven) 26) Update 7.2.23 TV.10, 7.2.24 TM.8/TM.9[G] rules 27) Delete "Metal dummy design minima" section, add to MnDUMCK.7[NC]/TMDUMCK.5[NC]/MTTDUMCK.5[NC] 28) Delete "(for 0.11um design)" in 7.2.25 MTT.2b rule-No, modify MTT.1/6a, add MTT.11[G] to cover MTT process 29) Delete "(for 0.11um design)" in 7.2.26 ALPA.10a/10b, update >35um to >32um in ALPA.10a/notes3; add ALPA.15[NC], delete note4. 30) Update 7.2.27 PA.3/PA.5, update PA.1 to PA.1a/1b[G], add PA.6 (Lesson learnt driven). 31) Update 7.2.28 MD design guideline, add DRC rule. 32) Add 7.2.29 NW/AA/Poly resistor rules (rule completeness). 33) Update 7.2.29.4 HRP.3/4/8/10 rules, update wording above the rule table and update HRP sketch map. 34) Delete original 7.3.8-12, update to 7.2.30-7.2.32 section, update Dummy MIM/bottom plate definition. 35) Update 7.2.30.2 MIM.11/13/18/MiM.14[G]/17[G], delete MiM.15[G] (MIM strategy optimized) 36) Update 7.2.31.1 BMiM.6[G]/8/13[G], delete BMiM.12[G] (MIM strategy optimized) 37) Update 7.2.32 SMiM.11/14[G]/18[G] rules, delete SMiM.16[G] (MIM strategy optimized) 38) Update 7.2.30.3 Metal shield guidelines. 39) Add 7.2.35 CDR.8a[NC]/ 8b[NC]/45[NC] /46[NC]. 40) Add 7.2.36 Antenna rule (Merged the branch rule) 41) Add 7.2.37 Conventional rule (Lesson learn driven) 42) Update 7.2.38 MTTDUMCK.1/2 to delete MTT.3b 43) Add 7.2.39 Seal Ring check rule 44) Update 7.3.1 Metal Slot Guideline rules add [G]. 45) Update 7.3.2 Metal fuse guideline 45) Update 7.3.3 Guideline for metal fuse repairing alignment mark 46) Add 7.3.5 Poly E-Fuse guideline (E-fuse committee conclusion)

				47) Add 7.3.6 Logo guideline (Lesson learnt driven) 48) Add 7.3.7 ESD guideline (Merged the branch rule) 49) Add 7.3.8 Latch up guideline (Merged the branch rule) 50) Add 7.3.9 MOM device layout guideline (Lesson learn driven) 51) Update 7.4.6 Non-shrinkage design guideline, and move into 7.4.3.2. 52) Optimize all rule table to follow template format.
21	1.25	2018-02-08	Minna Xu	1. 7.1.4.8 add seal ring and HRP switch, DG.8[R]. Update 7.1.4.4/7 2. 7.1.5.1 Correct 39/40 design rule name 3. 7.1.5.2 CAD table add EXCLU, LUWMK1, VDDMK1, VSSMK1,MARKS, ESDIO2. 4. 7.1.6.1/3 mask truth table update MOS Varactor NLL/NLH 0 -> 1. 5. 7.1.11.1/3 update picture. 6. Update AA.1, AA.2, AA.3, AA.4, AA.5, AA.6, AA.7, NC.5, GT.2, GT.3, GT.4, GT.5, GT.6, GT.13[R], CT.1, CT.3, CT.4a, CT.5, CT.6, CT.7, CT.8, CT.9, CT.10, SN.1, SN.3, SN.5, SN.6, SN.7, SN.8, SN.9, SN.10, SP.1, SP.3, SP.4, SP.5, SP.6, SP.7, SP.8, SP.10, M1,1, M1.2, Mn.2, V1,4, V1.5, V1.6, V1.7, V1.8, V1.9, Vn.1, Vn.3, Vn.4, Vn.7, MTT.1, MTT.2a, MTT.3, MTT.4, Convention.2 to exclude SRAM region in 7.2. 7. 7.2.2 update AA.9 8. 7.2.4 update PSUB.9[R] to PSUB.9.Update PSUB.4/8 description. 9. Update 7.2.5 NC.3, 7.2.6 PC.3, 7.2.7 MVN.3, 7.2.8 MVP.3 description. 10. 7.2.9 add DG.8 for lesson learnt driven. 11. Update 7.2.9 DG.5 7.2.18 CT.5 description to add device AA definition. 12. 7.2.10 Modify GT.14[R] operation from < change to ⩽. 13. Update 7.2.12 PLL.11[R] operation from > change to ⩾. 14. 7.2.15 add SN.4b for lesson learn extension. 15. 7.2.22 update Vn.11. 16. 7.2.24 update TM.8 description. 17. 7.2.25 update MTT.1a, MTT.5. 18. 7.2.26 update ALPA.10a/10b. 19. 7.2.27 add PA note for customer request. 20. 7.2.28 update MD.6. 21. 7.2.29.1 RESNW update definition, RESNW.7. Add RESNW.10/11 for customer driven. 22. 7.2.29.2 RESAA update definition.

				23. 7.2.29.3 RESP1 update definition. 24. 7.2.37 update Conventional.3. 25. 7.2.39 add SRAM design rule. 26. 7.3.2 update FUSE.5[G], FUSE.6[G] to"=". 27. 7.3.7.1 update description. 28. 7.3.7.2 add ESD.22[G], ESD.22a[G], ESD.22b[G] and note for lesson learnt extension. 29. 7.3.7.3 ESD1 Update rule for lesson learnt extension. 30. Change ESDHV to ESD5V 31. 7.3.8 update LU.4[G] description. 32. 7.3.9 update MOM.4[G][NC] to MOM.4[G], update description. Add table 1. 33. 7.3.10 Add seal ring guideline for DR integrality. 34. Move 7.2.39 0.13SR check rule into 7.3.10.3. Update 0.13um SRCK.16/17/18, note. Add SRCK.31/32 for lesson learnt driven. Add SRCK.33/34 for customer request. Delete "square" in SRCK.4/5/6/19/20/21. 35. 7.3.10.4 add 0.11um SRCK. 36. Add 8 attachment of L013SEAL_RING20180122.gds and L011SEAL_RING20180122.gds. 37. Update reference document title and delete no need reference document TD-LO13-DR-2001.

SEMICONDUCTOR MANUFACTURING INTERNATIONAL CORPORATION

0.11um/0.13um Logic & Mix-Signal 1.2/2.5/3.3v generic and 1.5/3.3v low leakage Design Rule

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CONTENTS

1. Title:

0.11um/0.13um Logic & Mix-Signal 1.2/2.5/3.3v generic and 1.5/3.3v low leakage design rule

2. Purpose:

Layout rules to generate masks for 0.11um/0.13um Logic& Mixed Signal 1.2V/2.5V/3.3V generic and 1.5V/3.3V Low leakage technology.

3. Scope:

All SMIC Fabs

4. Nomenclature:

NA

5. Reference:

Item	Reference documents No	Reference documents title	Reference documents version	Reference part
Seal Ring Rules	TD-LO13-DR-2002	0.11um/0.13um Logic & Mix-Signal 1.2/2.5/3.3V Generic and 1.5/3.3V Low Leakage Seal-ring Design Guideline	5	All
Dummy Insertion Rules	TD-GENL-01-2004	SMIC Generic Logic and Mix-signal Dummy Pattern Insertion Rule (no 40K above UTM) for 0.11um or above technology nodes	9	All

6. Responsibility:

Technology Development Center is responsible before technology transfer and FAB PIE is responsible after technology transfer.

7. Subject Content:

7.1 User guide

7.1.1 Technology feature

- P substrate 8.5-10.5ohm-cm
- Device options for generic, low leakage and SC with high speed performance
- Core 1.2V/1.5V device
- Support 2.5V or 3.3V I/O devices

- Shallow trench isolation with 0.36um pitch
- 1.5~2.0nm furnace gate dielectric
- 0.07~0.10um poly gate CD using hard mask trimming
- 8 Cu layers with dual damascene technology.
- Al pad for bonding
- FSG with k=3.6 as dielectric without trench etch stop layer

7.1.2 Grid size

Minimum Layout grid size is 0.001um.

7.1.3 Non-DRC checking guideline

No DRC for the design rules with the superscript of [NC].
No DRC for Notes which are below design rules tables.

7.1.4 DRC checking guideline

1. The rules with the superscript of [R] are recommended rules which require performing a DRC runset, but DRC gating is not needed for them. It's strongly recommended customers to follow recommended rules which are to ensure better performance for process and device. Customers can consult with SMIC integration engineers if necessary.
2. The rules with the superscript of [G] are layout guidelines which require performing a DRC runset, but DRC gating is not needed for them. It's strongly recommended customers to follow layout guidelines which are to ensure better performance for process and device. SMIC spice model and PDK must strictly follow SMIC design rule guidelines. And SMIC don't provide spice model and PDK if customers don't follow the SMIC layout guidelines. Customers can consult with SMIC integration engineers if necessary.

3. The design rules in this document are not applicable for seal ring area (marked with MARKS layer). For seal ring constrains and dimension, please refer Seal Ring design guideline section.

4. No SRAM DRC checking for the design rules of AA.1, AA.2, AA.3, AA.4, AA.5, AA.6, AA.7, NC.5, GT.2, GT.3, GT.4, GT.5, GT.6, GT.13[R], CT.1, CT.3, CT.4a, CT.5, CT.6, CT.7, CT.8, CT.9, CT.10, SN.1, SN.3, SN.5, SN.6, SN.7, SN.8, SN.9, SN.10, SP.1, SP.3, SP.4, SP.5, SP.6, SP.7, SP.8, SP.10, M1,1, M1.2, Mn.2, V1,4, V1.5, V1.6, V1.7, V1.8, V1.9, Vn.1, Vn.3, Vn.4, Vn.7, MTT.1, MTT.2a, MTT.3, MTT.4, Convention.2. SRAM design rule please check 7.2.41.SRAM design rule. SRAM region covered by the marker layers of OPCBA or OPCBP or OPCBM.

5. For metal layers, DRC code checking should follow (Metal NOT Metal slot). For those rules which need check both MnDUM and MnSLOT, DRC checking should follow ((Mn-MnSLOT)+MnDUM).

6. For the density rules, DRC code checking should include dummy pattern.

7. For IO voltage switch setting, DRC default turn-on setting is IO 1533. When set #DEFINE IO 1533, check GT.1c and CT.4b rule; When set #DEFINE IO 1225, check GT.1b and CT.4c rule.

8. DRC switch setting for Design rule guideline and Recommended rules.

Category	**Rules**	**DRC switch setting by default**
Recommended Rule	V1.11[R],Vn.10[R], MIM.17[R], BMIM.13[R], SMIM.18[R], M1.3a[R], M1.3b[R], Mn.3a[R], Mn.3b[R], RESNW.3[R], RESNW.9[R], DG.8[R]	Turn-on
	Other recommended rules	Turn-off
Guideline (Rule number with [G])	ESD	Turn-off
	Latch Up	Turn-on
	DUP	Turn-on
	Logo	Turn-on
	Metal Slot	Turn-on
	MOM	Turn-on
	Metal Fuse	Turn-off
	Poly E-Fuse	Turn-off
	Align mark for metal fuse	Non-DRC check
	MIMDMY guideline	Turn-off
	Metal shield guideline	Turn-off
	Current density guideline	Non-DRC check
Seal Ring	0.11um	Turn-on
	0.13um	Turn-off
HRP / MIM	Mix-Signal	Turn-on
	Logic	Turn-off
ESD1	ESD1_Approach_A	Turn-on
	ESD1_Approach_B	Turn-off

7.1.5 SMIC layer mapping table

7.1.5.1 SMIC 0.13um drawn layer mapping table

Sequence number	Design layer name	GDS layer No.	GDS data type	Layer Description
1	DNW	19	0	Deep N Well
2	AA	10	0	Active area
3	NW	14	0	N-Well
4	NC	21	0	High Vt NMOS device and N-cell implant
5	PC	16	0	High Vt PMOS device
6	MVN	45	0	Core 1.2V low Vt NMOS device
7	MVP	44	0	Core 1.2V low Vt PMOS device
8	DG	29	0	2.5V or 3.3V IO device
9	GT	30	0	Poly gate
10	HRP	39	0	High Resistance Poly
11	ESD1	41	0	ESD1 implantation
12	SN	40	0	N+ S/D implantation
13	SP	43	0	P+ S/D implantation
14	SAB	48	0	Salicide Block
15	CT	50	0	Contact
16	M1	61	0	Metal-1
17	V1	70	0	VIA-1
18	M2	62	0	Metal-2
19	V2	71	0	VIA-2
20	M3	63	0	Metal-3
21	V3	72	0	VIA-3
22	M4	64	0	Metal-4
23	V4	73	0	VIA-4
24	M5	65	0	Metal-5
25	MIM	58	0	Capacitor Top Metal
26	V5	74	0	VIA-5
27	M6	66	0	Metal-6
28	P2	31	0	Capacitor bottom plate
29	V6	75	0	VIA-6
30	M7	67	0	Metal-7
31	V7	76	0	VIA-7
32	M8	68	0	Metal-8
33	TV1	121	0	1st top Via (Only used in 2 TM layers process)
34	TM1	120	0	1st top Metal (Only used in 2 TM layers process)
35	TV2	123	0	Top Via

Sequence number	Design layer name	GDS layer No.	GDS data type	Layer Description
36	TM2	122	0	Top Metal (Including normal thickness top metal and thick top metal)
37	PA	80	0	Passivation
38	MD	130	0	Metal about top metal for redistribution, Passivation 2
39	BORDER	127	0	Top Structure's Border
40	FUSE	81	0	Metal fuse
41	RESNW	95	0	Blocking layer for NW resistor
42	PSUB	85	0	Blocking layer for native device
43	RESP1	96	0	Dummy block layer for non-salicide Poly resistor
44	RESAA	97	0	Dummy block layer for non-salicide AA resistor
45	AADUM	10	1	AA Dummy Layer (For dummy AA insertion)
46	GTDUM	30	1	GT Dummy Layer (For dummy GT insertion)
47	M1DUM	61	1	Metal-1 Dummy Layer (For dummy metal insertion)
48	M2DUM	62	1	Metal-2 Dummy Layer (For dummy metal insertion)
49	M3DUM	63	1	Metal-3 Dummy Layer (For dummy metal insertion)
50	M4DUM	64	1	Metal-4 Dummy Layer (For density check)
51	M5DUM	65	1	Metal-5 Dummy Layer (For dummy metal insertion)
52	M6DUM	66	1	Metal-6 Dummy Layer (For dummy metal insertion)
53	M7DUM	67	1	Metal-7 Dummy Layer (For dummy metal insertion)
54	M8DUM	68	1	Metal-8 Dummy Layer (For dummy metal insertion)
55	TM1DUM	120	1	TM-1 Dummy Layer (For dummy metal insertion)
56	TM2DUM	122	1	TM2 Dummy Layer (For dummy metal insertion)
57	ALPA	83	0	AL Bonding Pad and AL RDL routing
58	M1SLOT	61	2	Metal-1 Slot
59	M2SLOT	62	2	Metal-2 Slot
60	M3SLOT	63	2	Metal-3 Slot
61	M4SLOT	64	2	Metal-4 Slot

Sequence number	Design layer name	GDS layer No.	GDS data type	Layer Description
62	M5SLOT	65	2	Metal-5 Slot
63	M6SLOT	66	2	Metal-6 Slot
64	M7SLOT	67	2	Metal-7 Slot
65	M8SLOT	68	2	Metal-8 Slot
66	TM1SLOT	120	2	Top Metal-1 Slot
67	TM2SLOT	122	2	Top Metal-2 Slot
68	VARMOS	93	0	Dummy block layer for MOS type varactor
69	VARJUN	94	0	Dummy block layer for Junction type varactor.

Remark: For metal and via layer option, please refer "Metal Options table".

Note:

1. Mask NWH, PWH and PW are generated from NW, DG, AA and (or) PSUB patterns by logic operation. Customers can't draw these layers.
2. NLL, PLL, NLH, PLH LDD layers are generated by logic operation. Designers can't draw these layers.
3. AlCu bond pad and passivation layers are generated from PA layer with bias. If using ALPA to redistributed Al bump pad and MD layers need to be drawn.
4. HRP, MiM layers are optional for Mixed Signal & RF process. There are three MiM options (one mask MiM, two masks MiM and stacked MiM), you can only select one to meet your requirement and inform SMIC which MiM option is chosen.
5. Once Thick Top Metal process is used with customer request for RF application, whole chip top metal layout must follow MS&RF MTT design rule instead of 0.13um Logic TM rule. SMIC also can provide two top metal layers' process.

7.1.5.2 SMIC 0.13um CAD layer mapping table

Designer must draw these mark layers when the relevant devices are used in their chip design.

Sequence number	Layer name	GDS No.	Data type	Description
1	HRPDMY	210	0	DRC/LVS Dummy layer for precious high P-Poly resistor
2	INDMY	212	0	DRC/LVS Dummy layer for MTT in Inductor application
3	RESP3T	96	1	LVS Dummy layer for Poly-1 Resistor with 3 terminal
4	RESCKT	131	3	LVS Dummy layer for subckt resistor
5	DSTR	138	0	DRC/LVS Dummy layer to distinguish a diode
6	DMPNP	134	0	DRC/LVS Dummy layer to define BJT
7	MIMDMY	211	0	DRC MIM Dummy Layer
8	DNWTR	19	2	LVS six terminal DNW MOS
9	SUBD	131	1	LVS substrate separation layer
10	DCTY	139	0	LVS marker layer for Area with no Extraction for LVS
11	RFDEV	181	0	LVS mark layer for RF device
12	RFMOSD	182	0	LVS mark layer for RF mos drain terminal
13	RF3T	183	2	LVS mark layer for RF 3 terminal devices and3 terminal MOM
14	MOMDMY	211	1	DRC/LVS mark layer for MOM
15	MOSCKT	131	2	LVS dummy layer to distinguish bsim mos and subckt mos
16	CLPDMY	87	2	DRC/LVS Dummy layer to define Clamp Diode/Shottky
17	DMRES	137	2	DRC/LVS Dummy layer to recognize resistors other than covered by Res_NW, Res_AA, Res_P1 CAD layers.
18	SURNW	209	0	DRC/LVS Dummy layer on surrounding NW for DRC check
19	MIMCKT	131	6	LVS marker layer for subckt MIM
20	MIMSHD	89	155	DRC/LVS marker layer for metal shield design under active MIM
21	LOGO	26	0	DRC/LVS marker layer for LOGO;L mark area
22	DUMBA	91	0	DRC/LVS marker layer to block dummy AA pattern fill
23	DUMBP	92	0	DRC/LVS marker layer to block dummy Poly pattern fill
24	DUMBM	90	0	DRC/LVS marker layer to block dummy metal patterns fill
25	GTFUSE	81	1	E-fuse function area marker layer
26	EFUSE	81	2	E-fuse element marker layer
27	NODMF	180	0	DRC/LVS marker layer for Non-shrink block layer for 0.11um and above mature technology node.
28	OPCBA	100	0	DRC/LVS marker layer for Blocking Layer for OPC operation on AA and SRAM marking layer.
29	OPCBP	101	0	DRC/LVS marker layer for Blocking Layer for OPC operation on GT and SRAM marking layer.

Sequence number	Layer name	GDS No.	Data type	Description
30	OPCBM	102	0	DRC/LVS marker layer for Blocking Layer for OPC operation on M1 and SRAM marking layer.
31	INST	60	0	DRC/LVS marker layer for SRAM blocking layer
32	CAPBP	137	0	DRC/LVS marker layer for Capacitor Bottom Plate
33	ALPAR	83	1	DRC/LVS marker layer for ALPA Resistor layer
34	M1R	171	0	LVS marker layer for M1 resistor layer
35	M2R	172	0	LVS marker layer for M2 resistor layer
36	M3R	173	0	LVS marker layer for M3 resistor layer
37	M4R	174	0	LVS marker layer for M4 resistor layer
38	M5R	175	0	LVS marker layer for M5 resistor layer
39	M6R	176	0	LVS marker layer for M6 resistor layer
40	M7R	177	0	LVS marker layer for M7 resistor layer
41	M8R	178	0	LVS marker layer for M8 resistor layer
42	TM1R	201	0	LVS marker layer for TM1 resistor layer
43	TM2R	202	0	LVS marker layer for TM2 resistor layer
44	M1TXT	141	0	LVS marker layer for metal 1 text layer
45	M2TXT	142	0	LVS marker layer for metal 2 text layer
46	M3TXT	143	0	LVS marker layer for metal 3 text layer
47	M4TXT	144	0	LVS marker layer for metal 4 text layer
48	M5TXT	145	0	LVS marker layer for metal 5 text layer
49	M6TXT	146	0	LVS marker layer for metal 6 text layer
50	M7TXT	147	0	LVS marker layer for metal 7 text layer
51	M8TXT	148	0	LVS marker layer for metal 8 text layer
52	TM1TXT	120	3	LVS marker layer for top metal 1 text layer
53	TM2TXT	122	3	LVS marker layer for top metal 2 text layer
54	ALPATXT	83	2	LVS marker layer for ALPA text layer
55	MARKS	189	151	Seal ring (chip level) marking layer for DRC and dummy auto-filling blockage for dummy fill utility
56	NFDMK	131	5	LVS marking layer for MOS multiple fingers LVS marking layer for inductor turns calculation in 013LLRF
57	INDR	212	1	LVS marker layer to calculate inductor radius
58	VSIA	63	63	VSIA tagging layer(Text Only)
59	MIMSTK	131	8	LVS mark layer for stack MIM
60	DUPMK1	89	156	DRC/LVS marker layer for pad with device underneath
61	FUSEMK1	81	152	All fuse elements marker layer
62	RFSD	181	3	RF MOS of even finger with S/D permute for LVS
63	ALMK1	83	151	DRC marking layer for dummy purpose ALPA

Sequence number	Layer name	GDS No.	Data type	Description
64	MOMMK1	211	11	DRC marking layer to identify M1 MOM region
65	MOMMK2	211	12	DRC marking layer to identify M2 MOM region
66	MOMMK3	211	13	DRC marking layer to identify M3 MOM region
67	MOMMK4	211	14	DRC marking layer to identify M4 MOM region
68	MOMMK5	211	15	DRC marking layer to identify M5 MOM region
69	MOMMK6	211	16	DRC marking layer to identify M6 MOM region
70	MOMMK7	211	17	DRC marking layer to identify M7 MOM region
71	EXCLU	132	0	DRC block layer only for SMIC internal usage
72	LUWMK1	131	177	Marking layer to waive latch up rules
73	VDDMK1	131	175	Marking layer for Power(Vdd) PAD for DRC use
74	VSSMK1	131	176	Marking layer for Power(Vss) PAD for DRC use
75	MARKS	189	151	Seal ring (chip level) marking layer for DRC and dummy auto-filling blockage
76	ESDIO2	133	3	Dummy layer for ESD devices and protection circuits.
77	ESD5V	133	1	Dummy layer for 5V tolerant I/O ESD device identification

7.1.5.3 SMIC 0.13um mask layer mapping table

a) SMIC mask layer mapping table (IO Voltage: 2.5V) for SMIC 1.2V/2.5V generic tape out usage. (Top tier table ID: LCMO13-V02)

Mask ID	Process Name	Dig. Area Tone	Mask Generation	Description
292	DNW	C	Drawn	Deep N well imp for substrate noise suppression
901	KV	C	Drawn	Alignment mark clearing
120	AA	D	Generated	Active Area/SDG
191	PW	C	Generated	P-Well / P-Tub
491	PWH	C	Generated	P well I/O
192	NW	C	Generated	N-Well / N-Tub
492	NWH	C	Generated	N well I/O
193	NC	C	Generated	N-Cell Implant
194	PC	C	Generated	P-Cell Implant/NFILED
296	MVN	C	Generated	Medium Vtn adjust
295	MVP	C	Generated	Medium Vtp adjust
131	DG	D	Generated	Dual Gate
130	GT	D	Generated	Poly Gate / Poly-1 / ONO Gate
116	NLL	C	Generated	NMOS LDD Implant for Low VDD
113	PLL	C	Generated	PMOS LDD Implant for Low VDD
115	PLH	C	Generated	PMOS LDD Implant for High VDD
114	NLH	C	Generated	NMOS LDD Implant for High VDD
110	ESD1	C	Drawn	ESD Implant for 1
198	SN	C	Drawn	N+ S/D Implant
197	SP	C	Drawn	P+ S/D Implant
155	SAB	D	Drawn	Resist Protect Oxide / Salicide Block
156	CT	C	Drawn	Contact Hole (Metal to Si/Poly)
160	M1	C	Generated	Metal-1
178	V1	C	Drawn	Via-1 Hole
180	M2	C	Generated	Metal-2
179	V2	C	Drawn	Via-2 Hole
181	M3	C	Generated	Metal-3
177	V3	C	Drawn	Via-3 Hole
182	M4	C	Generated	Metal-4
176	V4	C	Drawn	Via-4 Hole
183	M5	C	Generated	Metal-5
175	V5	C	Drawn	Via-5 Hole
184	M6	C	Generated	Metal-6
174	V6	C	Drawn	Via-6 Hole
185	M7	C	Generated	Metal-7
144	TV2	C	Drawn	Second Top Via
143	TM2	C	Generated	Second Top Metal
107	PA	C	Drawn	Passivation / Pad

Mask ID	Process Name	Dig. Area Tone	Mask Generation	Description
108	ALPA	D	Generated	AL Bonding Pad
163	MD	C	Drawn/Generated (Refer to Note2)	Metal about top metal for redistribution, Passivation 2.
106	FUSE	C	Drawn	Fuse Window

Note:

1. **Please refer DCC document PM-DATA-02-2001 layer mapping table 1 for the pure generated layer GDS No. /data type which is only for Tech. file development usage. Designers do not need to draw the layers.**
2. **For MD design rule, please refer to section of 7.2.28.**

b) SMIC mask layer mapping table (IO Voltage: 3.3V) for 1.2V/3.3V generic tape out usage.
(Top tier table ID: LCMO13-V03)

Mask ID	Process Name	Dig. Area Tone	Mask Generation	Description
292	DNW	C	Drawn	Deep N well imp for substrate noise suppression
901	KV	C	Drawn	Alignment mark clearing
120	AA	D	Generated	Active Area/SDG
191	PW	C	Generated	P-Well / P-Tub
491	PWH	C	Generated	P well I/O
192	NW	C	Generated	N-Well / N-Tub
492	NWH	C	Generated	N well I/O
193	NC	C	Generated	N-Cell Implant
194	PC	C	Generated	P-Cell Implant/NFILED
296	MVN	C	Generated	Medium Vtn adjust
295	MVP	C	Generated	Medium Vtp adjust
131	DG	D	Generated	Dual Gate
130	GT	D	Drawn	Poly Gate / Poly-1 / ONO Gate
116	NLL	C	Generated	NMOS LDD Implant for Low VDD
113	PLL	C	Generated	PMOS LDD Implant for Low VDD
115	PLH	C	Generated	PMOS LDD Implant for High VDD
114	NLH	C	Generated	NMOS LDD Implant for High VDD
110	ESD1	C	Drawn	ESD Implant for 1
198	SN	C	Drawn	N+ S/D Implant
197	SP	C	Drawn	P+ S/D Implant
155	SAB	D	Drawn	Resist Protect Oxide / Salicide Block
156	CT	C	Drawn	Contact Hole (Metal to Si/Poly)
160	M1	C	Generated	Metal-1
178	V1	C	Drawn	Via-1 Hole
180	M2	C	Generated	Metal-2
179	V2	C	Drawn	Via-2 Hole
181	M3	C	Generated	Metal-3
177	V3	C	Drawn	Via-3 Hole
182	M4	C	Generated	Metal-4
176	V4	C	Drawn	Via-4 Hole
183	M5	C	Generated	Metal-5
175	V5	C	Drawn	Via-5 Hole

Mask ID	Process Name	Dig. Area Tone	Mask Generation	Description
184	M6	C	Generated	Metal-6
174	V6	C	Drawn	Via-6 Hole
185	M7	C	Generated	Metal-7
144	TV2	C	Drawn	Second Top Via
143	TM2	C	Generated	Second Top Metal
107	PA	C	Drawn	Passivation / Pad
108	ALPA	D	Generated	AL Bonding Pad
163	MD	C	Drawn/Generated (Refer to Note2)	Metal about top metal for redistribution, Passivation 2
106	FUSE	C	Drawn	Fuse Window

Note:

1. **Please refer DCC document PM-DATA-02-2001 layer mapping table 1 for the pure generated layer GDS No. /data type which is only for Tech. file development usage. Designers do not need to draw the layers.**
2. **For MD design guideline, please refer to section of 7.2.28.**

c) SMIC mask layer mapping table (IO Voltage: 3.3V) for 1.5V/3.3V low leakage SMIC tape out usage. (Top tier table ID: LCMO13-V04)

Mask ID	Process Name	Dig. Area Tone	Mask Generation	Description	Optional
292	DNW	C	Drawn	Deep N well imp for substrate noise suppression	Optional
120	AA	D	Generated	Active Area/SDG	Must
901	KV	C	Drawn	Alignment mark clearing	Optional
191	PW	C	Generated	P-Well / P-Tub	Must
491	PWH	C	Generated	P well I/O	Must
192	NW	C	Generated	N-Well / N-Tub	Must
492	NWH	C	Generated	N well I/O	Must
193	NC	C	Generated	N-Cell Implant	Optional
131	DG	D	Generated	Dual Gate	Must
130	GT	D	Drawn	Poly Gate / Poly-1 / ONO Gate	Must
116	NLL	C	Generated	NMOS LDD Implant for Low VDD	Must
113	PLL	C	Generated	PMOS LDD Implant for Low VDD	Must
115	PLH	C	Generated	PMOS LDD Implant for High VDD	Must
114	NLH	C	Generated	NMOS LDD Implant for High VDD	Must
110	ESD1	C	Drawn	ESD Implant for 1	Optional
198	SN	C	Drawn	N+ S/D Implant	Must
197	SP	C	Drawn	P+ S/D Implant	Must
155	SAB	D	Drawn	Resist Protect Oxide / Salicide Block	Must
156	CT	C	Drawn	Contact Hole (Metal to Si/Poly)	Must
160	M1	C	Generated	Metal-1	Must
178	V1	C	Drawn	Via-1 Hole	Must
180	M2	C	Generated	Metal-2	Must
179	V2	C	Drawn	Via-2 Hole	Must
181	M3	C	Generated	Metal-3	Must
177	V3	C	Drawn	Via-3 Hole	Must
182	M4	C	Generated	Metal-4	Must
176	V4	C	Drawn	Via-4 Hole	Must
183	M5	C	Generated	Metal-5	Must
175	V5	C	Drawn	Via-5 Hole	Must
184	M6	C	Generated	Metal-6	Must

Mask ID	Process Name	Dig. Area Tone	Mask Generation	Description	Optional
174	V6	C	Drawn	Via-6 Hole	Must
185	M7	C	Generated	Metal-7	Must
144	TV2	C	Drawn	Second Top Via	Must
143	TM2	C	Generated	Second Top Metal	Must
107	PA	C	Drawn	Passivation / Pad	Must
108	ALPA	D	Generated	AL Bonding Pad	Must
163	MD	C	Drawn	Metal about top metal for redistribution, Passivation 2	Optional
106	FUSE	C	Drawn	Fuse Window	Optional

Note: Please refer DCC document PM-DATA-02-2001 layer mapping table 1 for the pure generated layer GDS No. /data type which is only for Tech. file development usage. Designers do not need to draw the layers.

d) SMIC mask layer name mapping table (IO Voltage: 2.5V) for 1.2V/2.5V mix-signal product SMIC tape out usage.(Top tier table ID: MSGL13-V02)

Mask ID	Mask Name	Dig. Area Tone	Mask Generation	Mask Purpose	Optional
292	DNW	C	Drawn	Deep N well imp for substrate noise suppression	Optional
120	AA	D	Generated	Active Area/SDG	Must
901	KV	C	Drawn	Alignment mark clearing	Optional
192	NW	C	Generated	N-Well / N-Tub	Must
191	PW	C	Generated	P-Well / P-Tub	Must
492	NWH	C	Generated	N well I/O	Must
491	PWH	C	Generated	P well I/O	Must
193	NC	C	Generated	N-Cell Implant and High	Optional
194	PC	C	Generated	P-Cell Implant/NFILED	Optional
296	MVN	C	Generated	Medium Vtn adjust	Optional
295	MVP	C	Generated	Medium Vtp adjust	Optional
131	DG	D	Generated	Dual Gate	Must
130	GT	D	Generated	Poly Gate / Poly-1 / ONO Gate	Must
116	NLL	C	Generated	NMOS LDD Implant for Low VDD	Must
113	PLL	C	Generated	PMOS LDD Implant for Low VDD	Must
115	PLH	C	Generated	PMOS LDD Implant for High VDD	Must
114	NLH	C	Generated	NMOS LDD Implant for High VDD	Must
110	ESD1	C	Drawn	ESD Implant for 1	Optional
198	SN	C	Drawn	N+ S/D Implant	Must
197	SP	C	Drawn	P+ S/D Implant	Must
413	HRP	C	Drawn	High Resistant Poly Imp	Optional
155	SAB	D	Drawn	Resist Protect Oxide / Salicide Block	Must
156	CT	C	Drawn	Contact Hole (Metal to Si/Poly)	Must

Mask ID	Mask Name	Dig. Area Tone	Mask Generation	Mask Purpose	Optional
160	M1	C	Generated	Metal-1	Must
178	V1	C	Drawn	Via-1 Hole	Must
180	M2	C	Generated	Metal-2	Must
179	V2	C	Drawn	Via-2 Hole	Must
181	M3	C	Generated	Metal-3	Must
177	V3	C	Drawn	Via-3 Hole	Must
182	M4	C	Generated	Metal-4	Must
176	V4	C	Drawn	Via-4 Hole	Must
183	M5	C	Generated	Metal-5	Must
175	V5	C	Drawn	Via-5 Hole	Must
184	M6	C	Generated	Metal-6	Must
174	V6	C	Drawn	Via-6 Hole	Must
185	M7	C	Generated	Metal-7	Must
162	MIM	D	Drawn	Top Plate of MIM Capacitor	Optional
132	P2	D	Drawn	Poly-2 or MIM plate 2	Optional
144	TV2	C	Drawn	Second Top Via	Must
143	TM2	C	Generated	Second Top Metal	Must
142	TV1	C	Drawn	First Top Via	Optional
141	TM1	C	Generated	First Top Metal	Optional
107	PA	C	Drawn	Passivation / Pad	Must
108	ALPA	D	Generated	AL Bonding Pad	Must
163	MD	C	Drawn	Metal about top metal for redistribution, Passivation 2	Optional
106	FUSE	C	Drawn	Fuse Window	Optional

Note: Please refer DCC document PM-DATA-02-2001 layer mapping table 1 for the pure generated layer GDS No. /data type which is only for Tech. file development usage. Designers do not need to draw the layers.

e) SMIC mask layer name mapping table (IO Voltage: 3.3V) for 1.2V/ 3.3V mix-signal product SMIC tape out usage. (Top tier table ID: MSGL13-V01)

Mask ID	Mask Name	Dig. Area Tone	Mask Generation	Mask Purpose	Optional
292	DNW	C	Drawn	Deep N well imp for substrate noise suppression	Optional
120	AA	D	Generated	Active Area/SDG	Must
901	KV	C	Drawn	Alignment mark clearing	Optional
192	NW	C	Generated	N-Well / N-Tub	Must
191	PW	C	Generated	P-Well / P-Tub	Must
492	NWH	C	Generated	N well I/O	Must
491	PWH	C	Generated	P well I/O	Must
193	NC	C	Generated	N-Cell Implant	Optional
194	PC	C	Generated	P-Cell Implant/NFILED	Optional
296	MVN	C	Generated	Medium Vtn adjust	Optional
295	MVP	C	Generated	Medium Vtp adjust	Optional
131	DG	D	Generated	Dual Gate	Must
130	GT	D	Drawn	Poly Gate / Poly-1 / ONO Gate	Must
116	NLL	C	Generated	NMOS LDD Implant for Low VDD	Must
113	PLL	C	Generated	PMOS LDD Implant for Low VDD	Must
115	PLH	C	Generated	PMOS LDD Implant for High VDD	Must
114	NLH	C	Generated	NMOS LDD Implant for High VDD	Must
110	ESD1	C	Drawn	ESD Implant for 1	Optional
198	SN	C	Drawn	N+ S/D Implant	Must
197	SP	C	Drawn	P+ S/D Implant	Must
413	HRP	C	Drawn	High Resistant Poly Imp	Optional
155	SAB	D	Drawn	Resist Protect Oxide / Salicide Block	Must
156	CT	C	Drawn	Contact Hole (Metal to Si/Poly)	Must

Mask ID	Mask Name	Dig. Area Tone	Mask Generation	Mask Purpose	Optional
160	M1	C	Generated	Metal-1	Must
178	V1	C	Drawn	Via-1 Hole	Must
180	M2	C	Generated	Metal-2	Must
179	V2	C	Drawn	Via-2 Hole	Must
181	M3	C	Generated	Metal-3	Must
177	V3	C	Drawn	Via-3 Hole	Must
182	M4	C	Generated	Metal-4	Must
176	V4	C	Drawn	Via-4 Hole	Must
183	M5	C	Generated	Metal-5	Must
175	V5	C	Drawn	Via-5 Hole	Must
184	M6	C	Generated	Metal-6	Must
174	V6	C	Drawn	Via-6 Hole	Must
185	M7	C	Generated	Metal-7	Must
162	MIM	D	Drawn	Top Plate of MIM Capacitor	Optional
132	P2	D	Drawn	Poly-2 or MIM plate 2	Optional
142	TV1	C	Drawn	First Top Via	Optional
141	TM1	C	Generated	First Top Metal	Optional
144	TV2	C	Drawn	Second Top Via	Must
143	TM2	C	Generated	Second Top Metal	Must
107	PA	C	Drawn	Passivation / Pad	Must
108	ALPA	D	Generated	AL Bonding Pad	Must
163	MD	C	Drawn	Metal about top metal for redistribution, Passivation 2	Optional
106	FUSE	C	Drawn	Fuse Window	Optional

Note: Please refer DCC document PM-DATA-02-2001 layer mapping table 1 for the pure generated layer GDS No. /data type which is only for Tech. file development usage. Designers do not need to draw the layers.

f) SMIC mask layer name mapping table (IO Voltage: 3.3V) for 1.5V/ 3.3V mix-signal product SMIC tape out usage. (Top tier table ID: MSGL13-V03)

Mask ID	Process Name	Dig. Area Tone	Mask Generation	Description	Optional
292	DNW	C	Drawn	Deep N well imp for substrate noise suppression	Optional
120	AA	D	Generated	Active Area/SDG	Must
901	KV	C	Drawn	Alignment mark clearing	Optional
192	NW	C	Generated	N-Well / N-Tub	Must
191	PW	C	Generated	P-Well / P-Tub	Must
492	NWH	C	Generated	N well I/O	Must
491	PWH	C	Generated	P well I/O	Must
193	NC	C	Generated	N-Cell Implant	Optional
131	DG	D	Generated	Dual Gate	Must
130	GT	D	Drawn	Poly Gate / Poly-1 / ONO Gate	Must
116	NLL	C	Generated	NMOS LDD Implant for Low VDD	Must
113	PLL	C	Generated	PMOS LDD Implant for Low VDD	Must
115	PLH	C	Generated	PMOS LDD Implant for High VDD	Must
114	NLH	C	Generated	NMOS LDD Implant for High VDD	Must
110	ESD1	C	Drawn	ESD Implant for 1	Optional
198	SN	C	Drawn	N+ S/D Implant	Must
197	SP	C	Drawn	P+ S/D Implant	Must
413	HRP	C	Drawn	High Resistant Poly Imp	Optional
155	SAB	D	Drawn	Resist Protect Oxide / Salicide Block	Must
156	CT	C	Drawn	Contact Hole (Metal to Si/Poly)	Must
160	M1	C	Generated	Metal-1	Must
178	V1	C	Drawn	Via-1 Hole	Must
180	M2	C	Generated	Metal-2	Must
179	V2	C	Drawn	Via-2 Hole	Must
181	M3	C	Generated	Metal-3	Must
177	V3	C	Drawn	Via-3 Hole	Must
182	M4	C	Generated	Metal-4	Must
176	V4	C	Drawn	Via-4 Hole	Must
183	M5	C	Generated	Metal-5	Must
175	V5	C	Drawn	Via-5 Hole	Must
184	M6	C	Generated	Metal-6	Must
174	V6	C	Drawn	Via-6 Hole	Must
185	M7	C	Generated	Metal-7	Must
162	MIM	D	Drawn	Top Plate of MIM Capacitor	Optional
132	P2	D	Drawn	Poly-2 or MIM plate 2/Poly gate trim slot	Optional
142	TV1	C	Drawn	First Top Via	Optional
141	TM1	C	Generated	First Top Metal	Optional

Mask ID	Process Name	Dig. Area Tone	Mask Generation	Description	Optional
144	TV2	C	Drawn	Second Top Via	Must
143	TM2	C	Generated	Second Top Metal	Must
107	PA	C	Drawn	Passivation / Pad	Must
108	ALPA	D	Generated	AL Bonding Pad	Must
163	MD	C	Drawn	Metal about top metal for redistribution, Passivation 2	Optional
106	FUSE	C	Drawn	Fuse Window	Optional

7.1.6 SMIC device mask truth table and device layout truth table

7.1.6.1 1.2/2.5/3.3V generic device Mask truth table

The layer marked in "1" denotes this mask layer is a must for the device.
The layer marked in "0" denotes this mask layer is must not for the device.
The layer marked in "*" denotes this mask layer is uncaring for the device structures or is based on circuit level design requirement.
For MOS SAB/ESD1 mask layers setting "0/*", the "0"denotes SAB/ESD1 mask layers are must not for typical MOS device; The "*" denotes the special usage for ESD MOS only. LVS will treat "0/*" as "*".

Device type	Mask layer		DNW	AA	NW	PW	NWH	PWH	NC	PC	MVN	MVP	DG	GT	PLL	NLL	PLH	NLH	SN	SP	HRP	SAB	ESD1	MIM	P2	FUSE
	Mask Layer No.		292	120	192	191	492	491	193	194	295	296	131	130	113	116	115	114	198	197	413	155	110	162	132	106
	Mask Layer Tone		C	D	C	C	C	C	C	C	C	C	D	D	C	C	C	C	C	C	C	D	C	D	D	C
MOS	1.2v SVT NMOS		*	1	0	1	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0/*	0/*	*	*	0
	1.2v SVT PMOS		*	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0/*	0	*	*	0
	1.2v HVT NMOS		*	1	0	1	0	0	1	0	0	0	0	1	0	1	0	0	1	0	0	0/*	0/*	*	*	0
	1.2v HVT PMOS		*	1	1	0	0	0	0	1	0	0	0	1	1	0	0	0	0	1	0	0/*	0	*	*	0
	1.2v LVT NMOS		*	1	0	1	0	0	0	0	1	0	0	1	0	1	0	0	1	0	0	0/*	0/*	*	*	0
	1.2v LVT PMOS		*	1	1	0	0	0	0	0	0	1	0	1	1	0	0	0	0	1	0	0/*	0	*	*	0
	2.5v/3.3v NMOS		*	1	0	0	0	1	0	0	0	0	1	1	0	0	0	1	1	0	0	0/*	0/*	*	*	0
	2.5v/3.3v PMOS		*	1	0	0	1	0	0	0	0	0	1	1	0	0	1	0	0	1	0	0/*	0	*	*	0
	Native NMOS	1.2v	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	*	*	0
		2.5v/3.3v	0	1	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	*	*	0
SRAM	NMOS		*	1	0	1	0	0	1	0	0	0	0	1	0	1	0	0	1	0	0	0	0	*	*	0
	PMOS		*	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	0	*	*	0
BJT	2.5v/3.3v PNP		0	1	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	1	0	0	0	*	*	0
	1.2v PNP		0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	*	*	0
	2.5v/3.3v NPN		1	1	0	0	0	1	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	*	*	0
	1.2v NPN		1	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	*	*	0
Resistor	Diffusion Non-salicide Resistor	N+	*	1	0	1	0	0	0	0	0	0	*	0	0	1	0	0	1	0	0	1	0	*	*	0
		P+	*	1	1	0	0	0	0	0	0	0	*	0	1	0	0	0	0	1	0	1	0	*	*	0
	Diffusion Salicide Resistor	N+	*	1	0	1	0	0	0	0	0	0	*	0	0	1	0	0	1	0	0	0	0	*	*	0
		P+	*	1	1	0	0	0	0	0	0	0	*	0	1	0	0	0	0	1	0	0	0	*	*	0
	Poly Non-salicide Resistor	N+	*	0	*	*	0	0	0	0	0	0	*	1	0	1	0	0	1	0	0	1	0	*	*	0
		P+	*	0	*	*	0	0	0	0	0	0	*	1	1	0	0	0	0	1	0	1	0	*	*	0
	Poly Salicide Resistor	N+	*	0	*	*	0	0	0	0	0	0	*	1	0	1	0	0	1	0	0	0	0	*	*	0
		P+	*	0	*	*	0	0	0	0	0	0	*	1	1	0	0	0	0	1	0	0	0	*	*	0
	Nwell Resistor	AA	0	1	1	0	0	0	0	0	0	0	*	0	0	0	0	0	0	0	0	1	0	*	*	0
		Under STI	0	0	1	0	0	0	0	0	0	0	*	0	0	0	0	0	*	0	0	0	0	*	*	0
	High Resistance Poly		*	0	*	*	0	0	0	0	0	0	*	1	0	0	0	0	0	0	1	1	0	*	*	0
Diode	1.2v N+ /Pwell		*	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	*	*	0

Device type	Mask layer		DNW	AA	NW	PW	NWH	PWH	NC	PC	MVN	MVP	DG	GT	PLL	NLL	PLH	NLH	SN	SP	HRP	SAB	ESD1	MIM	P2	FUSE
	Mask Layer No.		292	120	192	191	492	491	193	194	295	296	131	130	113	116	115	114	198	197	413	155	110	162	132	106
	Mask Layer Tone		C	D	C	C	C	C	C	C	C	C	D	D	C	C	C	C	C	C	C	D	C	D	D	C
	1.2v HVT N+ /Pwell		*	1	0	1	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	*	*	0
	1.2v LVT N+ /Pwell		*	1	0	1	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	*	*	0
	1.2v P+ /Nwell		*	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	*	*	0
	1.2v HVT P+ /Nwell		*	1	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	*	*	0
	1.2v LVT P+ /Nwell		*	1	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	*	*	0
	1.2v Native N+/Psub Diode		0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	*	*	0
	2.5v/3.3v N+ /Pwell		*	1	0	0	0	1	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	*	*	0
	2.5v/3.3v P+ /Nwell		*	1	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	1	0	0	0	*	*	0
	2.5/3.3v Native N+/Psub Diode		0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	*	*	0
	BPW(1.2v)/Dnwell		1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	0
	BPW(2.5v/3.3v)/Dnwell		1	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	*	*	0
	Dnwell/Psub		1	1	*	0	0	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	*	*	0
	Nwell(1.2v) /Psub		0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	*	*	0
	Nwell(2.5v/3.3v) /Psub		0	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	*	*	0
MOS Varactor	1.2v N+ Poly /NWell MOS Varactor		*	1	1	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	*	*	0
	2.5v/3.3v N+ Poly /NWell MOS Varactor		*	1	0	0	1	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	*	*	0
MIM capacitor	MIM capacitor (C = 1.0fF/um^2 or 1.5fF/um^2) one mask		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	0	0
	MIM capacitor (C = 2.0fF/um^2) two masks		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	1	0
	MIM capacitor (C = 3.0fF/um^2) stack MIM		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	0	0
FUSE	Poly E-FUSE		*	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	*	0	0	0	0	0	0
	Metal Laser Fuse		*	0	0	1	0	0	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	1
ESD	1.2v ESD NMOS		*	1	0	1	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	1	1	*	*	0
	1.2v ESD PMOS		*	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	*	*	0
	3.3v ESD NMOS		*	1	0	0	0	1	0	0	0	0	1	1	0	0	0	1	1	0	0	1	1	*	*	0
	3.3v ESD PMOS		*	1	0	0	1	0	0	0	0	0	1	1	0	0	1	0	0	1	0	1	0	*	*	0
Inductor			*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0	*	0	0	0	0
MOM capacitor			*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0

Note: MVN/MVP masks are used for SVT and HVT device implantation. If design exists LVT device,

MVN/MVP masks are must. If design doesn't exist LVT device, MVN/MVP masks are not necessary.

7.1.6.2 1.2/2.5/3.3V generic device layout truth table

The layer marked in "1" denotes this layer is a must for the device.
The layer marked in "0" denotes this layer is must not for the device.
The layer marked in "*" denotes this layer is uncaring for the device structures or is based on circuit level design requirement.
For MOS SAB/ESD1 layers setting "0/*", the "0"denotes SAB/ESD1 layers are must not for typical MOS device; The "*" denotes the special usage for ESD MOS only. LVS will treat "0/*" as "*".

Drawing Layer Name			Model Name	DNW	AA	NW	PSUB	NC	PC	MVN	MVP	DG	GT	SN	SP	HRP	SAB	RESP1	RESAA	RESNW	HRPDMY	VARMOS	DMPNP	OPCBA	OPCBP	OPCBM	INST	DSTR	ESD1	EFUSE	GTFUSE	FUSE	INDMY	MOMDMY	MIM	MIMDMY	P2
Drawing Layer GDS No.				19	10	14	85	21	16	45	44	29	30	40	43	39	48	96	97	95	210	93	134	100	101	102	60	138	41	81	81	81	212	211	58	211	31
Drawing Layer GDS Data Type				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	1	0	0	1	0	0	0
MOS	1.2v SVT NMOS		n12	*	1	0	0	0	0	0	0	0	1	1	0	0	0/*	0	0	0	0	0	0	0	0	0	0	0	0/*	0	0	0	0	*	*	*	*
	1.2v SVT PMOS		p12	*	1	1	0	0	0	0	0	0	1	0	1	0	0/*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	1.2v HVT NMOS		nhvt12	*	1	0	0	1	0	0	0	0	1	1	0	0	0/*	0	0	0	0	0	0	0	0	0	0	0	0/*	0	0	0	0	*	*	*	*
	1.2v HVT PMOS		phvt12	*	1	1	0	0	1	0	0	0	1	0	1	0	0/*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	1.2v LVT NMOS		nlvt12	*	1	0	0	0	0	1	0	0	1	1	0	0	0/*	0	0	0	0	0	0	0	0	0	0	0	0/*	0	0	0	0	*	*	*	*
	1.2v LVT PMOS		plvt12	*	1	1	0	0	0	0	1	0	1	0	1	0	0/*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*

Drawing Layer Name			Model Name	DNW	AA	NW	PSUB	NC	PC	MVN	MVP	DG	GT	SN	SP	HRP	SAB	RESP1	RESAA	RESNW	HRPDMY	VARMOS	DMPNP	OPCBA	OPCBP	OPCBM	INST	DSTR	ESD1	EFUSE	GTFUSE	FUSE	INDMY	MOMDMY	MIM	MIMDMY	P2
Drawing Layer GDS No.				19	10	14	85	21	16	45	44	29	30	40	43	39	48	96	97	95	210	93	134	100	101	102	60	138	41	81	81	81	212	211	58	211	31
Drawing Layer GDS Data Type				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	1	0	0	1	0	0	0
	2.5v/3.3v NMOS		n33	*	1	0	0	0	0	0	0	1	1	1	0	0	0/*	0	0	0	0	0	0	0	0	0	0	0	0/*	0	0	0	0	*	*	*	*
	2.5v/3.3v PMOS		p33	*	1	1	0	0	0	0	0	1	1	0	1	0	0/*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	Native NMOS	1.2v	nt12	0	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
		2.5v/3.3v	nt33	0	1	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
SRAM	NMOS			*	1	0	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	1	1	*	0	0	0	0	0	0	*	*	*	*
	PMOS			*	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	1	1	*	0	0	0	0	0	0	*	*	*	*
BJT	2.5v/3.3v PNP		pnp33	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	1.2v PNP		pnp12	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	2.5v/3.3v NPN		npn33	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	1.2v NPN		npn12	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	*	*	*	*
Resistor	Diffusion Non-salicide Resistor	N+	rndifsab	*	1	0	0	0	0	0	0	*	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
		P+	rpdifsab	*	1	1	0	0	0	0	0	*	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	Diffusion Salicide Resistor	N+	rndif	*	1	0	0	0	0	0	0	*	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
		P+	rpdif	*	1	1	0	0	0	0	0	*	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	Poly Non-salicide Resistor	N+	rnposab	*	0	*	0	0	0	0	0	*	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
		P+	rpposab	*	0	*	0	0	0	0	0	*	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	Poly Salicide Resistor	N+	rnpo	*	0	*	0	0	0	0	0	*	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*

Drawing Layer Name			Model Name	DNW	AA	NW	PSUB	NC	PC	MVN	MVP	DG	GT	SN	SP	HRP	SAB	RESP1	RESAA	RESNW	HRPDMY	VARMOS	DMPNP	OPCBA	OPCBP	OPCBM	INST	DSTR	ESD1	EFUSE	GTFUSE	FUSE	INDMY	MOMDMY	MIM	MIMDMY	P2
Drawing Layer GDS No.				19	10	14	85	21	16	45	44	29	30	40	43	39	48	96	97	95	210	93	134	100	101	102	60	138	41	81	81	81	212	211	58	211	31
Drawing Layer GDS Data Type				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	1	0	0	1	0	0	0
		P+	rppo	*	0	*	0	0	0	0	0	*	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	Nwell Resistor	AA	rnwaa	0	1	1	0	0	0	0	0	*	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
		Under STI	rnwsti	0	0	1	0	0	0	0	0	*	0	*	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	High Resistance Poly		rhrpo	*	0	*	0	0	0	0	0	*	1	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
Diode	1.2v N+ /Pwell		ndio12	*	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
	1.2v HVT N+ /Pwell		nhvtdio12	*	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
	1.2v LVT N+ /Pwell		nlvtdio12	*	1	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
	1.2v P+ /Nwell		pdio12	*	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
	1.2v HVT P+ /Nwell		phvtdio12	*	1	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
	1.2v LVT P+ /Nwell		plvtdio12	*	1	1	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
	1.2v Native N+/Psub Diode		ntdio12	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
	2.5v/3.3v N+ /Pwell		ndio33	*	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
	2.5v/3.3v P+ /Nwell		pdio33	*	1	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
	2.5/3.3v Native N+/Psub Diode		ntdio33	0	1	0	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
	BPW/Dnwell		rwdio33	1	1	0	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
	Dnwell/Psub		dnwdio33	1	1	*	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
	Nwell /Psub		nwdio	0	1	1	0	0	0	0	0	*	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
MOS Varactor	1.2v N+ Poly /NWell MOS Varactor		pvar12_ckt	*	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*

Drawing Layer Name			Model Name	DNW	AA	NW	PSUB	NC	PC	MVN	MVP	DG	GT	SN	SP	HRP	SAB	RESP1	RESAA	RESNW	HRPDMY	VARMOS	DMPNP	OPCBA	OPCBP	OPCBM	INST	DSTR	ESD1	EFUSE	GTFUSE	FUSE	INDMY	MOMDMY	MIM	MIMDMY	P2
Drawing Layer GDS No.				19	10	14	85	21	16	45	44	29	30	40	43	39	48	96	97	95	210	93	134	100	101	102	60	138	41	81	81	81	212	211	58	211	31
Drawing Layer GDS Data Type				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	1	0	0	1	0	0	0
	2.5v/3.3v N+ Poly /NWell MOS Varactor		pvar33_ckt	*	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
MIM capacitor	MIM capacitor (C = 1.0fF/um^2 or 1.5fF/um^2) one mask		mim1/ mim15	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0	0	0	0	*	1	1	0
	MIM capacitor (C = 2.0fF/um^2) two masks		mim2_tm	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0	0	0	0	*	1	1	1
	MIM capacitor (C = 3.0fF/um^2) stack MIM		mim3	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0	0	0	0	*	1	1	0
FUSE	Poly E-FUSE			*	0	0	0	0	0	0	0	0	1	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
	Metal Laser Fuse			*	0	0	0	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
ESD	1.2v ESD NMOS			*	1	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	*	*	*	*
	1.2v ESD PMOS			*	1	1	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	3.3v ESD NMOS			*	1	0	0	0	0	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	*	*	*	*
	3.3v ESD PMOS			*	1	1	0	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
Inductor				*	*	*	*	*	*	*	*	*	*	*	*	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
MOM capacitor				*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0	0	0	0	1	*	*	*

Note: For the drawn layers don't be listed in the device layout truth table, all of them are uncaring layers for the device list in above table. MVN/MVP drawing for LVT purpose.

7.1.6.3 1.5/3.3V low leakage device mask truth table.

The layer marked in "1" denotes this mask layer is a must for the device.
The layer marked in "0" denotes this mask layer is must not for the device.
The layer marked in "*" denotes this mask layer is uncaring for the device structures or is based on circuit level design requirement.
For MOS SAB/ESD1 mask layers setting "0/*", the "0"denotes SAB/ESD1 mask layers are must not for typical MOS device; The "*" denotes the special usage for ESD MOS only. LVS will treat "0/*" as "*".

Device Type	Mask Layer		DNW	AA	NW	PW	NWH	PWH	NC	DG	GT	PLL	NLL	PLH	NLH	SN	SP	HRP	SAB	ESD1	FUSE	MIM	P2
	Mask Layer No.		292	120	192	191	492	491	193	131	130	113	116	115	114	198	197	413	155	110	106	162	132
	Mask Layer Tone		C	D	C	C	C	C	C	D	D	C	C	C	C	C	C	C	D	C	C	D	D
MOS	1.5V NMOS		*	1	0	1	0	0	0	0	1	0	1	0	0	1	0	0	0/*	0/*	0	*	*
	1.5V PMOS		*	1	1	0	0	0	0	0	1	1	0	0	0	0	1	0	0/*	0	0	*	*
	3.3v NMOS		*	1	0	0	0	1	0	1	1	0	0	0	1	1	0	0	0/*	0/*	0	*	*
	3.3v PMOS		*	1	0	0	1	0	0	1	1	0	0	1	0	0	1	0	0/*	0	0	*	*
	Native NMOS	1.5V	0	1	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	0	*	*
		3.3v	0	1	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	*	*
SRAM	NMOS		*	1	0	1	0	0	1	0	1	0	1	0	0	1	0	0	0	0	0	*	*
	PMOS		*	1	1	0	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0	*	*
BJT	3.3v PNP		0	1	0	0	1	0	0	1	0	0	0	1	0	0	1	0	0	0	0	*	*
	1.5V PNP		0	1	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	*	*
	3.3v NPN		1	1	0	0	0	1	0	1	0	0	0	0	1	1	0	0	0	0	0	*	*

Device Type	Mask Layer		DNW	AA	NW	PW	NWH	PWH	NC	DG	GT	PLL	NLL	PLH	NLH	SN	SP	HRP	SAB	ESD1	FUSE	MIM	P2
	Mask Layer No.		292	120	192	191	492	491	193	131	130	113	116	115	114	198	197	413	155	110	106	162	132
	Mask Layer Tone		C	D	C	C	C	C	C	D	D	C	C	C	C	C	C	C	D	C	C	D	D
	1.5V NPN		1	1	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	*	*
Resistor	Diffusion Non-salicide Resistor	N+	*	1	0	1	0	0	0	*	0	0	1	0	0	1	0	0	1	0	0	*	*
		P+	*	1	1	0	0	0	0	*	0	1	0	0	0	0	1	0	1	0	0	*	*
	Diffusion Salicide Resistor	N+	*	1	0	1	0	0	0	*	0	0	1	0	0	1	0	0	0	0	0	*	*
		P+	*	1	1	0	0	0	0	*	0	1	0	0	0	0	1	0	0	0	0	*	*
	Poly Non-salicide Resistor	N+	*	0	*	*	0	0	0	*	1	0	1	0	0	1	0	0	1	0	0	*	*
		P+	*	0	*	*	0	0	0	*	1	1	0	0	0	0	1	0	1	0	0	*	*
	Poly Salicide Resistor	N+	*	0	*	*	0	0	0	*	1	0	1	0	0	1	0	0	0	0	0	*	*
		P+	*	0	*	*	0	0	0	*	1	1	0	0	0	0	1	0	0	0	0	*	*
	Nwell Resistor	AA	0	1	1	0	0	0	0	*	0	0	0	0	0	0	0	0	1	0	0	*	*
		Under STI	0	0	1	0	0	0	0	*	0	0	0	0	0	*	0	0	0	0	0	*	*
	High Resistance Poly		*	0	*	*	0	0	0	*	1	0	0	0	0	0	0	1	1	0	0	*	*
Diode	1.5V N+ /Pwell		*	1	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	*	*
	1.5V P+ /Nwell		*	1	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	*	*
	1.5V Native N+/Psub Diode		0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	*	*
	3.3v N+ /Pwell		*	1	0	0	0	1	0	1	0	0	0	0	1	1	0	0	0	0	0	*	*
	3.3v P+ /Nwell		*	1	0	0	1	0	0	1	0	0	0	1	0	0	1	0	0	0	0	*	*
	3.3v Native N+/Psub Diode		0	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	*	*

Device Type	Mask Layer		DNW	AA	NW	PW	NWH	PWH	NC	DG	GT	PLL	NLL	PLH	NLH	SN	SP	HRP	SAB	ESD1	FUSE	MIM	P2
	Mask Layer No.		292	120	192	191	492	491	193	131	130	113	116	115	114	198	197	413	155	110	106	162	132
	Mask Layer Tone		C	D	C	C	C	C	C	D	D	C	C	C	C	C	C	C	D	C	C	D	D
	Nwell(1.5v) /Psub		0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*
	Nwell(3.3v) /Psub		0	1	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	*	*
MOS Varactor	1.5V N+ Poly /Well MOS Varactor		*	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	0	*	*
	3.3v N+ Poly /Well MOS Varactor		*	1	0	0	1	0	0	1	1	0	0	0	1	1	0	0	0	0	0	*	*
MIM Capacitor	MIM capacitor (C = 1.0fF/um^2 or 1.5fF/um^2) one mask		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0	1	0
	MIM capacitor (C = 2.0fF/um^2) two masks		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0	1	1
	MIM capacitor (C = 3.0fF/um^2) stack MIM		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0	1	0
Fuse	E-FUSE		*	0	0	1	0	0	0	0	1	0	0	0	0	0	*	0	0	0	0	0	0
	Laser Fuse		*	0	0	1	0	0	0	0	*	0	0	0	0	0	0	0	0	0	1	0	0
ESD	1.5v ESD NMOS		*	1	0	1	0	0	0	0	1	0	1	0	0	1	0	0	1	1	0	*	*
	1.5v ESD PMOS		*	1	1	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	0	*	*
	3.3v ESD NMOS		*	1	0	0	0	1	0	1	1	0	0	0	1	1	0	0	1	1	0	*	*
	3.3v ESD PMOS		*	1	0	0	1	0	0	1	1	0	0	1	0	0	1	0	1	0	0	*	*
Inductor			*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0	*	0	0	0	0

Device Type	Mask Layer	DNW	AA	NW	PW	NWH	PWH	NC	DG	GT	PLL	NLL	PLH	NLH	SN	SP	HRP	SAB	ESD1	FUSE	MIM	P2
	Mask Layer No.	292	120	192	191	492	491	193	131	130	113	116	115	114	198	197	413	155	110	106	162	132
	Mask Layer Tone	C	D	C	C	C	C	C	D	D	C	C	C	C	C	C	C	D	C	C	D	D
MOM Capacitor		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0	*	*

7.1.6.4 1.5/3.3V low leakage device layout truth table.

The layer marked in "1" denotes this layer is a must for the device.
The layer marked in "0" denotes this layer is must not for the device.
The layer marked in "*" denotes this layer is uncaring for the device structures or is based on circuit level design requirement.
For MOS SAB/ESD1 layers setting "0/*", the "0"denotes SAB/ESD1 layers are must not for typical MOS device; The "*" denotes the special usage for ESD MOS only. LVS will treat "0/*" as "*".

Drawing Layer Name			Model Name	DNW	AA	NW	PSUB	NC	DG	GT	SN	SP	HRP	SAB	RESP1	RESAA	RESNW	HRPDMY	VARMOS	DMPNP	OPCBA	OPCBP	OPCBM	INST	DSTR	ESD1	EFUSE	GTFUSE	FUSE	INDMY	MOMDMY	MIM	MIMDMY	P2
Drawing Layer GDS No.				19	10	14	85	21	29	30	40	43	39	48	96	97	95	210	93	134	100	101	102	60	138	41	81	81	81	212	211	58	211	31
Drawing Layer GDS Data Type				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	1	0	0	1	0	0	0
MOS	1.5V NMOS		n15ll	*	1	0	0	0	0	1	1	0	0	0/*	0	0	0	0	0	0	0	0	0	0	0	0/*	0	0	0	0	*	*	*	*
	1.5V PMOS		p15ll	*	1	1	0	0	0	1	0	1	0	0/*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	3.3v NMOS		n33ll	*	1	0	0	0	1	1	1	0	0	0/*	0	0	0	0	0	0	0	0	0	0	0	0/*	0	0	0	0	*	*	*	*
	3.3v PMOS		p33ll	*	1	1	0	0	1	1	0	1	0	0/*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	Native NMOS	1.5v	nt15ll	0	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
		3.3v	nt33ll	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
SRAM	NMOS			*	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	1	1	*	0	0	0	0	0	0	*	*	*	*
	PMOS			*	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	1	1	*	0	0	0	0	0	0	*	*	*	*
BJT	3.3v PNP		pnp33	0	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	1.5V PNP		pnp15	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	3.3v NPN			1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	*	*	*	*

Drawing Layer Name			Model Name	DNW	AA	NW	PSUB	NC	DG	GT	SN	SP	HRP	SAB	RESP1	RESAA	RESNW	HRPDMY	VARMOS	DMPNP	OPCBA	OPCBP	OPCBM	INST	DSTR	ESD1	EFUSE	GTFUSE	FUSE	INDMY	MOMDMY	MIM	MIMDMY	P2
Drawing Layer GDS No.				19	10	14	85	21	29	30	40	43	39	48	96	97	95	210	93	134	100	101	102	60	138	41	81	81	81	212	211	58	211	31
Drawing Layer GDS Data Type				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	1	0	0	1	0	0	0
	1.5V NPN			1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	*	*	*	*
Resistor	Diffusion Non-salicide Resistor	N+	rndifsab	*	1	0	0	0	*	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
		P+	rpdifsab	*	1	1	0	0	*	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	Diffusion Salicide Resistor	N+	rndif	*	1	0	0	0	*	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
		P+	rpdif	*	1	1	0	0	*	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	Poly Non-salicide Resistor	N+	rnposab	*	0	*	0	0	*	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
		P+	rpposab	*	0	*	0	0	*	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	Poly Salicide Resistor	N+	rnpo	*	0	*	0	0	*	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
		P+	rppo	*	0	*	0	0	*	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	Nwell Resistor	AA	rnwaa	0	1	1	0	0	*	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
		Under STI	rnwsti	0	0	1	0	0	*	0	*	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	High Resistance Poly			*	0	*	0	0	*	1	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
Diode	1.5V N+ /Pwell		ndio15ll	*	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
	1.5V P+ /Nwell		pdio15ll	*	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
	1.5V Native N+/Psub Diode		ntdio15ll	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*

Drawing Layer Name			Model Name	DNW	AA	NW	PSUB	NC	DG	GT	SN	SP	HRP	SAB	RESP1	RESAA	RESNW	HRPDMY	VARMOS	DMPNP	OPCBA	OPCBP	OPCBM	INST	DSTR	ESD1	EFUSE	GTFUSE	FUSE	INDMY	MOMDMY	MIM	MIMDMY	P2
Drawing Layer GDS No.				19	10	14	85	21	29	30	40	43	39	48	96	97	95	210	93	134	100	101	102	60	138	41	81	81	81	212	211	58	211	31
Drawing Layer GDS Data Type				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	1	0	0	1	0	0	0
	3.3v N+ /Pwell		ndio33ll	*	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
	3.3v P+ /Nwell		pdio33ll	*	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
	3.3v Native N+/Psub Diode		ntdio33ll	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
	Nwell /Psub			0	1	1	0	0	*	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	*	*	*	*
MOS Varactor	1.5V N+ Poly /Well MOS Varactor			*	1	1	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	3.3v N+ Poly /Well MOS Varactor			*	1	1	0	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
MIM Capacitor	MIM capacitor (C = 1.0fF/um^2 or 1.5fF/um^2) one mask			*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0	0	0	0	*	1	1	0
	MIM capacitor (C = 2.0fF/um^2) two masks			*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0	0	0	0	*	1	1	1
	MIM capacitor (C = 3.0fF/um^2) stack MIM			*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0	0	0	0	*	1	1	0
FUSE	E-FUSE			*	0	0	0	0	0	1	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
	Laser Fuse			*	0	0	0	0	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Drawing Layer Name			Model Name	DNW	AA	NW	PSUB	NC	DG	GT	SN	SP	HRP	SAB	RESP1	RESAA	RESNW	HRPDMY	VARMOS	DMPNP	OPCBA	OPCBP	OPCBM	INST	DSTR	ESD1	EFUSE	GTFUSE	FUSE	INDMY	MOMDMY	MIM	MIMDMY	P2
Drawing Layer GDS No.				19	10	14	85	21	29	30	40	43	39	48	96	97	95	210	93	134	100	101	102	60	138	41	81	81	81	212	211	58	211	31
Drawing Layer GDS Data Type				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	1	0	0	1	0	0	0
ESD	1.5V ESD NMOS			*	1	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	*	*	*	*
	1.5V ESD PMOS			*	1	1	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
	3.3v ESD NMOS			*	1	0	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	*	*	*	*
	3.3v ESD PMOS			*	1	1	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	*	*
Inductor				*	*	*	*	*	*	*	*	*	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
MOM Capacitor				*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	0	0	0	0	1	*	*	*	*

Note: For the drawn layers don't be listed in the device layout truth table, all of them are uncaring layers.

7.1.7 Device table for dummy insertion

1. This table is for SMIC 0.11um or above technology dummy insertion script.

2. For 0.18um and above technology, If customers specially request SMIC to do dummy auto insertion when tape out, customers must draw dummy block layers: DUMBA (91;0), DUMBP(92;0) and DUMBM(90;0) to cover all SMIC IPs and 3rd party IPs, in order to prevent dummy patterns inserted in those IPs region.

3. Designers can add the dummy patterns according to their requirement, then add related dummy block layers to prevent SMIC auto dummy patterns insertion into the sensitive areas.

Dummy patterns / Device Category	Marker Layer	GDS No.	AA Dummy	Poly Dummy	Inter Metal Dummy	Top Metal dummy	Remark
	DUMBA	91;0	N	Y	Y	Y	
	DUMBP	92;0	Y	N	Y	Y	
	DUMBM	90;0	Y	Y	N	N	
AA Resistor	RESAA	97; 0	N	N	Y	Y	
NW Resistor	RESNW	95; 0	N	N	Y	Y	
Poly Resistor	RESP1	96; 0	N	N	Y	Y	
HRP	HRPDMY	210; 0	Y	Y	Y	Y	
MOS Varactor	VARMOS	93; 0	Y	Y	Y	Y	
LOGO, LMARK	LOGO; LMARK	26; 0	Y	Y	Y	Y	

Dummy patterns / **Device Category**	**Marker Layer**	**GDS No.**	**AA Dummy**	**Poly Dummy**	**Inter Metal Dummy**	**Top Metal dummy**	**Remark**
MIM	MIMDMY	211;0	Y	Y	Y	Y	
MOM	MOMDMY	211;1	Y	Y	Y	Y	
Inductor	INDMY	212; 0	Y	Y	Y	Y	Designers can draw dummy block layer based on their requirement
Fuse	FUSE	81;0	Y	Y	Y	Y	
Junction Varactor	VARJUN	94; 0	Y	Y	Y	Y	
Diode	DSTR	138; 0	Y	Y	Y	Y	
BJT	DMPNP	134;0	Y	Y	Y	Y	
Y: do dummy filling by script automatically							
N: block dummy filling by marker layer of device, and will be defined in the dummy insertion rules to avoid dummy filling.							

Note: INDMY/MIMDMY are used for mix-signal and RF device. For logic design, Designer can ignore it.

7.1.8 SMIC Metal Options table

0.13um metal options definition scheme was denoted in this section for metal layer, and is limited only to those options present in the table.

Metal Option Naming Rules:

xPyM_mIc_qTMc_sMTTc _tALPA

Where:

P = poly layers.
M = total metal layers excluding AL pad/AL RDL.
x = number of poly layers.
y = number of total metal layers excluding AL pad/AL RDL, (y = m+q+s).
Ic = Cu inter metal layers (included M1),
TMc = Cu top metal layers,
MTTc =Cu Ultra thick metal layers,
ALPA = AL pad/AL RDL layers,
m = number of Cu inter metal layers (included M1),
q = number of Cu top metal layers,
s = number of Cu ultra thick metal layers.
t = number of AL pad/AL RDL layers, (if only one ALPA layer, just remove code “t”)

For m, q, s or t =0, please remove the related items from the naming of metallization table.

Option Number		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
		TM drawn with TM GDS number (0.13um only)														TM drawn with inter metal GDS number (0.13um only)													

Metallization Options		1P4M_3Ic_1TMc_ALPA	1P4M_3Ic_1MTTc_ALPA	1P5M_4Ic_1TMc_ALPA	1P5M_4Ic_1MTTc_ALPA	1P5M_3Ic_1TMc_1MTTc_ALPA	1P6M_5Ic_1TMc_ALPA	1P6M_5Ic_1MTTc_ALPA	1P6M_4Ic_1TMc_1MTTc_ALPA	1P7M_6Ic_1TMc_ALPA	1P7M_6Ic_1MTTc_ALPA	1P7M_5Ic_1TMc_1MTTc_ALPA	1P8M_7Ic_1TMc_ALPA	1P8M_7Ic_1MTTc_ALPA	1P8M_6Ic_1TMc_1MTTc_ALPA	1P4M_3Ic_1TMc_ALPA	1P4M_3Ic_1MTTc_ALPA	1P5M_4Ic_1TMc_ALPA	1P5M_4Ic_1MTTc_ALPA	1P5M_3Ic_1TMc_1MTTc_ALPA	1P6M_5Ic_1TMc_ALPA	1P6M_5Ic_1MTTc_ALPA	1P6M_4Ic_1TMc_1MTTc_ALPA	1P7M_6Ic_1TMc_ALPA	1P7M_6Ic_1MTTc_ALPA	1P7M_5Ic_1TMc_1MTTc_ALPA	1P8M_7Ic_1TMc_ALPA	1P8M_7Ic_1MTTc_ALPA	1P8M_6Ic_1TMc_1MTTc_ALPA
M1 wiring level in FSG metal minimum pitch W / S = 0.16um / 0.17um M1 typical thickness: 2600A M1 typical Sheet Resistance: 0.0995 ohm/sq	**M1**	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
	V1	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
Mn (n = 2 ~ 8) wiring level in FSG metal minimum pitch W / S = 0.20um / 0.20um Mn typical thickness: 3850A Mn typical Sheet Resistance: 0.0606 ohm/sq	**M2**	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
	V2	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
	M3	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
	V3			V	V		V	V	V	V	V	V	V	V	V			V	V		V	V	V	V	V	V	V	V	V	V
	M4			V	V		V	V	V	V	V	V	V	V	V			V	V		V	V	V	V	V	V	V	V	V	V
	V4						V	V		V	V	V	V	V	V						V	V		V	V	V	V	V	V	V
	M5						V	V		V	V	V	V	V	V						V	V		V	V	V	V	V	V	V
	V5									V	V		V	V	V									V	V		V	V	V	V
	M6									V	V		V	V	V									V	V		V	V	V	V
	V6												V	V													V	V		
	M7												V	V													V	V		

Option Number		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
		TM drawn with TM GDS number (0.13um only)														TM drawn with inter metal GDS number (0.13um only)													
Metallization Options		1P4M_3Ic_1TMc_ALPA	1P4M_3Ic_1MTTc_ALPA	1P5M_4Ic_1TMc_ALPA	1P5M_4Ic_1MTTc_ALPA	1P5M_3Ic_1TMc_1MTTc_ALPA	1P6M_5Ic_1TMc_ALPA	1P6M_5Ic_1MTTc_ALPA	1P6M_4Ic_1TMc_1MTTc_ALPA	1P7M_6Ic_1TMc_ALPA	1P7M_6Ic_1MTTc_ALPA	1P7M_5Ic_1TMc_1MTTc_ALPA	1P8M_7Ic_1TMc_ALPA	1P8M_7Ic_1MTTc_ALPA	1P8M_6Ic_1TMc_1MTTc_ALPA	1P4M_3Ic_1TMc_ALPA	1P4M_3Ic_1MTTc_ALPA	1P5M_4Ic_1TMc_ALPA	1P5M_4Ic_1MTTc_ALPA	1P5M_3Ic_1TMc_1MTTc_ALPA	1P6M_5Ic_1TMc_ALPA	1P6M_5Ic_1MTTc_ALPA	1P6M_4Ic_1TMc_1MTTc_ALPA	1P7M_6Ic_1TMc_ALPA	1P7M_6Ic_1MTTc_ALPA	1P7M_5Ic_1TMc_1MTTc_ALPA	1P8M_7Ic_1TMc_ALPA	1P8M_7Ic_1MTTc_ALPA	1P8M_6Ic_1TMc_1MTTc_ALPA
Top Metal wiring level in USG metal minimum pitch W / S = 0.42um / 0.42um TM typical thickness: 9000A TM typical Sheet Resistance: 0.0202 ohm/sq	V3															V				V									
	M4															V				V									
	V4																	V					V						
	M5																	V					V						
	V5																				V					V			
	M6																				V					V			
	V6																							V					V
	M7																							V					V
	V7																										V		
	M8																										V		
	TV1					V			V			V			V														
	TM1					V			V			V			V														
	TV2	V	V	V	V	V	V	V	V	V	V	V	V	V	V														
	TM2	V		V			V			V			V																
Ultra Thick Metal	V3																V												

Option Number		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
		TM drawn with TM GDS number (0.13um only)														TM drawn with inter metal GDS number (0.13um only)													
Metallization Options		1P4M_3Ic_1TMc_ALPA	1P4M_3Ic_1MTTc_ALPA	1P5M_4Ic_1TMc_ALPA	1P5M_4Ic_1MTTc_ALPA	1P5M_3Ic_1TMc_1MTTc_ALPA	1P6M_5Ic_1TMc_ALPA	1P6M_5Ic_1MTTc_ALPA	1P6M_4Ic_1TMc_1MTTc_ALPA	1P7M_6Ic_1TMc_ALPA	1P7M_6Ic_1MTTc_ALPA	1P7M_5Ic_1TMc_1MTTc_ALPA	1P8M_7Ic_1TMc_ALPA	1P8M_7Ic_1MTTc_ALPA	1P8M_6Ic_1TMc_1MTTc_ALPA	1P4M_3Ic_1TMc_ALPA	1P4M_3Ic_1MTTc_ALPA	1P5M_4Ic_1TMc_ALPA	1P5M_4Ic_1MTTc_ALPA	1P5M_3Ic_1TMc_1MTTc_ALPA	1P6M_5Ic_1TMc_ALPA	1P6M_5Ic_1MTTc_ALPA	1P6M_4Ic_1TMc_1MTTc_ALPA	1P7M_6Ic_1TMc_ALPA	1P7M_6Ic_1MTTc_ALPA	1P7M_5Ic_1TMc_1MTTc_ALPA	1P8M_7Ic_1TMc_ALPA	1P8M_7Ic_1MTTc_ALPA	1P8M_6Ic_1TMc_1MTTc_ALPA
wiring level in USG metal minimum pitch W / S = 1.50um / 1.50um TM typical thickness: 30000A TM typical Sheet Resistance: 0.007ohm/sq	**M4**																V												
	V4																		V	V									
	M5																		V	V									
	V5																					V	V						
	M6																					V	V						
	V6																								V	V			
	M7																								V	V			
	V7																											V	V
	M8																											V	V
	TM2		V		V	V		V	V		V	V		V	V														
MIM Options	MIM (1 mask, 1.0 or 1.5 fF/um^2)	V	V	V	V	**V**	V	V	**V**	V	V	**V**	V	V	**V**	V	V	V	V	**V**	V	V	**V**	V	V	**V**	V	V	**V**
	BMIM (2 masks, 2.0 fF/um^2)			V	V	V	V	V	V	V	V	V	V	V	V			V	V	V	V	V	V	V	V	V	V	V	V

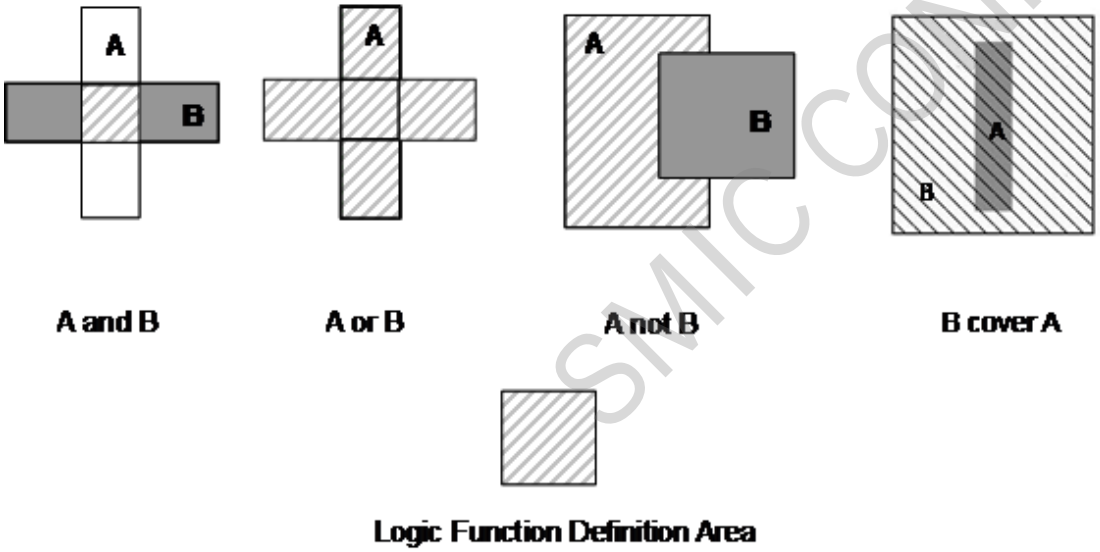
Option Number		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
		TM drawn with TM GDS number (0.13um only)														TM drawn with inter metal GDS number (0.13um only)													
Metallization Options		1P4M_3Ic_1TMc_ALPA	1P4M_3Ic_1MTTc_ALPA	1P5M_4Ic_1TMc_ALPA	1P5M_4Ic_1MTTc_ALPA	1P5M_3Ic_1TMc_1MTTc_ALPA	1P6M_5Ic_1TMc_ALPA	1P6M_5Ic_1MTTc_ALPA	1P6M_4Ic_1TMc_1MTTc_ALPA	1P7M_6Ic_1TMc_ALPA	1P7M_6Ic_1MTTc_ALPA	1P7M_5Ic_1TMc_1MTTc_ALPA	1P8M_7Ic_1TMc_ALPA	1P8M_7Ic_1MTTc_ALPA	1P8M_6Ic_1TMc_1MTTc_ALPA	1P4M_3Ic_1TMc_ALPA	1P4M_3Ic_1MTTc_ALPA	1P5M_4Ic_1TMc_ALPA	1P5M_4Ic_1MTTc_ALPA	1P5M_3Ic_1TMc_1MTTc_ALPA	1P6M_5Ic_1TMc_ALPA	1P6M_5Ic_1MTTc_ALPA	1P6M_4Ic_1TMc_1MTTc_ALPA	1P7M_6Ic_1TMc_ALPA	1P7M_6Ic_1MTTc_ALPA	1P7M_5Ic_1TMc_1MTTc_ALPA	1P8M_7Ic_1TMc_ALPA	1P8M_7Ic_1MTTc_ALPA	1P8M_6Ic_1TMc_1MTTc_ALPA
	SMIM (Stack, 3.0 fF/um^2)						V	V		V	V		V	V							V	V		V	V		V	V	
PA	**PA**	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
ALPA (ALRDL & AL PAD)	**ALPA**	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V

Note:
1. For the details about metal thickness and sheet resistance, please refer to spice model document:TD-LO13-SP-2001, TD-LO13-SP-2003.
2. SMIC IP and PDK draw TM with inter-metal GDS number. For the design with SMIC IP/PDK, it's strongly recommended to draw TM with inter-metal GDS number. For the design without SMIC IP/PDK, it's strongly recommended to draw TM with top metal GDS number.

7.1.9 Design Rule Nomenclatures and Abbreviations

(A) Logic Function Definitions

Logic Function	Definition
A **AND** B	Define the intersection area of A and B
A **OR** B	Define the union area of A and B
A **NOT** B	Define the area of A excluding the common area of A and B
B **COVER** A	Define the B area where there is A inside B.



(B) Nomenclatures and Abbreviations

Layer Name	Description
NWH	NW AND DG
PW	NOT (NW OR PSUB)
STI	NOT (AA OR AADUM)
SRAM	OPCBA or OPCBP or OPCBM

7.1.10 DRC methodology of Connectivity definition

.

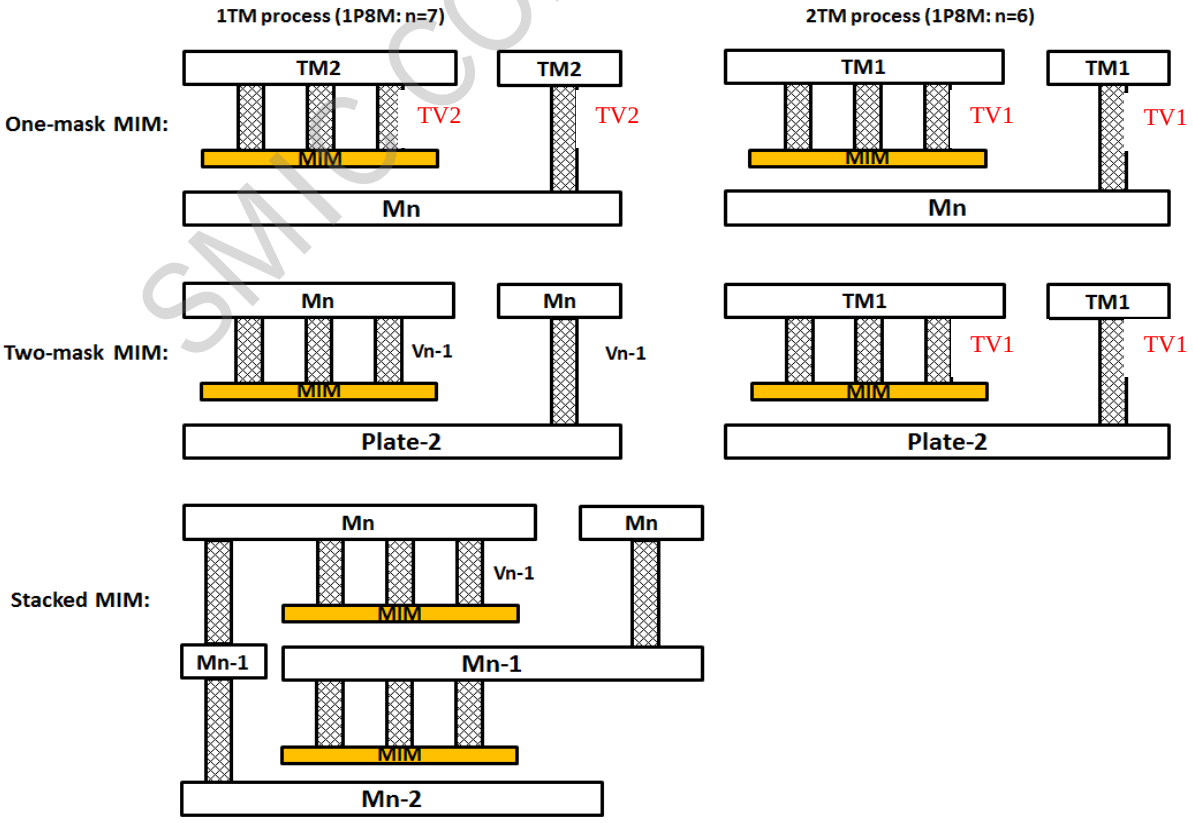
1. Poly connectivity:
   - Interconnect non-resistor silicided poly, dummy poly is excluded
   - Interconnect poly = (GT NOT (SAB OR (RESP1 OR HRPDMY))

2. NW and DNW connectivity:
   - NW interact with DNW

3. Pickup connectivity:
   - N+pickup interact with NW; P+pickup interact with (NOT (NW OR PSUB))
   - N+pickup butted P+ silicided S/D; P+pickup butted N+ silicided S/D

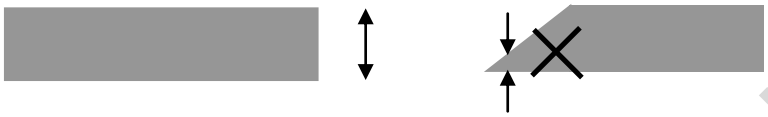
4. BEOL connectivity:
   - Silicided S/D, interconnect poly, pickup connected with M1 by CT.
   - BEOL metal (NOT metal slot), via are defined as conducting layers by default, metal dummy is excluded
   - Metal resistors and inductors are treated as conducting metal

5. MIM connectivity:
   - MIM is treated as blocking the via between metal layers of the layer above and below.
   - The via above MIM is treated as connecting MIM and its above metal layer.



7.1.11 Definition of terminology used in this design rules

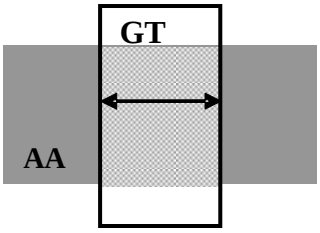
1. **Width**
   - Distance from one inside edge to a parallel inside edge within a shape along the shorter dimension of the shape.



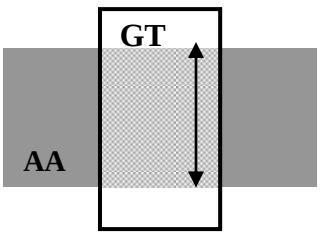
2. **Length**
   - Distance from one inside edge to a parallel inside edge within a same rectangular shape along the longer dimension of the shape.

3. **Space**
   - Distance between the outside edge of a shape to a parallel outside edge of another shape on the same layer.
   - The word "space" is also generally used to denote separation of shapes, whether or not they are on the same layer.

4. **Gate poly**
   - Channel Length: The dimension from GT edge to GT edge over AA.

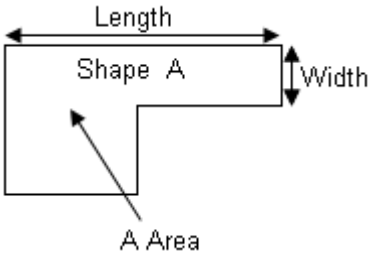


   - Channel Width: The dimension from AA edge to AA edge over GT.



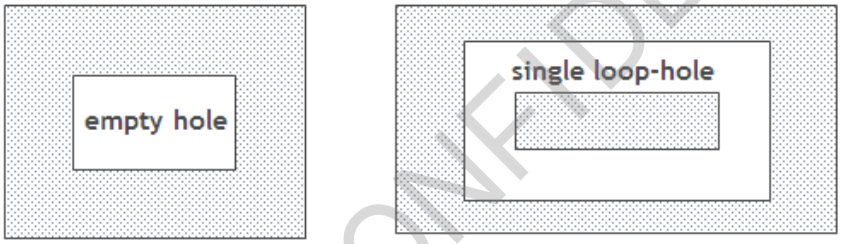
5. Area

- The area of the shape



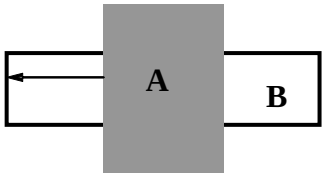
6. Enclosed Area

- The area of empty hole or single loop-hole.



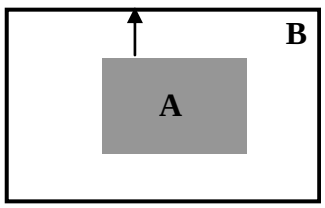
7. Extension

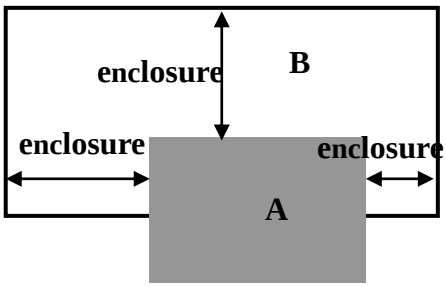
- Layer B shape extends outside layer A shape in one direction, with no restriction on the other directions.
- The minimum distance from the outside edge of the layer A shape to the inside edge of the layer B shape.



8. Enclosure

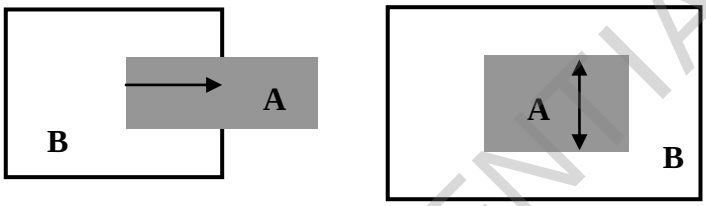
- A enclosed by B: The layer A shape is completely within the layer B shape.
- A enclosed by B: The minimum distance from the outside edge of A to the inside edge of B in all directions.





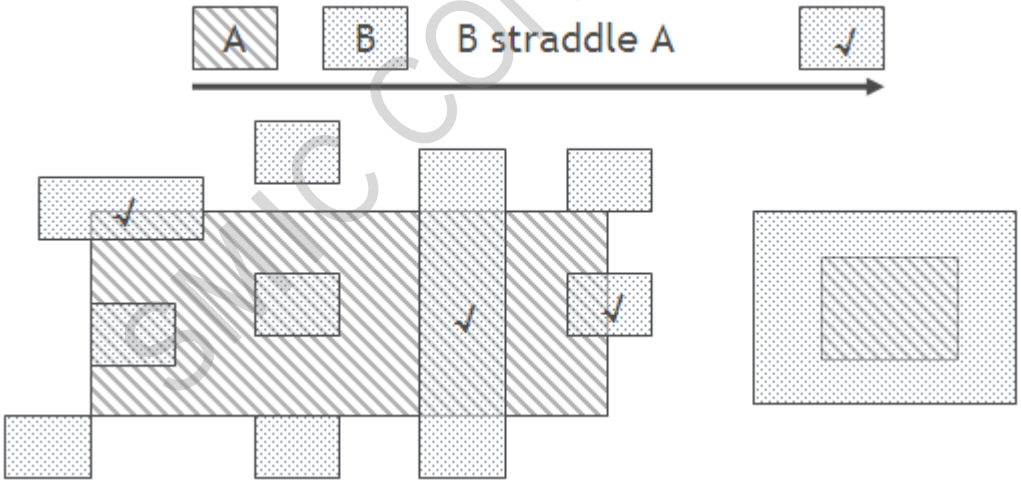
9. Overlap

- The layer A shape crosses a boundary of the layer B shape, or the layer A shape is completely enclosed by the layer B shape.
- The distance:
- (1) This distance from the inside edge of the layer A shape to the inside edge of the layer B shape.
- (2) The distance is also the width of the layer A shape for enclosed A.



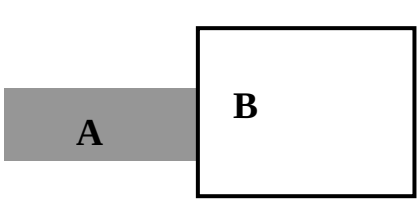
10. Straddle

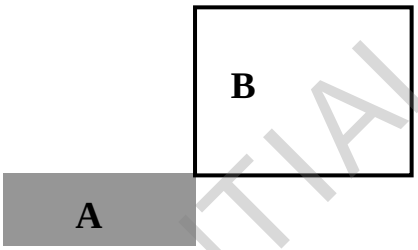
- A straddle B: A and B share part (not all) of area with each other.
- B straddle A: B and A share part (not all) of area with each other.



11. Butted

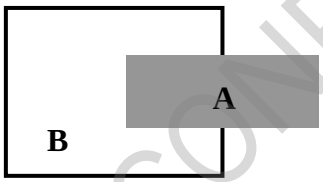
- When the layer A shape meets without going beyond a boundary of the layer B shape.

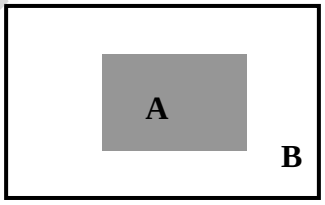


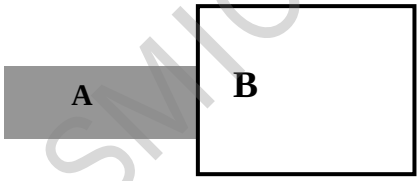


12. Interact with

- When the layer A shape overlaps or crosses or meets the layer B shape, interact with include overlap, straddle, butted three condition.

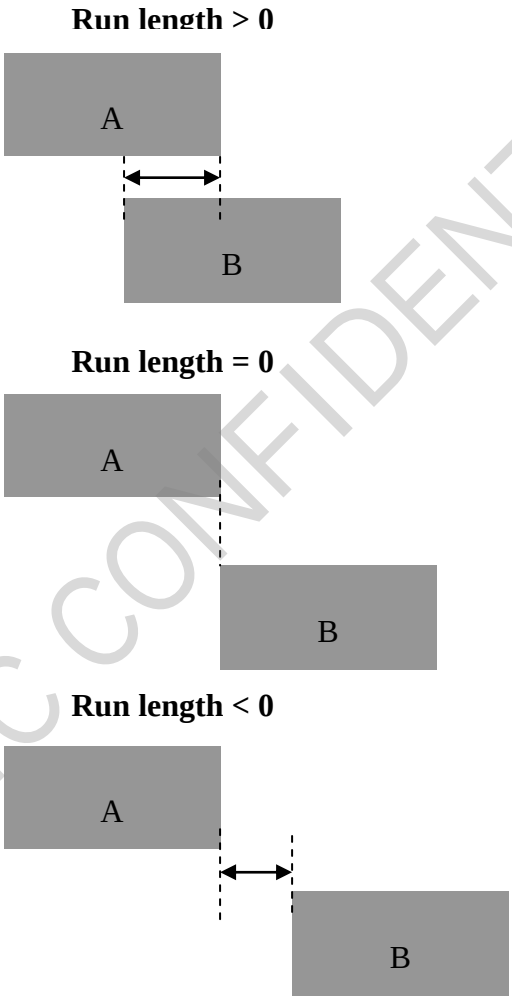






13. Run length

- The distance in which two parallel lines continuously run alongside one another.



7.1.12 Design requirements

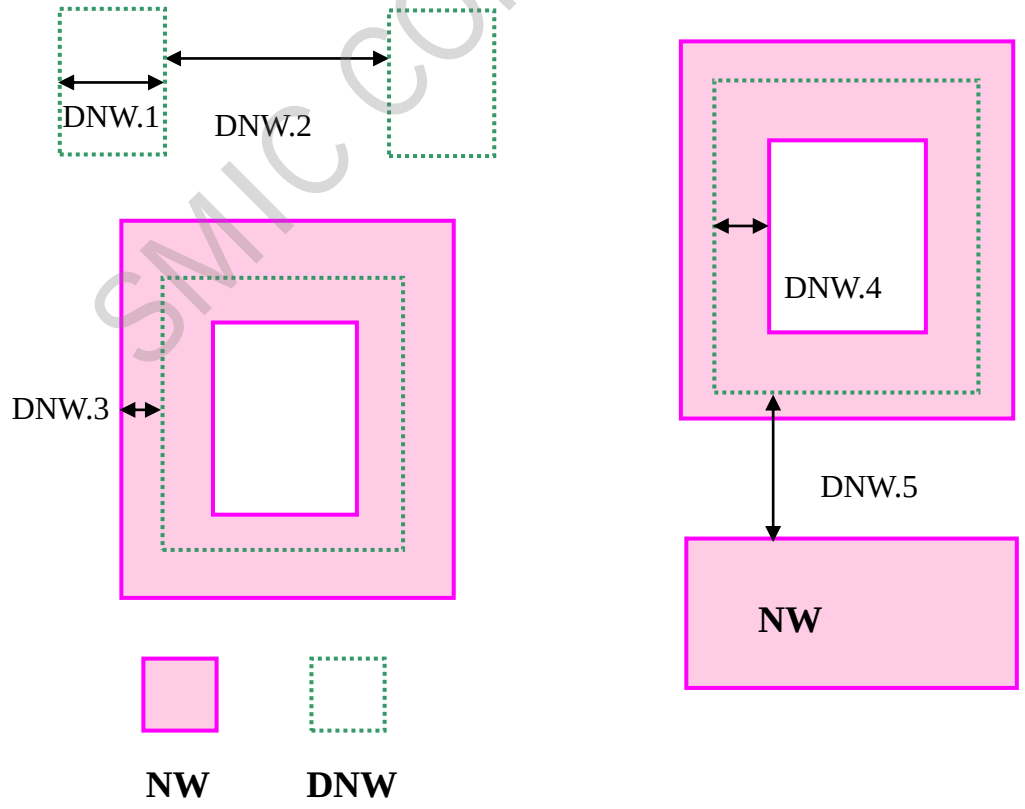
Designers should follow design requirement guidelines in this section in order to reduce the OPC loading and then enhance the OPC efficiency.

Guidelines number	Description
DGR.1[NC]	All the geometry design must be an integer multiple of 0.001 um. (0.001 um is defined base on grid size).
DGR.2[NC]	Design geometry shape must be polygons.
DGR.3	Only shapes of geometry that are orthogonal or 45-degree angle are allowed, excluding Inductor region.
DGR.4[R][NC]	Recommended to design simple rectangular shape geometry as possible, avoid L, U, H, or O shapes.
DGR.5[NC]	All line-end are must be rectangular.
DGR.6[NC]	Self-intersecting shapes are not allowed.
DGR.7[NC]	All the text or labels in the chip must be covered by the marker layer LOGO (26;0).
DGR.8[NC]	Make sure the designs are DRC clean.
DGR.9[NC]	Recommended use greater or equal half of the minimum width of each layer to avoid small jogs of geometry.
DGR.10[NC]	The layout of designs should have the well organized hierarchical structures.
DGR.11[NC]	The layout of auto dummy insertion designs should be put in a separate hierarchy from the main designs, and try to avoid the flattened dummy insertion designs.

7.2 Layout Rule Description

7.2.1 DNW: Deep N-Well design

Rules number	Description	Operation	Design Value	Unit
DNW.1	DNW width	≥	3.00	um
DNW.2	Space between DNWs	≥	6.00	um
DNW.3	DNW enclosure by NW (DNW edge outside of NW is not allowed)	≥	2.00	um
DNW.4	Overlap of NW and DNW	≥	2.00	um
DNW.5	Space between DNW and NW	≥	4.10	um
DNW.6	Space between (PW INSIDE DNW) and PW at different nets.	≥	1.20	um

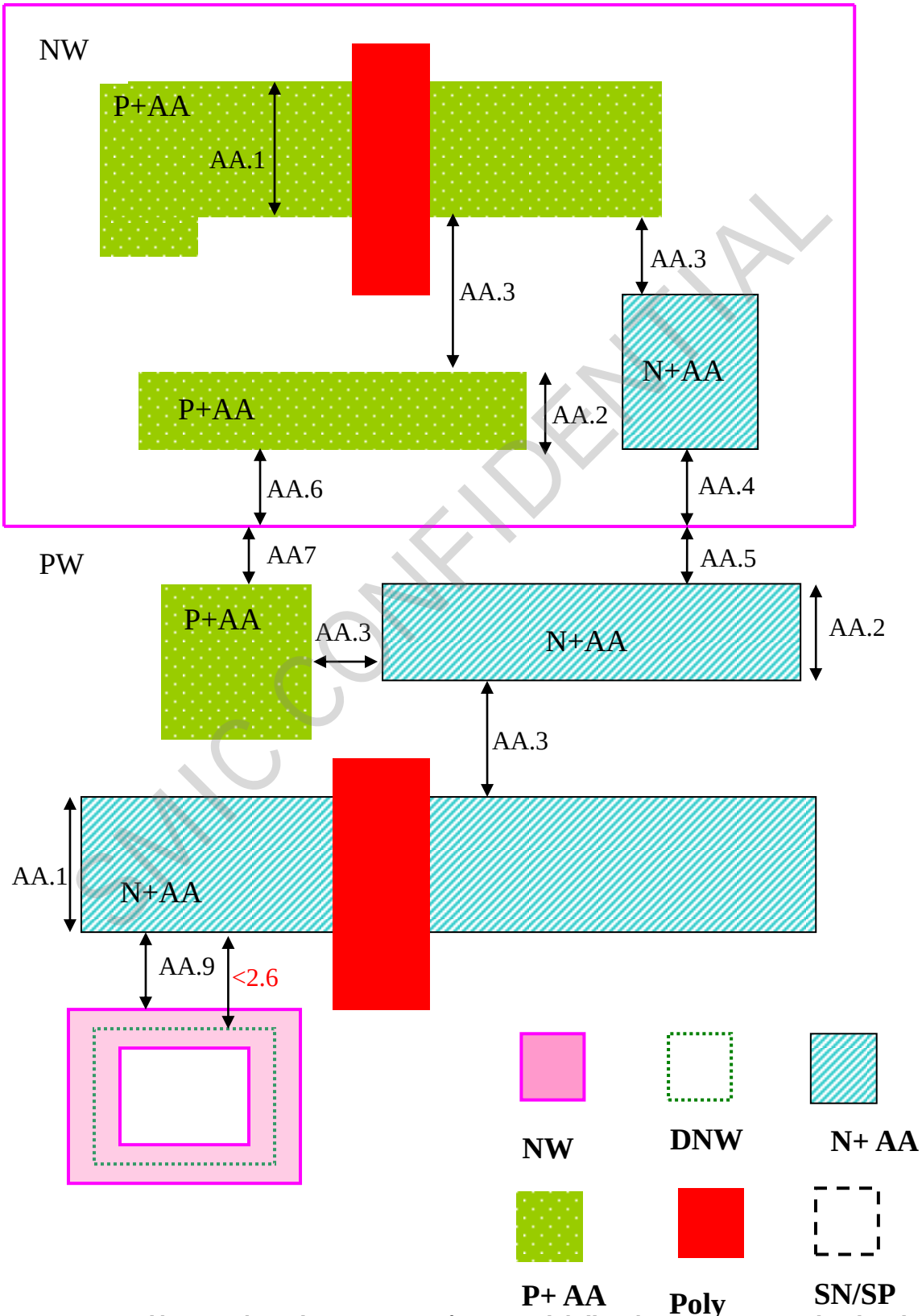


7.2.2 AA: Active Area design

Rules number	Description	Operation	Design Value	Unit
AA.1	AA width for NMOS/PMOS transistors, exclude (NW INTERACT OPCBA), SRAM region	≥	0.15	um
AA.2	AA width for interconnect, exclude (NW INTERACT OPCBA), SRAM region.	≥	0.15	um
AA.3	Space between AAs that are on the same well, exclude INDMY (212;0) covered regions, and SRAM region	≥	0.21	um
AA.4	N+AA enclosure by NW except NW resistor region, and SRAM region	≥	0.23	um
AA.5	Space between NW and N+AA, exclude SRAM region.	≥	0.30	um
AA.6	P+AA enclosure by NW, exclude (NW INTERACT OPCBA), SRAM region.	≥	0.30	um
AA.7	Space between NW to P+AA inside PW, exclude SRAM region.	≥	0.23	um
AA.8	AA area (in um^2)	≥	0.10	um^2
AA.9	Space between N+AA and NW which encloses a DNW. (DRC doesn't flag N+AA inside NW or DNW) , DRC waive check when space between DNW to N+AA is >= 2.6um in same direction.	≥	0.40	um
AA.10	AA or AA dummy pattern is not allowed to straddle on a boundary of NW except NW resistor region.			
AA.11	AA density (including dummy AA). density check window size 500μm*500μm with step size 250μm. Waive RESNW, Metal Fuse, L Mark, LOGO and Inductor. Please refer to Note1 for DRC check methodology.	≥	20%	
		≤	80%	
AA.12	AA density (including dummy AA) overlapping with DUMBA. Density check window size500μm*500μm with step size 250μm.	≥	20%	
		≤	80%	

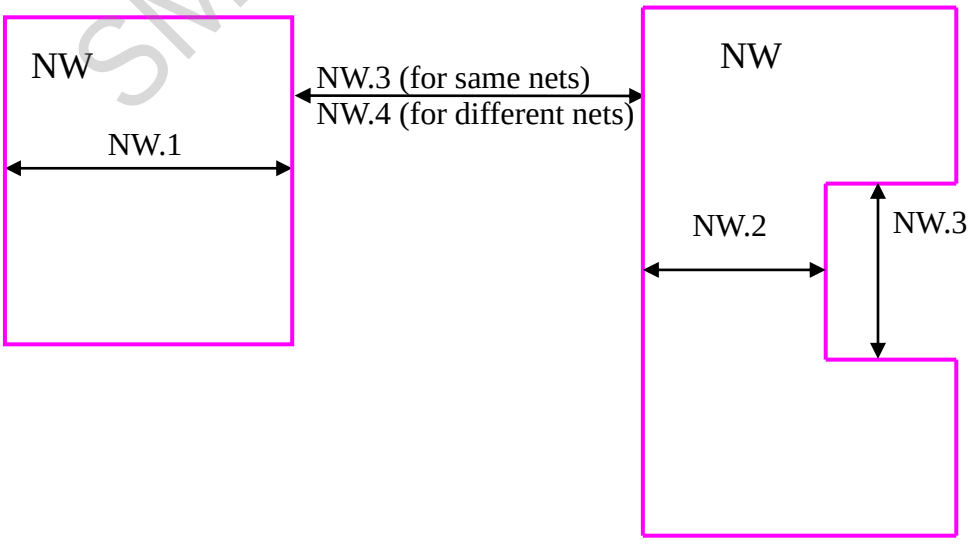
Note:

1. AA.11 DRC check with the said window size and rule number and highlight as X. Y = X not (RESNW or Metal Fuse or LMARK or LOGO or INDMY), Z= (Y area)/(250*250) If Z > 25%, highlight Y for AA density inside of Y that cannot meet of rule value requirement.
2. PIE need waive the AA.11, AA.12 DRC violation in the chip corner stress relief area and seal ring if the seal ring is added by SMIC.



7.2.3 NW: N-Well design

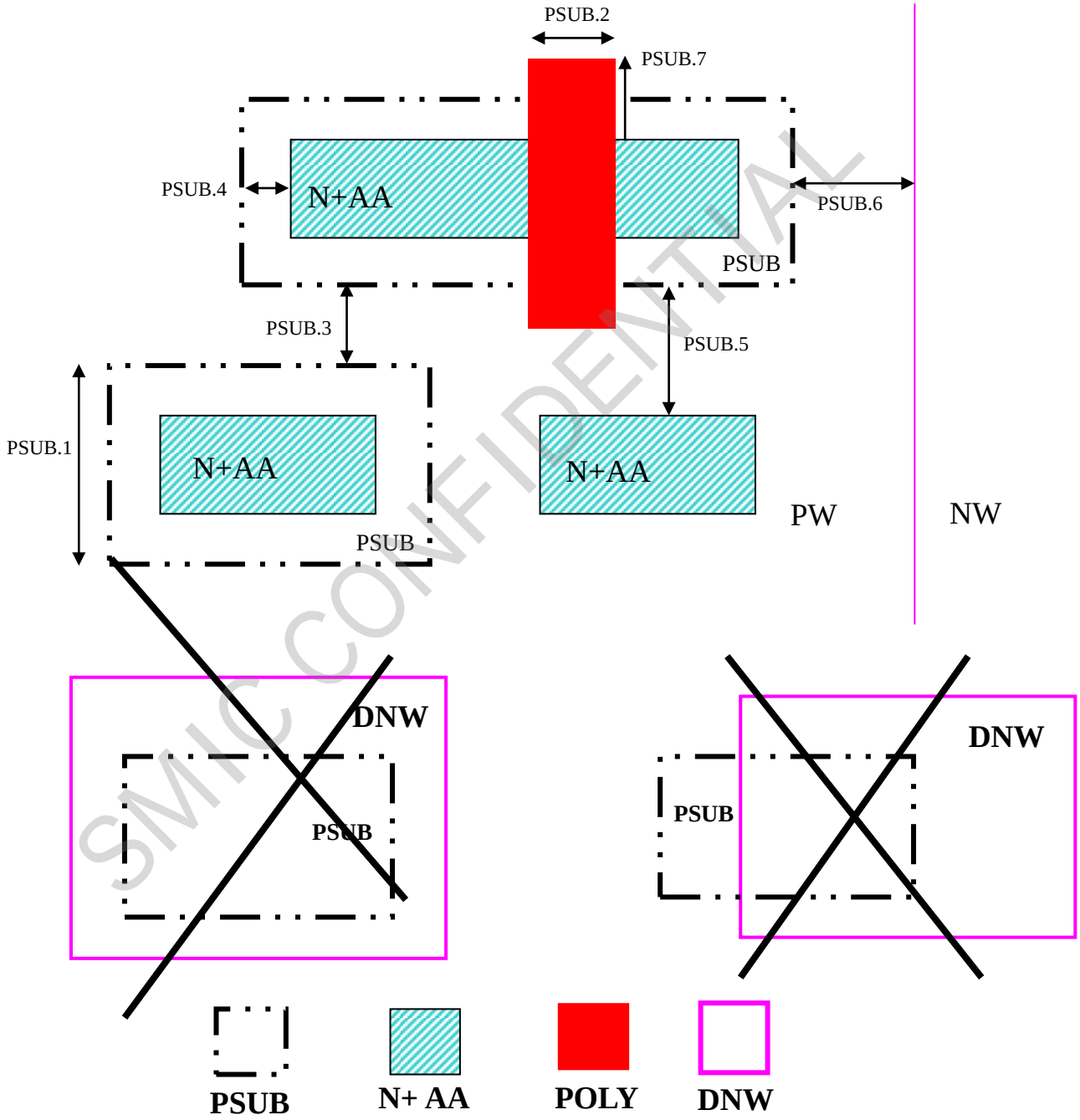
Rules number	Description	Operation	Design Value	Unit
NW.1	NW width	≥	0.60	um
NW.2	NW width for NW resistor	≥	1.60	um
NW.3	NW minimum space to NW for same nets.	≥	0.60	um
NW.4	NW minimum space between 1.2V/1.5V NWs for different nets	≥	1.00	um
NW.4a	NW minimum space between 1.2V/1.5V NW to 2.5V/ 3.3v NW for different nets	≥	1.20	um
NW.4b	NW minimum space between 2.5V or 3.3v NWs for different nets	≥	1.20	um
NW.5	NW area (um^2)	≥	0.92	um^2
NW.6	It is not allowed if N+AA/P+AA straddle on a boundary of the NW except NW resistor region.			
NW.7[NC]	Recommend not using unintentional floating Well.			



7.2.4 PSUB: Design to define native NMOS

PSUB is to define area for native NMOS device on P-substrate, which is not on NW nor on PW.

Rules number	Description	Operation	Design Value	Unit
PSUB.1	PSUB width	≥	0.60	um
PSUB.2a	1.2V/1.5V NMOS channel length	≥	0.30	um
PSUB.2b	2.5/3.3V NMOS channel length	≥	1.00	um
PSUB.3	Space between PSUBs.	≥	0.60	um
PSUB.4	Fixed AA enclosure by PSUB, INDMY (212;0) covered regions and NMOS capacitor are excluded for this rule check.	=	0.22	um
PSUB.5	Space between PSUB and AA	≥	0.37	um
PSUB.6	Space between PSUB and NW	≥	1.20	um
PSUB.7	Extension of native NMOS poly gate outside of AA, INDMY (212;0) covered regions are excluded for this rule check.	≥	0.31	um
PSUB.8	PSUB inside or overlap or cross over a Deep N-Well/NW is not allowed			
PSUB.9	One AA shape per PSUB shape, except for NMOS capacitor and inductor region covered by INDMY.			
PSUB.10[NC]	If PSUB is not used for Native device, DRC doesn't flag the native device related rules.			

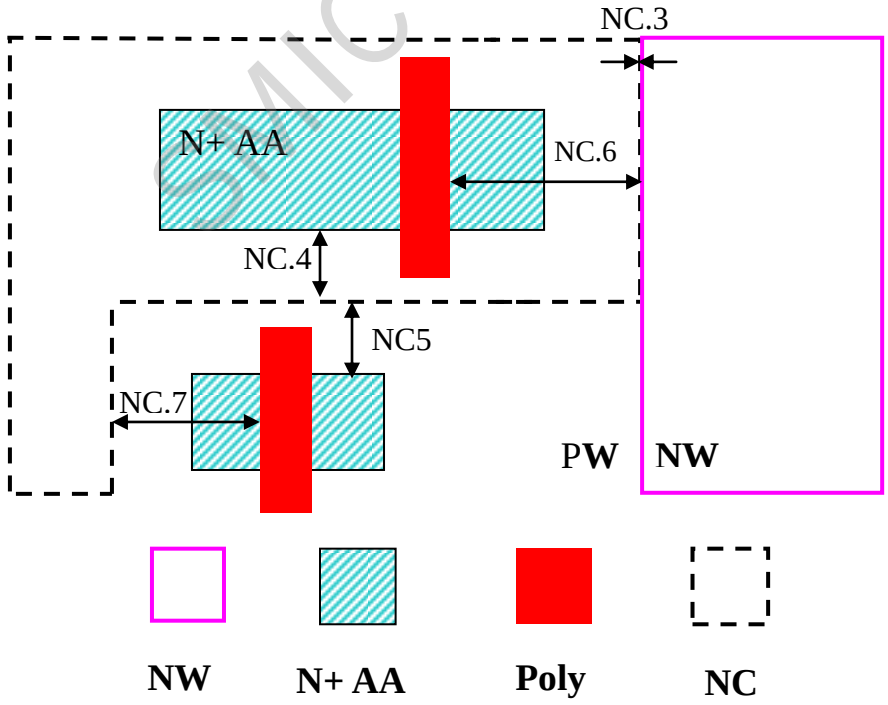


7.2.5 NC: High Vt NMOS design (optional)

A drawn layer is needed to receive additional VTN implant, if high Vt NMOS is used in the circuit. NC is for 1.2V core high Vt device only.

Rules number	Description	Operation	Design Value	Unit
NC.1	NC width	≥	0.60	um
NC.2	Space between NCs	≥	0.60	um
NC.3	NC overlap with NW is not allowed			
NC.4	NC extension outside of N+AA along poly length direction	≥	0.18	um
NC.5	Space between NC and N+AA for nominal NMOS along poly length direction, exclude SRAM region.	≥	0.18	um
NC.6	NC extension outside of poly gate along source/drain direction	≥	0.27	um
NC.7	Space between NC and poly gate for nominal device along source/drain direction	≥	0.27	um
NC.8	No NC and PSUB overlap is allowed			

Note: NC.1/NC.2 only check core HVT MOS device region

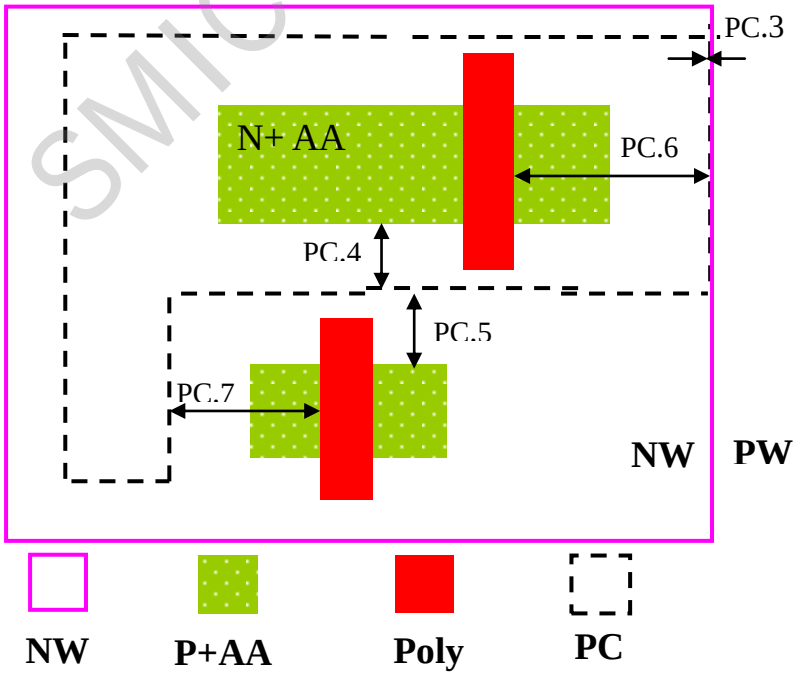


7.2.6 PC: High Vt PMOS design (optional)

A drawn layer is needed to receive additional VTP implant, if high Vt PMOS is used in the circuit. PC is for 1.2V core high Vt device only.

Rules number	Description	Operation	Design Value	Unit
PC.1	PC width	≥	0.60	um
PC.2	Space between PCs	≥	0.60	um
PC.3	PC must be fully enclosure by NW			
PC.4	PC extension outside of P+AA along poly length direction	≥	0.18	um
PC.5	Space between PC and P+AA for nominal PMOS along poly length direction	≥	0.18	um
PC.6	PC extension outside of poly gate along source/drain direction	≥	0.27	um
PC.7	Space between PC and poly gate for nominal device along source/drain direction	≥	0.27	um
PC.8	No PC and PSUB overlap is allowed			

Note: PC.1/PC.2 only check core HVT MOS device region

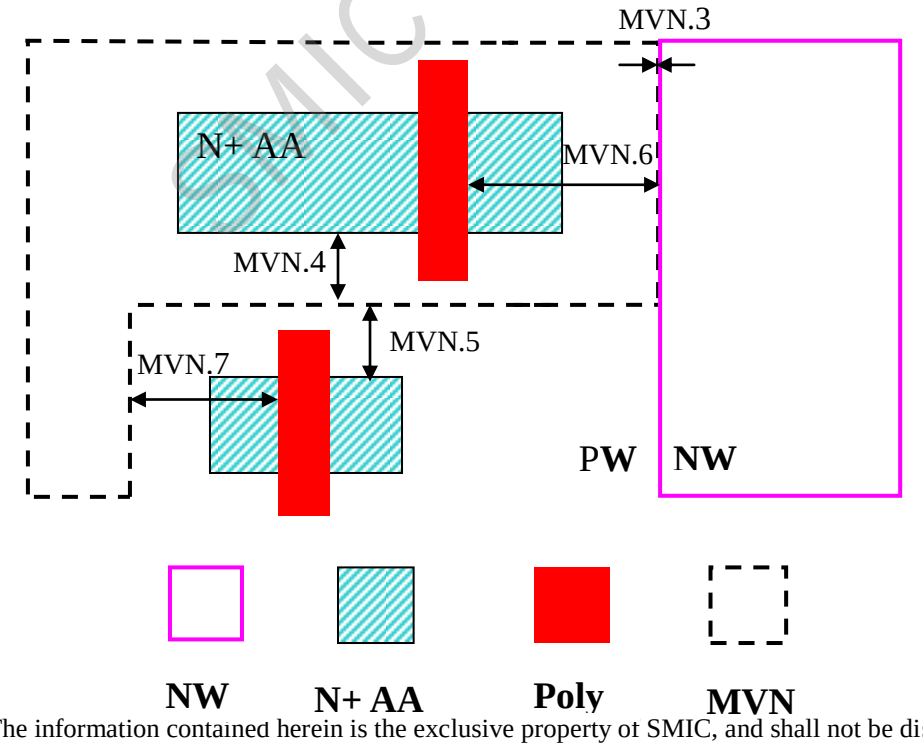


7.2.7 MVN : Low Vt NMOS design (optional)

A drawn MVN layer is needed to define low Vt NMOS devices. MVN is for 1.2V core low Vt device only.

Rules number	Description	Operation	Design Value	Unit
MVN.1	MVN width	≥	0.60	um
MVN.2	Space between MVNs	≥	0.60	um
MVN.3	MVN overlap with NW is not allowed.			
MVN.4	MVN extension outside of N+AA along poly length direction	≥	0.18	um
MVN.5	Space between MVN and N+AA for nominal NMOS along poly length direction	≥	0.18	um
MVN.6	MVN extension outside of poly gate along source/drain direction	≥	0.27	um
MVN.7	Space between MVN and poly gate for nominal device along source/drain direction	≥	0.27	um
MVN.8	No MVN and PSUB overlap is allowed			

Note: MVN.1/MVN.2 only check core LVT MOS device region

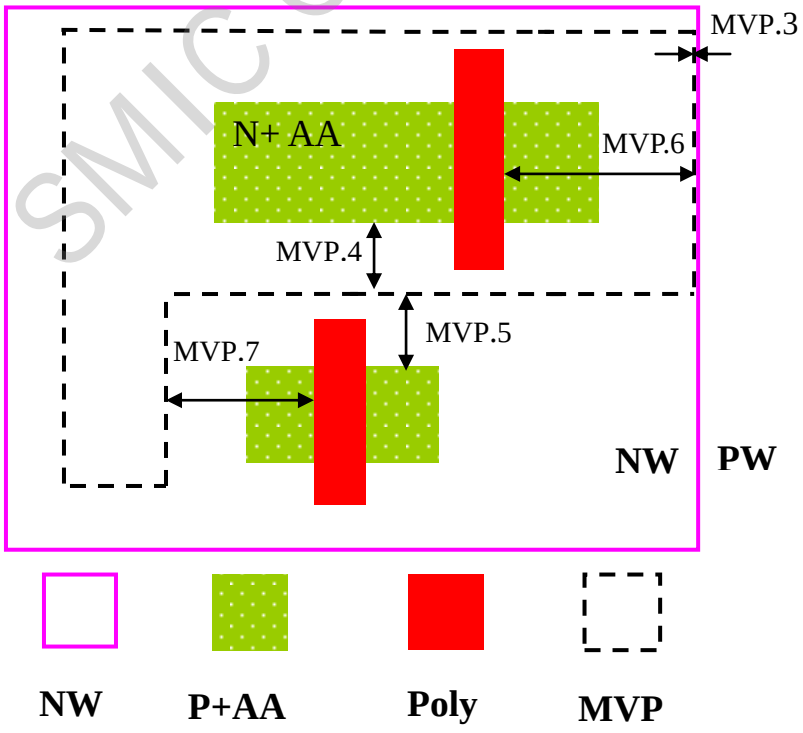


7.2.8 MVP : Low Vt PMOS design (optional)

A drawn MVP layer is needed to define low Vt PMOS devices. MVP is for 1.2V core low Vt device only.

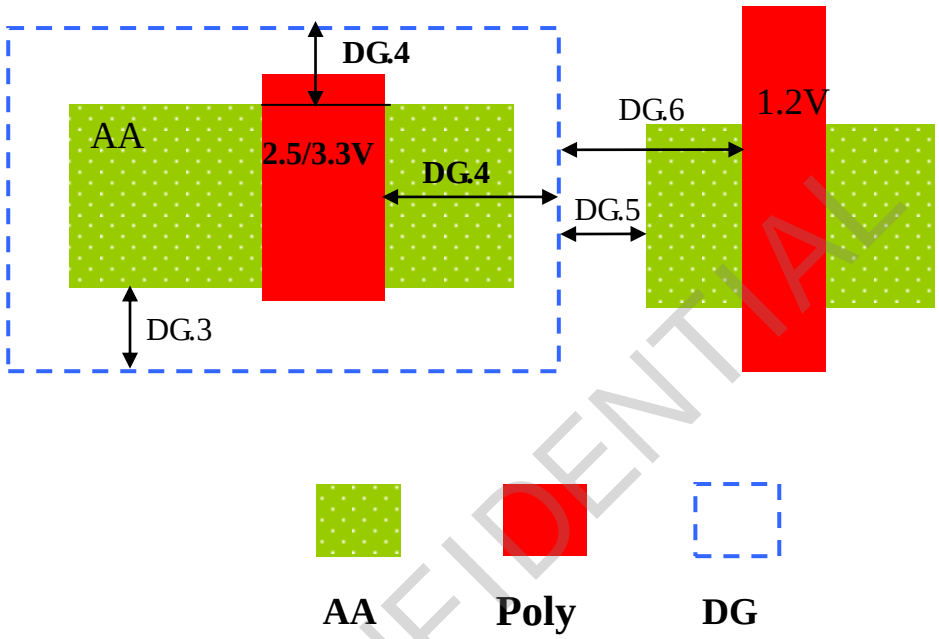
Rules number	Description	Operation	Design Value	Unit
MVP.1	MVP width	≥	0.60	um
MVP.2	Space between MVPs	≥	0.60	um
MVP.3	MVP must be fully enclosure by NW			
MVP.4	MVP extension outside of P+AA along poly length direction	≥	0.18	um
MVP.5	Space between MVP and P+AA for nominal PMOS along poly length direction	≥	0.18	um
MVP.6	MVP extension outside of poly gate along source/drain direction	≥	0.27	um
MVP.7	Space between MVP and poly gate for nominal device along source/drain direction	≥	0.27	um
MVP.8	No MVP and PSUB overlap is allowed			

Note: MVP.1/MVP.2 only check core LVT MOS device region



7.2.9 DG: Dual Gate design to define 2.5/3.3V transistor for AA

Rules number	Description	Operation	Design Value	Unit
DG.1	DG width	≥	0.70	um
DG.2	Space between two DGs	≥	0.70	um
DG.3	AA enclosure by DG	≥	0.25	um
DG.4	For 0.13um design, 2.5/3.3V transistor channel (overlap of Poly and AA) enclosure by DG. (This rule is only used for the 0.13um design DRC default switch turn-on for 0.13um design only. Designer can waive this rule for 0.11um design only.)	≥	0.27	um
DG.4b	For 0.11um design, 2.5/3.3V transistor channel (overlap of Poly and AA) enclosure by DG. (This rule is only used for the design that it will be shrinkage from 0.13um to 0.11um. DRC default switch turn-off for 0.13um design only. Designer can waive this rule for 0.13um design only)	≥	0.30	um
DG.5	Space between DG and device AA (include all the devices in the section 7.1.6 SMIC Mask layer device table)	≥	0.25	um
DG.6	Space between DG and 1.2V/1.5V transistor channel (overlap of poly and AA)	≥	0.33	um
DG.7	(Purposely blank)			
DG.8[R]	DG straddle GATE (AA AND GT) is not allowed			

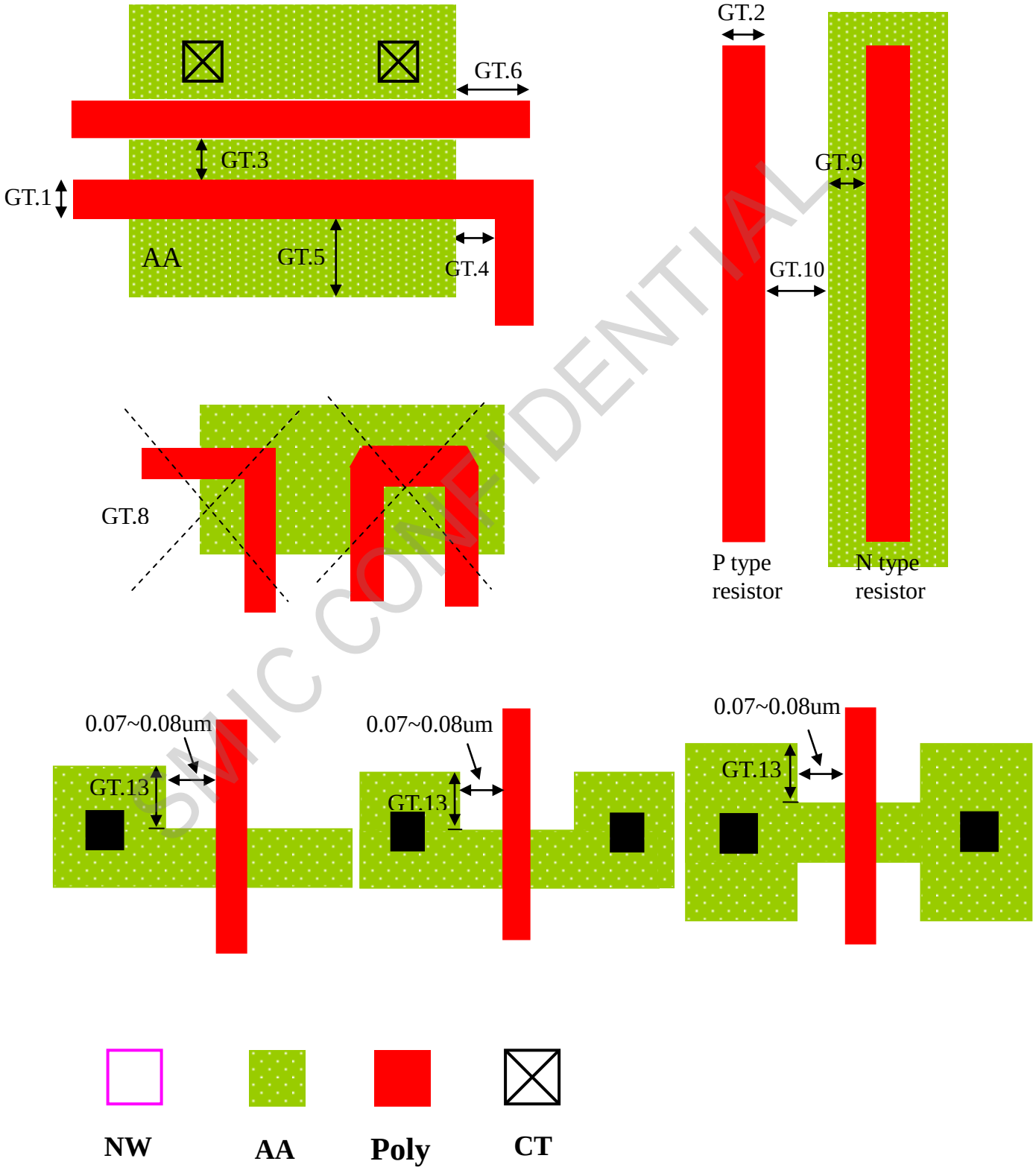


7.2.10 GT: Poly design

Rules number	Description	Operation	Design Value	Unit
GT.1a	GT width for 1.2V/1.5V NMOS /PMOS transistor	≥	0.13	um
GT.1b	GT width for 2.5V NMOS /PMOS transistor	≥	0.28	um
GT.1c	GT width for 3.3V NMOS/PMOS transistor	≥	0.35/0.30	um
GT.2	Interconnect width, exclude SRAM region.	≥	0.13	um
GT.3	Space between GTs, exclude INDMY (212;0) covered regions, and SRAM region.	≥	0.18	um
GT.4	Space between AA and GT on field oxide, exclude INDMY (212;0) covered regions, and (GT INTERACT (GT AND OPCBP)).	≥	0.07	um
GT.5	Extension of AA outside of GT (exclude GT within INDMY (212;0) covered regions, and SRAM region.	≥	0.23	um
GT.6	Extension of GT outside of AA, exclude SRAM region.	≥	0.17	um
GT.7	GT pattern density	≥	15%	
GT.8	No bent GT on AA are allowed. All GT patterns on AA have to be orthogonal to AA edge, INDMY (212;0) covered regions are excluded for this rule check.			
GT.9	NLL, NLH, SN, PLL, PLH, SP extension outside of poly resistor. Poly resistor enclosure by NLL, NLH, SN, PLL, PLH, SP	≥	0.18	um
GT.10	Space between NLL, NLH, SN and P type poly resistor or PLL, PLH, SP to N type poly resistor	≥	0.18	um
GT.11	GT used as MOS Gate poly (except HRP resistor region) must be enclosed by SN/SP/(SN or SP).			
GT.12	SN and SP overlap on gate is not allowed			

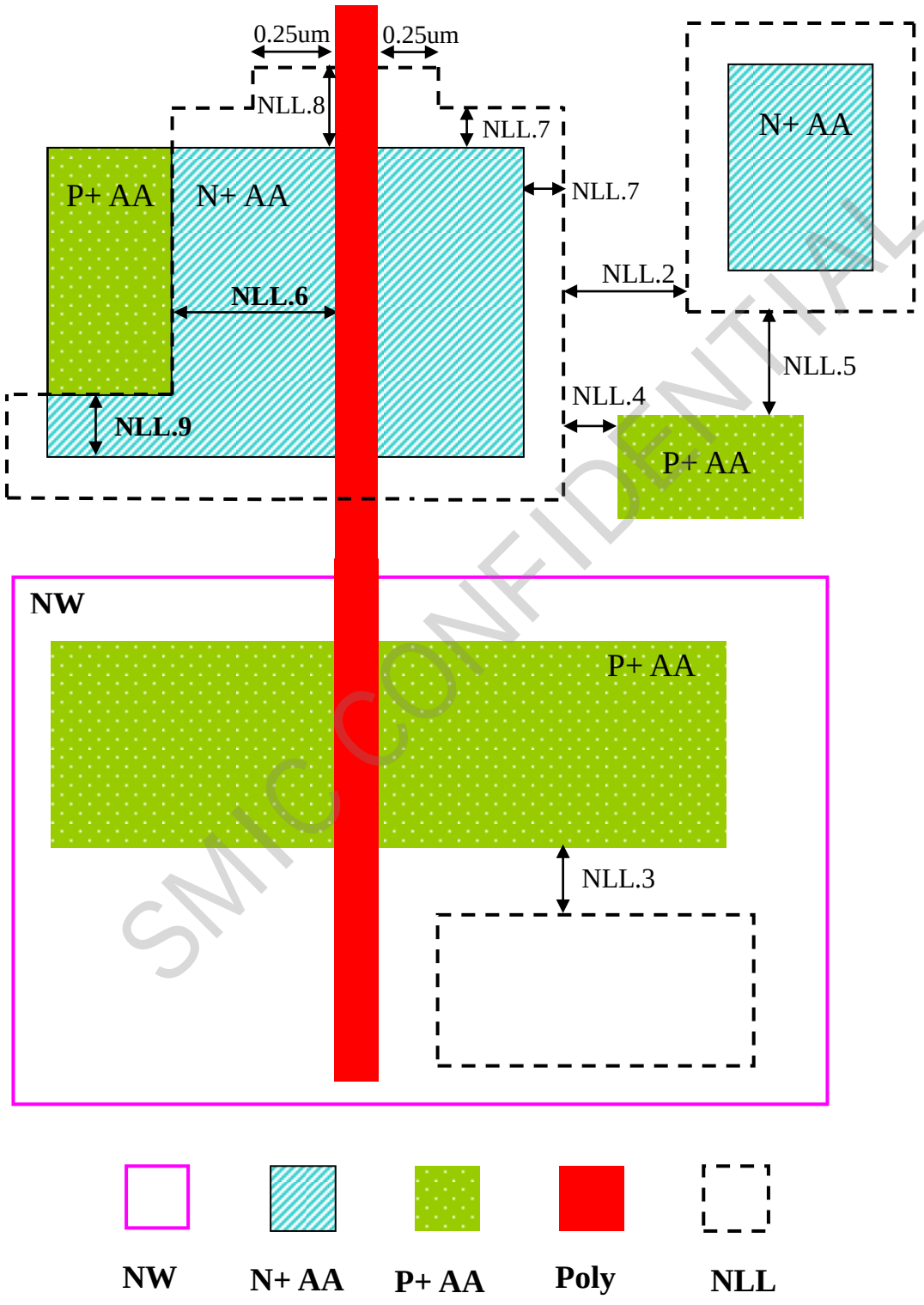
GT.13[R]	For small MOS (channel width ≤ 0.3um), Max AA size along channel width direction from the turning point when L-shape or H-shape AA space to GT is ≥ 0.07um and ≤ 0.08um, exclude SRAM region.	≤	0.075	um
GT.14[R]	Space between two CTs on poly (poly width <0.24um) to avoid voltage drop.	≤	1.00	um
GT.15[R]	Poly area	≥	0.09	um^2
GT.16[R]	Enclosed poly area	≥	0.15	um^2

Note:
1. DUMBP layer is used to block poly dummy pattern from placing on that area of chip.



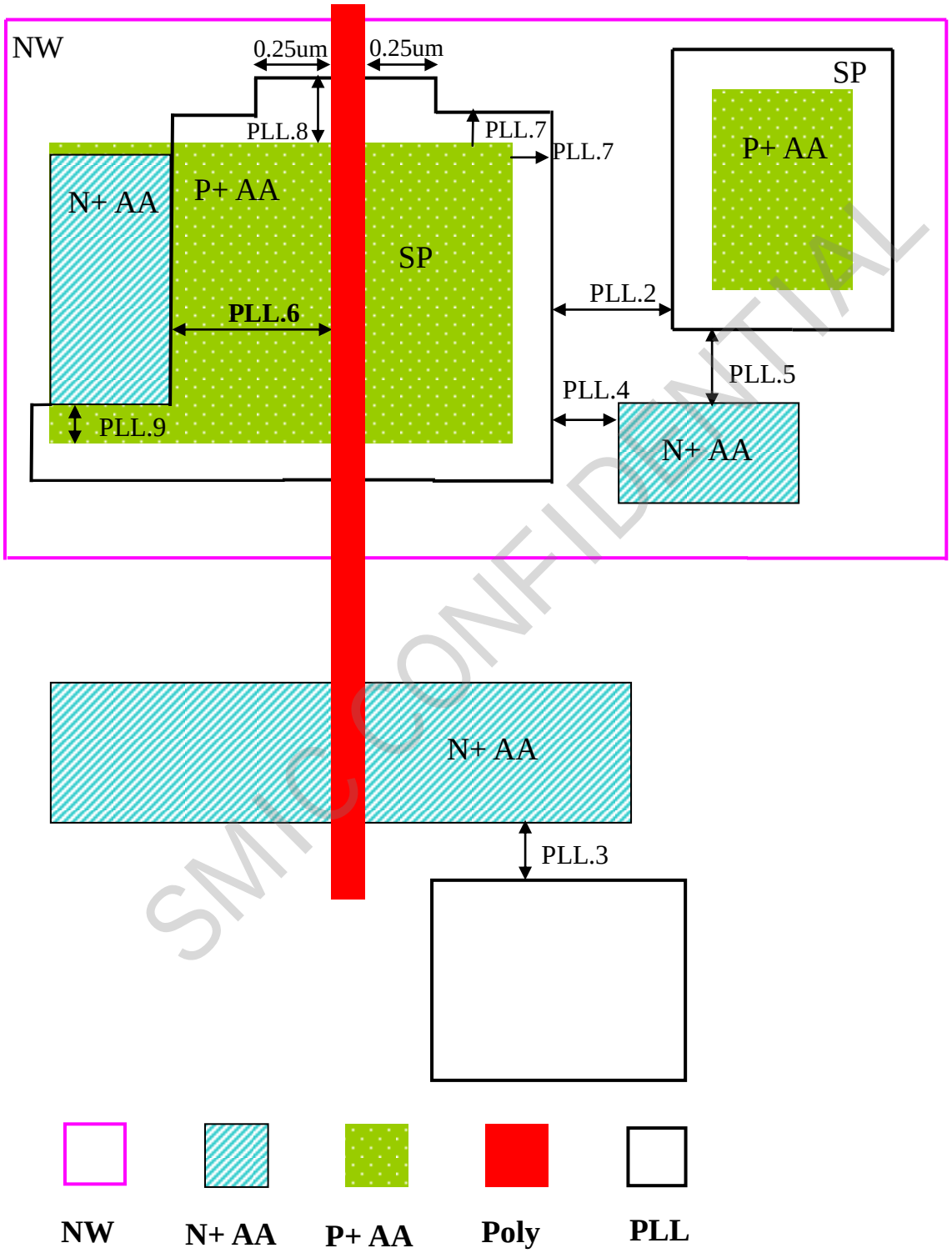
7.2.11 NLL: 1.2V/1.5V NLDD implantation design

Rules number	Description	Operation	Design Value	Unit
NLL.1	NLL width	≥	0.30	um
NLL.2	Space between NLLs.	≥	0.30	um
NLL.3	Space between NLL and P+ AA inside N well	≥	0.16	um
NLL.4	Space between NLL and P+ AA inside P well	≥	0.03	um
NLL.4b	Space between a NLL and a butted P+ AA	=	0	um
NLL.5	Space between NLL and AA with NLH, PLL or PLH implantation	≥	0.16	um
NLL.6	NLL extension outside of NMOS poly gate along source/drain direction	≥	0.40	um
NLL.7	NLL extension outside of N+AA, if distance to the related poly is larger than 0.25um	≥	0.16	um
NLL.8	NLL extension outside of N+AA, if distance to the related poly is less than 0.25um	≥	0.30	um
NLL.9	NLL and AA overlap	≥	0.16	um
NLL.10	NLL area (um^2)	≥	0.23	μm^2



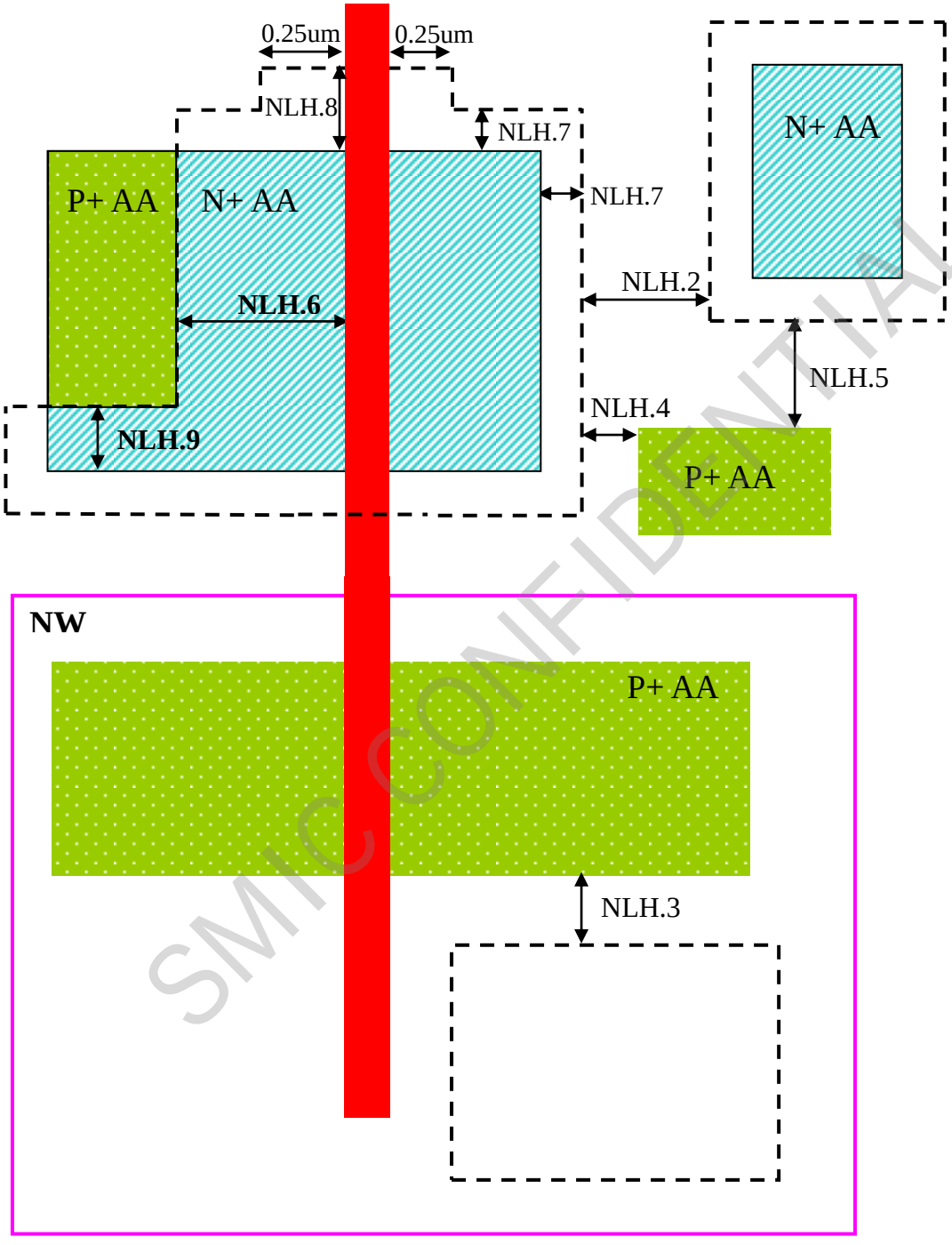
7.2.12 PLL: 1.2V/1.5V PLDD implantation design

Rules number	Description	Operation	Design Value	Unit
PLL.1	PLL width	≥	0.30	um
PLL.2	Space between PLLs	≥	0.30	um
PLL.3	Space between PLL and N+ AA inside P well	≥	0.16	um
PLL.4	Space between PLL and N+ AA inside N well	≥	0.03	um
PLL.4b	Space between a PLL and a butted N+ AA	=	0	um
PLL.5	Space between PLL and AA with PLH, NLL or NLH implantation	≥	0.16	um
PLL.6	PLL extension outside of PMOS poly gate along source/drain direction	≥	0.40	um
PLL.7	PLL extension outside of P+AA, if the distance to the related poly is larger than 0.25μm	≥	0.16	um
PLL.8	PLL extension outside of P+AA, if the distance to the related poly is less than 0.25μm	≥	0.30	um
PLL.9	PLL and AA overlap	≥	0.16	um
PLL.10	PLL area (um^2)	≥	0.23	μm^2
PLL.11[R]	Required PLL space when the PLL length ≥ 10um, and PLL is located between (Polys on STI) , which poly space ≤ 0.66um.	≥	0.30	um



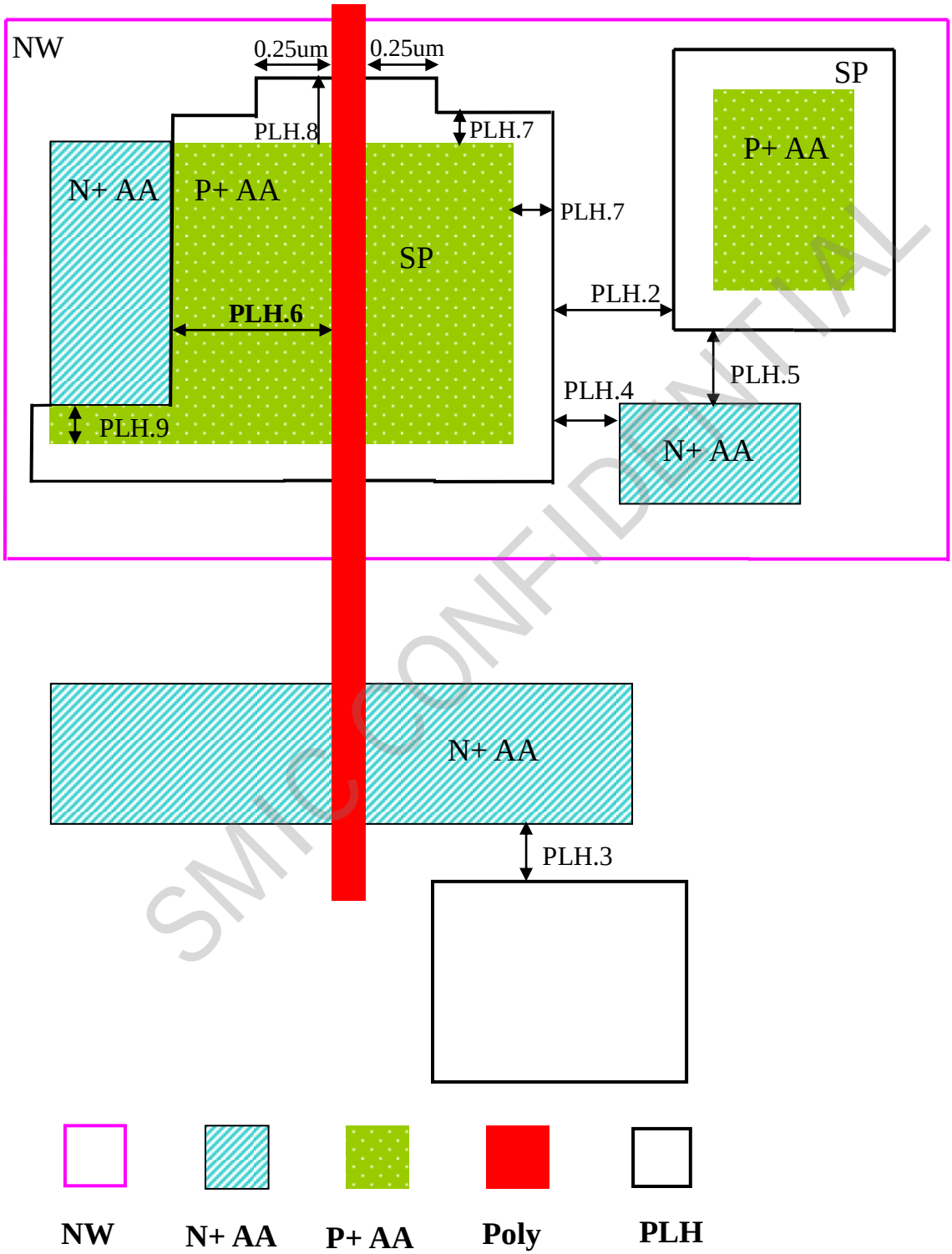
7.2.13 NLH: 2.5/3.3V NLDD implantation design

Rules number	Description	Operation	Design Value	Unit
NLH.1	NLH width	≥	0.30	um
NLH.2	Space between NLHs.	≥	0.30	um
NLH.3	Space between NLH and P+ AA inside NW	≥	0.16	um
NLH.4	Space between NLH and P+ AA inside PW	≥	0.03	um
NLH.4b	Space between a NLH and a butted P+ AA	=	0	um
NLH.5	Space between NLH and AA with NLL, PLL or PLH implantation	≥	0.16	um
NLH.6	NLH extension outside of NMOS poly gate along source/drain direction	≥	0.40	um
NLH.7	NLH extension outside of N+AA, if distance to the related poly is larger than 0.25um	≥	0.16	um
NLH.8	NLH extension outside of N+AA, if distance to the related poly is less than 0.25um	≥	0.30	um
NLH.9	NLH and AA overlap	≥	0.16	um
NLH.10	NLH area (um^2)	≥	0.23	μm^2



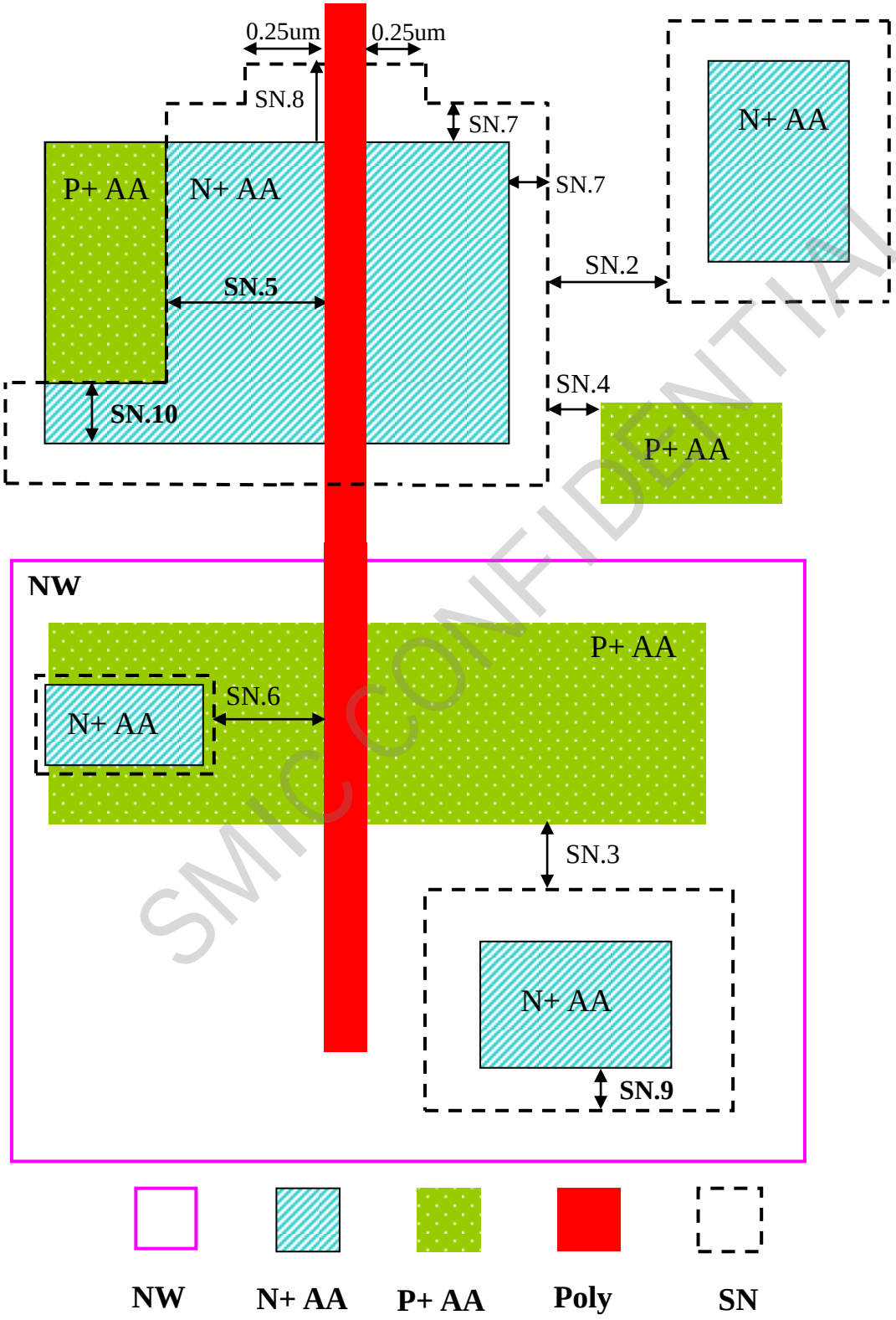
7.2.14 PLH: 2.5/3.3V PLDD implantation design

Rules number	Description	Operation	Design Value	Unit
PLH.1	PLH width	≥	0.30	um
PLH.2	Space between PLHs	≥	0.30	um
PLH.3	Space between PLH and N+ AA inside P well	≥	0.16	um
PLH.4	Space between PLH and N+ AA inside N well	≥	0.03	um
PLH.4b	Space between a PLH and a butted N+ AA	=	0	um
PLH.5	Space between PLH and AA with PLL, NLL or NLH implantation	≥	0.16	um
PLH.6	PLH extension outside of PMOS poly gate along source/drain direction	≥	0.40	um
PLH.7	PLH extension outside of P+AA, if the distance to the related poly is larger than 0.25um	≥	0.16	um
PLH.8	PLH extension outside of P+AA, if the distance to the related poly is less than 0.25um	≥	0.30	um
PLH.9	PLH and AA overlap	≥	0.16	um
PLH.10	PLH area (um^2)	≥	0.23	μm^2



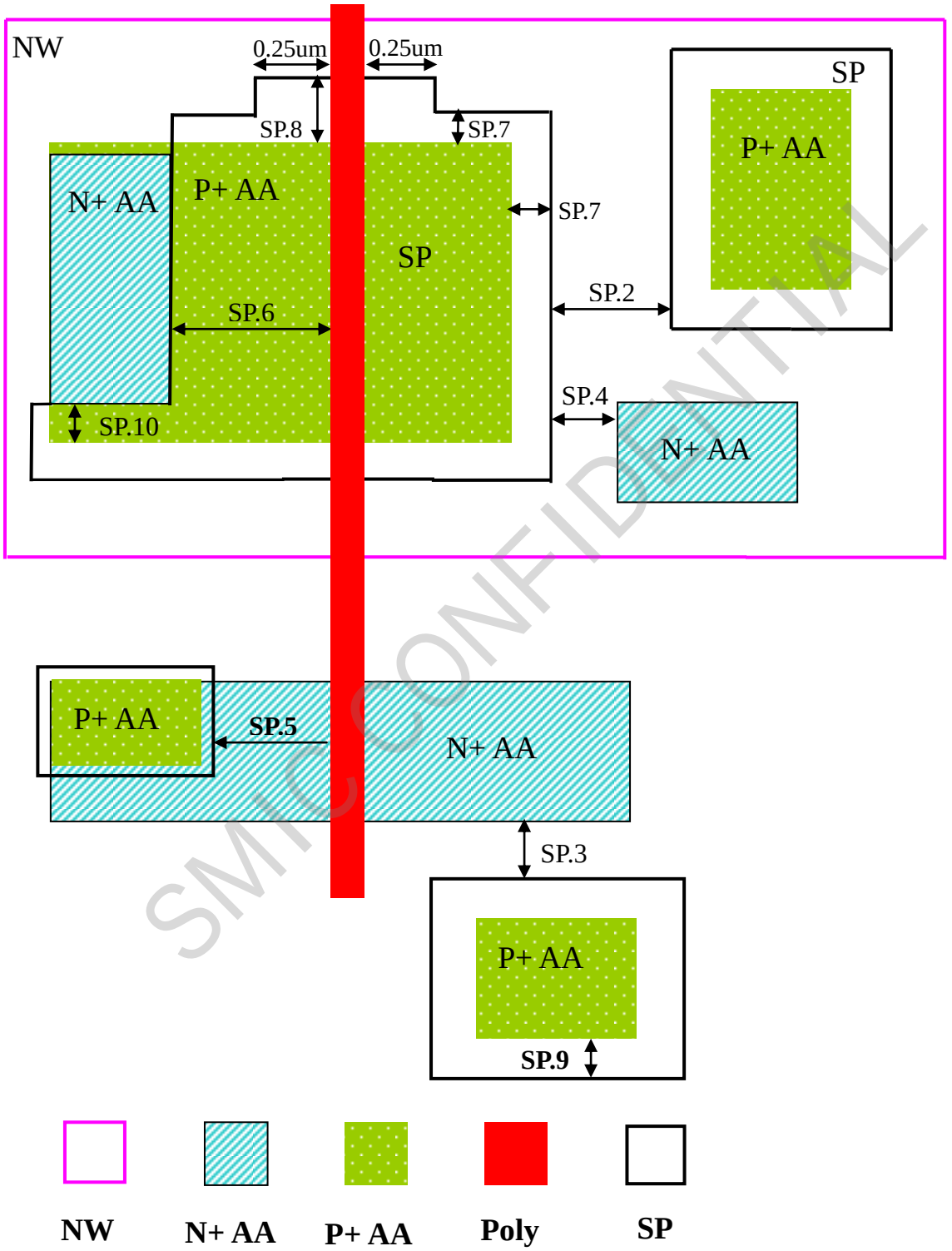
7.2.15 SN: N+ S/D implantation design

Rules number	Description	Operation	Design Value	Unit
SN.1	SN width, exclude (SN INTERACT OPCBA).	≥	0.30	um
SN.2	Space between SNs.	≥	0.30	um
SN.3	Space between SN and P+ AA inside NW, exclude SRAM region.	≥	0.16	um
SN.4	Space between SN and P+ pick-up AA inside PW	≥	0.03	um
SN.5	SN extension outside of Poly gate for NMOS, exclude SRAM region.	≥	0.40	um
SN.6	Space between SN and poly gate for PMOS, exclude SRAM region.	≥	0.40	um
SN.7	SN extension outside of N+AA, if the distance to the related poly is larger than 0.25um except NW resistor region, and SRAM region.	≥	0.16	um
SN.8	SN extension outside of N+AA , if the distance to the related poly is less than 0.25um except NW resistor region, and SRAM region.	≥	0.30	um
SN.9	N+AA enclosure by SN in NW and NWH exclude NW resistor region, and SRAM region.	≥	0.03	um
SN.10	SN and AA overlap, exclude SRAM region.	≥	0.16	um
SN.11	SN area (um^2)	≥	0.23	μm^2



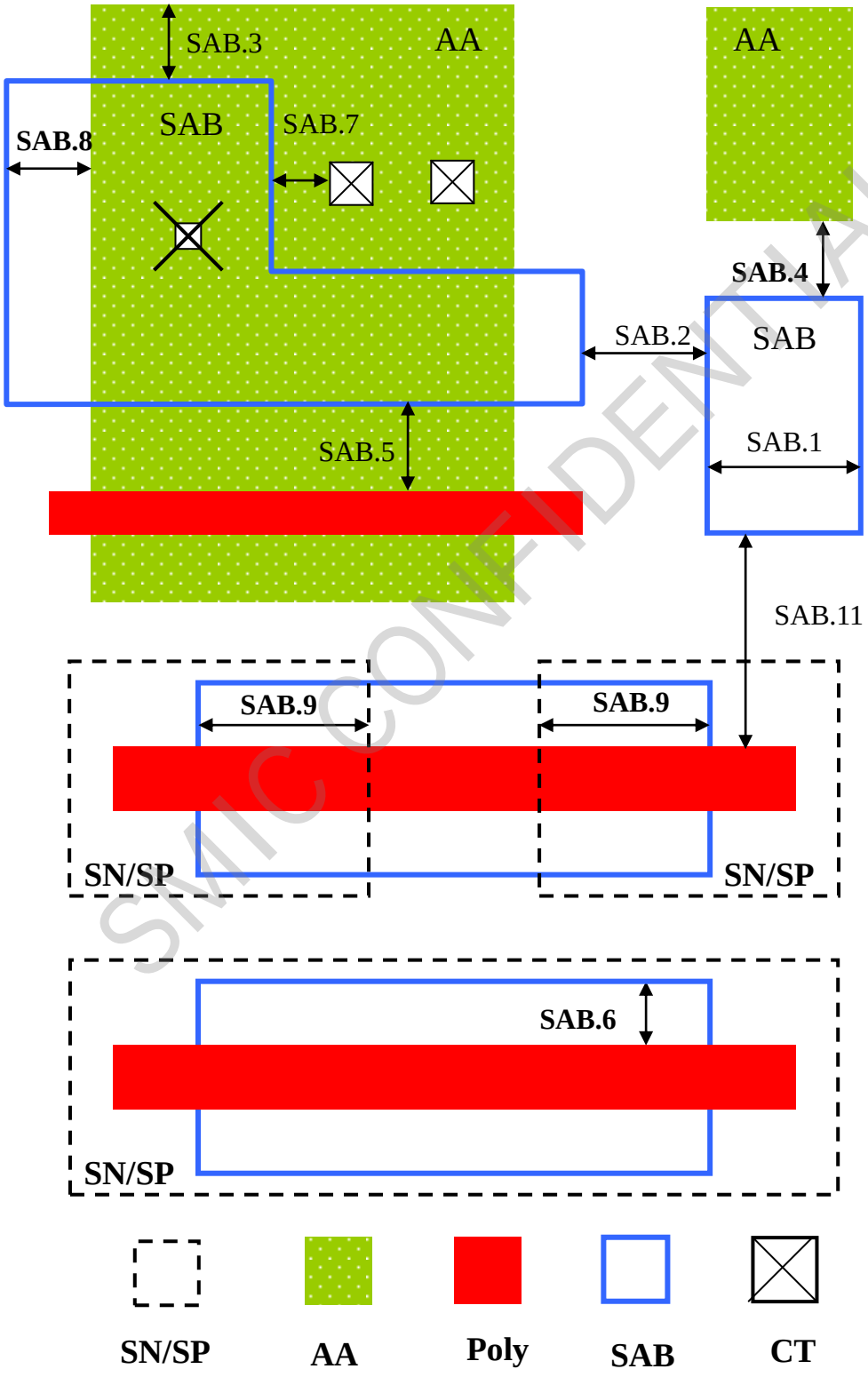
7.2.16 SP: P+ S/D implantation design

Rules number	Description	Operation	Design Value	Unit
SP.1	SP width, exclude SRAM region.	≥	0.30	um
SP.2	Space between SPs.	≥	0.30	um
SP.3	Space between SP and N+ AA inside P well, exclude SRAM region.	≥	0.16	um
SP.4	Space between SP and N+ AA inside N well, exclude SRAM region.	≥	0.03	um
SP.5	Space between SP and N-channel poly gate, exclude SRAM region.	≥	0.40	um
SP.6	SP extension outside of PMOS poly gate, exclude SRAM region.	≥	0.40	um
SP.7	SP extension outside of P+AA, if the distance to the related poly is larger than 0.25μm, exclude SRAM region.	≥	0.16	um
SP.8	SP extension outside of P+AA, if the distance to the related poly is less than 0.25μm, exclude SRAM region.	≥	0.30	um
SP.9	P+ AA enclosure by SP in PW	≥	0.03	um
SP.10	SP and AA overlap, exclude (SP INTERACT OPCBA).	≥	0.18	um
SP.11	SP area (um^2)	≥	0.23	μm^2
SP.12	No SP and SN overlap is allowed			
SP.13[NC]	SP cannot be generated by the reverse tone of SN.			



7.2.17 SAB: Salicide Block design

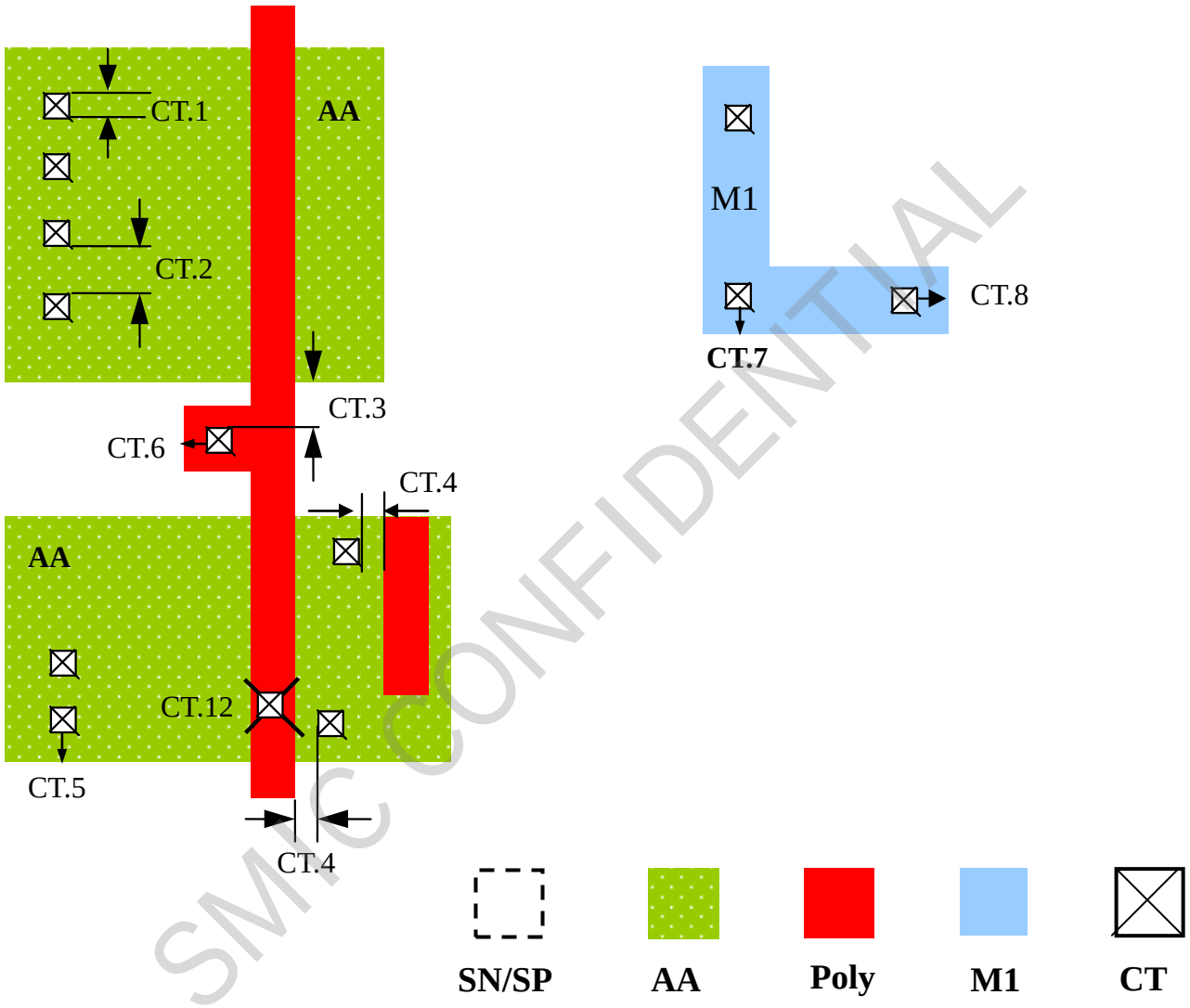
Rules number	Description	Operation	Design Value	Unit
SAB.1	SAB width	≥	0.42	um
SAB.2	Space between SABs	≥	0.42	um
SAB.2a	Space between SABs on poly. (DRC only checks the space when the space region interacted with poly).	≥	0.45	um
SAB.3	Extension of related AA outside of SAB	≥	0.20	um
SAB.4	Space between SAB and AA	≥	0.20	um
SAB.5	Space between SAB and GT on AA	≥	0.36	um
SAB.6	Extension of SAB outside of poly on field oxide	≥	0.20	um
SAB.7	Space between SAB and CT	≥	0.20	um
SAB.8	Extension of SAB outside of AA	≥	0.20	um
SAB.9	SAB overlap with SN or SP	≥	0.28	um
SAB.10	SAB area (um^2)	≥	1.0	μm^2
SAB.10a[R]	SAB enclosed area (um^2)	≥	1.0	μm^2
SAB.11	Space between SAB and poly on field oxide.	≥	0.28	um



7.2.18 CT: Contact design

Rules number	Description	Operation	Design Value	Unit
CT.1	Fixed contact size (edge of a square via) , exclude SRAM region.	=	0.16	um
CT.2	Space between contacts	≥	0.18	um
CT.3	Space between AA and contact on poly, exclude SRAM region.	≥	0.12	um
CT.4a	Space between poly and contact on AA for 1.2V, and 1.5V, exclude SRAM region.	≥	0.11	um
CT.4b	Space between poly and contact on AA for 3.3v	≥	0.13	um
CT.4c	Space between poly and contact on AA for 2.5V	≥	0.11	um
CT.5	CT enclosure by AA for CT landed on device AA, exclude SRAM region.	≥	0.06	um
CT.5a	CT enclosure by AA for CT landed on pickup AA	≥	0.05	um
CT.6	CT enclosure by poly for CT landed on poly, exclude SRAM region.	≥	0.06	um
CT.7	CT enclosure by M1, exclude SRAM region.	≥	0.00	um
CT.8	M1 line end extension outside of CT, exclude SRAM region.	≥	0.05	um
CT.9	CT is not allowed to land on gate, exclude INDMY (212;0) covered regions and SRAM region.			
CT.10	CT can not overlap with SAB layer or (STI NOT GT) region, exclude SRAM region.			
CT.11	CT must be fully covered by M1 and (AA OR GT)			
CT.12	It's not allowed CT overlap with NW, AA, Poly or M1 resistor. For NW, AA, Poly resistor, please refer each resistor section definition.			

	M1 resistor definition: (M1 AND M1R).			

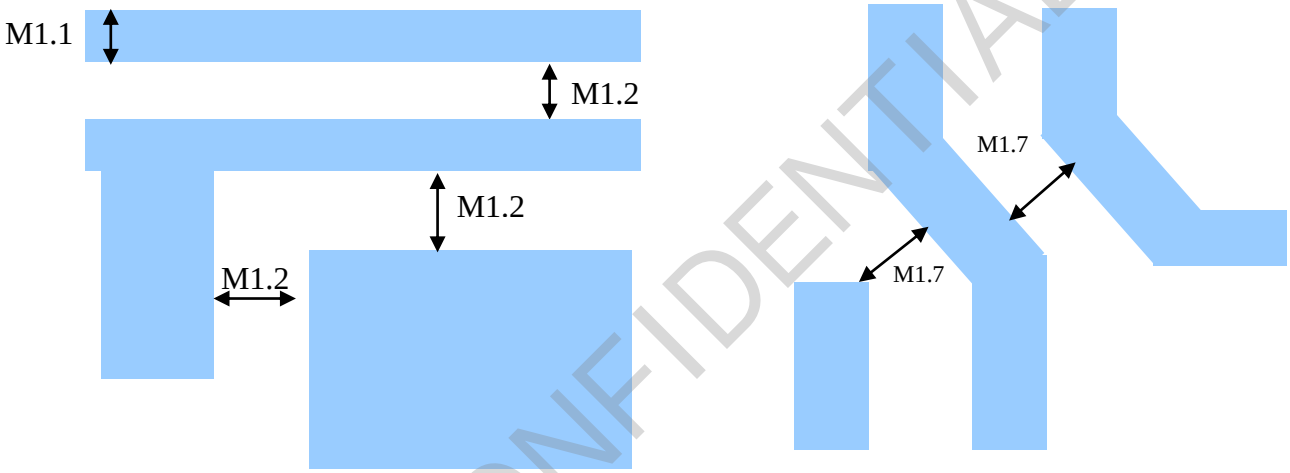


7.2.19 M1: Metal 1 design

Rules number	Description	Operation	Design Value	Unit
M1.1	M1 width, exclude SRAM region.	≥	0.16	um
M1.2	Space between M1s, exclude SRAM region.	≥	0.17	um
M1.3a[R]	Suggested space between M1s with one or both M1 width greater than 0.4um when run length > 1um.	≥	0.20	um
M1.3b[R]	Suggested space between M1s with one or both M1 width greater than 2um	≥	0.40	um
M1.3c	Space between M1s with one or both M1 width greater than 10um	≥	0.50	um
M1.4	M1 area (um^2)	≥	0.08	μm^2
M1.5	Dielectric area enclosed by M1 (um^2)	≥	0.17	μm^2
M1.6	Dummy pattern is required in case M1 density is less than 16%. See metal dummy rule in section 7.2.38.3. Density check window size is 200x200 µm, step 100um.	≥	16%	
		≤	82%	
M1.7	Space between metal line and 45 degree bent metal line that are longer than 0.5um	≥	0.20	um
M1.8	Maximum line width allowed. Metal slot rule will apply for a metal with line width greater than this value. DRC skip to check (M1 interact with PA pattern).	≤	14.00	um
M1.9[NC]	CT or Via should be enclosed by M1 as large as layout allowed.			

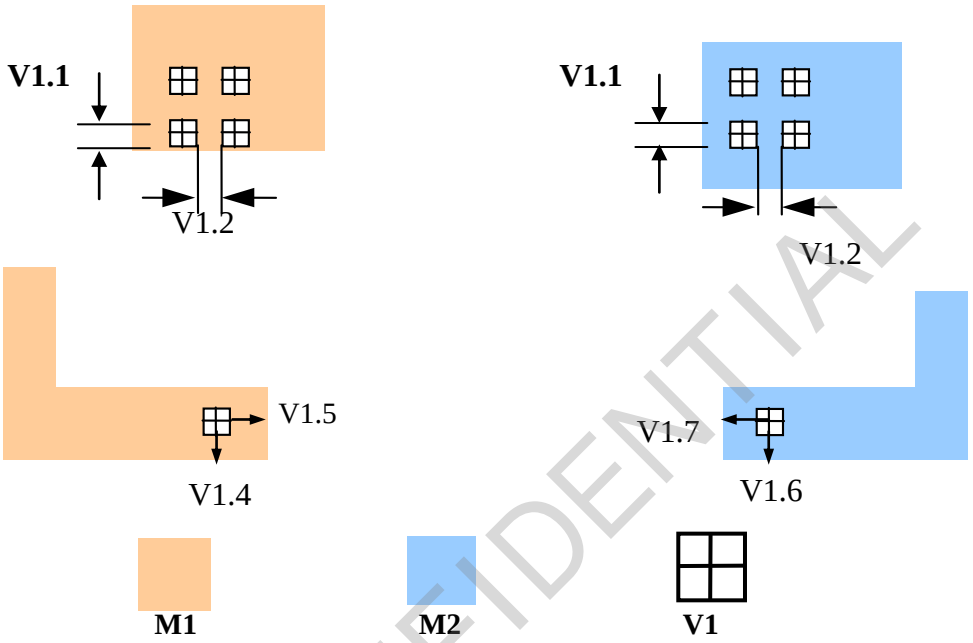
Note:

1. Recommend that the length of metal lines is orthogonal to the length of metal lines on neighboring layers.
2. DUMBM layer is used to block metal dummy layers from placing on the area. DUMBM blocks dummy pattern on every metal layer.



7.2.20 V1: Via1 design

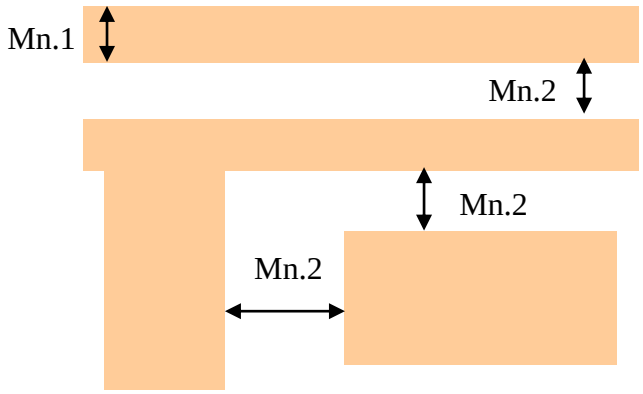
Rules number	Description	Operation	Design Value	Unit
V1.1	Fixed V1 size (square shape) (except FUSE protection ring region).	=	0.19	um
V1.2a	Space between V1s	≥	0.21	um
V1.2b	Space between V1s within array greater or equal to 4x4; Two via regions whose space is ≤0.27um are considered to be in the same array	≥	0.25	um
V1.4	V1 enclosure by M1, exclude SRAM region.	≥	0.005	um
V1.5	Extension of M1 line end outside of V1, exclude SRAM region.	≥	0.05	um
V1.6	V1 enclosure by M2, exclude SRAM region.	≥	0.005	um
V1.7	Extension of M2 line end outside of V1, exclude SRAM region.	≥	0.03	um
V1.8	For V1 enclosed at the 90 degree corner by M1, M1 extension at least along one direction outside V1, exclude SRAM region.	≥	0.05	um
V1.9	For V1 enclosed at the 90 degree corner by M2, M2 extension at least along one direction outside V1, exclude SRAM region.	≥	0.03	um
V1.10	V1 must be enclosed by both M1 and M2			
V1.11[R]	Via redundancy is recommended wherever layout allows. When either or both M1 and M2 width >0.9um there should be two V1s.			
V1.12	It's not allowed V1 overlap with M1 or M2 resistor. M1 resistor definition: (M1 AND M1R). M2 resistor definition: (M2 AND M2R).			

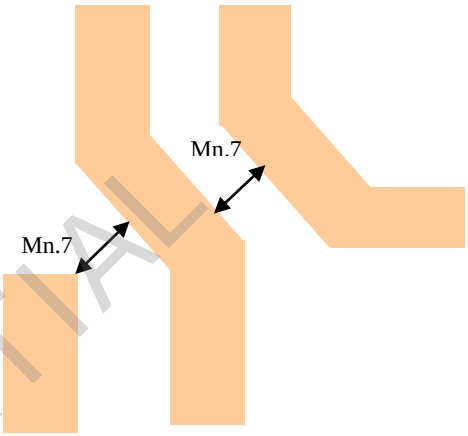


7.2.21 Mn: Metal n (n=2,3,4,5,6,7) design

Rules number	Description	Operation	Design Value	Unit
Mn.1	Mn width	≥	0.20	um
Mn.2	Space between Mns, exclude SRAM region.	≥	0.20	um
Mn.3a[R]	Suggested space between Mns with one or both Mn width greater than 0.4um when run length > 1um.	≥	0.25	um
Mn.3b[R]	Suggested space between Mns with one or both Mn width greater than 2um	≥	0.40	um
Mn.3c	Space between Mns with one or both Mn width greater than 10um.	≥	0.50	um
Mn.4	Mn area (in um^2)	≥	0.12	μm^2
Mn.5	Dielectric area enclosed by Mn (um^2)	≥	0.26	μm^2
Mn.6	Dummy pattern is required in case Mn density is less than 16%. Density check window size is 200x200 μm, step 100um.	≥	16%	
		≤	82%	
Mn.7	Space between metal line and 45 degree bent metal line that are longer than 0.5um	≥	0.22	um
Mn.8	Maximum line width. Metal line greater than this width will comply metal slot design rule (DRC waive: Mn interact with PA pattern, (TM-1 AND DUPMK1) region for one top metal design, MIM bottom plate and MIM shield under MIM design).	≤	15.00	um
Mn.9[NC]	Via should be enclosed by Mn as large as layout allowed.			

Note:
1. Recommend that the length of metal lines is orthogonal to the length of metal lines on neighboring layers.
2. DUMBM layer is used to block metal dummy layers from placing on the area. DUMBM blocks dummy pattern on every metal layer.





7.2.22 Vn: Via n (n=2,3,4,5,6) design

Rules number	Description	Operation	Design Value	Unit
Vn.1	Fixed Vn size (square shape) (except FUSE protection ring region , andSRAM region).	=	0.19	um
Vn.2a	Space between Vns	≥	0.21	um
Vn.2b	Minimum space between Vns within array greater or equal to 4x4; Two via regions whose space is ≤0.27um are considered to be in the same array	≥	0.25	um
Vn.3	Vn enclosure by Mn, exclude SRAM region.	≥	0.005	um
Vn.4	Extension of Mn line end outside of Vn, exclude SRAM region.	≥	0.05	um
Vn.5	Vn enclosure by Mn+1	≥	0.005	um
Vn.6	Extension of Mn+1 line end outside of Vn	≥	0.03	um
Vn.7	For Vn enclosed at the 90 degree corner by Mn, Mn extension at least along one direction outside a V1, exclude SRAM region.	≥	0.05	um
Vn.8	For Vn enclosed at the 90 degree corner by M n+1, M n+1 extension at least along one direction outside a V1	≥	0.03	um
Vn.10[R]	Via redundancy is recommended wherever layout allows. When either or both Mn and Mn+1 width >0.9um there should be two Vns.			
Vn.11	Vn must be enclosed by both Mn(or P2 in MIMDMY) and Mn+1.			
Vn.12	It's not allowed V_n overlap with M_n or M_{n+1} resistor. M_n resistor definition: (M_n AND M_nR). M_{n+1} resistor definition: (M_{n+1} AND $M_{n+1}R$).			

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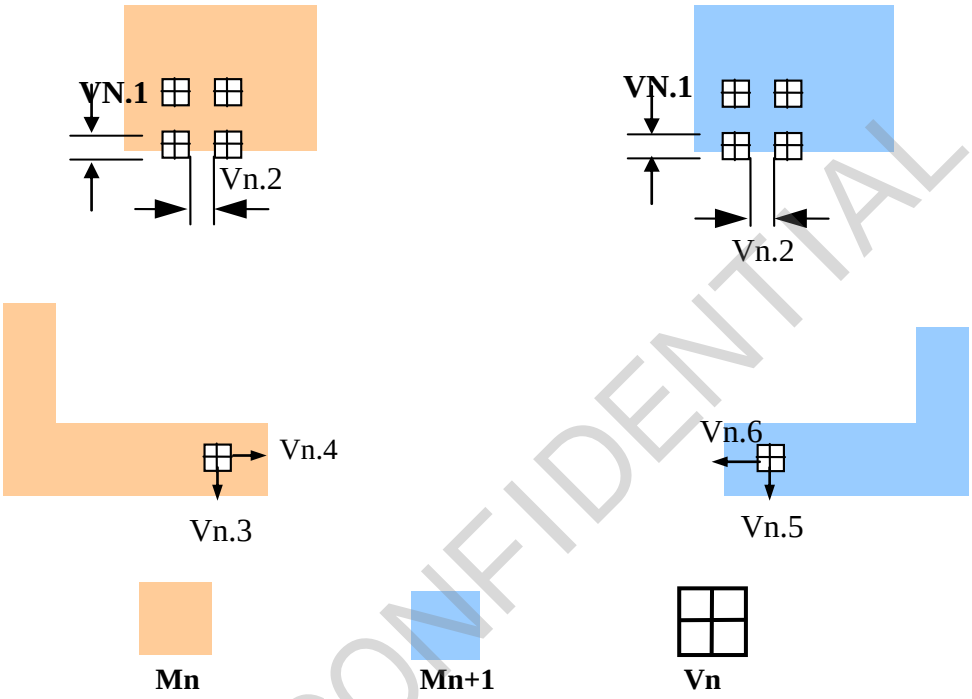
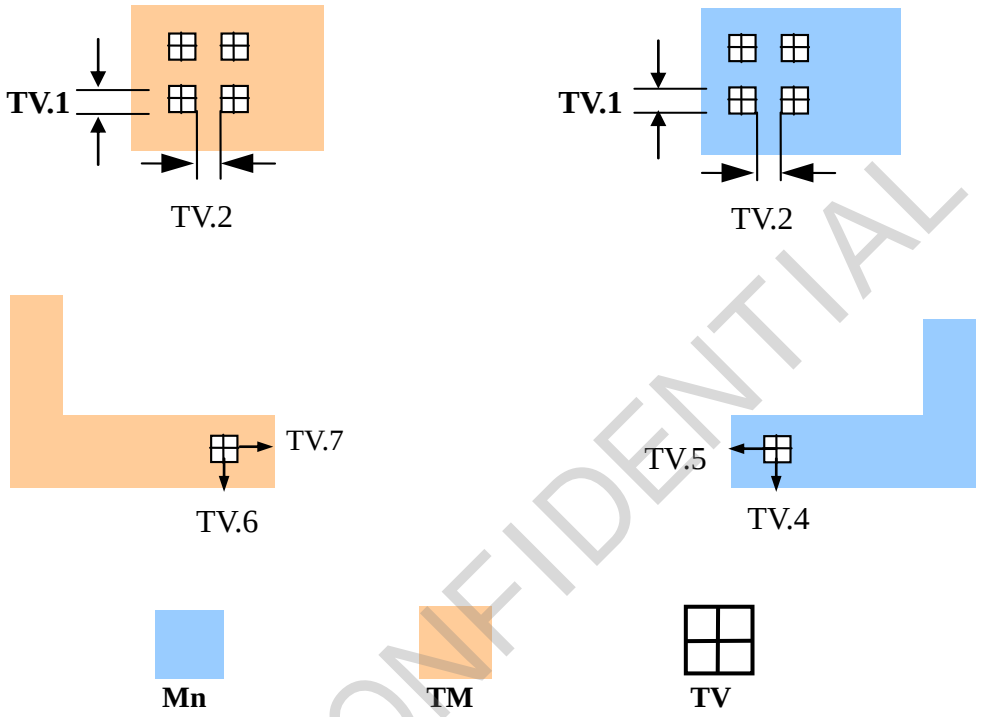


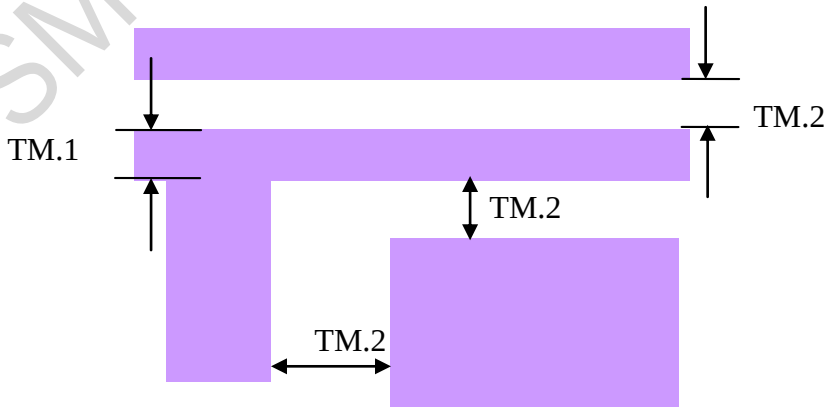
7.2.23 TVn (n=1,2): Top Via design

Rules number	Description	Operation	Design Value	Unit
TV.1	Fixed TV size (square) (except FUSE protection ring region).	=	0.36	um
TV.2a	Space between TVs	≥	0.34	um
TV.2b	Space between TVs within array greater or equal to 3x3; Two via regions whose space is ≤ 0.52um are considered to be in the same array	≥	0.50	um
TV.4	TV enclosure by metal layer directly underneath TV	≥	0.01	um
TV.5	Extension of Mn line end outside of TV. Mn is a metal layer directly underneath TV.	≥	0.05	um
TV.6	TV enclosure by TM.	≥	0.03	um
TV.7	Extension of TM line end outside of TV.	≥	0.07	um
TV.10	TV must be enclosed by directly above metal layer, and underneath metal layer or P2.			
TV.11	For TV1: It's not allowed TV1 overlap with Mn or TM1 resistor. Mn resistor definition: (Mn AND MnR). TM1 resistor definition: (TM1 AND TM1R). For TV2: It's not allowed TV2 overlap with Mn/TM1 resistor when Mn/TM1 directly underneath TV2. And It's not allowed TV2 overlap with TM2/MTT* resistor when TM2/MTT* directly above TV2. Mn resistor definition: (Mn AND MnR). TM1 resistor definition: (TM1 AND TM1R). TM2 resistor definition: (TM2 AND TM2R). MTT* resistor definition: (MTT* AND TM2R) (The MTT* resistor layer name depends on each Tech. node definition)			



7.2.24 TMn (n=1,2): Top Metal design

Rules number	Description	Operation	Design Value	Unit
TM.1	TM width	≥	0.42	um
TM.2	Space between TMs.	≥	0.42	um
TM.4	Space between TMs with one or both width greater than 2um	≥	0.50	um
TM.5	TM area (in um^2)	≥	0.42	um^2
TM.6	Dielectric area enclosed by TM	≥	1.00	um^2
TM.7	Dummy pattern is recommended in case Metal density is less than 16%. Density check window size is 200x200 μm, step 100um.	≥	16%	
		≤	82%	
TM.8	Width that does not require metal slots (exclude DUPMK1 region and TM interact with PA pattern).	≤	30.00	um
TM.9[G]	It is forbidden that designers use both TM1/TM2 GDS and inter metal GDS for top metal layout in one chip at the same time. DRC checking should cover metal layer ALL corresponding GDS layer/data type, include metal main pattern, metal dummy pattern and metal slot pattern.			



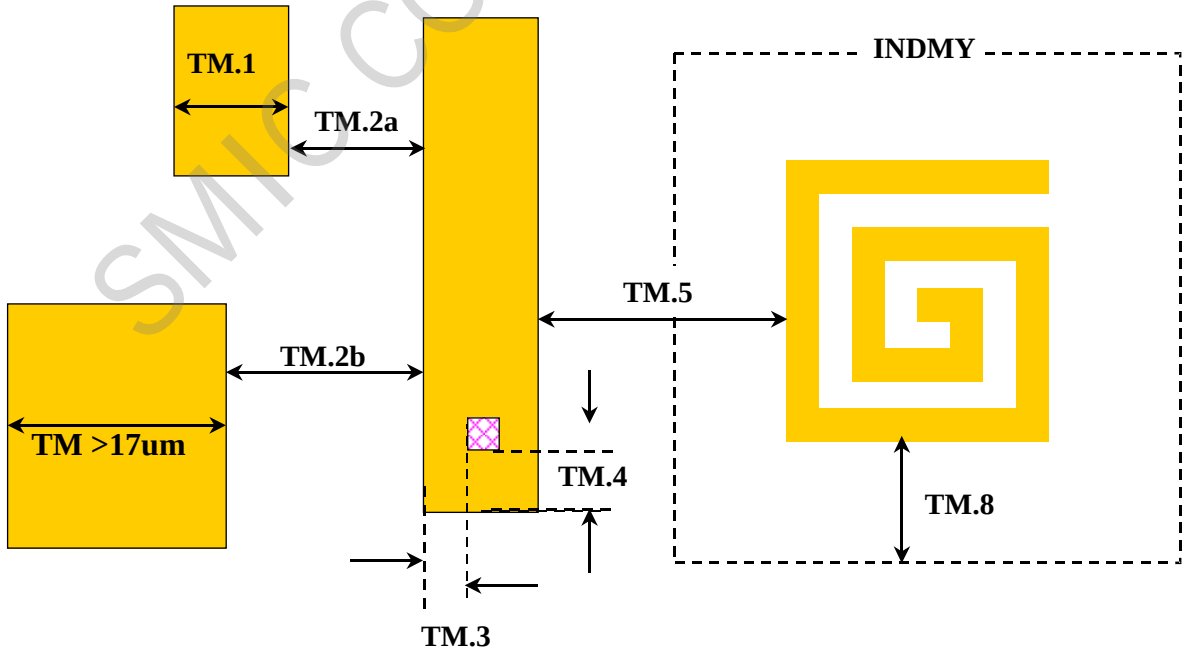
7.2.25 MTT design (for Thick Top Metal process)

For TM, RF customers can choose logic standard top metal process or MS&RF thick top metal process based on special necessity. If choose logic standard top metal process, TM layout will follow 0.13um logic design rules, and please skip below chapter. If choose thick top metal, please follow below rules to define MTT instead of logic TM design rule.

Rule number	Description	Operation	Design Value	Unit
MTT.1	MTT width, exclude SRAM region. DRC waive check between 86 to 90 degree angel widths in the INDMY covered region.	≥	1.50	μm
MTT.1a	MTT max. width that is not required metal slot (exclude DUPMK1 region and (MTT AND PA) pattern).	≤	30	μm
MTT.2a	Space between MTTs, exclude SRAM region. (DRC allows 0.007um checking tolerance in INDMY).	≥	1.50	μm
MTT.2b	Space between MTTs with one or both TM width larger than 17um.	≥	3.00	μm
MTT.3	MTT region extension outside of top Via, exclude SRAM region.	≥	0.30	μm
MTT.4	MTT region extension outside of top Via at the end of MTT, exclude SRAM region.	≥	0.42	μm
MTT.5	Space from MTT used as Inductor to other MTT region when projected run length>0. Inductor MTT definition: (INDMY AND MTT) DRC doesn't check the space under the same INDMY region. DRC doesn't check if the Inductor MTT is connected with other MTT through Mn(n=1~7)/TMn(n=1~2)/ALPA conductor layers..	≥	30	μm
MTT.6	MTT area	≥	2.25	μm^2
MTT.6a	Enclosed dielectric area by MTTs	≥	1.00	μm^2
MTT.7	MTT area density.	≥	30%	
MTT.7a[R] [NC]	Dummy MTT pattern suggested 2 X 5um with line space 2.0um is required if density less than 30%			
MTT.7b	MTT max. pattern density on the whole chip (including	≤	80%	

	dummy patterns)			
MTT.8	Dummy layer "INDMY" extension outside of MTT region used as Inductor	≥	30	μm
MTT.9	Both active and passive devices inside Inductor region are not allowed			
MTT.10[NC]	Via and metal layers inside "INDMY" is not allowed except Inductor connection			
MTT.11[G]	It is forbidden that designers use both TM1/TM2 GDS and inter metal GDS for top metal layout in one chip at the same time. DRC checking should cover metal layer ALL corresponding GDS layer/data type, include metal main pattern, metal dummy pattern and metal slot pattern.			

Note:
Recommend customers to follow SMIC dummy insertion rules for metal density uniformity improvement. SMIC agrees to waive density violations for below three cases: 1) still violates low density rules even after SMIC dummy insertion (no blockage layer exists); 2) Original gds file does not violate high density rules, but has some high density violations after SMIC dummy insertion.

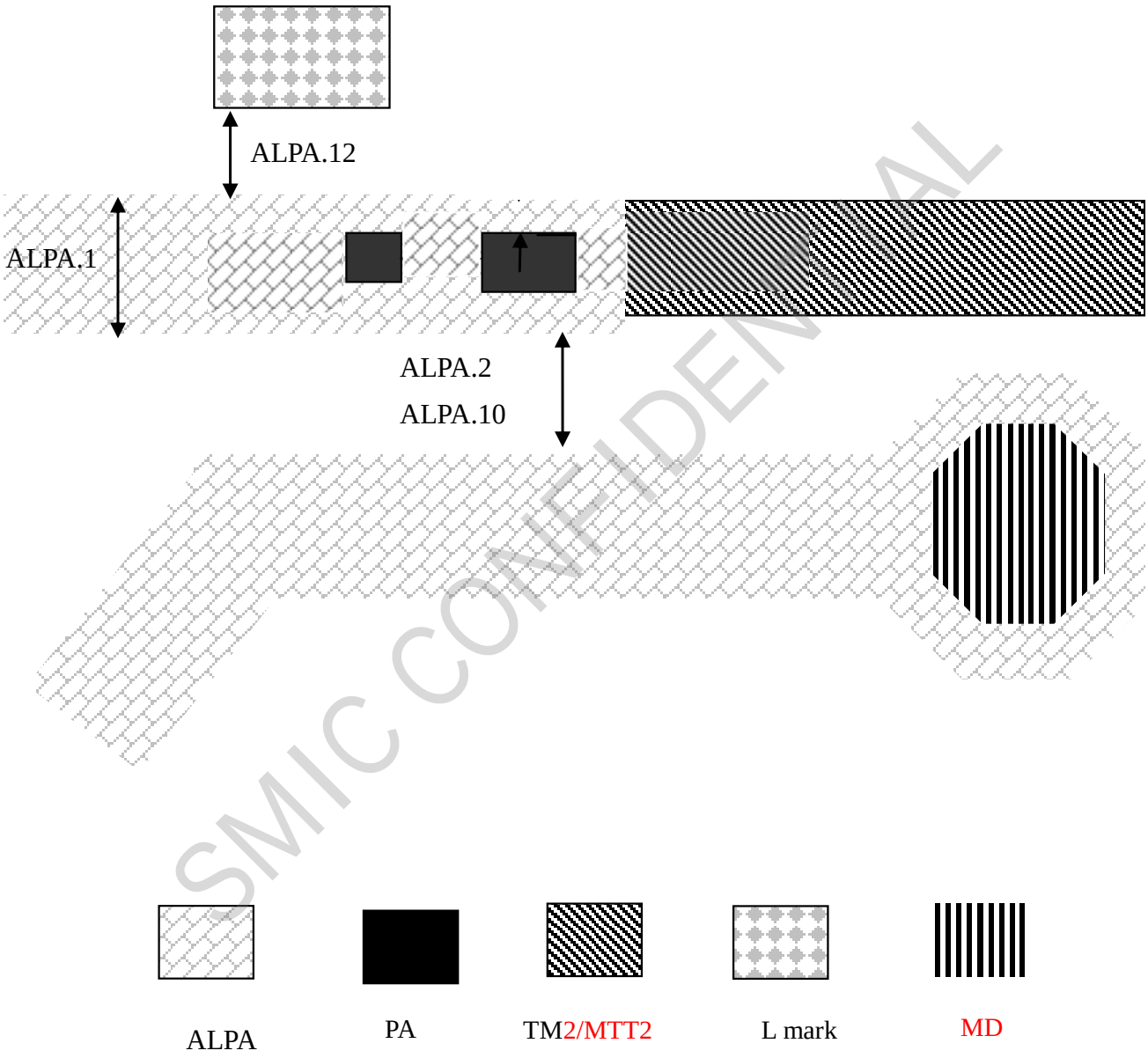


7.2.26 ALPA design

ALPA (83;0) layer can be used to draw AL bump pads, RDL (redistribution layer), etc.

1. ALPA layout includes Al bump Pad and RDL.
2. RDL is defined as ALPA layer width equal or smaller than 35μm.
3. Al bump Pad is defined as ALPA layer width larger than 35μm and interact with PA (PA width> 32um).

Rules number	Description	Operation	Design Value	Unit
ALPA.1	ALPA Width	≥	3.00	um
ALPA.2	Space between two ALPAs	≥	3.00	um
ALPA.3	(purposely blank)			
ALPA.4	(purposely blank)			
ALPA.5	(purposely blank)			
ALPA.6	(purposely blank)			
ALPA.7	(purposely blank)			
ALPA.8	(purposely blank)			
ALPA.9	(purposely blank)			
ALPA.10a	Space between RDL and Al bump pad, exclude (RDL interact Al bump pad)	≥	10.0	um
ALPA.10b	Space between RDL and PA (PA width >32um) , exclude (RDL interact Al bump pad)	≥	11.5	um
ALPA.11	Space between RDL and FUSE window	≥	10.0	um
ALPA.12	Space between RDL and L mark window	≥	10.0	um
ALPA.13	Al bump pad to Fuse window space	≥	50.0	um
ALPA.14	Pattern density of ALPA layer should be between 0~50%			
ALPA.15[NC]	If using ALPA to redistribute Al bump pad, MD (PA2) layer is must.			

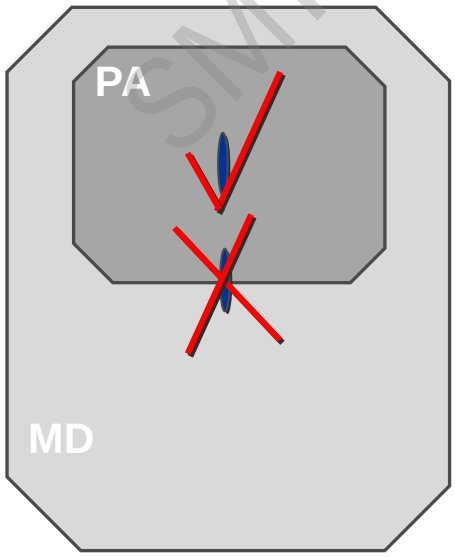


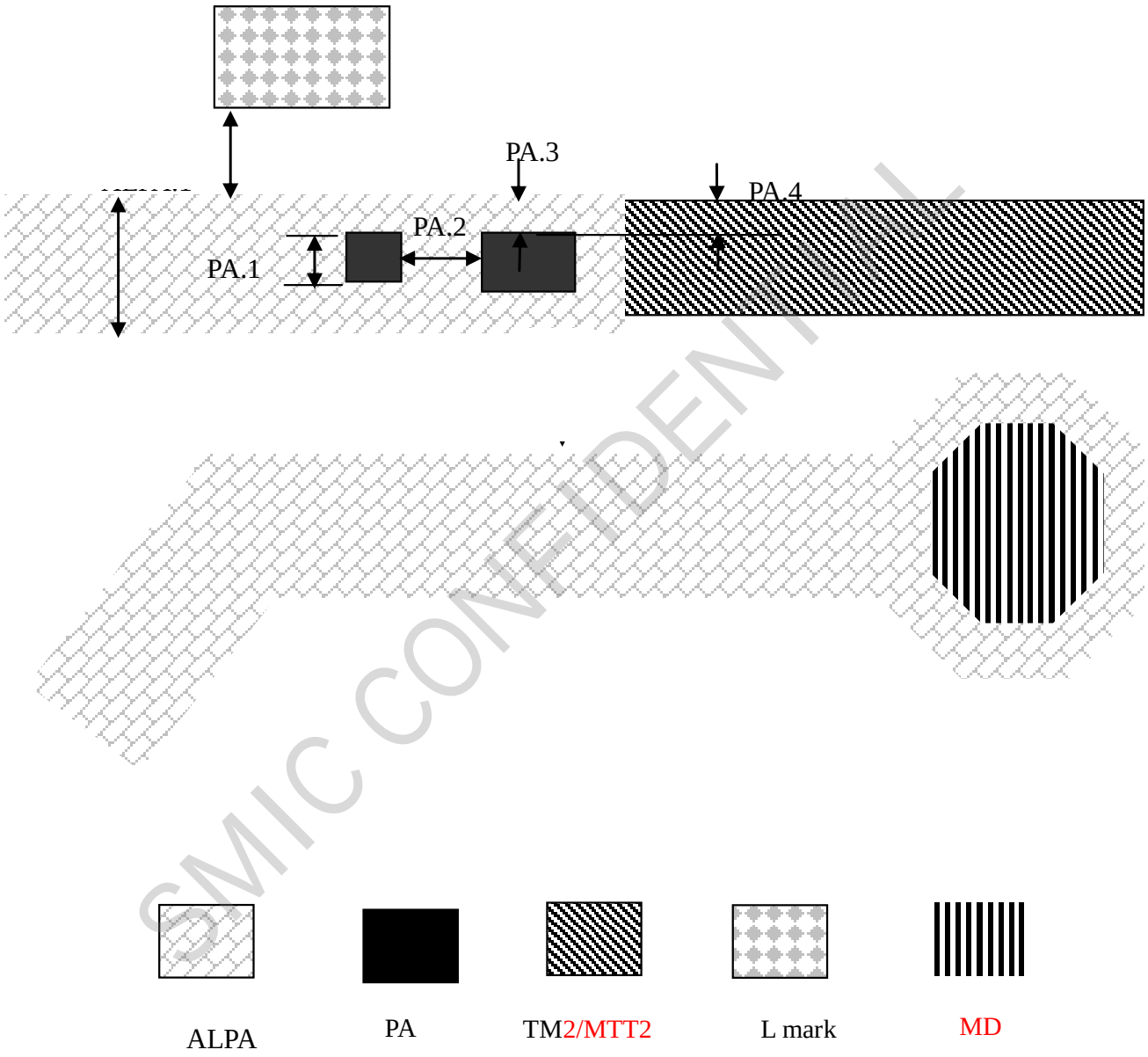
7.2.27 PA: Passivation-1 design

PA (81;0) layer can be used to design PA pad (≥ 40um) or PA for connection (=4um) for RDL application.

Rule number	Description	Operation	Rule Value	Unit
PA.1a	PA size for RDL connection, excluding PA pad.	=	4.0	um
PA.1b[G]	PA size for pad	≥	40.0	um
PA.2a	Space between two PAs when both PA size < 10um.	≥	4.0	um
PA.2b	Space between two PAs when one or both PA size ≥ 10um.	≥	7.0	um
PA.3	PA enclosed by ALPA, only check PA interact with ALPA/ALRDL pattern.	≥	1.5	um
PA.4	PA enclosed by top metal	≥	1.5	um
PA.5	ALPA must interact with PA(except ALPA resistor). DRC waive check the ALPA interact with ALPAR and DRC waive ALMK1 covered region (The ALMK1 layer must be drawn identically to dummy purpose ALPA).			
PA.6	No PA pad design (PA size ≥40um) is not allowed.			

Note:
Suggest putting probe card making at PA layer center. Probe card mark straddles on PA boundary design may cause test issue.





7.2.28 MD: MD design rule

If there is no RDL designs, please skip this section directly, MD layer can be auto generated with logic operation formula when tape out.

If designs have RDL applications for either Al bump pad redistribution or metal routing purpose, designers can refer to below MD design guidelines to draw/generate MD layout.

MD opening on Al bump pad can be generated with PA layout, while the MD opening on RDL need be drawn by designer. The final MD layout should pass DRC checking in below table.

The final MD layout on mask can be generated with below logic operation formula, which is applicable when designers follow SMIC design rule (PA hole size is = 4um). If designer doesn't follow SMIC design rule to design the PA hole, please consult with SMIC process integration engineers.

MD = (((PA sd 2.5) su 2.5) + MD)

Rule number	Description	Operation	Rule Value	Unit
MD.1	MD size	≥	4.0	um
MD.2[G]	Guideline for the MD dimension. Generally, It is designers' responsibility to early consult the assembly house for additional constraints according to their wafer sort and assembly capabilities, and take these additional constraints into consideration during layout.	≥	40.0	um
MD.3	Space between two MDs	≥	4.0	um
MD.4	Space between two MDs when one or both MD size ≥ 10um	≥	7.0	um
MD.5	Space between MD to PA, if MD not interact with PA.	≥	6.0	um
MD.6	MD must be fully enclosed by Al bump pad ((PA su 1.5) + ALPA) DRC allows 0.001um checking tolerance.	≥	1.5	um
MD.7	MD is not allowed to overlap with PA for RDL connection (size = 4um)			
MD.8[G][NC]	Guideline for the MD space. Generally, It is designers' responsibility to early consult the assembly house for additional constraints according to their wafer sort and assembly capabilities, and take these additional constraints into consideration during layout.			
MD.9[G][NC]	If designer has RDL application for Al bump pad redistribution which is drawn on ALPA layer, MD (PA2) layer is must.			

7.2.29 NW/AA/Poly Resistor rules

7.2.29.1 NW resistor rule

RESNW is the marker layer for NW resistor. NW resistor must be within RESNW marker layer.
RESNW layer is to define the NW resistor area where no other implantations except for NW.
NW resistor should have SAB layer on top except the contact region.
NW resistor under STI is allowed.

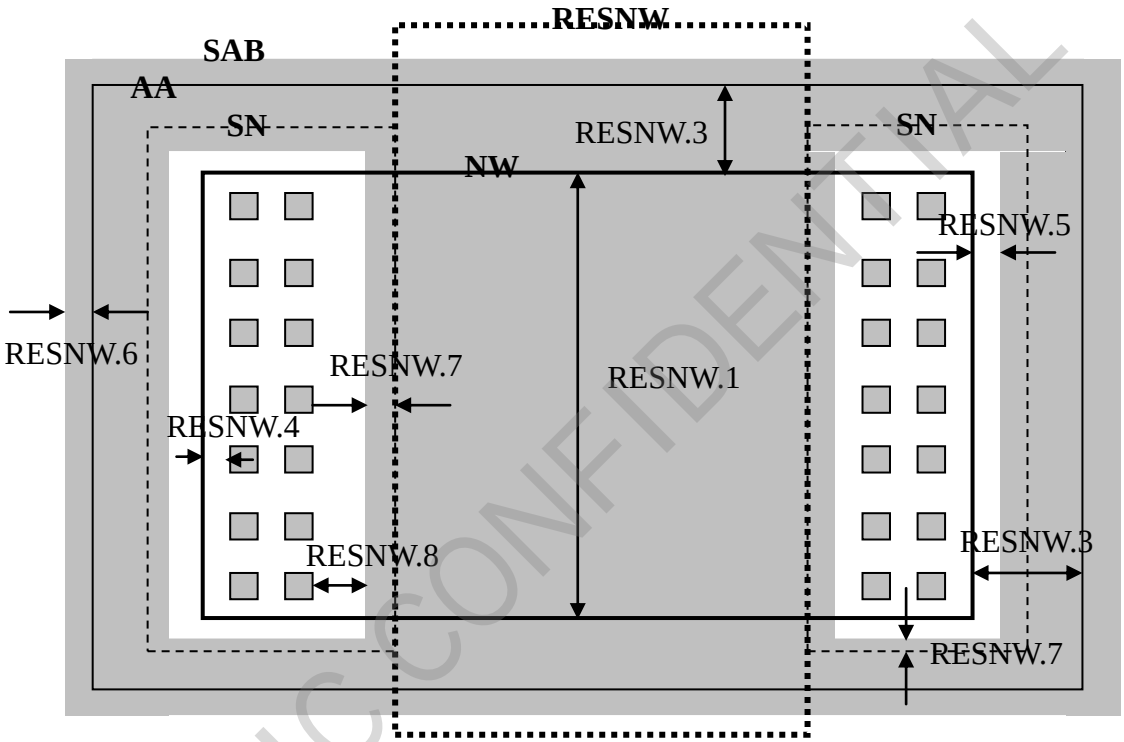
NW resistor region:

* NW resistor under AA: (((RESNW AND AA) AND NW) AND SAB)
* NW resistor under STI: ((RESNW AND NW) NOT INTERACT SAB)

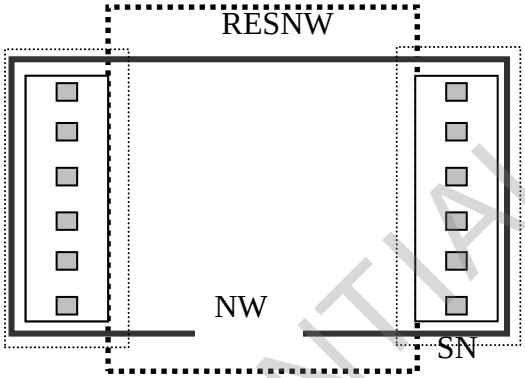
Rules number	Description	Operation	Design Value	Unit
RESNW.1	NW resistor width	≥	1.60	um
RESNW.2	NW space	≥	1.20	um
RESNW.3[R]	Enclosure of an AA beyond a NW	≥	1.00	um
RESNW.4	Enclosure of a salicide NW beyond a CT	≥	0.30	um
RESNW.5	Space between SAB and related NW	≥	0.30	um
RESNW.6	Enclosure of a SAB beyond a related AA	≥	0.22	um
RESNW.7	For well resistor with AA , Overlap of a SN to SAB (SAB hole must be fully enclosed by SN)	≥	0.40	um
RESNW.8	Space between SAB and related CT in SAB hole	≥	0.30	um
RESNW.9[R]	LDD, SN or SP is not allowed in the NW resistor area. DRC only check the NW resistor under AA.			
RESNW.10	For NW resistor under STI, NW enclosure CT	≥	0.21	um
RESNW.11[R]	For NW resistor under STI, space between RESNW to salicide AA area	=	0	um

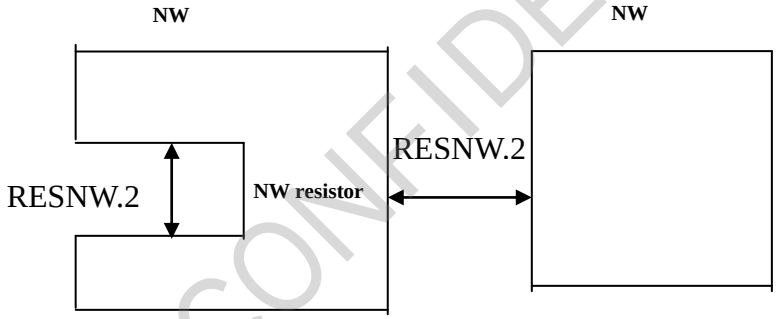
a. NW resistor under AA

* Use SAB to prevent the NW resistance region from forming salicide
* Use a RESNW layer to prevent LDD and SN/SP from penetrating into the NW resistor region



b. NW resistor under STI





7.2.29.2 AA resistor rule

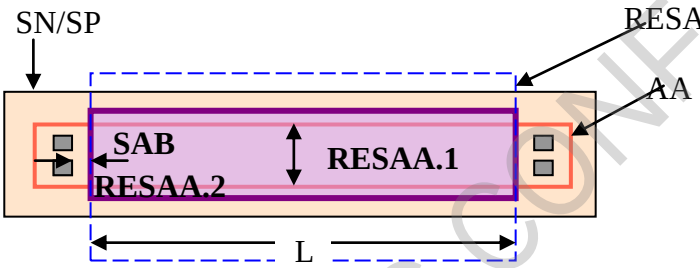
RESAA is the marker layer for AA resistor. AA resistor must be within RESAA marker layer.

Non-silicide AA resistor region: ((RESAA AND AA) AND SAB)

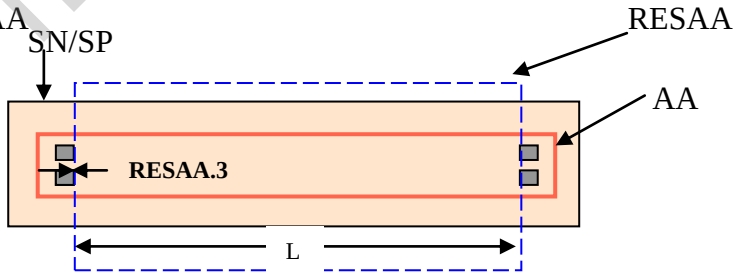
Silicide AA resistor region: ((RESAA AND AA) NOT INTERACT SAB)

Rules number	Description	Operation	Design Value	Unit
RESAA.1 [R]	Width of AA resistor with SAB	≥	1.00	um
RESAA.1a [R]	Suggest the Nsq ≥ 1 for stable Resistivity.			

Note: Nsq means square numbers of the resistor.



AA Resistor with SAB



AA Resistor without SAB

7.2.29.3 Poly resistor rule

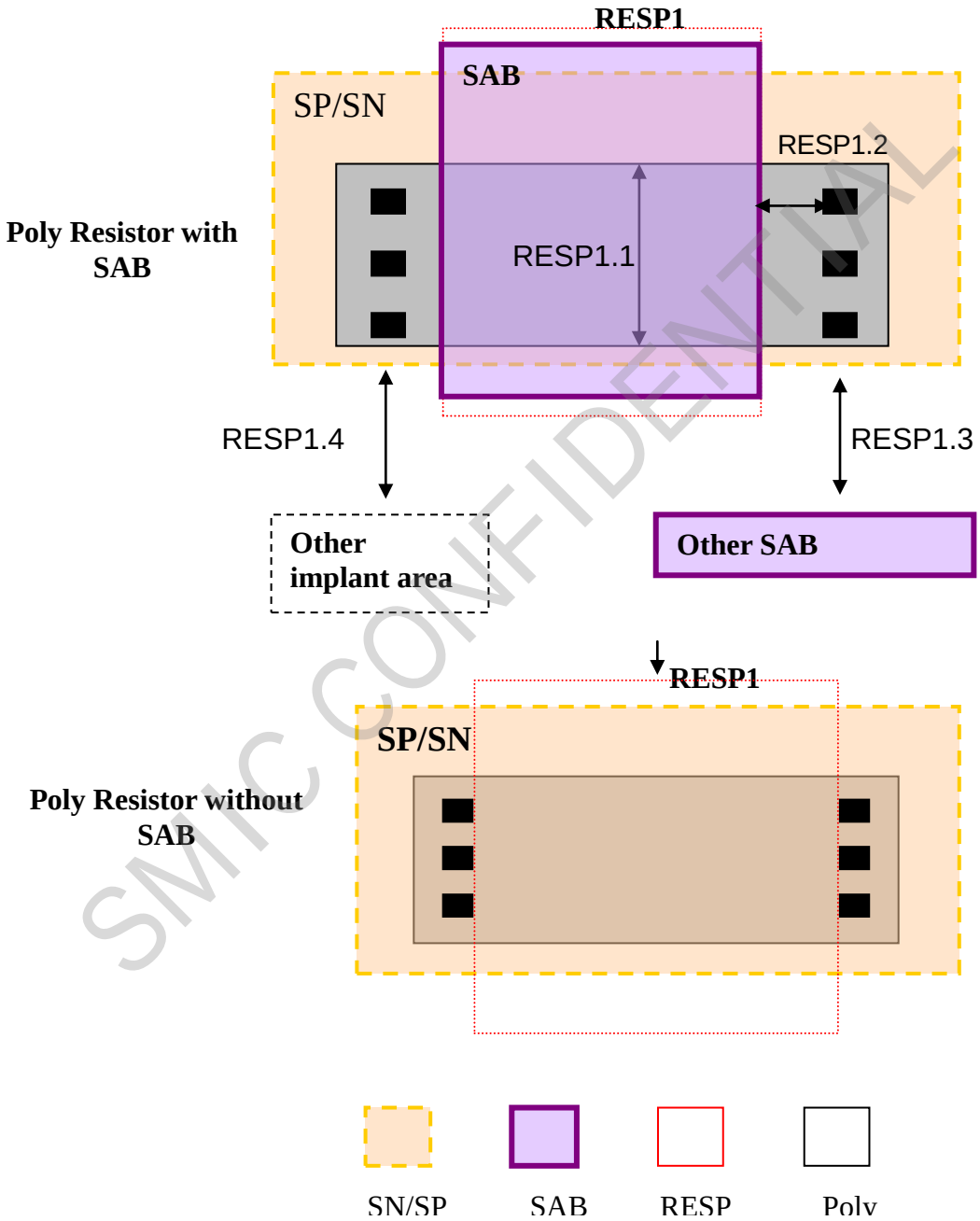
RESP1 is the marker layer for poly resistor. Poly resistor must be within RESP1 marker layer.

Non-silicide Poly resistor region: ((RESP1 AND Poly) AND SAB)

Silicide Poly resistor region: ((RESP1 AND Poly) NOT INTERACT SAB)

Rules number	Description	Operation	Design Value	Unit
RESP1.1[R]	Width of poly resistor with SAB	≥	1.00	um
RESP1.1a[R]	Suggest poly resistor Nsq ≥ 1 for stable resistivity			
RESP1.2[R]	Space between SAB and contact on poly	=	0.22	μm
RESP1.3	Space between the resistor poly(poly interact RESP1) and un-related SAB(poly not interact SAB)	≥	0.30	um
RESP1.4[R]	Space between the resistor poly(poly interact RESP1) and un-related implant regions (poly not interact implant region)	≥	0.26	um
RESP1.5 [R] [NC]	It's recommended to place a single column CT to pick-up poly resistor.			
RESP1.6[R]	Dog-bone design at the end of poly resistor for contact pick-up is not suggested.			
RESP1.7	PLL, PLH, NLH implants are not allowed in the N+ poly resistor region; NLL, PLH, NLH implant are not allowed in the P+ poly resistor region.			

Note: Nsq means square numbers of the resistor.

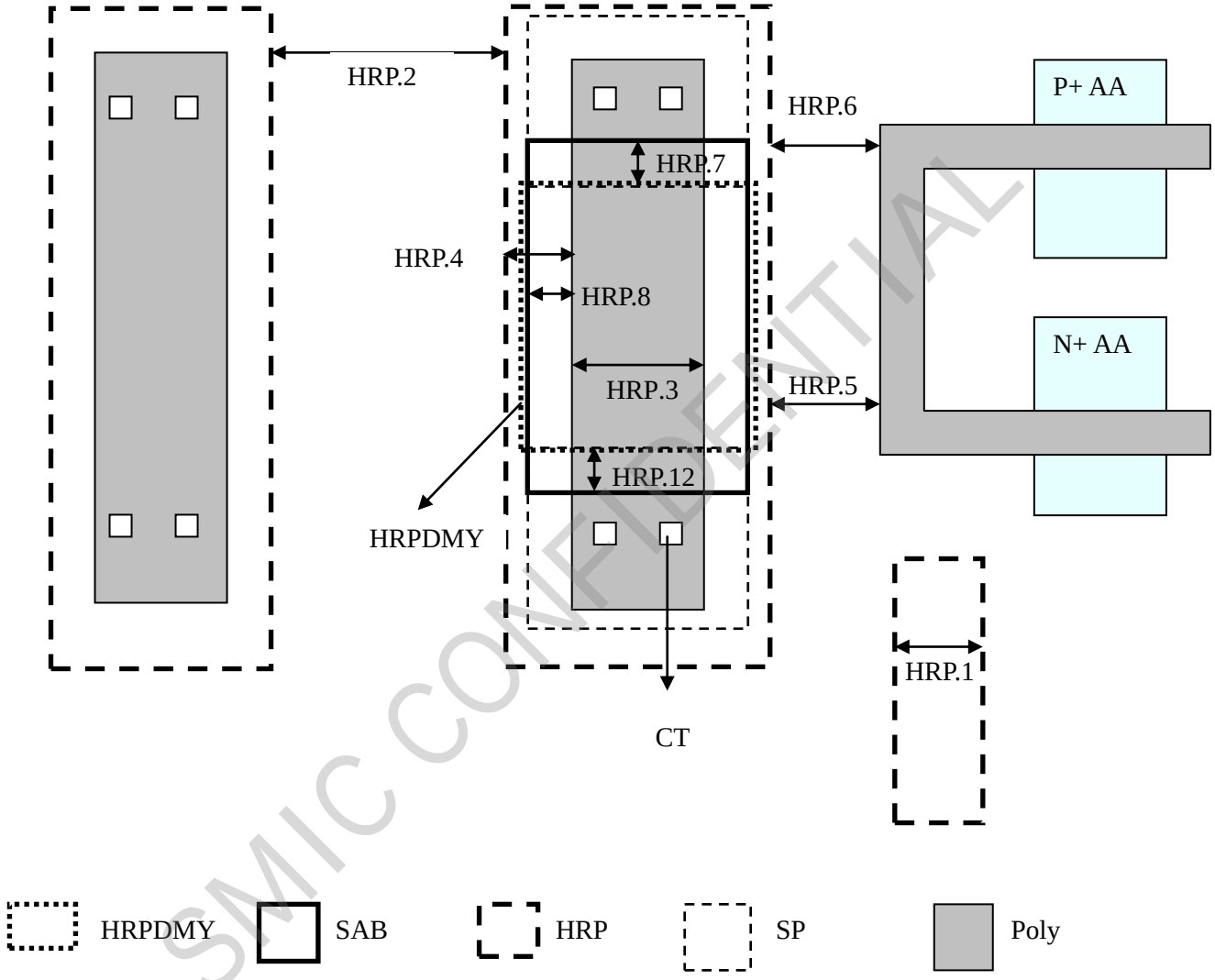


7.2.29.4 HRP (High Resistance Poly) rule

HRPDMY is the marker layer for High Resistance poly resistor. High Resistance poly resistor must be within HRPDMY marker layer.

High Resistance poly resistor region: ((HRPDMY AND Poly) AND SAB)

Rule number	Description	Operation	Design Value	Unit
HRP.1	HRP width (for HRP opening area)	≥	0.30	μm
HRP.2	Space between two HRPs	≥	0.30	μm
HRP.3	Poly width for high resistance poly resistor	≥	1.00	μm
HRP.4	HRP extension outside of poly resistor region	≥	0.20	μm
HRP.5	HRP space to Poly gate of NMOS	≥	0.20	μm
HRP.6	HRP space to Poly gate of PMOS	≥	0.20	μm
HRP.7	P+ region for pickup overlap with SAB	=	0.30	μm
HRP.8	SAB extension outside of poly resistor region	≥	0.22	μm
HRP.9[NC]	Dummy layer “HRPDMY” is needed for DRC/LVS to define high resistance Poly region			
HRP.10[R]	(strongly suggest) resistor square number ≥ 5 for precision Rs			
HRP.11	SN, SP and LDD(NLL, PLL, NLH, PLH) is not allowed in the HRPDMY region			
HRP.12	SAB extension outside of HRPDMY along the length direction of high resistance poly resistor	=	0.30	μm



7.2.30 MiM (Top plate of Metal-Insulator-Metal) rule

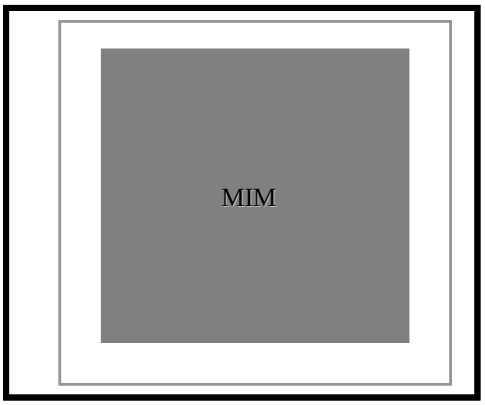
7.2.30.1 MIMDMY design guideline

MIMDMY is the DRC marking layer for active MIM, which must not include dummy MIM. Active MIM can not do DRC checking if customers don't draw MIMDMY layer.

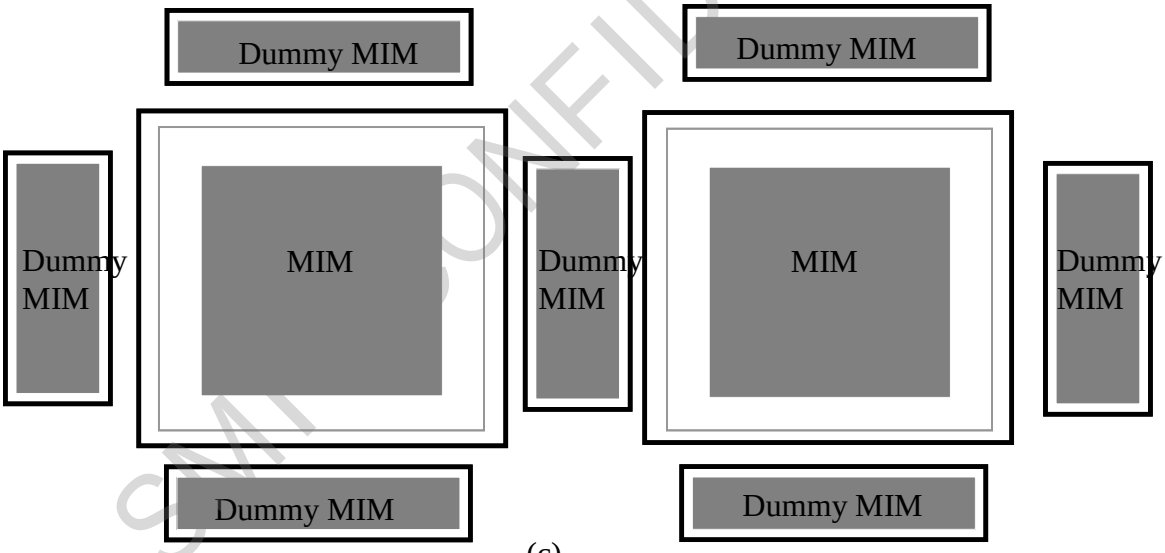
MIMDMY design is layout guideline which requires performing a DRC runset, but DRC checking is not gated for them. It's strongly recommended customers to follow layout guidelines which purpose is to ensure better performance for process and device. Customers can waive violations based on their own judgment, and please consult with process integration engineers if customers feel the need.

SMIC spice model and PDK is based on SMIC layout guidelines. And SMIC don't provide spice model and PDK if customers don't follow the layout guidelines.

Rules Number	Description	Operation	Design Value	Unit
MIMDMY.1[G] [NC]	MIMDMY is the DRC marking layer for active MIM, which must not include dummy MIM. Active MIM can not do DRC checking if customers don't draw MIMDMY layer.			
MIMDMY.2[G]	MIMDMY must fully cover active MIM region. Active MIM is enclosed by MIMDMY	=	0.2	um



(a)



(c)

Mn (bottom plate) MIM MIMDMY

7.2.30.2 One mask MIM rules

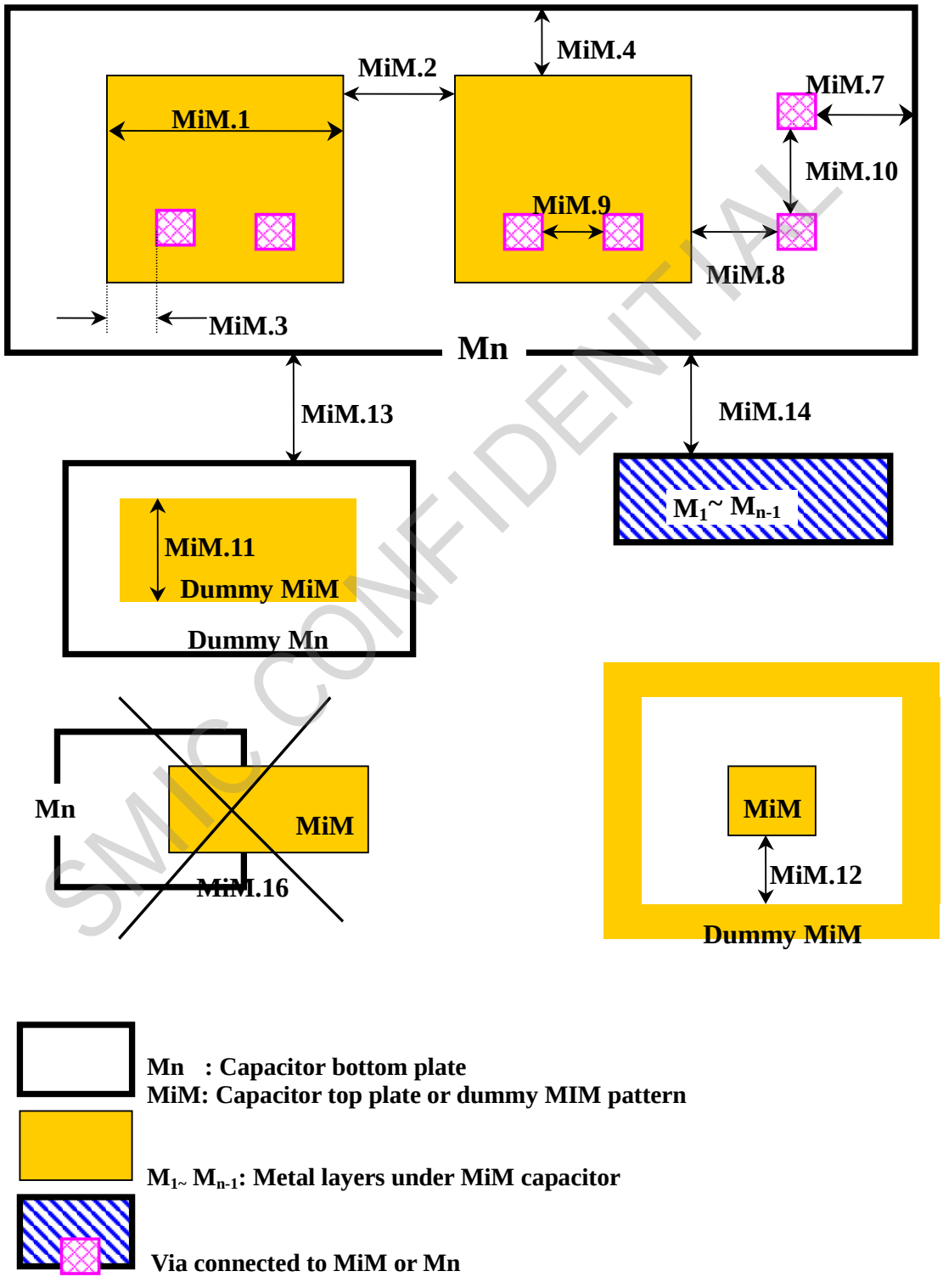
The MIM structure is placed between top metal and adjacent inter metal.
Bottom plate: Mn interact with active MIM and Mn width>3um.
Active MIM: MIM blocked by MIMDMY or MIM interact with top via.
Dummy MIM: MIM NOT active MIM

Rule number	Description	Operation	Design Value	Unit
MIM.1	MIM width and length as capacitor top plate	≥	3.00	μm
	If capacitor larger than 25*25, please use combination of smaller capacitor	≤	25.0	μm
MIM.2	Space between MIMs as top plate	≥	1.20	μm
MIM.3	MIM extension outside of Via which connect to this MIM	≥	0.24	μm
MIM.4	Bottom plate(Mn) extension outside of MIM region	≥	0.40	μm
MIM.5	Bottom metal(Mn) width and length in capacitor If capacitor larger than 30*30, please use combination of smaller capacitor. For this bottom Metal structure, the slot rules don't need follow.	≤	30.0	μm
MIM.6[R]	MIM pattern density.	≥	3%	
MIM.6a[R][NC]	Dummy MIM pattern suggested 2 X 5um with line space 1.5um is required if density less than 3%			
MIM.7	Capacitor bottom metal extension outside of Via connect to Mn	≥	0.12	μm
MIM.8	Top Via space to MIM	≥	0.40	μm
MIM.9	Space between two Vias on MIM	≥	1.00	μm
MIM.10	Space between Vias on bottom metal(Mn)	≥	0.36	μm
MIM.11	Dummy MIM width	≥	0.78	μm
MIM.12	Space between dummy MIM and MIM region	≥	0.80	μm
MIM.13	Space from MIM capacitor bottom Mn to dummy Mn which interacts with dummy MIM	≥	0.80	μm

Rule number	Description	Operation	Design Value	Unit
MIM.14[R]	To avoid strong coupling, M_{n-1} is not recommended to put beneath MIM bottom plate (except MIMSHD metal design). Minimum space between M_{n-1} and MIM bottom plate.	≥	2.00	μm
MIM.15[G]	(Purposely blank)			
MIM.16	It's not allowed MIM straddle bottom plate (Mn).			
MIM.17[R]	It's not recommended to put sensitivity devices under MIM . The sensitivity devices include RF, Analog, etc.			
MIM.18[NC]	MIM structure is required to be placed between top metal and Mn which Mn is inter-metal directly underneath of top metal. If two top metal layers process are used, the MIM layer must be placed between 1st top metal and inter metal (Mn) directly underneath of top metal..			

Note:

1. "MIM" in above design rules denote active MIM and dummy MIM.



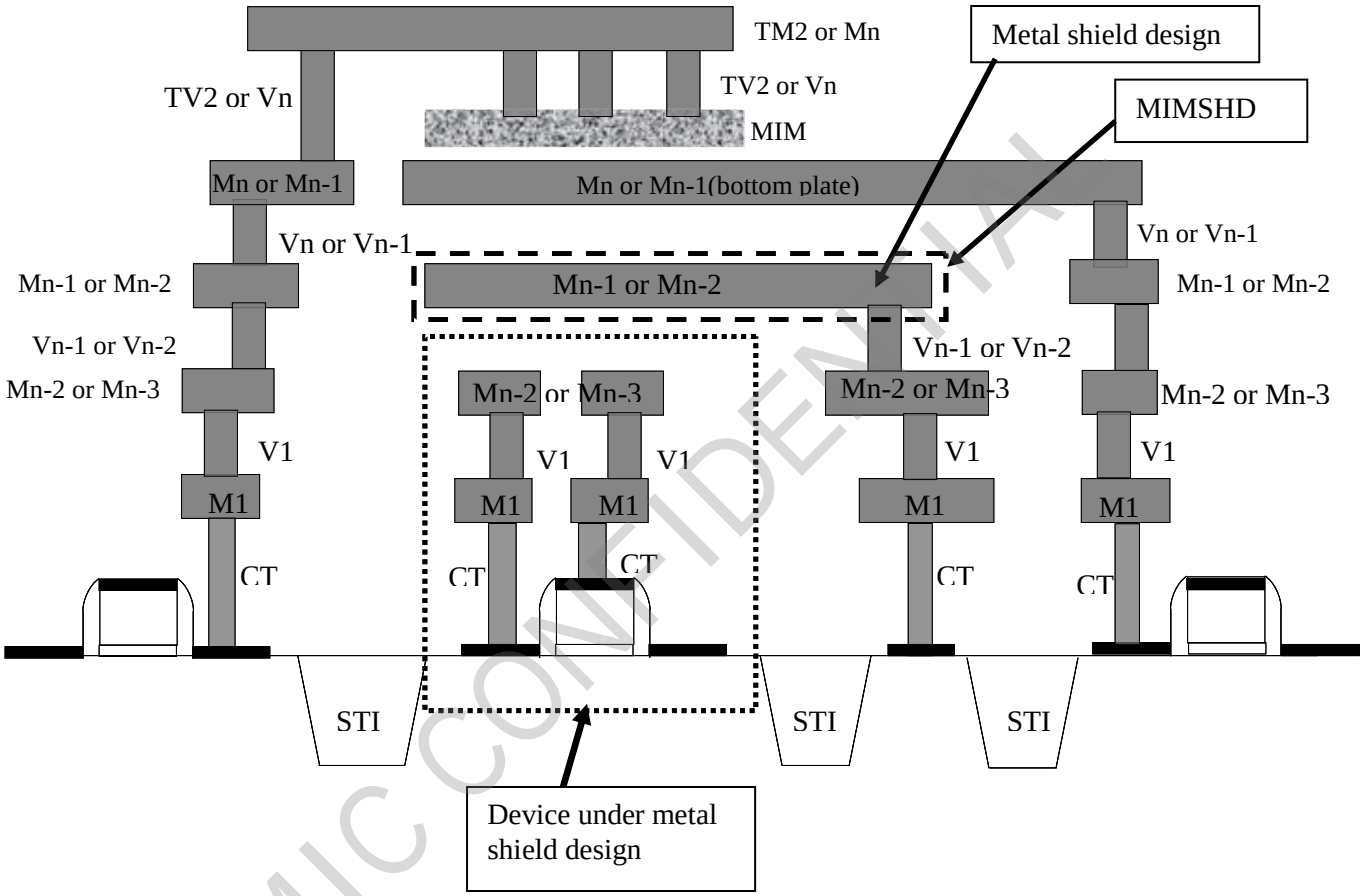
7.2.30.3 Metal shield guidelines

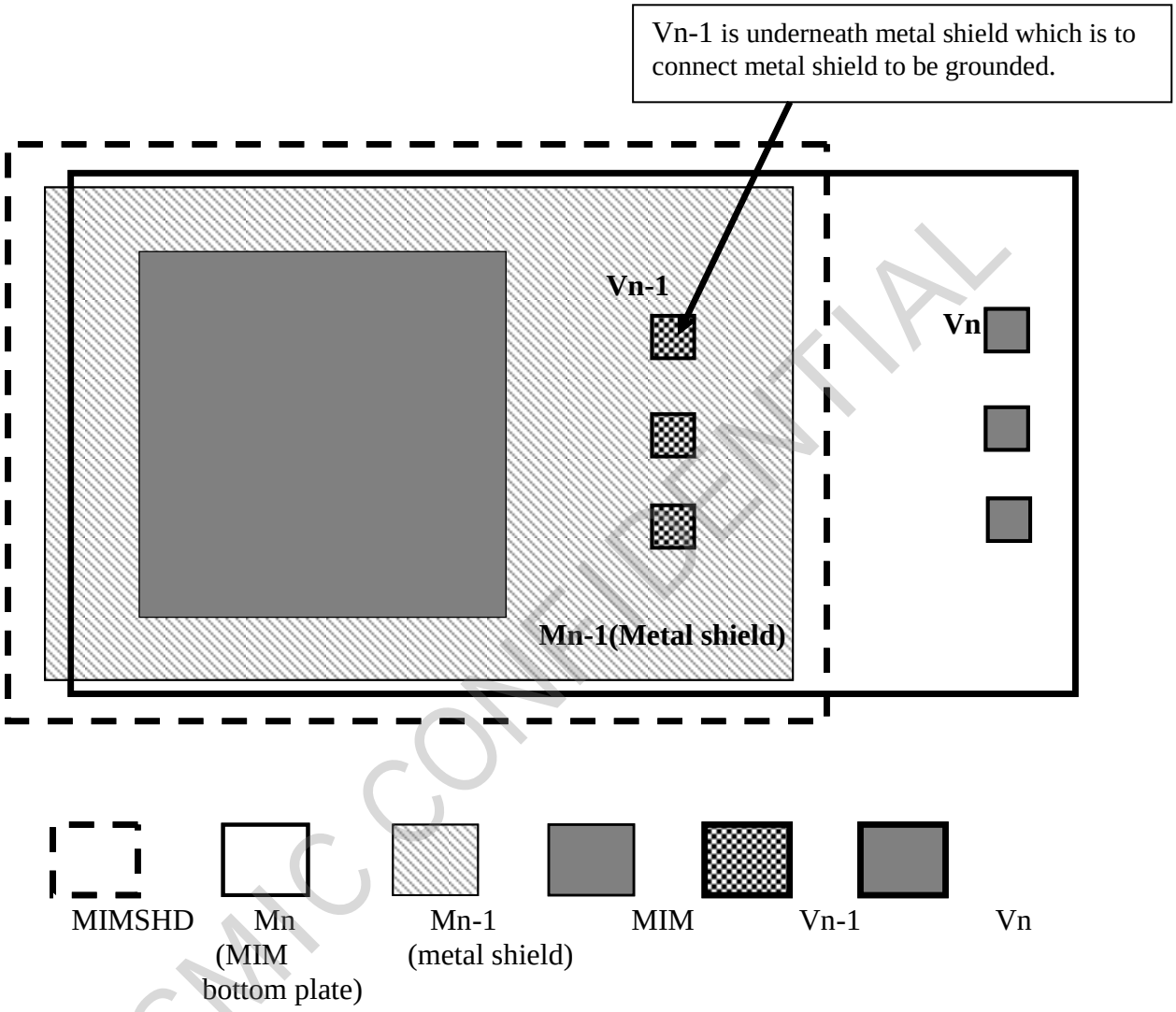
Designers need to do risk assessment if they want to use MIM shield design. For metal shield design, MIMSHD marking layer is must to be drawn.

Metal shield design is layout guideline which requires performing a DRC runset, but DRC checking is not gated for them. It's strongly recommended customers to follow layout guidelines. SMIC spice model and PDK is based on SMIC layout guidelines. And SMIC don't provide spice model and PDK if customers don't follow the layout guidelines. Customers can consult with SMIC integration engineers if customers feel the need.

Rules Number	Description	Operation	Design Value	Unit
MIMSHD.1[G] [NC]	(Purposely blank)			
MIMSHD.2[G] [NC]	Metal shield design must be covered by the marker layer of MIMSHD.			
MIMSHD.2a[G]	(Purposely blank)			
MIMSHD.3[G]	MIMSHD solid metal (MIMSHD AND Mn-1) must enclose of MIM bottom metal	≥	4	um
MIMSHD.4[G] [NC]	Metal shield design must be solid and without metal slot, and isolated from MIM bottom plate, and be grounded.			
MIMSHD.5 [G] [NC]	Metal shield design can not connect with other metal lines at the same metal layer, which the other metal lines are not grounded.			
MIMSHD.6[G] [NC]	The via layer directly underneath metal shied design is not allowed in MIM area, which means metal shield design isn't connected to metal underneath MIM.			

Note:
"MIM" in above design rules denote active MIM and dummy MIM.





7.2.31 Two masks MiM (Using 2 plate form Metal-Insulator-Metal) rule

7.2.31.1 MiM (Top plate of two masks MiM) rule

Active MIM: MIM blocked by MIMDMY or MIM interact with top via.

Rule number	Description	Operation	Design Value	Unit
BMIM.1	MIM width and length as capacitor top plate	≥	2.00	μm
		≤	25.0	μm
BMIM.2	Space between two MIMs as top plate	≥	0.80	μm
BMIM.3	MIM extension outside of Via which connect to this MIM	≥	0.24	μm
BMIM.4	Space of Via which connect with bottom plate (plate-2) to MIM region	≥	0.40	μm
BMIM.5	Space between two Vias on MIM	≥	0.80	μm
BMIM.6[R]	To avoid strong coupling, M_{n-1} is not recommended to put beneath MIM (except MIMSHD metal design). Minimum space for M_{n-1} to MIM.	≥	1.00	μm
BMIM.7[R]	MIM pattern density.	≥	3%	
BMIM.8	Dummy MIM width	≥	0.78	μm
BMIM.9	Space between dummy MIM and MIM region	≥	0.80	μm
BMIM.10	Space between dummy MIM and Plate-2	≥	0.80	μm
BMIM.11	MIM region cross plate-2 region is not allowed			
BMIM.12[R]	(Purposely blank)			
BMIM.13[R]	It's not recommended to put sensitivity devices under MIM. The sensitivity devices include RF, Analog, etc.			
BMIM.14[NC]	For one top metal process, two-mask MIM structure is required to be placed between Mn and Mn-1, where Mn is inter-metal directly underneath of top metal.			
BMIM.15[NC]	For two top metal process, two-mask MIM structure is required to be placed within TM1(1st top metal) and Mn, where Mn is inter metal directly beneath the top metal.			

7.2.31.2 0.13um Plate-2 (Bottom plate of two masks MiM) rule

The plate-2 pattern is beneath MiM layer.

Rule number	Description	Operation	Design Value	Unit
P2.1	Extension of plate-2 region on a MiM region	≥	0.40	µm
P2.2	Space between two Vias on plate-2	≥	0.36	µm
P2.3	Plate-2 extension for Via which contact to this plate-2	≥	0.20	µm
P2.4	Space of plate-2 to plate-2	≥	0.40	µm
P2.5	M_{n-1} is not allowed to put beneath plate-2 (except MIMSHD metal design). Minimum space for M_{n-1} to plate-2	≥	0.50	µm
P2.6	DUMBM layer is needed in plate-2 region to avoid dummy metal insertion. Minimum distance of plate-2 enclosure by DUMBM	≥	2.0	µm
P2.7	P2 width and length	≥	0.46	µm
		≤	30.0	µm

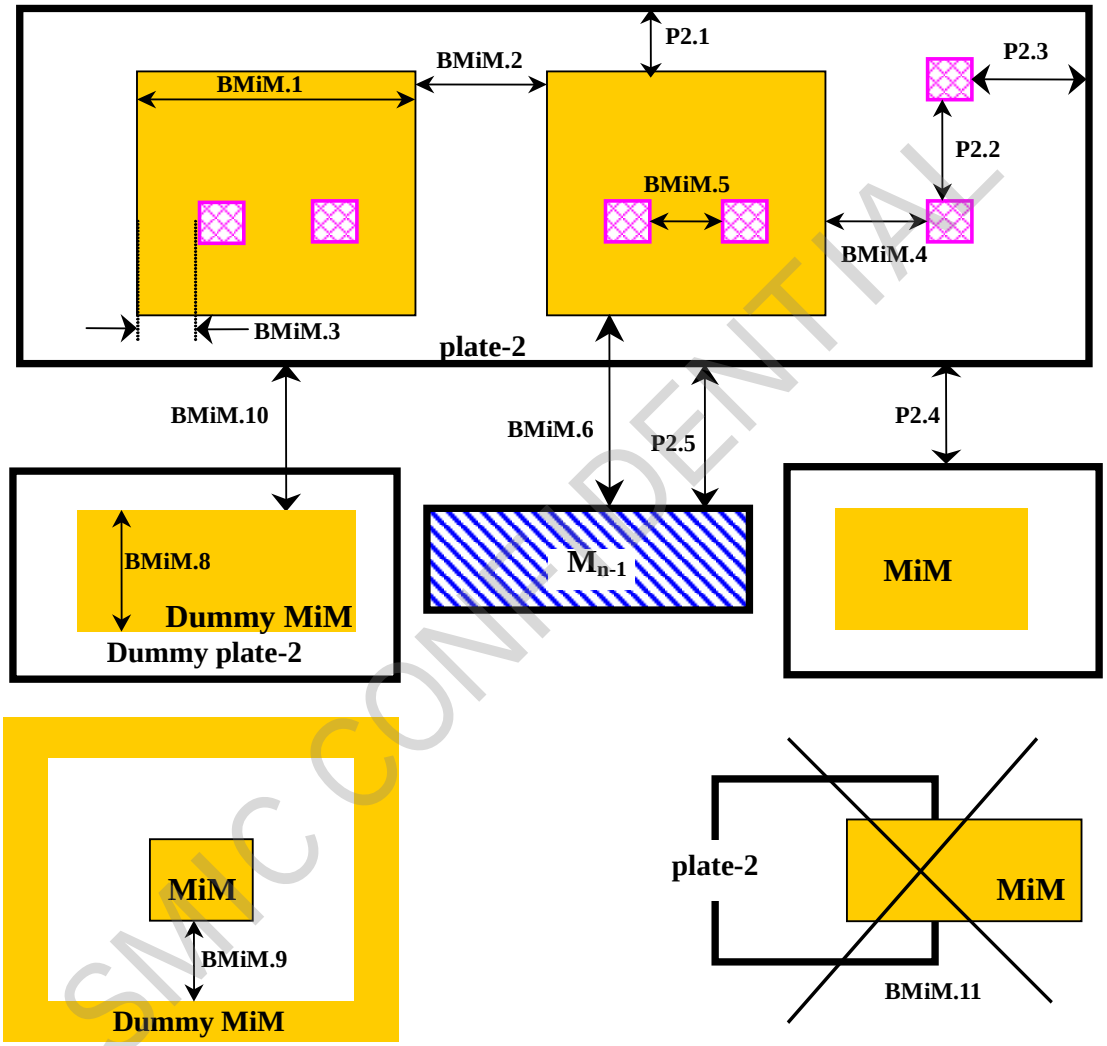


Plate-2: Capacitor bottom plate or dummy

MiM: Capacitor top plate or dummy MIM pattern

M_1~M_{n-1}: Normal metal layer

Via connected to MiM or plate-2

7.2.32 Stacked MiM (Using inter metal to stacked Metal-Insulator-Metal) rule

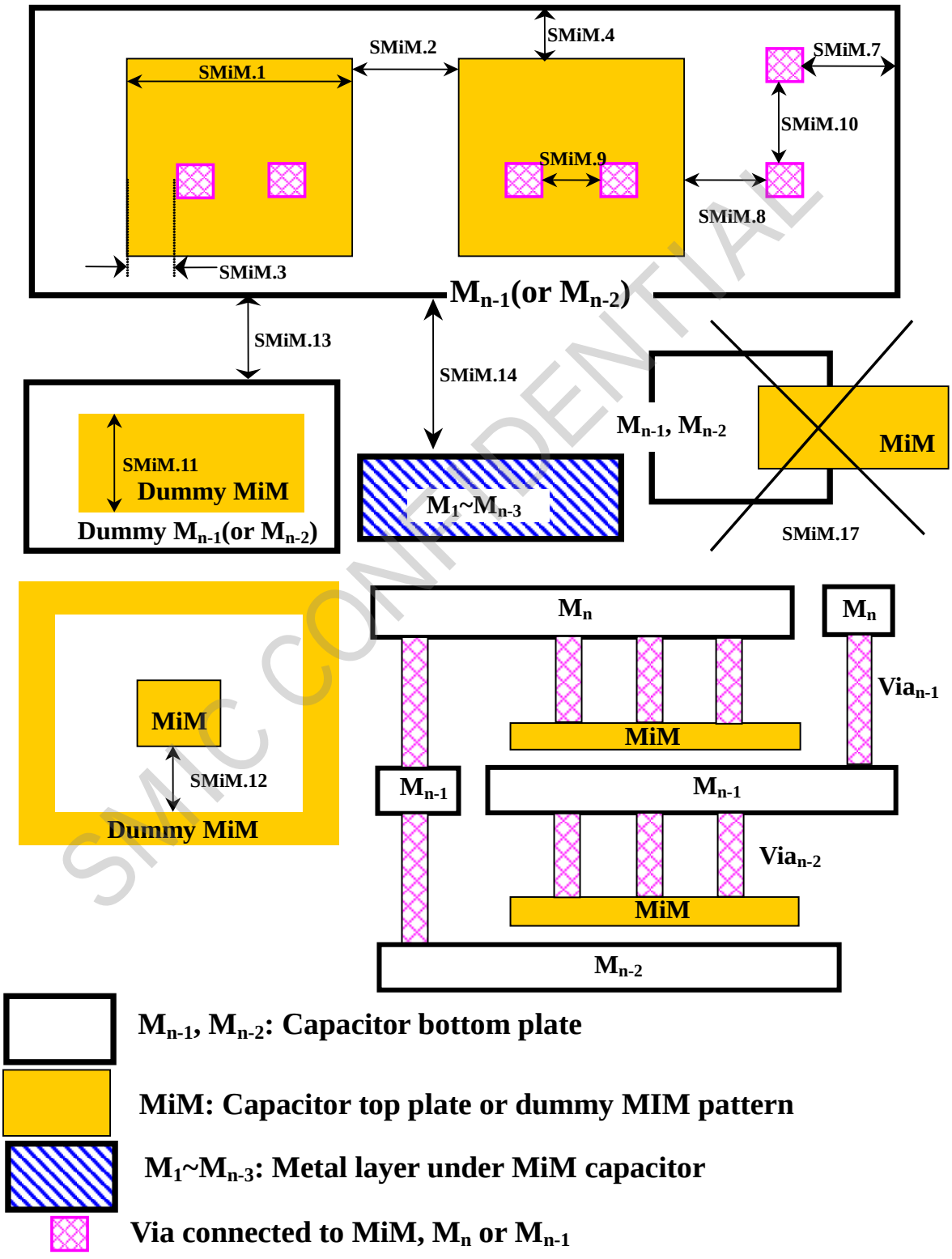
The stacked MiM structure is placed between M_n that next to the top metal and two adjacent inter metals. Use metal M_{n-1} to realize the capacitor parallel connection of two MiM structures.

Bottom plate: Mn interact with active MIM and Mn width>3um..

Active MIM: MIM blocked by MIMDMY or MIM interact with top via.

Rule number	Description	Operation	Design Value	Unit
SMIM.1	MIM width and length as capacitor top plate	≥	3.00	μm
	If capacitor larger than 25*25, please use combination of smaller capacitor	≤	25.0	μm
SMIM.2	Space between MIMs as top plate	≥	1.20	μm
SMIM.3	MIM extension outside of Via which connect to this MIM	≥	0.24	μm
SMIM.4	Bottom plate (M_{n-1} or M_{n-2}) extension outside of MIM region	≥	0.40	μm
SMIM.5	Bottom metal (M_{n-1} or M_{n-2}) width and length in capacitor If capacitor larger than 30*30, please use combination of smaller capacitor. For this bottom Metal structure, the slot rules don't need follow.	≤	30.0	μm
SMIM.6[R]	MIM pattern density.	≥	3%	
SMIM.6a[R][NC]	Dummy MIM pattern suggested 2 x 5um with line space 1.5um is required if density less than 3%			
SMIM.7	Capacitor bottom metal extension outside of Via connect to M_{n-1} (or M_{n-2})	≥	0.12	μm
SMIM.8	Space from Via to MIM region	≥	0.40	μm
SMIM.9	Space between two Vias on MIM	≥	1.00	μm
SMIM.10	Space between Vias on bottom metal (M_{n-1} or M_{n-2})	≥	0.36	μm
SMIM.11	Dummy MIM width	≥	0.78	μm
SMIM.12	Space between dummy MIM and MIM region	≥	0.80	μm
SMIM.13	Space from MIM capacitor bottom metal M_{n-1} (or M_{n-2}) to dummy metal M_{n-1} (or M_{n-2})	≥	0.80	μm
SMIM.14[R]	To avoid strong coupling, M_{n-3} is not recommended to put	≥	2.0	μm

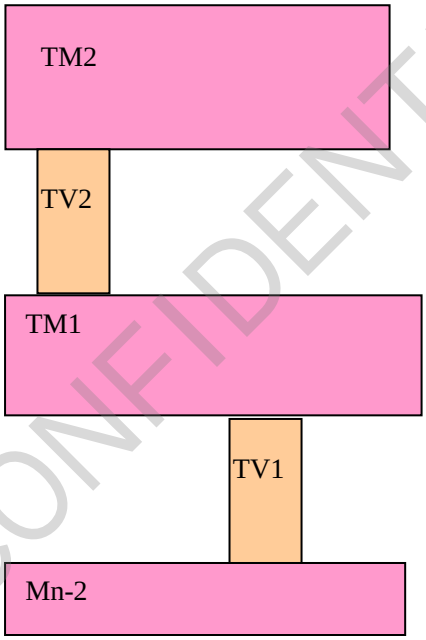
Rule number	Description	Operation	Design Value	Unit
	beneath MIM bottom plate M_{n-1} (or M_{n-2}) (except MIMSHD metal design). Minimum space between M_{n-3} and MIM bottom plate M_{n-1} (or M_{n-2}).			
SMIM.15	DUMBM layer is needed in MIM region to avoid dummy metal insertion. Minimum distance of bottom metal (M_{n-1} or M_{n-2}) enclosure by DUMBM	≥	2.0	μm
SMIM.16[G]	(Purposely blank)			
SMIM.17	MIM region cross bottom plate (M_{n-1} or M_{n-2}) metal region is not allowed			
SMIM.18[R]	It's not recommended to put sensitivity devices under MIM. The sensitivity devices include RF, Analog, etc.			
SMIM.19[NC]	Only using one MIM mask to realize two stacked MIM process			
SMIM.20[NC]	MIM structure is required to be placed between Mn and Mn-1, where Mn is inter-metal directly underneath of top metal.			
SMIM.21[NC]	Stacked MIM structure is not allowed to be used in two top metal layers process.			



7.2.33 Two top metal layers rule (option)

For TM, RF customers can also choose 2 top metal layers process. 1st top metal (TM1) must follow logic standard top metal design rule, 2nd top metal (TM2) must follow MS&RF thick top metal design rule. Two top via (TV1 & TV2) follow logic standard top via design rule. Two top metal layers process can not be used with-stacked MIM (7.2.32) together.

Two top metal layers cross-section:



7.2.34 Chip edge BORDER layer design rule

BORDER layer is used to define chip edge. Designers must draw BORDER layer following BORDER design rules below.

Rules Number	Description	Operation	Design Value	Unit
BD.1	The BORDER layer must enclose all chip layout patterns, which all chip layout patterns include seal ring if seal ring has been added by designers. This rule checking includes the layers of DNW,AA,NW,NC,PC,MVN, MVP,DG,GT,SN,SP,SAB,CT,M1,V1,Mn,Vn,P2,TMn,TVn,PA,MD,Fuse,ALPA,AADUM, GTDUM, MnDUM, TMnDUM.			
BD.2a	Enclosure of AA, GT, CT, M1, V1, Mn, Vn by BORDER layer if it need SMIC to add seal ring.	≥	0.73	um
BD.2b	Enclosure of DNW by the chip edge (BORDER layer) if it need SMIC to add seal ring.	≥	6	um
BD.3[NC]	BORDER layer size should be exactly same with the seal ring window edge if seal ring has been added by designers.			
BD.4	Enclosure of seal ring outer ring outline edge by BORDER layer if seal ring has been added by designers.	≥	2	um
BD.5[NC]	BORDER layer size should be exact same with chip window size in LDDI form (chip window size when tape-out).			
BD.6[NC]	BORDER layer rules BD.1~ BD.5 are only for chip level design rules; DRC does not check IP level BORDER.			

Note:

1. DRC runset provides switch for BORDER rule DRC checking, which is turned on by default, this switch should be turned off for IP level DRC checking.
2. Chip border: represents the minimum bounding box (solid rectangle) of all border layer (127;0).

7.2.35 Current Density Rule

Above rule value is calculated based on 0.13um design rule. For 0.11um design, when calculate the current density please remember to do "x 90%" rule value conversion considering the original layout will be done 90% shrinkage.

7.2.35.1 Current Density Rule (DC/AC)

Rule Number	Description	Operation	Design Value	Unit
Jmax is maximum DC current allowed per um of metal line width or per via/contact.				
CDR.1[NC]	DC current allowed per μm of M1 line at 110℃	≤	1.50	mA/um
CDR.2[NC]	DC current allowed per μm of M2 line at 110℃	≤	2.00	mA/um
CDR.3[NC]	DC current allowed per μm of M3 line at 110℃	≤	2.00	mA/um
CDR.4[NC]	DC current allowed per μm of M4 line at 110℃	≤	2.00	mA/um
CDR.5[NC]	DC current allowed per μm of M5 line at 110℃	≤	2.00	mA/um
CDR.6[NC]	DC current allowed per μm of M6 line at 110℃	≤	2.00	mA/um
CDR.7[NC]	DC current allowed per μm of M7 line at 110℃	≤	2.00	mA/um
CDR.8[NC]	DC current allowed per μm of TM(9K) line at 110℃	≤	5.00	mA/um
CDR.8a[NC]	DC current allowed per μm of UTM(30K) line at 110℃	≤	7.00	mA/um
CDR.8b[NC]	DC current allowed per μm of ALRDL line at 110℃	≤	2.55	mA/um
CDR.9[NC]	DC current allowed per CT at 110℃	≤	0.18	mA/CT
CDR.10[NC]	DC current allowed per V1 at 110℃	≤	0.205	mA/via
CDR.11[NC]	DC current allowed per V2 at 110℃	≤	0.205	mA/via
CDR.12[NC]	DC current allowed per V3 at 110℃	≤	0.205	mA/via
CDR.13[NC]	DC current allowed per V4 at 110℃	≤	0.205	mA/via
CDR.14[NC]	DC current allowed per V5 at 110℃	≤	0.205	mA/via

CDR.15[NC]	DC current allowed per V6 at 110℃	≤	0.205	mA/via
CDR.16[NC]	DC current allowed per TV at 110℃	≤	0.72	mA/via
CDR.17[NC]	DC current allowed per stacked V1/V2 at 110℃	≤	0.205	mA/via
CDR.18[NC]	DC current allowed per stacked V1/V2/V3 at 110℃	≤	0.205	mA/via
CDR.19[NC]	DC current allowed per stacked V1/V2/V3/V4 at 110℃	≤	0.205	mA/via
CDR.20[NC]	DC current allowed per stacked V1/V2/V3/V4/V5 at 110℃	≤	0.205	mA/via
CDR.21[NC]	DC current allowed per stacked V1/V2/V3/V4/V5/V6 at 110℃	≤	0.205	mA/via
CDR.22[NC]	DC current allowed per stacked V1/V2/V3/V4/V5/V6/TV at 110℃	≤	0.205	mA/via
CDR.23[NC]	DC current allowed per stacked V2/V3 at 110℃	≤	0.205	mA/via
CDR.24[NC]	DC current allowed per stacked V2/V3/V4 at 110℃	≤	0.205	mA/via
CDR.25[NC]	DC current allowed per stacked V2/V3/V4/V5 at 110℃	≤	0.205	mA/via
CDR.26[NC]	DC current allowed per stacked V2/V3/V4/V5/V6 at 110℃	≤	0.205	mA/via
CDR.27[NC]	DC current allowed per stacked V2/V3/V4/V5/V6/TV at 110℃	≤	0.205	mA/via
CDR.28[NC]	DC current allowed per stacked V3/V4 at 110℃	≤	0.205	mA/via
CDR.29[NC]	DC current allowed per stacked V3/V4/V5 at 110℃	≤	0.205	mA/via
CDR.30[NC]	DC current allowed per stacked V3/V4/V5/V6 at 110℃	≤	0.205	mA/via
CDR.31[NC]	DC current allowed per stacked V3/V4/V5/V6/TV at 110℃	≤	0.205	mA/via
CDR.32[NC]	DC current allowed per stacked V4/V5 at 110℃	≤	0.205	mA/via
CDR.33[NC]	DC current allowed per stacked V4/V5/V6 at 110℃	≤	0.205	mA/via
CDR.33a[NC]	DC current allowed per stacked V4/V5/V6/TV at 110℃	≤	0.205	mA/via
CDR.34[NC]	DC current allowed per stacked V5/V6 at 110℃	≤	0.205	mA/via
CDR.35[NC]	DC current allowed per stacked V5/V6/TV at 110℃	≤	0.205	mA/via

CDR.36[NC]	DC current allowed per stacked V6/TV at 110℃	≤	0.205	mA/via
CDR.37[NC]	DC current under different temperatures: 70℃: 4.110 x (corresponding value of CDR.1 – CDR.36 under 110℃) 85℃: 2.330 x (corresponding value of CDR.1 – CDR.36 under 110℃) 100℃: 1.380 x (corresponding value of CDR.1 – CDR.36 under 110℃) 125℃: 0.633 x (corresponding value of CDR.1 – CDR.36 under 110℃) 150℃: 0.318 x (corresponding value of CDR.1 – CDR.36 under 110℃) 175℃: 0.172 x (corresponding value of CDR.1 – CDR.36 under 110℃)			
Javg is recommended average AC current density through a metal line. But operating current density may exceed average value due to Joule heating. $J_{avg} = \left[\left(\int_0^{\tau} I(t)dt\right)/\tau\right]/w$ τ: the period of AC pulse				
CDR.38[NC]	Average AC current allowed per μm of M1 line at 110℃	≤	1.50	mA/um
CDR.39[NC]	Average AC current allowed per μm of M2 line at 110℃	≤	2.00	mA/um
CDR.40[NC]	Average AC current allowed per μm of M3 line at 110℃	≤	2.00	mA/um
CDR.41[NC]	Average AC current allowed per μm of M4 line at 110℃	≤	2.00	mA/um
CDR.42[NC]	Average AC current allowed per μm of M5 line at 110℃	≤	2.00	mA/um
CDR.43[NC]	Average AC current allowed per μm of M6 line at 110℃	≤	2.00	mA/um
CDR.44[NC]	Average AC current allowed per μm of M7 line at 110℃	≤	2.00	mA/um
CDR.45[NC]	Average AC current allowed per μm of TM(9K) line at 110℃	≤	5.00	mA/um
CDR.45a[NC]	Average AC current allowed per μm of UTM(30K) line at 110℃	≤	7.00	mA/um
CDR.46[NC]	Average AC current allowed per μm of ALRDL line at 110℃	≤	2.55	mA/um

7.2.35.2 Current density rule for non-salicide poly resistor

The table below listed Jmax: DC current allowed per μm of poly line at 110℃.

Non-salicide resistor	Operation	Jmax (DC)	Unit
N+ non-salicide Poly resistor[NC]	≤	0.5	mA/um
P+ non-salicide Poly resistor[NC]	≤	0.5	mA/um

Note: Non-salicide poly current density is not sensitive to temperature.

7.2.36 Antenna Ratio Effect Generic Prevention Rules

Antenna Ratio effect generic prevention rules are intended to reduce gate oxide damage, which was caused when exposed polysilicon and metal structures, connected to a thin oxide transistor, collect charge from the processing environment (e.g., reactive ion etch) and develop potentials sufficiently large to cause Fowler-Nordheim current to flow through the oxide during high density plasma processing in chip fabrication. Given the known process charge fluence, a figure of exposed conductor area to transistor gate area ratio is determined which guarantees Gate Oxide Integrity (GOI) reliability requirements. Failure to consider antenna rules in a design may lead to either reduced performance in transistors exposed to process induced damage, or may lead to total failure if the antenna rules are seriously violated.

Rule No.	DESCRIPTION	Op.	Design Value	Unit
ANT.GT1[G]	Maximum drawn ratio of field poly perimeter area to the active poly gate area connected directly to it	≤	500	
ANT.GT2[G]	Maximum drawn ratio of CT area to the active poly gate area connected directly to it	≤	10	
ANT.GT3[G]	When a protection diode is not used, the maximum ratio of cumulative metal area to the thick active poly gate area (from M1 to TM) (if double TM used, TM layer defined as TM2 layer)	≤	600	
	When a protection diode is not used, the maximum ratio of cumulative metal area to the thin active poly gate area (from M1 to TM) (if double TM used, TM layer defined as TM2 layer)	≤	5000	
ANT.GT4[G]	When a protection diode with area larger than 0.16um^2 is used, the maximum ratio of cumulative metal area to the active poly gate area can be calculated by the following equation (from M1 to Sub-TM and single TM layer) : (if double TM used, this rule spread both for TM1 layer and TM2 layer)	≤	diode area * 400 + 44000 for M1 to sub-TM; diode area * 7800 + 55000 for TM;	
ANT.GT5[G]	When the protection diode is not used, the maximum drawn ratio of Via area to the active poly gate area connected directly	≤	20	

Rule No.	DESCRIPTION	Op.	Design Value	Unit
	to it			
ANT.GT6[G]	When the protection diode with area larger than 0.16um^2 is used, the maximum drawn ratio of Via area to the active poly gate area	≤	diode area (um^2) * 200 + 1000	

A. The definition of field poly antenna ratio

Ratio = 2[(L+W)x t]/ (W2 x l)

L : floating field poly length connected to gate

W1 : floating field poly width connected to gate

t : field poly thickness (1750A in reference document TD-LO13-SP-2001)

W2 : connected transistor channel width

l : connected transistor channel length

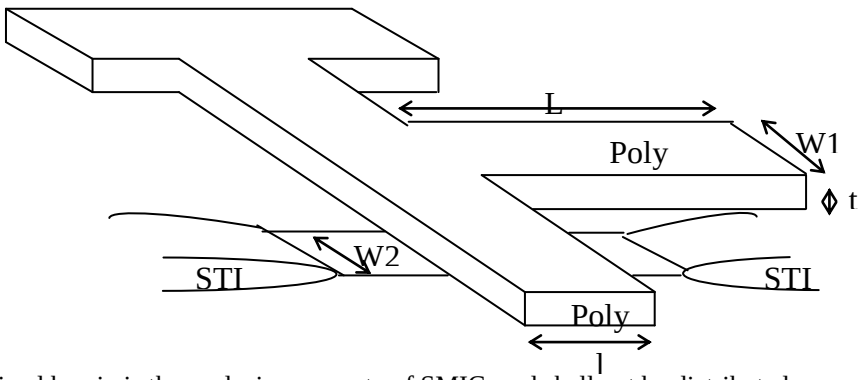
B. The definition of CT, Via1-Via7 antenna ratio is

Ratio={total CT (Via) area }/(W2 x l)

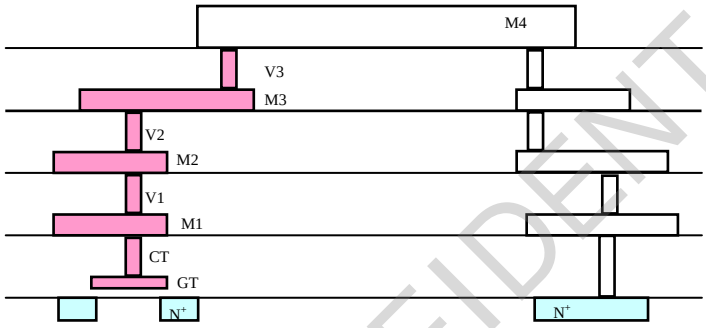
C. The definition of Cumulative Metal antenna ratio is

Ratio=(A_{M1}+…)/(W2 x l)

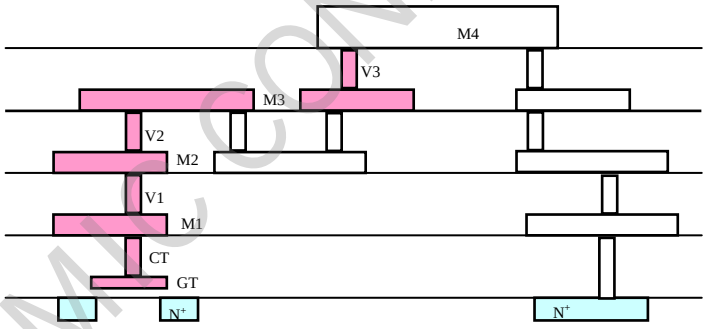
A_{Mx} : Effective metal(x) area that is electrically connected to gate without using Metal(x+1), and not to connected to active area. Cumulative Metal antenna ratio is relative to total effective metal layer area.



• **In case of 4 metal level (I)**



• **In case of 4 metal level (II)**



C.A.R. (Cumulative antenna ratio)

7.2.37 Conventional rule

Rules number	Description	Operation	Design Value	Unit
Convention.1	NW not interacting with N+ pickup is not allowed			
Convention.2	PMOS in PW is not allowed, exclude SRAM region.			
Convention.3	AA must be fully enclosed by (SN OR SP), except AA interact RESNW			
Convention.4	For two top-metal process, TM1 is a must layer. For one top-metal process, TM1 layer is not allowed.			

7.2.38 Dummy check rule

7.2.38.1 AA Dummy pattern check rules

Suggest following SMIC AA dummy insertion rules for dummy filling.
For non-SMIC AA dummy patterns (data type 1), SMIC data process will follow below table for DRC checking.

Rules number	Description	Operation	Design Value	Unit
AADUMCK.1	AA dummy can not violate AA.2, AA.3, AA.8, AA.10.			
AADUMCK.2	Space between AA dummy and AA main patterns can not violate AA.3.			
AADUMCK.3	Space between AA dummy and poly main pattern can not violate GT.4.			
AADUMCK.4	AA dummy patterns cannot touch AA/GT.			
AADUMCK.5	Dummy AA pattern is not allowed inside RESAA/RESNW/RESP1 covered areas.			
AADUMCK.6	Space between dummy AA and DUMBA /NW edge	≥	2	um

7.2.38.2 Poly Dummy pattern check rules

Suggest following SMIC poly dummy insertion rules for dummy filling.
For non-SMIC poly dummy patterns (data type 1), SMIC data process will follow below table for DRC checking.

Rule numbers	Description	Operation	Design Value	Unit
GTDUMCK.1	Poly dummy can not violate GT.2, GT.3.			
GTDUMCK.2	Space between poly dummy and poly main pattern can not violate GT.3.			
GTDUMCK.3	Dummy poly pattern is not allowed to exist above AA (not include dummy AA). Space between poly dummy and AA main pattern can not violate GT.4.			
GTDUMCK.4	Poly dummy patterns cannot touch GT main patterns.			
GTDUMCK.5	Dummy poly pattern is not allowed inside RESAA/RESNW/RESP1 covered areas.			
GTDUMCK.6	Space between dummy poly and DUMBP.	≥	2	um

7.2.38.3 Mn (n=1~7) Metal Dummy pattern check rules

Please follow SMIC's Mn dummy insertion rules for dummy insertion. If designers use their own dummy insertion patterns or methods, all metals (effective circuits plus dummy) must pass SMIC DRC.

For non-SMIC Mn dummy patterns (data type 1), SMIC data process will follow below table for DRC checking.

Rule numbers	Description	Operation	Design Value	Unit
MnDUMCK.1	M1 dummy patterns must not violate M1.1, M1.2, M1.3c, M1.4, M1.5			
MnDUMCK.2	Space between M1 dummy patterns and M1 main patterns must not violate M1.2 and M1.3c.			
MnDUMCK.3	Mn dummy patterns must not violate Mn.1, Mn.2, Mn.3c, Mn.4, Mn.5 (n=2~7)			
MnDUMCK.4	Space between Mn dummy patterns and Mn main patterns must not violate Mn.2 and Mn.3c. (n=2~7)			
MnDUMCK.5	Mn dummy metal can not be interacted with Mn metal design patterns. (n=1~7)			
MnDUMCK.6	Space between dummy metal and DUMBM	≥	2	um
MnDUMCK.7[NC]	There should be no active RF device underneath dummy metal pattern.			

7.2.38.4 TM Dummy pattern check rules

Please follow SMIC's TMn dummy pattern insertion rules for dummy filling. If designers use their own dummy fill patterns or methods, all TMn patterns (effective circuits plus dummy) must pass SMIC DRC.

For non-SMIC TM dummy patterns (data type 1), SMIC data process will follow below table for DRC checking.

Rule numbers	Description	Operation	Design Value	Unit
TMDUMCK.1	TM dummy patterns must not violate TM.1, TM.2, TM.4, TM.5, TM.6.			
TMDUMCK.2	Space between TM dummy patterns and TM main patterns must not violate TM.2 and TM.4.			
TMDUMCK.3	TM dummy metal can not interact with TM metal design patterns.			
TMDUMCK.4	Space between TM dummy patterns and DUMBM	≥	2	um
TMDUMCK.5[NC]	There should be no active RF device underneath dummy metal pattern.			

7.2.38.5 MTT (for Thick Top Metal process) Dummy pattern check rules

Please follow SMIC's TM2 dummy pattern insertion rules for dummy filling. If designers use their own dummy fill patterns or methods, all MTT patterns (effective circuits plus dummy) must pass SMIC DRC.

For non-SMIC MTT dummy patterns (data type 1), SMIC data process will follow below table for DRC checking.

Rule number	Description	Operation	Design Value	Unit
MTTDUMCK.1	MTT dummy patterns must not violate MTT.1, MTT.2a, MTT.6			
MTTDUMCK.2	Space between MTTDUM patterns and MTT main patterns must not violate MTT.2a			
MTTDUMCK.3	MTTDUM metal can not interact with MTT metal design patterns.			
MTTDUMCK.4	Space between MTTDUM patterns and DUMBM	≥	2	um
MTTDUMCK.5[NC]	There should be no active RF device underneath dummy metal pattern.			

7.2.39 SRAM design rule

It's strongly recommended designers to use SMIC SRAM IP. If designers use their owned SRAM,SMIC can't guarantee the SRAM quality, Please consult with SMIC before tape-out.

Rule number	Description	Operation	Design Value	Unit
SRAA.1	AA width	≥	0.11	um
SRAA.3	Space between AAs that are on the same well	≥	0.15	um
SRAA.4	N+ AA enclosure by NW except NW resistor region	≥	0.1	um
SRAA.5	Space between NW and N+ AA	≥	0.18	um
SRAA.6	P+ AA enclosure by NW	≥	0.16	um
SRAA.7	Space between NW to P+AA inside PW	≥	0.15	um

Rule number	Description	Operation	Design Value	Unit
SRNC.5	Space between NC and N+AA for nominal NMOS along poly length	≥	0.025	um

Rule number	Description	Operation	Design Value	Unit
SRGT.2	GT width	≥	0.07	um
SRGT.3	GT space	≥	0.14	um
SRGT.5	Extension of AA outside of GT	≥	0.155	um
SRGT.6	Extension of GT outside of AA	≥	0.01	um
SRGT.13[R]	For small MOS(channel width <=0.3um), Max AA size along channel width direction from the turning point when L-shape or H-shape AA space to GT is >=0.07um and <=0.08um	≤	0.51	um

share CT definition: Rectangle CT with area 0.064 ~ 0.058 in SRAM area

Rule number	Description	Operation	Design Value	Unit
SRCT.1	CT width and length, exclude share CT	=	0.16	um
SRCT.3	Space between AA and contact on poly	≥	0.075	um
SRCT.4a	Space between poly and contact on AA for 1.2 and 1.5V, exclude share CT	≥	0.055	um
SRCT.5	CT enclosure by AA for CT landed on device AA, exclude share CT	≥	0	um
SRCT.6	CT enclosure by poly for CT landed on poly, exclude share CT	≥	0	um

SRCT.7	CT enclosure by M1, check the CTs after corner cut 0.035, exclude share CT	≥	0	um
SRCT.9	CT is not allowed to land on gate, exclude share CT			
SRCT.10	CT can not overlap with SAB layer or (STI NOT GT) region, exclude share CT			

Rule number	Description	Operation	Design Value	Unit
SRSN.1	SN width (single point touch is allowed)	≥	0.285	um
SRSN.3	Space between SN and P+ AA inside NW	≥	0.105	um
SRSN.5	SN extension outside of NMOS poly gate	≥	0.27	um
SRSN.6	Space between SN and poly gate for PMOS	≥	0.305	um
SRSN.10	SN and AA overlap	≥	0.075	um

Rule number	Description	Operation	Design Value	Unit
SRSP.1	SP width (single point touch is allowed)	≥	0.295	um
SRSP.3	Space between SP and N+ AA inside PW	≥	0.105	um
SRSP.5	Space between SP and N-channel poly gate	≥	0.27	um
SRSP.6	SP extension outside of PMOS poly gate	≥	0.305	um
SRSP.10	SP and AA overlap	≥	0.065	um

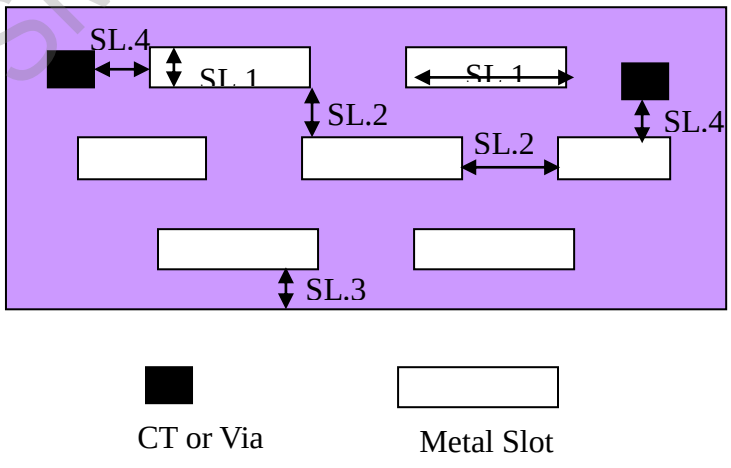
Rule number	Description	Operation	Design Value	Unit
SRM1.1	M1 width	≥	0.075	um
SRM1.2	M1 space	≥	0.095	um
SRM2.2	M2 space	≥	0.175	um

Rule number	Description	Operation	Design Value	Unit
SRV1.6	V1 enclosure by M2	≥	0.005	um
SRV2.1	V2 width and length, V2 must be square	=	0.19 or 0.36	um
SRV2.3	V2 enclosure by M2	≥	0.005	um

7.3 Layout Guidelines
7.3.1 Metal Slot Guideline

Slot is used to offset metal CMP erosion for large metals.

Rule Number	Descriptions	Operation	Rule Value	Unit
SL.1[G]	Slot width	≥	1	um
SL.2[G]	Space between two open slots.	≥	1.5	um
SL.3[G]	Open slot must be fully enclosed by metal line.	≥	2	um
SL.4a[G]	Space between M1 slot edge or inter-metal slot edge and immediately below and above contact or vias.	≥	0.05	um
SL.4b[G]	Space between top metal slot edge and immediately below and above vias.	≥	0.07	um
SL.4c[G]	Space between MTT slot edge and immediately below vias.	≥	0.42	um
SL.5[G]	Slot density of each piece of wide metal. When wide metal meet below condition: 1. Wide metal interact with metal slot. 2. Metal width ≥ 14um for M1 and inter-metal; Metal width ≥ 30um for top metal and MTT.	≥	10%	
SL.6[G] [NC]	The length of the slot should be parallel to current flow direction at this layer.			
SL.7[G] [NC]	It's strongly recommended Metal slots should be drawn with the GDS No. of corresponding metal slot layers (61;2, 62;2, 63;2 …).Then it can be performed DRC check with above slot rules. Otherwise, if metal slots are drawn with the same GDS layers of active metal (61;0, 62;0, 63;0 …), it can be only performed DRC check with main rule.			

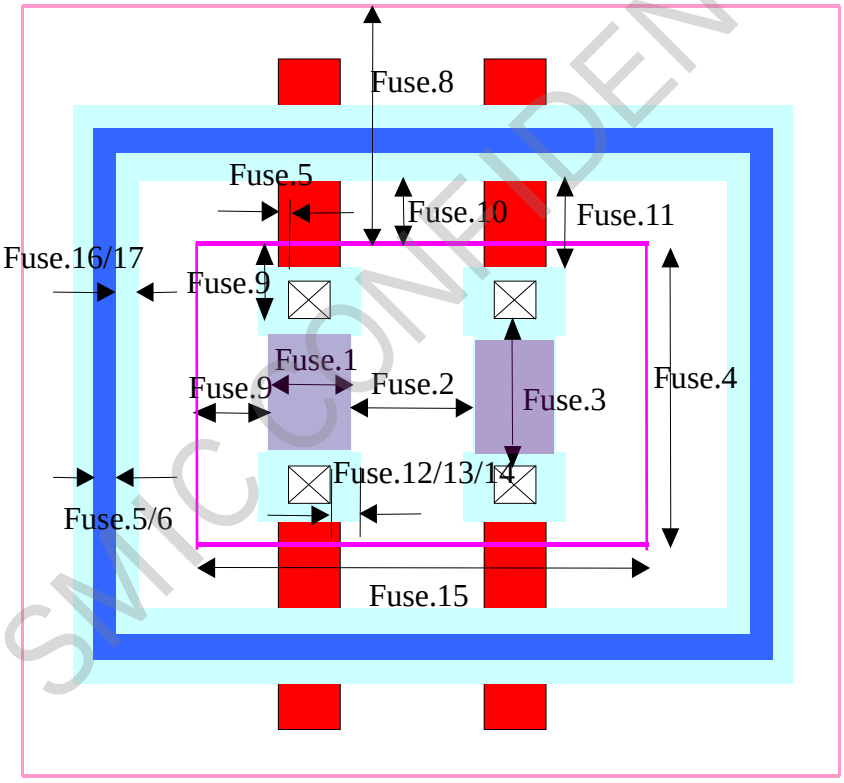


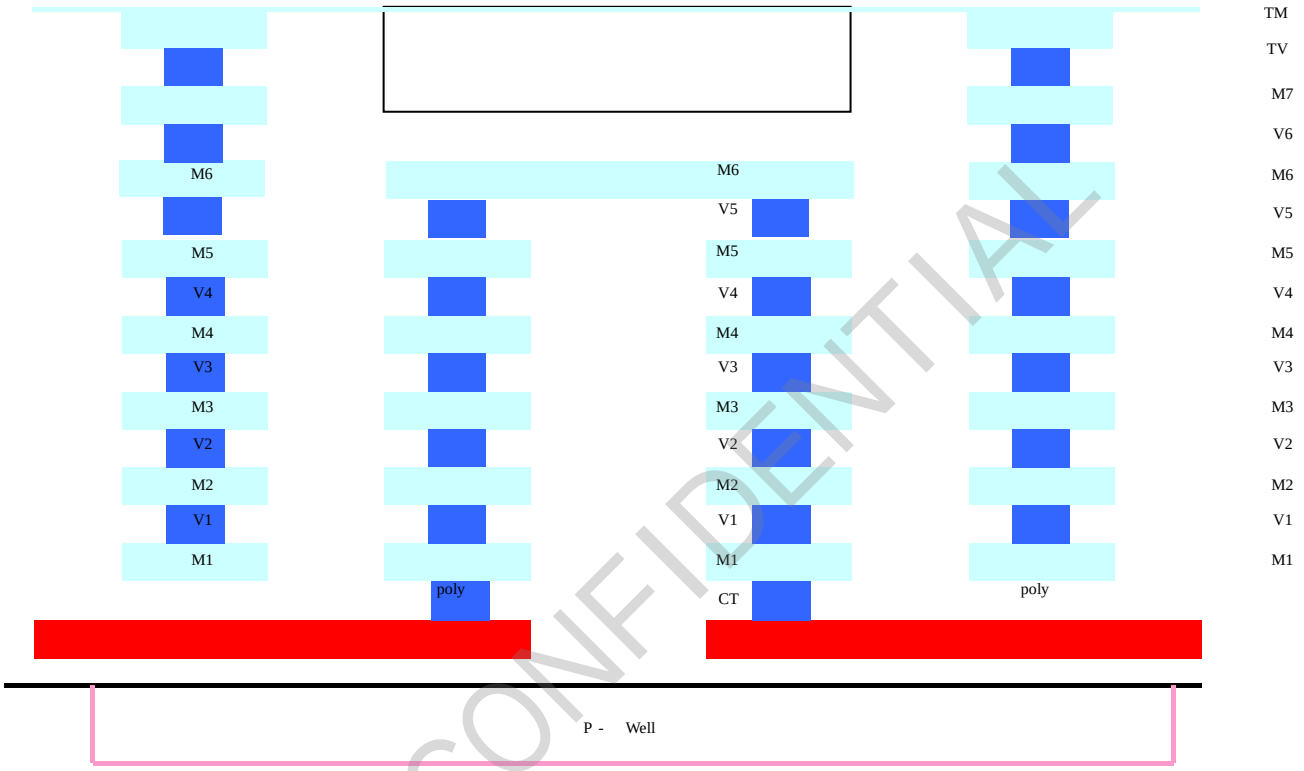
7.3.2 Metal Fuse Guideline

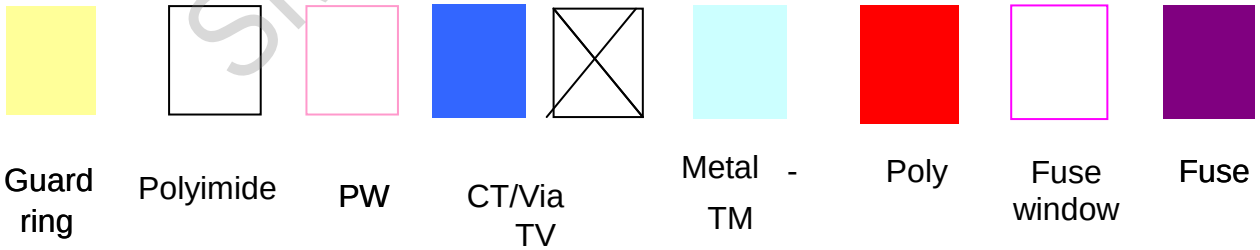
Metal fuse: Metal AND FUSE(81;0), the metal layer please refer to Fuse.20 definition.

Rules number	Description	Operation	Design Value	Unit
Fuse.1[G]	Metal fuse width	≥	0.80	um
Fuse.2[G]	Metal fuse space	≥	4.00	um
Fuse.3[G]	Metal fuse length (metal length between two Vias)	≥	4.00	um
Fuse.4[G]	FUSE(81;0) width	≥	5.00	um
Fuse.5[G]	V1and Vn(n=1~6) slot width in protection ring	=	0.19	um
Fuse.6[G]	TVn(n=1~2) slot width in protection ring	=	0.36	um
Fuse.7[G]	(Purposely blank)			
Fuse.8[G]	Space between Metal fuse edge and p-well edge	≥	8.00	um
Fuse.9[G]	Metal fuse enclosure by FUSE(81;0) region	≥	3.50	um
Fuse.10[G]	Space between FUSE(81;0) and protection ring	≥	1.50	um
Fuse.11[G]	Space between metal island (Mn interact FUSE, n=1~6) and protection ring	≥	1.00	um
Fuse.12[G]	CT enclosure by GT in FUSE(81;0) region	≥	0.30	um
Fuse.13[G]	(Purposely blank)			
Fuse.14[G]	Vn (n=1~5) enclosure by Mn/Mn+1 for stacked via in FUSE(81;0) region	≥	0.30	um
Fuse.15[G]	(Purposely blank)			
Fuse.16[G]	Vn(n=1~7) enclosure by Mn/Mn+1 in protection ring	≥	0.40	um
Fuse.17[G]	TVn(n=1~2) enclosure by TMn(n=1~2) in protection ring	≥	0.40	um
Fuse.18[G]	(Purposely blank)			
Fuse.19[G]	Metal fuse must be connected to GT through stacked via/metal/contact.			

Fuse.20[G] [NC]	For 1P8M process, M6 is required to be used as fuse; For 1P7M process, M5 is required to be used as fuse; For 1P6M process, M4 is required to be used as fuse; For 1P5M process, M3 is required to be used as fuse; For 1P4M process, M2 is required to be used as fuse; For 1P3M process, M1 is required to be used as fuse.			







Protection ring

7.3.3 Guideline for metal fuse repairing alignment mark

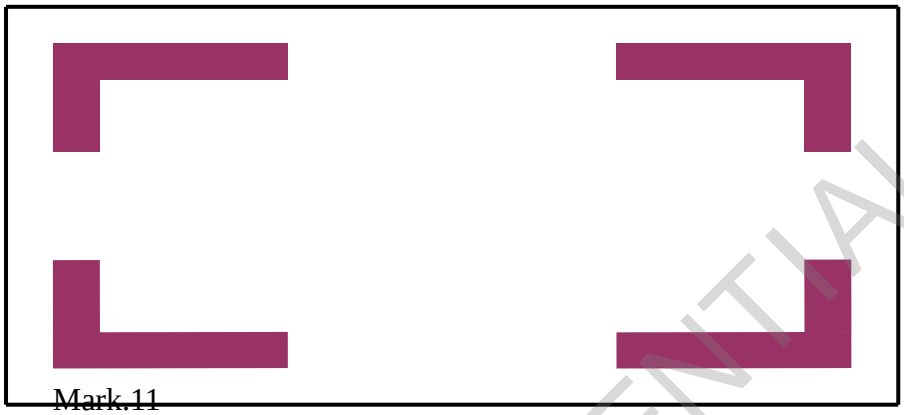
L mark should be on each corner of a chip

L mark should be the top metal layer and with passivation open above the target

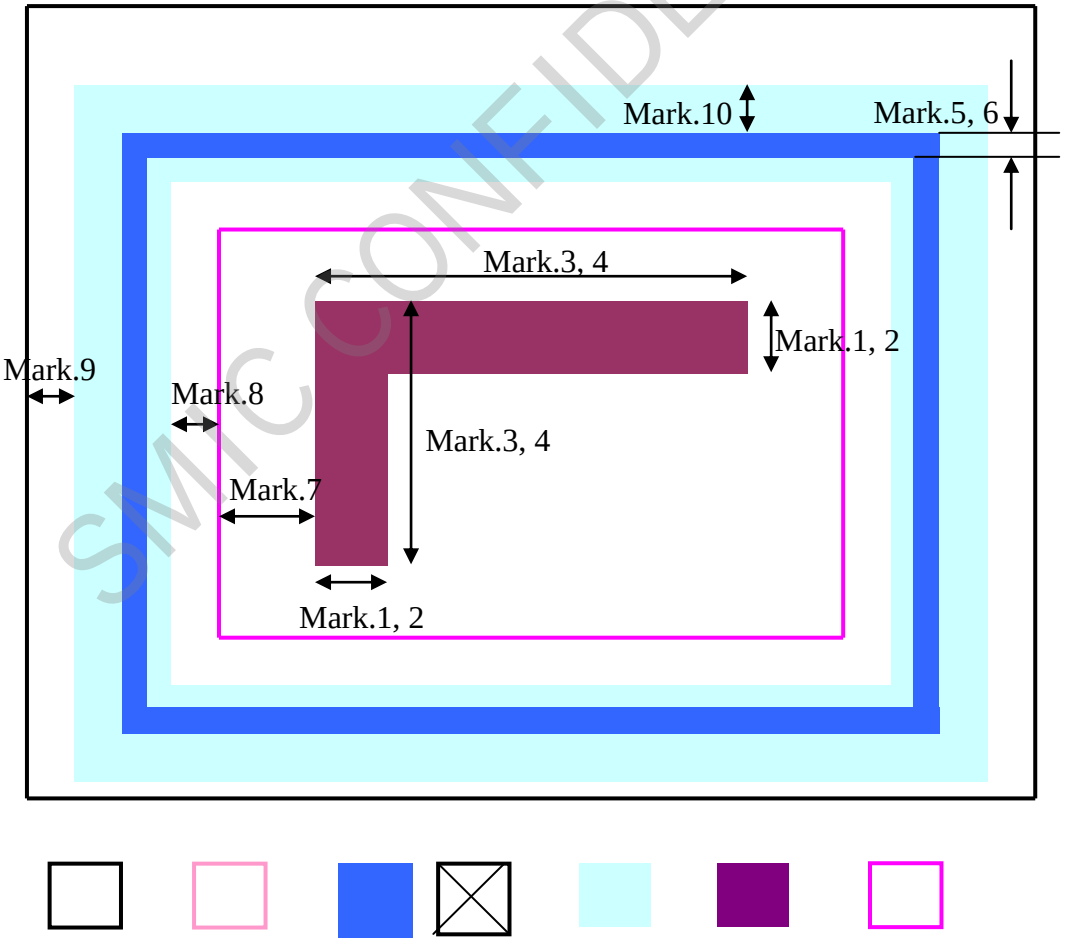
L mark should be surrounded by protection ring

L mark and its protection ring can replace corner dummy pads to serve as stress-relieve structure, i.e. alignment marks do not occupy extra die area.

Rule number	Description	Dimension (um)
Mark.1[G][NC]	L mark minimum width	10.00
Mark.2[G][NC]	L mark maximum width	20.00
Mark.3[G][NC]	L mark minimum length	30.00
Mark.4[G][NC]	L mark maximum length	50.00
Mark.5[G][NC]	V1 - Vn slot width in protection ring	0.19
Mark.6[G][NC]	TV slot width in protection ring	0.36
Mark.7[G][NC]	Minimum space between L mark and passivation opening	10.00
Mark.8[G][NC]	Minimum space between passivation opening and protection ring	1.50
Mark.9[G][NC]	Minimum space between protection ring and chip edge	7.00
Mark.10[G][NC]	V1-TV minimum enclosure by M1-TM	0.40
Mark.11[G][NC]	L mark should be on each corner of a chip	



Mark.11



Chip Edge PW CT/Via1-6 Metal 1-7 Fuse Fuse window

7.3.4 DUP (Device Under Pad) Pad Guidelines

DUPMK1 (89;156) is the marking layer for pad with device underneath.

For the design without MD (one passivation process), DUP pad area in below rules is (((PA sd 5) su 5) AND DUPMK1).

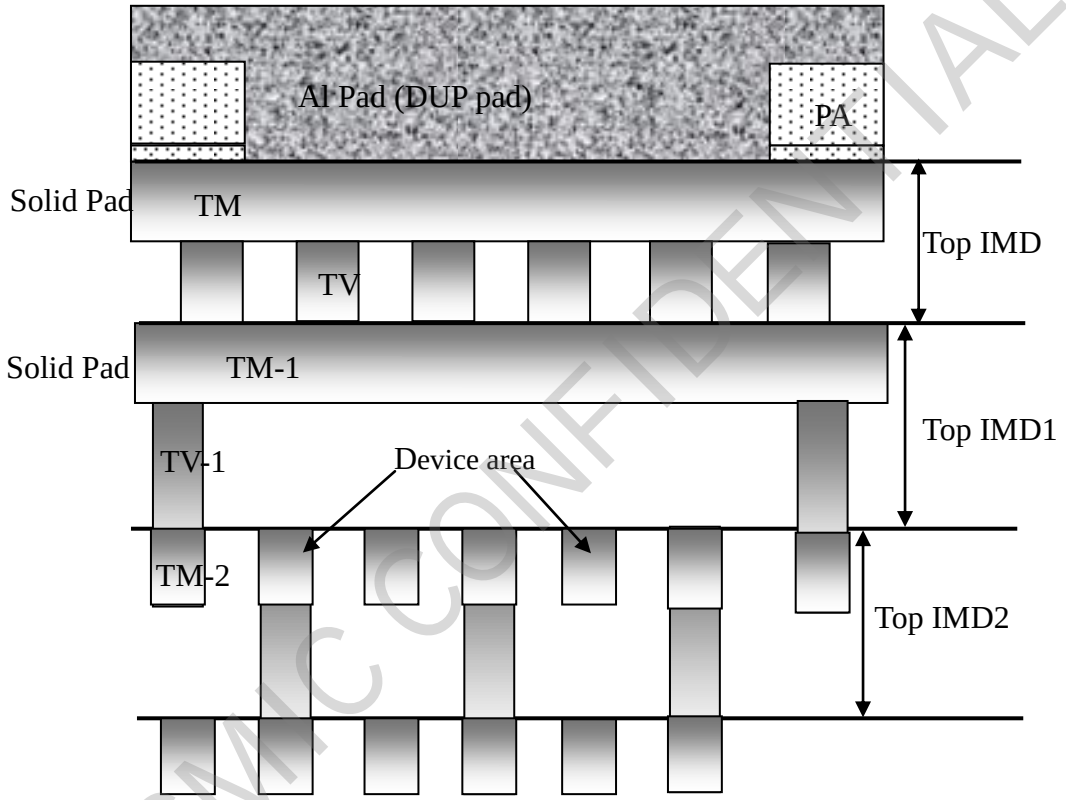
For the design with MD (two passivation process), DUP pad area in below rules is (DUPMK1 AND MD).

Rules Number	DESCRIPTION	Operation	Layout Value	Unit
DUP.1a[G]	For the design without MD (one passivation process), DUPMK1 must enclose PA for DUP pad area.			
DUP.1b[G]	For the design with MD (two passivation process), DUPMK1 must enclose MD for DUP pad area.			
DUP.2[G]	Two metal layers (TM and TM-1) are needed in DUP pad area, these two metal layers design must be solid.			
DUP.3[NC]	Device (transistor, metal resistor, MOM, BJT, etc) must be located underneath TM-1 layer.			
DUP.3a[G]	ALPAR, MOMDMY, INDMY, Resistor of TM or TM-1 must be outside of DUP pad area.			
DUP.4[G]	TV-1 pattern must be outside of DUP pad area			
DUP.5[G]	DUP pad area must have TV array between TM and TM-1. Two Via areas whose space is within 0.52μm are considered to be in the same array. TV space within array in DUP pad opening area should follow TV.2b.			

Notes:

1. TM is TM2, MTT2 or inter-metal (Mn) used as top metal.
2. TM-1 is the metal layer directly underneath TM layer. It can be inter-metal (Mn) or TM1.

3. TV is TV2. TV-1(connecting TM-1 and TM-2) is directly underneath TV layer, it can be inter-via (Vn) or TV1.

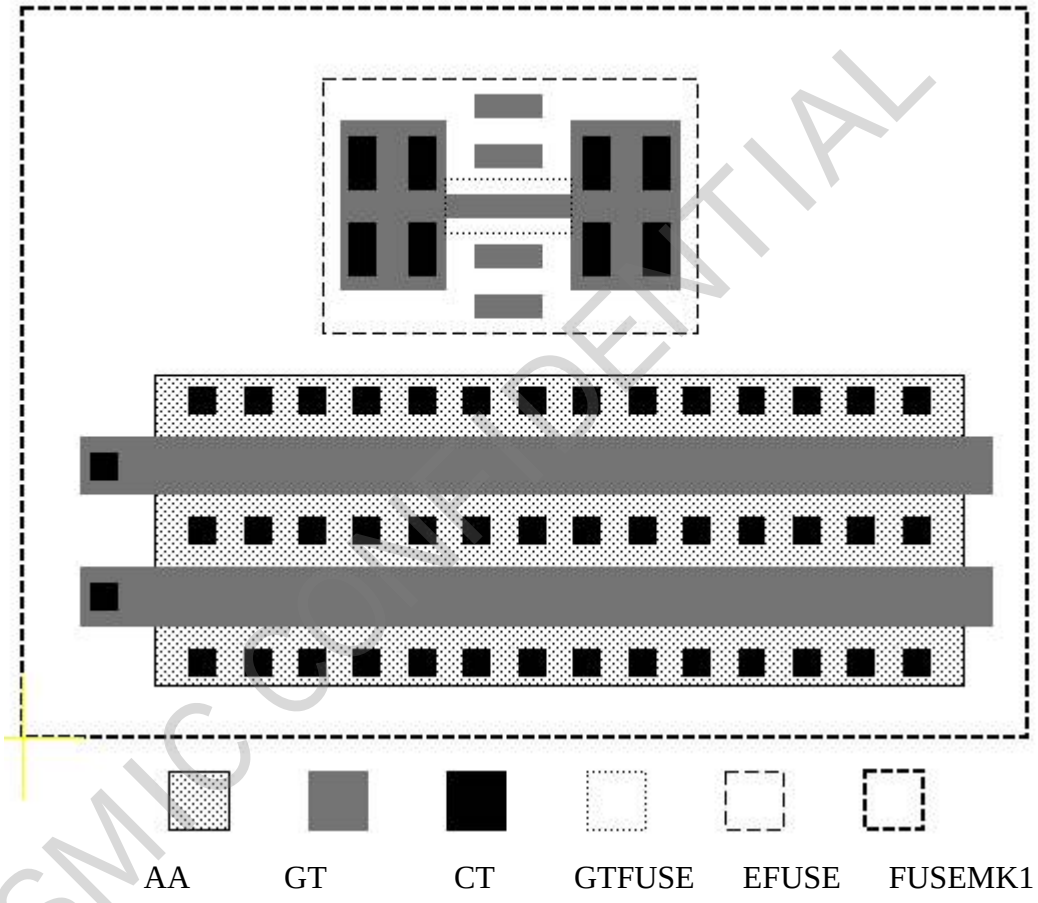


Cross section of DUP pad

7.3.5 Poly E-Fuse Layout Guidelines

For the fuse component, it must be drawn EFUSE (81;2), GTFUSE (81;1),FUSEMK1 (81;152) marker layer.
E-fuse element is covered by EFUSE (81;2).
E-fuse function area is marked with GTFUSE (81;1).
All fuse component must be fully covered by FUSEMK1 (81;152).

Rules number	Description	Operation	Design Value	Unit
EFU.1a[G][NC]	FUSEMK1 (81;152) must fully enclose all fuse component, including EFUSE (81;2) region, program transistor, etc.			
EFU.1b[G]	FUSEMK1 (81;152) must interact with EFUSE (81;2) region.			
EFU.1c[G]	FUSEMK1 (81;152) must fully cover EFUSE (81;2) region.			
EFU.2a[G][NC]	EFUSE (81;2) must fully enclose the whole fuse element and related dummy region.			
EFU.2b[G]	EFUSE (81;2) must interact with GTFUSE(81;1).			
EFU.2c[G]	EFUSE (81;2) must fully cover GTFUSE(81;1).			
EFU.3[G][NC]	(GTFUSE AND GT) is just the EFUSE function area.			
EFU.4[G][NC]	It is strongly recommended to adopt SMIC standard efuse element, including program transistor.			
EFU.5[G][NC]	If designers plan to adopt customer own design, designers must provide efuse layout to SMIC for risk assessment before design start.			



7.3.6 Logo Design Guideline

Please use rectangular or 45-degree polygons to write words, logos, and other marks that are not part of the circuit.

1. Product label region must be bully covered by LOGO (26;0) marking layer.
2. Please don't use minimum rule for LOGO pattern, except CT and Via layer.
   For the minimum width and space are less than 1um rules, please use greater, or equal 1um of width and space to draw LOGO patterns.
   If the minimum rule value is greater than 1um, please follow the minimum rule at least.

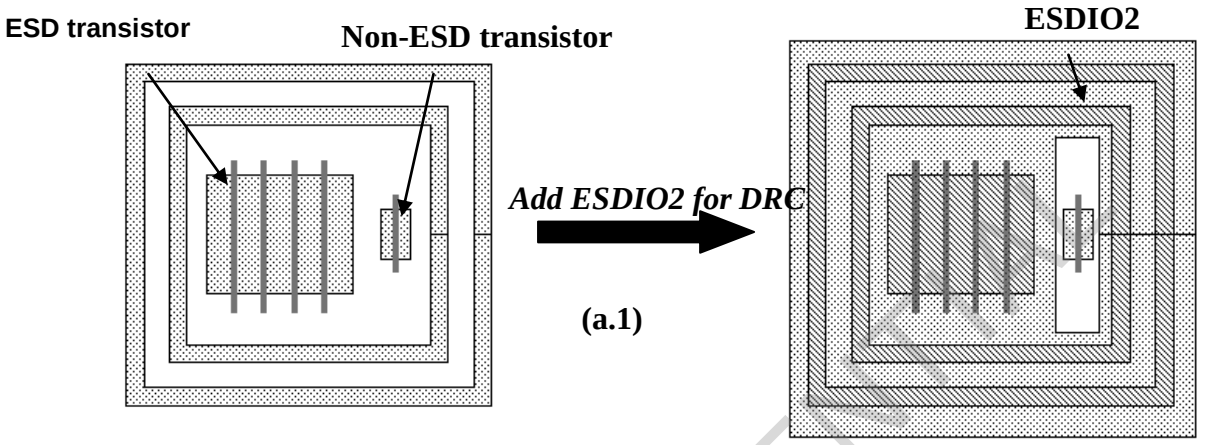
Rule number	Description	Operation	Rule Value	Unit
LOGO.1[G]	Space between LOGO and AA, GT or Metal. DRC doesn't check dummy AA, dummy GT, dummy metal.	≥	10.00	um
LOGO.2[G]	LOGO overlap with PA, ALPA, Metal fuse or Polymide window is not allowed.			
LOGO.3[G] [NC]	A circuit in the LOGO is not allowed.			

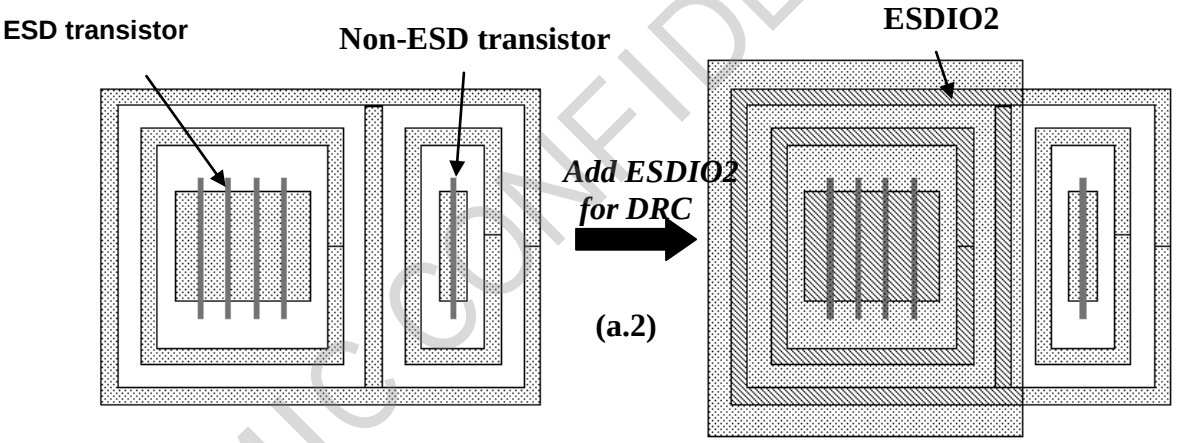
7.3.7 ESD Guideline

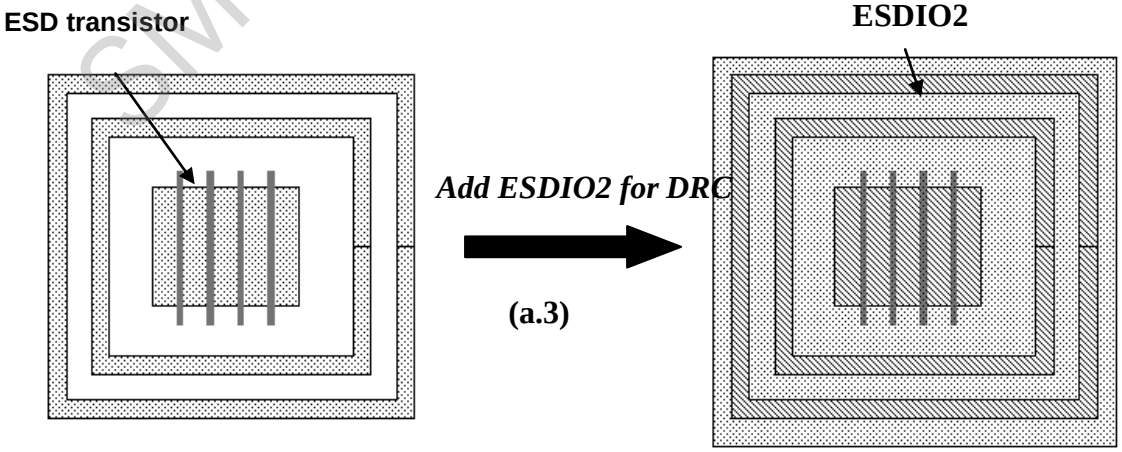
The ESD guidelines are targeted to meet HBM-2KV(Human Body Mode) and MM-200V (Machine mode) spec according to EIA/JEDEC standard and EIA/JESD22 test standard, SMIC does not guarantee the final ESD device performance. If designers do not follow SMIC ESD guideline, chip level ESD test should be done for ESD verification.

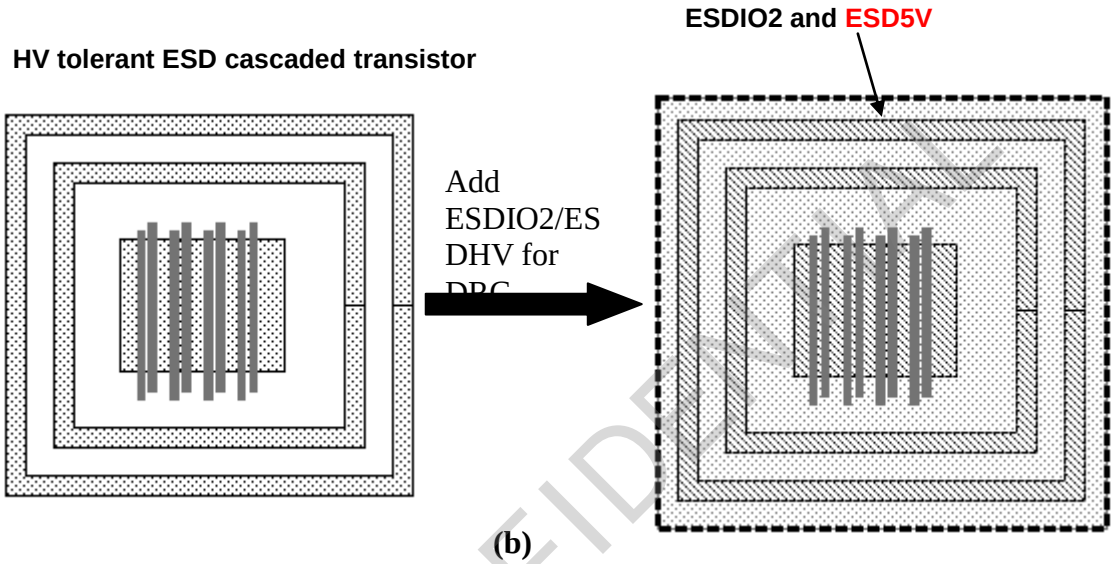
7.3.7.1 ESDIO2 (DRC marker layer for ESD component)

ESDIO2 (GDS No.:133;3) is DRC marking layer for I/O ESD N/P MOS for ESD protection. This layer should cover ESD N/PMOS (except secondary ESD N/PMOS) and its N and P guard rings, but non-ESD N/PMOS inside the same guard ring should be excluded. Otherwise, all the devices and circuits inside ESDIO2 will be regarded as ESD N/PMOS and may induce false DRC alarms. ESDIO2 should be drawn at each individual ESD N/PMOS. ESD5V (GDS: 133;1) is DRC marking layer for HV tolerant ESD protection devices using cascoded NMOS. Please refer to the examples in 7.3.7.1 Fig.1.









7.3.7.1 Fig.1 Examples of ESDIO2/ESD5V for ESD DRC

7.3.7.2 ESD design and layout guideline

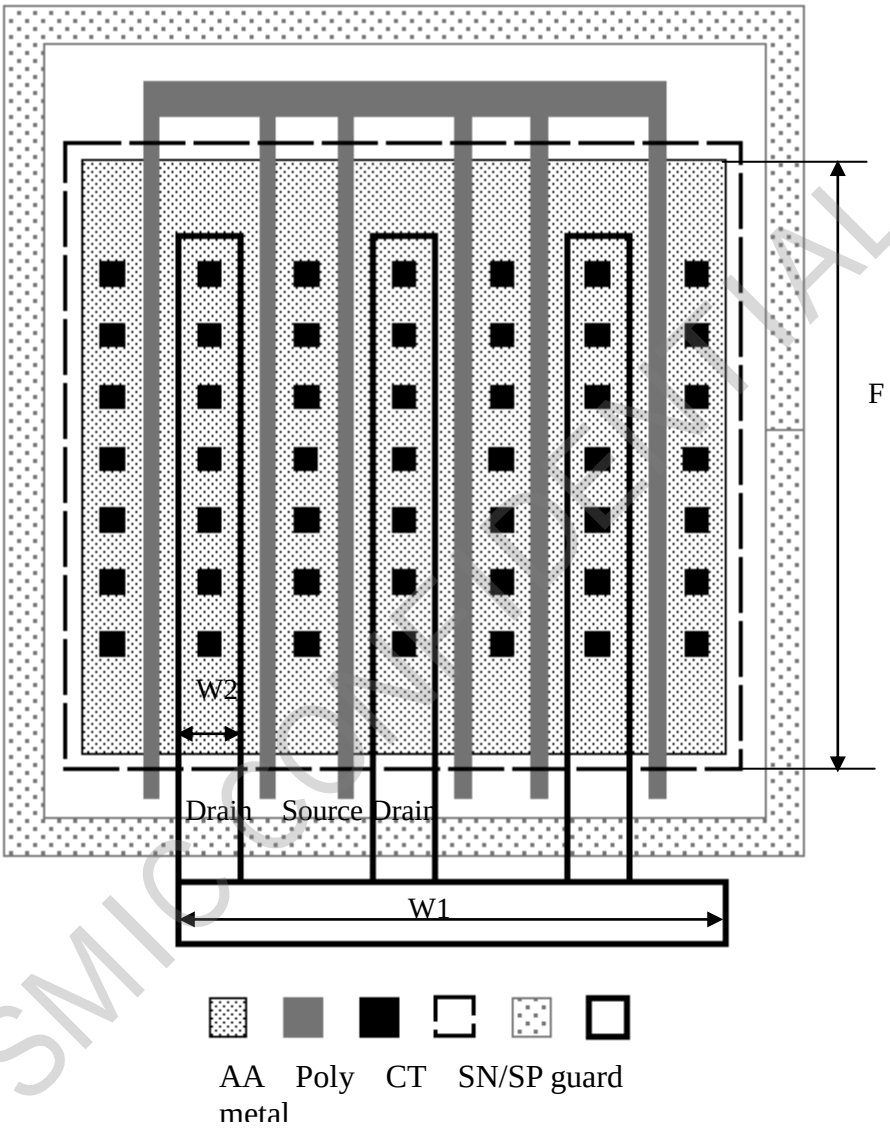
The guideline provided layout structure and dimension for N/P MOS ESD protection device design. SAB on drain side is essential for ESD protection devices.

Items	DESCRIPTION	Operation	Design Value	Unit
ESD.1[NC]	Finger-type structure with uniform finger width is suggested for N/P MOS ESD protection design			
ESD.2[G]	Unit finger width (F) of NMOS and PMOS for ESD protection device (Fig.2)	≥	20	um
		≤	60	um
ESD.3[G]	ESD.3[G] is defined for total channel width of ESD N/PMOS. The total channel width is calculated by the ESD MOS in the same Drain connection. SAB in ESDIO2 region is used for drain recognition in DRC runset. The connectivity (not limited in ESDIO2 region) can be formed by all metal, via, ALPA, PA and MD and not broken by resistors. Channel width (W) of N/PMOS for ESD protection device (Channel width=Finger width x Finger No.)	≥	360	um
ESD.4a[G]	Channel length of 3.3V I/O NMOS for protection device	≥	0.35	um
ESD.4b[G]	Channel length of 3.3V I/O PMOS for protection device	≥	0.3	um
ESD.4c[G]	Channel length of 2.5V I/O N/PMOS for protection device	≥	0.28	um
ESD.4d[G]	Channel length of 1.2/1.5V core N/PMOS for protection device	≥	0.13	um
ESD.5[G]	Space from poly edge to CT edge on source side (SCP) for NMOS and PMOS (Fig. 4 and Fig.6).	≥	0.5	um
ESD.6[G]	Space from poly edge to CT edge on drain side (DCP) (Fig. 4 and Fig.6)	≥	1.8	um
ESD.7[G]	SAB should block on drain side of NMOS and PMOS (contact region should be kept silicided.) SAB drawn on source side is not necessary.			
ESD.8[G]	Width of SAB on the drain side (A) for 1.0/1.2/1.8/2.5/3.3V NMOS and PMOS, note: A does not include the overlap of SAB area and GT(Fig. 4 and Fig.6)	≥	1.5	um
ESD.9[G]	ESD protection devices should be surrounded by guard ring, this			

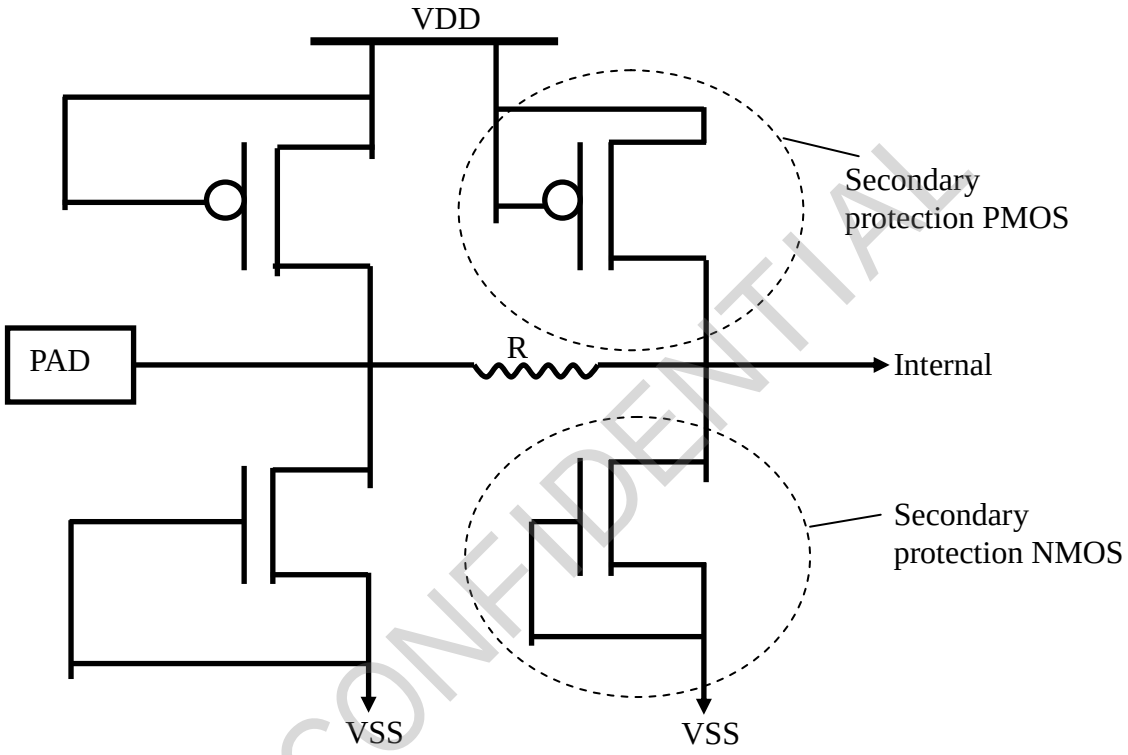
	guard ring also can be designed as the pickup of the ESD device. (Fig.2)			
ESD.10 [NC]	The NMOS/PMOS should be added after the input resistor R as the secondary ESD protection for better ESD immunity if there is no conflict with circuit operation.			
ESD.11 [NC]	value of input resister R. (Fig. 3)	≥	200	Ω
ESD.13 [NC]	The suggested channel width for secondary ESD protection device	=	20	um
ESD.13a[NC]	The suggested channel length of 3.3V I/O NMOS for secondary protection device	=	0.35	um
ESD.13b[NC]	The suggested channel length of 3.3V I/O PMOS for secondary protection device	=	0.3	um
ESD.13c[NC]	The suggested channel length of 2.5V I/O N/PMOS for secondary protection device	=	0.28	um
ESD.13d[NC]	The suggested channel length of 1.2V/1.5V N/PMOS for secondary protection device	=	0.13	um
ESD.14[G]	The overlap (Sd) of SAB and poly for ESD N/PMOS (Fig. 4)	≥	0.05	um
ESD.15[G]	For high voltage tolerant I/O using Cascoded 2.5V/3.3V NMOS, (ESDIO2 AND ESD5V) must overlap with ESD1. (refer to Fig.5& 6)			
ESD.16[G]	The space (S) between active poly gate and inactive poly gate of Cascoded NMOS should be (Fig.6)	≤	0.6	um
ESD.17[G]	For high voltage tolerant I/O designed by 2.5V/3.3V cascoded, SAB should cover all top poly gates and extend to overlap the second poly gate by (Fig. 6)	≥	0.05	um
ESD.18 [NC]	Contacts should be used as many as possible, and at least capable of bearing 100mA DC current. That is, the number of contact drawn on rule is	≥	558	count
ESD.19 [NC]	Vias should be used as many as possible, and at least capable of bearing 100mA DC current. That is, the number of via drawn on rule is	≥	502	count
ESD.20a [NC]	Total width (W2) of each individual inter metal(M1~M8) lines of the nearest current path between ESD devices and bonding pad	≥	20	um
ESD.20b [NC]	Total width (W2) of each individual top metal(TM1,TM2) line of the nearest current path between ESD devices and bonding pad	≥	3	um
ESD.21[NC]	In Chip level ESD guideline, the poly gate of N/PMOS of internal			

	and I/O circuit is not allowed to connect to power/ground or input/output pad directly. Please refer to ESD.21a, ESD.21b, ESD.21c rules below.			
ESD.21a[NC]	Secondary ESD protection or tie-high/tie-low cell is strongly recommended to insert between poly gate and power/ground pad or input/out pad.			
ESD.21b[NC]	N/PMOS used for capacitor is not recommended to connect power/ground or input/output pad directly.			
ESD.21c[NC]	Poly resistor and ESD protection N/PMOS (including primary and secondary ESD protection) can be exempt for this rule.			
ESD.22[G]	ESD.22a or ESD.22b must be followed to generate correct ESD1 implant pattern with SMIC logic operation.(For ESD1 layer Approach A)			
ESD.22a[G]	Space (C) between two SAB on the same drain AA area	<	1	um
ESD.22b[G]	Width (D) of the SAB hole in source/drain direction	<	1	um

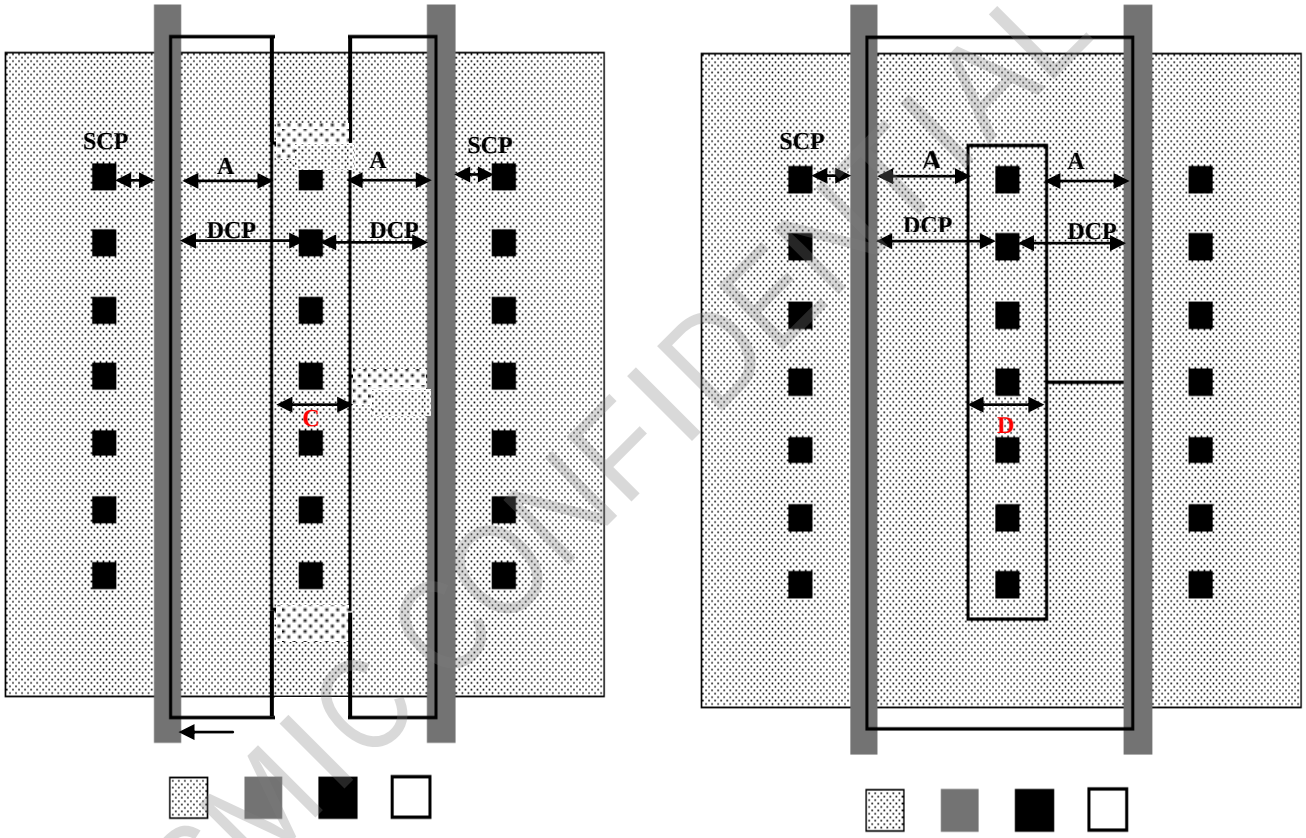
ESD.8[G] is needed to check when ESD guideline switch ON or ESD1_Approach_A switch ON



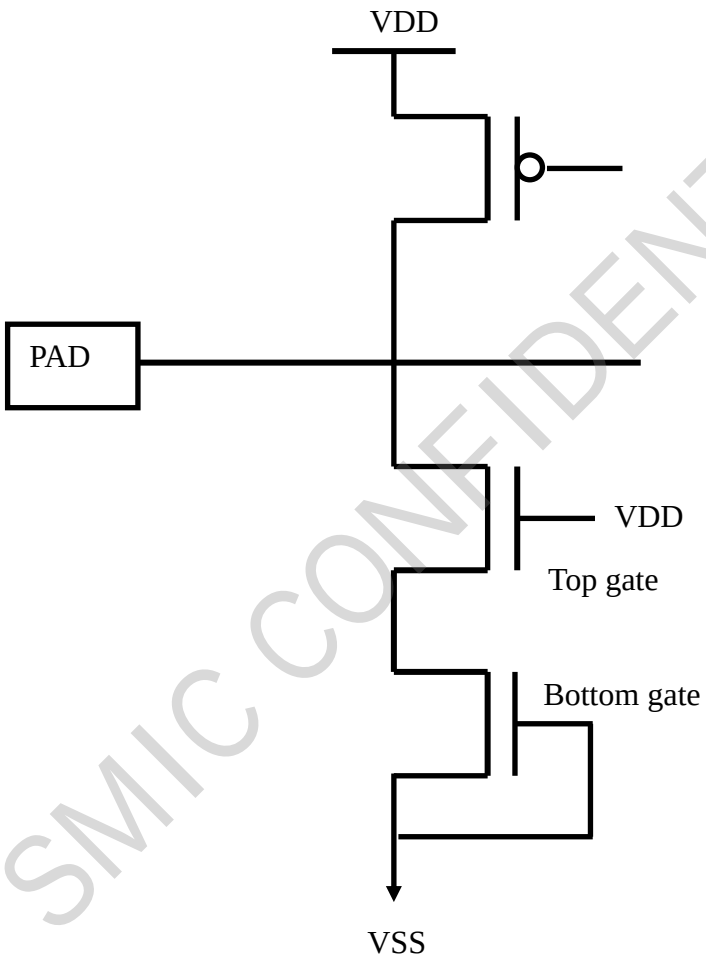
7.3.7.2 Fig.2 ESD Cell Layout Example



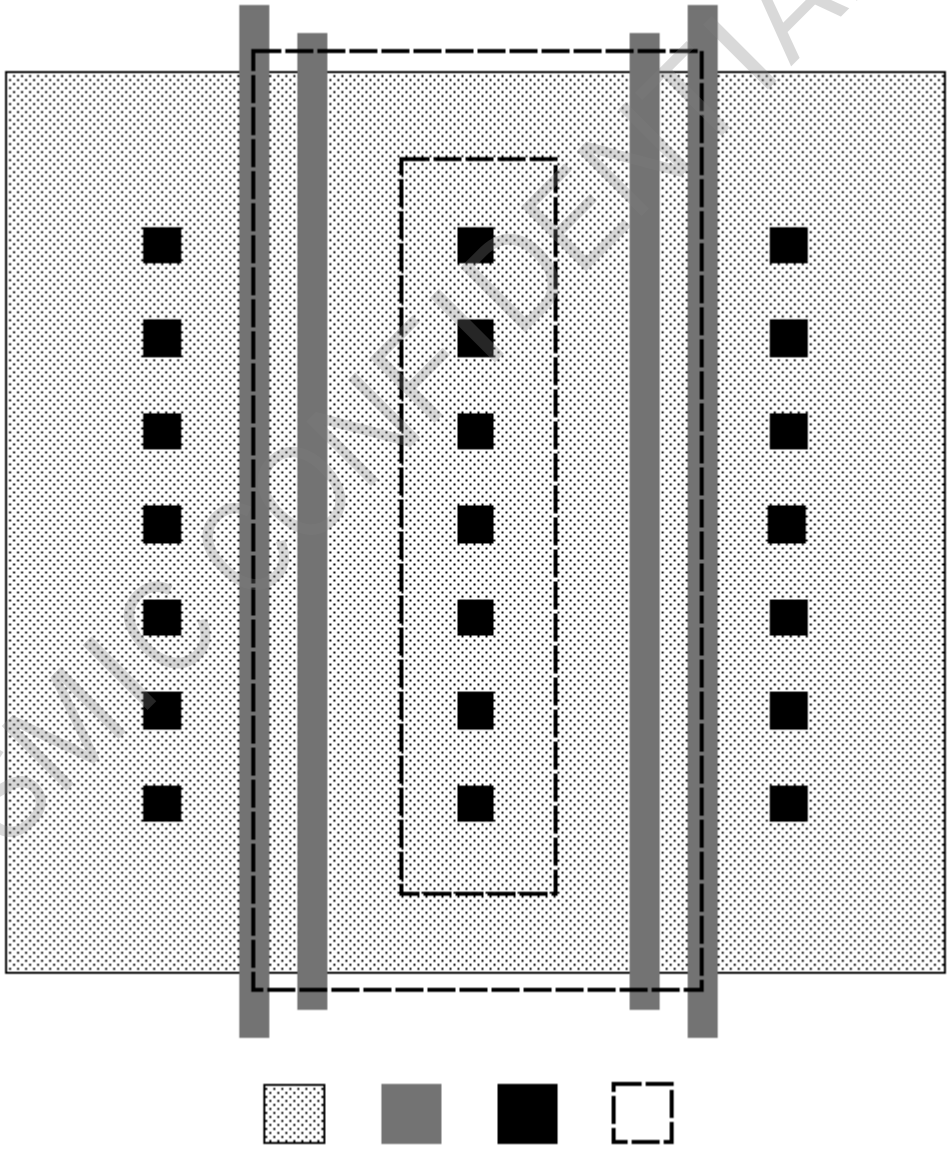
7.3.7.2 Fig. 3 ESD Protection Scheme



7.3.7.2 Fig.4 NMOS/PMOS I/O for ESD Protection with two layout styles of SAB



7.3.7.2 Fig. 5 HV Tolerant 2.5/3.3V I/O ESD protection using cascoded NMOS



7.3.7.2 Fig.6 Cascoded NMOS for HV Tolerant I/O (two layout styles of SAB as Fig.4 are allowed)

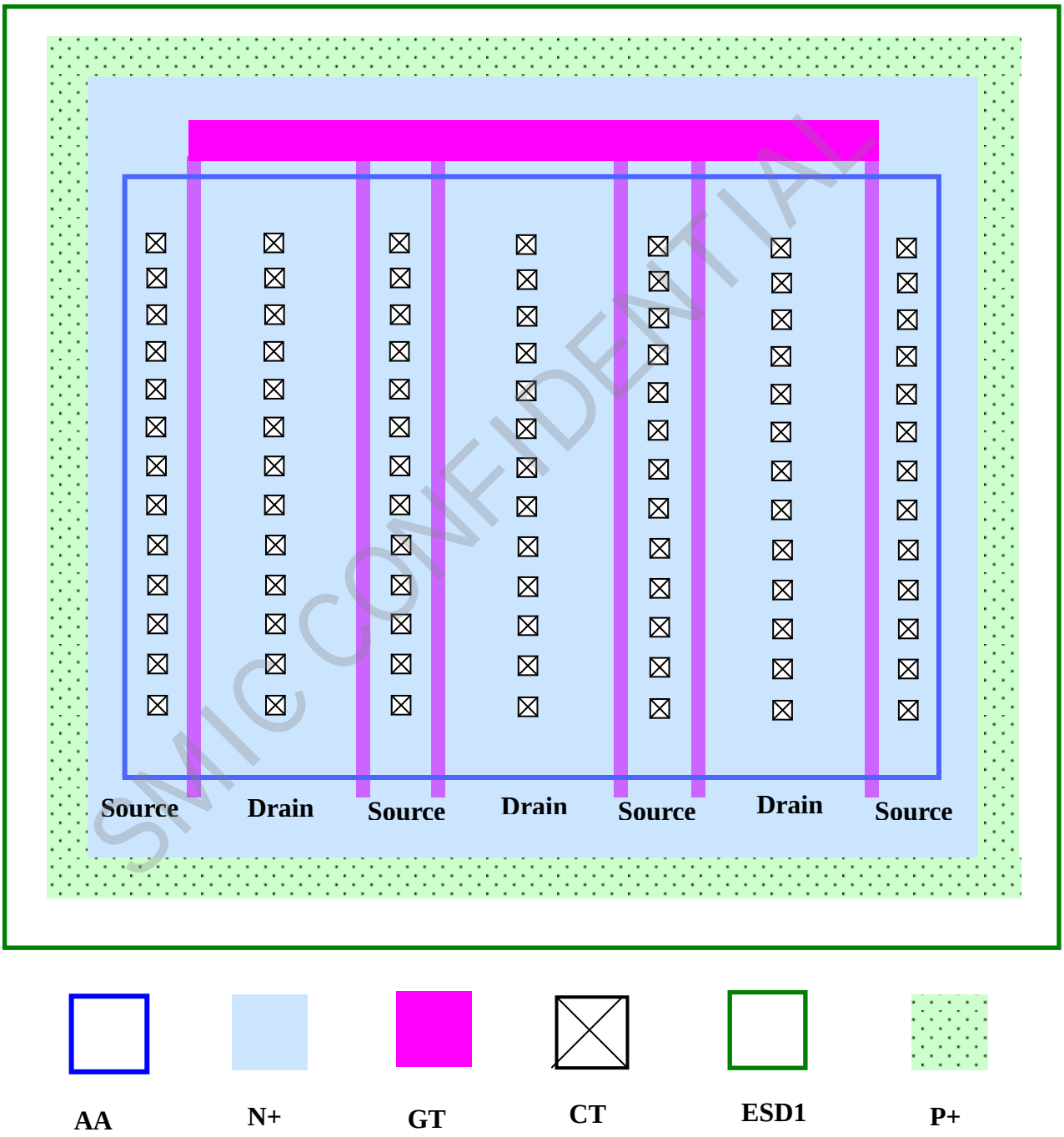
7.3.7.3 ESD1 implant layer rules

ESD1 implant layer is an optional layer to define ESD implant location for ESD NMOS to improve ESD performance. There are two approaches for ESD1 layout drawing and mask layer generation. Design rule for the two approaches is separated. There are DRC switch for two approaches, ESD1_A(DRC turn on by default) and ESD1_B(DRC turn off by default), is set for these two approaches respectively.

- **Approach A**: SMIC ESD designs follow Approach A , where ESD1 mask is generated with SMIC logic operation formula. In this approach, ESD1 is drawn to cover ESD NMOS. If you apply SMIC ESD IO in your design, please follow approach A and must use SMIC logic operation formula for ESD1 mask tape out.
- **Approach B**: ESD1 is a pure drawing layer for mask tape out. No logic operation formula is needed for ESD1 mask tape out. If SMIC ESD IO will not be adopted in the design, you can follow approach B for ESD1 layout design.

7.3.7.3.1 ESD1 implant rules for ESD1_Approach_A:

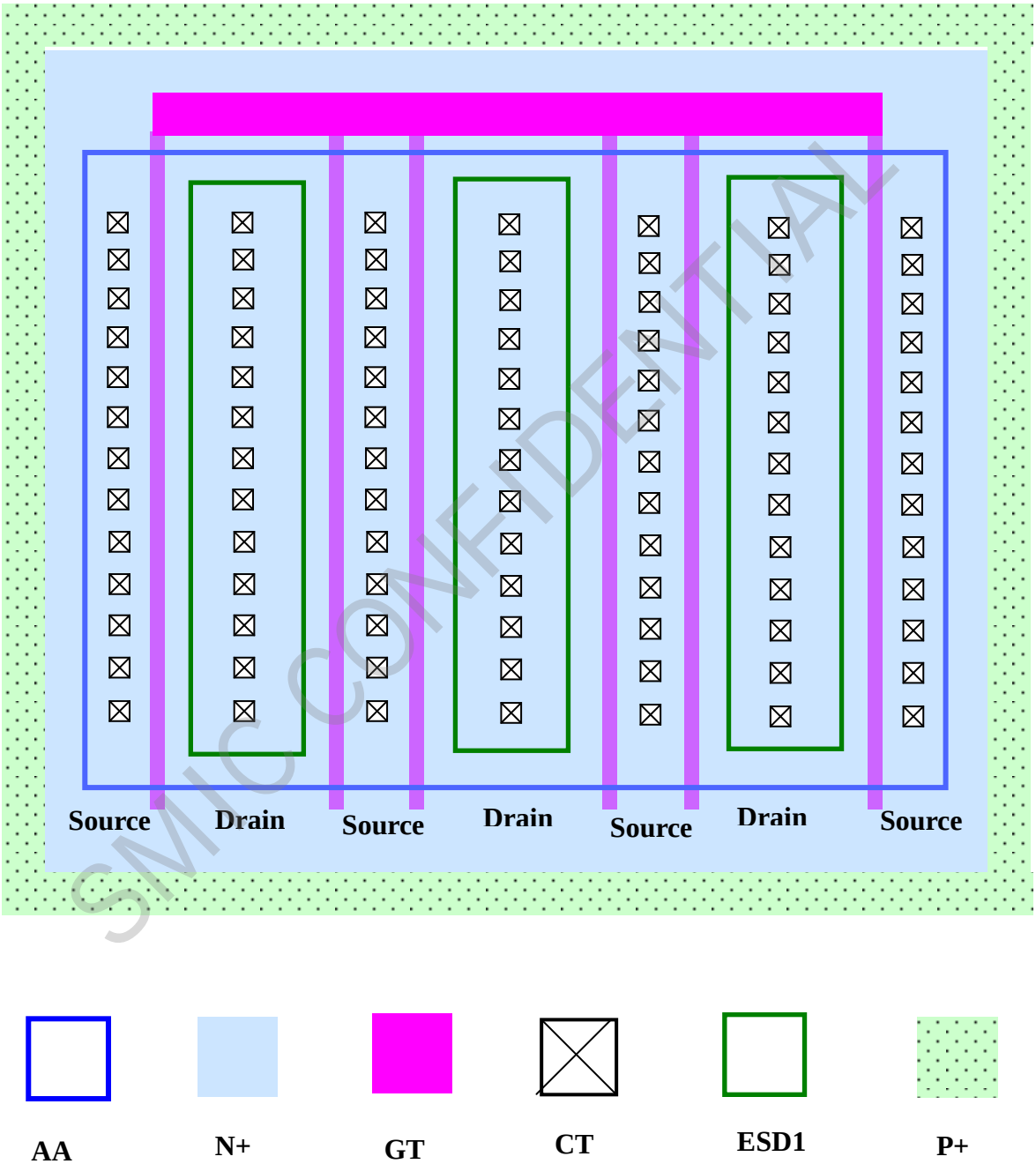
Rule Number	Description	Operation	Design Value	Unit
ESD1_A.0[NC]	It is strongly recommended to adopt SMIC standard ESD IO. If customer plans to adopt their own ESD IO instead of SMIC ESD IO in the design, please designer must contact SMIC for risk assessment before tape out			
ESD1_A.1	ESD1 width.	≥	0.4	um
ESD1_A.2	Space between two ESD1s. Merge if space is less than this value.	≥	0.4	um
ESD1_A.3	ESD1 area.	≥	1	um^2
ESD1_A.4	(Purposely blank)			
ESD1_A.5	N+AA must be fully enclosed by ESD1	≥	0	um
ESD1_A.6[NC]	ESD.8[G] and ESD.22[G] (ESD.22a[G] or ESD.22b[G]) must be strictly followed to generate correct ESD1 implant pattern with SMIC logic operation.			
ESD1_A.7[NC]	If SMIC IP ESD or 3rd party IP ESD applied in customer's chip, need to follow ESD1_Approach_A to drawing ESD1 layer.			



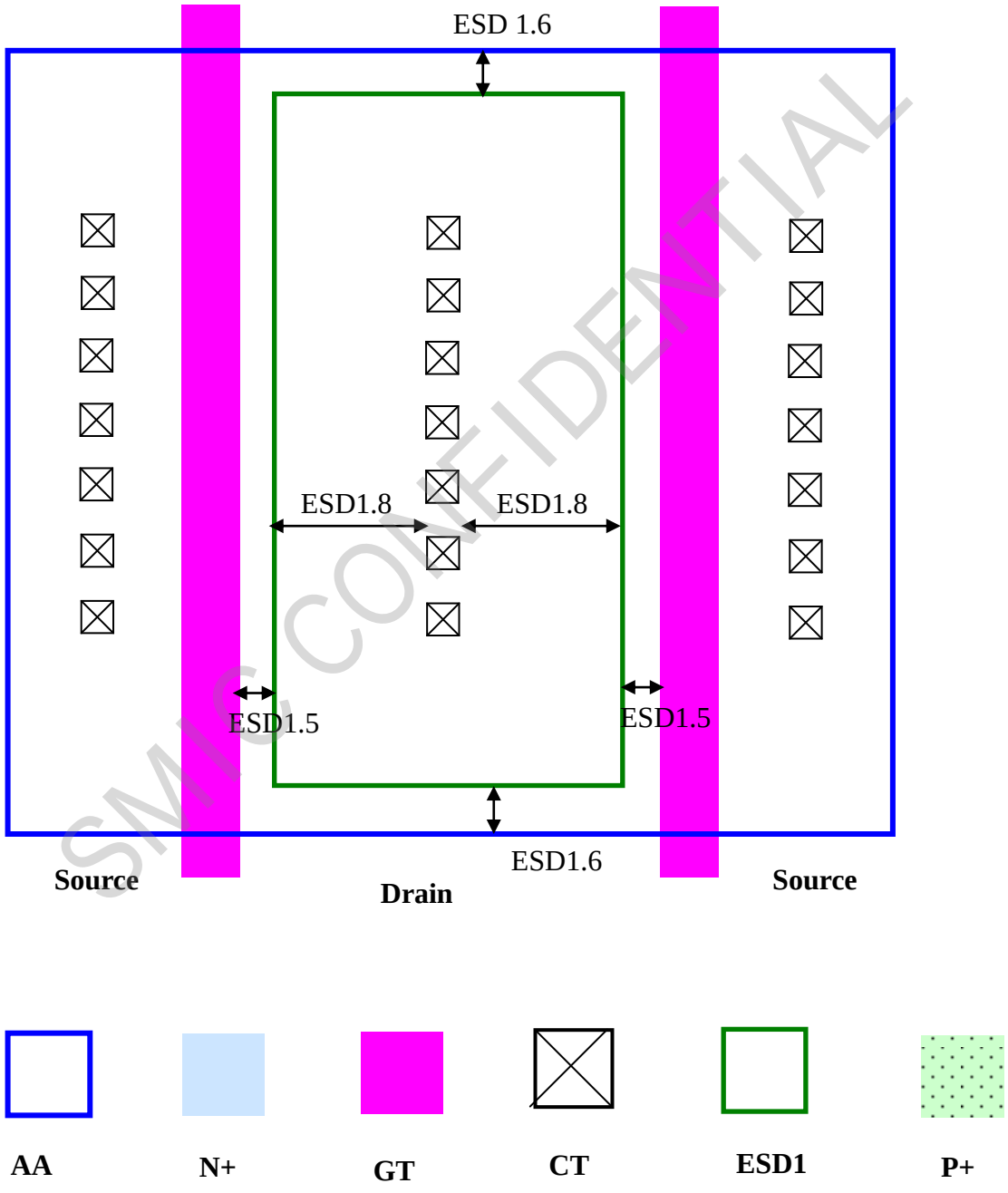
7.3.7.3 Fig. 1 ESD Implant drawing for ESD1_Approach_A.

7.3.7.3.2 ESD1 implant rules for ESD1_Approach_B:

Rule Number	Description	Operation	Design Value	Unit
ESD1_B.0[NC]	It is strongly recommended to adopt SMIC standard ESD IO, If customer plans to adopt their own ESD IO instead of SMIC ESD IO in the design, please designer must contact SMIC for risk assessment before tape out			
ESD1_B.1	ESD1 width.	≥	0.4	um
ESD1_B.2	Space between two ESD1s. Merge if space is less than this value.	≥	0.4	um
ESD1_B.3	ESD1 area.	≥	1	um^2
ESD1_B.4	(Purposely blank)			
ESD1_B.5	Space between an ESD1 and an N-channel gate, ESD1 cannot butt gate. (7.3.7.3 Fig. 3)	≥	0.4	um
ESD1_B.6	ESD1 must be enclosed by AA at least. (7.3.7.3 Fig. 3)	≥	0.2	um
ESD1_B.7	ESD1 is not allowed to overlap with SP.			
ESD1_B.8	ESD1 enclosure of CT (CT must be fully enclosed by (ESD1 AND ESDIO2)) on AA (excluding pick up AA); (7.3.7.3 Fig. 3)	≥	0.4	um



7.3.7.3 Fig. 2 ESD Implant drawing for ESD_Approach_B.



7.3.7.3 Fig. 3 ESD1 Implant rules for ESD_Approach_B

7.3.8 Latch Up Prevention Layout Guidelines

7.3.8.1. Definition of nomenclature in latch up guidelines

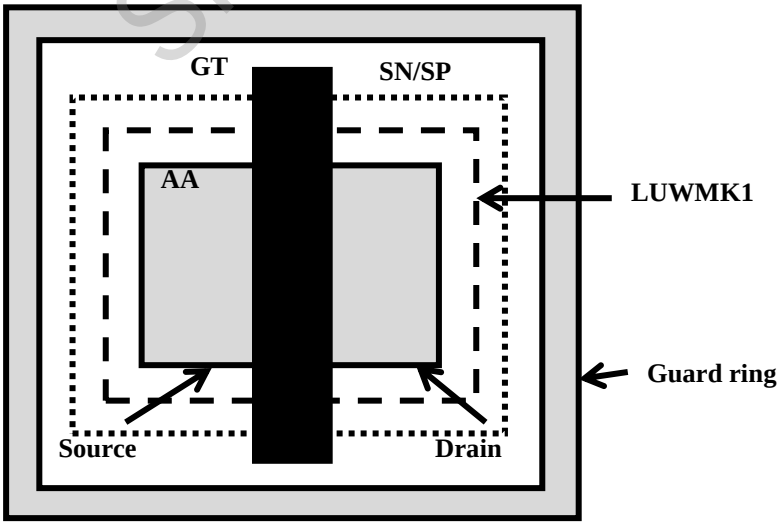
Name	Definitions
I/O pads	Pads except Vdd pad , Vss pad
Power Pads	Vdd pad, Vss pad
Guard-ring	Complete un-broken ring-type AA and M1 with CT as many as possible, connected to Vdd or Vss
P+ guard-ring	Complete un-broken ring-type (SP AND AA) and M1 with CT as many as possible, connected to Vss.
N+ guard-ring	Complete un-broken ring-type (SN AND AA) and M1 with CT as many as possible, connected to Vdd.
AA injector	Any AA directly connected to I/O pad, ex. MOS, diode, AA resistor, and well resistor directly connected to I/O pad.
P+ injector	((SP AND AA) NOT GT) directly connected to I/O pad
N+ injector	((SN AND AA) NOT GT) directly connected to I/O pad

7.3.8.2. Definition of Latch up Dummy Layer

LUWMK1 (131;177) is a dummy layer for designer to waive latch up rules (LU.1~LU.3)

Note:

1) DRC will not check the area which is blocked by LUWMK1.
2) It will have risk if designer draw this layer to exempt latch up rule check without silicon proven of package level latch up test.
3) This layer is for DRC use, not a tapeout required CAD layer.
4) Designer need to follow the following guidelines to draw LUWMK1.
   Draw LUWMK1 to fully cover AA injector, including the source, gate, drain, diode and resistor, but not necessarily to cover well pickup and guard-ring.



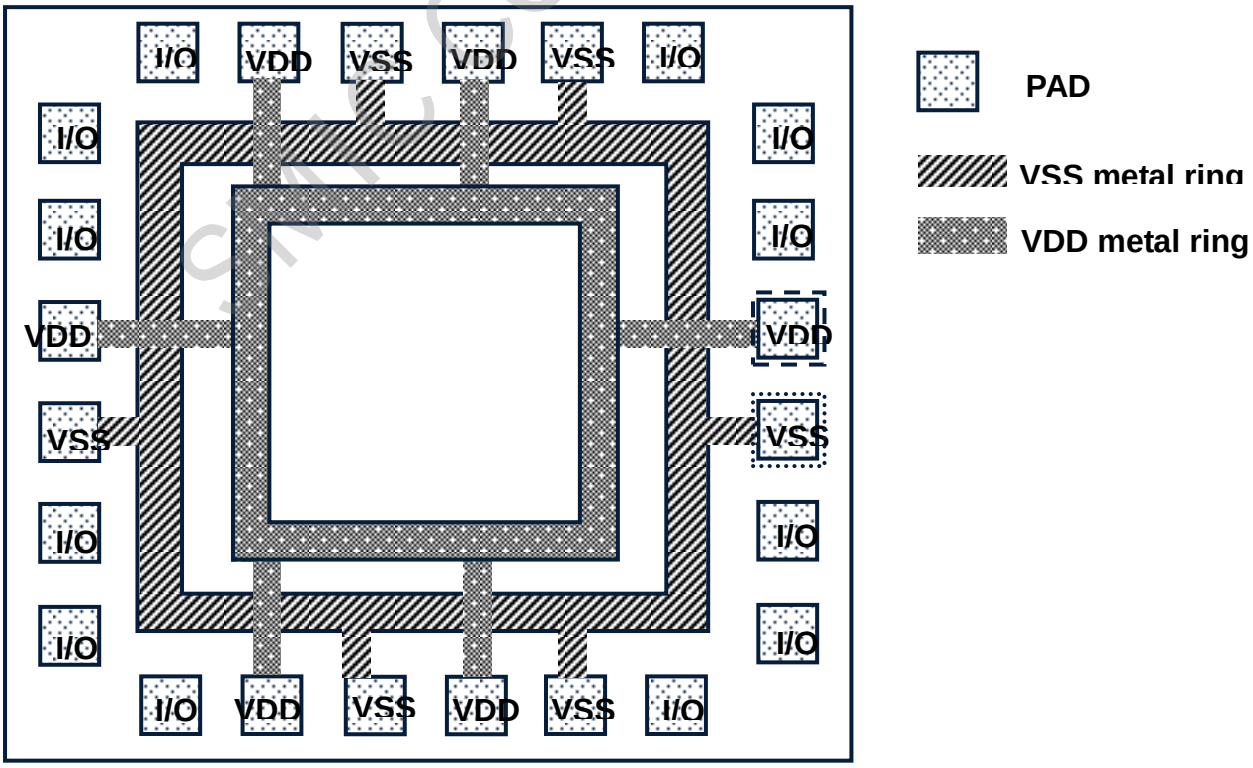
7.3.8.3 DRC use the following features to check the connectivity:

1) The connectivity is formed by metal, via, ALPA, PA, MD and MTT2.
2) If resistors including AA resistor, poly resistor, well resistor are between PAD and AA injector, the connection is broken.
3) The switch of CONNECT_ALL_RESISTOR (to connect AA resistor, poly resistor, well resistor between PAD and AA injector) can control the connectivity of resistor. This switch is off by default.
4) DRC runset provides the following options for designer's control.

Option	Turn on CONNECT_ALL_RESISTOR
A	No (default)
B	Yes

7.3.8.4 DRC uses the following features to identify the Power PAD and I/O PAD.

1) DRC will recognize the PAD by PA layer according to the connectivity defined in 7.3.8.3.
2) Recognize Power PAD by checking the PAD with VDDMK1(131;175) and VSSMK1(131;176).
   VDDMK1 (131;175): Marking layer for Power (Vdd) PAD for DRC use
   VSSMK1 (131;176): Marking layer for Power (Vss) PAD for DRC use
3) Recognize Power PAD with the label of top level text using any metal layer. This function is optional when VDDMK1 and VSSMK1 are not drawn by designer.
   a. Control by the switch of #DEFINE_PAD_BY_TEXT. The switch is turn on by default.
   b. Default Power text name are "?VDD?","?VCC?", "?VSS?","?GND?".
4) Except for the recognized Power PAD, all the other pads are defined as I/O PAD.



Rules Number	DESCRIPTION	Operation	Layout Value	Unit
LU.1[G]	Guard ring should be used to surround AA injector or a group of AA injectors which are connected to an I/O pad. N+ injector must be surrounded by a P+ guard-ring. P+ injector must be surrounded by a N+ guard-ring.			
LU.2[G]	Guard-ring width for AA injector connected to an I/O pad.	≥	0.5	μm
LU.3[G]	LU.3a-LU.3d define minimum space (S1) between NMOS and PMOS with either one of NMOS or PMOS AA connected to I/O pad. (Fig. 7.3.8-1)			
LU.3a[G]	For core N/PMOS AA connected to an I/O pad Spacing between NMOS and PMOS	≥	3	μm
LU.3b[G]	For 2.5V N/PMOS AA connected to an I/O pad Spacing between 2.5V NMOS and 2.5V/Core PMOS and Spacing between 2.5V PMOS and 2.5V/Core NMOS	≥	5	μm
LU.3c[G]	For 3.3V N/PMOS AA connected to an I/O pad Spacing between 3.3V NMOS and 3.3V/Core PMOS and Spacing between 3.3V PMOS and 3.3V/Core NMOS	≥	8	μm
LU.3d[G]	For 5V tolerant N/PMOS (covered by ESD5V mark layer) connected to an I/O pad Spacing between 5V NMOS and 5V/core PMOS and Spacing between 5V PMOS and 5V/core NMOS	≥	15	um
LU.4[G]	Maximum space (S2) from any point within the Source/Drain region to the nearest pickup AA region inside the same well for I/O and internal circuits. (Fig. 7.3.8-2) For native device, DRC check the pickup AA inside the PSUB butted PW area, and PW is still treated as connection by substrate even one NW ring inserted.	≤	35	μm
LU.5[NC]	Minimum space (S3) between I/O circuit and internal circuit region. (Fig. 7.3.8-3)	≥	15	μm

LU.6[NC]	All the guard rings and pickups should be connected to VDD/VSS with low series resistance. Contacts and Via's should be used as many as possible.			

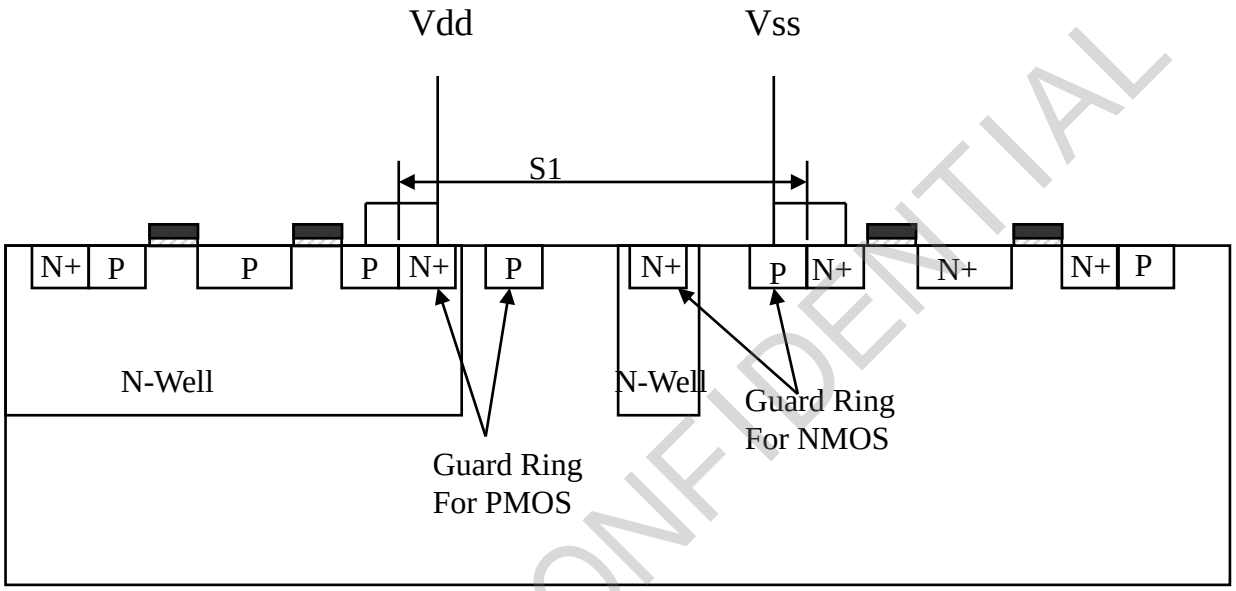


Fig. 7.3.8-1 **space (S1) between NMOS and PMOS connected to I/O pad**

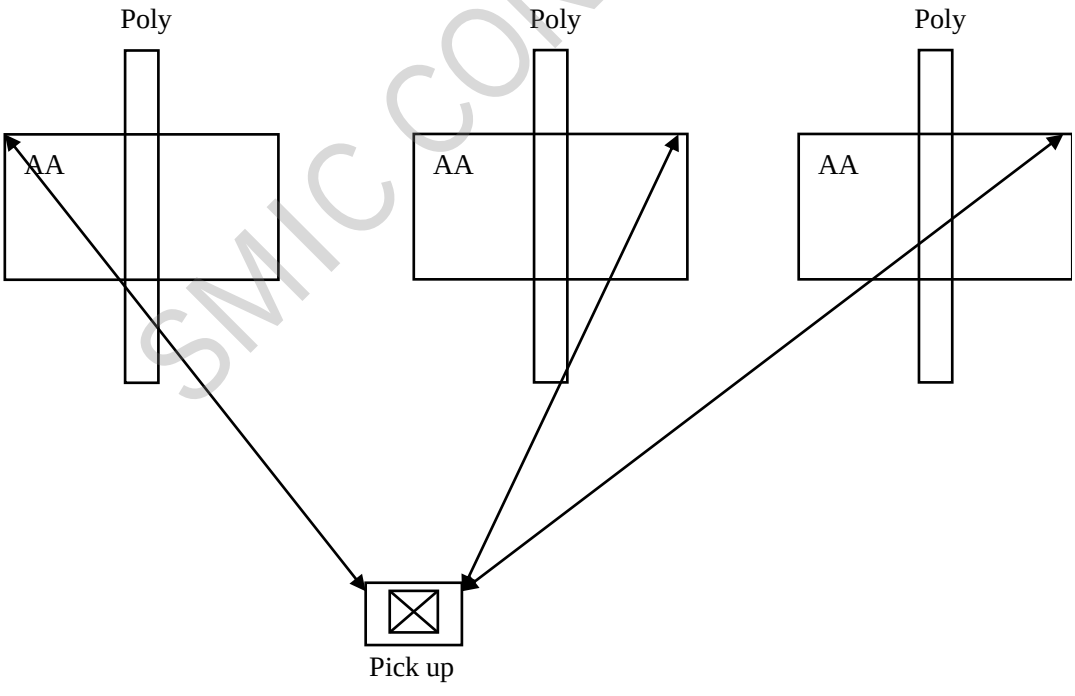


Fig. 7.3.8-2 **Space (S2) between pickup AA to MOS AA**

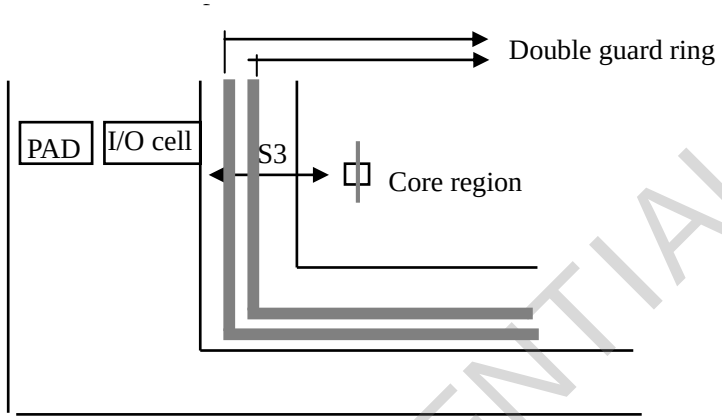


Fig. 7.3.8-3 **Space (S3) I/O circuit to internal circuit**

7.3.9 MOM device layout guideline

MOM(metal oxide metal) capacitor is based on the capacitance between parallel same layer metal lines and different layer metal lines

MOMDMY(211;1) is a mark layer for MOM region, including terminal and capacitor area

MOMMKn(211;11~211;18) is a mark layer to identify the MOM region, only enclose finger area.

Recommend designer to use the MOM provided by SMIC PDK to have better characterization prediction and LVS check.

Layer name	GDS No	Data Type	Description
MOMDMY	211	1	LVS marking layer to identify MOM device
MOMMK1	211	11	DRC marking layer to identify M1 MOM region
MOMMK2	211	12	DRC marking layer to identify M2 MOM region
MOMMK3	211	13	DRC marking layer to identify M3 MOM region
MOMMK4	211	14	DRC marking layer to identify M4 MOM region
MOMMK5	211	15	DRC marking layer to identify M5 MOM region
MOMMK6	211	16	DRC marking layer to identify M6 MOM region
MOMMK7	211	17	DRC marking layer to identify M7 MOM region

Rules number	Description	Operation	Design Value	Unit
MOM.1[G][NC]	Use symmetrical dummy metal around the matched pairs of MOM cells instead of auto inserted dummy.			
MOM.2[G][NC]	Active device underneath or above MOM cell should be put into couple capacitance consideration in design.			
MOM.3[G][NC]	SMIC dummy insertion script does not block out MOM area. Designer should add related dummy block layers.			
MOM.4[G]	MOMDMY and MOMMKn layers are must for MOM device DRC checking is based on the label text by MOMDMY layer. Possible label texts and related MOMMKn follow the Table-1.DRC need flag the stack MOM structure.			
MOM.5[G]	It is not allowed: 1) V1 in MOMMK1 2) Vn/Vn-1 in MOMMKn (n=2~7), whereVn-1 is the via underneath Mn, and Vn is the via above Mn. Vn can be inter-via or TV1 or TV2.			
MOM.6[G]	The space between (Mn AND MOMMKn AND MOMDMY) and Vn /Vn-1 (n=1~7) outside of MOMDMY, whereVn-1 is the via underneath Mn, and Vn is the via above Mn. Vn can be inter-via or TV1 or TV2.	≥	0.21	um

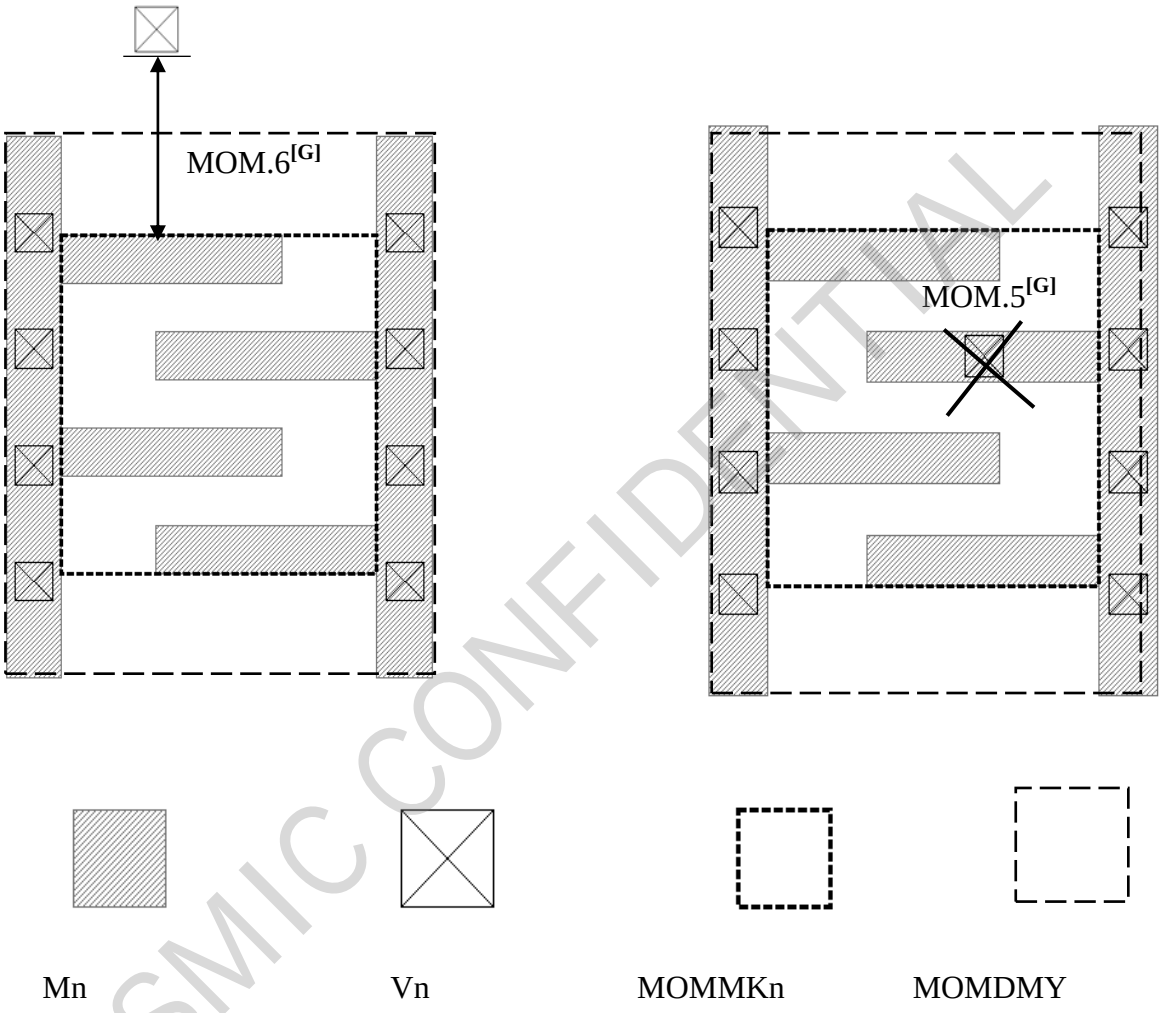


Table1

MOM Label	Marking Layers
momcap12	MOMMK1, MOMMK2
momcap13	MOMMK1~ MOMMK3
momcap14	MOMMK1~ MOMMK4
momcap15	MOMMK1~ MOMMK5
momcap16	MOMMK1~ MOMMK6
momcap17	MOMMK1~ MOMMK7
momcap23	MOMMK2, MOMMK3
momcap24	MOMMK2~ MOMMK4
momcap25	MOMMK2~ MOMMK5
momcap26	MOMMK2~ MOMMK6
momcap27	MOMMK2~ MOMMK7
momcap34	MOMMK3, MOMMK4
momcap35	MOMMK3~ MOMMK5
momcap36	MOMMK3~ MOMMK6
momcap37	MOMMK3~ MOMMK7
momcap45	MOMMK4~ MOMMK5
momcap46	MOMMK4~ MOMMK6
momcap47	MOMMK4~ MOMMK7
momcap56	MOMMK5, MOMMK6
momcap57	MOMMK5~ MOMMK7
momcap67	MOMMK6, MOMMK7

7.3.10 Seal Ring Guideline

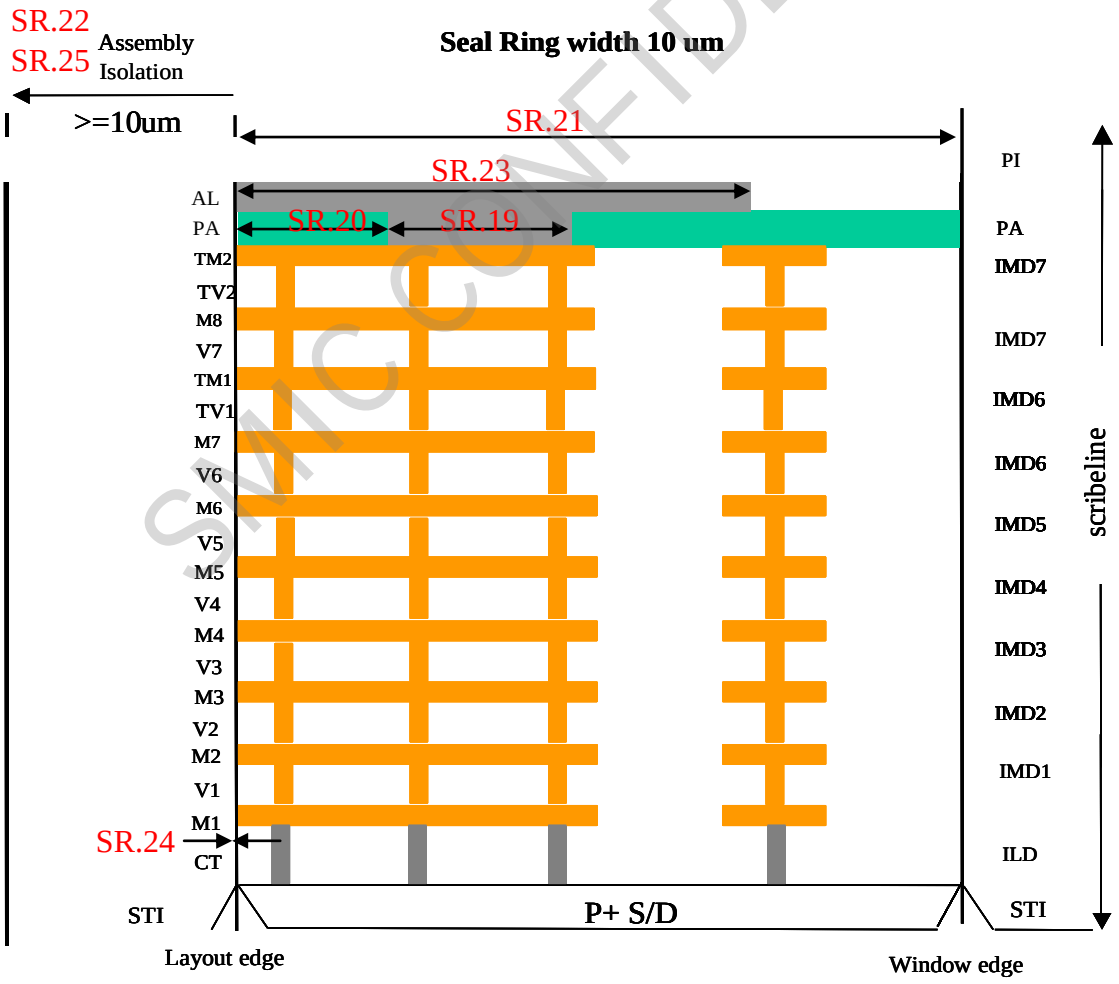
7.3.10.1 Seal Ring introduction

Seal ring is the structure to protect circuit from mechanical damage during die saw. Use of the scribe line seal ring to protect test chip is recommended. A continuous scribe line and seal ring is required on all sides of a chip that is intended for dicing and packaging. A completed seal ring structure includes metal guard rings, die corner stress relief patterns and assembly isolation areas.

The seal ring provides both a low resistance path to ground for surge currents and a metal seal against ionic contaminations. 45 degree bend is expected around every die corner. Multiple stacked via/Metal trench are considered to suppress crack risk during dicing saw operation in assembly.

Fig.-1 shows the typical structure of scribe line seal ring. (All units are in um)

Fig.1 Cross-section schematic of 0.13um 8-metal seal ring scheme



7.3.10.2 Seal Ring Design Guideline

The dimensions given in Figs. 1-5 and in the tables of this section are used by SMIC. The numbers in the table1 are gds drawn dimension. The numbers in the table2 are on mask size in which OPC and mask bias operation have been taken into consideration.

A. Typical structure of Seal rings

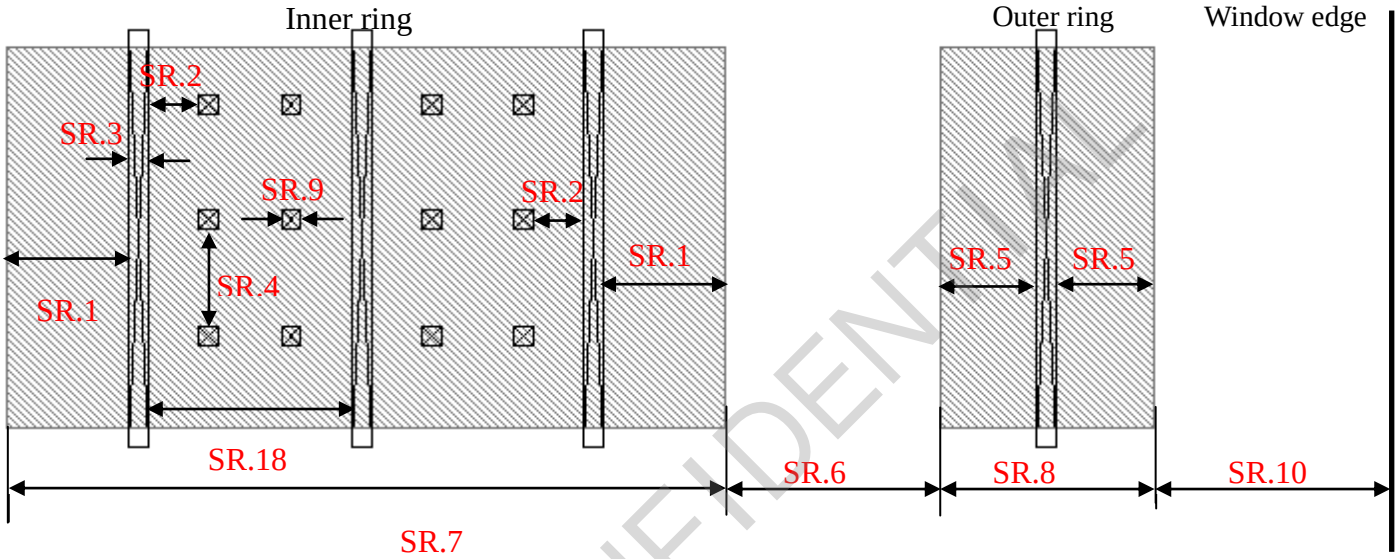
Continuous metal rings are required on all sides of a chip that is intended for dicing and packaging. A 45 degree bending is expected around every die corner. Multiple stacked via/metal trench patterns are used to suppress crack risk during dicing saw operation in assembly. Refer to Fig.1 and Fig.2 for the schematics. For products having less than 8 metal layers, please skip the metal and via layers those are not used.

It is recommended that scribe line seal and scribe guard ring rules follow the schematic diagram and table below. Assembly isolation depends on the capability of assembly house. 10μm is for reference.

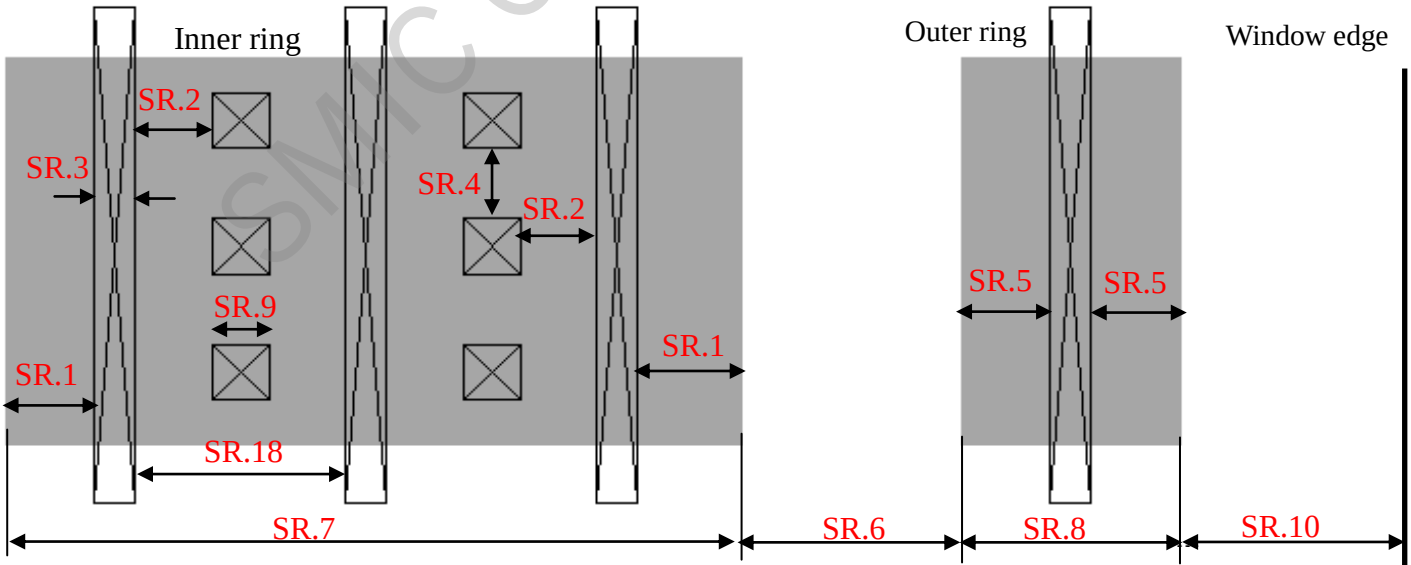
B. Die corner stress relief pattern layout

The seal ring corner layout is recommended to manage local stress at each die corner. Metal & via dummy pattern is recommended at each corner of seal ring. The dimension of each segment of the corner layout is given in Fig. 3~4. Same as metal ring parts, there are only AA/SP layers needed under contact layer on die corner stress relief areas.

For those who wish SMIC to apply seal rings for the customers, a separate seal ring corner will be used, since SMIC is not going to change the corner part of customer's original layout. Please refer to Fig.4 shows the schematic of the seal ring corner design for the customers who want SMIC to add the seal rings for them. **In summary, Fig. 4 is SMIC internal standard.**



(a) CT, M1-M6,V1-V5



(b) V7, TM, TV

Figure2 Schematic top view of the seal ring structure

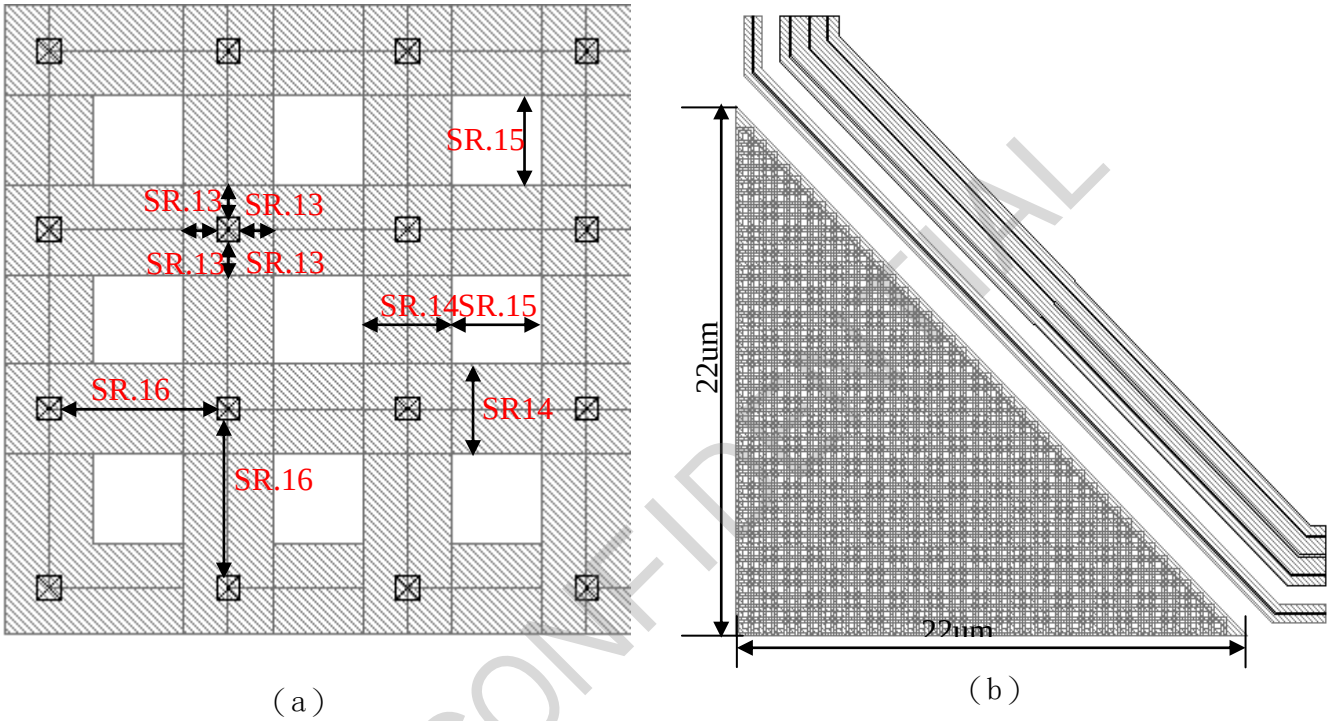


Fig.3 Die corner stress relief structure layout for customer layout (a) for M1~M6/TM, CT, V1~V5/TV (b) zoom in images for the corner area of (a).

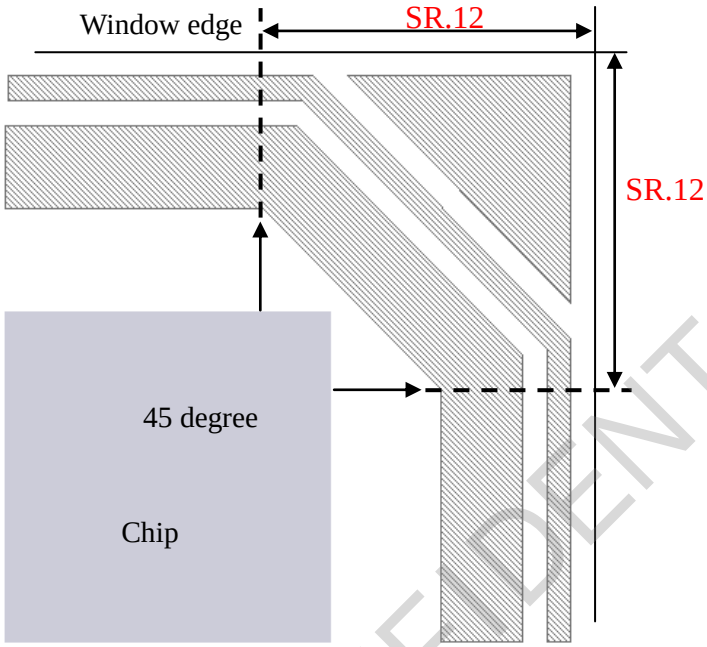


Fig.4 Seal ring corner if applied at SMIC

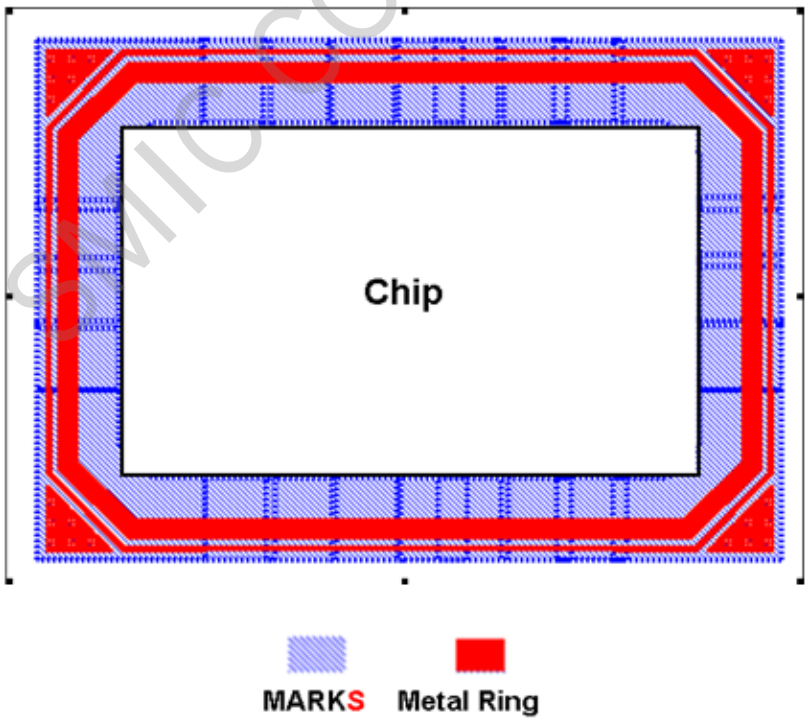


Fig.5 MARKS covered Seal ring area

Table 1(a) Drawn dimension of 0.13um seal ring structure

Rule No.	Description	Operation	Rule value	unit
SR.1a[NC]	Space between inner CT slot and the metal ring edge	≥	0.706	um
SR.1b[NC]	Space between inner Via(V1~V6) slot and the metal ring edge	≥	0.702	um
SR.1c[NC]	Space between inner V7,TV1,TV2 slot and the metal ring edge	≥	0.67	um
SR.2a[NC]	Double column square CT to CT slot distance	=	0.398	um
SR.2b[NC]	Double column square via (V1-V6) to via slot distance	=	0.377	um
SR.2c[NC]	V7, TV1, TV2 to use single column of square vias. V7/TV1/TV2 to via slot distance.	≥	0.555	um
SR.3a[NC]	Contact slot width	=	0.167	um
SR.3b[NC]	V1-V6 slot width	=	0.175	um
SR.3c[NC]	V7, TV1, TV2 slot width	=	0.21	um
SR.4a[NC]	Space between square CT along the direction of seal ring	=	0.653	um
SR.4b[NC]	Space between square via(V1~V6) along the direction of seal ring	=	0.62	um
SR.4c[NC]	Space between square V7/TV1/TV2 along the direction of seal ring	=	0.45	um
SR.5a[NC]	Space between outer ring CT slot and the metal ring edge	≥	0.66	um
SR.5b[NC]	Space between outer ring via1~via6 slot and the metal ring edge	≥	0.66	um
SR.5c[NC]	Space between outer ring V7/TV1/TV2 slot and the metal ring edge	≥	0.64	um
SR.6[NC]	Space between inner and outer metal ring	=	1.5	um
SR.7[NC]	Metal width of inner ring	=	5.0	um
SR.8[NC]	Metal width of outer ring	=	1.5	um
SR.9a[NC]	Square CT size	=	0.187	um
SR.9b[NC]	Square V1-V6 size	=	0.221	um

Rule No.	Description	Operation	Rule value	unit
SR.9c[NC]	Square V7, TV1, TV2 size	=	0.39	um
SR.10[NC]	Space between outer metal ring to window edge	=	2.0	um
SR.11a[NC]	Distance from window edges to the point that inner ring start to bend 45 degree at corners. This rule is for customer layout and for die size with at least one side <10 mm	=	50	um
SR.11b[NC]	Distance from window edges to the point that inner ring start to bend 45 degree at corners. This rule is for customer layout and for die size with no one side < 10 mm.	=	70	um
SR.12[NC]	Distance from window edges to the point that inner ring start to bend 45 degree at corners. This rule is for SMIC to apply seal rings for customer.	=	24	um
SR.13a[NC]	Space between square CT and M1 edge in the die corner dummy relief area.	=	0.406	um
SR.13b[NC]	Space between square via1~via6 and inter-metal edge in the die corner dummy relief area.	=	0.39	um
SR.13c[NC]	Space between square via7/TV and TM edge in the die corner dummy relief area.	≥	0.305	um
SR.14a[NC]	Metal width of die corner dummy pattern for M1 to M7.	=	1.0	um
SR.14b[NC]	Top Metal width of die corner dummy pattern.	=	2.0	um
SR.15a[NC]	Space between metal of die corner dummy pattern for M1 to M7.	=	1.0	um
SR.15b[NC]	Space between TMs of die corner dummy pattern.	=	2.0	um
SR.16a[NC]	CT distance from each other in die corner dummy area.	=	0.813	um
SR.16b[NC]	Via distance from each other in die corner dummy area.	=	0.779	um
SR.16c[NC]	TV1/TV2 distance from each other in die corner dummy area.	=	0.61	um
SR.17[NC]	Space between inner metal ring and layout edge.	=	0	um
SR.18a[NC]	Space between inner CT slot	≥	1.543	um
SR.18b[NC]	Space between inner V1~V6 slot	≥	1.535	um

Rule No.	Description	Operation	Rule value	unit
SR.18c[NC]	Space between inner V7,TV1,TV2 slot	≥	1.5	um
SR.19[NC]	Passivation slot width.	=	2.2	um
SR.20[NC]	Space between passivation slot and layout edge.	=	2.5	um
SR.21[NC]	Total seal ring width	=	10	um
SR.22[NC]	Space between seal ring and chip (assembly isolation)	=	10	um
SR.23[NC]	AL ring width.	=	7.2	um
SR.24[NC]	Space between AL ring and layout edge.	=	0	um
SR.25[NC]	Assembly isolation between active AA/GT/METAL/Al RDL patterns and internal metal ring edge.	=	10	um

Table 1(b) Drawn dimension of 0.11um seal ring structure

Rule No.	Description	Operation	Rule value	unit
SR.1a[NC]	Space between inner CT slot and the metal ring edge	≥	0.784	um
SR.1b[NC]	Space between inner Via(V1~V6) slot and the metal ring edge	≥	0.779	um
SR.1c[NC]	Space between inner V7,TV1,TV2 slot and the metal ring edge	≥	0.744	um
SR.2a[NC]	Double column square CT to CT slot distance	=	0.441	um
SR.2b[NC]	Double column square via (V1-V6) to via slot distance	=	0.418	um
SR.2c[NC]	V7, TV1, TV2 to use single column of square vias. V7/TV1/TV2 to via slot distance.	≥	0.616	um
SR.3a[NC]	Contact slot width	=	0.185	um
SR.3b[NC]	V1-V6 slot width	=	0.194	um
SR.3c[NC]	V7, TV1, TV2 slot width	=	0.233	um
SR.4a[NC]	Space between square CT along the direction of seal ring	=	0.724	um
SR.4b[NC]	Space between square via(V1~V6) along the direction of seal ring	=	0.688	um

Rule No.	Description	Operation	Rule value	unit
SR.4c[NC]	Space between square V7/TV1/TV2 along the direction of seal ring	=	0.50	um
SR.5a[NC]	Space between outer ring CT slot and the metal ring edge	≥	0.734	um
SR.5b[NC]	Space between outer ring via1~via6 slot and the metal ring edge	≥	0.735	um
SR.5c[NC]	Space between outer ring V7/TV1/TV2 slot and the metal ring edge	≥	0.71	um
SR.6[NC]	Space between inner and outer metal ring	=	1.665	um
SR.7[NC]	Metal width of inner ring	=	5.55	um
SR.8[NC]	Metal width of outer ring	=	1.665	um
SR.9a[NC]	Square CT size	=	0.208	um
SR.9b[NC]	Square V1-V6 size	=	0.245	um
SR.9c[NC]	Square V7, TV1, TV2 size	=	0.433	um
SR.10[NC]	Space between outer metal ring to window edge	=	2.22	um
SR.11a[NC]	Distance from window edges to the point that inner ring start to bend 45 degree at corners. This rule is for customer layout and for die size with at least one side <10 mm	=	50	um
SR.11b[NC]	Distance from window edges to the point that inner ring start to bend 45 degree at corners. This rule is for customer layout and for die size with no one side < 10 mm.	=	70	um
SR.12[NC]	Distance from window edges to the point that inner ring start to bend 45 degree at corners. This rule is for SMIC to apply seal rings for customer.	=	24	um
SR.13a[NC]	Space between square CT and M1 edge in the die corner dummy relief area.	=	0.451	um
SR.13b[NC]	Space between square via1~via6 and inter-metal edge in the die corner dummy relief area.	=	0.432	um
SR.13c[NC]	Space between square via7/TV and TM edge in the die corner dummy relief area.	≥	0.339	um

Rule No.	Description	Operation	Rule value	unit
SR.14a[NC]	Metal width of die corner dummy pattern for M1 to M7.	=	1.11	um
SR.14b[NC]	Top Metal width of die corner dummy pattern.	=	2.22	um
SR.15a[NC]	Space between metal of die corner dummy pattern for M1 to M7.	=	1.11	um
SR.15b[NC]	Space between TMs of die corner dummy pattern.	=	2.22	um
SR.16a[NC]	CT distance from each other in die corner dummy area.	=	0.902	um
SR.16b[NC]	Via distance from each other in die corner dummy area.	=	0.865	um
SR.16c[NC]	TV1/TV2 distance from each other in die corner dummy area.	=	0.678	um
SR.17[NC]	Space between inner metal ring and layout edge.	=	0	um
SR.18a[NC]	Space between inner CT slot	≥	1.713	um
SR.18b[NC]	Space between inner V1~V6 slot	≥	1.703	um
SR.18c[NC]	Space between inner V7,TV1,TV2 slot	≥	1.665	um
SR.19[NC]	Passivation slot width.	=	2.442	um
SR.20[NC]	Space between passivation slot and layout edge.	=	2.775	um
SR.21[NC]	Total seal ring width	=	11.1	um
SR.22[NC]	Space between seal ring and chip (assembly isolation)	=	11.1	um
SR.23[NC]	AL ring width.	=	7.992	um
SR.24[NC]	Space between AL ring and layout edge.	=	0	um
SR.25[NC]	Assembly isolation between active AA/GT/METAL/Al RDL patterns and internal metal ring edge.	=	11.1	um

Table2 Detailed dimension for 0.13um scribe line guard ring layout.

For detailed dimension of scribe line guard ring layout, please refer to the following table. X=0 defines the inner (die-side) edge of the guard ring structure.

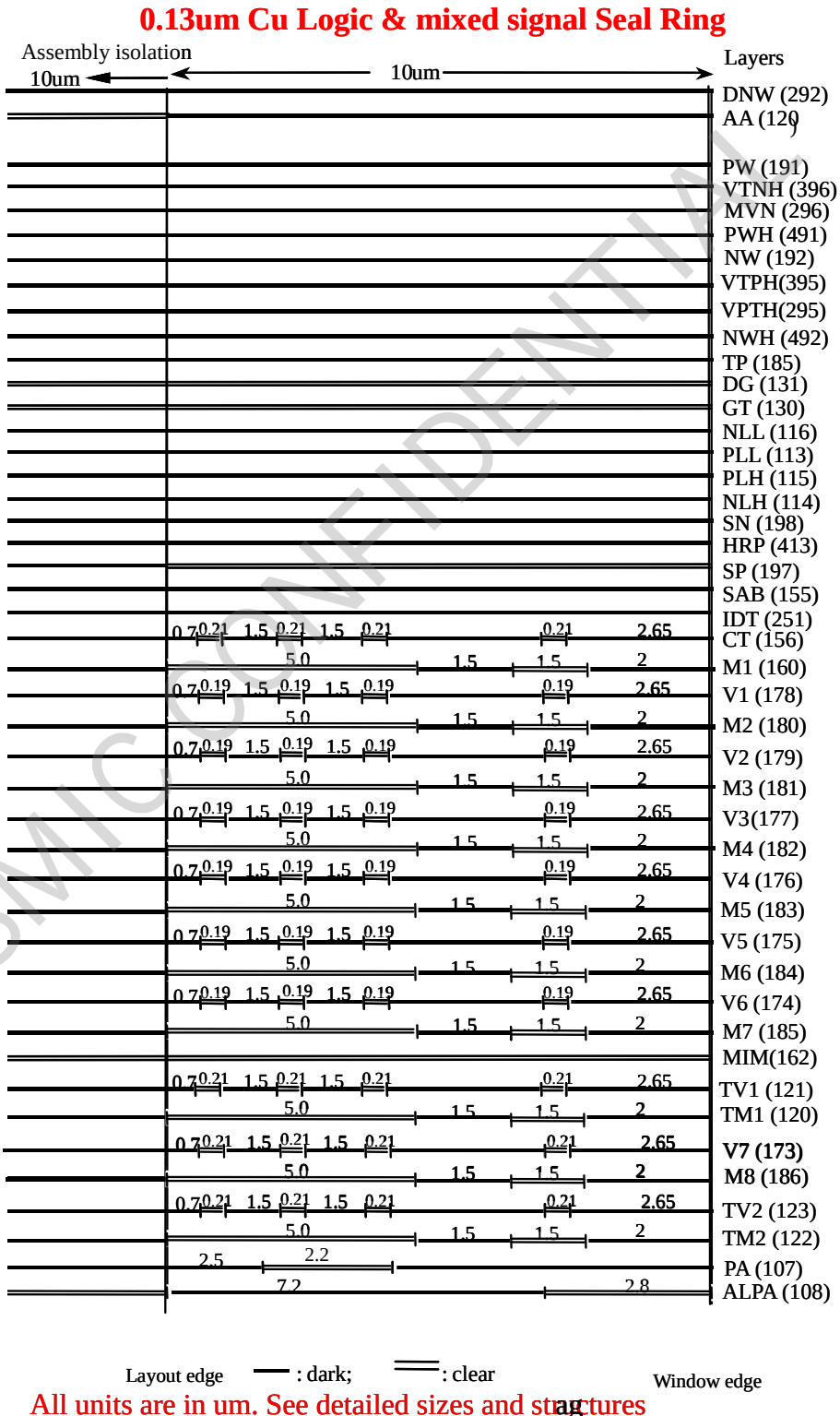
Ring	Assemble Isolation Tone	Starting Coordinate	Ending Coordinate	Size (μm)	Pattern Tone
DNW	D	0.0	10.0	10.0	D
AA	C	0.0	10.0	10.0	D
PW	D	0.0	10.0	10.0	D
VTNH	D	0.0	10.0	10.0	D
MVN	D	0.0	10.0	10.0	D
PWH	D	0.0	10.0	10.0	D
TN	D	0.0	10.0	10.0	D
NW	D	0.0	10.0	10.0	D
VTPH	D	0.0	10.0	10.0	D
MVP	D	0.0	10.0	10.0	D
NWH	D	0.0	10.0	10.0	D
TP	D	0.0	10.0	10.0	D
DG	C	0.0	10.0	10.0	C
GT	C	0.0	10.0	10.0	C
NLL	D	0.0	10.0	10.0	D
PLL	D	0.0	10.0	10.0	D
PLH	D	0.0	10.0	10.0	D
NLH	D	0.0	10.0	10.0	D
SN	D	0.0	10.0	10.0	D
HRP	D	0.0	10.0	10.0	D
SP	D	0.0	10.0	10.0	C
ESD1	D	0.0	10.0	10.0	D
IDT	D	0.0	10.0	10.0	D
SAB	D	0.0	10.0	10.0	D
CT	D	0.7	0.91	0.21	C
CT	D	2.41	2.62	0.21	C
CT	D	4.12	4.33	0.21	C

Ring	Assemble Isolation Tone	Starting Coordinate	Ending Coordinate	Size (μm)	Pattern Tone
CT	D	7.14	7.35	0.21	C
Metal 1	D	0.00	5.0	5.0	C
Metal 1	D	6.5	8.0	1.5	C
Via 1	D	0.7	0.89	0.19	C
Via 1	D	2.39	2.58	0.19	C
Via 1	D	4.08	4.27	0.19	C
Via 1	D	7.16	7.35	0.19	C
Metal 2	D	0.00	5.0	5.0	C
Metal 2	D	6.5	8.0	1.5	C
Via 2	D	0.7	0.89	0.19	C
Via 2	D	2.39	2.58	0.19	C
Via 2	D	4.08	4.27	0.19	C
Via2	D	7.16	7.35	0.19	C
Metal 3	D	0.00	5.0	5.0	C
Metal 3	D	6.5	8.0	1.5	C
Via 3	D	0.7	0.89	0.19	C
Via 3	D	2.39	2.58	0.19	C
Via 3	D	4.08	4.27	0.19	C
Via 3	D	7.16	7.35	0.19	C
Metal 4	D	0.00	5.0	5.0	C
Metal 4	D	6.5	8.0	1.5	C
Via 4	D	0.7	0.89	0.19	C
Via 4	D	2.39	2.58	0.19	C
Via 4	D	4.08	4.27	0.19	C
Via 4	D	7.16	7.35	0.19	C
Metal 5	D	0.00	5.0	5.0	C
Metal 5	D	6.5	8.0	1.5	C

Ring	Assemble Isolation Tone	Starting Coordinate	Ending Coordinate	Size (μm)	Pattern Tone
Via 5	D	0.7	0.89	0.19	C
Via 5	D	2.39	2.58	0.19	C
Via 5	D	4.08	4.27	0.19	C
Via 5	D	7.16	7.35	0.19	C
Metal 6	D	0.00	5.0	5.0	C
Metal 6	D	6.5	8.0	1.5	C
Via 6	D	0.7	0.89	0.19	C
Via 6	D	2.39	2.58	0.19	C
Via 6	D	4.08	4.27	0.19	C
Via 6	D	7.16	7.35	0.19	C
Metal 7	D	0.00	5.0	5.0	C
Metal 7	D	6.5	8.0	1.5	C
MIM	C	0.00	10.0	10.0	C
TV1	D	0.7	0.91	0.21	C
TV1	D	2.41	2.62	0.21	C
TV1	D	4.12	4.33	0.21	C
TV1	D	7.14	7.35	0.21	C
TM1	D	0.00	5.0	5.0	C
TM1	D	6.5	8.0	1.5	C
Via 7	D	0.7	0.91	0.21	C
Via 7	D	2.41	2.62	0.21	C
Via 7	D	4.12	4.33	0.21	C
Via 7	D	7.14	7.35	0.21	C
Metal 8	D	0.00	5.0	5.0	C
Metal 8	D	6.5	8.0	1.5	C
TV2	D	0.7	0.91	0.21	C
TV2	D	2.41	2.62	0.21	C

Ring	Assemble Isolation Tone	Starting Coordinate	Ending Coordinate	Size (μm)	Pattern Tone
TV2	D	4.12	4.33	0.21	C
TV2	D	7.14	7.35	0.21	C
TM2	D	0.00	5.0	5.0	C
TM2	D	6.5	8.0	1.5	C
PA	D	2.5	4.7	2.2	C
ALPA	C	0.00	7.2	7.2	D
MD	D	0.0	10.0	10.0	D

Fig.5 Schematic of 0.13um seal ring tone definition



All units are in um. See detailed sizes and structures

7.3.10.3 Seal Ring check rule for 0.13um

For Seal-Ring design, please refer to TD-LO13-DR-2002. Use of the scribe line seal ring to protect test chip is recommended. A completed seal ring structure includes metal guard rings, die corner stress relief patterns and assembly isolation areas.

MARKS is the marking layer of seal ring. All of the seal ring region must be blocked by MARKS.

If the Seal Ring is added by designer, the marking layer MARKS must be drawn.

SMIC Maskshop can help to add seal ring structure upon customer's request. If customers draw seal ring by themselves and combine it with main chip, the seal ring layout should not violate general seal ring design rules except special notices. It's strongly recommended designers to follow SMIC seal ring GDS sample structure. If designers use their owned seal ring structure, SMIC can't guarantee the seal ring quality.

Seal ring outer ring definition:

From BORDER layer go inside to check the outermost close metal ring.

1) When the seal ring region doesn't be drawn mark layer (MARKS), the outermost closed metal ring which included all the layout (except dummy relief area) should be checked as seal ring outer ring. If there are patterns (refer BD.1 listed layers) between outer ring and border, the closed metal ring can't be considered as outer ring.

2) When the seal ring region has been drawn mark layer (MARKS), the un-closed ring don't need to be checked as seal ring structure in MARKS blockage region. It needs to exclude seal ring corner region.

Die corner dummy area definition: 22*22um size region.

Rule No.	Description	Operation	Design value	Unit
SRCK.1	Contact slot width	=	0.167	um
SRCK.2	V1-V6 slot width	=	0.175	um
SRCK.3	V7, TV1, TV2 slot width	=	0.21	um
SRCK.4	Space between CT along the direction of seal ring	=	0.653	um
SRCK.5	Space between via(V1~V6) along the direction of seal ring	=	0.62	um
SRCK.6	Space between V7/TV1/TV2 along the direction of seal ring.	=	0.45	um
SRCK.7	Space between inner CT slot and the metal ring edge	≥	0.706	um
SRCK.8	Space between inner Via(V1~V6) slot and the metal ring edge	≥	0.702	um
SRCK.9	Space between inner V7,TV1,TV2 slot and the metal ring edge	≥	0.67	um
SRCK.10	Space between inner CT slot	≥	1.543	um
SRCK.11	Space between inner V1~V6 slot	≥	1.535	um

Rule No.	Description	Operation	Design value	Unit
SRCK.12	Space between inner V7,TV1,TV2 slot	≥	1.5	um
SRCK.13	Space between outer ring CT slot and the metal ring edge	≥	0.661	um
SRCK.14	Space between outer ring via1~via6 slot and the metal ring edge	≥	0.662	um
SRCK.15	Space between outer ring V7/TV1/TV2 slot and the metal ring edge	≥	0.64	um
SRCK.16	CT width and length, DRC waive CT slot pattern with width = 0.167um in seal ring region.	=	0.187	um
SRCK.17	V1-V6 width and length. DRC waive V1-V6 slot pattern with width = 0.175um in seal ring region.	=	0.221	um
SRCK.18	V7, TV1, TV2 width and length. DRC waive V7, TV1, TV2 slot pattern with width = 0.21um in seal ring region.	=	0.39	um
SRCK.19	Space between CT and M1 edge in the die corner dummy relief area	≥	0.406	um
SRCK.20	Space between via1~via6 and inter-metal edge in the die corner dummy relief area	≥	0.389	um
SRCK.21	Space between via7/TV and TM edge in the die corner dummy relief area	≥	0.305	um
SRCK.22	Metal width of die corner dummy pattern for M1 to M7	=	1	um
SRCK.23	Space between metal of die corner dummy pattern for M1 to M7	=	1	um
SRCK.24	Top Metal width of die corner dummy pattern	=	2	um
SRCK.25	Space between TMs of die corner dummy pattern	=	2	um
SRCK.26	CT distance from each other in die corner dummy area	≥	0.813	um
SRCK.27	Via distance from each other in die corner dummy area	≥	0.779	um
SRCK.28	TV1/TV2 distance from each other in die corner dummy area	≥	0.61	um
SRCK.29	Passivation slot width in MARKS covered areas	=	2.2	um
SRCK.30	Space between active AA/GT/METAL/Al RDL patterns and internal metal ring edge assembly isolation.	≥	10	um

Rule No.	Description	Operation	Design value	Unit
SRCK.31	Seal ring must be a close ring. DRC check CT/Metal/Via/Top metal/Top via/PA/ALPA layers and all the listed layers must be drawn. For non-SMIC standard seal ring design, SMIC can't guarantee the seal ring quality. It's strongly recommended to qualify in SMIC before it used in product tape-out.			
SRCK.32	For SRCK.1/2/3/4/5/6/16/17/18/29/33/34, DRC allows 0.003um checking tolerance.			
SRCK.33	Top metal enclosure of PA	≥	0.212	um
SRCK.34	ALPA enclosure of PA	≥	0.989	um

7.3.10.4 Seal Ring check rule for 0.11um

Use of the scribe line seal ring to protect test chip is recommended. A completed seal ring structure includes metal guard rings, die corner stress relief patterns and assembly isolation areas.

MARKS is the marking layer of seal ring. All of the seal ring region must be blocked by MARKS.

SMIC Maskshop can help to add seal ring structure upon customer's request. If the Seal Ring is added by designer, the marking layer MARKS must be drawn.

If customers draw seal ring by themselves and combine it with main chip, the seal ring layout should not violate general seal ring design rules except special notices. It's strongly recommended designers to follow SMIC seal ring GDS sample structure. If designers use their owned seal ring structure, SMIC can't guarantee the seal ring quality.

Rule No.	Description	Operation	Design value	Unit
SRCK.1	Contact slot width	=	0.185	um
SRCK.2	V1-V6 slot width	=	0.194	um
SRCK.3	V7, TV1, TV2 slot width	=	0.233	um
SRCK.4	Space between inner CT slot and the metal ring edge	≥	0.784	um
SRCK.5	Space between inner Via(V1~V6) slot and the metal ring edge	≥	0.779	um
SRCK.6	Space between inner V7,TV1,TV2 slot and the metal ring edge	≥	0.744	um
SRCK.7	CT width and length, DRC waive CT slot pattern with width = 0.185um in seal ring region.	=	0.208	um
SRCK.8	V1-V6 width and length, DRC waive via slot pattern with width = 0.195um in seal ring region.	=	0.245	um
SRCK.9	V7, TV1, TV2 width and length, DRC waive top via slot pattern with width = 0.233um in seal ring region.	=	0.433	um
SRCK.10	Space between CT along the direction of seal ring	=	0.724	um
SRCK.11	Space between via(V1~V6) along the direction of seal ring	=	0.688	um
SRCK.12	Space between V7/TV1/TV2 along the direction of seal ring.	=	0.50	um
SRCK.13	Space between outer ring CT slot and the metal ring edge	≥	0.734	um
SRCK.14	Space between outer ring via1~via6 slot and the metal ring edge	≥	0.735	um
SRCK.15	Space between outer ring V7/TV1/TV2 slot and the metal ring	≥	0.71	um

Rule No.	Description	Operation	Design value	Unit
	edge			
SRCK.16	Passivation slot width in MARKS covered areas	=	2.442	um
SRCK.17	Space between active AA/GT/METAL/Al RDL patterns and internal metal ring edge assembly isolation.	≥	10	um
SRCK.18	Seal ring must be a close ring. DRC check CT/Metal/Via/Top metal/Top via/PA/ALPA layers and all the listed layers must be drawn. For non-SMIC standard seal ring design, SMIC can't guarantee the seal ring quality. It's strongly recommended to qualify in SMIC before it used in product tape-out.			
SRCK.19	For SRCK.1/2/3/7/8/9/10/11/12/16/20/21, DRC allows 0.003um checking tolerance.			
SRCK.20	Top metal enclosure of PA	≥	0.235	um
SRCK.21	ALPA enclosure of PA	≥	1.099	um

7.4 0.11um design guideline

7.4.1 Layout drawing and shrinking process

0.11um logic layout drawing rules are the same as 0.13um layout drawing rules of this document. After customer's tape-out, SMIC does a 90% shrink on the designs.

7.4.2 DRC

Please expect the design to run through fabrication successfully once the design rule checking (DRC) based on the current 0.13um design rules is passed.

7.4.3 Size-up process

7.4.3.1 Shinkage design guideline

Gate lengths of 0.11um designs undergo a size-up before 90% shrinking. After shrinking, the gate lengths go back to a value close to the drawn dimension, details as shown in below table 7.4.3.2. Neither this nor other 0.11um processes imposes additional and special design rules for designers to follow.

7.4.3.2 Non-shrinkage design guideline

NODMF is defined as non-shrinkage device marker layer, which should be drawn with (180;0) GDS layer. In NODMF covered area, designer should size up "x1.11" the layout which he does not want to shrink before data base tape out.

SMIC Pcell library(Inductor/ BJT/MOM devices) for the 0.11 design already size up "x1.11" and cover with NODMF marker layer. For CTM design, it's supposed that only the non-shrinkage device can be put under SMIC Pcell (such as: Inductor/BJT/MOM) with NODMF covered region, and designer should size up "x1.11" the original layout before put under SMIC Pcell.

Basing on SMIC existing T/O procedure for the 0.11 design, it is minor different for the GT layer LOTA operation between shrinkage design(without NODMF covered region) and non-shrinkage design(with NODMF covered region), as shown in below table. For the shrinkage design GT logic operation will extra size-up minima GT size before do 90% global shrinkage, to ensure final minima GT size go back to drawn size; For non-shrinkage design(with NODMF covered region), it's executed 90% global shrinkage only.

GT size for 0.11 design	GDS drawn size	Post-LOTA size	Post-90% shrink size	Tape-out size
Shrinkage design (Without NODMF covered region)	0.13um	0.144um (minima GT single side size-up 0.007um)	0.13um	0.13um
Non-shrinkage design (With NODMF covered region)	0.144um (Layout size-up"x1.11")	0.144um (no change post LOTA)	0.13um	0.13um

Note:

If design miss put shrinkage-purpose device under SMIC Pcell with NODMF covered region, the poly CD such as 0.13um will be changed to 0.11um after 90% shrinkage, not size back to target 0.13um.

7.4.4 Tooling flow

The SMIC database tooling procedure is shown figure 1 below.

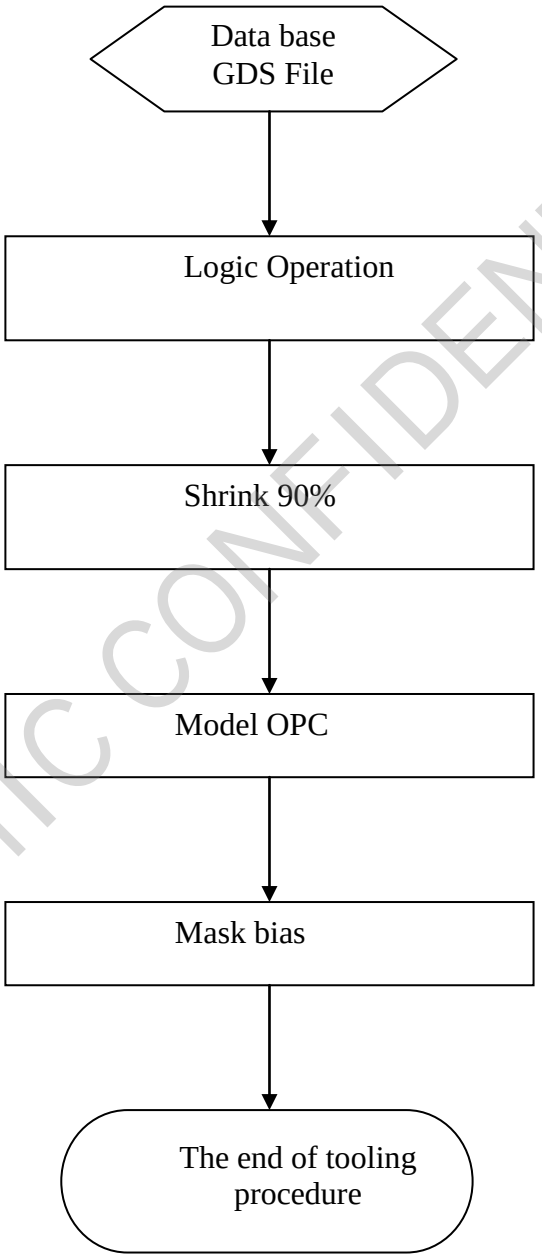


Figure 1

7.4.5 The 90% shrinkage data base treatment procedure

7.4.5.1 Designer draw layout base on 0.13um design rule.
7.4.5.2 Customer tape out the 0.13um layout in SMIC.
7.4.5.3 Logic operation for all layers except 130 GT layer: 0.13um logic LOTA, namely SMICLC13GE0 and SMICLC13GE1 should be used for 1.2/2.5V and 1.2/3.3V design respectively.
7.4.5.4 Logic operation for 130 GT layer. For 1.2/2.5V device: follow 0.11um logic LOTA SMICMS11GE0. For 1.2/3.3V device: follow 0.11um logic LOTA SMICMS11GE1.
Shrink 90% for all layers.
7.4.5.5 OPC treatment
7.4.5.6 Add mask bias (follow tech. ID mask bias table)
7.4.5.7 JDV and mask making.

7.4.6 SMIC 0.11um mask layer mapping table

a) SMIC mask layer mapping table (IO Voltage: 2.5V) for SMIC 0.11um 1.2V/2.5V mix-signal product tape out usage. (Top tier table ID: LCMO11-V00)

Mask ID	Process Name	Dig. Area Tone	Mask Generation	Description	Optional
292	DNW	C	Drawn	Deep N well imp for substrate noise suppression	Optional
901	KV	C	Drawn	Alignment mark clearing	Optional
120	AA	D	Generated	Active Area/SDG	Must
191	PW	C	Generated	P-Well / P-Tub	Must
491	PWH	C	Generated	P well I/O	Must
192	NW	C	Generated	N-Well / N-Tub	Must
492	NWH	C	Generated	N well I/O	Must
193	NC	C	Generated	N-Cell Implant	Optional
194	PC	C	Generated	P-Cell Implant/NFILED	Optional
296	MVN	C	Generated	Medium Vtn adjust	Optional
295	MVP	C	Generated	Medium Vtp adjust	Optional
131	DG	D	Generated	Dual Gate	Must
130	GT	D	Generated	Poly Gate / Poly-1 / ONO Gate	Must
116	NLL	C	Generated	NMOS LDD Implant for Low VDD	Must
113	PLL	C	Generated	PMOS LDD Implant for Low VDD	Must
115	PLH	C	Generated	PMOS LDD Implant for High VDD	Must
114	NLH	C	Generated	NMOS LDD Implant for High VDD	Must
110	ESD1	C	Drawn	ESD Implant for 1	Optional
198	SN	C	Drawn	N+ S/D Implant	Must
197	SP	C	Drawn	P+ S/D Implant	Must
155	SAB	D	Drawn	Resist Protect Oxide / Salicide Block	Must
156	CT	C	Drawn	Contact Hole (Metal to Si/Poly)	Must
160	M1	C	Generated	Metal-1	Must
178	V1	C	Drawn	Via-1 Hole	Must
180	M2	C	Generated	Metal-2	Must
179	V2	C	Drawn	Via-2 Hole	Must

Mask ID	Process Name	Dig. Area Tone	Mask Generation	Description	Optional
181	M3	C	Generated	Metal-3	Must
177	V3	C	Drawn	Via-3 Hole	Must
182	M4	C	Generated	Metal-4	Must
176	V4	C	Drawn	Via-4 Hole	Must
183	M5	C	Generated	Metal-5	Must
175	V5	C	Drawn	Via-5 Hole	Must
184	M6	C	Generated	Metal-6	Must
174	V6	C	Drawn	Via-6 Hole	Must
185	M7	C	Generated	Metal-7	Must
142	TV1	C	Drawn	First Top Via	Optional
141	TM1	C	Generated	First Top Metal	Optional
144	TV2	C	Drawn	Second Top Via	Must
143	TM2	C	Generated	Second Top Metal	Must
107	PA	C	Drawn	Passivation / Pad	Must
108	ALPA	D	Generated	AL Bonding Pad	Must
163	MD	C	Drawn	Metal about top metal for redistribution passivation2	Optional
106	FUSE	C	Drawn	Fuse Window	Optional

Note: Please refer DCC document PM-DATA-02-2001 layer mapping table 1 for the pure generated layer GDS No. /data type which is only for Tech. file development usage. Designers do not need to draw the layers.

b) SMIC mask layer mapping table (IO Voltage: 3.3V) for SMIC 0.11um 1.2V/3.3V mix-signal product tape out usage. (Top tier table ID: LCMO11-V01)

Mask ID	Process Name	Dig. Area Tone	Mask Generation	Description	Optional
292	DNW	C	Drawn	Deep N well imp for substrate noise suppression	Optional
901	KV	C	Drawn	Alignment mark clearing	Optional
120	AA	D	Generated	Active Area/SDG	Must
191	PW	C	Generated	P-Well / P-Tub	Must
491	PWH	C	Generated	P well I/O	Must
192	NW	C	Generated	N-Well / N-Tub	Must
492	NWH	C	Generated	N well I/O	Must
193	NC	C	Generated	N-Cell Implant	Optional
194	PC	C	Generated	P-Cell Implant/NFILED	Optional
296	MVN	C	Generated	Medium Vtn adjust	Optional
295	MVP	C	Generated	Medium Vtp adjust	Optional
131	DG	D	Generated	Dual Gate	Must
130	GT	D	Generated	Poly Gate / Poly-1 / ONO Gate	Must
116	NLL	C	Generated	NMOS LDD Implant for Low VDD	Must
113	PLL	C	Generated	PMOS LDD Implant for Low VDD	Must
115	PLH	C	Generated	PMOS LDD Implant for High VDD	Must
114	NLH	C	Generated	NMOS LDD Implant for High VDD	Must
110	ESD1	C	Drawn	ESD Implant for 1	Optional
198	SN	C	Drawn	N+ S/D Implant	Must
197	SP	C	Drawn	P+ S/D Implant	Must
155	SAB	D	Drawn	Resist Protect Oxide / Salicide Block	Must
156	CT	C	Drawn	Contact Hole (Metal to Si/Poly)	Must
160	M1	C	Generated	Metal-1	Must
178	V1	C	Drawn	Via-1 Hole	Must
180	M2	C	Generated	Metal-2	Must
179	V2	C	Drawn	Via-2 Hole	Must
181	M3	C	Generated	Metal-3	Must

Mask ID	Process Name	Dig. Area Tone	Mask Generation	Description	Optional
177	V3	C	Drawn	Via-3 Hole	Must
182	M4	C	Generated	Metal-4	Must
176	V4	C	Drawn	Via-4 Hole	Must
183	M5	C	Generated	Metal-5	Must
175	V5	C	Drawn	Via-5 Hole	Must
184	M6	C	Generated	Metal-6	Must
174	V6	C	Drawn	Via-6 Hole	Must
185	M7	C	Generated	Metal-7	Must
142	TV1	C	Drawn	First Top Via	Optional
141	TM1	C	Generated	First Top Metal	Optional
144	TV2	C	Drawn	Second Top Via	Must
143	TM2	C	Generated	Second Top Metal	Must
107	PA	C	Drawn	Passivation / Pad	Must
108	ALPA	D	Generated	AL Bonding Pad	Must
163	MD	C	Drawn	Metal about top metal for redistribution Passivation2	Optional
106	FUSE	C	Drawn	Fuse Window	Optional

Note: Please refer DCC document PM-DATA-02-2001 layer mapping table 1 for the pure generated layer GDS No. /data type which is only for Tech. file development usage. Designers do not need to draw the layers.

c) SMIC mask layer mapping table (IO Voltage: 2.5V) for SMIC 0.11um 1.2V/2.5V mix-signal product tape out usage. (Top tier table ID: MSGL11-V01)

Mask ID	Mask Name	Dig. Area Tone	Mask Generation	Mask Purpose	Optional
292	DNW	C	Drawn	Deep N well imp for substrate noise suppression	Optional
120	AA	D	Generated	Active Area/SDG	Must
901	KV	C	Drawn	Alignment mark clearing	Optional
192	NW	C	Generated	N-Well / N-Tub	Must
191	PW	C	Generated	P-Well / P-Tub	Must
492	NWH	C	Generated	N well I/O	Must
491	PWH	C	Generated	P well I/O	Must
193	NC	C	Generated	N-Cell Implant and High	Optional
194	PC	C	Generated	P-Cell Implant/NFILED	Optional
296	MVN	C	Generated	Medium Vtn adjust	Optional
295	MVP	C	Generated	Medium Vtp adjust	Optional
131	DG	D	Generated	Dual Gate	Must
130	GT	D	Generated	Poly Gate / Poly-1 / ONO Gate	Must
116	NLL	C	Generated	NMOS LDD Implant for Low VDD	Must
113	PLL	C	Generated	PMOS LDD Implant for Low VDD	Must
115	PLH	C	Generated	PMOS LDD Implant for High VDD	Must
114	NLH	C	Generated	NMOS LDD Implant for High VDD	Must
110	ESD1	C	Drawn	ESD Implant for 1	Optional
198	SN	C	Drawn	N+ S/D Implant	Must
197	SP	C	Drawn	P+ S/D Implant	Must
413	HRP	C	Drawn	High Resistant Poly Imp	Optional
155	SAB	D	Drawn	Resist Protect Oxide / Salicide Block	Must

Mask ID	Mask Name	Dig. Area Tone	Mask Generation	Mask Purpose	Optional
156	CT	C	Drawn	Contact Hole (Metal to Si/Poly)	Must
160	M1	C	Generated	Metal-1	Must
178	V1	C	Drawn	Via-1 Hole	Must
180	M2	C	Generated	Metal-2	Must
179	V2	C	Drawn	Via-2 Hole	Must
181	M3	C	Generated	Metal-3	Must
177	V3	C	Drawn	Via-3 Hole	Must
182	M4	C	Generated	Metal-4	Must
176	V4	C	Drawn	Via-4 Hole	Must
183	M5	C	Generated	Metal-5	Must
175	V5	C	Drawn	Via-5 Hole	Must
184	M6	C	Generated	Metal-6	Must
174	V6	C	Drawn	Via-6 Hole	Must
185	M7	C	Generated	Metal-7	Must
162	MIM	D	Drawn	Top Plate of MIM Capacitor	Optional
132	P2	D	Drawn	Poly-2 or MIM plate 2	Optional
142	TV1	C	Drawn	First Top Via	Optional
141	TM1	C	Generated	First Top Metal	Optional
144	TV2	C	Drawn	Second Top Via	Must
143	TM2	C	Generated	Second Top Metal	Must
107	PA	C	Drawn	Passivation / Pad	Must
108	ALPA	D	Generated	AL Bonding Pad	Must
163	MD	C	Drawn	Metal about topmetal for redistribution, Passivation 2	Optional
106	FUSE	C	Drawn	Fuse Window	Optional

Note: Please refer DCC document PM-DATA-02-2001 layer mapping table 1 for the pure generated layer GDS No. /data type which is only for Tech. file development usage. Designers do not need to draw the layers.

d) SMIC mask layer mapping table (IO Voltage: 3.3V) for SMIC 0.11um 1.2V/3.3V mix-signal product tape out usage. (Top tier table ID: MSGL11-V00)

Mask ID	Mask Name	Dig. Area Tone	Mask Generation	Mask Purpose	Optional
292	DNW	C	Drawn	Deep N well imp for substrate noise suppression	Optional
120	AA	D	Generated	Active Area/SDG	Must
901	KV	C	Drawn	Alignment mark clearing	Optional
192	NW	C	Generated	N-Well / N-Tub	Must
191	PW	C	Generated	P-Well / P-Tub	Must
492	NWH	C	Generated	N well I/O	Must
491	PWH	C	Generated	P well I/O	Must
193	NC	C	Generated	N-Cell Implant and High	Optional
194	PC	C	Generated	P-Cell Implant/NFILED	Optional
296	MVN	C	Generated	Medium Vtn adjust	Optional
295	MVP	C	Generated	Medium Vtp adjust	Optional
131	DG	D	Generated	Dual Gate	Must
130	GT	D	Generated	Poly Gate / Poly-1 / ONO Gate	Must
116	NLL	C	Generated	NMOS LDD Implant for Low VDD	Must
113	PLL	C	Generated	PMOS LDD Implant for Low VDD	Must
115	PLH	C	Generated	PMOS LDD Implant for High VDD	Must
114	NLH	C	Generated	NMOS LDD Implant for High VDD	Must
110	ESD1	C	Drawn	ESD Implant for 1	Optional
198	SN	C	Drawn	N+ S/D Implant	Must
197	SP	C	Drawn	P+ S/D Implant	Must
413	HRP	C	Drawn	High Resistant Poly Imp	Optional
155	SAB	D	Drawn	Resist Protect Oxide / Salicide Block	Must
156	CT	C	Drawn	Contact Hole (Metal to Si/Poly)	Must

Mask ID	Mask Name	Dig. Area Tone	Mask Generation	Mask Purpose	Optional
160	M1	C	Generated	Metal-1	Must
178	V1	C	Drawn	Via-1 Hole	Must
180	M2	C	Generated	Metal-2	Must
179	V2	C	Drawn	Via-2 Hole	Must
181	M3	C	Generated	Metal-3	Must
177	V3	C	Drawn	Via-3 Hole	Must
182	M4	C	Generated	Metal-4	Must
176	V4	C	Drawn	Via-4 Hole	Must
183	M5	C	Generated	Metal-5	Must
175	V5	C	Drawn	Via-5 Hole	Must
184	M6	C	Generated	Metal-6	Must
174	V6	C	Drawn	Via-6 Hole	Must
185	M7	C	Generated	Metal-7	Must
162	MIM	D	Drawn	Top Plate of MIM Capacitor	Optional
132	P2	D	Drawn	Poly-2 or MIM plate 2	Optional
142	TV1	C	Drawn	First Top Via	Optional
141	TM1	C	Generated	First Top Metal	Optional
144	TV2	C	Drawn	Second Top Via	Must
143	TM2	C	Generated	Second Top Metal	Must
107	PA	C	Drawn	Passivation / Pad	Must
108	ALPA	D	Generated	AL Bonding Pad	Must
163	MD	C	Drawn	Metal about top metal for redistribution, Passivation2	Optional
106	FUSE	C	Drawn	Fuse Window	Optional

Note: Please refer DCC document PM-DATA-02-2001 layer mapping table 1 for the pure generated layer GDS No. /data type which is only for Tech. file development usage. Designers do not need to draw the layers.

8. Attachment:

1) L013SEAL_RING20180122.GDS
2) L011SEAL_RING20180122.GDS

Change History:

Document Change History				
Doc. Rev.	Tech Dev. Rev.	Effective Date	Author	Change Description
0T	0.0	2002-8-7	TzuChiang Yu	Initiate
1T	0.1	2003-05-16	Wayne Zheng	◆ Change via 1-6 size ◆ Modify metal 1-8 design rules ◆ Modify metal slot rules ◆ Modify metal dummy rules ◆ Modify seal ring rules ◆ 7.2.4 NN Note 1: DNW->NW 7.2.7 GT GT14: Forbidden->allowed
2T	0.2	2003-06-24	Jay Ning	To update seal ring rules
3T	0.3	2003-12-29	Brandon_Li	◆ 7.2.12 SN.8 butted N+AA-> butted P+AA ◆ 7.2.13 SP.8 butted P+AA-> butted N+AA ◆ 7.2.8 NLL.7 0.27->0.4 ◆ 7.2.8 NLL.8 delete ◆ 7.2.9 PLL.7 0.27->0.4 ◆ 7.2.9 PLL.8 delete ◆ 7.2.10 NLH.7 0.27->0.4 ◆ 7.2.10 NLH.8 delete ◆ 7.2.11 PLH.7 0.27->0.4 ◆ 7.2.11 PLH.8 delete ◆ 7.2.12 SN.6 0.27->0.4 ◆ 7.2.12 SN.7 0.27->0.4 ◆ 7.2.12 SN14 modify the description ◆ 7.2.12 SN.18 delete ◆ 7.2.13 SP.6 0.27->0.4 ◆ 7.2.13 SP.7 0.27->0.4 ◆ 7.2.13 SP.14 modify the description ◆ 7.2.13 SP.18 delete ◆ 7.2.7 GT.16 delete ◆ 7.2.7 note 1 added Suggestion 4 added

				Change maximum metal width to 12um in 7.2.17, 7.2.19, 7.2.22. Regroup recommended rule from regular restriction in metal slot, metal dummy section in 7.2.23, 7.2.24. Define minimum slot density rule in 7.2.24. Modified 7.2.17 M1.3, 7.2.19 Mn.3 and 7.2.22 MT.3 rules for minimum metal space Specify favorable metal slot design in M1.11, Mn.5 and MT.7. Modified minimum space in metal slot rules 7.2.23 SL.3, 4, 5. Recommended clearance in metal slot design in 7.2.23. Add comments behind each metal and via design rule section for non-restrictive SMIC recommendations in 7.2.17, 7.2.18, 7.2.19, 7.2.20, 7.2.21, 7.2.22.
4R	0.4	2004-06-17	WenYue _Zheng	7.2.15 revised Min. M1 enclosure beyond CT in CT.10; **7.2.16 summary of BEOL feature sizes;** 7.2.17 revised M1 feature size in M1.1; Add min pitch rule in M1.2; Revised overlay in M1.6, M1.7; 7.2.18 revised V1.4; 7.2.19 revised Mn.4, Mn.6-9; 7.2.22 revised MT.5; 7.2.23 revised SL.3, SL.4 and SL.5; 7.2.25 updated Jmax according to new RE data, and changes of metal rules.
5R	1.0	2004-08-19	Brandon Li	Update “suggestion for the optimized circuit design” 1 Modify title: add 3.3v 7.2.5 note 1 added 7.2.7 note 1 updated GT.2 include 3.3V rule 7.1.1 note 2 deleted 7.2.15 CT.5 include 3.3V rule 7.2.5 AA.11 update the description 7.2.6 DG.4 0.86 —> 0.62 DG.7 0.86 —> 0.62 DG.8 0.86 —> 0.62 7.2.2 NW.7 updated
6R	1.1	2004-09-23	Brandon Li	Add 7.2.29 VTNH rule(optional) 7.2.30 VTPH rule(optional) 7.1.1 note 3

7R	1.2	2004-12-10	Brandon Li	Update DG.4, DG.7 description. Add recommendation for NWR usage. 7.2.29 replace layer name VTNH with NC 7.2.30 replace layer name VTPH with PC Replace layer name Res_AA with RESAA Replace layer name Res_P1 with RESP1

8R	1.3	2005-1-10	Brandon Li	Update NC.3, NC.4, NC.7, NC.8
				Add NC.9,NC.10
				Update PC.3, PC.4, PC.7, PC.8
				Add PC.9,PC.10
				Add 7.2.31 MVN rule, add 7.2.32 MVP rule
				Add 7.1.1 note 4
				Update DNW.2 and DNW.5

9R	1.4	2005-8-2	Jay Ning	Text and format: changed to simplified description for all sections. Contents: Design rule updated on all sections according to silicon data and all rules are more relaxed than previous versions
10R	1.5	2005-09-30	Jay Ning	Correct SP.8 from 0.2 to 0.3 Add doc. Numbers for section 5. Add metal fuse location rule. Correct SAB.9 SAB overlap poly to SAB overlap SN/SP Add NW.7a space between 2.5 or 3.3 at same potential DG1. 0.8 ->0.7 DG2. 0.8 >0.7 Mn.5: 0.26->0.30 M1.7 and Mn.7 to add 0.5um length require for 45 bend line
11R	1.6	2006-04-14	James Cui	7.2: Layout rule description typing error update for 2’nd MVN where MVN ->MVP; NMOS ->PMOS 7.1.2: SMIC Mask Layer Name mapping table, NC for Hi NMOS; PC for Hi PMOS; MVN for Low Vt NMOS,MVP for Low Vt PMOS 7.2.8: Update typing error “High” Vt ->”Low” Vt 7.2.21: Mn.6 where M1->Mn 7.2.24 TM.7 add Dummy pattern add recommend for lower density TM.

12R	1.7	2006-10-25	Touber Tseng	Add 7.2.25 Guideline for ALPad layout minima Remove the content of 7.2.32 Seal Ring guideline, define this rule in another document TD-LO13-DR-2002.
13R	1.8	2007-07-02	Touber Tseng	Modify 0.13um DR for legal requirement: 1.modify 7.2.29 Current Density Rule 2.add “SC with high speed performance” at item 7.1.1 3.change item 5 from “0.13um Logic 1P8M Salicide 1.2/3.3V High Speed PCM Specification” to “0.13um Logic 1P8M Salicide 1.2V/3.3V SC with high speed performance PCM Specification” for legal requirement
14R	1.8	2007-11-09	Brian Zhang	Add “MD” layer to 7.1.2 table, add more explain in this table note 3. Add 7.3.32 AL RDL Rules. Change 6.Responsibility to Technology Development Center is responsible before technology transfer and FAB PIE is responsible after technology transfer. Add 7.2.29 CDR.33a. Change 7.2.31 Mark.5 V5 to Vn. add reference document to item 5

15R	2.0	2009-03-24	Xiaoliang_Tang	1.Add 7.2.34 Passivation layout minima rules 2.Add LOTA TD-LO13-LO-2003 and OPC TD-GENL-01-2023 No in the Reference. 3.Update 7.1.2 SMIC mask layer name mapping table description: Change Design layer name to Mask layer name Modify the layer's GDS number which generated from logic operation to NA. Add the LOTA No. Modify the ESD layer from "Draw" to logic operation. Update the Fuse layer description. Allow ALPA, MD, PI can be drawn refer to Note-3. 4.Add GDS No in the 7.2.32 AL RDL rule picture. 5.Add GDS No in the 7.2.25 picture for ALPAD. 6.Modify 7.2.25, 7.2.26 from guideline to rule. 7.Modify 7.1.2 Note-2. Not suggest to draw LDD layer according to DS request. 8.Add 7.1.2 Note-4 to allow M6 (66)/M7 (67)/M8(68) as topmetal for1P6M/1P7M/1P8M design according to DS request. 9.Delete reference document TD-LO13-DR-2001no need
16P	2.1	2010-07-30	Li Ping Zheng	Revise SMIC 0.13G/MS design rule DG.4 (Page-24) 1) 0.13 DG.4 modify from "2.5/3.3V transistor gate poly enclosure by DG" to "2.5/3.3V transistor channel (overlap of Poly and AA) enclosure by DG" 2) DG.4 change from 0.33um to 0.4um 3) Schematic chart change from Y direction only to X/Y direction both. 4) Schematic chart change from "Poly edge to DG edge" to "channel edge to DG edge".

17P	2.2	2011-07-22	Amy Wong	For TD-LO13-DR-2001V16P document, need to update and modify total has 37 item below: 1)7. Update Subject Content user guideline. 2)7.1.2 mask layer table updated as A, B, C three tables 3)7.1.2 table A drawing layer update 4)7.1.2 Modify LDD layer for Generated layer only. 5)7.1.2 Modify A table of note 2 description. 6)7.1.3 Insert Mask layer device table 7)7.1.4 Insert Metal Options table. 8)7.1.5 Insert section design rule abbreviation, update old 7.1.6, 7.1.5 section number as 7.1.5, 7.1.6 9)7.2.1 DNW.5 figure update; 10)7.1.5 Add straddle definition 11)7.2.2 add AA.10 rule description. 12)7.2.3 Update NW.3, NW.4, delete NW.6, NW.7a, NW.7b, update NW.8 rule number to be NW.5 13)7.2.3 add new rule for NW6. 14)7.2.3 Updata NW.4 and NW.4a rule description 15)7.2.4 add new PSUB rule: PSUB.8; PSUB note2 16)7.2.4 add PSUB.8 device structure. 17)7.2.9 DG.4 figure and rule value update. DG.6 rule description update 18)7.2.9 Update DG.5 rule description 19)7.2.9 add DG.7 rule description. 20)7.2.9 Modify DG.6 Arrow. 21)7.2.10 add note 3 description. 22)7.2.15 Update SN.9 rule adding NWH 23)7.2.18 Update the figure of CT 24)7.2.19 M1.6 rule of density check window definition 25)7.2.20 V1.2b rule description 26)7.2.21 Mn.6 rule for density check window definition 27)7.2.22 Update Vn.2b rule description 28)7.2.23 Add TV.2b rule description and update TV.2 rule number. 29)7.2.24 TM.7 rule for density check window definition 30)7.2.32 Add new rule RDL.14 and note 31)Add 7.2.34 new section for border layer 32)7.2.35: update previous 7.2.34 section number to be 7.2.35 33)7.2.23 Update TV.10 rule description. 34)7.2.10 Update GT.12 and GT.11rule description. 35)7.2.32 Update RDL.8 rule description. 36)7.2.9 Update DG.4 rule description.

				37)delete the reference :Salicide 1.0/3.3V LV PCM Specification and TD-LO13-SP-2004 0.13um Logic Low Voltage 1P8M(1P7M, 1P6M) Salicide 1.0V/3.3V SPICE model (version 1.1),for no need.
18P	2.3	2013-07-17	Pretty_Chen	1. 7.1.7 Update “space” definition for MVN, MVP, NC, PC, SN, SP layers. Add “runlength” definition. 2. 7.2.5~7.2.8: Add note for NC, PC MVN, MVP. 3. 7.2.10: Add GT.13 recommended rule. 4. 7.2.20/7.2.22 Add V1.11[R]/ Vn.10[R] recommended rule, delete note rule. 5. 7.2.18 Update CT.5 and CT.5a rule description. 6. Add 1.5v device into DR. Update Title (1) / Purpose (2) / Technology Feature (7.1.1) description. Add 1.5V device into 7.2.3/7.2.4/7.2.9/7.2.10/7.2.18 (NW.4/NW.4a/PSUB.2a/DG.6/GT.1a). 7. 7.2.19/7.2.21 Add [R] for M1.3a/ Mn.3a/M1.3b/ Mn.3b rule number. Optimize M1.3a/ Mn.3a rule description. 8. Add user guideline: 2/3/4/5/6/7 into 7 subject content. 9. 7.1.2 /7.1.3:update all the tables’ format (SMIC drawing, mask layer mapping table, device truth table, CAD layer mapping table). Update 7.1.2.1 Note. Add note under each mask layer mapping table. 10. 7.1.4: update metal option table format and add note2. 11. 7.2.11/7.2.12/7.2.23/7.2.24 Update NLL/PLL/TV/TM title description. 12. 7.2.2: add AA density rule: AA.11/AA.12. Modify AA note 1 description. Add AA note 2.

				13. Update 7.2.30 ALRDL/ 7.2.31 PA section design rules/sketch map. 14. Delete original 7.2.26 PI/ 7.2.25 ALPad design rule due to don't provide this process. 15. Delete 7.2.10 GT note 3 due to this note is not reasonable. 16. Update reference document and format for 5 Reference section. 17. 7.2.9 Optimized DG.4 rule description. Add DG.4b to cover 0.11um design. Delete DG.7 and DG note. 18. 7.2.3/7.2.24/7.2.32: Add NW.7[G] /TM.9[G] /MD design guideline. 19. 7.2.16 Add [NC] for SP.13. 20. 7.2.2/7.2.4/7.2.10/7.2.18/7.2.19~7.2.23 Optimized AA.3/ PSUB.4/ PSUB.7/ GT.3/ GT.4/GT.5/GT.8/ CT.9/PSUB.3/GT. 11/CT.10/M1.3a and Mn.3a/Mn.8/ TM.8/Vn.11/V1.1/Vn.1/TV.1 rule description. 21. Original 7.2.27 change to 7.2.25: Optimize metal slot section design rule. 22. Add 7.2.27.2 non-salicide poly current density rule resistor and 7.2.40 dummy check rule. 23. Add 7.2.27.1 Current Density Rule (DC/AC) title. 24. 7.2.39 update whole border layer design rule. 25. Add 7.2.33~7.2.38.Merge Mix-signal & RF sub-ECN design rule(TD1302050002) into this document and update below items: a. Update HRP.12/P2.5/P2.7/MTT.5/MTT.2b/MIM.1/MIM.5/SMIM.1/SMIM.5/ BMIM.6 rule description. b. Add [NC] for HRP.10/MTT.10 rule number. c. Modify P2.7/ MIMDMY.2[G] rule value. d. Add Bottom plate and active MIM definition above each MIM design rule table. e. Update BMiM.1 rule description and rule value. 26. Update document title. 27. Update 7.1.2/7.1.3 all the tables' format. 28. 7.2.27 Add [NC] for all current density rule number. 29. Add 7.3: 0.11um design guideline. 30. Add 7.2.40 DUP Pad guideline. 31. Add CT.11.

19P	1.23	2014-10-31	Kelpy_Pan	1. Modify Tech Ver to 1.23 follow DR version naming rule. (when latest Tech. Dev. Rev ≥ 1, the new value should be aligned to "1.xx" [xx = (10 + N - 1)] in next version if the accumulative total count of existing Tech. Dev. Rev ≥ 1 is N) 2. Update page 10 file title to "0.11um/0.13um Logic & Mix-Signal 1.2/2.5/3.3v generic and 0.13um 1.5/3.3v low leakage Design Rule" 3. 7.2.19 Update M1.8 description to "Maximum line width allowed. Metal slot rule will apply for a metal with line width greater than this value. DRC skip to check (M1 interact with PA pattern)." follow special release notice. 4. 7.2.21 Update Mn.8 description to "Maximum line width. Metal line greater than this width will comply metal slot design rule (DRC waive: Mn interact with PA pattern, (TM-1 AND DUPMK1) region for one top metal design, MIM bottom plate and MIM shield under MIM design)."follow TECN TD13090002 5. 7.2.30 Add "ALPA.10a (for 0.11um design)", "ALPA.10b (for 0.11um design)" for 0.11um DRC, add Note5 "For 0.11um, Al bump Pad is defined as ALPA layer width larger than 35μm and interact with PA (PA width> 35um)." for 0.11um DRC follow TECN TD13090002 6. 7.2.34 add "0.13um" for each section title 7. 7.2.35 Add "MTT.2b (for 0.11um design)" for 0.11um DRC, follow TECN TD13090002 8. 7.2.36 add "0.13um" for each section title 9. 7.2.37 add "0.13um" for each section title 10. 7.2.38 add "0.13um" for each section title 11. 7.3.4 update flow chart shape follow template 12. Add 7.3.8 section to define DRC check rules switch setting for 0.11um and 0.13um DRC 13. Add 7.3.9; 7.3.10; 7.3.11; 7.3.12 sections for 0.11um MIM DRC check

20	1.24	2015-12-22	Amy Wang	1) Update rule 1.Title/2.Purpose to remove “0.13um” in “0.13um 1.5/3.3v”. 2) Update 5.Reference table to remove ESD/Antenna (Merged into main rule) 3) Update 7.1.1 Technology feature, rearrange P15 User guideline to 7.1.2/7.1.4 4) Add 7.1.3 Non-DRC checking guideline 5) Update 7.1.5.1/2 layer mapping table, 7.1.5.3 table update MD layer and add note2. 6) Update 7.1.6.1/2/3/4 Device truth tables, optimize the notes above the table, update ESD1/SAB setting to “0/*” for MOS, SP form “0” to “*” for poly e-Fuse, DNW to “0” for NW/Psub diode, NW to “*’ for DNW/Psub diode. 7) Add 7.1.7 Device table for dummy insertion 8) Update 7.1.9 Design Rule Nome. and Abbr. 9) Add 7.1.10 DRC methodology of Connectivity definition 10) Update 7.1.11 Definition of terminology 11) Update 7.1.12 Design requirements 12) Add 7.2.1 DNW.6 (lesson learn driven), update DNW.3, delete Notes1/2 (covered in main rule). 13) Update 7.2.2 AA.4/9/10/11 rule description 14) Update 7.2.3 NW.6, delete Notes1/2/3 (NW resistor rule covered). 15) Update 7.2.4 PSUB.4 “≥” to “=”, add PSUB.9[R]/ PSUB.10[NC], delete Notes1/2 (covered in main rule). 16) Update 7.2.5/6 NC.4/5/6/7/PC.4/5/6/7 rule description 17) Update 7.2.7/8 MVN.4/5/6/7/MVP.4/5/6/7 rule description 18) Update 7.2.9 DG.4/.4b rule to add 0.11/0.13 DRC switch 19) Add 7.2.10 GT.14[R]/GT.15[R] (rule completeness), delete notes2 to add as GT.16[R]. 20) Add 7.2.11-14 NLL.4b/PLL/4b/NLH.4b/PLH.4b, update NLL.6/PLL.6/NLH.6 /PLH.6 (Rule optimize for DR/DRC match) 21) Update 7.2.15 SN.7/8/9 to exclude NW resistor region. 22) Add 7.2.17 SAB.2a/10a[R], tighten SAB.10 rule value from 0.5 to 1.0um^2 (Lesson learnt driven) 23) Update 7.2.18 CT.4a to add “1.5V”, add CT.4c rule. 24) Delete 7.2.19/21 note1 to add as M1/Mn.19[NC] rules. 25) Add CT.15/V1.12/Vn.12/TV.11(Lesson learn driven) 26) Update 7.2.23 TV.10, 7.2.24 TM.8/TM.9[G] rules

				27) Delete “Metal dummy design minima” section, add to MnDUMCK.7[NC]/TMDUMCK.5[NC]/MTTDUMCK.5[NC] 28) Delete “(for 0.11um design)” in 7.2.25 MTT.2b rule-No, modify MTT.1/6a, add MTT.11[G] to cover MTT process 29) Delete “(for 0.11um design)” in 7.2.26 ALPA.10a/10b, update >35um to >32um in ALPA.10a/notes3; add ALPA.15[NC], delete note4. 30) Update 7.2.27 PA.3/PA.5, update PA.1 to PA.1a/1b[G], add PA.6 (Lesson learnt driven). 31) Update 7.2.28 MD design guideline, add DRC rule. 32) Add 7.2.29 NW/AA/Poly resistor rules (rule completeness). 33) Update 7.2.29.4 HRP.3/4/8/10 rules, update wording above the rule table and update HRP sketch map. 34) Delete original 7.3.8-12, update to 7.2.30-7.2.32 section, update Dummy MIM/bottom plate definition. 35) Update 7.2.30.2 MIM.11/13/18/MiM.14[G]/17[G], delete MiM.15[G] (MIM strategy optimized) 36) Update 7.2.31.1 BMiM.6[G]/8/13[G], delete BMiM.12[G] (MIM strategy optimized) 37) Update 7.2.32 SMiM.11/14[G]/18[G] rules, delete SMiM.16[G] (MIM strategy optimized) 38) Update 7.2.30.3 Metal shield guidelines. 39) Add 7.2.35 CDR.8a[NC]/ 8b[NC]/45[NC] /46[NC]. 40) Add 7.2.36 Antenna rule (Merged the branch rule) 41) Add 7.2.37 Conventional rule (Lesson learn driven) 42) Update 7.2.38 MTTDUMCK.1/2 to delete MTT.3b 43) Add 7.2.39 Seal Ring check rule 44) Update 7.3.1 Metal Slot Guideline rules add [G]. 45) Update 7.3.2 Metal fuse guideline 45) Update 7.3.3 Guideline for metal fuse repairing alignment mark 46) Add 7.3.5 Poly E-Fuse guideline (E-fuse committee conclusion) 47) Add 7.3.6 Logo guideline (Lesson learnt driven) 48) Add 7.3.7 ESD guideline (Merged the branch rule) 49) Add 7.3.8 Latch up guideline (Merged the branch rule) 50) Add 7.3.9 MOM device layout guideline (Lesson learn driven) 51) Update 7.4.6 Non-shrinkage design guideline, and move into 7.4.3.2. 52) Optimize all rule tables to follow template format.

21	1.25	2018-02-08	Minna_Xu	1. 7.1.4.8 add seal ring and HRP switch, DG.8[R]. Update 7.1.4.4/7 2. 7.1.5.1 Correct 39/40 design rule name 3. 7.1.5.2 CAD table add EXCLU, LUWMK1, VDDMK1, VSSMK1,MARKS, ESDIO2. 4. 7.1.6.1/3 mask truth table update MOS Varactor NLL/NLH 0 -> 1. 5. 7.1.11.1/3 update picture. 6. Update AA.1, AA.2, AA.3, AA.4, AA.5, AA.6, AA.7, NC.5, GT.2, GT.3, GT.4, GT.5, GT.6, GT.13[R], CT.1, CT.3, CT.4a, CT.5, CT.6, CT.7, CT.8, CT.9, CT.10, SN.1, SN.3, SN.5, SN.6, SN.7, SN.8, SN.9, SN.10, SP.1, SP.3, SP.4, SP.5, SP.6, SP.7, SP.8, SP.10, M1,1, M1.2, Mn.2, V1,4, V1.5, V1.6, V1.7, V1.8, V1.9, Vn.1, Vn.3, Vn.4, Vn.7, MTT.1, MTT.2a, MTT.3, MTT.4, Convention.2 to exclude SRAM region in 7.2. 7. 7.2.2 update AA.9 8. 7.2.4 update PSUB.9[R] to PSUB.9.Update PSUB.4/8 description. 9. Update 7.2.5 NC.3, 7.2.6 PC.3, 7.2.7 MVN.3, 7.2.8 MVP.3 description. 10. 7.2.9 add DG.8 for lesson learnt driven. 11. Update 7.2.9 DG.5 7.2.18 CT.5 description to add device AA definition. 12. 7.2.10 Modify GT.14[R] operation from < change to ⩽. 13. Update 7.2.12 PLL.11[R] operation from > change to ⩾. 14. 7.2.15 add SN.4b for lesson learn extension. 15. 7.2.22 update Vn.11. 16. 7.2.24 update TM.8 description. 17. 7.2.25 update MTT.1a, MTT.5. 18. 7.2.26 update ALPA.10a/10b. 19. 7.2.27 add PA note for customer request. 20. 7.2.28 update MD.6. 21. 7.2.29.1 RESNW update definition, RESNW.7. Add RESNW.10/11 for customer driven. 22. 7.2.29.2 RESAA update definition. 23. 7.2.29.3 RESP1 update definition. 24. 7.2.37 update Conventional.3. 25. 7.2.39 add SRAM design rule.

				26. 7.3.2 update FUSE.5[G], FUSE.6[G] to"=". 27. 7.3.7.1 update description. 28. 7.3.7.2 add ESD.22[G], ESD.22a[G], ESD.22b[G] and note for lesson learnt extension. 29. 7.3.7.3 ESD1 Update rule for lesson learnt extension. 30. Change ESDHV to ESD5V 31. 7.3.8 update LU.4[G] description. 32. 7.3.9 update MOM.4[G][NC] to MOM.4[G], update description. Add table 1. 33. 7.3.10 Add seal ring guideline for DR integrality. 34. Move 7.2.39 0.13SR check rule into 7.3.10.3. Update 0.13um SRCK.16/17/18, note. Add SRCK.31/32 for lesson learnt driven. Add SRCK.33/34 for customer request. Delete "square" in SRCK.4/5/6/19/20/21. 35. 7.3.10.4 add 0.11um SRCK. 36. Add 8 attachment of L013SEAL_RING20180122.gds and L011SEAL_RING20180122.gds. 37. Update reference document title and delete no need reference document TD-LO13-DR-2001.