



Doc. TD-LO13-DC-2001	No.: Doc. 0.11um/0.13um Logic & Mix-Signal Title: 1.2/2.5/3.3v generic and 1.5/3.3v low leakage Calibre DRC	Doc.Rev: 6	Tech Dev Rev: 1.25_0	Page No.:1/7
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Document Level: (For Engineering & Quality Document/工程暨品质文件专用)				
<input type="checkbox"/> Level 1 - Manual <input checked="" type="checkbox"/> Level 2 – Procedure/SPEC/Report <input type="checkbox"/> Level 3 - Operation Instruction				
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<input type="checkbox"/> Security 1 - SMIC Confidential <input checked="" type="checkbox"/> Security 2 - SMIC Restricted <input type="checkbox"/> Security 3 - SMIC Internal				
Document Change History				
Doc. Rev.	Tech Dev. Rev.	Effective Date	Author	Change Description
0P	2.3	2013-08-05	Liu Li	Initiate
1P	2.3	2013-10-30	Liu Li	1. add version number of reference file in term 5 2. add DRC's Revision history in term 8 3. update the description of <Choice 1> in term 9 4. change from SmicDR18P_cal013_cal011_mixlog_sali_V2.3_0P.tar.gz to SmicDR18P_cal013_cal011_mixlog_sali_V2.3_1P.tar.gz In the deck. Update Mn.8 TM1.7a/7b,MTT.7/7b, MIM.14/15,CT.5,CT.5a ALPA.10, BMIM.6,P2.5 to avoid false alarm; Tighten TMn.7b,MTT.7b coding for density rule
2P	2.3	2014-02-26	Liu Li	1. update title in item 1 to 0.11um/0.13um Logic & Mix-Signal 1.2/2.5/3.3v generic and 0.13um 1.5/3.3v low leakage Design Rule Check (DRC) runset of Calibre DRC 2. update version number of reference file in item 5 3. update DRC's Revision history in item 8 4. add TV.10 rule description due to DR update in item 10 5. change from SmicDR18P_cal013_cal011_mixlog_sali_V2.3_1P.tar.gz to SmicDR18P_cal013_cal011_mixlog_sali_V2.3_2P.tar.gz In *drc deck. Update TV1_4_5 coding due to DR update
3P	1.23	2014-11-18	Liu Li	1. Update version number of reference file in item 5 2. Delete DRC Revision History in item 8, for the Revision History is clearly written in DRC . 3. Add "Calibre tool version" in item 8. 4. Delete item 10 "Known Issue", for it is recorded in DR special notes.

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-------------------------	------	--	------------	-------------------------	-----------------

				<p>5. In item 10,Change from SmicDR18P_cal013_cal011_mixlog_sali_V2.3_2P.tar.gz to SmicDR19P_cal013_cal011_mixlog_sali_V1.23_3P.tar.gz that include both folders(SmicDR19P_cal011_mixlog_sali_DRC and SmicDR19P_cal013_mixlog_sali_DRC). 0.11um and 0.13um drc files is in the both folders.</p> <p>In drc deck: modify Tech Ver to 1.23 follow DR version naming</p>
4	1.24_0	2016-02-03	Liu Li	<p>1. Update the title from “0.11um/0.13um Logic & Mix-Signal 1.2/2.5/3.3v generic and 0.13um 1.5/3.3v low leakage Design Rule Check (DRC) runset of Calibre DRC” to “0.11um/0.13um Logic & Mix-Signal 1.2/2.5/3.3v generic and 1.5/3.3v low leakage Design Rule Check (DRC) runset of Calibre DRC “ in item 1 due to DR title update Delete the “013um” in item 2 and 3 due to DR title update</p> <p>2. Update DR version No. in item 5</p> <p>3. Update the item 6</p> <p>4. Delete item 8, for put the item 8 information in item 7</p> <p>5. Delete item 9: Calibre DRC script options setup, for the information is written in UserGuide of DRC package deck</p> <p>6. Update DRC package name and these files name in the package in item 8 In *drc, 1.Add switch for 0.11/0.13 process,PAD_TEXT,resistor connectivity,MOM_4_G for pcell. 2.Add layer FUSEMK1,GTFUSE,ESDIO2,ESDHV,ALMK1,MOMD MY,MOMMK(1-6). 3.Update the description for rule:DNW.3,AA.4/9/10,NW.6,NC.6/7,PC.6/7,MVN.6/7, MVP.6/7, NLL.4b/6,PLL.4b/6,NLH.4b/6,PLH.4b/6,SN.7/8,SP.7/8, CT.4a,V(1-7).1,TV2.1,PA.3. 4.Update rule:CT.3,TM2.9.G,PA.1a.1b.G,HRP.3,MIMDMY.2.G,A</p>

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-------------------------	------	--	------------	-------------------------	-----------------

				ADUMCK.5, GTDUMCK.5/6, SL.5.G.MTT.7a/7b, MIM.6.R, SMIM.6.R, SMIM.15, GConvention, SAB_10. 5.Modify rule:GSL=>GSL.G, GFUSE=>GFUSE.G, MIM.(14/17).G=>MIM.(14/17).R, GSRCK.G=>GSRCK, ALAP.10=>ALPA.10a, SMIM.14.G=>SMIM.14.R. 6.Add rule:DNW.6, PSUB.9_R, GT.(14/15/16).R, PLL.11.R, CT.4c/15, V(1-7).12, TV2.11, MTT.11.G, PA.6, ALPA.10b, SAB_2a, SAB_10a_R. 7.Add group rule:GMD, GRESAA, GRESNW, GRESP1, GEFU, GLOGO, GESD, GLU, GESD1, GMOM. 8.Del rule:MIM.15.G, MIM.SHD.2, BMIM.12.R, SMIM.SHD.2 In *ant initial
5	1.24_1	2016-04-13	Li Liu	1. Update DRC version No from V1.24_0 to V1.24_1 in item 5 2. Change organization to Technology R&D Management \ Tech-Bas Des-Enb Division \ Phy.Verification&Yield Enh. Dept .in item 6 due to personal organization information 3. Change deck package name from SmicDR20_cal013_mixlog_sali_p1mtx_xtm_V1.24_0.tar.gz to SmicDR20_cal013_mixlog_sali_p1mtx_xtm_V1.24_1.tar.gz in item 8 in *drc, update MOM_4_G coding in 1P8M_1TM to reduce false alarm. update HRP_12 coding to avoid false alarm In *ant, no update



Doc. TD-LO13-DC-2001	No.:	Doc. 0.11um/0.13um Logic & Mix-Signal Title: 1.2/2.5/3.3v generic and 1.5/3.3v low leakage Calibre DRC	Doc.Rev: 6	Tech Dev Rev: 1.25_0	Page No.:4/7
-------------------------	------	--	------------	-------------------------	-----------------

6	1.25_0	2018-02-12	SS_YANG	<ol style="list-style-type: none">1. Change Item1 Tiltle to be "0.11um/0.13um Logic & Mix-Signal 1.2/2.5/3.3v generic and 1.5/3.3v low leakage Calibre DRC"2. Update the Item 5 Reference's Document version3. Update Item 6 Responsibility to be "Design Service/PDK Division/Physical Verification/DRC&Dummy Deck"4. Update the Item 7 calibre tool version to be "2016.3_19.12"5. Update the Item8 Attachment<ol style="list-style-type: none">a) DRC script file to be "SMIC_CalDRC_011013LGLLMS_122533_V1.25_0.tar.gz"b)After decompress to be " SMIC_CalDRC_011013LGLLMS_122533_V1.25_0_DRC"" and "SMIC_CalDRC_011013LGLLMS_122533_V1.25_0.ant"c) In drc deck ,update following items:<ol style="list-style-type: none">1).ADD for DR update: DG_8_R,SRCK_31,RESNW_10,RESNW_11_R,SRCK_33,SRCK_34,SRCK_20_b,SRCK_21_b,MTT_2a,MVP_3,MVN_3,PC_3,NC_3,seal ring group rule for 0.112).Update for DR update: AA_9,CT_7_8,,MTT_1a,MTT_4,MTT_5,RESNW_7,SRCK_1,SRCK_2,SRCK_3,SRCK_4,SRCK_5_Vn,SRCK_6_TVn,SRCK_16,SRCK_17,SRCK_18,SRCK_19,SRCK_20,SRCK_21,MOM_4_G,PSUB_4,DG_5,PSUB_8,NC_5,LU_4,FUSE_5,FUSE_6,ESD_22a_G,ESD_22b_G,ALPA_10a,ALPA_10b3).Update for history issue:M1_3a_R,Mn_3a_R,BD_4,MD_6,RESP1_7,ESD_3_G4).Update rule comment to aline DR:Convention_35).Update all the switch format for standardization
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Doc. TD-LO13-DC-2001	No.:	Doc. 0.11um/0.13um Logic & Mix-Signal Title: 1.2/2.5/3.3v generic and 1.5/3.3v low leakage Calibre DRC	Doc.Rev: 6	Tech Dev Rev: 1.25_0	Page No.:5/7
-------------------------	------	--	------------	----------------------------	-----------------

				<p>6).Add Seal Ring switch for DR update</p> <p>7).Add and update layer mapping for DR update</p> <p>8).Change the PSUB_9_R rule name to main rule as PSUB_9 for DR update</p> <p>9).Change the rule name CT_15 to CT_12 to aline DR</p> <p>10).Update the Latch up group derived layer define for history issue</p> <p>11).Update Connect for MTT_5 for DR update</p> <p>12). Update the RESP1_4_R rule name to match DR</p> <p>13).Update skew_edge_check MTT_1 to match DR</p> <p>14).Update rule to exclude SRAM region for DR update:AA_1_2,AA_3,AA_4,AA_5,AA_6,AA_7,GT_2,GT_3,GT_4,GT_5,GT_6,GT_13_R,SN_1,SN_3,SN_5,SN_6,SN_7,SN_8,SN_9,SN_10,SP_1,SP_3,SP_4,SP_5,SP_6,SP_7,S P_8,SP_10,CT_1,CT_3,CT_4a,CT_5,CT_6,CT_7_8,CT_9,C T_10,M1_1,M1_2,V1_4_5_8,V1_6_7_9,Mn_2,Vn_1,Vn_3_4_7,MTT_1,MTT_1a,MTT_2a,MTT_3,Convention_2</p> <p>15).Add SRAM group rule for DR update</p> <p>16).Update ESD1 group rule for DR update</p> <p>17).Add ESD_8_G switch for DR update</p> <p>d) in ant runset:</p> <p>1).update the switch setting for DRC standardization</p> <p>2).Update the DR version and calibre tool version</p>
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Doc. TD-LO13-DC-2001	No.:	Doc. 0.11um/0.13um Logic & Mix-Signal Title: 1.2/2.5/3.3v generic and 1.5/3.3v low leakage Calibre DRC	Doc.Rev: 6	Tech Dev Rev: 1.25_0	Page No.:6/7
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1 Title

0.11um/0.13um Logic & Mix-Signal 1.2/2.5/3.3v generic and 1.5/3.3v low leakage Calibre DRC

2 Purpose

This document is intended to be a release note for the users who adopt SMIC 0.11um/0.13um Logic & Mix-Signal 1.2/2.5/3.3v generic and 1.5/3.3v low leakage rule's runset for their design reference.

3 Scope

This document describes the Calibre DRC script of 0.11um/0.13um Logic&MS release. Switches selection will be discussed within.

4 Nomenclature:

NA

5 Reference

This document and the Calibre DRC runset (Revision V1.25_0) are based on:

LOGIC DESIGN RULE:

0.11um/0.13um Logic & Mix-Signal 1.2/2.5/3.3v generic and 1.5/3.3v low leakage design rule

TD-LO13-DR-2001 Rev: 21 Tech Dev. Rev.: 1.25

6 Responsibility

Design Service/PDK Division/Physical Verification/DRC&Dummy Deck

7 Subject Content:

Caliber version: 2016.3_19.12

8 Attachment

DRC script file:

SMIC_CalDRC_011013LGLLMS_122533_V1.25_0.tar.gz

After decompress:

SMIC_CalDRC_011013LGLLMS_122533_V1.25_0_DRC

SMIC_CalDRC_011013LGLLMS_122533_V1.25_0.ant

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Doc. No.:	Doc. 0.11um/0.13um Logic & Mix-Signal	Doc.Rev:	Tech Dev	Page
TD-LO13-DC-2001	Title: 1.2/2.5/3.3v generic and 1.5/3.3v low leakage Calibre DRC	6	Rev: 1.25_0	No.:7/7

Release_Note

UserGuide