0.153um 5V CMOS EN
Process Technology Topological Design Rule

Catalog

1.0 Purpose:

This document provides the necessary information of the topological layout rules for 0.153um 5V CMOS EN Process technology.

2.0 Reference:

Item	Document name
Design rule	0.153um 5V CMOS EN Process Topological Design Rule -FAB2
Mask tooling	0.153um 5V CMOS EN Process Mask Tooling Information -FAB2
Spice model	C1513X50V01_20181206.zip
PDK	0d153um_5V_CMOS_EN_Process_design_Kit_Fab2_20181206.zip
Command file	CSMC0d153um_5V_CMOS_EN_Calibre_File_Fab2_20181130.zip
Mismatch report	0.153um CMOS EN Process Device Mismatch Characterization Report-FAB2
STD library	0.153um_CMOS_EN_1P6M_Process_5V_9T_Core_StandardCell_Library-with_GDS_20181207.tar.gz
IP	

3.0 Technology overview:

Process information:

Process Name: C151XX50XXXX CMOS EN Process
Technology: 0.15um
Number of Poly Layers: 1
Number of Metal Layer: 2~6
Process Description: 0.153um Poly Gate CMOS EN 1P6M Process
Poly Gate Type: Co-Salicide Gate
Operation Voltage: Core device 5V

4.0 General layer information:

4.1 Drawing layer table

Scope：
0.153um 5V CMOS EN Process

No.	Layer	Layer No.	Digitized Tone	Description
1	Active	2	Dark	Active
2	N-well	1	Clear	N-Well implant
3	Poly	3	Dark	Gate of the N & P channel
4	N+	5	Clear	N+ implant
5	P+	4	Clear	P+ implant
6	SAB	25	Dark	Salicide Block
7	Contact	6	Clear	Metal 1 Contact to Poly or Active
8	Metal1	7	Dark	Metal1 interconnect
9	Via1	8	Clear	Metal1 Contact to Metal2
10	Metal2	9	Dark	Metal2 interconnect
11	Via2	40	Clear	Metal2 Contact to Metal3
12	Metal3	41	Dark	Metal3 interconnect
13	Via3	61	Clear	Metal3 Contact to Metal4
14	Metal4	62	Dark	Metal4 interconnect
15	Via4	91	Clear	Metal4 Contact to Meta5
16	Metal5	92	Dark	Metal5 interconnect

17	Top Via	93	Clear	Metal5 Contact to Top Metal
18	Top Metal	94	Dark	Top Metal interconnect
19	Pad	10	Clear	Bond Pad opening
optional Layout Layer				
1	Deep N-well	55	Clear	P-well isolated for NMOS and parasitic VNPN
2	High resistor	33	Clear	Poly High Resistor implant
3	MIM	78	Dark	MIM Capacitor Top
4	MT	78:2	Dark	Dual MIM Capacitor Top
5	Top Thick Metal	86	Dark	Top Thick Metal
6	PWB	31		P-well block layer for Native NMOS region
7	NWDMY	112		Defines the N-well resistor region and to prevent adding dummy active on N-well resistor region
8	DUMBM	157		Block layer for Dummy operation on all Metal
9	DUMBP	158		Block layer for Dummy operation on all Poly
10	DUMBA	159		Block layer for Dummy operation on all active
11	NODMF	160		Block layer for all dummy operations
12	NOOPC	181		Block layer for all OPC operations
13	HT	185		Mark layer for PSM area, half tone

4.2 Mask Information

Scope：
0.153um 5V CMOS EN Process

No.	Mask ID	Layer	Digitized Area	Digitized Tone	Drawn/ Generated	Description
Baseline Layout Layer						
1	TO	Active	Active	Dark	Drawn	Active
2	TB	N-well	N-well	Clear	Drawn	N-Well implant
3	PT	P-well	N-well	Dark	Generated	P-Well implant
7	GT	Poly	Poly	Dark	Drawn	Gate of the N & P channel
8	SN	N+	N+	Clear	Drawn	N+ implant
9	SP	P+	P+	Clear	Drawn	P+ implant
10	SI	SAB	SAB	Dark	Drawn	Salicide Block
11	W1	Contact	Contact	Clear	Drawn	Metal 1 Contact to Poly or Active
12	A1	Metal1	Metal1	Dark	Drawn	Metal1 interconnect
13	W2	Via1	Via1	Clear	Drawn	Metal1 Contact to Metal2
14	A2	Metal2	Metal2	Dark	Drawn	Metal2 interconnect
15	W3	Via2	Via2	Clear	Drawn	Metal2 Contact to Metal3
16	A3	Metal3	Metal3	Dark	Drawn	Metal3 interconnect
17	W4	Via3	Via3	Clear	Drawn	Metal3 Contact to Metal4
18	A4	Metal4	Metal4	Dark	Drawn	Metal4 interconnect
19	W5	Via4	Via4	Clear	Drawn	Metal4 Contact to Meta5
20	A5	Metal5	Metal5	Dark	Drawn	Metal5 interconnect
21	WT	Top Via	Top Via	Clear	Drawn	Metal5 Contact to Top Metal
22	AT	Top Metal	Top Metal	Dark	Drawn	Top Metal interconnect
23	CP	Pad	Pad	Clear	Drawn	Bond Pad opening
optional Layout Layer						
24	DN	Deep N-well	Deep N-well	Clear	Drawn	Isolated P-well for NMOS and parasitic VNPN
25	HR	High resistor	High resistor	Clear	Drawn	Poly High Resistor implant
27	CT	MIM	MIM	Dark	Drawn	MIM Capacitor Top
28	MT	Dual MIM	Dual MIM	Dark	Drawn	Dual MIM Capacitor Top
29	TT	Top Thick Metal	Top Thick Metal	Dark	Drawn	Top Thick Metal

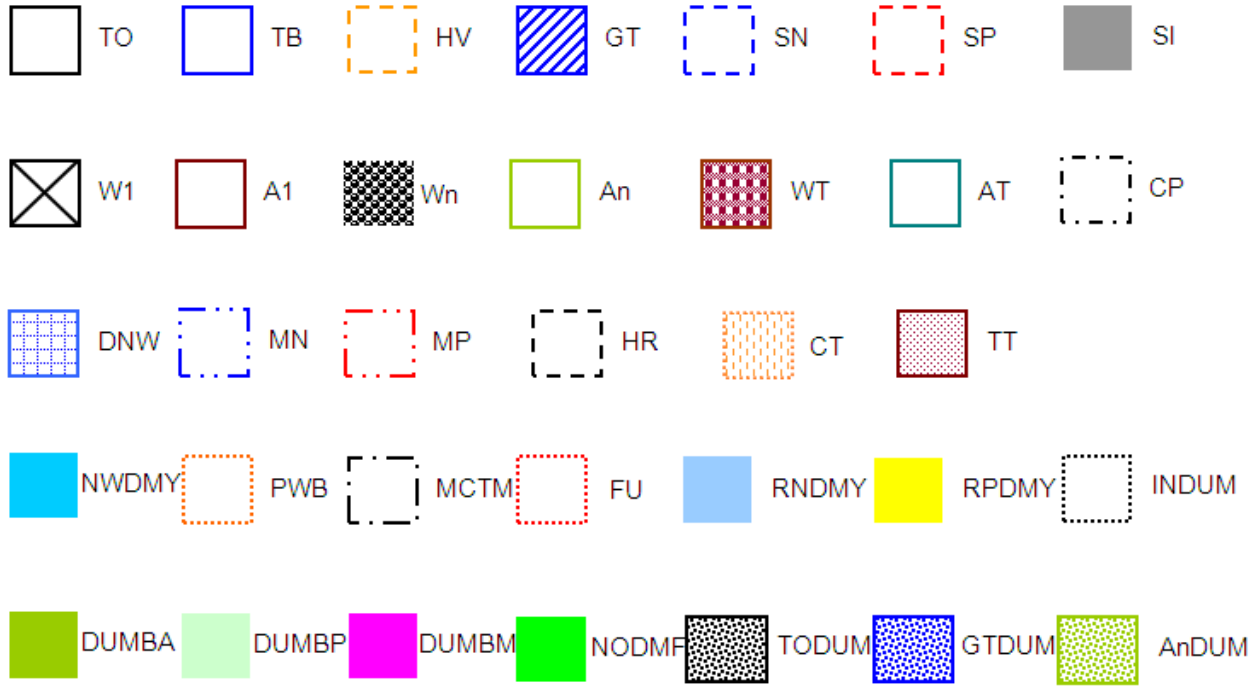
4.3 Special Layer for Logic Operation

Drawing Layer only for Logic Operation			
No.	**Layer Name**	**Layer No.**	**Description**
1	PWB	31	P-well block layer for Native NMOS region
3	FU*	81	Fuse mark layer
4	NWDMY	112	Defines the N-well resistor region and to prevent adding dummy active on N-well resistor region
5	INDUM	117	Inductor mark layer
6	MCTM	151	MIM Capacitor top plate mark layer
9	DUMBM	157	Block layer for Dummy operation on all Metal
10	DUMBP	158	Block layer for Dummy operation on all Poly
11	DUMBA	159	Block layer for Dummy operation on all Active
12	NODMF	160	Block layer for all dummy operations
Generated Layer after Logic Operation			
No.	**Layer Name**	**Layer No.**	**Description**
1	TODUM	148	Generated layer for dummy Active

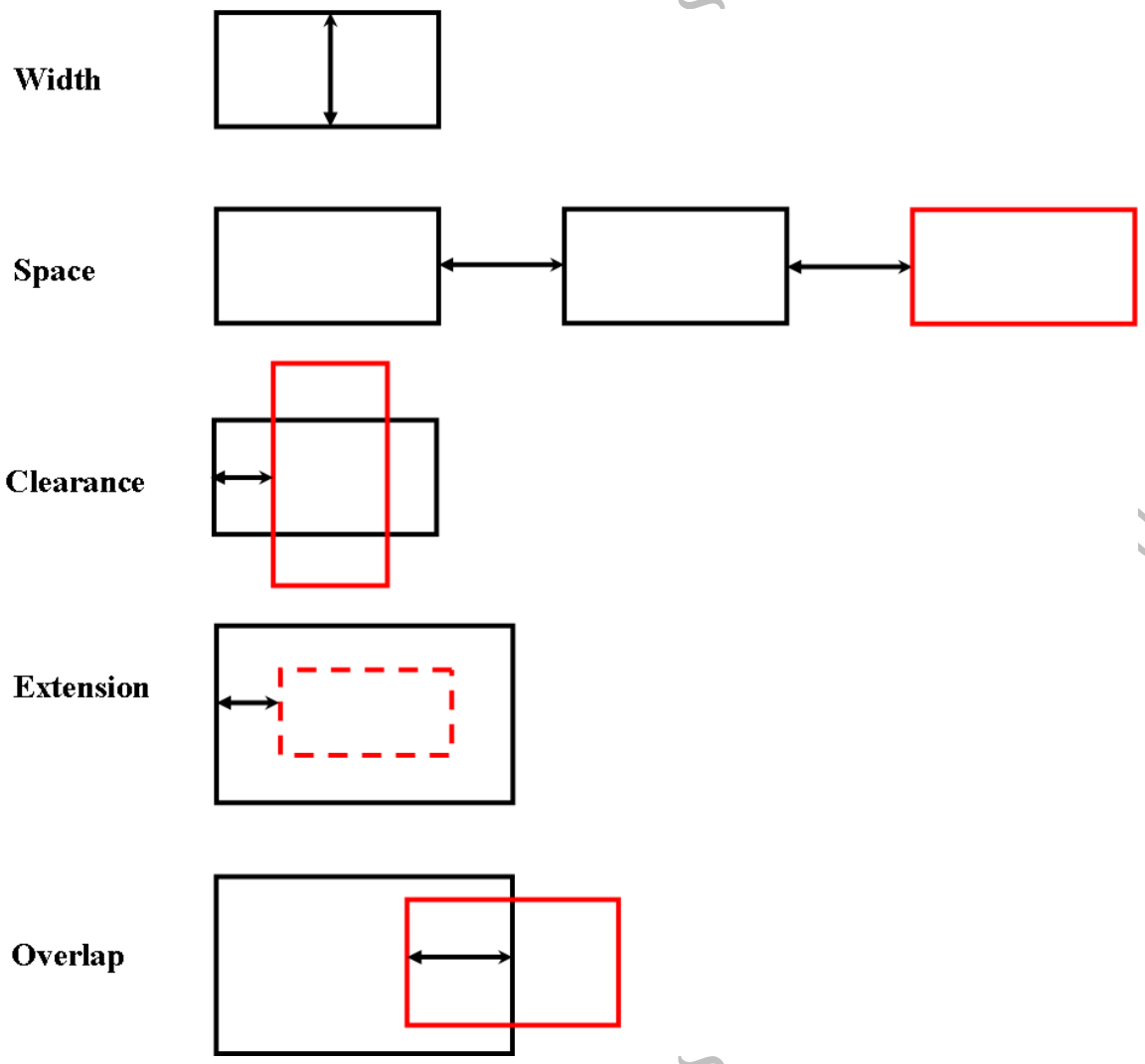
2	GTDUM	149	Generated layer for dummy Poly
3	A1DUM	170	Generated layer for dummy A1
4	A2DUM	171	Generated layer for dummy A2
5	A3DUM	172	Generated layer for dummy A3
6	A4DUM	173	Generated layer for dummy A4
7	A5DUM	174	Generated layer for dummy A5
8	ATDUM	175	Generated layer for dummy AT
9	TTDUM	176	Generated layer for dummy TT

* All fuse structure (such as poly and metal fuse) need add FU mark layer to avoid adding TO, GT and metal dummy. For poly Fuse, please refer to “Electrical Poly1 Fuse Design Guideline for 5V Operating Voltage-FAB2”

4.4 Layout Figures Legend



4.5 Definition of the Layout Layers

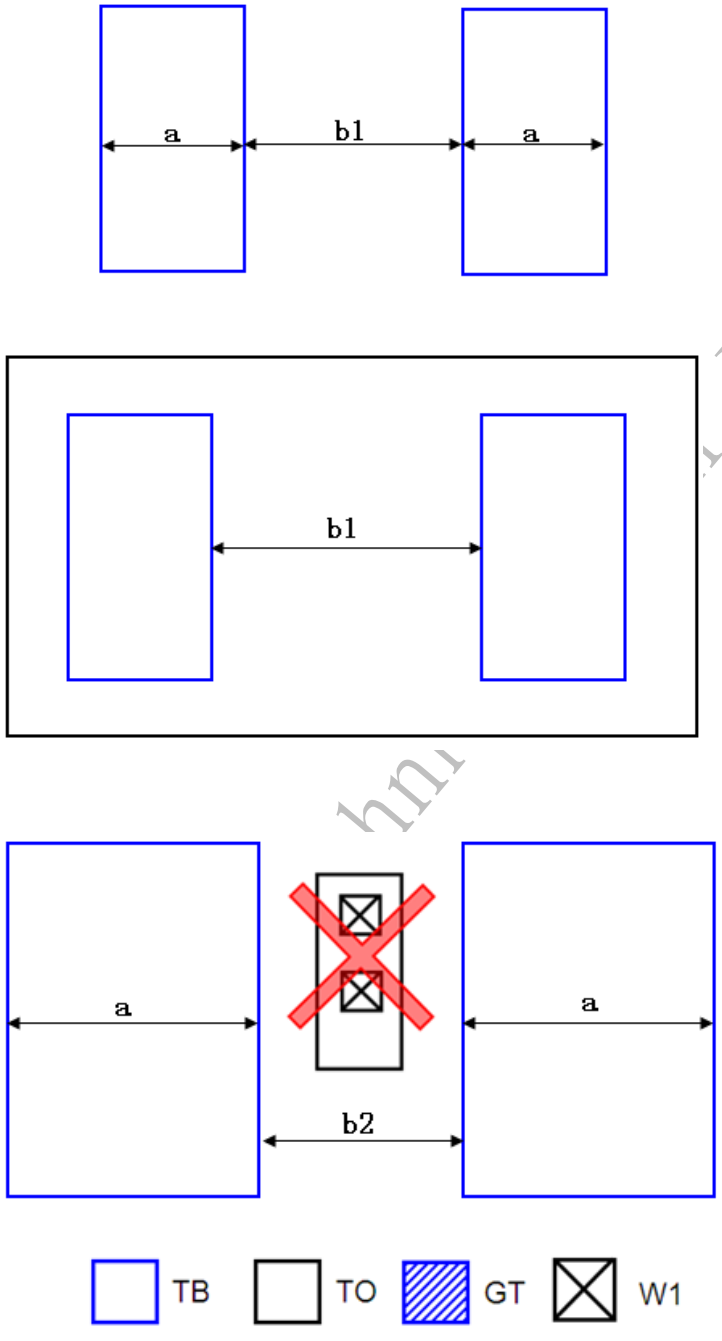


5.0 Topological Design Rule

Ⅰ Baseline Layer Layout Design Rule

5.1 TB (N-well)

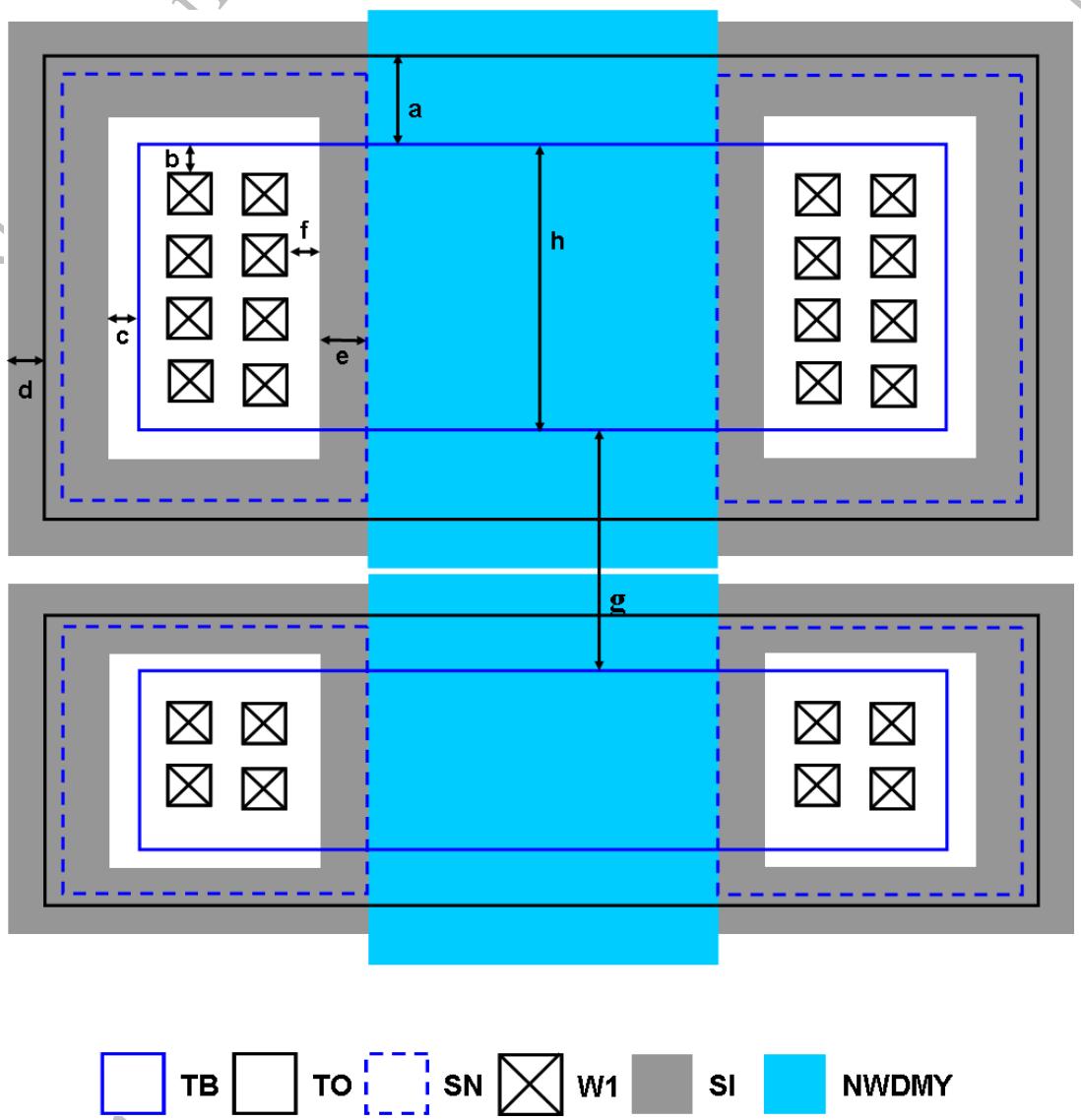
No.	Description	Rule(um)
a	Minimum width of TB	0.8
b1	Minimum space of TB with different potential.	1.53
	Minimum space of TB (on the same TO) with different potential.	1.8
b2	Minimum space of TB with the same potential. Merge if space is less than 0.6um	0.8
c	Minimum width of hot TB (not connect to the most positive power supply)	1.784
d	Minimum area: 4.0um^2	
e	TO between two TB area is not allowed while the TB space ≤0.96um	



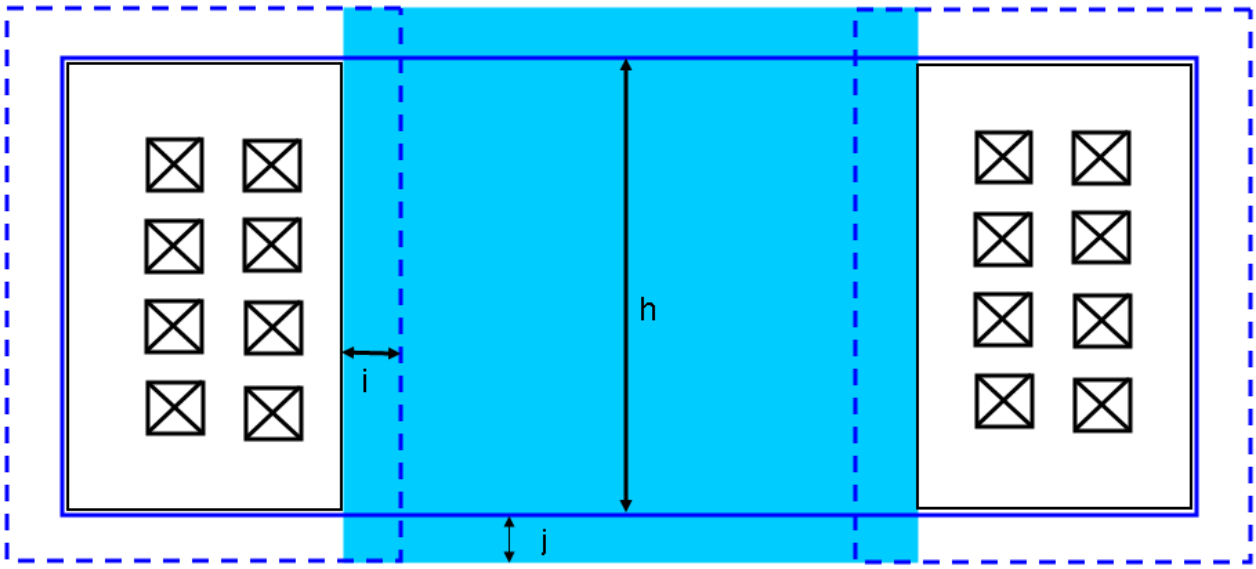
N-well Resistor

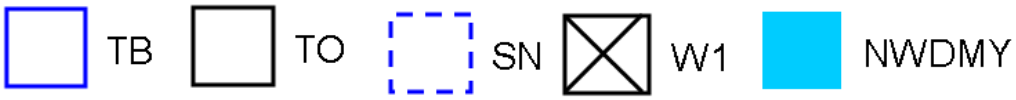
No.	Description	Rule(um)
a	Minimum extension of TO beyond TB	0.85
b	Minimum extension of TB region beyond W1 with salicide	0.254
c	Minimum clearance from TB region to SI	0.254
d	Minimum extension of SI beyond TO	0.186
e	Minimum overlap of SN and SI in TB	0.34
f	Minimum clearance from SI beyond W1 in TB	0.254
g	Minimum space of TB under STI	1.53
	Minimum space of TB under Active	1.8
h	Minimum TB width of N-well Resistor	1.7
i	Minimum extension of SN beyond TO for N-well resistor under STI	0.152
j	Min Clearance from NWDMY to TB（NWDMY layer in order to avoid add TO dummy after logic operation）	0.254
k	N+/P+ implant inside N-well resistor area is forbidden	
l	N-well resistor only for 5V work voltage application	

N-well Resistor within Active

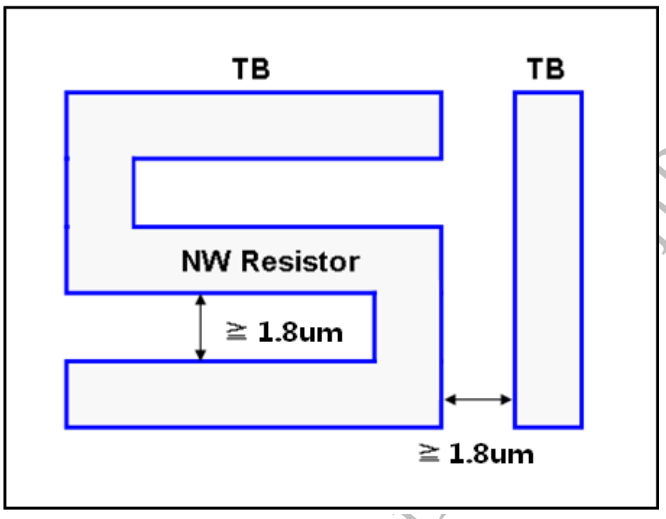


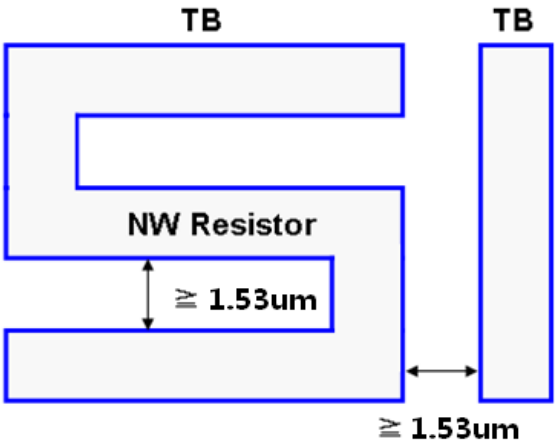
N-well Resistor under STI





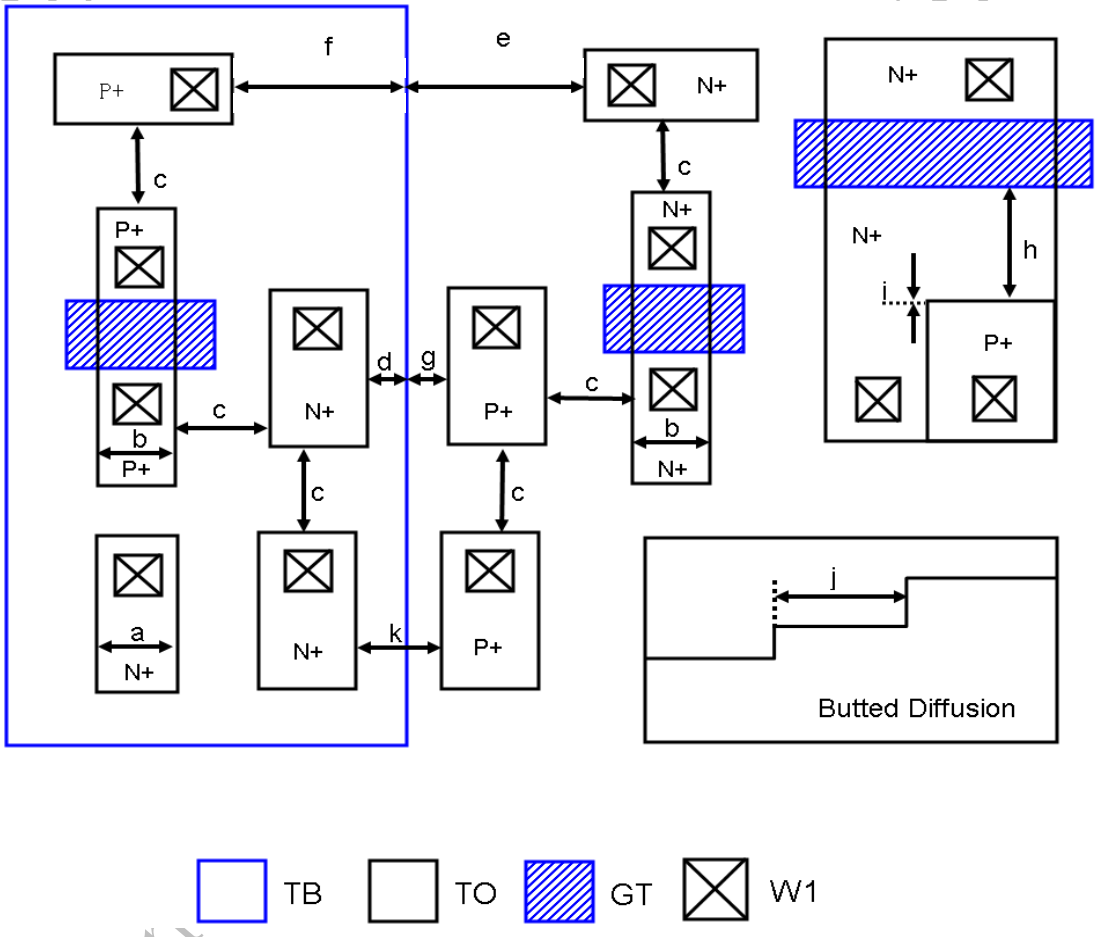
In order to ensure N-well resistor accuracy, N-well resistor minimum dimension is1.7um, square number Nsq≧**5** and minimum space is 1.53um under STI and is 1.8um under Active., N-well resistor can be designed as the below pattern





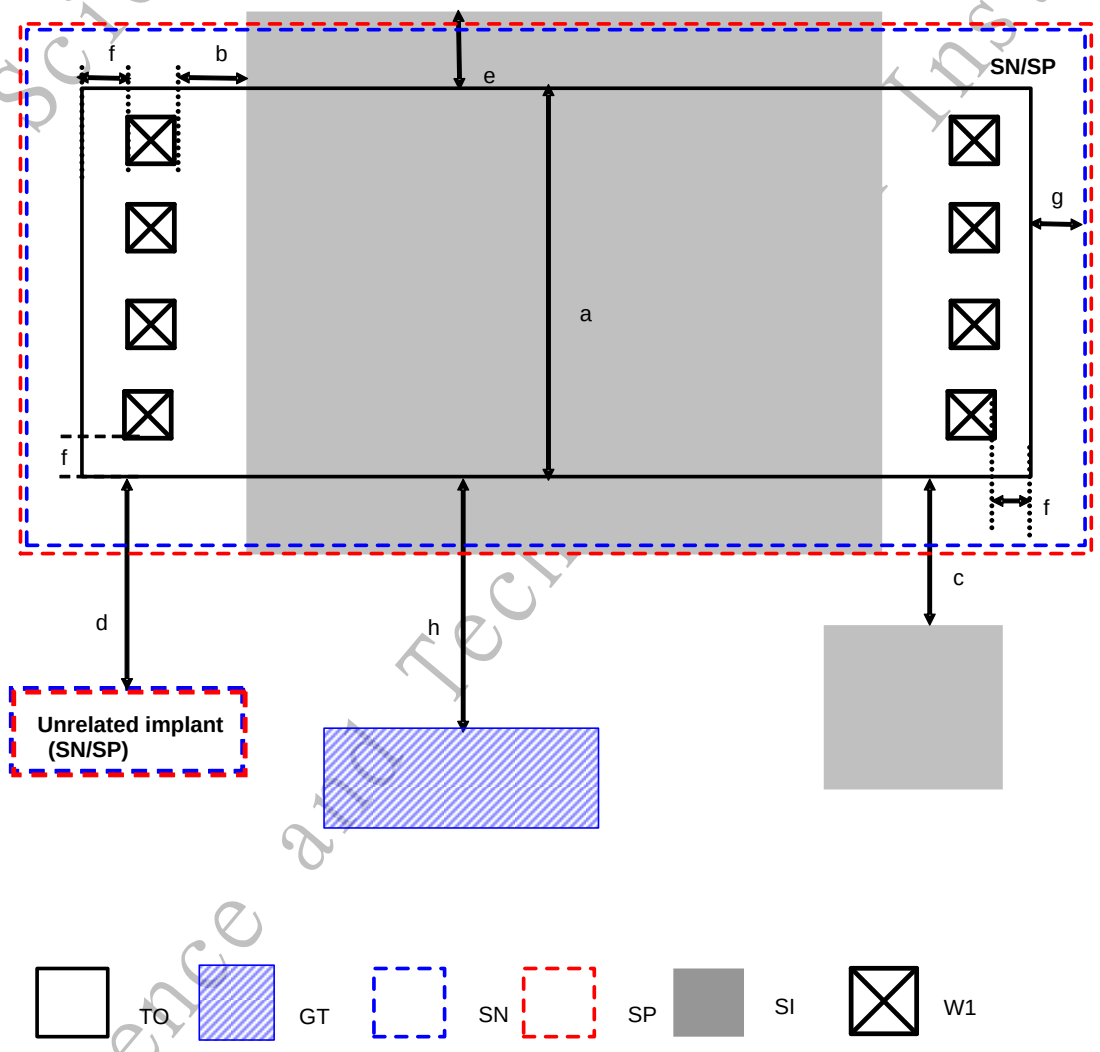
5.2 TO (Active)

No.	Description	Rule(um)
a	Minimum TO width for interconnect	0.186
b	Minimum TO width of channel width (NMOS and PMOS)	0.186
c	Minimum space of TO (N+ to N+ TO,P+ to P+ TO or N+ to P+ TO inside or outside a TB)	0.238
d	Minimum extension of TB edge beyond N+ TO within TB	0.102
e	Minimum space of TB edge to N+ TO outside TB	0.45
f	Minimum extension of TB edge beyond P+ TO inside TB	0.45
g	Minimum space of TB edge to P+ TO outside TB	0.102
h	Minimum clearance from GT edge to the edge of butted TO	0.272
i	Minimum space of N+ TO to P+ TO for butted TO	0
j	Minimum width of one or more segment of the consecutive P+ butted TO or N+ butted TO	0.326
k	In order to meet the implant rules, When N+ TO within TB and P+ TO outside TB are put head-to-head across the boundary of well, the space of N+ TO within TB to P+ TO outside TB	0.304
l	Minimum TO area of a stand alone region: 0.2 um^2	
m	Minimum TO area of a butted TO: 0.13 um^2	
n	Length and width should be less than 60um	



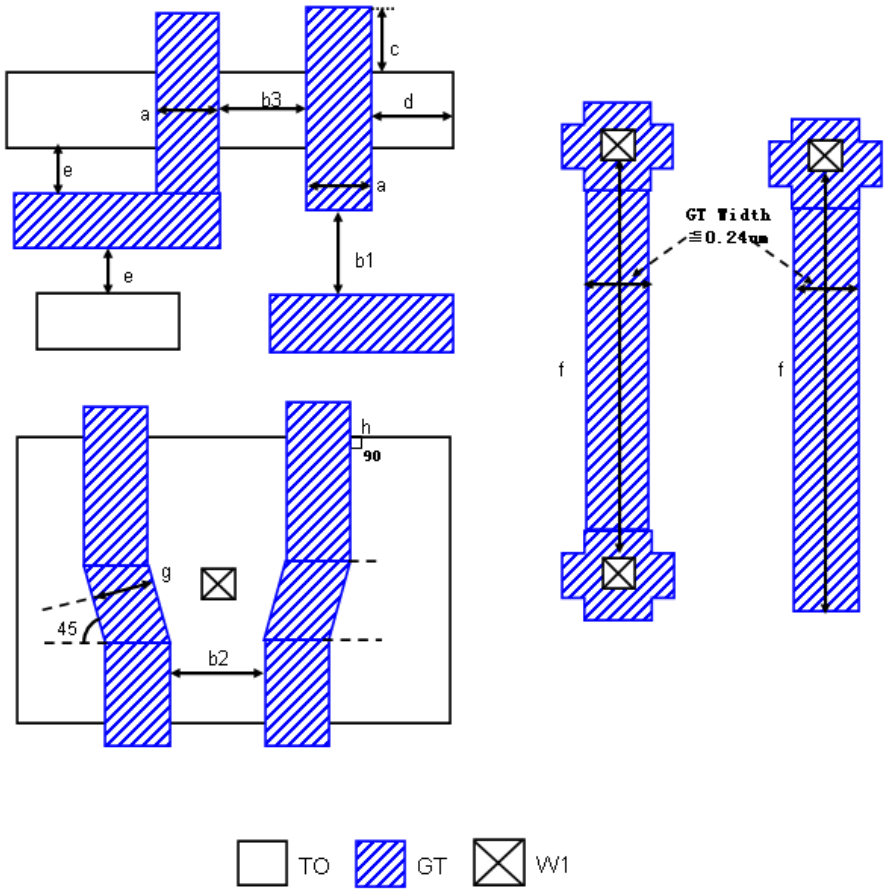
Active Resistor

No.	Description	Rule(um)
a	Minimum width of TO for Active resistor (Nsq≧5) Strongly Recommended: Active resistor minimum width is 2um for mismatch and accuracy concern	1
b	Minimum space of SI to W1 on TO for Active resistor	0.15
c	Minimum space of unrelated SI to TO for Active resistor	0.254
d	Minimum space of unrelated implant region to TO for Active resistor	0.22
e	Minimum clearance from SI to TO for Active resistor	0.186
f	Minimum extension of TO beyond W1	0.07
g	Minimum extension of SN or SP beyond TO for Active resistor	0.152
h	Minimum space of unrelated GT to TO for Active resistor	0.51
I	Recommend :The W1 for active resistor pick-up should be layout as single column	
j	Dog-bone is not recommended at the end of Active resistor for W1 pick-up	



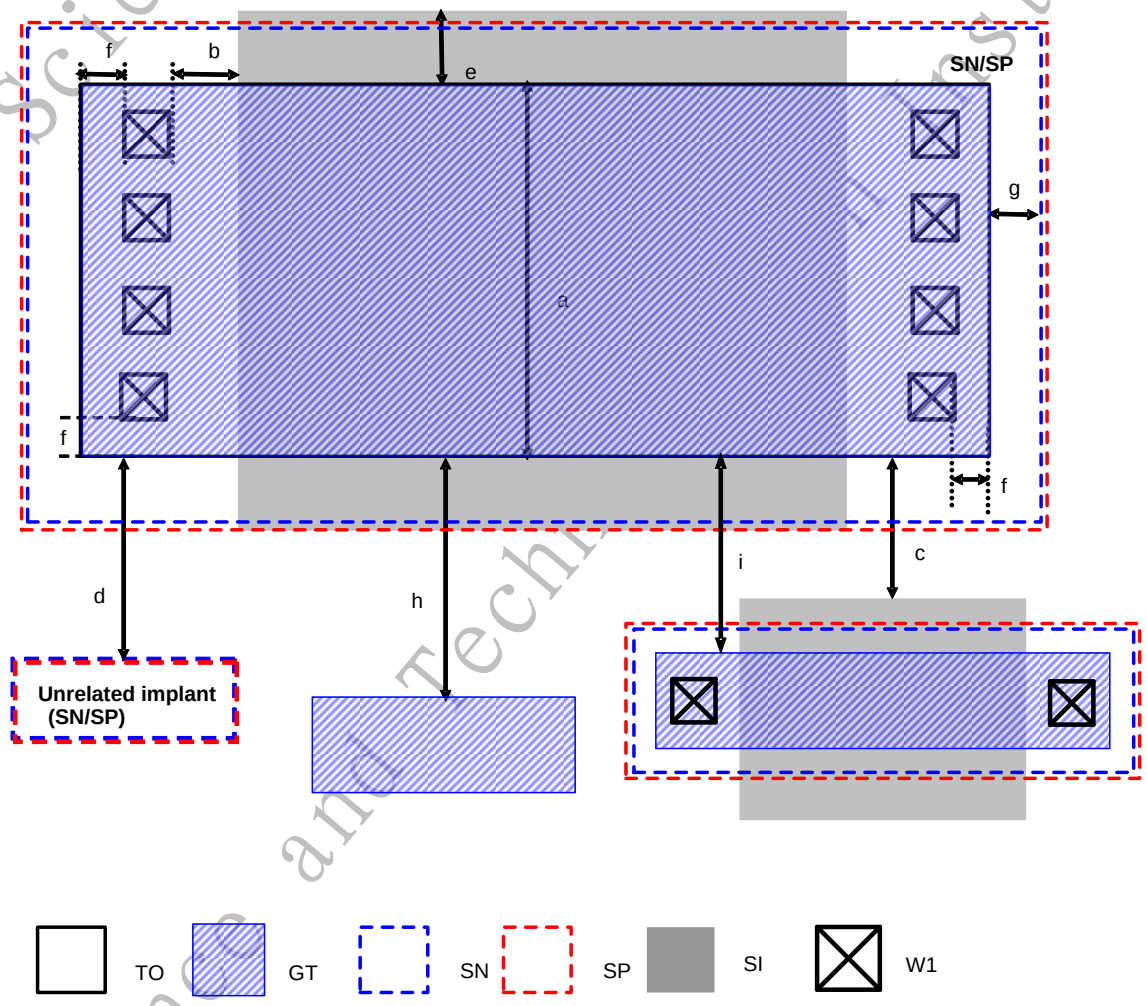
5.3 GT (Poly)

No.	Description	Rule(um)
a	Minimum GT width for interconnection	0.18
	Minimum GT width for 5V HV NMOS channel length	0.50
	Minimum GT width for 5V HV PMOS channel length	0.42
b	b1 Minimum space of GT on field oxide	0.212
	b2 Minimum space of two GT with W1 on TO	0.318
	b3 Minimum space of GT on TO	0.25
c	Minimum clearance of GT extended into field oxide (End cap)	0.186
d	Minimum clearance from TO to GT	0.27
e	Minimum space of GT to TO	0.084
f	Maximum length of salicide GT not on TO between two contacts when GT width is less than or equal to 0.24um	50
	Maximum length of salicide GT not on TO between one contact and GT line end when GT width is less than or equal to 0.24um	50
g	Minimum GT width for NMOS channel length which has 45 degree bent on TO	0.54
	Minimum GT width for PMOS channel length which has 45 degree bent on TO	0.46
	Minimum GT width which has 45 degree bent on field oxide	0.26
h	GT must enter the TO region perpendicularly(horizontal or vertical direction)	
i	Bent Poly is permitted only 45 degree	
j	GT pattern density must be greater than 15%.If not, adding GT dummy pattern not on TO region	
k	Minimum space between poly interconnects with one or both poly width and length are grater than 0.28um and 0.5um respectively	0.22



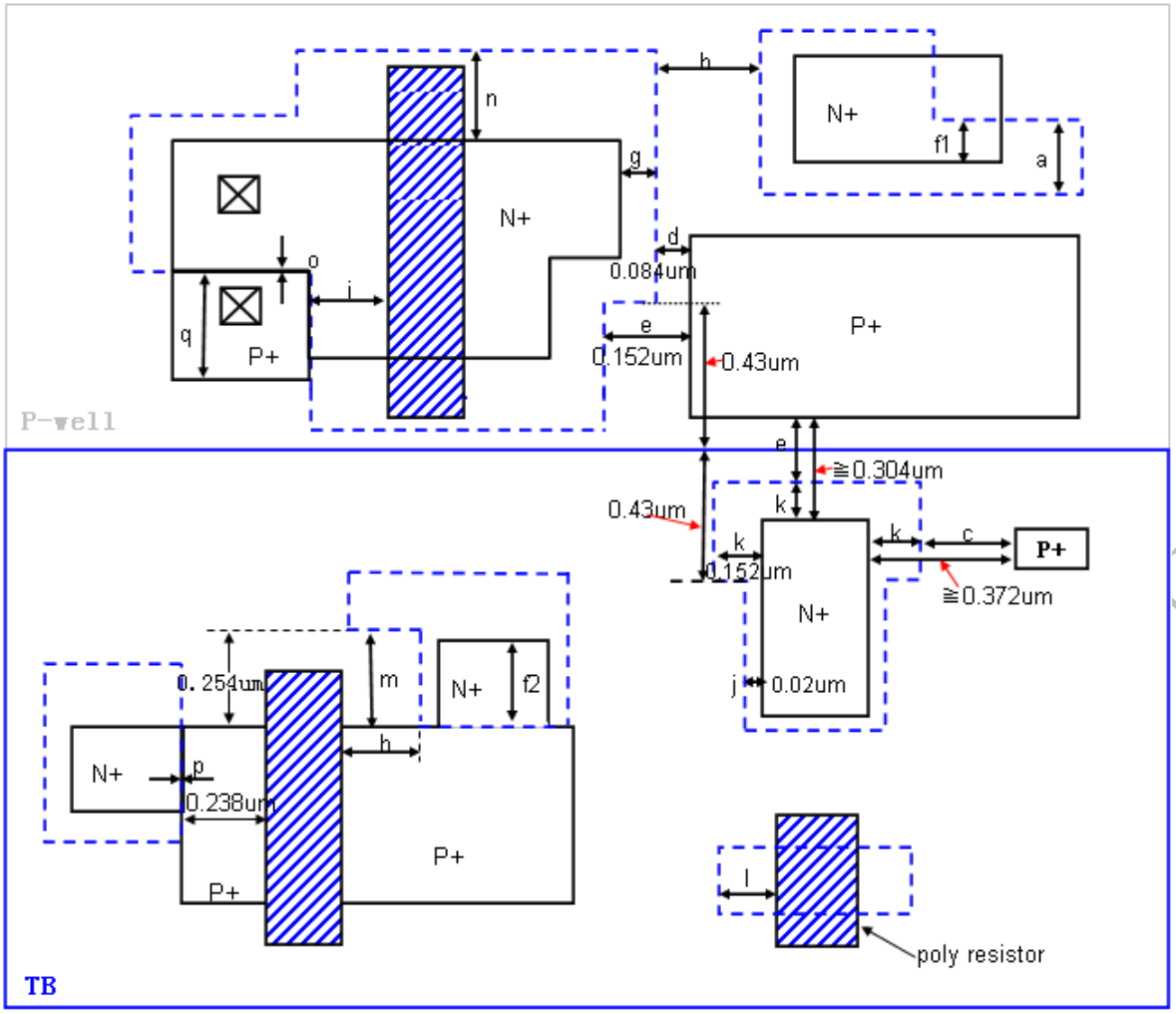
Poly resistor (Not Including Poly HR)

No.	Description	Rule(um)
a	Minimum width of GT for poly resistor (Nsq >=5) Recommend: Poly resistor minimum width is 2um for mismatch and accuracy concern	1
b	Minimum space of SI to W1 on TO or GT	0.15
c	Minimum space of unrelated SI to GT for poly resistor	0.254
d	Minimum space of unrelated implant region to GT for Poly resistor	0.22
e	Minimum clearance from SI to GT for Poly resistor	0.186
f	Minimum extension of GT for poly resistor beyond W1	0.07
g	Minimum extension of SN or SP beyond GT for Poly resistor	0.152
h	Minimum space of unrelated GT to GT for poly resistor	0.51
i	Minimum space of GT for Poly resistor	0.34
j	Recommend :The W1 for Poly resistor pick-up should be layout as single column	
k	Dog-bone is not recommended at the end of Poly resistor for W1 pick-up	
l	Poly resistor laid on TO is not recommended	



5.4 SN (N+ implant area)

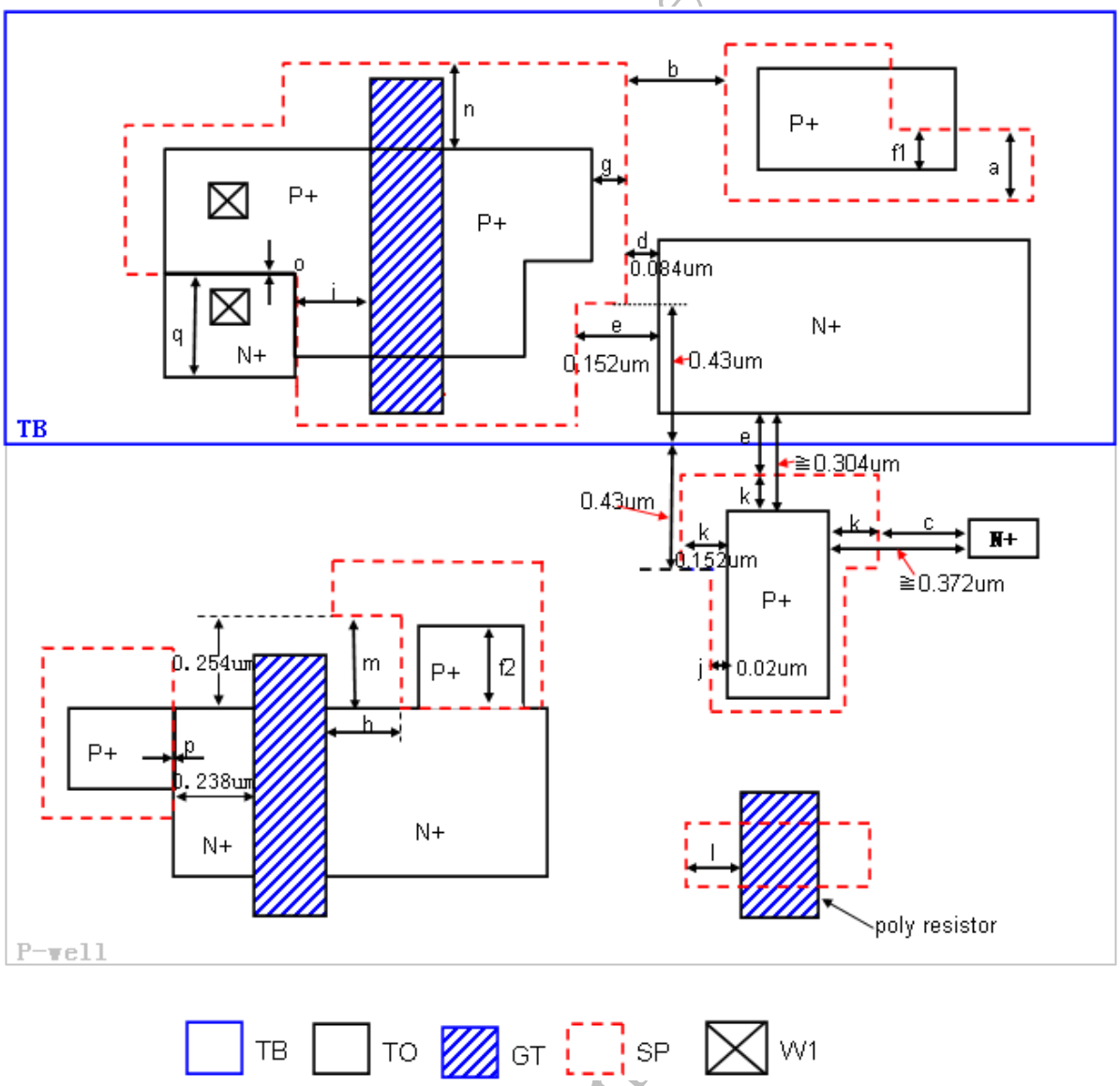
No.	Description	Rule(um)
a	Minimum width of SN	0.356
b	Minimum space of SN (if the space is less than 0.358um, please merge it)	0.356
	Minimum space of SN on STI (if the space is less than 0.42um, please merge it)	0.42
c	Minimum space of SN to P+ TO inside TB	0.22
d	Minimum space of SN to P+ TO outside TB (non-butted TO) if the distance between P+ TO outside TB and TB >=0.43um	0.084
e	Minimum space of SN to P+ TO outside TB(non-butted TO) if the distance between P+ TO outside TB and TB<0.43um	0.152
f	f1 Minimum overlap of SN and TO	0.194
	f2 Minimum overlap of SN and TO (Butted rules)	0.17
g	Minimum extension of SN region beyond N+ TO region	0.152
h	Minimum space of SN edge to a P-channel poly gate	0.238
i	Minimum clearance of SN region beyond N-channel poly gate	0.45
j	Minimum extension of SN region beyond N+ TO within TB if the distance between N+ TO within TB and TB >= 0.43um	0.02
k	Minimum extension of SN region beyond N+ TO within TB, if the distance between N+ TO within TB and TB < 0.43um To obey the rule “k” and “c” simultaneously, the minimum space of N+ TO within TB to P+ TO increased to 0.372um To obey the rule “k” and “e” simultaneously, the minimum space of N+ TO within TB to P+ TO increased to 0.304um	0.152
l	Minimum clearance from SN region to poly resistor.(Npoly resistor with SAB and SN implant).	0.152
m	Minimum space of SN region to P+ TO along the direction of poly gate width	0.31
n	Minimum extension of SN region beyond N+ TO along the direction of poly gate width	0.296
o	Minimum space of SN to the butted diffusion P+ TO (outside TB)	0
p	Minimum space of SN region to the edge of a butted diffusion N+ TO within TB /P+ TO	0
q	Minimum width of Butted contact region	0.296
r	Minimum area of Butted contact junction 0.126 um2	
s	Minimum SN area 0.4um2	
t	SN is not allowed to overlap SP	
u	It is forbidden that SN being generated by the reverse tone of SP, since this operation might violate “c” and “d”	
v	Minimum SN area for a N-channel poly gate must follow “i” and “n”	
w	Minimum resist pattern area within NPLUS region is 0.64um2.	



TB TO GT SN W1

5.5 SP (P+ implant)

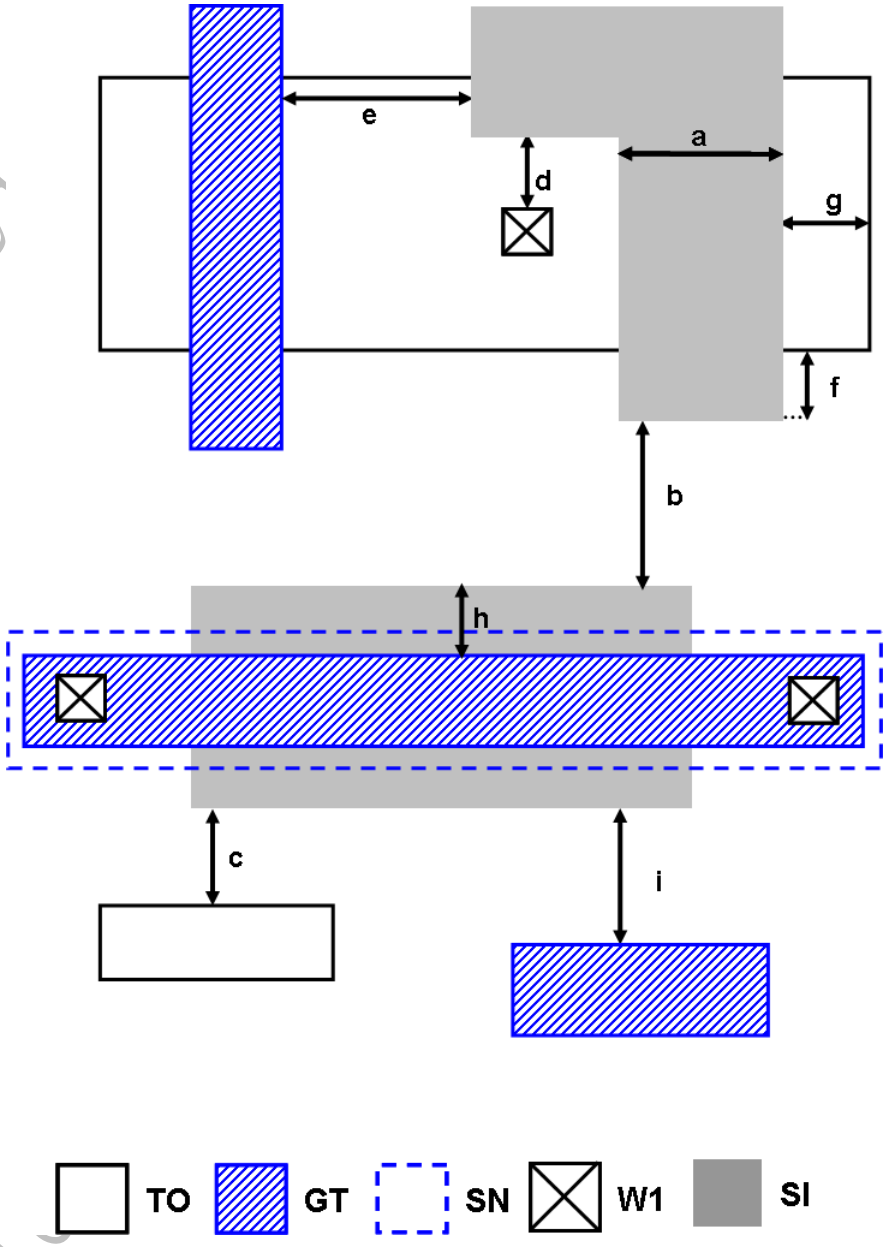
No.	Description	Rule(um)
a	Minimum width of SP	0.356
b	Minimum space of SP (if the space is less than 0.358um, please merge it)	0.356
	Minimum space of SP on STI (if the space is less than 0.42um, please merge it)	0.42
c	Minimum space of SP to a N+ TO outside TB	0.22
d	Minimum space of SP to N+ TO within TB (non-butted active).if the distance between N+ TO within TB and TB >=0.43um	0.084
e	Minimum space of SP to N+ TO within TB (non-butted active).if the distance between N+ TO within TB and TB <0.43um	0.152
f	Minimum overlap of SP and TO	0.194
	Minimum overlap of SP and TO (Butted rules)	0.17
g	Minimum extension of SP region beyond P+ TO inside TB region	0.152
h	Minimum clearance from SP edge to a N-channel or P-channel poly gate	0.238
i	Minimum extension of a SP region beyond a P-channel poly gate	0.4
j	Minimum extension of a SP region beyond P+ TO outside TB if the distance between P+ TO outside TB and TB >= 0.43um	0.02
k	Minimum extension of a SP region beyond a P+ TO outside TB if the distance between P+ TO outside TB and TB < 0.43um To obey this rule and “c” simultaneously, the minimum space of P+ TO outside TB to P+ TO outside TB increased to 0.372um To obey this rule and “e” simultaneously, the minimum space of P+ TO outside TB to P+ TO outside TB increased to 0.304um	0.152
l	Minimum extension of a SP region beyond a resistor poly(Ppoly resistor with SAB and SP implant).	0.152
m	Minimum space of SP edge to a N+ TO along the direction of poly gate width	0.254
n	Minimum extension of a SP region beyond P-channel along the direction of poly gate	0.296
o	Separation from a SP to a butted edge of a butted diffusion N+ TO (inside TB)	0
p	Minimum space of a SP region beyond the edge of a butted diffusion N+ TO/ P+ TO outside TB	0
q	Minimum width of Butted contact region	0.296
r	Minimum area of Butted contact junction 0.126 um^2	
s	Minimum SP area 0.4um^2	
t	SP is not allowed to overlap SN	
u	It is forbidden that SP being generated by the reverse tone of SN, since this operation might violate “c” and “d”	
v	Minimum SP area for a P-channel poly gate must follow “i” and “n”	
w	Minimum resist pattern area within PPLUS region is 0.64um^2.	



TB TO GT SP W1

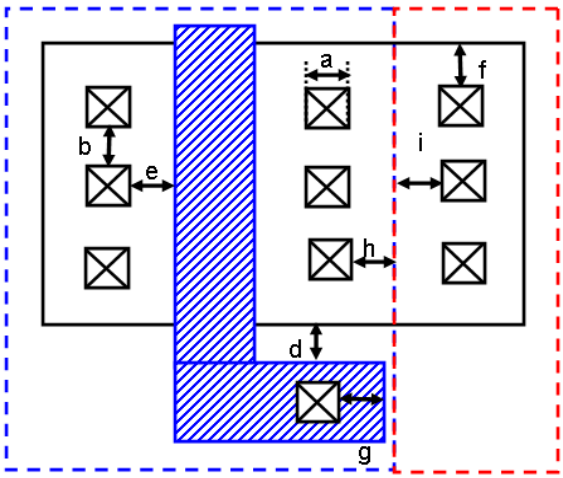
5.6 SI (SAB-Salicide Block)

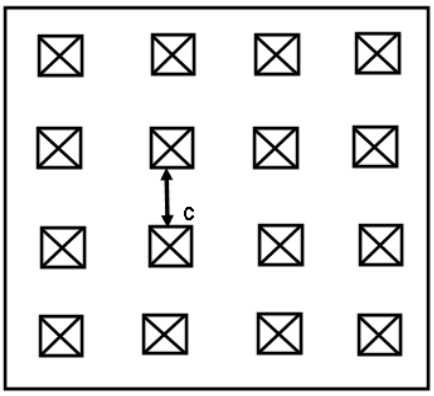
No.	Description	Rule(um)
a	Minimum width of SI	0.356
b	Minimum space of SI	0.356
c	Minimum space of SI to unrelated TO	0.186
d	Minimum space of SI to W1	0.15
e	Minimum space of SI to GT on TO	0.238
f	Minimum clearance from SI extend over TO	0.186
g	Minimum clearance from SI to TO	0.186
h	Minimum clearance from SI to related GT not on TO	0.186
i	Minimum space of SI to unrelated GT not on TO	0.254
j	Minimum area of SI is 1.7um^2	
k	Contacts in SAB area are not allowed.	

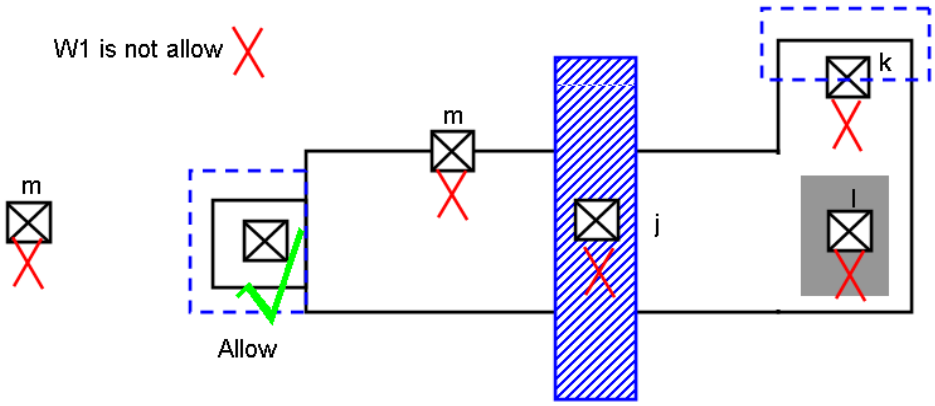


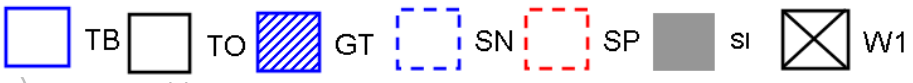
5.7 W1 (Contact)

No.	Description	Rule(um)
a	Minimum and Maximum size of W1	0.186
b	Minimum space of W1	0.212
c	Minimum space when the row and column numbers are both greater than 3 in the contact array	0.238
d	Minimum space from W1 on GT to TO	0.144
e	Minimum space of GT to W1 on TO	0.14
f	Minimum extension of TO beyond W1	0.07
g	Minimum extension of GT beyond W1	0.07
h	Minimum extension of SN beyond W1	0.102
i	Minimum extension of SP beyond W1	0.102
j	W1 on GT is forbidden to locate active region	
k	W1 on TO is not allowed to locate on the boundary of N+ TO and P+ TO	
l	Non-salicide W1 is not allowed	
m	W1 without the cover of GT or TO is not allowed	
n	Recommend placing 2 contacts on one node if possible	



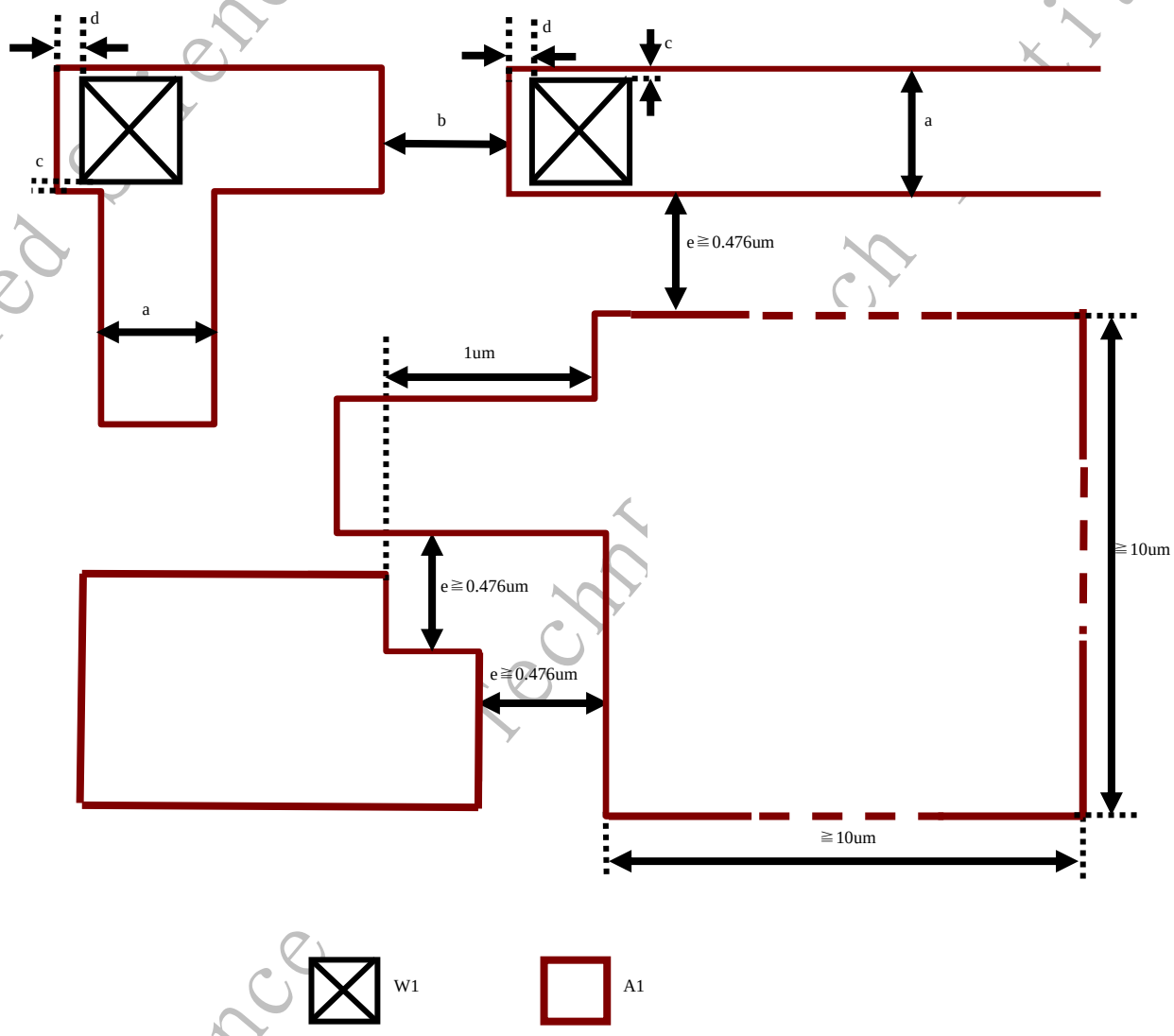






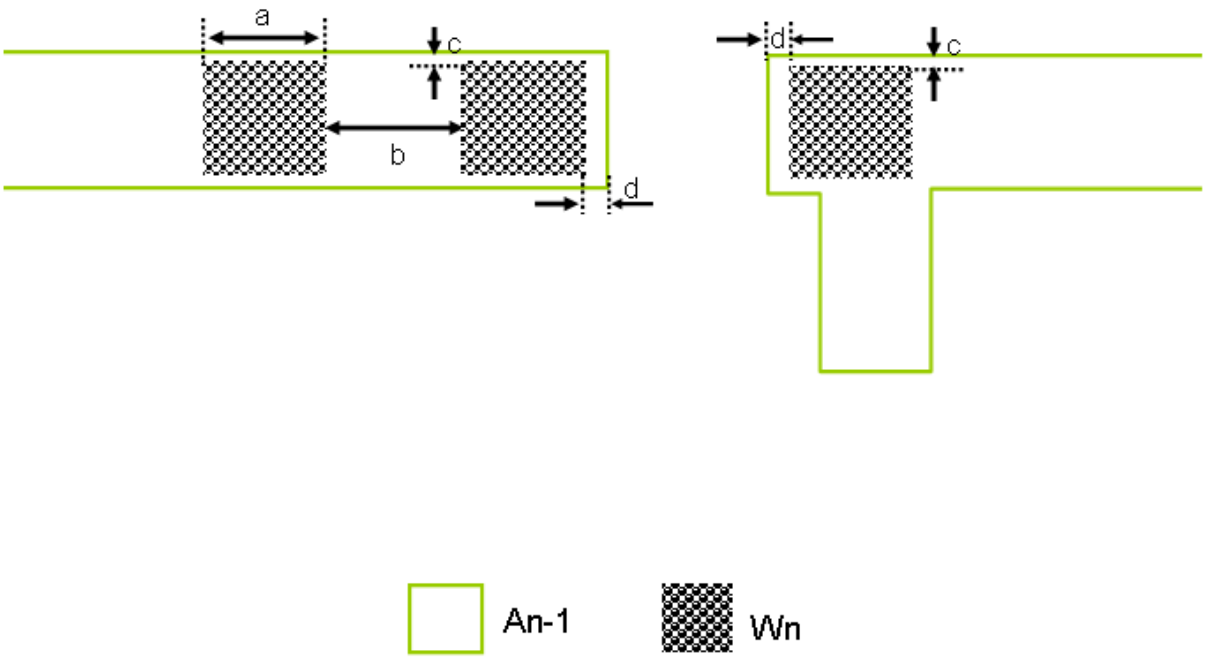
5.8 A1 (Metal 1)

No.	Description	Rule(um)
a	Minimum width of A1	0.194
b	Minimum space of A1	0.194
c	Minimum extension of A1 region beyond W1	0.004
d	Minimum extension of A1 line end region beyond W1(When W1 at 90 degree corner, one side of metal extension must be considered as line end region)	0.05
e	Minimum space of A1 lines with one or both metal line width and length are greater than 10um; the minimum space must be maintained between a metal line and a small piece of metal (<10um) that is connected to the wide metal within 1.0 um range from the wide metal	0.476
f	Metal density if less than 30%, please add dummy metal and follow “8.29 AnDUM (Metal Dummy)”	
g	Minimum area of A1 island is $0.2um^2$	
h	For two adjacent outer corner sides, at least one side should be treated as metal line end	



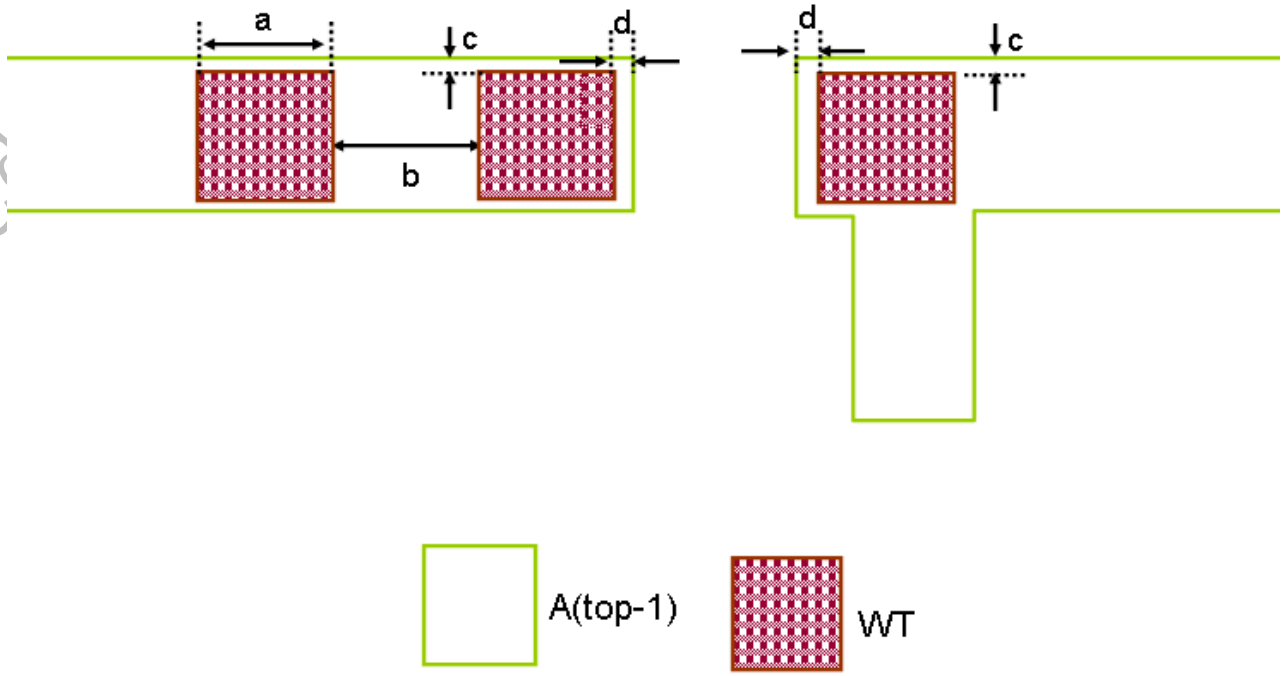
5.9 Wn (VIAn-1, n=2, 3, 4, 5)

No.	Description	Rule(um)
a	Minimum and Maximum size of Wn	0.22
b	Minimum space of Wn	0.22
c	Minimum extension from An-1 beyond Wn	0
d	Minimum extension from An-1 line end beyond Wn.	0.06
e	Wn can be fully or partially stacked on Wn-1	
f	For two adjacent outer corner sides, at least one side should be treated as metal line end	
g	Wn without An-1 and An coverage is not allowed	
h	Recommend placing 2 Wns on one node if possible	



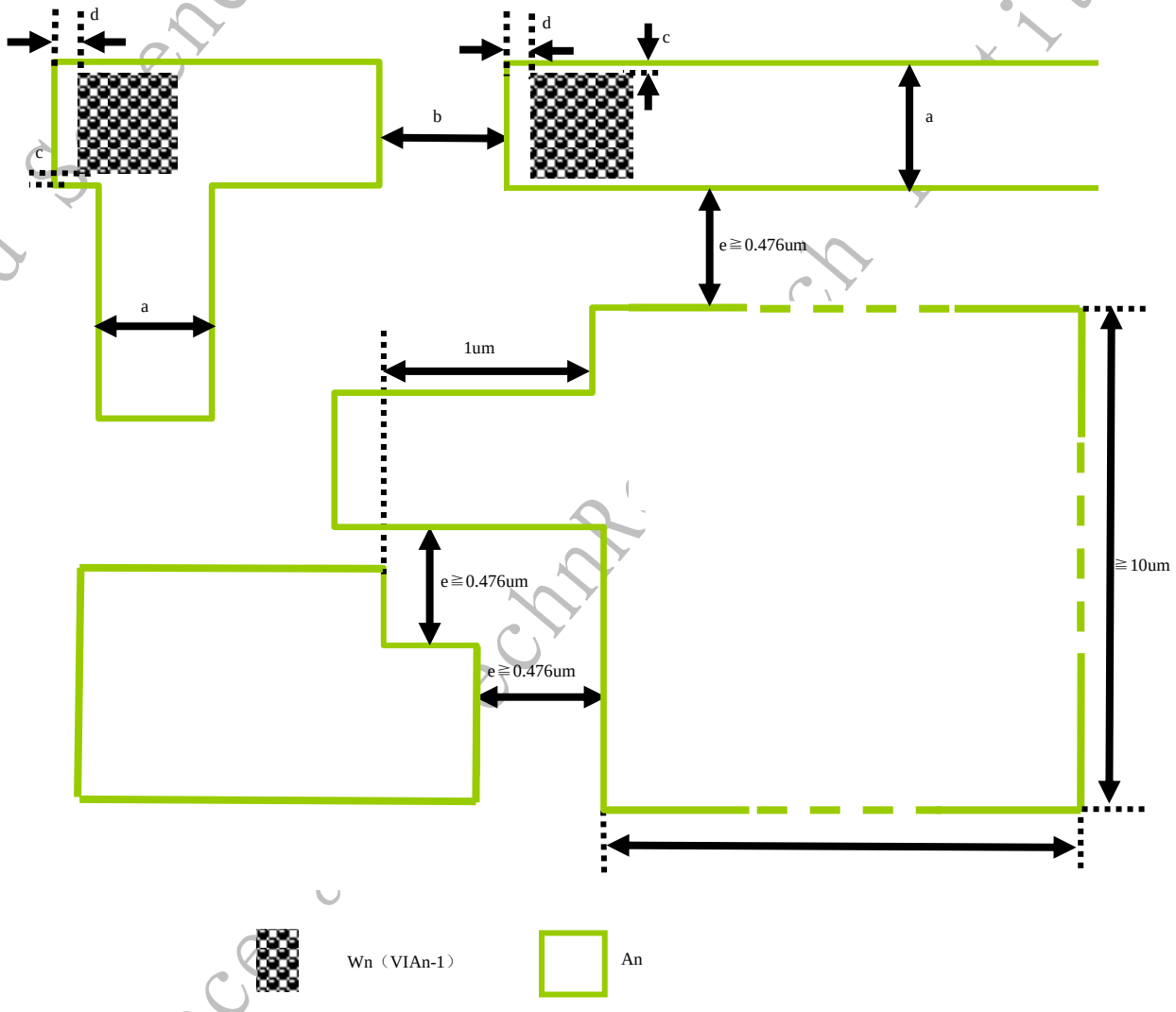
5.10 WT (Top Via)

No.	Description	Rule(um)
a	Minimum and Maximum size of WT	0.238
b	Minimum space of WT	0.238
c	Minimum extension from A(top-1) beyond WT	0
d	Minimum extension from A(top-1) line end beyond WT (When WT at 90 degree corner, one side of metal enclosure must be considered as line end region)	0.06
e	WT can be fully or partially stacked on W(top-1)	
f	For two adjacent outer corner sides, at least one side should be treated as metal line end	
g	WT without A(top-1) and AT(or TT) coverage is not allowed	
h	Recommend placing 2 Wns on one node if possible	



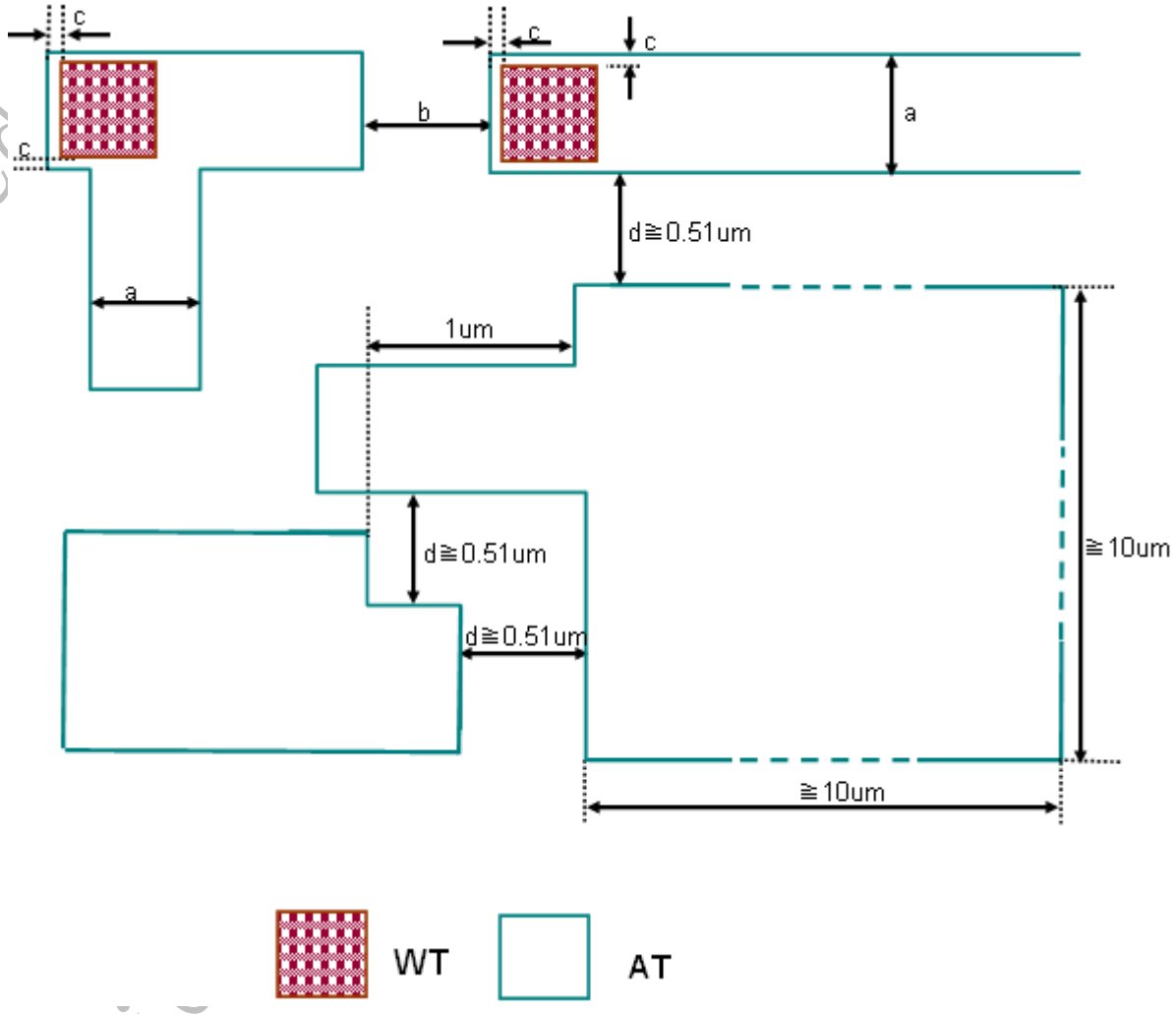
5.11 An (Metal n , n=2, 3, 4, 5)

No.	Description	Rule(um)
a	Minimum width of An	0.238
b	Minimum space of An	0.238
c	Minimum extension from An region beyond Wn region	0
d	Minimum extension from An line end region beyond Wn region(When Wn at 90 degree corner, one side of metal extension must be considered as line end region)	0.05
e	Minimum space of A1 lines with one or both metal line width and length are greater than 10um; the minimum space must be maintained between a metal line and a small piece of metal (<10um) that is connected to the wide metal within 1.0 um range from the wide metal	0.476
f	Minimum area of An island is 0.2um^2	
g	If Metal density less than 30%, please add dummy metal and follow “8.29 AnDUM (Metal Dummy)”	
h	For two adjacent outer corner sides, at least one side should be treated as metal line end	



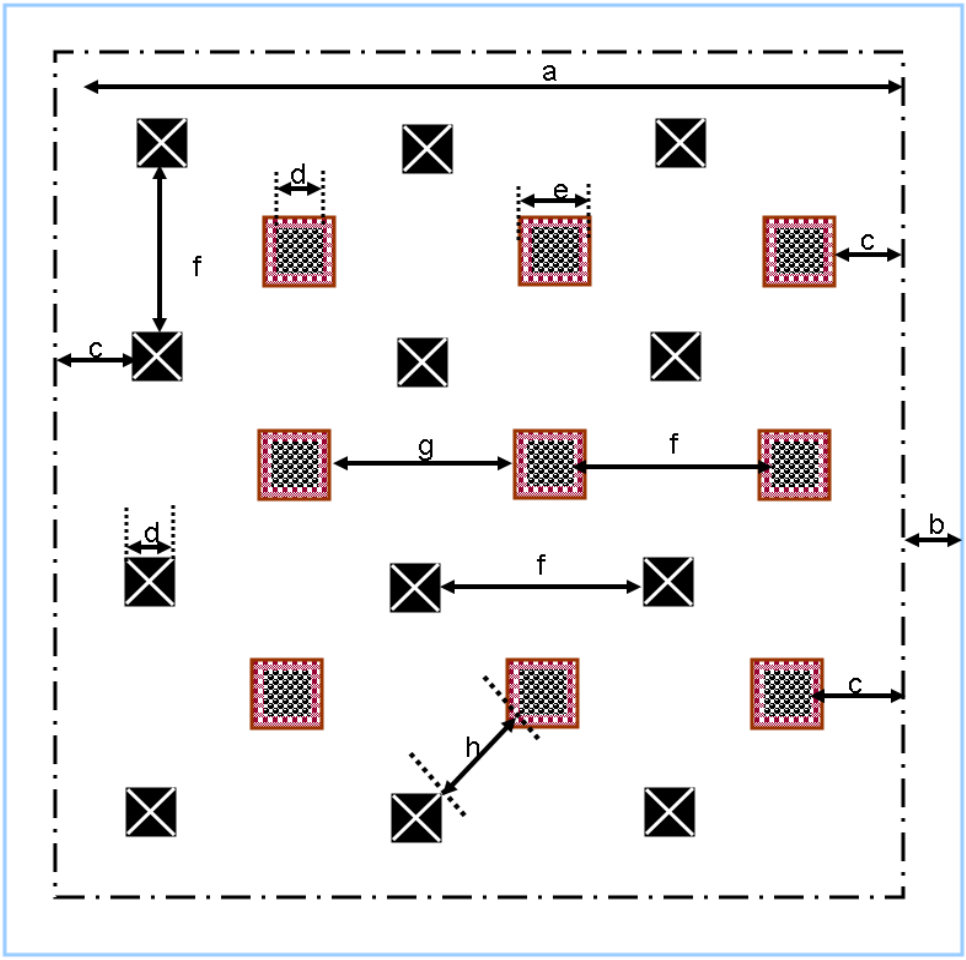
5.12 AT (Top Metal)

No.	Description	12K Metal Rule(um)
a	Minimum width of AT	0.42
b	Minimum space of AT	0.42
c	Minimum extension from AT region beyond WT region	0.07
	Minimum extension from AT end-of-line beyond WT region	0.1
	Minimum extension from AT region beyond WT region if AT width greater than 10um	0.084
	Minimum extension from AT end-of-line beyond WT region if AT width greater than 10um	0.1
d	Minimum space of top metal line with one or both top metal line width and length are greater than 10um; this also includes all metals attached to these areas or extending out for a distance of 1.0um or less	0.51
e	If Metal density less than 30%, please add dummy metal and follow “AnDUM (Metal Dummy)”,for 12KA top metal the metal density must be within 30%~80%.	
f	WT without AT coverage is not allowed	
g	Minimum area of island is 0.56 um^2	
h	For two adjacent outer corner sides, at least one side should be treated as metal line end	



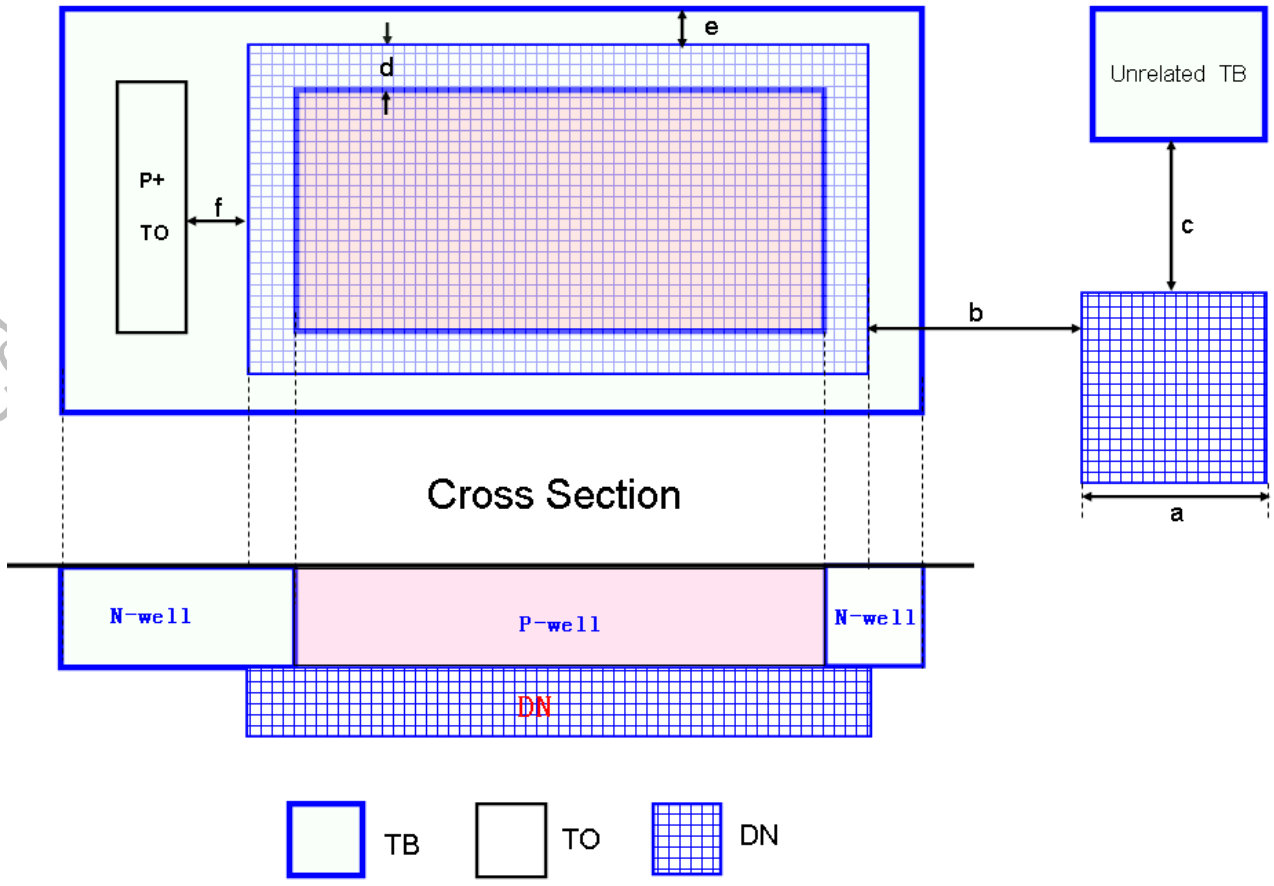
5.13 CP (Bonding Pad)

No.	Description	Rule(um)
a	Minimum CP opening	50x50
b	Minimum and Maximum extension of An or TT beyond CP (n=1~5,T)	2
c	Minimum extension of CP beyond Wn (n=2~5,T)	2.55
d	Minimum and Maximum width of Wn (n=2~5)	0.22
e	Minimum and Maximum width of WT	0.238
f	Minimum space of Wn (n=2~5)	0.382
g	Minimum space of WT	0.296
h	Minimum space of Wn (n=3,5) to Wn (n=2, 4)	0.11
i	This layer defines the opening where the bond wires connect the circuit to the lead frame. The design rule provides a reference only. The design rule of bonding pad please confirm with assembly shop before tape out, since some of rules are related to the capability of bonding	
j	For the 8K top metal, Cu wire is forbidden to the formation of bonding, we suggest Au wire. Otherwise, please confirm with CSMC.CE before tape out. And need study the golden bonding conditions with assembly shop.	
k	CP to Chip boundary =0um or >=5um(<5um has PR lift Risk), please refer to seal ring.	



5.14 DN (Deep N-well)

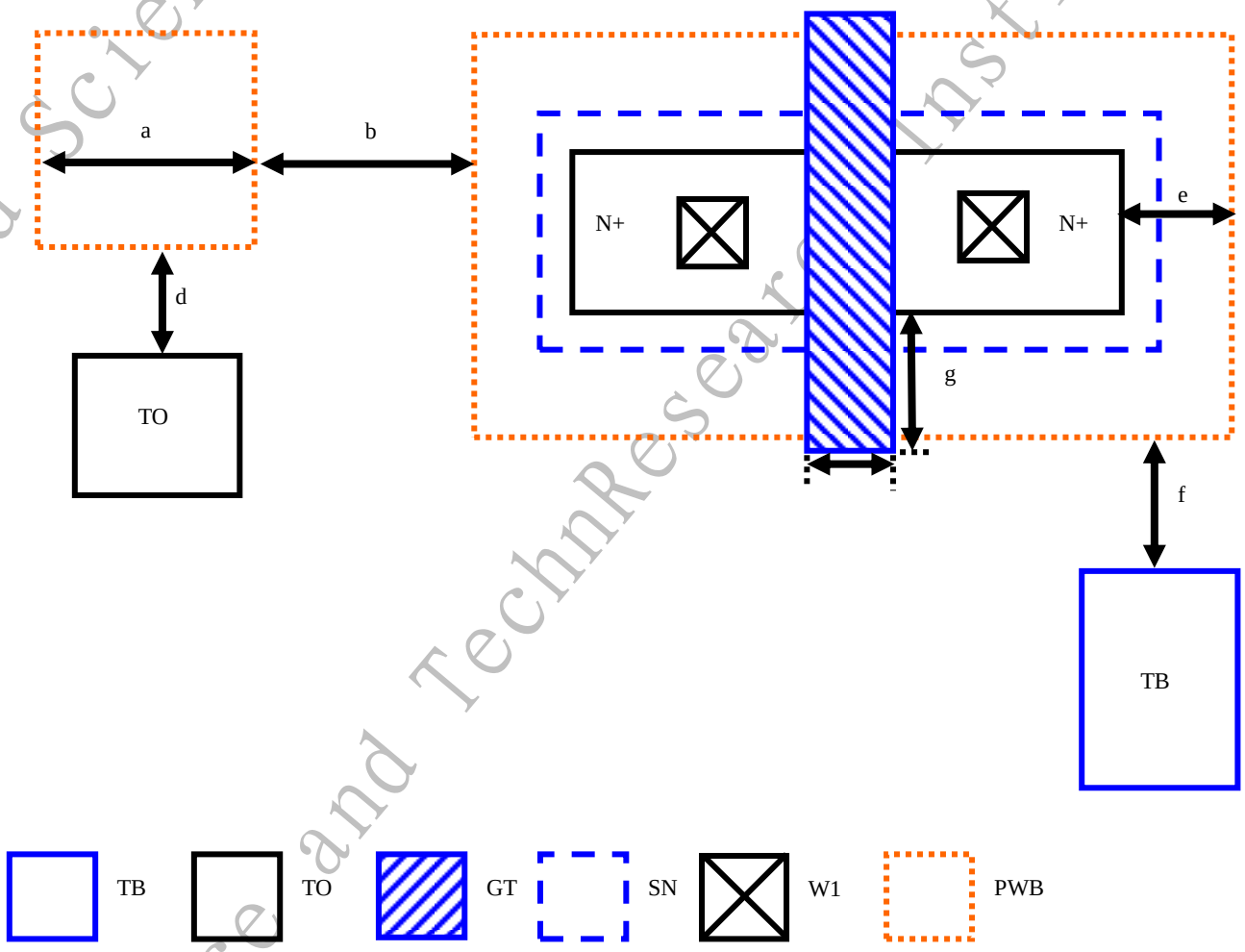
No.	Description	Rule(um)
a	Minimum width of DN	2.55
b	Minimum space of DN	4.25
c	Minimum space of DN to unrelated TB	2.974
d	Minimum overlap of TB and DN	1.7
e	Minimum extension of TB beyond DN	1.274
f	Minimum space of P+ TO to DN	1.274



5.15 PWB (P-Well Block)

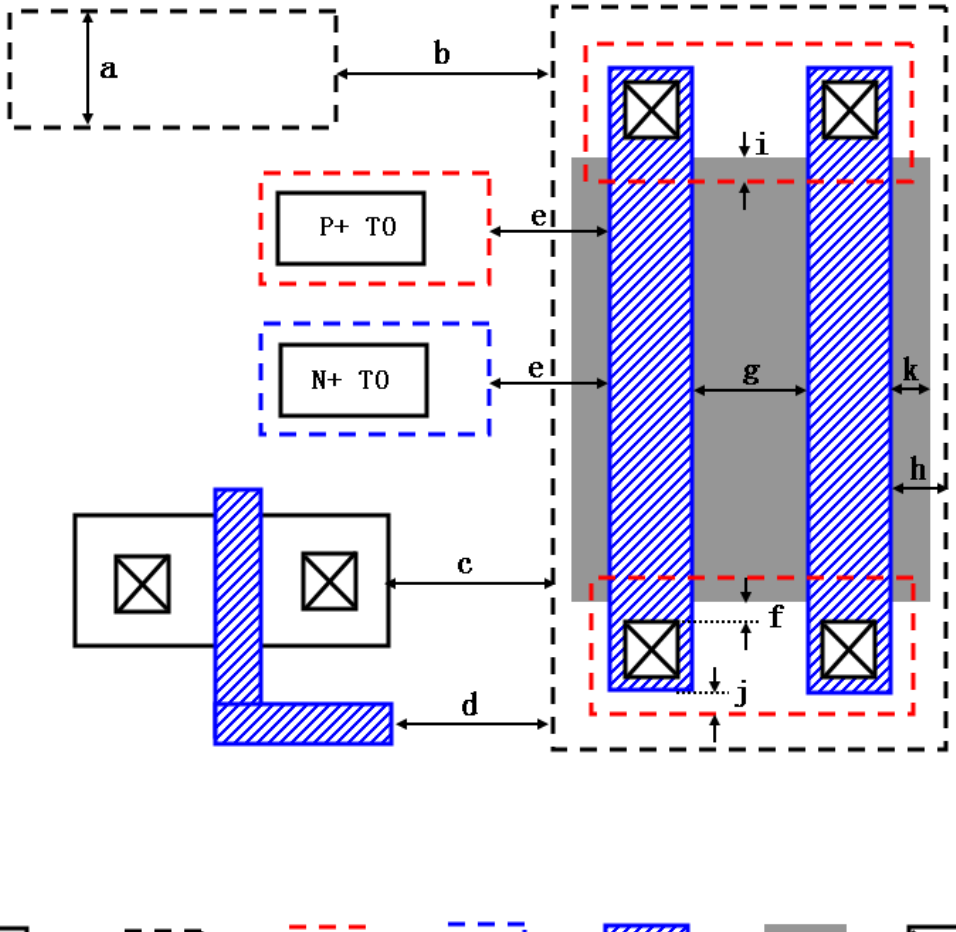
P-well block layer for Native NMOS region

No.	Description	Rule(um)
a	Minimum width of PWB	0.8
b	Minimum space of PWB	0.8
c	Minimum channel length for 5.0V native NMOS	2.5
d	Minimum space of PWB to TO	0.442
e1	Minimum and Maximum extension of PWB beyond TO for Native NMOS	0.26
e2	Minimum extension of PWB beyond TO	0.26
f	Minimum space of PWB to TB	1.41
g	Minimum clearance with GT over TO of native NMOS device(End cap)	0.296
h	Only one native device per PWBLK is allowed	
i	Only one active is allowed to put in PWBLK region	
j	A P+ active is not allowed to put in PWBLK region	
k	A bent poly on active is not allowed to be put in PWBLK region	
l	PWBLK overlap TB is not allowed	
m	PWBLK overlap DNW is not allowed	



5.16 HR (Poly High Resistor implant)

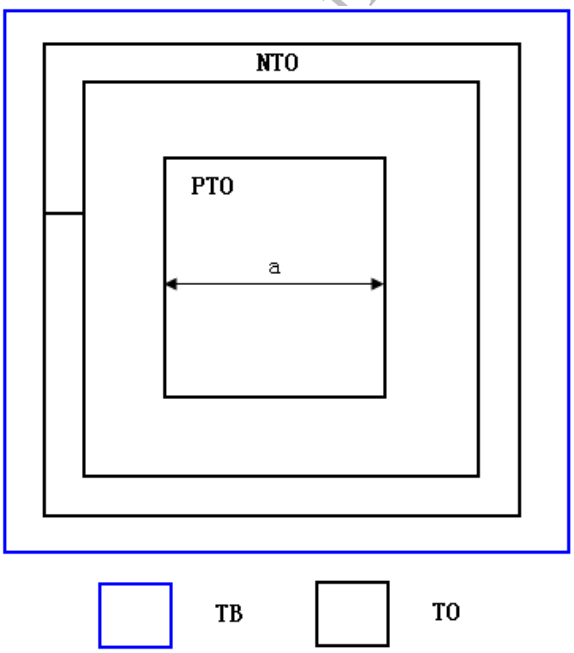
No.	Description	Rule(um)
a	Minimum width of HR	0.374
b	Minimum space of HR	0.374
c	Minimum space of HR to TO	0.254
d	Minimum space of HR to unrelated Gate	0.272
e	Minimum space of unrelated SP/SN to GT of poly resistor with HR	0.254
f	Minimum and Maximum clearance from SI to W1	0.15
g	Minimum space of two GT for HR resistor	0.34
h	Minimum extension of HR beyond GT of HR resistor	0.254
i	Minimum and Maximum overlap of SP and SI in HR region	0.186
j	Minimum extension of SP beyond poly GT	0.152
k	Minimum clearance of SI beyond GT of HR resistor in width direction	0.238
l	Minimum width of GT used as poly HR(Nsq≧5) Recommend: High Poly resistor minimum width is 2um for mismatch and accuracy concern	1
m	Minimum area of HR 0.38 um^2	
n	Overlap of SN and HR is not allowed	
o	Overlap of TO and HR is not allowed	



5.17 Diode

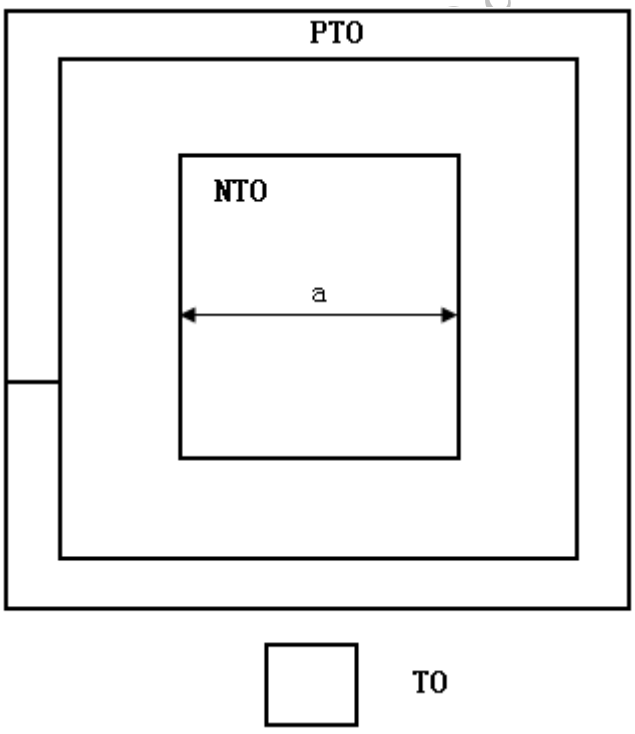
5.17.1 5V P+/NW Diode（Dppnw）

No.	Description	Rule(um)
a	P+/NW Diode dimension decided by PTO area (Junction BV=11.4V)	



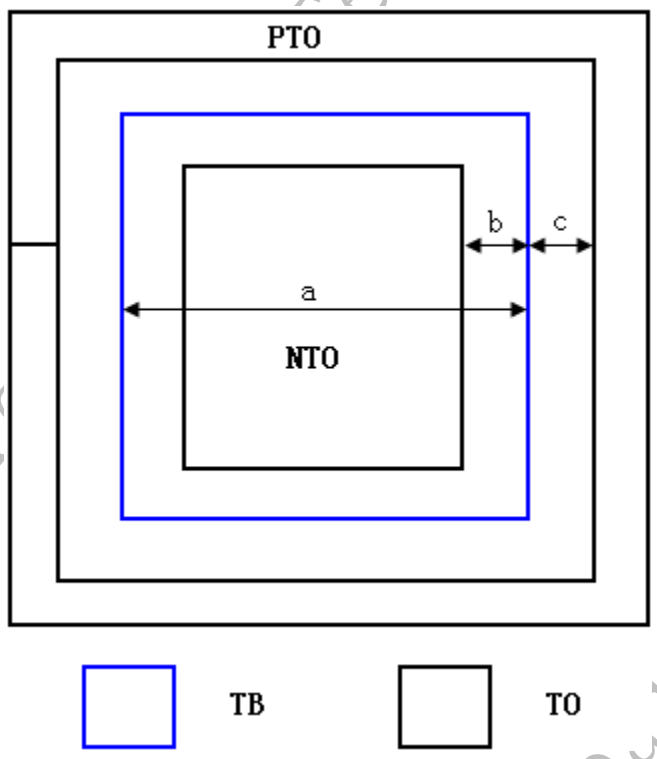
5.17.2 5V N+/PW Diode(Dnppw)

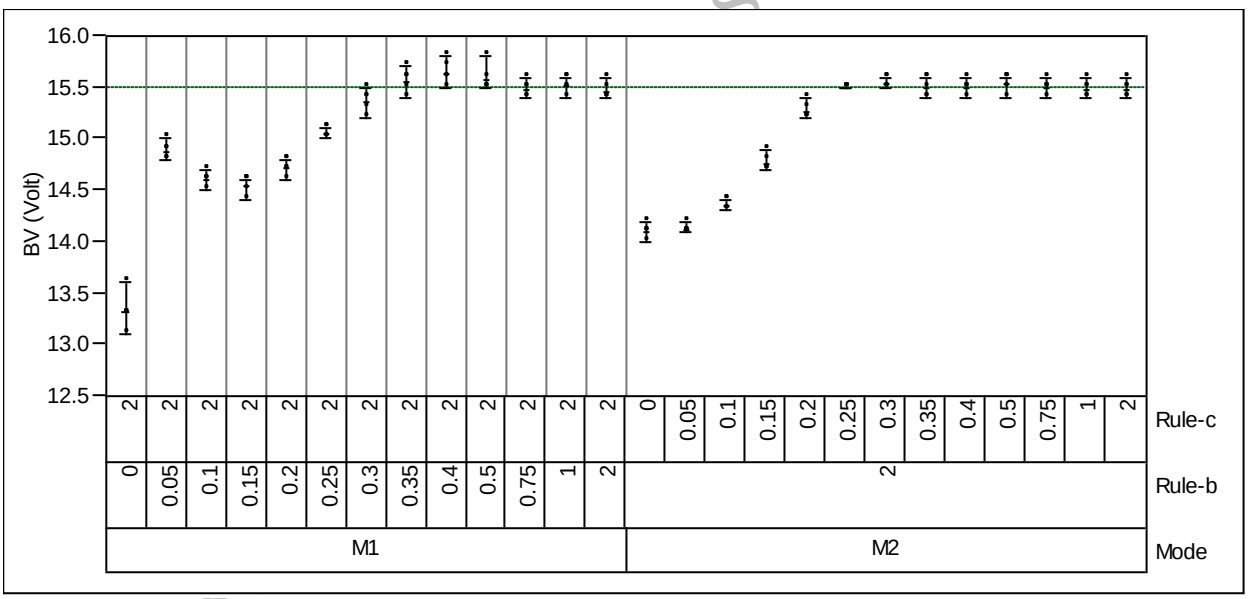
No.	Description	Rule(um)
a	N+/PW Diode dimension decided by NTO area, Junction BV=10.4V	



5.17.3 5V NW/PW Diode（Dnwpw）

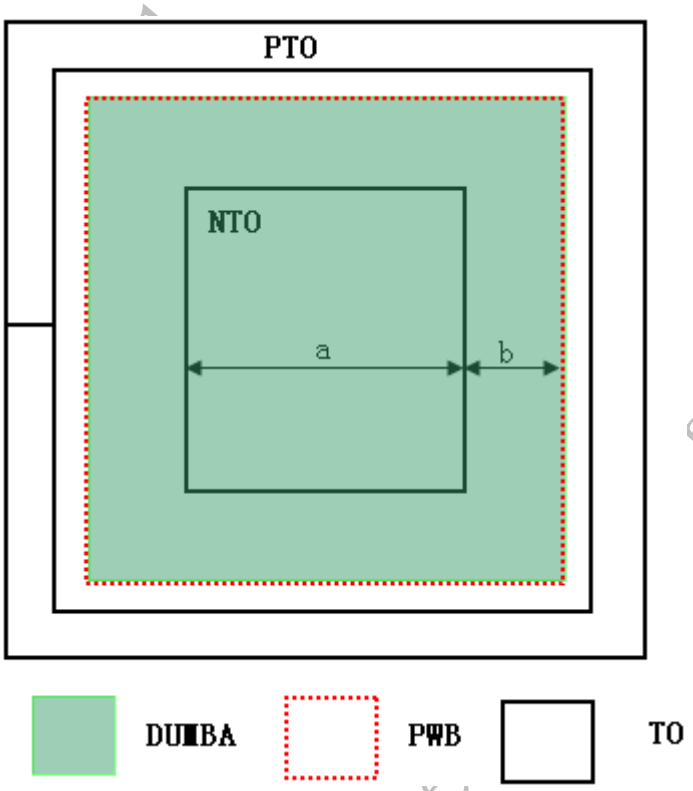
No.	Description	Rule(um)
a	NW/PW Diode dimension decided by TB area (Junction BV=15.5V)	
b	Minimum extension of TB beyond NTO	0.45
c	Minimum Space of TB and PTO（PW Pickup）	0.35
	NW and PW Junction breakdown Voltage variation with b and c rule	

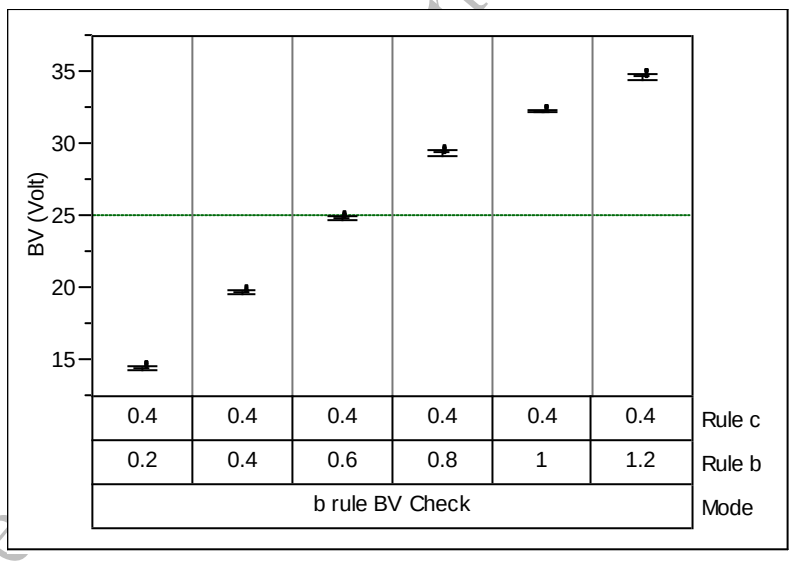




5.17.4 5V N+/Psub diode (Dnppsub)

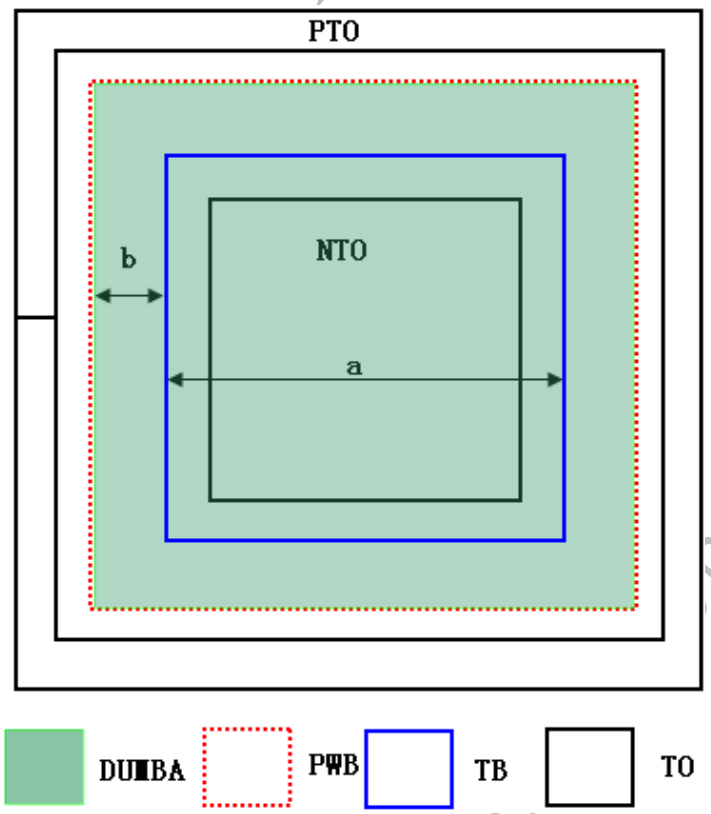
No.	Description	Rule(um)
a	N+/Psub Diode dimension decided by NTO area	
b	Minimum extension of PWB beyond NTO（BV=35V）	1.6
note	Please Refer to Single N+(area:30*30)/Psub diode BV versus b rule curve N+ and Psub Junction breakdown Voltage variation with b, consider process fluctuation, please add extra 0.5um to b rule to get design request breakdown voltage, for example, b=0.6+0.5=1.1um get 25V BV Need draw DUMBA(159) Layer to prevent adding dummy active on diode region, DUMBA is same as PWB	

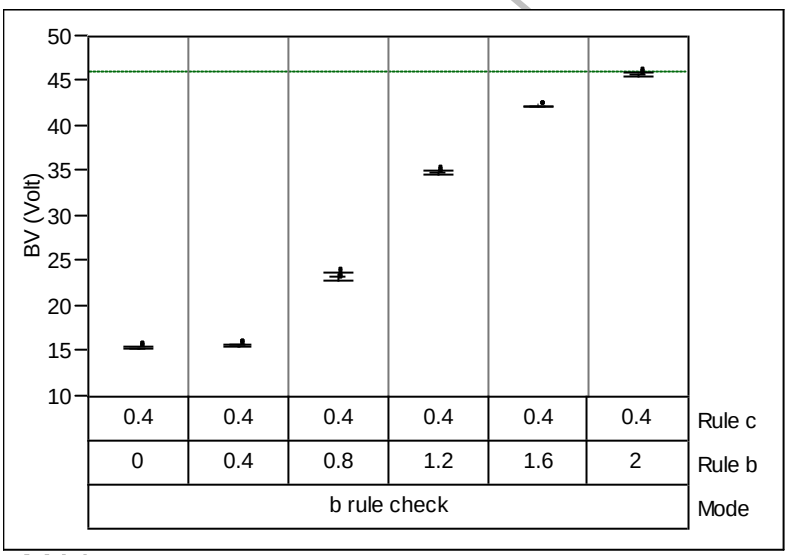




5.17.5 5V NW/Psub Diode (Dnwpsub)

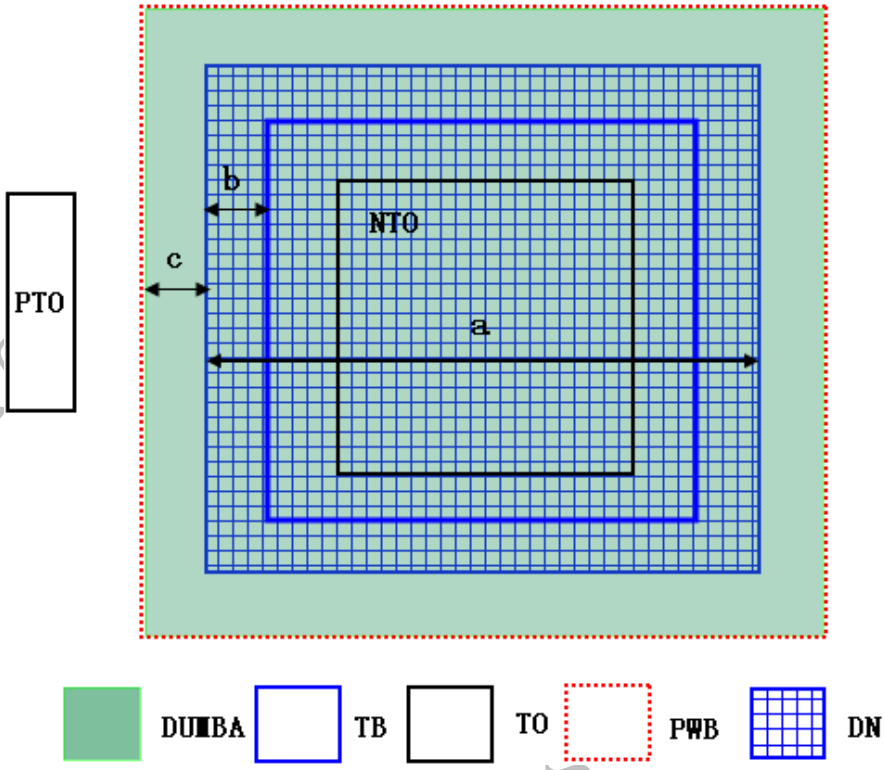
No.	Description	Rule(um)
a	NW/Psub Diode dimension decided by TB area	
b	Minimum extension of PWB beyond TB（BV=46V）	2.5
note	Please Refer to Single NW(area:50*50)/Psub diode BV versus b rule curve NW and Psub Junction breakdown Voltage variation with b, consider process fluctuation, please add extra 0.5um to b rule to get design request breakdown voltage, for example, b=2+0.5=2.5um get 46V BV. Need draw DUMBA(159) Layer to prevent adding dummy active on diode region, DUMBA is same as PWB	

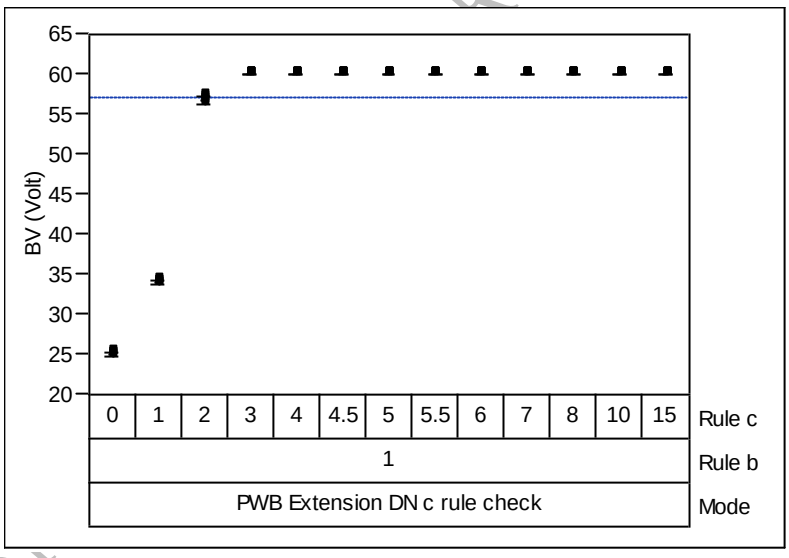




5.17.6 5V DN(NW)/Psub Diode（Ddnwpsub）

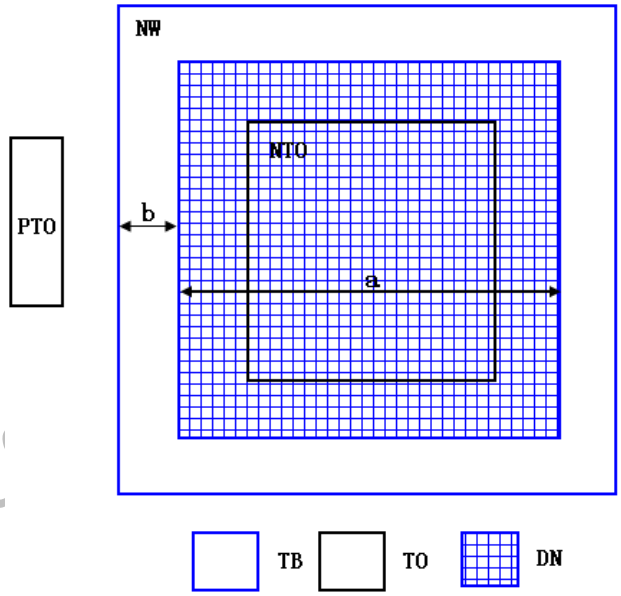
No.	Description	Rule(um)
a	DNW/Psub Diode dimension decided by DN area	
b	Minimum extension of DN beyond TB	1
c	Minimum extension of PWB beyond DN（BV=57V）	3
note	Please Refer to Single DN(area:14*14)/Psub diode BV versus c rule curve DN and Psub Junction breakdown Voltage variation with c, consider process fluctuation, please add extra 1um to b rule to get design request breakdown voltage, for example, c=2+1=3um get 57V BV Need draw DUMBA (159) Layer to prevent adding dummy active on diode region, DUMBA is same as PWB	





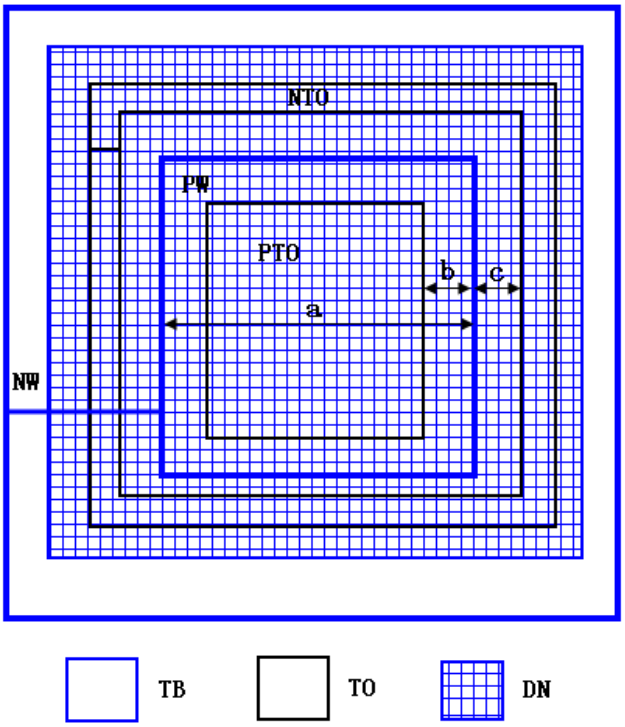
5.17.7 DN/PW(Psub) Diode（Ddnpwpsub）

No.	Description	Rule(um)
a	DN/PW(Psub) Diode dimension decided by DN area	
b	Minimum Space of NW and PTO(PW pickup)	0.35
	DN/PW(Psub) Junction breakdown Voltage 15.25V	



5.17.8 Pw/DN(nw) Diode (Dpwdn)

No.	Description	Rule(um)
a	PW/DW(nw) Diode dimension decided by PW area	
b	Minimum Space of PTO and TB	0.35
c	Minimum extension of TB beyond NTO	0.45
	DN/PW(Psub) Junction breakdown Voltage 15.25V	



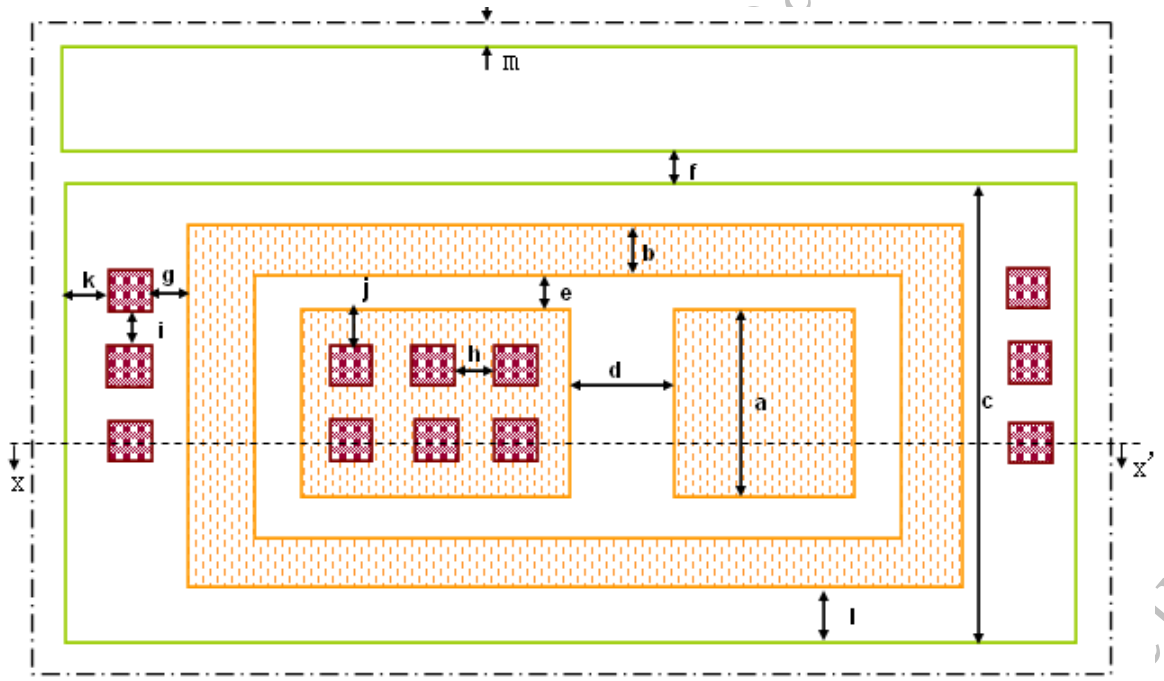
5.18 CT (MIM Capacitor Top)

（1）For Single MIM Process, CT Mask use for top-1 Metal CAP Top Plate

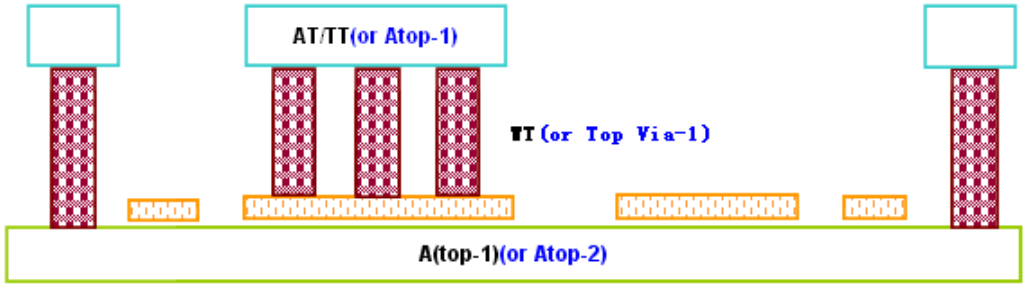
（2）For Dual MIM Process with only CT Mask, CT user for both Top-1 and Top-2 Metal CAP Top plate

（3）For Dual MIM Process with CT and MT Mask，CT Mask only use for top-2 Metal CAP Top plate，MT Mask for Top-1 metal CAP Top Plate

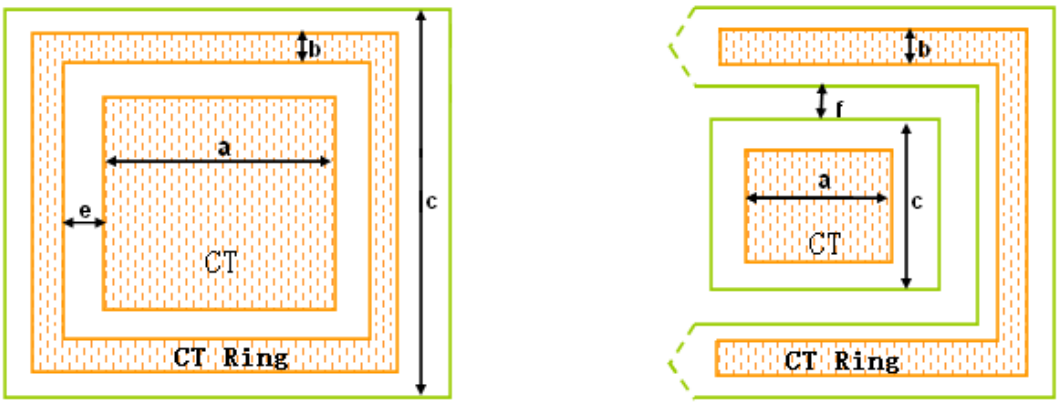
No.	Description	Rule(um)
a	Minimum width of CT used for capacitor top plate	3.4
	Maximum width of CT used for capacitor top plate	30
b	CT ring no recommendation this process，if with CT Ring, Minimum width of CT ring	0.85
c	Maximum width of A(top-1 or top-2) used for capacitor bottom plate	35
d	Minimum space of capacitor CT	1.02
e	Minimum space from capacitor CT and CT ring	0.8
f	Minimum space of A(top-1 or top-2) used for capacitor bottom plates	0.68
g	Minimum space from CT to WT(or Top Via-1)	0.4
h	Minimum space of WT(or Top Via-1) which are covered by CT	1.7
i	Minimum space of WT(or Top Via-1) which are covered by A(top-1)(or A(top-2))	1.7
j	Minimum extension of CT beyond WT(or Top Via-1)	0.24
k	Minimum extension of A(top-1)(or A(top-2)) beyond WT(or Top Via-1)	0.12
l	Minimum extension of A(top-1)(or A(top-2)) beyond CT	0.34
m	Minimum extension of MCTM beyond A(top-1 or top-2)	2
n	Minimum density of WT (or Top Via-1)which is covered by CT: 1%	
o	Minimum pattern density of CT: 3%	
p	Minimum area of CT: 1 um^2	
q	Both the active and passive device under MIM region are not allowed	
r	CT without A(top-1) or A(top-2）cover is not allowed	
s	MIM capacitor is formed by CT layer and A(top-1 or top-2) (bottom metal is optional, Layer from 2 to5). CT is used as the top plate of MIM capacitor, and A(top-1 or top-2) as the bottom plate. CT ring no recommendation for this process.	



>>xx' cross section<<



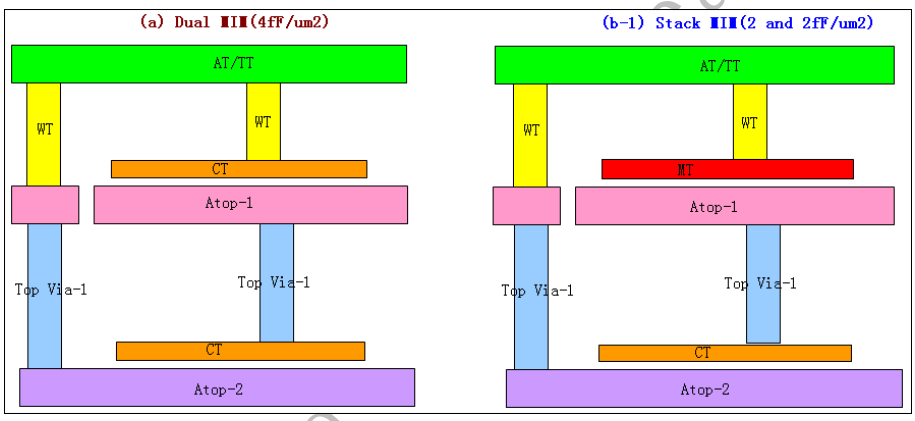
>>CT ring pattern<<

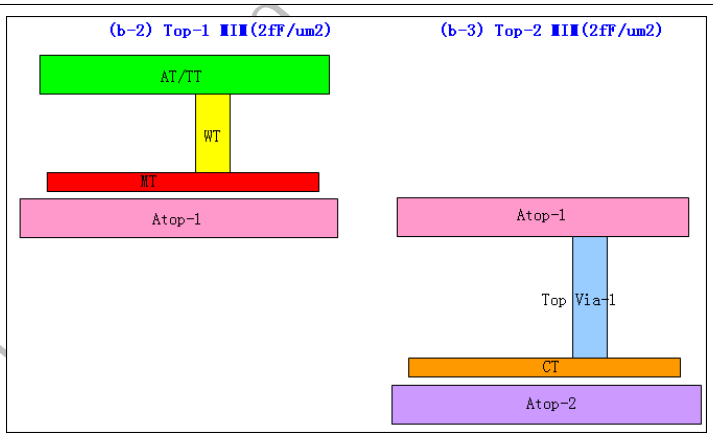


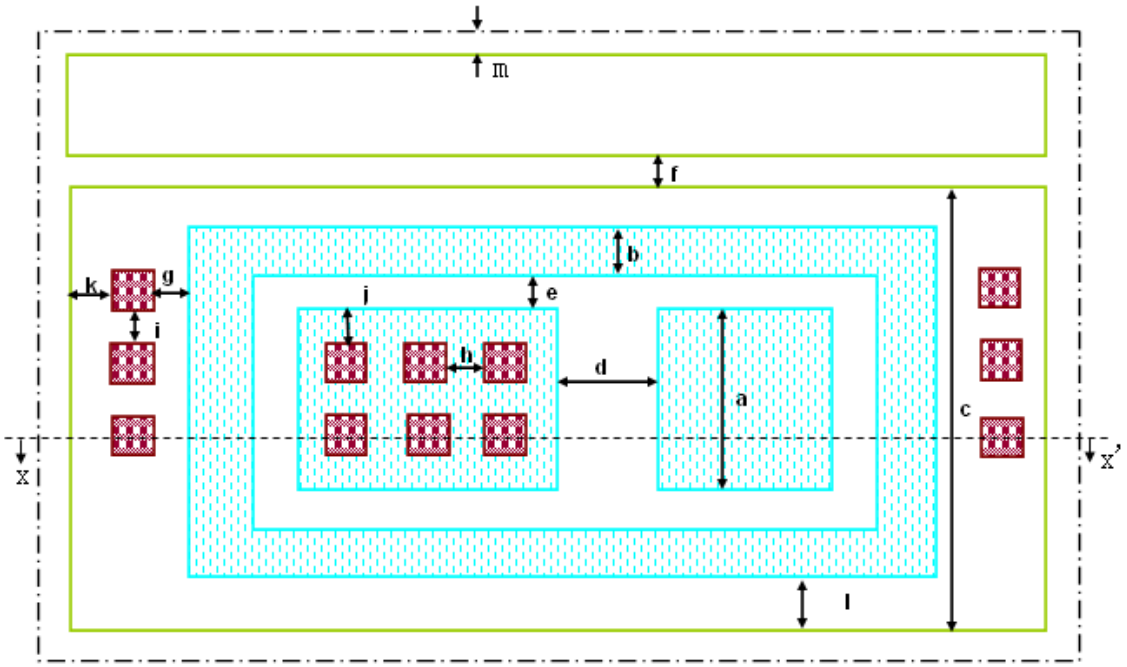
5.19 MT (Dual MIM Capacitor Top 78:2)

For Dual MIM Process, MT only use for Top-1 metal CAP top Plate and CT for Top-2 Metal CAP Top Plate

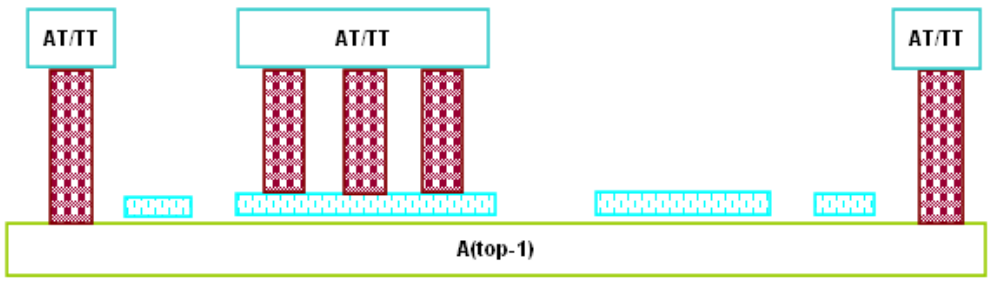
No.	Description	Rule(um)
a	Minimum width of MT（layer：**78:2**）used for capacitor top plate	3.4
	Maximum width of MT used for capacitor top plate	30
b	MT ring no recommendation this process，if with MT Ring, Minimum width of MT ring	0.85
c	Maximum width of A(top-1) used for capacitor bottom plate	35
d	Minimum space of capacitor MT	1.02
e	Minimum space from capacitor MT and MT ring	0.8
f	Minimum space of A(top-1) used for capacitor bottom plates	0.68
g	Minimum space from MT to WT	0.4
h	Minimum space of WT which are covered by MT	1.7
i	Minimum space of WT which are covered by A(top-1)	1.7
j	Minimum extension of MT beyond WT	0.24
k	Minimum extension of A(top-1) beyond WT	0.12
l	Minimum extension of A(top-1) beyond MT	0.34
m	Minimum extension of MCTM beyond A(top-1)	2
n	Minimum density of WT which is covered by MT: 1%	
o	Minimum pattern density of MT: 3%	
p	Minimum area of MT: 1 um^2	
q	Both the active and passive device under MIM region are not allowed	
r	MT without A(top-1) cover is not allowed	
s	For Dual MIM Process, exist a(only CT Mask) and b(with CT and MT Mask) 2 main Layout(see the below profile picture) ,MT and CT ring no recommendation for this process. Dual MIM top capacitor is formed by MT or CT layer and A(top-1) (bottom metal is optional, layer from 3 to 5). Dual MIM bottom capacitor is formed by CT and A(top-2). (bottom metal is optional, layer from 2 to 4)	



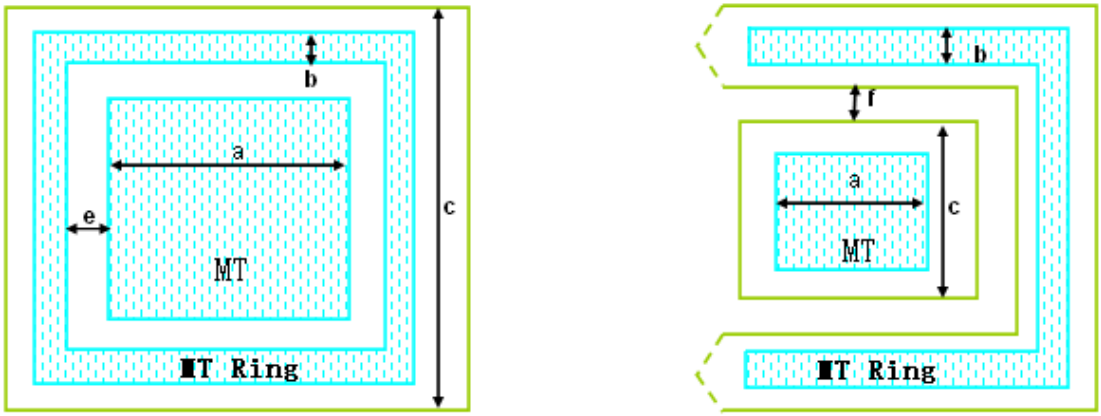




>>xx' cross section<<

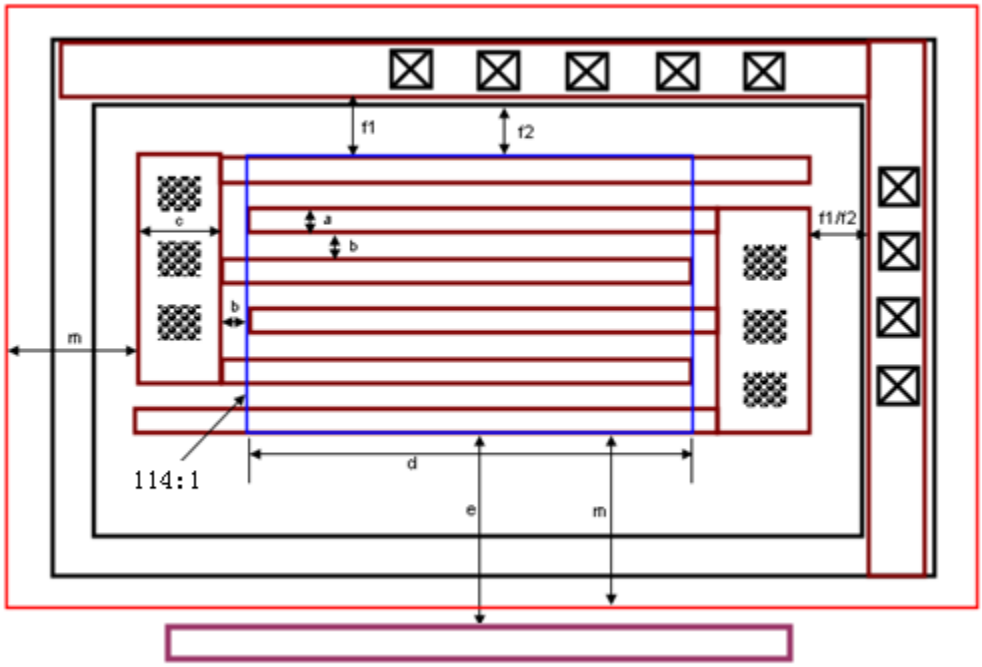


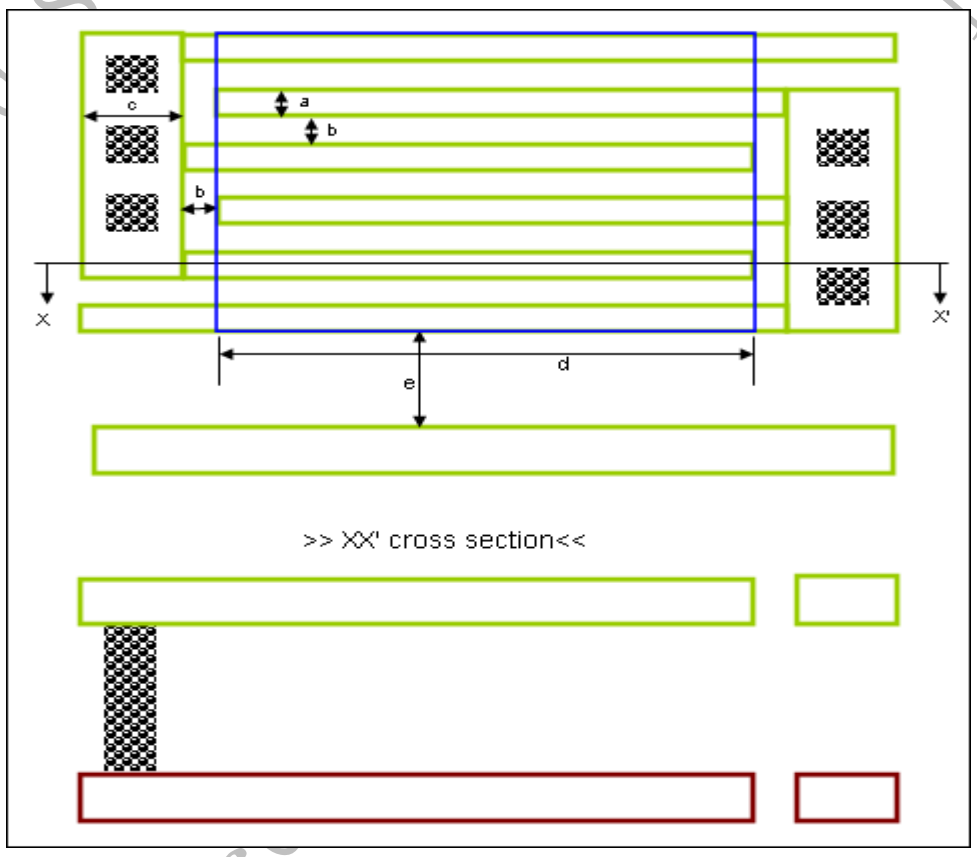
>>MT ring pattern<<



5.20 MOM Capacitor

No.	Description	Rule(um)
a	Min and Max width of every A1 finger	0.238
	Min and Max width of every An finger	0.238
b	Min and Max space of every A1 finger	0.238
	Min and Max space of every An finger	0.238
c	Min width for metal strip on two terminals	0.5
d	Min length of A1 finger	20
	Min length of An finger	20
e	Min space from MOM to unrelated metal	4.2
f1	If use guard ring, min clearance from MOM A1/An to guard ring metal	0.42
f2	If use guard ring, min clearance from MOM to guard ring TO	0.42
g	Min MOM finger number for good precision	105
h	MOM device need to be marked by layer 114:6, and the mark layer size is same with MOM capacitance area which is a rectangle enclosed by most edge of metal fingers and end of metal fingers.	
i	Min MOM capacitance area(defined by layer 114:6) is 1000um2 for good precision	
j	Max area of a single MOM cell (defined by layer 114:6) is 10000um2. If size greater than 10000um2 then either of two sides should not be greater than	90
k	Both the active and passive device under MOM region are not allowed	
l	MOM capacitor is formed by A1 to A(top-1)	
m	All dummy pattern is not allowed in MOM region, need cover NODMF(160:1)，and min NODMY enclosure of MOM metal	1
n	MOM model support single Layer Metal capacitance, for precision consideration, recommend use as MOM CAP's Metal Layer number n>=3	



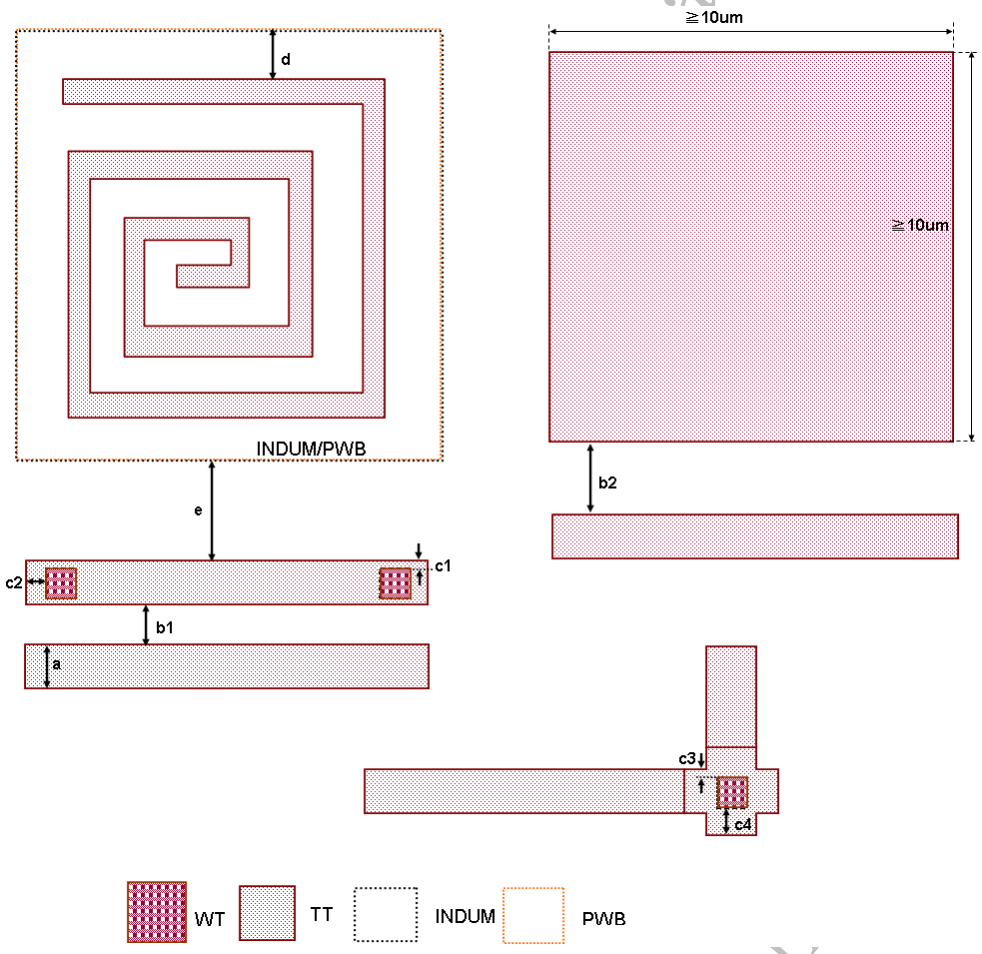


5.21 TT (Thick Top Metal)

TT (Thick Top Metal-25K)

No.	Description	Rule(um)
a	Minimum width of TT	1.2
b	b1 Minimum space of TT	1.2
	b2 Minimum space of TT If the width and length of one metal both larger than 10um (except for inductor)	2.55
c	Minimum extension of TT beyond WT	
c1	In Line	0.254
c2	Line-end	0.382
c3	inner corner	0.254
c4	outer corner	0.382
d	Minimum extension of INDUM beyond TT	50
e	Minimum space of TT of inductor to other TT	50
f	Minimum area of TT island 2.25 um^2	
g	Minimum pattern density of TT 30%	
h	Dummy metal will be added according to Dummy Rule “8.29 AnDUM (Metal Dummy)”. If TT pattern density < 30%	
i	No Via and metal layers inside INDUM region are allowed except underpass via and metal interconnect of inductor	
j	Both active and passive devices inside INNDUM region are not allowed	
k	TT is an optional layer for Inductor application in RF product. You need to chose AT or TT as top metal	
l	For two adjacent outer corner sides, at least one side should be treated as metal line end	

Note: PWB layer is drawn under the inductor coil to generate native substrate after logic operation, it can minimize inductor coil eddy current, PWB pattern is same as INDUM

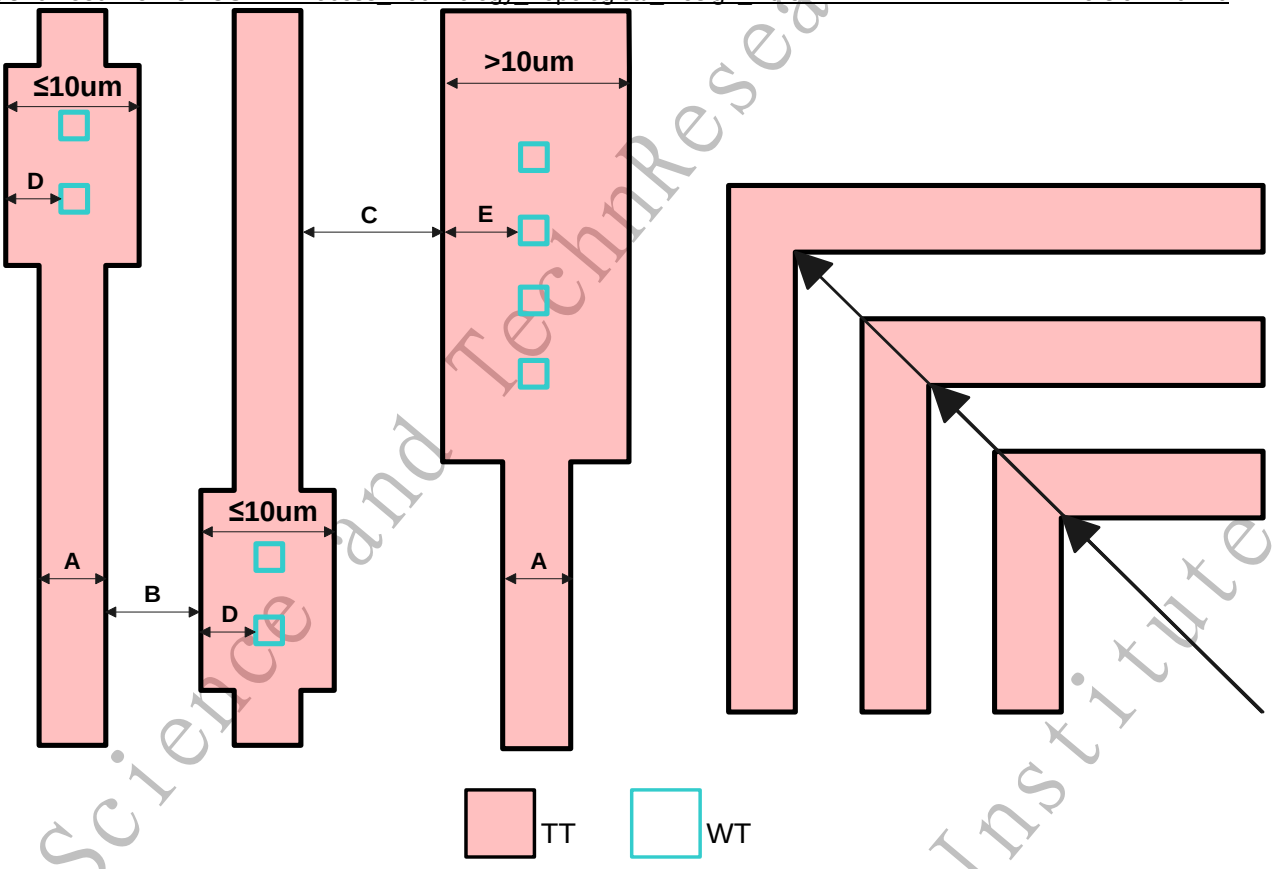


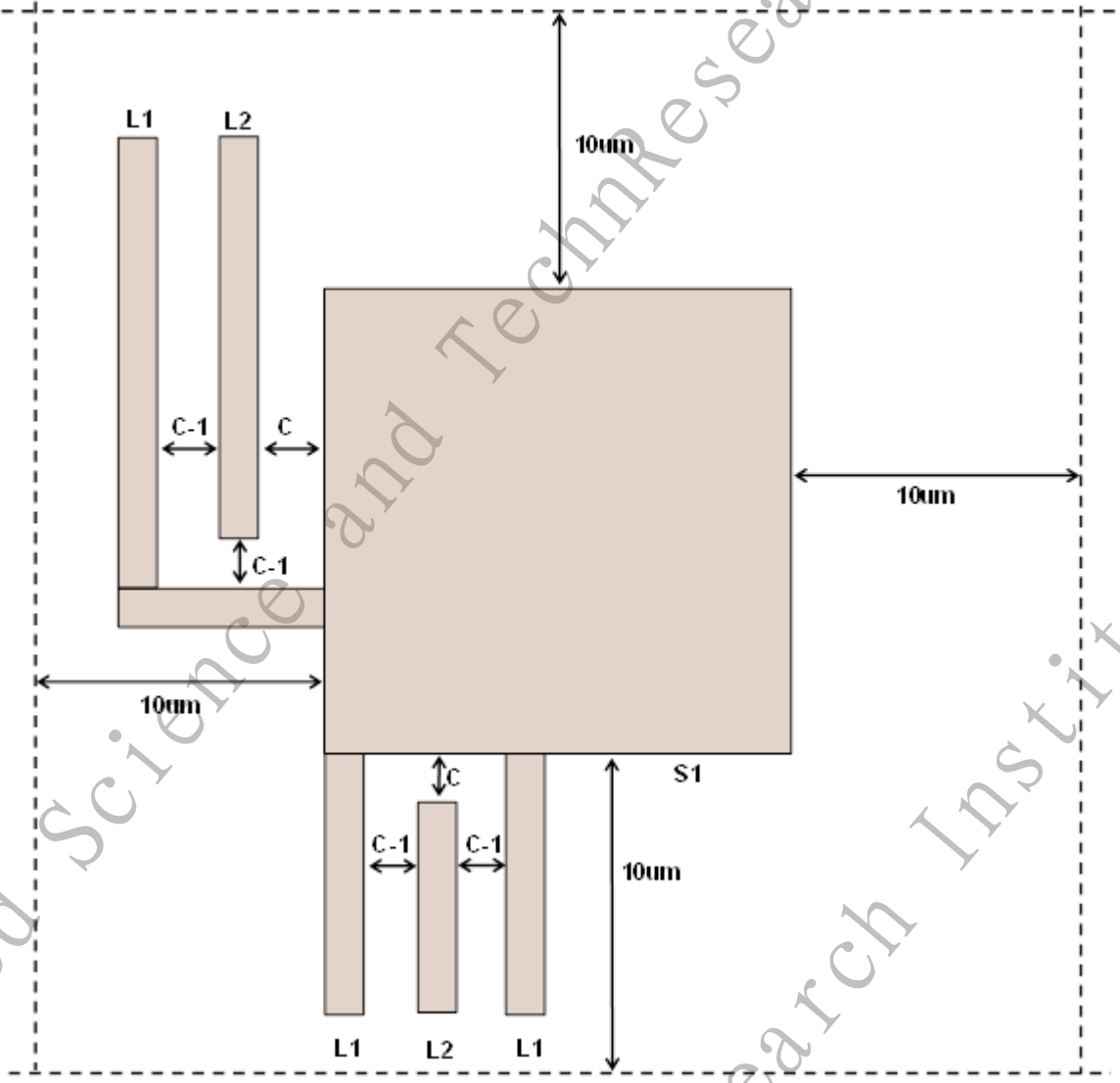
TT (Thick Top Metal-35K)

No.	Description	Rule	
A	Min. **TT** width.	≥	2 um
B	Min. **TT** to **TT** space	≥	2 um
C	Min. **TT** to **TT** space when the width of **TT** is large than 10um.	≥	2.55 um
C-1	For PR shrink issue, when the width of metal S1 is equal or larger than 10um, in the range of 10um beyond each side of S1, if the metal L1 connected with S1, Min. space between L1 to unrelated L2 and S2/L1	≥	2.55 um
D	Min. extension of **TT** to **WT**.	≥	0.5 um
E	Min. extension of **TT** to **WT** when the width of **TT** is large than 10um.	≥	2.5 um
F	90 degree metal line corner is not allowed.		
G	Minimum area of TT island 6 um^2		

Note:

Metal density, if more than 70%, please inform CSMC; if less than 40%, please follow metal dummy rule to add dummy metal





5.22 Seal ring (Scribe Line Guard Ring)

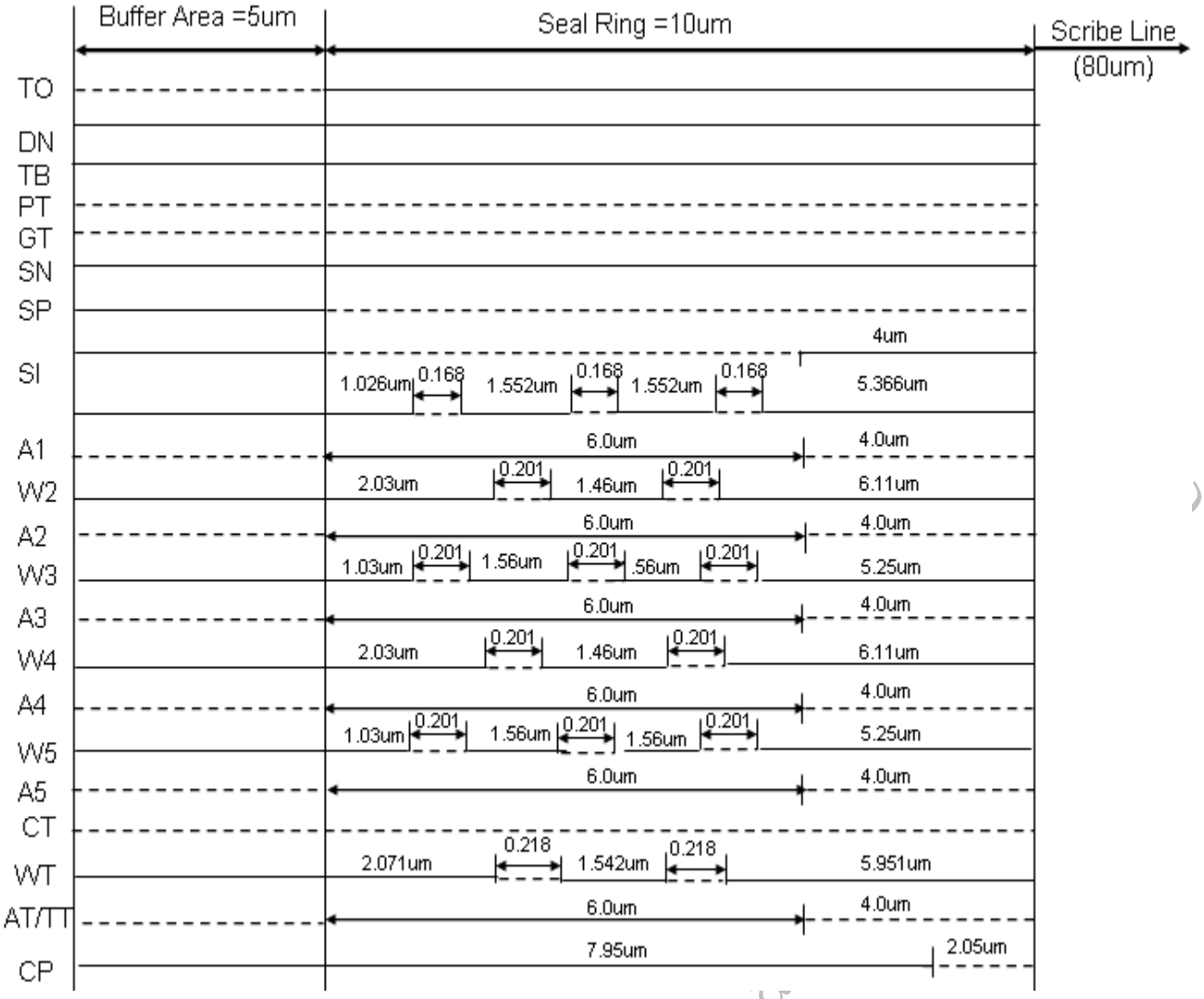
A. continuous scribe line and seal ring is required on all sides of a chip that is intended for dicing and packaging. It is recommended that test patterns and alignment key into scribe line

No.	Description	Rule(um)
a	Scribe lines Minimum vertical and horizontal scribe line width (not including the seal ring)	80
b	Minimum buffer width between seal ring to Au bonding pad (circuit) edge	5
	Minimum buffer width between seal ring to Al bonding pad (circuit) edge	20
c	Seal ring site W1/Wx/WT (trench) CD need do size down handle	
c1	Minimum and Maximum W1 CD (trench)	0.168
c2	Minimum and Maximum inter Via CD (trench)	0.201
c3	Minimum and Maximum top Via CD (trench)	0.218

B. Six metal seal ring structure (Schematic diagram of CSMC 1P6M Die seal ring structure)

Digitized area is clear on mask

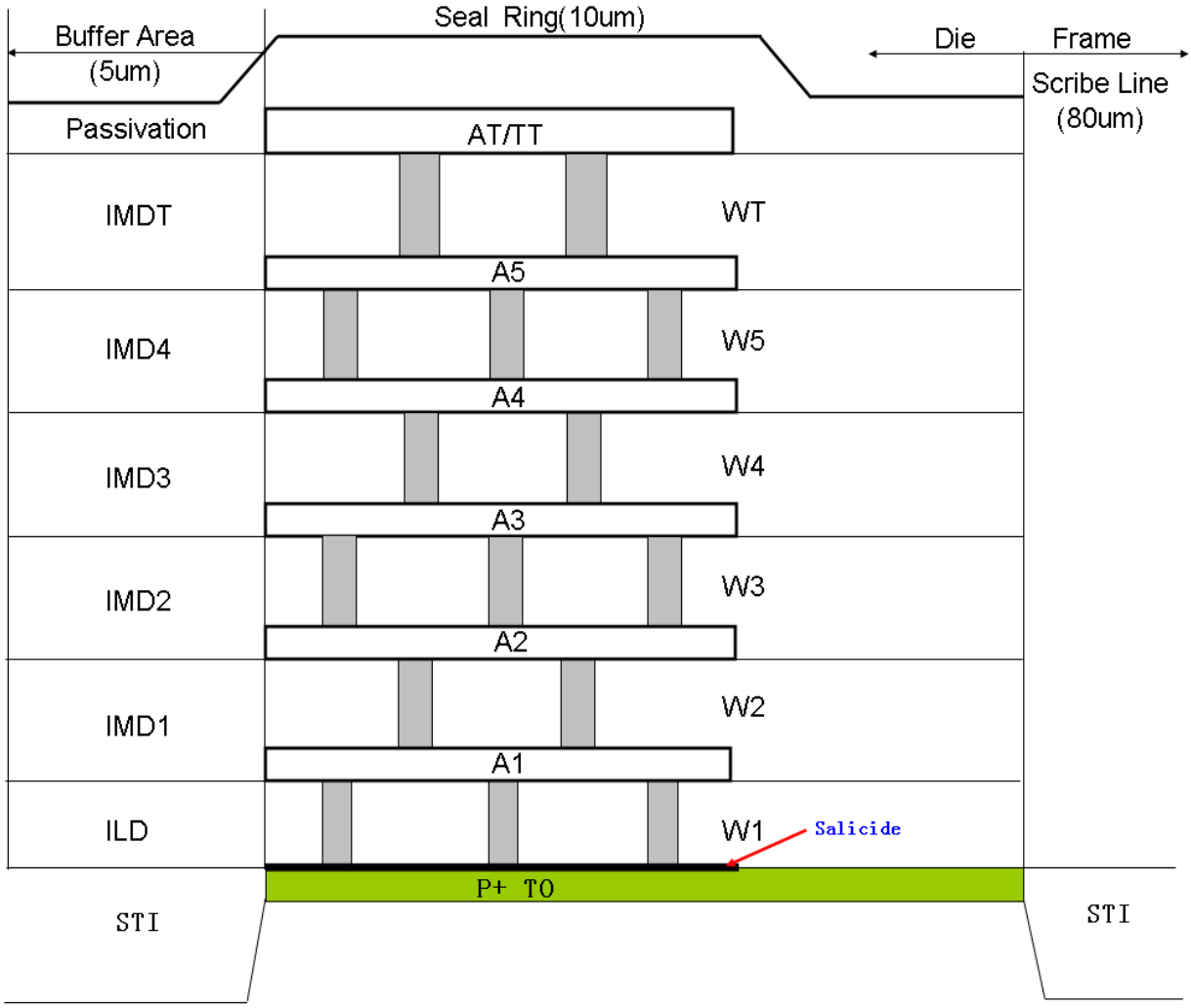
Digitized area is dark on mask



Note:

For 1P5M process, please skip M5, W5 layers
For 1P4M process, please skip M5, W5, M4, W4 layers
For 1P3M process, please skip M5, W5, M4, W4, M3, W3 layers

C. The schematic cross section for 1P6M process is as below:



5.23 Placement and Electrical Connection of Seal Ring

5.23.1 Seal ring space to any other circuits:

The minimum space from seal ring metal to any other unrelated Active, Poly, Metal and N-well is 5um.

5.23.2 Seal ring and Vss bus:

Seal ring and metal Vss bus must be connected directly to Vss pads. The seal ring metal maybe butted with the Vss bus. Then the width of the metal Vss bus before merging with the seal ring has to meet the current density requirement and rest if the related Active, Poly , Metal and N-well should be at least 5um away from the original seal ring.

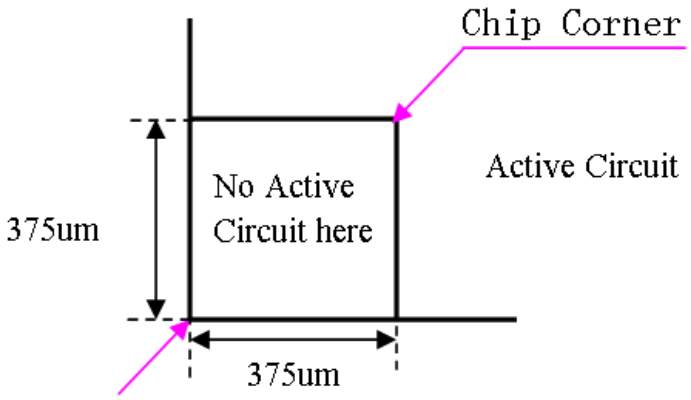
5.24 Power Supply Routing

Rules in this apply to very wide power supply busses and ground busses. If a design involves a shrink, these rules apply to the shrunk dimensions For stress relief rules, there are reliability problems associated with very wide metal busses in large die, these problems manifest themselves in cracks propagating from edges and corners of a die. These rules are intended to prevent surface stress points from which these cracks can emanate

5.24.1 Slots of Metal lines:

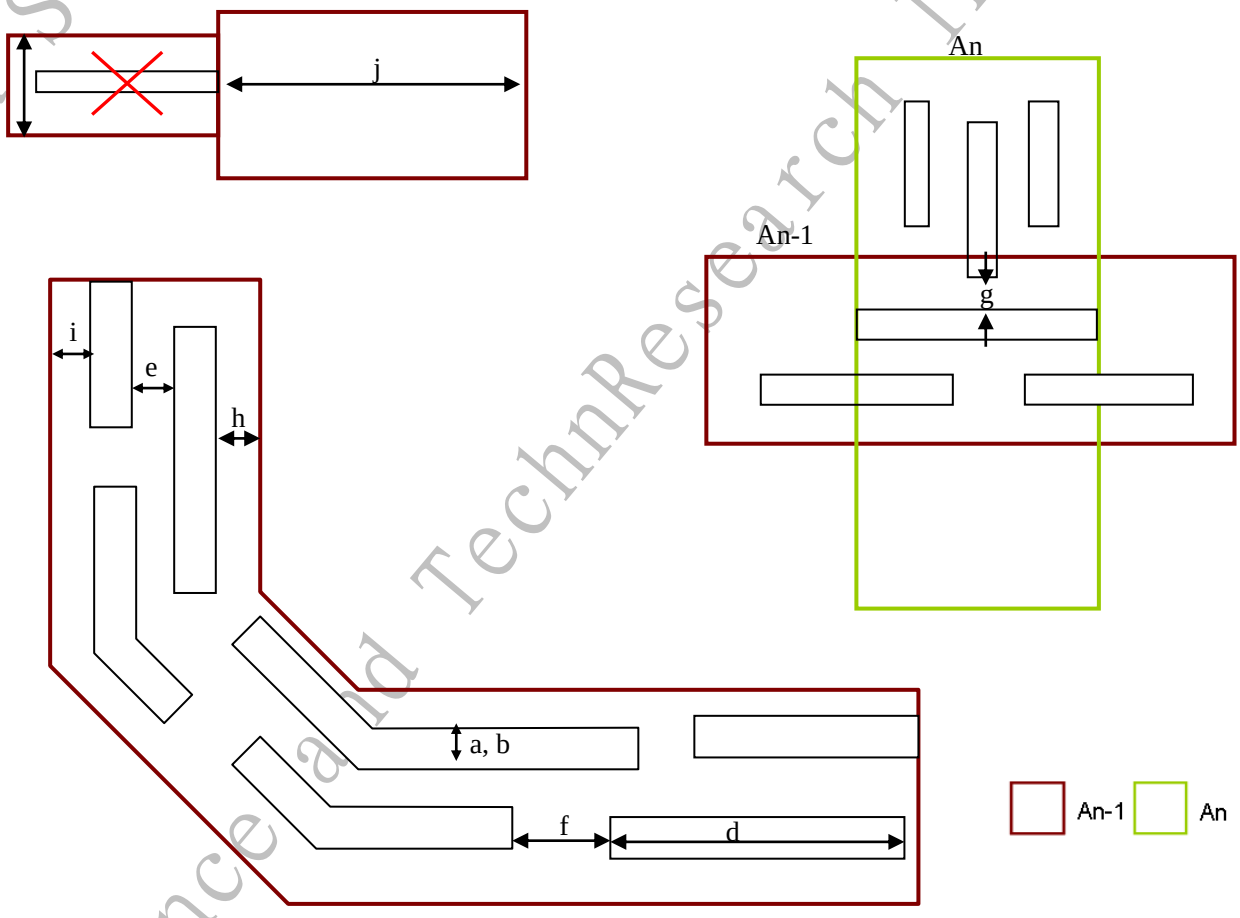
Metal slots shall be used on any metal line that is wider than 30um. Although it is most important at die corners, it should be done at all places on the die where metal is more than 30um wide and more than 500um long. And the slots shall be spaced parallel with the direction of current flow

5.24.2 No active circuit is allowed within 375um of a die corner. Any metal busses are allowedwithin 375um from die corner, but shall use 45 diagonal line.



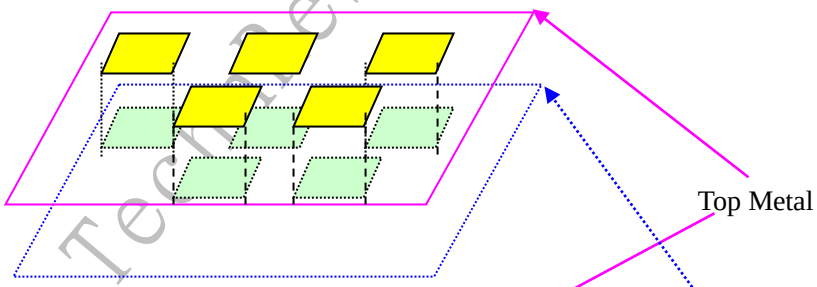
5.25 Metal Slotting Rules

No.	Description	Rule(um)
a	Minimum width of an open slot	2
b	Maximum width of an open slot	5
c	Minimum width of a metal line which is connected to wide metal line. No slot is allowed to be placed opposite this metal.	10.0
d	Minimum length of a open slot	20
e	Minimum space of any two parallel open slots	10
f	Minimum space of any two slots in a coaxial line. To avoid the EM problems resulting from current tunneling due to slot, the length of the slot must be parallel to current flow direction	10.0
g	Minimum space of two slots in neighbor layers (Example: A1 slot and A2 slot, A2 slot and A3 slot, A3 slot and A4 slot)	2.0
h	Minimum extension of two any open slot beyond the inner metal edge	10
i	Minimum extension from two any open slot beyond the outer metal edge The starting position of the parallel slots should be staggered	10.0
j	Maximum Metal width without slotting	35
k	Metal run at chip corner for 45 degree bend must start 350um before	
L	All slots are positioned parallel with the direction of current flow on the Metal line	
M	Due to reliability issue caused by thermal stress .All sizes are on silicon dimension. All slots are positioned parallel with the direction of current flow on the metal line. The above rules are applied to all metal	

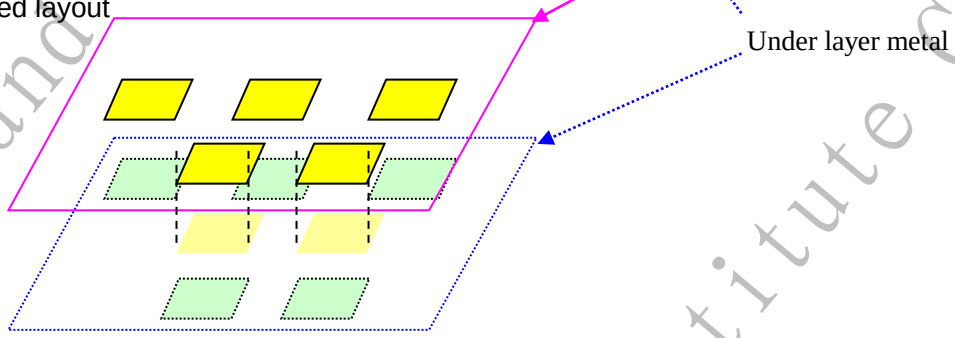


5.25.1 Stacking Slot Layout

5.25.1.1 Not recommended layout

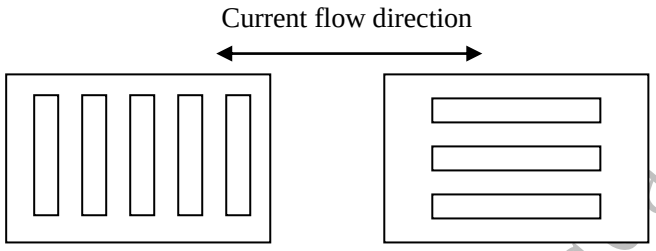


5.25.1.2 Recommended layout

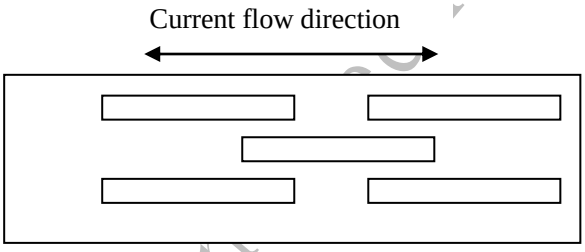


5.25.2 Schematic diagram for staggered start

5.25.2.1 Forbidden cases

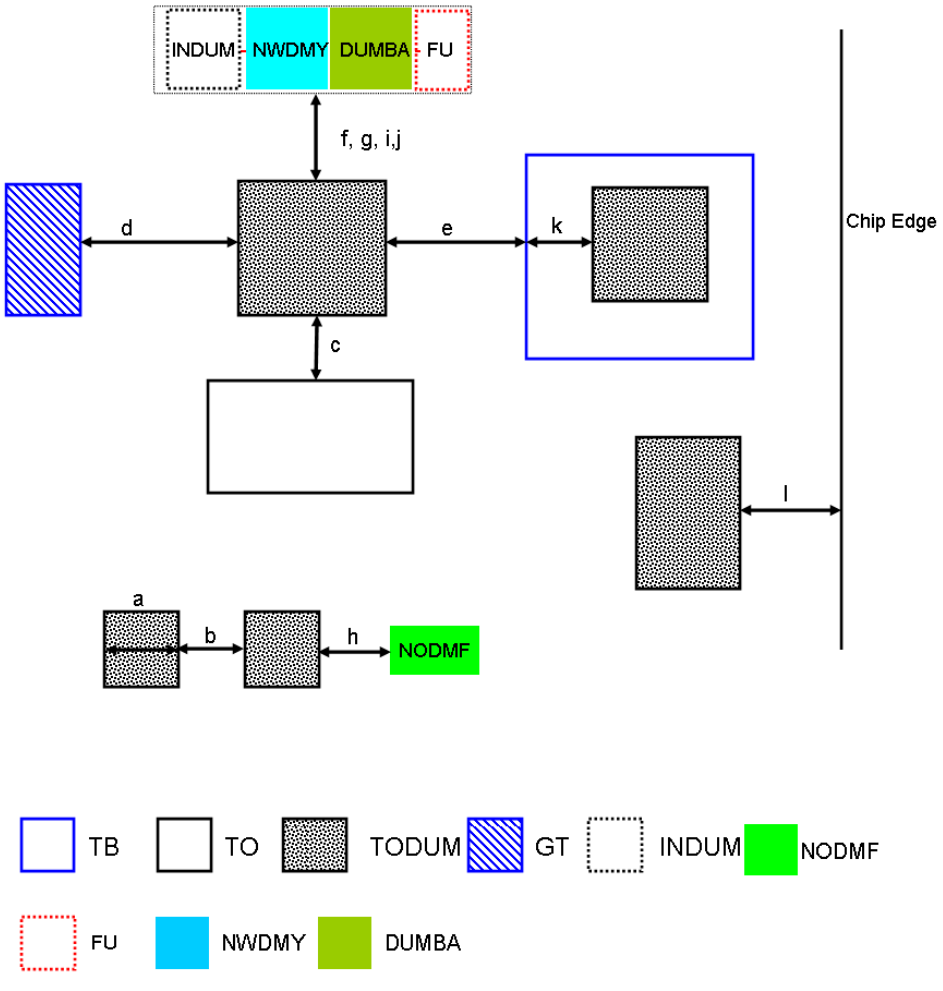


5.25.2.2 Recommended case



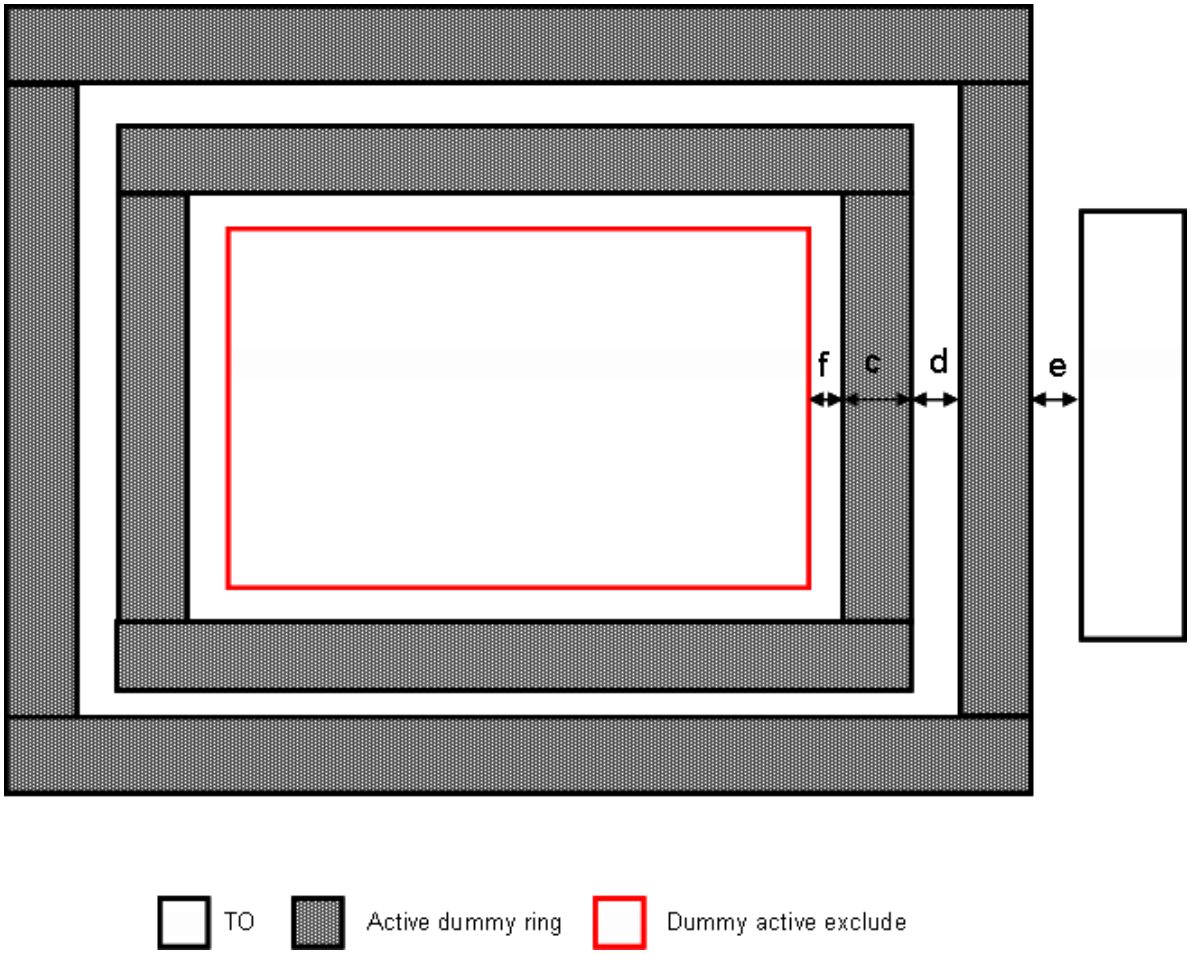
5.26 TODUM (TO Dummy)

No.	Description	Rule (um)
a	Minimum width	2.0
b	Minimum space	1.2
c	Minimum space from TODUM to TO (overlap is not allowed)	1.2
d	Minimum space from TODUM to GT (overlap is not allowed)	1.2
e	Minimum space from TODUM to TB (overlap is not allowed)	0.6
f	Minimum space from TODUM to FU (overlap is not allowed)	1.2
g	Minimum space from TODUM to NWDMY (overlap is not allowed)	1.2
h	Minimum space from TODUM toNODMF (overlap is not allowed)	0
i	Minimum space from TODUM to INDUM (overlap is not allowed)	1.2
j	Minimum space from TODUM to DUMBA (overlap is not allowed)	1.2
k	Minimum extension of TB beyond TODUM	0.6
l	Minimum extension of chip edge beyond TODUM	2.5
m	Minimum local density of (TO or TODUM):20%	
n	Maximum local density of (TO or TODUM):80%	
o	Minimum density of (TO or TODUM) across full chip:25%	
p	Maximum density of (TO or TODUM) across full chip:75%	
q	TODUM only shape allowed are square or rectangular	
r	Local density is checked over any 200umx200um area(stepping in 100um increment)	



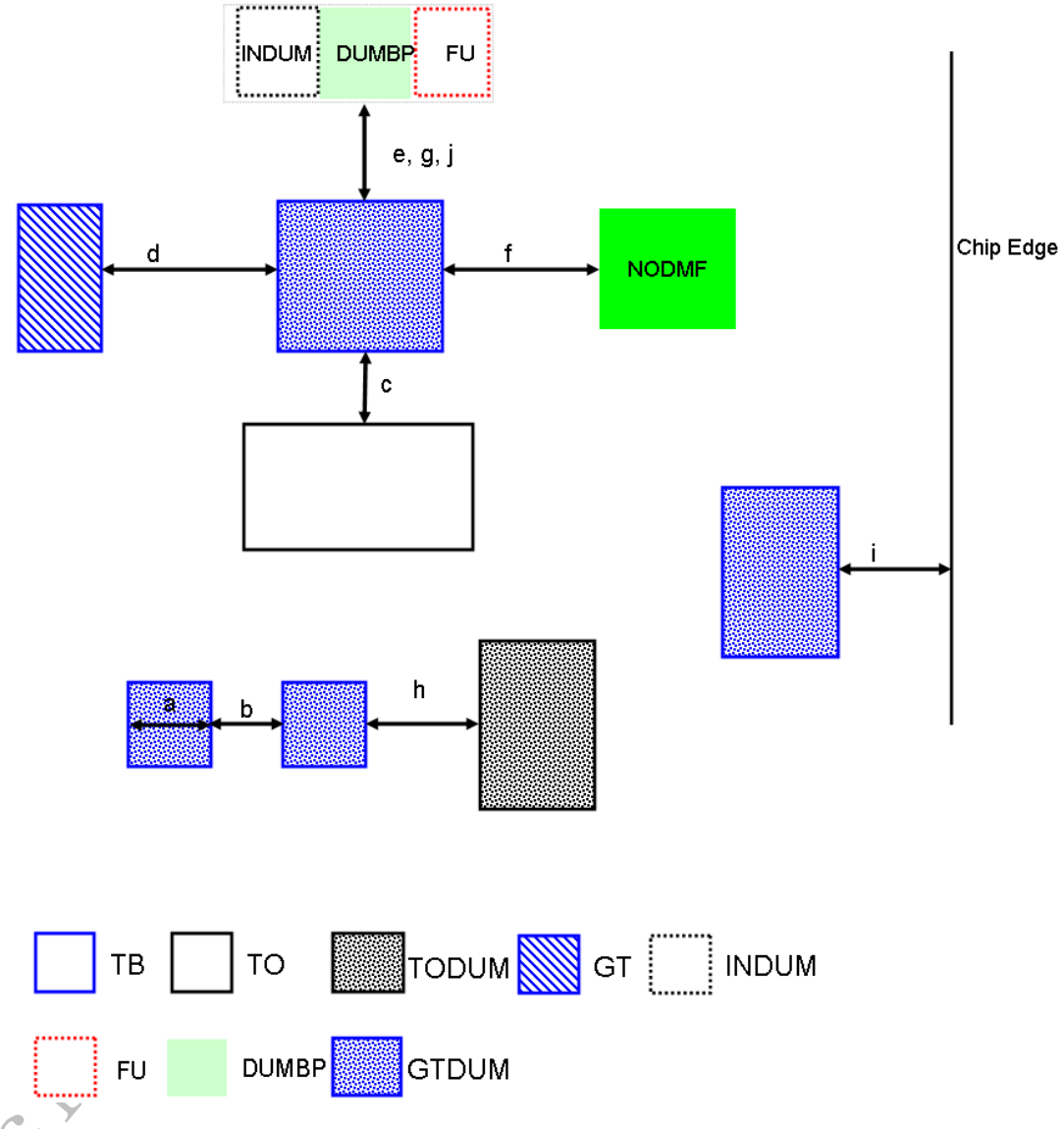
Special TODUM (TO Dummy)

No.	Description	Rule (um)
	Dummy active exclude layer shall be drawn only if necessary (for example NW&Poly resistor, MIM Capacitor, Inductor or for certain critical RF circuit area where RF coupling is critical), and please add two active dummy rings	
a	Maximum dummy active exclude layer area (um2)	10000
b	If size greater than 10000um2 then two sides should not be greater than (um)	50
c	Minimum active dummy ring	5
d	Minimum & Maximum space between active dummy ring	1
e	Minimum space from active dummy ring to functional active	2
f	Minimum space from active dummy ring to Dummy active exclude layer (overlap is not allowed)	0



5.27 GTDUM (GT Dummy)

No.	Description	Rule (um)
a	Minimum width	0.6
b	Minimum space	0.3
c	Minimum space from GTDUM to TO (overlap is not allowed)	1.2
d	Minimum space from GTDUM to GT (overlap is not allowed)	1.2
e	Minimum space from GTDUM to FU (overlap is not allowed)	1.2
f	Minimum space from GTDUM to NODMF (overlap is not allowed)	0
g	Minimum space from GTDUM to INDUM (overlap is not allowed)	1.2
h	Minimum space from GTDUM to TODUM (overlap is not allowed)	0.3
i	Minimum extension of chip edge beyond GTDUM	2.5
j	Minimum space from GTDUM to DUMBP (overlap is not allowed)	1.2
k	Minimum density of (GT or GTDUM) across full chip:15%	
l	The GTDUM inside chip corner stress relief area is not allowed (except for seal ring and stress relief pattern drawn by customer)	
m	GTDUM only shape allowed are square rectangular	
n	Minimum GTDUM area:1.2um^2	



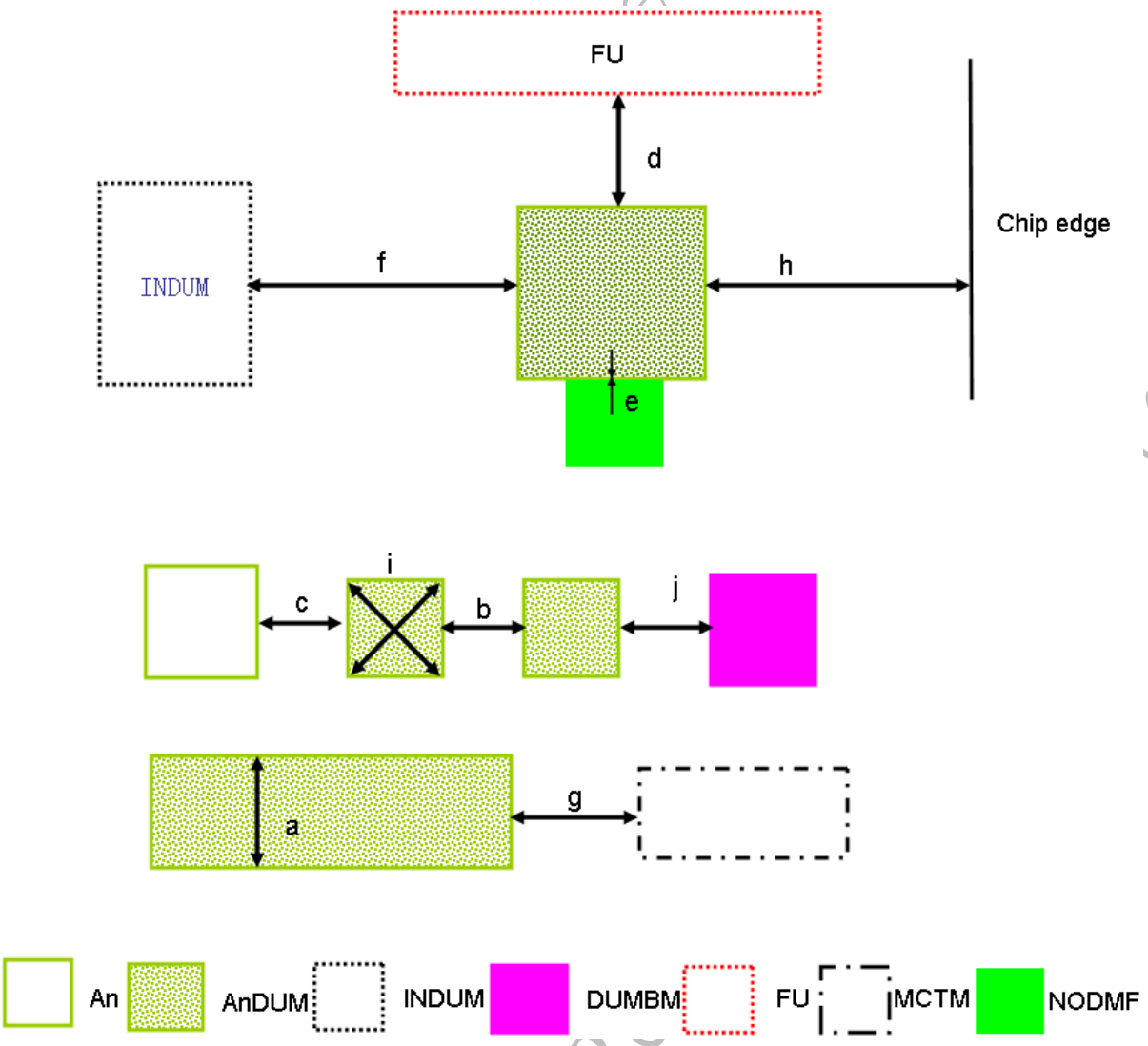
5.28 AnDUM (Metal Dummy)

No.	Description	Rule (um)
a	a1 Minimum width	below
	a2 Maximum width	3.0
b	Minimum space	below
c	Minimum space from AnDUM to An (overlap is not allowed)	below
d	Minimum space from AnDUM to FU (overlap is not allowed)	5.0
e	Minimum space from AnDUM to NODMF (overlap is not allowed)	0
f	Minimum space from AnDUM to INDUM (overlap is not allowed)	18.0
g	Minimum space from AnDUM to MCTM (overlap is not allowed)	1.5
h	Minimum extension of chip edge beyond AnDUM	2.5
i	i1 Minimum AnDUM area (um^2)	below
	i2 Maximum AnDUM area (um^2)	below

Layer	Dimension				
	a1	b	c	i1	i2
A1-An (n<6)	0.4	0.4	0.6	0.36	80
AT	0.8	0.8	0.6	0.8	160
TT	3.0	3.0	3.0	9.0	600

j	Minimum space from AnDUM to DUMBM (overlap is not allowed)	0.6
k	Minimum local density of (An or AnDUM) for A1-An (n<6):30%	
l	Minimum local density of (AT or ATDUM) or (TT or TTDUM):30%	
m	Minimum density of (An to AnDUM)(AT or ATDUM) or (TT or TTDUM) across full chip:30%	
n	Maximum density of (An to AnDUM)(AT or ATDUM) or (TT or TTDUM) across full chip:70%	
o	Maximum local density of (An or AnDUM) or (AT or ATDUM) or (TT or TTDUM):80%	
p	Minimum metal local density within DUMBM for A1-An (n<6):30%	
q	Minimum metal local density within DUMBM for AT or TT:30%	
r	Maximum metal local density within DUMBM:80%	
s	AnDUM only shape allowed are square or rectangular	
t	Recommend AnDUM size (width * length) and space is as below	
u	Adding Dummy Metal is used for improve CMP uniformity	
v	Local density is checked over any 200umx200um area(stepping in 100um increment)	

Layer	Rectangle		Square
	Width*Length/Space	AnDUM to An Space	Width*Length
A1-An (n<6)	0.4x1~0.4x10/0.83	0.93	0.6x0.6~3x3
AT	0.8x1~0.8x10/0.84	1.04	1x1~3x3
TT	3x3~3x10/3	3	3x3



5.29 Current Density Specification

For DC current density, please follow below items

5.29.1 Metal line

Jmax of A1 =1.0mA/um (at 110℃)
Jmax of A2 =1.0mA/um (at 110℃)
Jmax of A3 =1.0mA/um (at 110℃)
Jmax of A4 =1.0mA/um (at 110℃)
Jmax of A5 =1.0mA/um (at 110℃)
Jmax of A6 =1.6mA/um (at 110℃)
Jmax of TT (12K) =2.4mA/um (at 110℃)
Jmax of TT (25K) =4.5mA/um (at 110℃)
Jmax of TT (35K) =6.3mA/um (at 110℃)

5.29.2 W1,Wn (n=2, 3, 4, 5) and WT

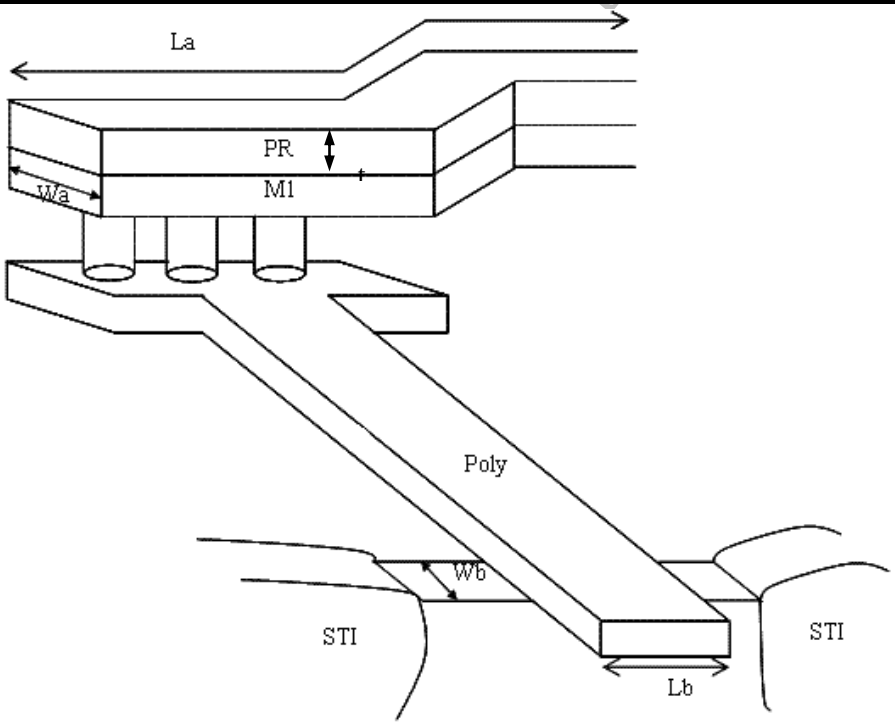
Jmax per W1 =0.16 mA (at 110℃)
Jmax per W2 =0.28 mA (at 110℃)
Jmax per W3 =0.28 mA (at 110℃)
Jmax per W4 =0.28 mA (at 110℃)
Jmax per W5 =0.28 mA (at 110℃)
Jmax per WT =0.28 mA (at 110℃)

5.29.3 Stack W1/VIA

Jmax per W1/W2 = 0.16 mA (at 110℃)
Jmax per W1/W2/W3 = 0.16 mA (at 110℃)
Jmax per W1/W2/W3/W4 = 0.16 mA (at 110℃)
Jmax per W1/W2/W3/W4/W5 = 0.16 mA (at 110℃)
Jmax per W1/W2/W3/W4/W5/WT = 0.16 mA (at 110℃)
Jmax per W2/W3 = 0.28 mA (at 110℃)
Jmax per W2/W3/W4 = 0.28 mA (at 110℃)
Jmax per W2/W3/W4/W5 = 0.28 mA (at 110℃)
Jmax per W2/W3/W4/W5/WT = 0.28 mA (at 110℃)
Jmax per W3/W4 = 0.28 mA (at 110℃)
Jmax per W3/W4/W5 = 0.28 mA (at 110℃)
Jmax per W3/W4/W5/WT = 0.28 mA (at 110℃)
Jmax per W4/W5 = 0.28 mA (at 110℃)
Jmax per W4/W5/WT = 0.28 mA (at 110℃)
Jmax per W5/WT = 0.28 mA (at 110℃)

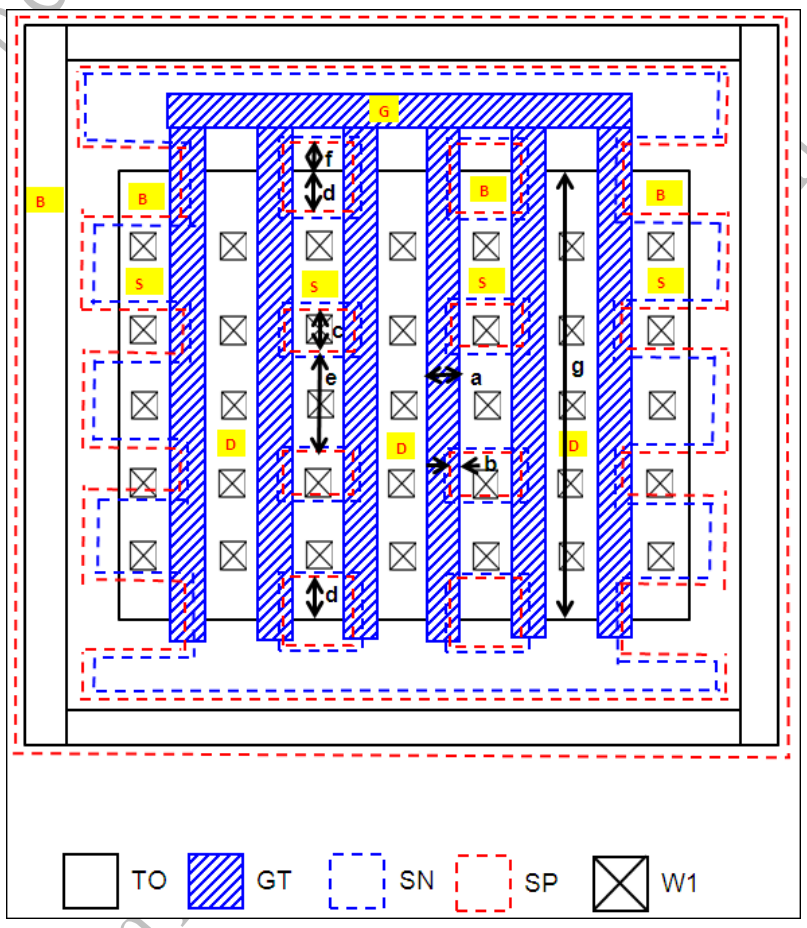
5.30 Antenna

No.	Description	Rule
a	Maximum drawn ratio of Field Poly perimeter area to the active poly gate area connected directly to it	100
b	Maximum ratio of single-layer Metal Top area to active poly gate area(for A1 to A5)	125
b1	When use a protection diode with area larger than 0.203um2, max ratio of single-layer Metal Top area to active poly gate area can be calculated by the following equation: Ratio = diode area*400+2200 for A1,2,3,4 and 5 single layer. Ratio = diode area*8000+30000 for AT single layer.	
c	Maximum drawn ratio of Poly Contact area to the active poly gate area connected directly to it.	10
d	Maximum single-layer drawn ratio of Via area to the active poly gate area connected directly to it.	20
d1	When use a protection diode with area larger than 0.203um2, max single-layer drawn ratio of Via area to the active poly gate area can be calculated by the following equation: Ratio = diode area*83.33+75 for single layer.	
e	The definition of Poly, A1~A5 antenna ratio is ratio = 2 * [(La +Wa) * t1] / (Wb * Lb)	
f	The definition of W1, Wn antenna ratio is ratio = {total contact (via) area} / (Wb * Lb)	
La	length of metal line connected to gate	
Wa	width of metal line connected to gate	
t	metal thickness	
Wb	transistor channel width	
Lb	transistor channel length	
PR	photo Resist	



5.31 Power NMOS

No.	Description	Rule（um）
a	Power NMOS Channel Length for SN/SP=1/0.5	0.5
	Power NMOS Channel Length for SN/SP=1/0.5 or 1.5/0.5	0.6
b	Minimum and Maximum SP overlap Poly	0.2
c	Minimum and Maximum SP width at the inside	0.5
d	Overlap of SP and TO at two sides	0.5
e	SP to SP Space for channel length=0.5um	1.0
	SP to SP Space for channel length=0.6um	1.0 or 1.5
f	SP extension TO at two sides.	0.31
g	Note: （1）Power NMOS Single finger channel width： For SN/SP=1/0.5 L=0.5 or 0.6um; 3.5≤Channel Width≤300um For SN/SP=1.5/0.5 L= 0.6um; 4.5≤Channel Width≤300um（2） Insert SP width fix 0.5um(including two sides, SP overlap TO=0.5um) ,SN overlap SN is forbidden	



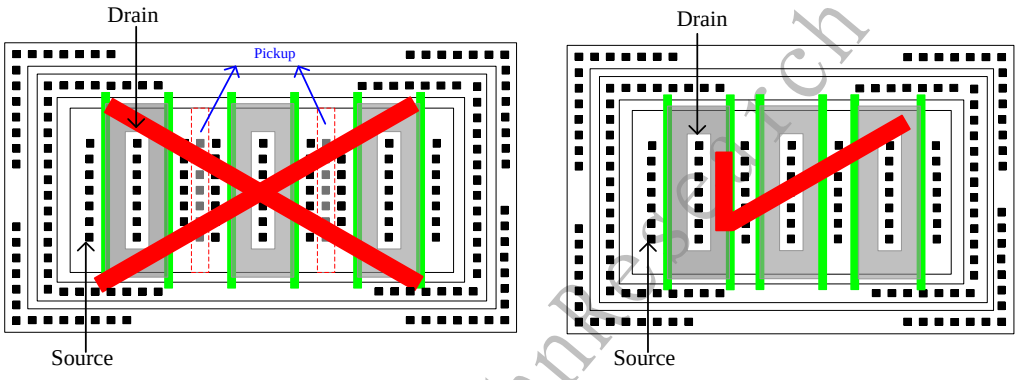
6.0 ESD design guideline:

This guideline is to meet the ESD specifications of HBM≥2KV and MM≥200V In this table, there are several ESD devices for circuit ESD protection. The ESD performance also depends on layout-style, which can not be completely described in this guideline.

ESD device Name	Description	Remark
esd_mn5_io_3t	5v IO ESD Protection	3 terminal(d/gbs/5p0v_vdd)
esd_mn5_io_5t	5v IO ESD Protection	3 terminal(d/g/b/s/5p0v_vdd)
esd_mp5_io_3t	5v IO ESD Protection	3 terminal(d/gbs/psub)
esd_mp5_io_5t	5v IO ESD Protection	3 terminal(d/g/b/s/psub)
esd_mn5_pp_3t	5v Power Clamp ESD Protection	3 terminal(d/gbs/5p0v_vdd)
esd_mn5_iso_io_4t	5v IO ESD Protection	4 terminal(d/iso/gbs/psub)
esd_mn5_iso_io_6t	5v IO ESD Protection	4 terminal(d/iso/g/b/s/psub)
esd_mn5_iso_pp_4t	5v IO ESD Protection	4 terminal(d/iso/gbs/psub)

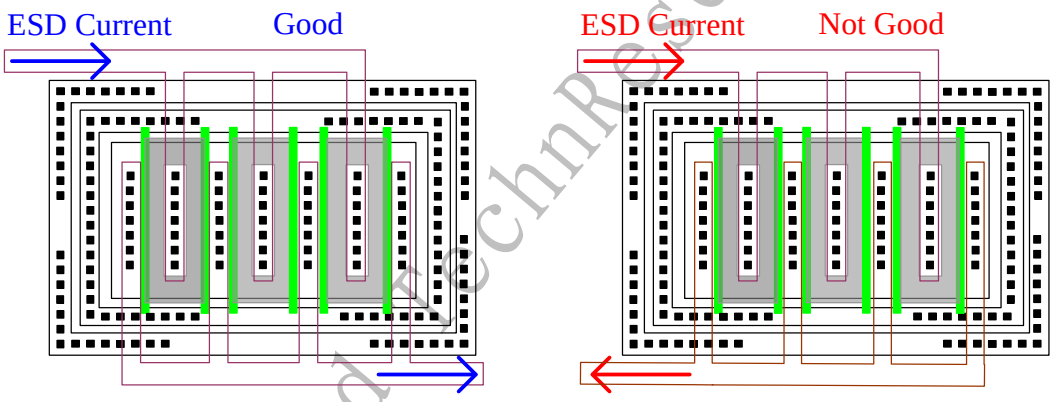
Note: in this chapter, we will give you ESD key design rules. The other design rules you must follow chapter 5.0.

1）Butting or Device inserted pickup between source diffusion of LV ESD protection devices are prohibited. IO ESD protection devices should be located in a double guard ring.

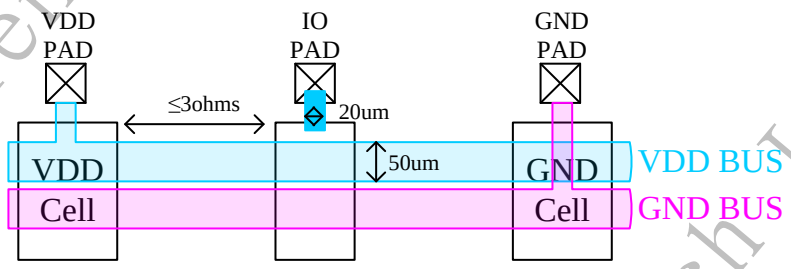


All ESD devices used in the I/Os must have the same minimum channel width. If the driver transistor with the ESD Rules it must have the same minimum channel length.

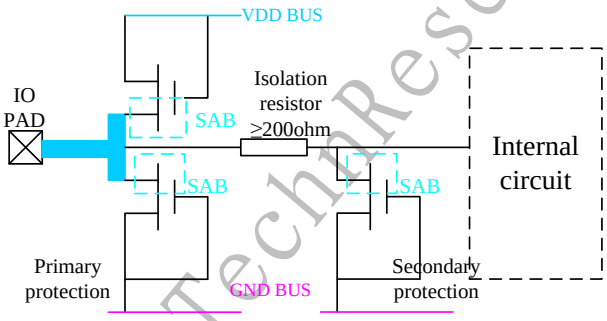
Contact density should be maximum and contact spacing should be uniform. All of the ESD devices the Source must be Outer side. The ESD devices' metal routing should be designed to avoid the current crowding.



2）The metal width directly connected between bonding pad and ESD protection devices should be at least 20um. The VDD Bus and GND Bus metal width should be at least 50um to minimize the parasitic BUS resistance. The resistance of the BUS wire from the IO cell to the VDD/VSS Cell should not exceed 3ohms. If the metal resistance is 100mohm/□, the metal width is 50um, and then the BUS distance from the VDD/VSS cell to I/O cell is restricted to 1500um.



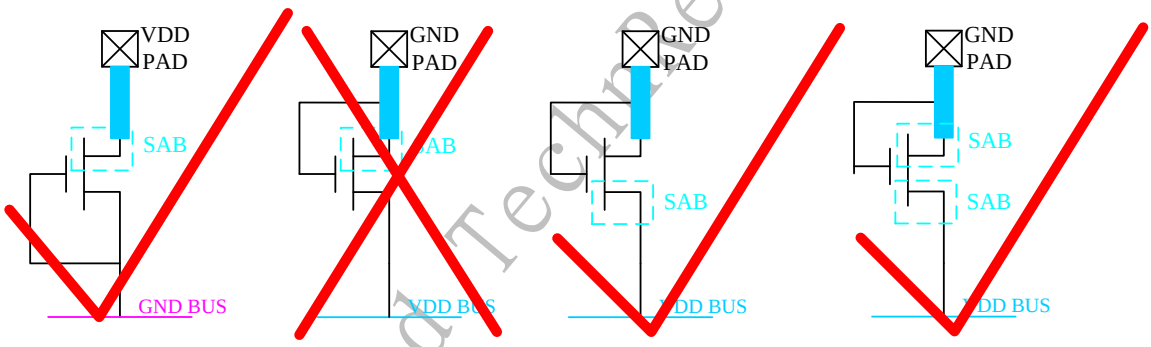
3）The IO bonding pad must be connected to the SAB in drain or source with ESD protection circuitry or device. The bonding pad of an input I/O should be connected to the primary circuitry by means of the isolation poly resistor at least 200ohms. The secondary protection device should be added after isolation resistor.



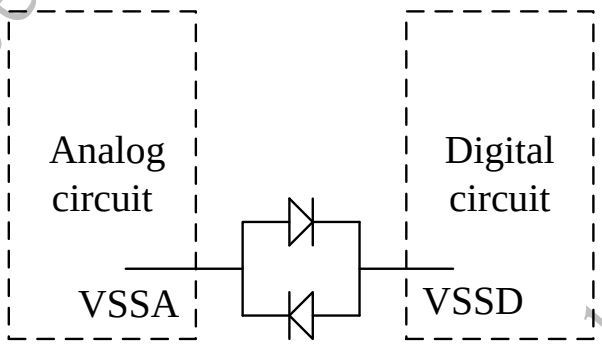
If the performance of CDM is concerned, the secondary protection device should be put close to the device gate being protected.

	Isolation Resistor(ohm)	Secondary protection	
		GGNMOS (W/L * finger)	GDPMOS
5V	<200	20/0.6*	N/A
	200<R<500	10/0.6*	N/A
	1K	N/A	N/A

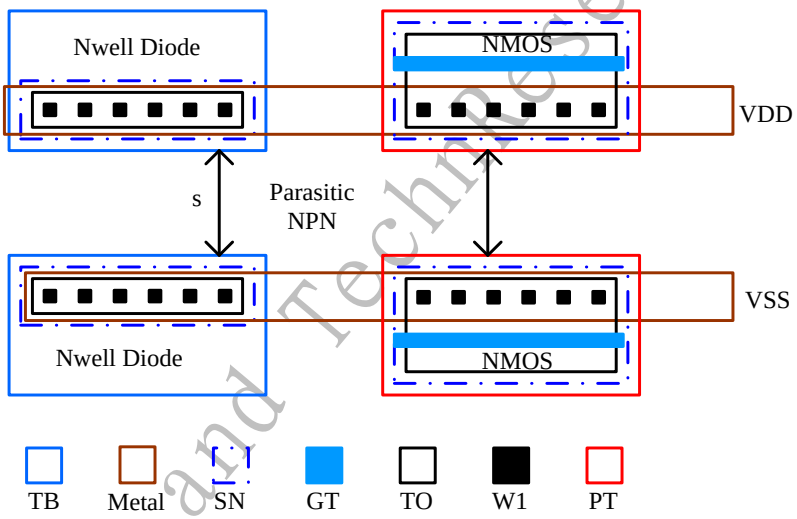
4）The GND bonding pad is connected to an area with ESD protection circuitry or devices that cannot be isolated from the SAB are prohibited.



5）In the mixed-mode IC, the separate digital and analog powers are used, inter-power ESD protection circuits should be added. The power protection may be as simple as back to back diodes if power supply voltages are the same.

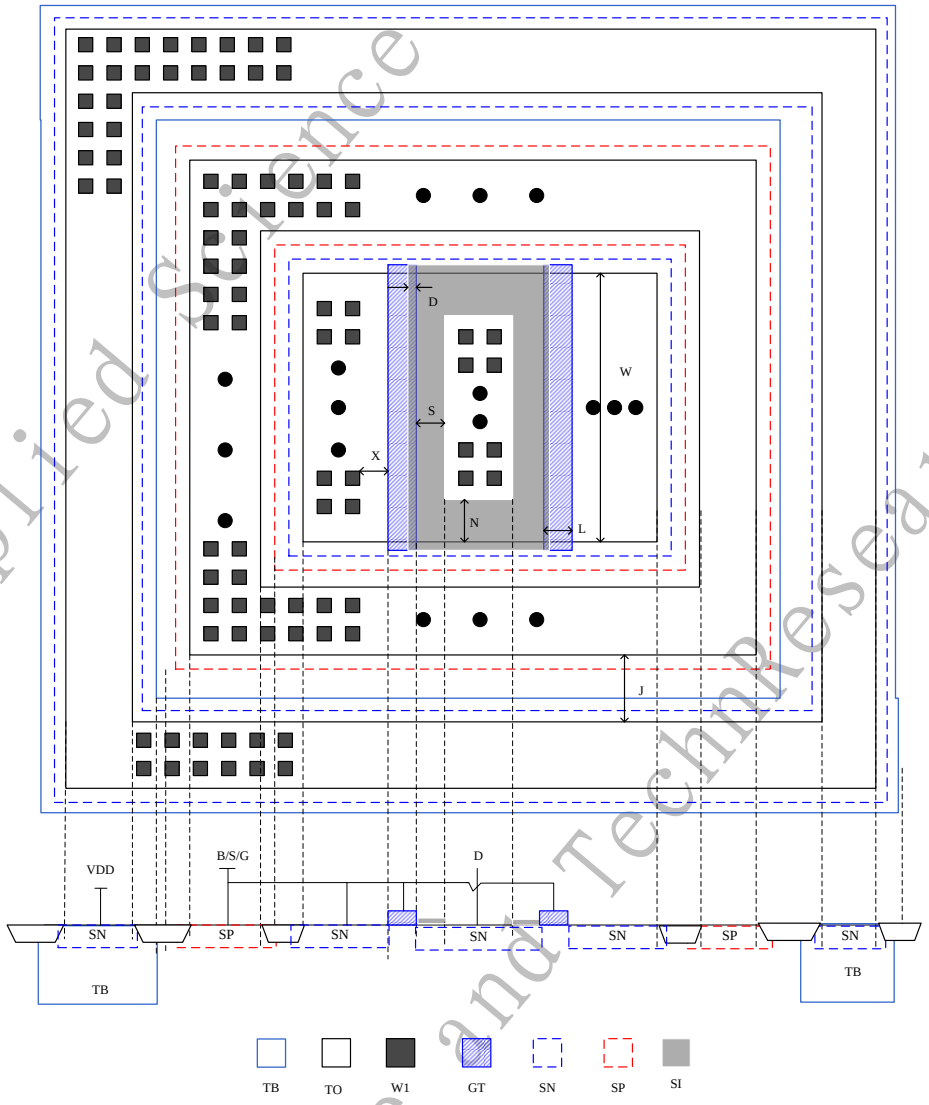


When the back to back diodes or two Active areas of the same type are used you must be take notice of the space. The ESD failure occurred to the parasitic NPN or PNP, so the Rule space of “s” as possible as larger(s>2* min D/R).



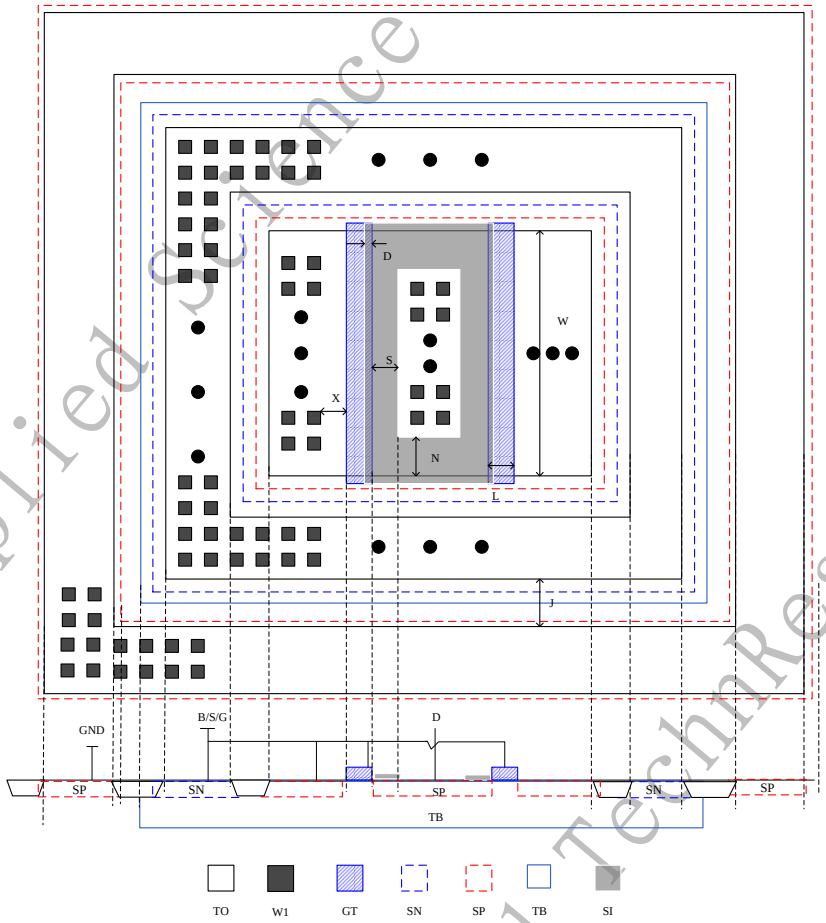
6.1 5V GGNMOS (esd_mn5 _io_3t/esd_mn5_io_5t)

No.	Description		layout rule/um
W	Per finger width should be the same.	-	20~60
	Min. Total width for 5VGGNMOS	≥	336
L	Min. channel length	≥	0.7
S	Min. clearance from SI to GT	≥	1.5
D	Min. SI overlap GT	≥	0.05
N	Min. extension from drain SI to Drain TO in Width direction	≥	S
X	Min. Source side contact to GT spacing	≥	0.5
J	Min. space between P+ pickup ring TO and TB Guard ring TO	≥	1
	Min. the number rows of contacts in drain and source	≥	2



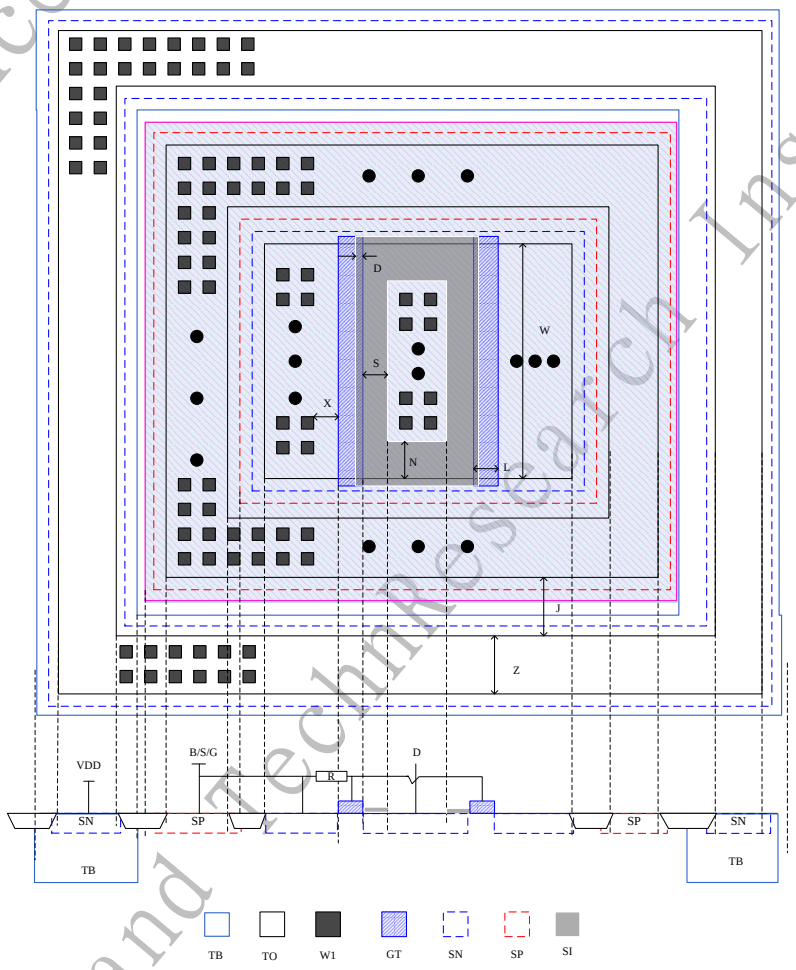
6.2 5V GDPMOS (esd_mp5_io_3t/esd_mp5_io_5t)

No.	Description		layout rule/um
W	Per finger width should be the same.	-	20~60
	Min. Total width for 5V GDPMOS	≥	504
L	Min. channel length	≥	0.7
S	Min. clearance from SI to GT	≥	1.5
D	Min. SI overlap GT	≥	0.05
N	Min. clearance from SI to TO	≥	S
X	Min. Source side contact to GT spacing	≥	0.5
J	Min. space between N+ pickup ring TO and PT Guard ring TO	≥	1
	Min. the number rows of contacts in drain and source	≥	2



6.3 5VGRNMOS (esd_mn5_pp_3t)

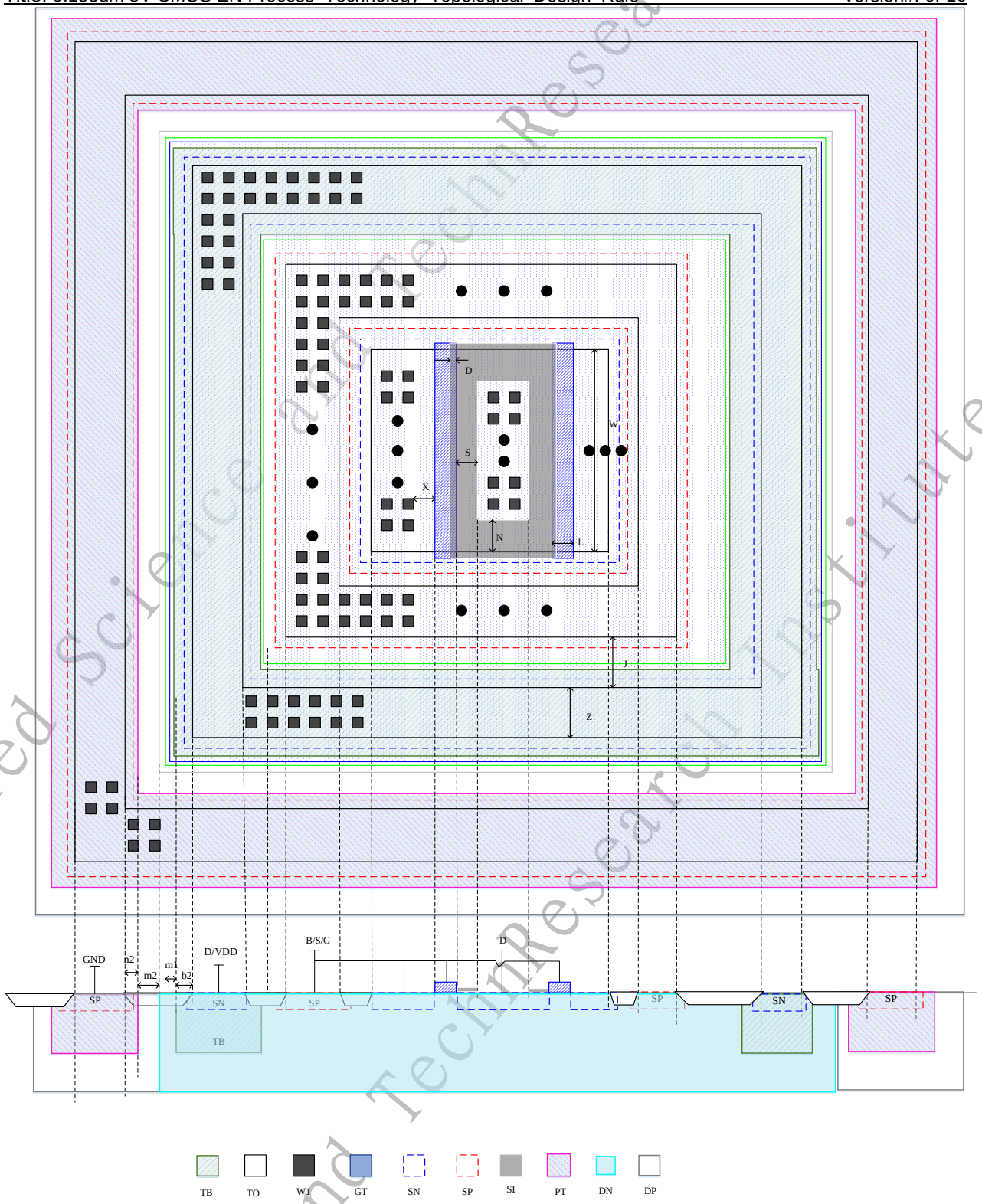
No.	Description		layout rule/um
W	Per finger width should be the same.	-	20~60
	Min. Total finger width for 5V GRNMOS	≥	840
L	Min. channel length	≥	0.7
S	Min. clearance from SI to GT	≥	1.5
D	Min. SI overlap GT	≥	0.05
N	Min. extension from drain SI to Drain TO in Width direction	≥	S
X	Min. Source side contact to GT spacing	≥	0.5
J	Min. space between P+ pickup ring TO and TB Guard ring TO	≥	1
R	Poly Resistance between Gate and Source	≥	10Kohm
	Min. length	≥	16
	Min. and Max. width	=	1
	Min. the number rows of contacts in drain and source	≥	2



6.4 5V GGNMOS_ISO and GRNMOS_ISO

(esd_mn5_iso_io_4t and esd_mn5_iso_pp_4t/ esd_mn5_iso_io_6t)

No.	Description		layout rule/um
W	Per finger width should be the same.		20~60
	Min. Total width for 5V GGNMOS_ISO	≥	336
	Min. Total width for 5V GRNMOS_ISO	≥	840
L	Min. channel length for 5V GGNMOS_ISO	≥	0.7
	Min. channel length for 5V GRNMOS_ISO	≥	0.7
S	Min. clearance from SI to GT	≥	1.5
D	Min. SI overlap GT	≥	0.05
N	Min. extension from drain SI to Drain TO in Width direction	≥	S
X	Min. Source side contact to GT spacing	≥	0.75
J	Min. space between P+ pickup ring TO and TB Guard ring TO	≥	2
n2	Min. extension from PT to TO(W/O DN)	≥	0.5
m2	Min. space from DN to PT	≥	1
m1	Min. extension of DN to TB	≥	1
b2	Min. extension from TB to TO	≥	0.5
R	Poly Resistance between Gate and Source for GRNMOS	≥	10Kohm
	Min. length	≥	16
	Min. and Max. width	=	0.5
	Min. the number rows of contacts in drain and source	≥	2



Note:
1) The P+/PT/DP isolation ring in the device periphery is necessary;
2) PT (5V Pwell) within ISO ring will be generated by Boolean rule.
3) Please keep the voltage between Iso-ring to bulk and keep the voltage between Iso-ring to substrate follow rule.

7.0 Document correlation matrix:

Document name	Design rule	Mask Tooling	Application note	Mismatch report	SPICE model	Command file	PDK(pcell)	STD library	IP
Design rule		●	●	●	●	●	●	●	●
Mask Tooling	●		●	●	●	●	●	●	●
Application note(EDR)				●	●	●	●	●	●
Mismatch Report					●				●
SPICE model						●	●	●	●
Command file(DRC/LVS/XRC)	●						●	●	
PDK(Pcell Design kitl)	●					●		●	●
STD library									●
IP									

8.0 Modify Record:

Page.	Modify Date	Old Version	New Version	Responsibility	Content
	2019-3-25	8A12	9B03	X F SUN	Change5.21;
	2019-4-9	9B03	9C04	X F SUN	Change5.21;
	2019-8-5	9C04	9D08	X F SUN	Change6.1、6.2;
	2020-1-9	9D08	0E01	X F SUN	Add5.31;
	2020-10-9	0E01	0F10	X F SUN	Change5.3、6.0;

——END——