CSMC 0.11um e-FLASH_2P8M_Salicide Process 1.5V 6T STD Library (including PMK)

Version 0.2
Sep. 2019
CSMC Corp.

Notice

Disclaimer
CSMC CORPORATION RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS DESCRIBED HEREIN. CSMC CORPORATION MAKES NO WARRANTY, REPRESENTATION, OR GUARANTEE REGARDING THE SUITABILITY OF ITS PRODUCTS FOR ANY PARTICULAR PURPOSE, NOR DOES CSMC CORPORATION ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT, AND SPECIFICALLY DISCLAIMS ANY AND ALL LIABILITY, INCLUDING WITHOUT LIMITATION, CONSEQUENTIAL OR INCIDENTAL DAMAGES.

Proprietary Rights Notice
This document contains information of a proprietary nature. No part of this manual may be copied or distributed without the prior written consent of CSMC corporation. This document and the software described herein is only provided under a written license agreement or a type of written non-disclosure agreement with CSMC corporation or its subsidiaries.

ALL INFORMATION CONTAINED HEREIN SHALL BE KEPT IN CONFIDENCE AND USED STRICTLY IN ACCORDANCE WITH THE TERMS OF THE WRITTEN NON-DISCLOSURE AGREEMENT OR WRITTEN LICENSE AGREEMENT WITH CSMC CORPORATION OR ITS SUBSIDIARIES.

Trademark/Service-Mark Notice
Planet, Planet-PL, Planet-RTL, Solar, Star-Sim, Star-Hspice, HSPICE, Star-HspiceLink, HSPICE-LINK, AvanWaves, Sirius, Star-DC, Star-RC, Star-Power, Star-MTB, MASTER Toolbox, Hercules, LTL, Passport, V- Formal, Lynx-VHDL, laybool, Lynx-LB, Datapath Compiler, Chip Compiler, PathFinder, ChipPlanner, DesignVP, Optimum Silicone, QTV, Polaris, Polaris-CBS, Polaris-MT, Device Model Builder (DMB), Avan Test-chip, ArcCell, ArcChip, ArcUtil, ADM, ATEM, Evaccess, Explorer, Pure Speed, CycleLink, BaseLine, SimLine, DriveLine, Dynamic Model Switcher, Base Line Software Accelerator, Smart Extraction, VeriView, VeriCheck, Chips Crunch, and Time are trademarks of CSMC Corporation and its subsidiaries.

CSMC Corporation, CSMC logo, and AvanLabs are trademarks and service-marks of CSMC Corporation.

All other trademarks are the property of their respective owners.

Revision History

Document Version Number	Library Version Number	Date	Notes
0.0	0.0	Sep 2018	Initial Production Release
0.1	0.1	Jan 2019	Improve pmk description
0.2	0.2	Sep.2019	1.2v corner not provided

Table of content

Introduction

This manual addresses the design engineer who is doing a preliminary feasibility evaluation and wishes to make comparisons among the available technologies. Additionally, you can use this library manual while designing a chip, to see which cells are available, and to check the power consumption, critical timing values, propagation delay equations, and functions of a cell.

The datasheets only show individual pin-to-pin timings for the storage elements. For other cells, the delays in the datasheets are combined as typical-case delays for the purpose of readability.

Product Description

The Synthesis Standard Cell Library is a new set of standard cells that replaces the current high-density and high-performance standard cell sets. The cell set functionality and drive strengths are optimized for industry standard synthesis design entry using Verilog or VHDL driving Synopsys or the ASIC Synthesizer. The cell layout is optimized for industry-leading, area-based routers.

The CSMC011 Library is a high-performance, standard cell library in CSMC 0.11- micron Eflash 2P8M process.

Contents of This Manual

This introduction contains the following sections:

- The *General Information* section of this book gives basic information on the conditions under which this library was characterized and offers assistance in using derating factors and estimating propagation delay.
- The *Cells* section describes the contents of the datasheets and how to interpret them. It also explains how to decode the cell names.
- The tables in the *Cell Matrices* section give a quick reference to the features of storage elements in the library.

Following this introduction, there are three sections:

- Simple Logic Gates - AND, AND-OR-Invert, NAND, NOR, OR, OR-AND- Invert, exclusive-OR, and exclusive-NOR gates; buffers, clock buffers and 3- state buffers with both active-high and active-low enables.
- Storage Elements - D flip-flops, JK flip-flops, latches, multiplexed flip-flops, latches, scan latches, and scan flip-flops.
- Special Functions - Adders, adder/subtractors, carry generators, multiplexers, and symbolic cells.

Within these divisions, the library cells are listed in alphabetical order where possible. Cells of a similar type have been combined. For example, the information for all the 2-input NAND gates - ND02D0, ND02D1, ND02D2, and ND02D4 - has been combined into one datasheet.

For storage elements, there is a cover page listing the common information for all cells of that type, then the following pages give information specific to individual cells in the grouping. For example, there is a cover page for D flip-flops with set and clear, then a page each on DFBRB1 and DFBRB2.

Buffers have been grouped together by type with different drive capabilities. For example, INV0D0, INV0D1, INV0D2, IN0VD4 and IN0VD8 have been combined on a single datasheet.

Recommended Operating Conditions

Table 1 shows the physical design specifications of this library.

Drawn Gate Length (um)	0.13
Layers of Metal	4,5,6, 7 or 8
Layout Grid (um)	0.001
Vertical Pin Grid (um)	0.366
Horizontal Pin Grid (um)	0.37
Cell height (um)	2.196
Cell Power and Ground Rail Width (um)	0.26

Table 1. Physical Specifications

In this library, all pins are located on the vertical and horizontal pin grids. Most place-and-route tools work more efficiently with all pins on grids, and some tools even require it.

The library supports designs with four,five,six, seven or eight layers of metal. You may need to change the design rules in the technology file, because the top-level metal has a greater minimum width and greater minimum spacing requirement.

Table 2 describes the electrical specifications for this library.

Conner	**Minimum (0 ℃)**	**Minimum (125 ℃)**	**Minimum (-40 ℃)**	**TYPICAL**	**Maximum**	**Maximum**
DC Supply Voltage (Vdd)	1.65	1.65v	1.65v	1.5v	1.35v	1.35v
Junction Temperature	0℃	125℃	-40 ℃	25℃	125℃	85℃

Table 2. 1.5V Electrical Specifications

AC Characteristics

Timing Measurement Conditions

Unless otherwise specified:

VDD = 1.5 volts

Junction Temperature = 25 degrees C

Process = typical case

AC Timing Definitions

Propagation Delay and Transition Time

The propagation delay through a cell is the sum of the intrinsic delay, theload dependent delay, and the input-slew dependent delay. Delays are defined as thetime interval between the input stimulus crossing 50% of Vdd and the output rossing 50% of Vdd. Figure 1 illustrates the propagation delay.

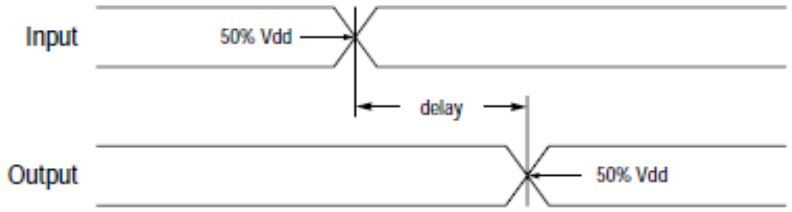


Figure 1. Propagation Delay

The transition times (slews) on input and output pins are defined as the timeinterval between the signal crossing 10% of Vdd and 90% of Vdd. Figure 2 llustrates transition time measurements for rising and falling signals.

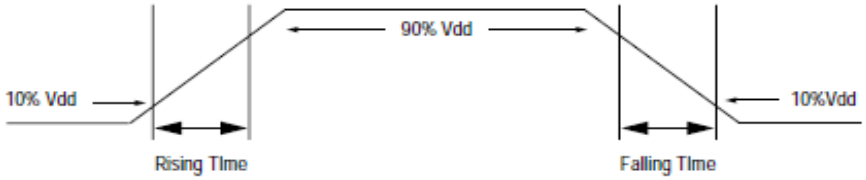


Figure 2. Transition Time

Timing Constraints

Timing constraints define minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing constraints include: setup time, hold time, recovery time, and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time and data-signal and clock-signal polarity on timing constraints. Timing constraints can affect propagation delays. The intrinsic delays given in the datasheets are measured with relaxed timing constraints (longer than necessary setup times, hold times, recovery times, and pulse widths). The use of shorter timing constraint intervals may increase delay. Each cell is considered functional as long as the actual delay does not exceed the delay given in the datasheets by more than 10%.

Setup Time

The setup time for a sequential cell is the minimum length of time the data-input signal must

remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.
Setup constraint values are measured as the interval between the data signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd. For the measurement of setup time, the data input signal is kept stable after the active clock edge for an infinite hold time. Figure 3 illustrates setup time for a positive-edge-triggered sequential cell.

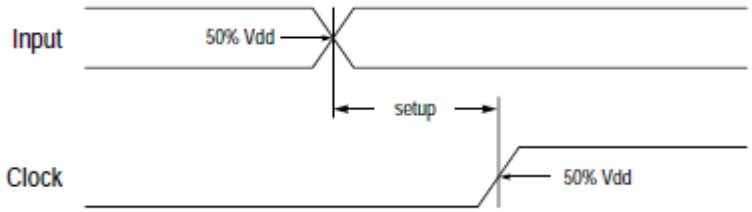


Figure 3. Setup Time

Hold Time

The hold time for a sequential cell is the minimum length of time the data-input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.
Hold-constraint values are measured as the interval between the data signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd. For the measurement of hold time, the data input signal is held stable before the active clock edge for an infinite setup time. Figure 4 illustrates hold time for a positive-edge-triggered sequential cell.

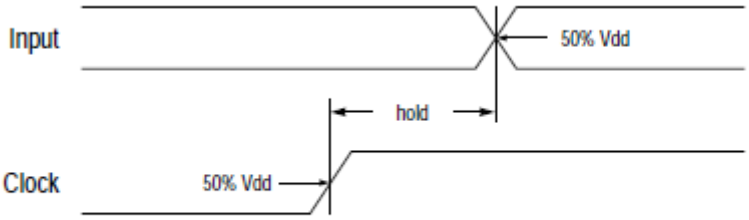


Figure 4. Hold Time

Recovery Time

Recovery time for sequential cells is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%.
Recovery constraint values are measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd. For the measurement of recovery time, the set or reset signal is held stable after the active clock edge for an infinite hold time.Figure 5 illustrates recovery time.

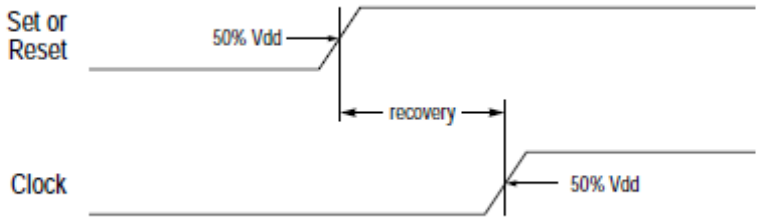


Figure 5. Recovery Time

Minimum Pulse Width

Minimum pulse width is the minimum length of time between the leading and trailing edges of a pulse waveform. Minimum pulse width high (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of Vdd and the falling edge of the signal crossing 50% of Vdd. Minimum pulse width low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of Vdd and the rising edge of the signal crossing 50% of Vdd. Figure 6 illustrates minimum pulse width.

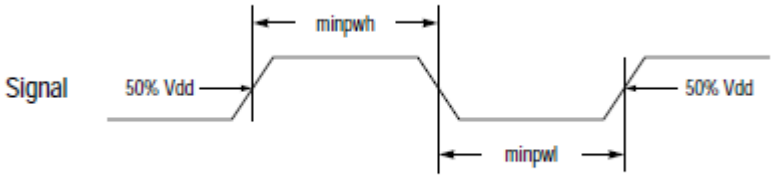


Figure 6. Minimum Pulse Width

The value in this datasheet is just for customer reference.

Cells

Buffers and Gates

Name Decoding Scheme: *aaaa*D*n*

aaaa = Name of the cell:

AN = AND Gate
AOI = AND-OR-Invert Gate
AOR = AND-OR Gate
BH = Bus Holder
BUFF = Non-Inverting Buffer
BUFT = Non-Inverting 3-State Buffer
CLK2 = 2-Phase Non-Overlapping Clocks
CKAND = CLOCK AND Gate
CKBUF = CLOCK Non-Inverting Buffer
CKINV = CLOCK Inverter
CKXR = CLOCK Exclusive OR Gate
DL = Non Inverting Delay Buffer
INV0 = Inverter
INVT = Inverting 3-State Buffer
ND = NAND Gate
NR = NOR Gate
OAI = OR-AND-Invert Gate
OR = OR Gate
ORA = OR-AND Gate
XN = Exclusive NOR Gate
XR = Exclusive OR Gate

n = Drive Strength

0 = Minimum drive
M = Between 0 and 1
1 = Basic drive speed
2 = 2 times basic drive speed
3 = 3 times basic drive speed
4 = 4 times basic drive speed

Multiplexers

Name Decoding Scheme: *aabc*D*n*

aa = Name of the Cell:

MX = Multiplexer
MI = Inverting Multiplexer
CKMX = CLOCK Multiplexer

b = Number of Inversions in the Input

c = Number of Inputs

n = Drive Strength

Flip-Flops

Name Decoding Scheme: *aabcdn*

aa = Name of the Cell
- DF = D Flip-Flop
- DE = D Flip-Flop with D Enable
- JK = JK Flip-Flop

b = Preset and Clear Notation
- B = Both Preset and Clear
- C = Clear
- P = Preset
- N = None

c = Clock Edge
- R = Positive Rising Edge
- F = Negative Falling Edge

d = Number of Output Pins:
- B = Both Q and QN
- Q = Q Only
- N = QN Only

n = Drive Strength

Scan Flip-Flops

Name Decoding Scheme: *aabcdn*

aa = Name of the Cell:
- SD = Multiplexed Scan D Flip-Flop
- SE = Multiplexed Scan D Flip-Flop with D Enable

b = Preset and Clear Notation:
- B = Both Preset and Clear
- C = Clear
- P = Preset
- N = None

c = Enable:
- H = Active High Enable
- L = Active Low Enable

d = Number of Output Pins:
- B = Both Q and QN
- Q = Q Only
- N = QN Only

n = Drive Strength

Latches

Name Decoding Scheme: *aabcdn*

aa = Name of the Cell:

LA = D Latch

b = Preset and Clear Notation:
- B = Both Preset and Clear
- C = Clear
- P = Preset
- N = None

c = Enable:
- H = Active High Enable
- L = Active Low Enable

d = Number of Output Pins:
- B = Both Q and QN
- Q = Q Only
- N = QN Only
- T = Z Only

n = Drive Strength

Adders/Subtractors

Name Decoding Scheme: *aabc*D*n*

aa = Name of the Cell
- AD = Adder
- AH = Half Adder

b = Number of Inversions in the Input

c = Number of Bits

n = Drive Strength

Decoding the Cell Name

This section describes the naming conventions for the cells in the CSMC011 . Each cell name begins with either a two-, three-,four- or five-letters code that defines the type of cell. These codes are listed in the following table; the sections that follow give the detailed naming conventions for each cell type.

STD

Code	Description
AD	Adder
AH	Half Adder
AN	AND Gate
AOI	AND-OR-Invert Gate
AOR	AND-OR Gate
BH	Bus Holder
BUFF	Non-Inverting Buffer
BUFT	Non-Inverting 3-State Buffer
CKAND	Clock AND Gate
CKBUF	Clock Non-Inverting Buffer
CKINV	Clock Inverter
CKMX	Clock Multiplexer
CKXR	Clock Exclusive OR Gate
DE	D-Enabled Flip-Flop
DF	D Flip-Flop
INV0	Inverter
INVT	Inverting 3-State Buffer
LA	D Latch
MI	Inverting Multiplexer
MX	Multiplexer
ND	NAND Gate
NR	NOR Gate
OAI	OR-AND-Invert Gate
OR	OR Gate
ORA	OR-AND Gate
SD	Multiplexed Scan D Flip-Flop
SE	Multiplexed Scan Enable D Flip-Flop
XN	Exclusive NOR Gate
XR	Exclusive OR Gate

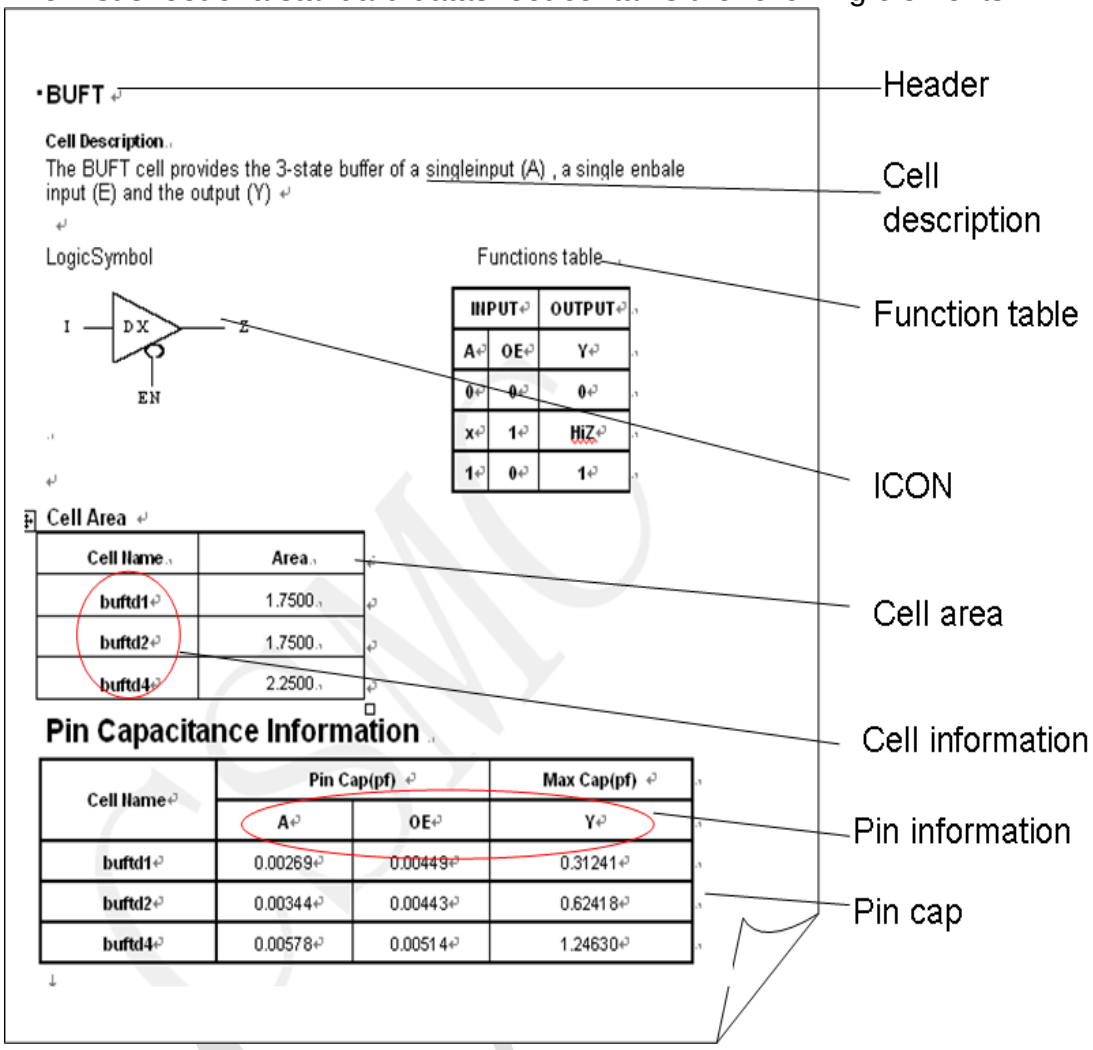
PMK

Code	Description
GPG	Always On
Head	Power Gating
ISO	Isolation Cell
DRF	Retention DFF

SRD	Retention DFF With Scan

Reading the Datasheet

The first sheet of a standard datasheet contains the following elements:



Header and cell Description

The cell header in the large font describes the cell type, such as Clock Buffer with Positive Clock Input. Under the header is a list of the cells included in the category, in a smaller font. The text block following the headers gives a brief description of the cells included in this datasheet.

Icon

The icon pictured on the datasheet is the one you will see in the DC_vision Tools when you place a schematic element.

Truth Table

The Truth Table gives all the possible combinations of input and output signals for this cell type. The following symbols are used in the Truth Tables on the datasheets

0	=	Low level	Q	=	Current Q

1	=	High level	Qn	=	Current QN, also complement of Q
R	=	Low to High transition	Q0	=	Previous level of Q
F	=	High to Low transition	QN0	=	Previous level of QN, also complement of Q0
X	=	Any level (Don't Care)	HiZ	=	High impedance state
U	=	Unknown	Zrl	=	3-state output with resistive pull down
Rh	=	Resistive High	Zrh	=	3-state output with resistive pullup
Rl	=	Resistive Low	Z	=	3-state output

Cell Information and Cell Area

More details please refer to doc/DATASHEET/*

Pin Iinformation and Pin capcacitance

More details please refer to doc/DATASHEET/*

The a details on standard datasheet contains the following information:

Propagation Delays for Sample Loads

The Propagation Cell Delays e Loads table are extrapolated from the characterized look-up table values using the max , middle , min load and skew input. The value can be used for reference.

Pin Power Table

The pin power table gives for each pin of the table a dissipated power from the Synopsys look-up table models. This power is given for a standard load and a standard input transition. The power data provided are the internal power for input pin when outputs doesn't switch, and the internal power for output pins.

Note:

Conditions that all of these data is gotten under are Ctyp_tt_1p5v_25c, 25.0℃,VDD 1.5V, GND 0V. The RISE and FALL times represent the total delay time from the change of the input pin to the corresponding response on the output pin. Actual interconnect length and load cannot be determined until a design has completed placement and routing. When using these tables, you must estimate the interconnect load in units of standard loads and add that to the fanout. A rough rule of thumb is that, for every input load, there is a corresponding interconnect load approximately equal to it. For example, to estimate the delay of a NAND gate driving a fanout of two, use the column in the datasheet specifying four standard loads: two for fanout and two for the interconnect loading.

Arithmetic Gates

AD01

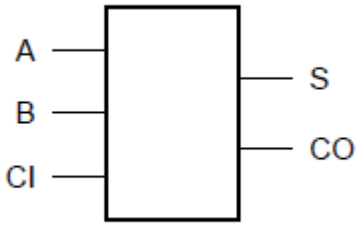
Cell Description

The AD01 cell provides the arithmetic sum (S) and carry out (CO) of two operands (A, B) with carry in (CI). The two outputs (S, CO) are represented by the logic equations:

$S = (A \oplus B \oplus CI)$

$$CO = (A \oplus B) \bullet CI + (A \bullet B)$$

Logic Symbol



Truth Table

CI	A	B	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

More details refer to doc/DATASHEET/

ADFH

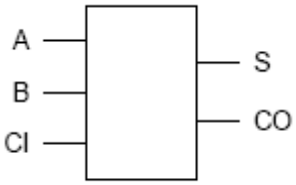
Cell Description

The ADFH01 cell is a high-speed cell providing the arithmetic sum (S) and carry out (CO) of two operands (A, B) with carry in (CI). The two outputs (S, CO) are represented by the logic equations:

$$S = (A \oplus B \oplus CI)$$

$$CO = (A \oplus B) \bullet CI + (A \bullet B)$$

Logic Symbol



Truth Table

INPUT			OUTPUT	
A	B	CI	CO	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

More details refer to doc/DATASHEET/*

AH01

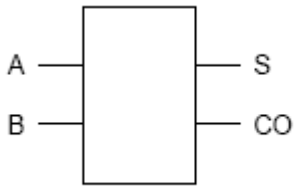
Cell Description

The AH01 cell provides the arithmetic sum (S) and carry out (CO) of two operands (A, B). The two outputs (S, CO) are represented by the logic equations:

S=A^B

CO = A • B

Logic Symbol



Truth Table

INPUT		OUTPUT	
A	B	CO	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

More details refer to doc/DATASHEET

BUFFS

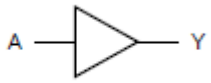
CKBUF

Cell Description

The CKBUF cell provides the logical buffer of a single input (A), with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$$Y = A$$

LogicSymbol



Truth Table

A	Y
0	0
1	1

More details refer to doc/DATASHEET/*

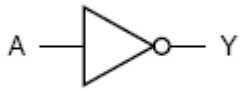
CKINV

Cell description:

The CLKINV cell provides the logical inversion of a single input (A), with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$$Y = !A$$

Logic Symbol



Truth Table

INPUT	OUTPUT
A	Y
0	1
1	0

More details refer to doc/DATASHEET/*

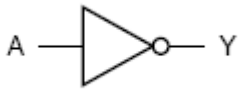
INV0

Cell Description

The INV0 cell provides the logical inversion of a single input (A). The output (Y) is represented by the logic equation:

$$Y = !A$$

Logic Symbol



Truth Table

INPUT	OUTPUT
A	Y
0	1
1	0

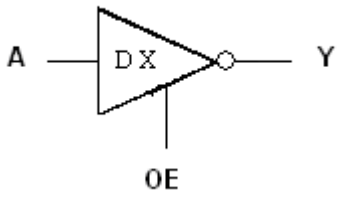
More details refer to doc/DATASHEET/*

INVTL

Cell Description

The INVTL cell provides the 3-state inverter of a singleinput (A) , a single high enable input (OE) and the output (Y)

LogicSymbol



Truth Table

INPUT		OUTPUT
A	OE	Y
x	0	HiZ
0	1	1
1	1	0

More details refer to doc/DATASHEET/*

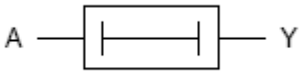
DL01

Cell Description

The DL01 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$$Y = A$$

Logic Symbol



Truth Table

INPUT	OUTPUT
A	Y
0	0
1	1

More details refer to doc/DATASHEET/*

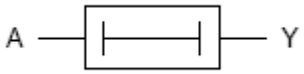
DL02

Cell Description

The DL02 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$$Y = A$$

Logic Symbol



Truth Table

INPUT	OUTPUT
A	Y
0	0
1	1

More details refer to doc/DATASHEET/*

COMPLEX Gates

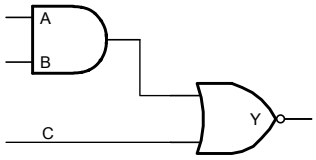
AOI21

Cell Description

The AOI21 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = !((A \bullet B) + C)$$

Logic Symbol



Truth Table

INPUT			OUTPUT
A	B	C	Y
0	x	0	1
x	x	1	0
1	0	0	1
1	1	x	0

More details refer to doc/DATASHEET/*

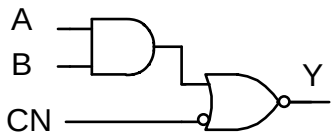
AOI21M

Cell Description

The AOI21M cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = (!((\ A \bullet\ B)+(\ !CN)))$$

Logic Symbol



Truth Table

INPUT			OUTPUT
A	**B**	**CN**	**Y**
x	**x**	**0**	**0**
0	**x**	**1**	**1**
1	**0**	**1**	**1**
1	**1**	**1**	**0**

More details refer to doc/DATASHEET/*

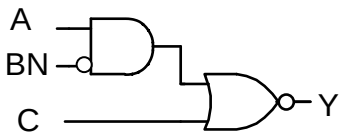
AOI2M1

Cell Description

The AOI2M1 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = (!((A \bullet (!BN)) + C))$$

Logic Symbol



Truth Table

INPUT			OUTPUT
A	BN	C	Y
0	x	0	1
0	x	1	0
1	0	x	0
1	1	0	1
1	1	1	0

More details refer to doc/DATASHEET/*

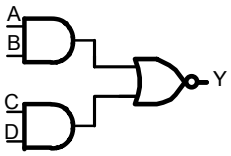
AOI22

Cell Description

The AOI22 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = !\ (\ (\ A \bullet\ B) + (C \bullet\ D)\ )$$

Logic Symbol



Truth Table

INPUT				OUTPUT
A	B	C	D	Y
0	x	0	x	1
0	x	1	0	1
x	x	1	1	0
1	0	0	x	1
1	0	1	0	1
1	1	x	x	0

More details refer to doc/DATASHEET/*

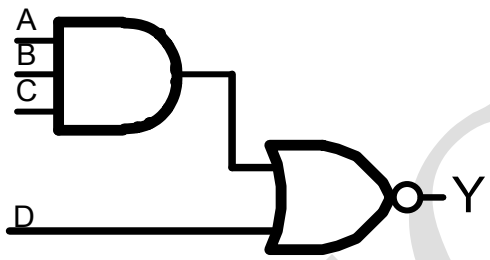
AOI31

Cell Description

The AOI31 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \ !\ （\ (A \bullet B \bullet C) + D）$$

Logic Symbol



Truth Table

INPUT				OUTPUT
A	B	C	D	Y
0	x	x	0	1
x	x	x	1	0
1	0	x	0	1
1	1	0	0	1
1	1	1	x	0

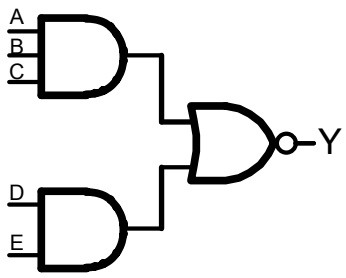
More details refer to doc/DATASHEET/*

AOI32

The AOI32 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = !((A \bullet B \bullet C)+(D \bullet E))$$

Logic Symbol



Truth Table

INPUT					OUTPUT
A	B	C	D	E	Y
0	x	x	0	x	1
0	x	x	1	0	1
x	x	x	1	1	0
1	0	x	0	x	1
1	0	x	1	0	1
1	1	0	0	x	1
1	1	0	1	0	1
1	1	1	x	x	0

More details refer to doc/DATASHEET/*

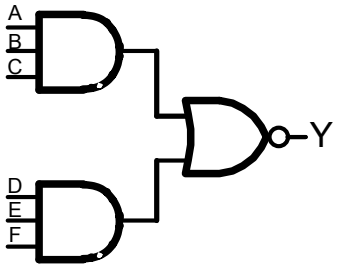
AOI33

Cell Description

The AOI33 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \ !\ (\ (\ A \bullet B \bullet C) + (D \bullet E \bullet F)\ )$$

Logic Symbol



Truth Table

INPUT						OUTPUT
A	B	C	D	E	F	Y
0	x	x	0	x	x	1
0	x	x	1	0	x	1
0	x	x	1	1	0	1
x	x	x	1	1	1	0
1	0	x	0	x	x	1
1	0	x	1	0	x	1
1	0	x	1	1	0	1
1	1	0	0	x	x	1
1	1	0	1	0	x	1
1	1	0	1	1	0	1
1	1	1	x	x	x	0

More details refer to doc/DATASHEET/*

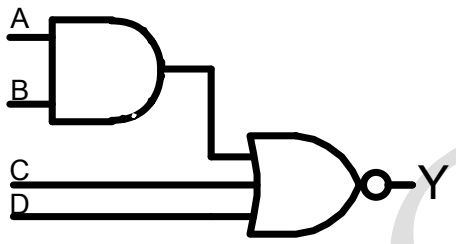
AOI211

Cell Description

The AOI211 cell provides the logical inverted OR of one AND groups and two addition inputs. The output (Y) is represented by the logic equation:

$$Y = (!(D|C|(A\&B)))$$

Logic Symbol



Truth Table

INPUT				OUTPUT
A	B	C	D	Y
0	x	0	0	1
0	x	x	1	0
x	x	1	x	0
1	0	0	0	1
1	0	x	1	0
1	1	x	x	0

More details refer to doc/DATASHEET/*

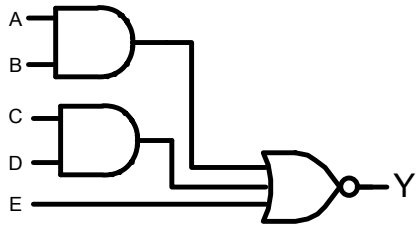
AOI221

Cell Description

The AOI221 cell provides the logical inverted OR of two AND groups and a third input. The output (Y) is represented by the logic equation:

$$Y = !((A \bullet B)+(C \bullet D)+E)$$

Logic Symbol



Truth Table

INPUT					OUTPUT
A	B	C	D	E	Y
0	x	0	x	0	1
0	x	x	x	1	0
0	x	1	0	0	1
x	x	1	1	x	0
1	0	0	x	0	1
1	0	x	x	1	0
1	0	1	0	0	1
1	1	x	x	x	0

More details refer to doc/DATASHEET/*

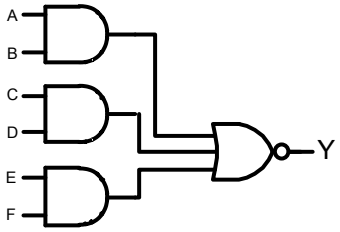
AOI222

Cell Description

The AOI222 cell provides the logical inverted OR of three AND groups. The output (Y) is represented by the logic equation:

$$Y = !((A \bullet B)+(C \bullet D)+(E \bullet F))$$

Logic Symbol



Truth Table

INPUT						OUTPUT
A	B	C	D	E	F	Y
0	x	0	x	0	x	1
0	x	0	x	1	0	1
0	x	x	x	1	1	0
0	x	1	0	0	x	1
0	x	1	0	1	0	1
x	x	1	1	x	x	0
1	0	0	x	0	x	1
1	0	0	x	1	0	1
1	0	x	x	1	1	0
1	0	1	0	0	x	1
1	0	1	0	1	0	1
1	1	x	x	x	x	0

More details refer to doc/DATASHEET/*

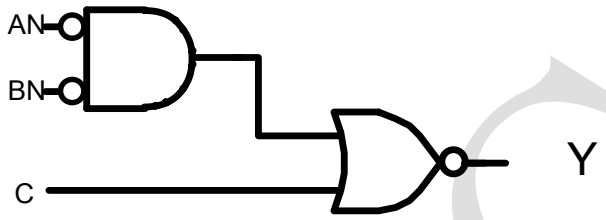
AOIM21

Cell Description

The AOIM21 cell provides the logical inverted OR of one AND group of two inverted inputs (A0N, A1N) and an additional non-inverted input (B0).The output (Y) is represented by the logic equation:

Y = ((!C)&(AN|BN))

Logic Symbol



INPUT			OUTPUT
AN	BN	C	Y
0	0	x	0
x	1	0	1
x	1	1	0
1	x	0	1
1	x	1	0

Truth Table

More details refer to doc/DATASHEET/*

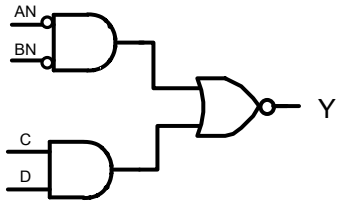
AOIM22

Cell Description

The AOIM22 cell provides the logical inverted OR of one AND group of two inverted inputs (A0N, A1N)and one AND group of two non-inverted inputs (B0,B1).The output (Y) is represented by the logic equation:

Y = (!(((!AN)&(!BN))|(C&D)))

Logic Symbol



Truth Table

INPUT				OUTPUT
AN	**BN**	**C**	**D**	**Y**
0	**0**	**x**	**x**	**0**
x	**1**	**0**	**x**	**1**
x	**1**	**1**	**0**	**1**
x	**1**	**1**	**1**	**0**
1	**x**	**0**	**x**	**1**
1	**x**	**1**	**0**	**1**
1	**x**	**1**	**1**	**0**

More details refer to doc/DATASHEET/*

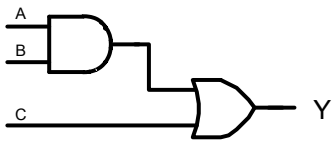
AOR21

Cell Description

The AOR21 cell provides the logical OR of one AND group of two inputs (A0, A1) and an additional inputs (B0).The output (Y) is represented by the logic equation:

$$Y = ((A\&B)|C)$$

Logic Symbol



Truth Table

INPUT			OUTPUT
A	B	C	Y
0	x	0	0
x	x	1	1
1	0	0	0
1	1	x	1

More details refer to doc/DATASHEET/*

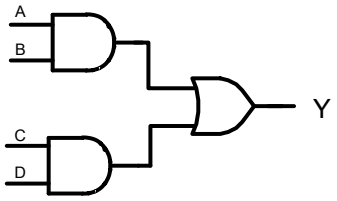
AOR22

Cell Description

The AOR22 cell provides the logical OR of two AND group of two inputs. The output (Y) is represented by the logic equation:

$$Y= ((A\&B)|(C\&D))$$

Logic Symbol



Truth Table

INPUT				OUTPUT
A	B	C	D	Y
0	x	0	x	0
0	x	1	0	0
x	x	1	1	1
1	0	0	x	0
1	0	1	0	0
1	1	x	x	1

More details refer to doc/DATASHEET/*

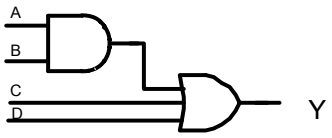
AOR211

Cell Description

The AOR211 cell provides the logical OR of one AND group of two inputs（A0,A1）and two addition inputs(B0 C0) .The output (Y) is represented by the logic equation:

Y = (D|C|(A&B))

Logic Symbol



Truth Table

INPUT				OUTPUT
A	B	C	D	Y
0	x	0	0	0
0	x	x	1	1
x	x	1	x	1
1	0	0	0	0
1	0	x	1	1
1	1	x	x	1

More details refer to doc/DATASHEET/*

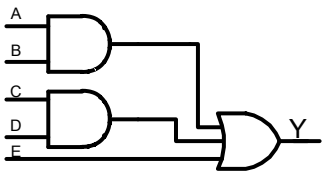
AOR221

Cell Description

The AOR221 cell provides the logical OR of two AND group of two inputs and an addition input .The output (Y) is represented by the logic equation:

$$Y = ((A\&B)|(C\&D)|E)$$

Logic Symbol



Truth Table

INPUT					OUTPUT
A	B	C	D	E	Y
0	x	0	x	0	0
0	x	x	x	1	1
0	x	1	0	0	0
x	x	1	1	x	1
1	0	0	x	0	0
1	0	x	x	1	1
1	0	1	0	0	0
1	1	x	x	x	1

More details refer to doc/DATASHEET/*

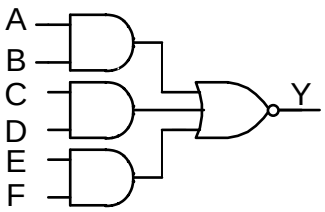
AOR222

Cell Description

The AOR221 cell provides the logical OR of two AND group of two inputs and an addition input .The output (Y) is represented by the logic equation:

Y =! ((A&B)|(C&D)|(E&F))

Logic Symbol



Truth Table

INPUT						OUTPUT
A	B	C	D	E	F	Y
0	x	0	x	0	x	0
0	x	0	x	1	0	0
0	x	x	x	1	1	1
0	x	1	0	0	x	0
0	x	1	0	1	0	0
x	x	1	1	x	x	1
1	0	0	x	0	x	0
1	0	0	x	1	0	0
1	0	x	x	1	1	1
1	0	1	0	0	x	0
1	0	1	0	1	0	0
1	1	x	x	x	x	1

More details refer to doc/DATASHEET/*

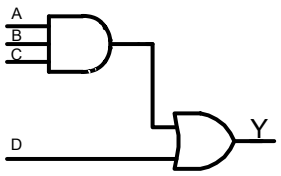
AOR31

Cell Description

The AOR31 cell provides the logical OR of one AND group of three inputs and an addition input .The output (Y) is represented by the logic equation:

$$Y = ((A\&B\&C)D)$$

Logic Symbol



Truth Table

INPUT				OUTPUT
A	B	C	D	Y
0	x	x	0	0
x	x	x	1	1
1	0	x	0	0
1	1	0	0	0
1	1	1	x	1

More details refer to doc/DATASHEET/*

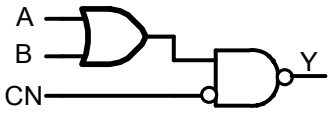
OAI21M

Cell Description

The OAI21Mcell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = (!((!CN)\&(A|B)))$$

Logic Symbol



Truth Table

INPUT			OUTPUT
A	B	CN	Y
0	0	x	1
x	1	0	0
x	1	1	1
1	x	0	0
1	x	1	1

More details refer to doc/DATASHEET/*

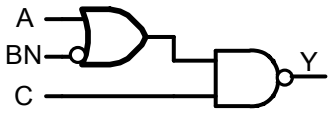
OAI2M1

Cell Description

The OAI2M1 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = (!(C\&(A|(!BN))))$$

Logic Symbol



Truth Table

INPUT			OUTPUT
A	BN	C	Y
x	x	0	1
x	0	1	0
0	1	1	1
1	1	1	0

More details refer to doc/DATASHEET/*

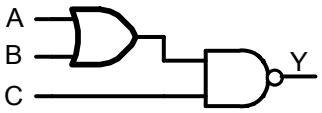
OAI21

Cell Description

The OAI21 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = (!(C\&(A|B)))$$

Logic Symbol



Truth Table

INPUT			OUTPUT
A	B	C	Y
0	0	x	1
x	1	0	1
x	1	1	0
1	x	0	1
1	x	1	0

More details refer to doc/DATASHEET/*

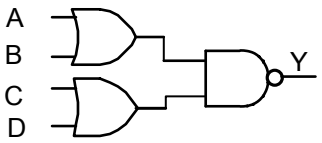
OAI22

Cell Description

The OAI21 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

$$Y = (!((C|D)\&(A|B)))$$

Logic Symbol



Truth Table

INPUT				OUTPUT
A	B	C	D	Y
0	0	x	x	1
x	1	0	0	1
x	1	x	1	0
x	1	1	x	0
1	x	0	0	1
1	x	x	1	0
1	x	1	x	0

More details refer to doc/DATASHEET/*

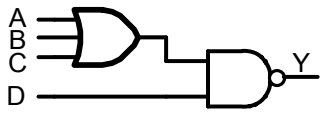
OAI31

Cell Description

The OAI31 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

$$Y = (!(D\&(A|B|C)))$$

Logic Symbol



Truth Table

INPUT				OUTPUT
A	B	C	D	Y
0	0	0	x	1
0	x	1	0	1
0	x	1	1	0
x	1	x	0	1
x	1	x	1	0
1	x	x	0	1
1	x	x	1	0

More details refer to doc/DATASHEET/*

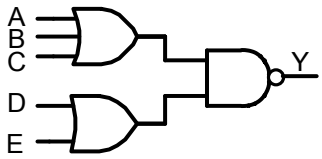
OAI32

Cell Description

The OAI32 cell provides the logical inverted AND of twoORgroups. The output (Y) is represented by the logic equation:

$$Y = (!((D|E)\&(A|B|C)))$$

Logic Symbol



Truth Table

INPUT					OUTPUT
A	B	C	D	E	Y
0	0	0	x	x	1
0	x	1	0	0	1
0	x	1	x	1	0
0	x	1	1	x	0
x	1	x	0	0	1
x	1	x	x	1	0
x	1	x	1	x	0
1	x	x	0	0	1
1	x	x	x	1	0
1	x	x	1	x	0

More details refer to doc/DATASHEET/*

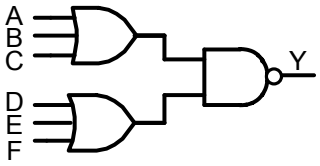
OAI33

Cell Description

The OAI33 cell provides the logical inverted AND of twoORgroups. The output (Y) is represented by the logic equation

Y = (!((A&B&C)|(D&E&F)))

Logic Symbol



Truth Table

INPUT						OUTPUT
A	B	C	D	E	F	Y
0	0	0	x	x	x	1
0	x	1	0	0	0	1
0	x	1	0	x	1	0
0	x	1	x	1	x	0
0	x	1	1	x	x	0
x	1	x	0	0	0	1
x	1	x	0	x	1	0
x	1	x	x	1	x	0
x	1	x	1	x	x	0
1	x	x	0	0	0	1
1	x	x	0	x	1	0
1	x	x	x	1	x	0
1	x	x	1	x	x	0

More details refer to doc/DATASHEET/*

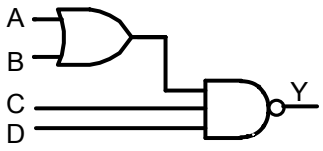
OAI211

Cell description

The OAI211 cell provides the logical inverted OR of one OR group and two additional inputs. The output (Y) is represented by the logic equation:

$$Y = (!(D|C|(A\&B)))$$

Logic Symbol



Truth Table

INPUT				OUTPUT
A	B	C	D	Y
0	0	x	x	1
x	1	0	x	1
x	1	1	0	1
x	1	1	1	0
1	x	0	x	1
1	x	1	0	1
1	x	1	1	0

More details refer to doc/DATASHEET/*

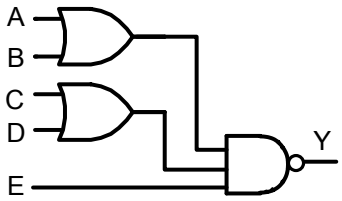
OAI221

Cell Description

The OAI221 cell provides the logical inverted AND of twoORgroups and an additional input. The output (Y) is represented by the logic equation:

Y = (!(E&(B|A)&(C|D)))

Logic Symbol



Truth Table

INPUT					OUTPUT
A	B	C	D	E	Y
0	0	x	x	x	1
x	1	0	0	x	1
x	1	x	1	0	1
x	1	x	1	1	0
x	1	1	x	0	1
x	1	1	x	1	0
1	x	0	0	x	1
1	x	x	1	0	1
1	x	x	1	1	0
1	x	1	x	0	1
1	x	1	x	1	0

More details refer to doc/DATASHEET/*

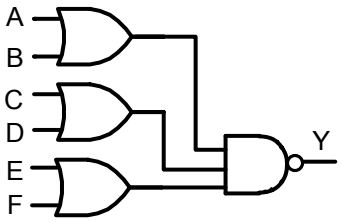
OAI222

Cell Description

The OAI222 cell provides the logical inverted AND of three OR groups. The output (Y) is represented by the logic equation:

Y = !((F|E)&(A|B)&(C|D))

Logic Symbol



Truth Table

INPUT						OUTPUT
A	B	C	D	E	F	Y
0	0	x	x	x	x	1
x	1	0	0	x	x	1
x	1	x	1	0	0	1
x	1	x	1	x	1	0
x	1	x	1	1	x	0
x	1	1	x	0	0	1
x	1	1	x	x	1	0
x	1	1	x	1	x	0
1	x	0	0	x	x	1
1	x	x	1	0	0	1
1	x	x	1	x	1	0
1	x	x	1	1	x	0
1	x	1	x	0	0	1
1	x	1	x	x	1	0
1	x	1	x	1	x	0

More details refer to doc/DATASHEET/*

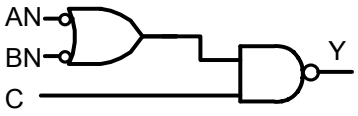
OAIM21

Cell Description

The OAIM21 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N, A1N) and an additional non-inverted input (B0).The output (Y) is represented by the logic equation:

Y = ((!C)|(AN&BN))

Logic Symbol



Truth Table

INPUT			OUTPUT
AN	BN	C	Y
x	x	0	1
0	x	1	0
1	0	1	0
1	1	1	1

More details refer to doc/DATASHEET/*

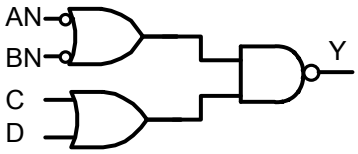
OAIM22

Cell Description

The OAIM22 cell provides the logical inverted AND of one OR group of two inverted inputs (AN,BN) and two additional non-inverted input (C , D).The output (Y) is represented by the logic equation:

Y=(!D)&(!C)|(AN&BN)

Logic Symbol



Truth Table

INPUT				OUTPUT
AN	BN	C	D	Y
x	x	0	0	1
0	x	x	1	0
0	x	1	x	0
1	0	x	1	0
1	0	1	x	0
1	1	x	1	1
1	1	1	x	1

More details refer to doc/DATASHEET/*

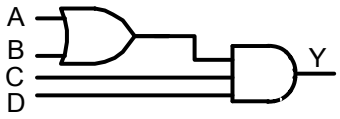
ORA211

Cell Description

The ORA211 cell provides the logical AND of one OR group of two inputs（A,B）and two addition inputs(C, D) .The output (Y) is represented by the logic equation

$$Y = (D\&C\&(A|B))$$

Logic Symbol



Truth Table

INPUT				OUTPUT
A	B	C	D	Y
0	0	x	x	0
x	1	0	x	0
x	1	1	0	0
x	1	1	1	1
1	x	0	x	0
1	x	1	0	0
1	x	1	1	1

More details refer to doc/DATASHEET/*

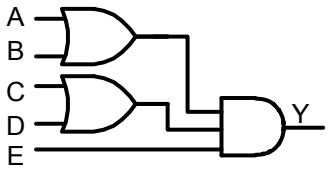
ORA221

Cell Description

The ORA221 cell provides the logical AND of two OR groups and an additional inputs (D).The output (Y) is represented by the logic equation:

$$Y = (E\&(A|B)\&(C|D)))$$

Logic Symbol



Truth Table

INPUT					OUTPUT
A	B	C	D	E	Y
0	0	x	x	x	0
x	1	0	0	x	0
x	1	x	1	0	0
x	1	x	1	1	1
x	1	1	x	0	0
x	1	1	x	1	1
1	x	0	0	x	0
1	x	x	1	0	0
1	x	x	1	1	1
1	x	1	x	0	0
1	x	1	x	1	1

More details refer to doc/DATASHEET/*

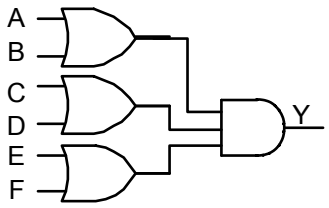
ORA222

Cell Description

The ORA222 cell provides the logical AND of two OR groups and an additional inputs (D).The output (Y) is represented by the logic equation:

$$Y = ((E|F)\&(A|B)\&(C|D))$$

Logic Symbol



Truth Table

INPUT						OUTPUT
A	**B**	**C**	**D**	**E**	**F**	**Y**
0	0	x	x	x	x	0
x	1	0	0	x	x	0
x	1	x	1	0	0	0
x	1	x	1	x	1	1
x	1	x	1	1	x	1
x	1	1	x	0	0	0
x	1	1	x	x	1	1
x	1	1	x	1	x	1
1	x	0	0	x	x	0
1	x	x	1	0	0	0
1	x	x	1	x	1	1
1	x	x	1	1	x	1
1	x	1	x	0	0	0
1	x	1	x	x	1	1
1	x	1	x	1	x	1

More details refer to doc/DATASHEET/*

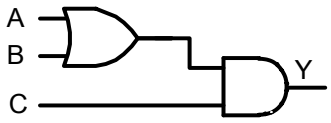
ORA21

Cell Description

The ORA21 cell provides the logical AND of one OR group of two inputs (A, B) and an additional inputs (C).The output (Y) is represented by the logic equation:

$$Y = (C\&(A|B))$$

Logic Symbol



Truth Table

INPUT			OUTPUT
A	B	C	Y
0	0	x	0
x	1	0	0
x	1	1	1
1	x	0	0
1	x	1	1

More details refer to doc/DATASHEET/*

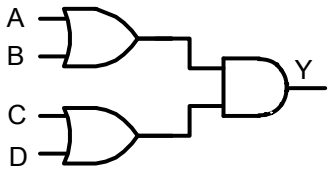
ORA22

Cell Description

The ORA22 cell provides the logical AND of two OR groups.The output (Y) is represented by the logic equation

$$Y = ((A|B)\&(C|D))$$

Logic Symbol



Truth Table

INPUT				OUTPUT
A	**B**	**C**	**D**	**Y**
0	**0**	**x**	**x**	**0**
x	**1**	**0**	**0**	**0**
x	**1**	**x**	**1**	**1**
x	**1**	**1**	**x**	**1**
1	**x**	**0**	**0**	**0**
1	**x**	**x**	**1**	**1**
1	**x**	**1**	**x**	**1**

More details refer to doc/DATASHEET/*

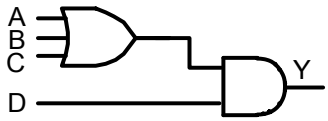
ORA31

Cell Description

The ORA31 cell provides the logical AND of one OR group of three inputs（A,B,C）and an addition inputs(D) .The output (Y) is represented by the logic equation

$$Y = (D\&(A|B|C))$$

Logic Symbol



Truth Table

INPUT				OUTPUT
A	B	C	D	Y
0	0	0	x	0
0	x	1	0	0
0	x	1	1	1
x	1	x	0	0
x	1	x	1	1
1	x	x	0	0
1	x	x	1	1

More details refer to doc/DATASHEET/*

Gates

AN02

Cell Description

TheAN02cell provides the logical AND of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = A \,\&\, B$$

Logic Symbol

Truth Table

INPUT		OUTPUT
A	B	Y
0	x	0
1	0	0
1	1	1

More details refer to doc/DATASHEET/*

AN03

Cell Description

The AN03 cell provides the logical AND of three inputs (A, B, C). The output (Y) is represented by the logic equation:

Y =(C&B&A)

Logic Symbol

Truth Table

INPUT			OUTPUT
A	B	C	Y
0	x	x	0
1	0	x	0
1	1	0	0
1	1	1	1

More details refer to doc/DATASHEET/*

AN04

Cell Description

The AN04cell provides the logical AND of four inputs (A, B, C, D).The output (Y) is represented by the logic equation:

Y = (D&C&B&A)

Logic Symbol

Truth Table

INPUT				OUTPUT
A	B	C	D	Y
0	x	x	x	0
1	0	x	x	0
1	1	0	x	0
1	1	1	0	0
1	1	1	1	1

More details refer to doc/DATASHEET/*

CKAND

Cell Description

The CKAND cell provides the logical AND of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = A \,\&\, B$$

Logic Symbol

Truth Table

INPUT		OUTPUT
A	B	Y
0	x	0
1	0	0
1	1	1

More details refer to doc/DATASHEET/*

CKOR02

Cell Description

The CKOR2 cell provides the logical OR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (B|A)$$

Logic Symbol

Truth Table

INPUT		OUTPUT
A	B	Y
0	0	0
x	1	1
1	x	1

More details refer to doc/DATASHEET/*

CKND02

Cell Description

The ND02 cell provides the logical NAND of two inputs (A, B). The output (Y) is represented by the logic equation:

Y = (!(B&A))

Logic Symbol

Truth Table

INPUT		OUTPUT
A	B	Y
0	x	0
1	0	1
1	1	0

More details refer to doc/DATASHEET/*

CKNR02

Cell Description

The CKNR02 cell provides a logical NOR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (!(B|A))$$

Logic Symbol

Truth Table

INPUT		OUTPUT
A	B	Y
0	0	1
x	1	1
1	x	0

More details refer to doc/DATASHEET/*

CKXN02

Cell Description

The CKXN02 cell provides a logical EXCLUSIVE NOR of two inputs (A, B). The output (Y) is represented by the logic equation:

Y = (!(B^A))

Logic Symbol

Truth Table

INPUT		OUTPUT
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

More details refer to doc/DATASHEET/*

CKXR02

Cell Description

The CKXR02 cell provides a logical EXCLUSIVE OR of two inputs (A, B) with balanced delays for clock signals. The output (Y) is represented by the logic equation:

$$Y = (B \hat{} A)$$

Logic Symbol

Truth Table

INPUT		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

More details refer to doc/DATASHEET/*

ND02

Cell Description

The ND02 cell provides the logical NAND of two inputs (A, B). The output (Y) is represented by the logic equation:

Y = (!(B&A))

Logic Symbol

Truth Table

INPUT		OUTPUT
A	B	Y
0	x	1
1	0	1
1	1	0

More details refer to doc/DATASHEET/*

ND03

Cell Description

The ND03 cell provides the logical NAND of three inputs (A, B, C). The output (Y) is represented by the logic equation:

Y = (!(C&B&A))

Logic Symbol

Truth Table

INPUT			OUTPUT
A	B	C	Y
0	x	x	1
1	0	x	1
1	1	0	1
1	1	1	0

More details refer to doc/DATASHEET/*

ND04

Cell Description

The ND04 cell provides a logical NAND of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

Y = (!(D&C&B&A))

Logic Symbol

Truth Table

INPUT				OUTPUT
A	B	C	D	Y
0	x	x	x	1
1	0	x	x	1
1	1	0	x	1
1	1	1	0	1
1	1	1	1	0

More details refer to doc/DATASHEET/*

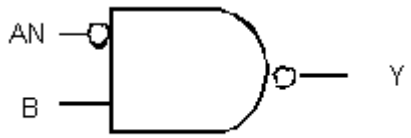
ND12

Cell Description

The ND12 cell provides the logical NAND of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

Y = ((!B)|AN)

Logic Symbol



Truth Table

INPUT		OUTPUT
AN	B	Y
x	0	1
0	1	0
1	1	1

More details refer to doc/DATASHEET/*

ND13

Cell Description

The ND13 cell provides the logical NAND of one inverted input (AN) and two non-inverted inputs (B,C). The output (Y) is represented by the logic equation:

Y = ((!C)|(!B)|AN)

Logic Symbol

Truth Table

INPUT			OUTPUT
AN	B	C	Y
x	0	x	1
x	1	0	1
0	1	1	0
1	1	1	1

More details refer to doc/DATASHEET/*

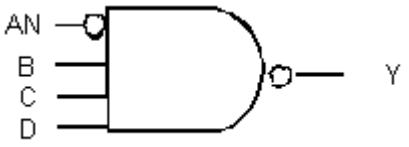
ND14

Cell Description

The ND14 cell provides a logical NAND of one inverted input (AN) and three non-inverted inputs (B,C, D). The output (Y) is represented by the logic equation:

Y =((!D)|(!C)|(!B)|AN)

Logic Symbol



Truth Table

INPUT				OUTPUT
AN	**B**	**C**	**D**	**Y**
x	**0**	**x**	**x**	**1**
x	**1**	**0**	**x**	**1**
x	**1**	**1**	**0**	**1**
0	**1**	**1**	**1**	**0**
1	**1**	**1**	**1**	**1**

More details refer to doc/DATASHEET/*

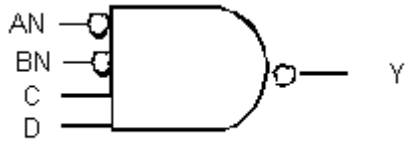
ND24

Cell Description

The ND24 cell provides a logical NAND of two inverted input (AN , BN) and two non-inverted inputs (C, D). The output (Y) is represented by the logic equation:

Y = ((!D)|(!C)|BN|AN)

Logic Symbol



Truth Table

INPUT				OUTPUT
AN	**BN**	**C**	**D**	**Y**
0	**x**	**0**	**x**	**1**
0	**x**	**1**	**0**	**1**
0	**0**	**1**	**1**	**0**
x	**1**	**1**	**1**	**1**
1	**x**	**x**	**x**	**1**

More details refer to doc/DATASHEET/*

NR02

Cell Description

The NR02 cell provides a logical NOR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (!(B|A))$$

Logic Symbol

Truth Table

INPUT		OUTPUT
A	B	Y
0	0	1
x	1	0
1	x	0

More details refer to doc/DATASHEET/*

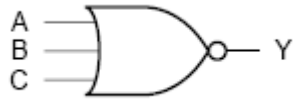
NR03

Cell Description

The NR03 cell provides a logical NOR of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = (!(C|B|A))$$

Logic Symbol



Truth Table

INPUT			OUTPUT
A	B	C	Y
0	0	0	1
0	x	1	0
x	1	x	0
1	x	x	0

More details refer to doc/DATASHEET/*

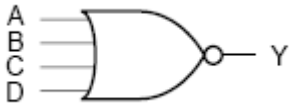
NR04

Cell Description

The NR04 cell provides a logical NOR of four inputs (A, B, C, D).The output (Y) is represented by the logic equation:

Y = (!(D&C&B&A))

Logic Symbol



Truth Table

INPUT				OUTPUT
A	B	C	D	Y
0	0	0	0	1
0	0	x	1	0
0	x	1	x	0
x	1	x	x	0
1	x	x	x	0

More details refer to doc/DATASHEET/*

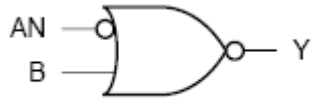
NR12

Cell Description

The NR12 cell provides a logical NOR of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

Y = ((!B)&AN)

Logic Symbol



Truth Table

INPUT		OUTPUT
AN	B	Y
0	x	0
1	0	1
1	1	0

More details refer to doc/DATASHEET/*

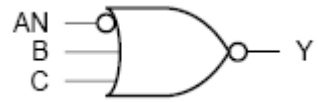
NR13

Cell Description

The NR13 cell provides a logical NOR of one inverted input (AN) and two non-inverted inputs (B, C). The output (Y) is represented by the logic equation:

Y = ((!C)&(!B)&AN)

Logic Symbol



Truth Table

INPUT			OUTPUT
AN	B	C	Y
0	x	x	0
1	0	0	1
1	x	1	0
1	1	x	0

More details refer to doc/DATASHEET/*

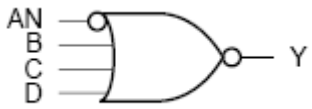
NR14

Cell Description

The NR14 cell provides a logical NOR of one inverted input (AN) and three non-inverted inputs (B, C, D). The output (Y) is represented by the logic equation:

Y = ((!D)&(!C)&(!B)&AN)

Logic Symbol



Truth Table

INPUT				OUTPUT
AN	B	C	D	Y
0	x	x	x	0
1	0	0	0	1
1	0	x	1	0
1	x	1	x	0
1	1	x	x	0

More details refer to doc/DATASHEET/*

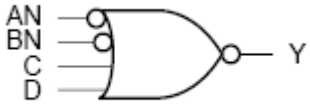
NR24

Cell Description

The NR24 cell provides a logical NOR of two inverted inputs (AN,BN)and two non-inverted inputs (C, D). The output (Y) is represented by the logic equation:

Y = ((!D)&(!C)&BN&AN)

Logic Symbol



Truth Table

INPUT				OUTPUT
AN	BN	C	D	Y
0	x	x	x	0
1	0	x	x	0
1	1	0	0	1
1	1	x	1	0
1	1	1	x	0

More details refer to doc/DATASHEET/*

OR02

Cell Description

The OR2 cell provides the logical OR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (B|A)$$

Logic Symbol

Truth Table

INPUT		OUTPUT
A	B	Y
0	0	0
x	1	1
1	x	1

More details refer to doc/DATASHEET/*

OR03

Cell Description

The OR3 cell provides the logical OR of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = (C|B|A)$$

Logic Symbol

Truth Table

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	x	1	1
x	1	x	1
1	x	x	1

More details refer to doc/DATASHEET/*

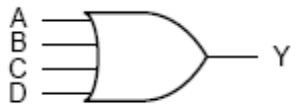
OR04

Cell Description

The OR4 cell provides the logical OR of four inputs (A, B, C, D).The output (Y) is represented by the logic equation:

$$Y = (D|C|B|A)$$

Logic Symbol



Truth Table

INPUT				OUTPUT
A	B	C	D	Y
0	0	0	0	0
0	0	x	1	1
0	x	1	x	1
x	1	x	x	1
1	x	x	x	1

More details refer to doc/DATASHEET/*

XN02

Cell Description

The XN02 cell provides a logical EXCLUSIVE NOR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (!(B \hat{} A))$$

Logic Symbol

Truth Table

INPUT		OUTPUT
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

More details refer to doc/DATASHEET/*

XN03

Cell Description

The XN03 cell provides a logical EXCLUSIVE NOR of three inputs (A, B, C). The output (Y) is represented by the logic equation:

Y = (!(C^B^A))

Logic Symbol

Truth Table

INPUT			OUTPUT
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

More details refer to doc/DATASHEET/*

XR02

Cell Description

The XR02 cell provides a logical EXCLUSIVE OR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (B \hat{} A)$$

Logic Symbol

Truth Table

INPUT		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

More details refer to doc/DATASHEET/*

XR03

Cell Description

The XR03 cell provides a logical EXCLUSIVE OR of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = (C \hat{} B \hat{} A)$$

Logic Symbol

Truth Table

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

More details refer to doc/DATASHEET/*

MULTIPLEXERS

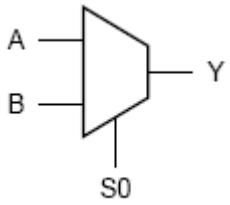
CKMX02

Cell Description

The MX02 cell is a 2-to-1 multiplexer with balanced delays for clock signals. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y).The output (Y) is represented by the logic equation:

Y = ((A&(!S0))|(B&S0))

Logic Symbol



Truth Table

INPUT			OUTPUT
A	B	S0	Y
0	0	x	0
0	1	0	0
x	1	1	1
1	x	0	1
1	0	1	0

More details refer to doc/DATASHEET/*

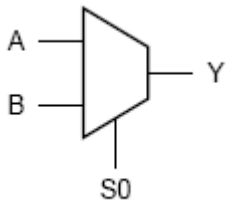
MX02

Cell Description

The MX02 cell is a 2-to-1 multiplexer. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y).The output (Y) is represented by the logic equation:

Y = ((A&(!S0))|(B&S0))

Logic Symbol



Truth Table

INPUT			OUTPUT
A	B	S0	Y
0	0	x	0
0	1	0	0
x	1	1	1
1	x	0	1
1	0	1	0

More details refer to doc/DATASHEET/*

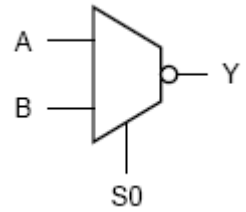
MI02

Cell Description

The MI02 cell is a 2-to-1 multiplexer with inverted output. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y). The output (Y) is represented by the logic equation:

Y =(!((A&(!S0))|(B&S0)))

Logic Symbol



Truth Table

INPUT			OUTPUT
A	B	S0	Y
0	0	x	1
0	1	0	1
x	1	1	0
1	x	0	0
1	0	1	1

More details refer to doc/DATASHEET/*

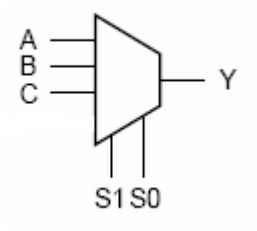
MX03

Cell Description

The MX03 cell is a 3-to-1 multiplexer. The state of the select inputs (S1, S0) determines which data input (A, B, C) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y= ((S1\&C)|((!S1)\&((S0\&B)|((!S0)\&A))))$$

Logic Symbol



Truth Table

INPUT					OUTPUT
A	B	C	S0	S1	Y
0	0	0	x	x	0
0	0	1	x	0	0
0	x	1	x	1	1
0	1	0	0	x	0
0	1	x	1	0	1
x	1	0	1	1	0
0	1	1	0	0	0
1	0	x	0	0	1
1	x	0	x	1	0
1	0	0	1	x	0
1	0	1	x	1	1
1	0	1	1	0	0
1	1	0	x	0	1
1	1	1	x	x	1

More details refer to doc/DATASHEET/*

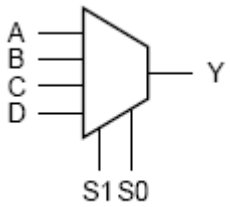
MX04

Cell Description

The MX04 cell is a 4-to-1 multiplexer. The state of the select inputs (S1, S0) determines which data input (A, B, C, D) is presented to the output (Y). The output (Y) is represented by the logic equation:

Y = ((A&(!S1)&(!S0))|(B&(!S1)&S0)|(D&S1&S0)|(C&S1&(!S0)))

Logic Symbol



Truth Table

INPUT						OUTPUT
A	B	C	D	S0	S1	Y
0	0	0	0	x	x	0
0	x	0	1	0	x	0
x	0	x	1	1	0	0
x	x	x	1	1	1	1
0	0	1	x	x	0	0
0	x	1	x	0	1	1
0	x	1	0	1	1	0
0	1	0	x	0	x	0
0	1	x	x	1	0	1
0	1	x	0	1	1	0
0	1	1	x	0	0	0
1	0	0	x	0	0	1
1	x	0	0	x	1	0
1	0	x	0	1	x	0
1	x	0	1	0	1	0
1	x	1	x	0	x	1
1	1	0	x	x	0	1
1	1	1	x	1	0	1
1	1	1	0	1	1	0

More details refer to doc/DATASHEET/*

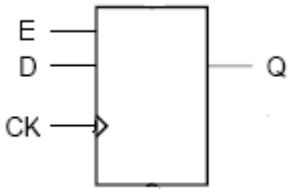
FLIP-FLOPS

DENRQ

Cell Description

The DENRQ cell is a positive-edge triggered, active-high enable (E), with a single output Q, static D-type flip-flop.

Logic Symbol



Truth Table

INPUT			OUTPUT
D	E	CK	Q
x	0	R	IQ
0	1	R	0
1	1	R	1
x	x	x	IQ

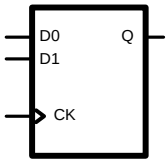
More details refer to doc/DATASHEET/*

DFANRQ

Cell Description

The DFANRQ cell is a positive-edge triggered, static NAND2 D-type D0,D2 flip-flop.

Logic Symbol



Truth Table

INPUT			OUTPUT
D0	D1	CK	Q
0	x	R	0
1	0	R	0
1	1	R	1
x	x	x	IQ

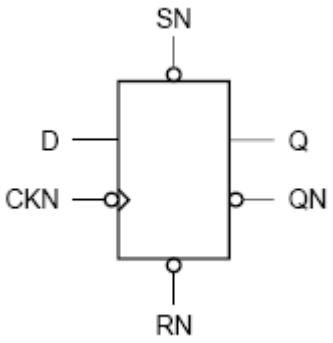
More details refer to doc/DATASHEET/*

DFBFB

Cell Description

The DFBFB cell is a negative-edge triggered, asynchronous active-low reset (RN) and set (SN), static D-type flip-flop.

Logic Symbol



Truth Table

INPUT				OUTPUT	
D	RN	SN	CKN	Q	QN
0	1	1	F	0	1
1	1	1	F	1	0
x	x	0	x	1	0
x	0	1	x	0	1
x	1	1	x	IQ	IQN

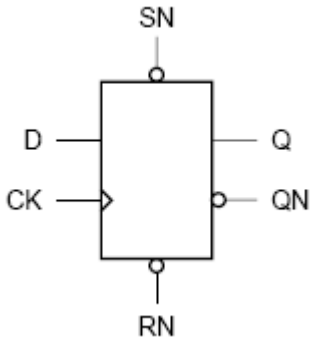
More details refer to doc/DATASHEET/*

DFBRB

Cell Description

The DFBRB cell is a positive-edge triggered, asynchronous active-low reset (RN) and set (SN), static D-type flip-flop.

Logic Symbol



Truth Table

INPUT				OUTPUT	
D	RN	SN	CK	Q	QN
0	1	1	R	0	1
1	1	1	R	1	0
x	x	0	x	1	0
x	0	1	x	0	1
x	1	1	x	IQ	IQN

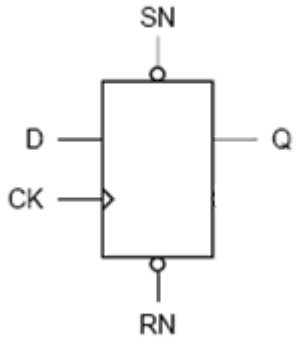
More details refer to doc/DATASHEET/*

DFBRQ

Cell Description

The DFBRQ cell is a positive-edge triggered, asynchronous active-low reset (RN) and set (SN), static D-type flip-flop.

Logic Symbol



Truth Table

INPUT				OUTPUT
D	RN	SN	CK	Q
0	1	1	R	0
1	1	1	R	1
x	x	0	x	1
x	0	1	x	0
x	1	1	x	IQ

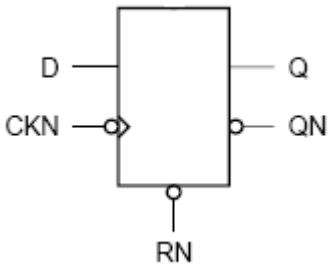
More details refer to doc/DATASHEET/*

DFCFB

Cell Description

The DFCFB cell is a negative-edge triggered, asynchronous active-low reset (RN) and, static D-type flip-flop.

Logic Symbol



Truth Table

INPUT			OUTPUT	
D	RN	CKN	Q	QN
0	1	F	0	1
1	1	F	1	0
x	0	x	0	1
x	1	x	IQ	IQN

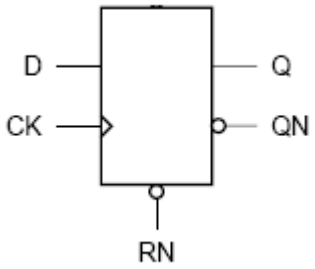
More details refer to doc/DATASHEET/*

DFCRB

Cell Description

The DFCRB cell is a positive-edge triggered, asynchronous active-low reset (RN), static D-type flip-flop.

Logic Symbol



Truth Table

INPUT			OUTPUT	
D	RN	CK	Q	QN
0	1	R	0	1
1	1	R	1	0
x	0	x	0	1
x	1	x	IQ	IQN

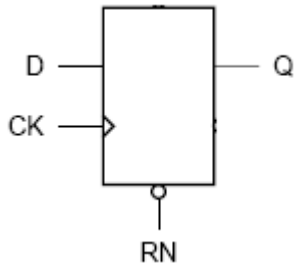
More details refer to doc/DATASHEET/*

DFCRQ

Cell Description

The DFCRQ cell is a positive-edge triggered, asynchronous active-low reset (RN) with a single output Q, static D-type flip-flop.

Logic Symbol



Truth Table

INPUT			OUTPUT
D	RN	CK	Q
0	1	R	0
1	1	R	1
x	0	x	0
x	1	x	IQ

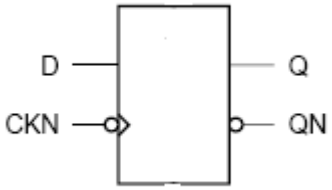
More details refer to doc/DATASHEET/*

DFNFB

Cell Description

The DFNFB cell is a negative-edge triggered, static D-type flip-flop.

Logic Symbol



Truth Table

INPUT		OUTPUT	
D	CKN	Q	QN
0	F	0	1
1	F	1	0
x	x	IQ	IQN

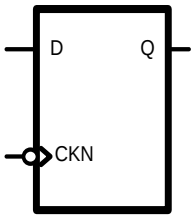
More details refer to doc/DATASHEET/*

DFNFQ

Cell Description

The DFNFB cell is a negative-edge triggered, static D-type flip-flop,with output Q only.

Logic Symbol



Truth Table

INPUT		OUTPUT
D	CKN	Q
0	F	0
1	F	1
x	x	IQ

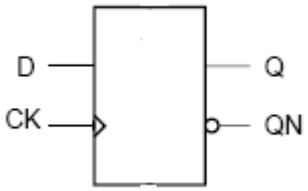
More details refer to doc/DATASHEET/*

DFNRB

Cell Description

The DFNRB cell is a positive-edge triggered, static D-type flip-flop.

Logic Symbol



Truth Table

INPUT		OUTPUT	
D	CK	Q	QN
0	R	0	1
1	R	1	0
x	x	IQ	IQN

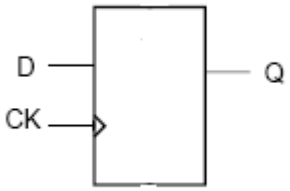
More details refer to doc/DATASHEET/*

DFNRQ

Cell Description

The DFNRQ cell is a positive-edge triggered, with a single output Q, static D-type flip-flop.

Logic Symbol



Truth Table

INPUT		OUTPUT
D	CK	Q
0	R	0
1	R	1
x	x	IQ

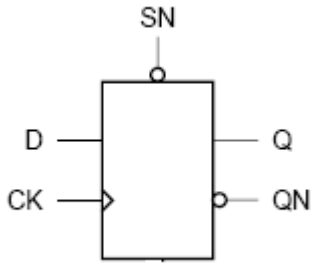
More details refer to doc/DATASHEET/*

DFPRB

Cell Description

The DFPRB cell is a positive-edge triggered, asynchronous active-low set (SN) static D-type flip-flop.

Logic Symbol



Truth Table

INPUT			OUTPUT	
D	SN	CK	Q	QN
0	1	R	0	1
1	1	R	1	0
x	0	x	1	0
x	1	x	IQ	IQN

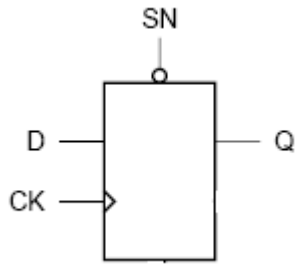
More details refer to doc/DATASHEET/*

DFPRQ

Cell Description

The DFPRQ cell is a positive-edge triggered, asynchronous active-low set (SN) with a single output Q, static D-type flip-flop.

Logic Symbol



Truth Table

INPUT			OUTPUT
D	SN	CK	Q
0	1	R	0
1	1	R	1
x	0	x	1
x	1	x	IQ

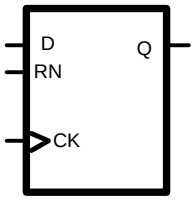
More details refer to doc/DATASHEET/*

DFSCRQ

Cell Description

The DFSCRB cell is a positive-edge triggered, synchronous active-low reset (RN), static D-type flip-flop,only with output Q .

Logic Symbol



Truth Table

INPUT			OUTPUT
D	RN	CK	Q
0	x	R	0
1	0	R	0
1	1	R	1
x	x	x	IQ

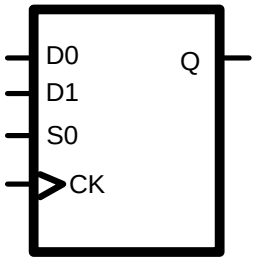
More details refer to doc/DATASHEET/*

DMNRQ

Cell Description

The DMNRQ cell is a positive-edge triggered, static D-type (D0,D1) controlled by S0 flip-flop,only with output Q .

Logic Symbol



Truth Table

INPUT				OUTPUT
D0	D1	S0	CK	Q
0	0	x	R	0
0	1	0	R	0
x	1	1	R	1
1	x	0	R	1
1	0	1	R	0
x	x	x	x	IQ

More details refer to doc/DATASHEET/*

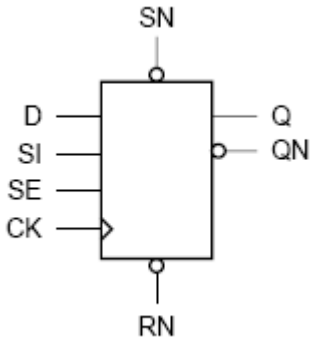
SCAN FLIP - FLOPS

SDANRQ

Cell Description

The SDANRQ cell is a positive-edge triggered, static D-type (NAND2 D0,D1)flip-flop with scan input (SI),

Logic Symbol



Truth Table

INPUT					OUTPUT
D0	D1	SE	SI	CK	Q
0	x	0	x	R	0
x	x	1	0	R	0
x	x	1	1	R	1
1	0	0	x	R	0
1	1	0	x	R	1
x	x	x	x	x	IQ

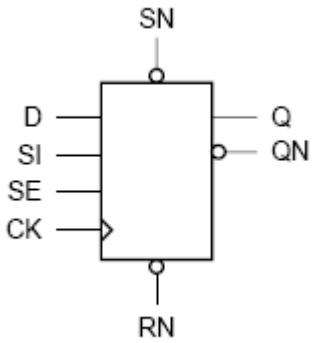
More details refer to doc/DATASHEET/*

SDBRB

Cell Description

The SDBRB cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN). Set (SN) dominates reset (RN).

Logic Symbol



Truth Table

INPUT						OUTPUT	
D	SE	SI	RN	SN	CK	Q	QN
0	0	x	1	1	R	0	1
x	1	0	1	1	R	0	1
x	1	1	1	1	R	1	0
1	0	x	1	1	R	1	0
x	x	x	x	0	x	1	0
x	x	x	0	1	x	0	1
x	x	x	1	1	x	IQ	IQN

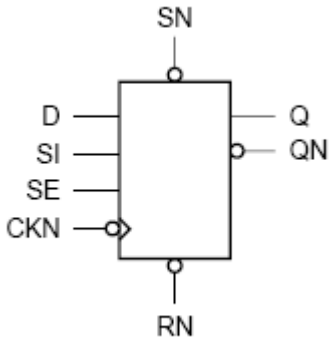
More details refer to doc/DATASHEET/*

SDBFB

Cell Description

The SDBFB cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN). Set (SN) dominates reset (RN).

Logic Symbol



Truth Table

INPUT						OUTPUT	
D	SE	SI	RN	SN	CKN	Q	QN
0	0	x	1	1	F	0	1
x	1	0	1	1	F	0	1
x	1	1	1	1	F	1	0
1	0	x	1	1	F	1	0
x	x	x	x	0	x	1	0
x	x	x	0	1	x	0	1
x	x	x	1	1	x	IQ	IQN

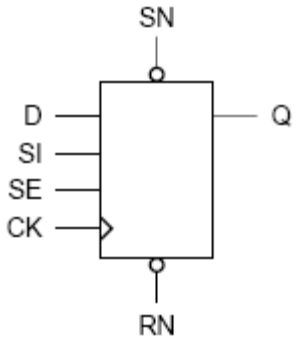
More details refer to doc/DATASHEET/*

SDBRQ

Cell Description

The SDBRQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN), and set dominating reset. The cell has a single output (Q)

Logic Symbol



Truth Table

INPUT						OUTPUT
D	SE	SI	RN	SN	CK	Q
0	0	x	1	1	R	0
x	1	0	1	1	R	0
x	1	1	1	1	R	1
1	0	x	1	1	R	1
x	x	x	x	0	x	1
x	x	x	0	1	x	0
x	x	x	1	1	x	IQ

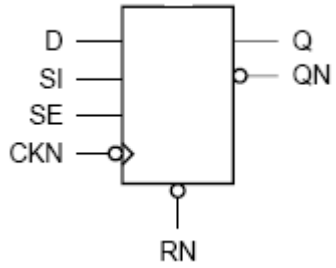
More details refer to doc/DATASHEET/*

SDCFB

Cell Description

The SDCFB cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN).

Logic Symbol



Truth Table

INPUT					OUTPUT	
D	SE	SI	RN	CKN	Q	QN
0	0	x	1	F	0	1
x	1	0	1	F	0	1
x	1	1	1	F	1	0
1	0	x	1	F	1	0
x	x	x	0	x	0	1
x	x	x	1	x	IQ	IQN

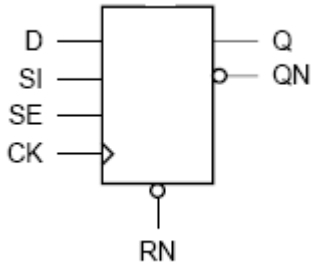
More details refer to doc/DATASHEET/*

SDCRB

Cell Description

The SDCRB cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN)

Logic Symbol



Truth Table

INPUT					OUTPUT	
D	SE	SI	RN	CK	Q	QN
0	0	x	1	R	0	1
x	1	0	1	R	0	1
x	1	1	1	R	1	0
1	0	x	1	R	1	0
x	x	x	0	x	0	1
x	x	x	1	x	IQ	IQN

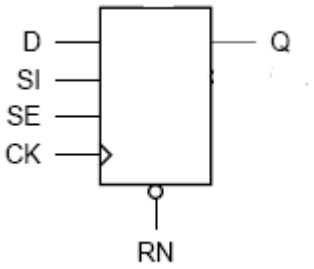
More details refer to doc/DATASHEET/*

SDCRQ

Cell Description

The SDCRQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) a single output (Q)

Logic Symbol



Truth Table

INPUT					OUTPUT
D	SE	SI	RN	CK	Q
0	0	x	1	R	0
x	1	0	1	R	0
x	1	1	1	R	1
1	0	x	1	R	1
x	x	x	0	x	0
x	x	x	1	x	IQ

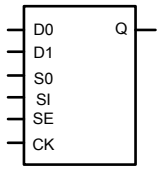
More details refer to doc/DATASHEET/*

SDMNRQ

Cell Description

The SDMNRQ cell is a Positive-edge triggered, static D-type (D0, D1)flip-flop, The state of the select input (S0) determines which data input (D0, D1),with scan input (SI),output Q only

Logic Symbol



Truth Table

INPUT						OUTPUT
D0	D1	S0	SE	SI	CK	Q
0	0	x	0	x	R	1
x	x	x	1	0	R	1
x	x	x	1	1	R	0
0	1	0	0	x	R	0
x	1	1	0	x	R	1
1	x	0	0	x	R	1
1	0	1	0	x	R	0
x	x	x	x	x	x	IQ

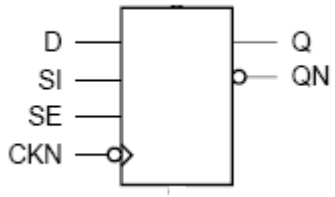
More details refer to doc/DATASHEET/*

SDNFB

Cell Description

The SDNFB cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE)

Logic Symbol



Truth Table

INPUT				OUTPUT	
D	SE	SI	CKN	Q	QN
0	0	x	F	0	1
x	1	0	F	0	1
x	1	1	F	1	0
1	0	x	F	1	0
x	x	x	x	IQ	IQN

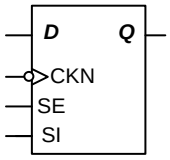
More details refer to doc/DATASHEET/*

SDNFQ

Cell Description

The SDNFB cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE),with only Q output pin

Logic Symbol



Truth Table

INPUT				OUTPUT
D	SE	SI	CKN	Q
0	0	x	F	0
x	1	0	F	0
x	1	1	F	1
1	0	x	F	1
x	x	x	x	IQ

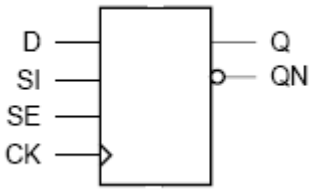
More details refer to doc/DATASHEET/*

SDNRB

Cell Description

The SDNRB cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE)

Logic Symbol



Truth Table

INPUT				OUTPUT	
D	SE	SI	CK	Q	QN
0	0	x	R	0	1
x	1	0	R	0	1
x	1	1	R	1	0
1	0	x	R	1	0
x	x	x	x	IQ	IQN

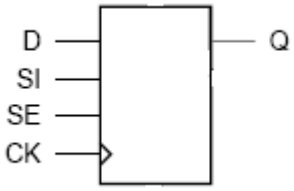
More details refer to doc/DATASHEET/*

SDNRQ

Cell Description

The SDNRQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), a single output (Q)

Logic Symbol



Truth Table

INPUT				OUTPUT
D	SE	SI	CK	Q
0	0	x	R	0
x	1	0	R	0
x	1	1	R	1
1	0	x	R	1
x	x	x	x	IQ

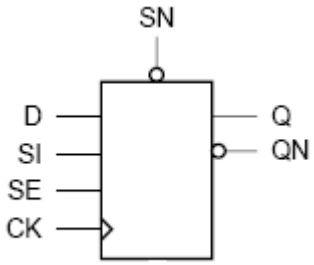
More details refer to doc/DATASHEET/*

SDPFB

Cell Description

The SDPFB cell is a Negtive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-high set (SN)

Logic Symbol



Truth Table

INPUT					OUTPUT	
D	SE	SI	SN	CKN	Q	QN
0	0	x	1	F	0	1
x	1	0	1	F	0	1
x	1	1	1	F	1	0
1	0	x	1	F	1	0
x	x	x	0	x	1	0
x	x	x	1	x	IQ	IQN

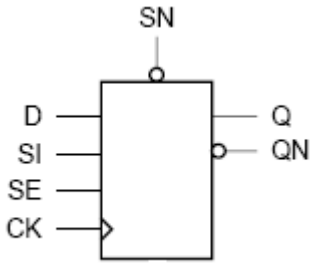
More details refer to doc/DATASHEET/*

SDPRB

Cell Description

The SDPRB cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-high set (SN)

Logic Symbol



Truth Table

INPUT					OUTPUT	
D	SE	SI	SN	CK	Q	QN
0	0	x	1	R	0	1
x	1	0	1	R	0	1
x	1	1	1	R	1	0
1	0	x	1	R	1	0
x	x	x	0	x	1	0
x	x	x	1	x	IQ	IQN

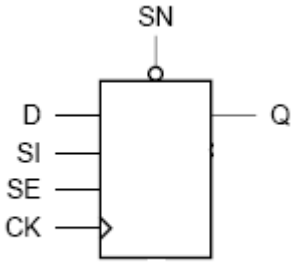
More details refer to doc/DATASHEET/*

SDPRQ

Cell Description

The SDPRQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN) a single output (Q)

Logic Symbol



Truth Table

INPUT					OUTPUT
D	SE	SI	SN	CK	Q
0	0	x	1	R	0
x	1	0	1	R	0
x	1	1	1	R	1
1	0	x	1	R	1
x	x	x	0	x	1
x	x	x	1	x	IQ

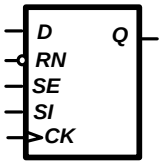
More details refer to doc/DATASHEET/*

SDSCRQ

Cell Description

The SDSCRQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), with output pin Q ,active-high scan enable (SE), and synchronous active-low reset (RN) ,with output pin Q only .

Logic Symbol



Truth Table

INPUT					OUTPUT
D	RN	SE	SI	CK	Q
0	x	0	x	R	0
x	x	1	0	R	0
x	x	1	x	R	1
1	0	0	x	R	0
1	1	0	x	R	1
x	x	x		x	IQ

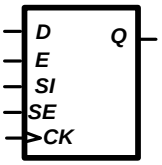
More details refer to doc/DATASHEET/*

SENRQ

Cell Description

The SENRQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and synchronous active-high enable (E). a single output (Q)

Logic Symbol



Truth Table

INPUT					OUTPUT
D	E	SE	SI	CK	Q
x	0	0	x	R	IQ
x	x	1	0	R	0
x	x	1	1	R	1
0	1	0	x	R	0
1	1	0	x	R	1
x	x	x	x	x	IQ

More details refer to doc/DATASHEET/*

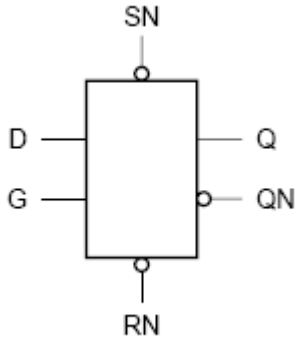
LATCHES

LABHB

Cell Description

The LABHB cell is an active-high D-type transparent latch with asynchronous active-low set (SN)and reset (RN),and set dominating reset.When the enable (G) is high, data is transferred to the outputs (Q, QN).

Logic Symbol



Truth Table

INPUT				OUTPUT	
D	RN	SN	G	Q	QN
x	x	0	x	1	0
x	0	1	x	0	1
x	1	1	0	IQ	IQN
0	1	1	1	0	1
1	1	1	1	1	0

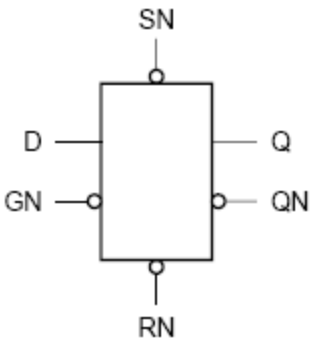
More details refer to doc/DATASHEET/*

LABLB

Cell Description

The LABLB cell is an active-high D-type transparent latch with asynchronous active-low set (SN)and reset (RN),and set dominating reset.When the enable (GN) is low, data is transferred to the outputs (Q, QN).

Logic Symbol



Truth Table

INPUT				OUTPUT	
D	RN	SN	GN	Q	QN
x	x	0	x	1	0
x	0	1	x	0	1
0	1	1	0	0	1
x	1	1	1	IQ	IQN
1	1	1	0	1	0

More details refer to doc/DATASHEET/*

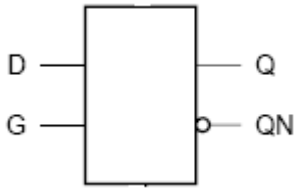
LANHB

Cell Description

The LANHB cell is an active-high D-type transparent latch When the enable (G) is high, data is transferred to the outputs (Q, QN).

Logic Symbol

Truth Table



INPUT		OUTPUT	
D	G	Q	QN
x	0	IQ	IQN
0	1	0	1
1	1	1	0

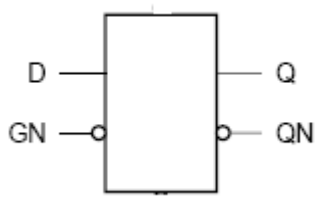
More details refer to doc/DATASHEET/*

LANLB

Cell Description

The LANLB cell is an active-low D-type transparent latch , When the enable (GN) is low, data is transferred to the outputs (Q, QN)

Logic Symbol



Truth Table

INPUT		OUTPUT	
D	GN	Q	QN
0	0	0	1
x	1	IQ	IQN
1	0	1	0

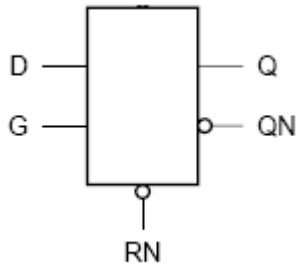
More details refer to doc/DATASHEET/*

LACHB

Cell Description

The LACHB cell is an active-high D-type transparent latch with asynchronous active-low reset (RN) and When the enable (G) is high, data is transferred to the outputs (Q, QN)

Logic Symbol



Truth Table

INPUT			OUTPUT	
D	RN	G	Q	QN
x	0	x	0	1
x	1	0	IQ	IQN
0	1	1	0	1
1	1	1	1	0

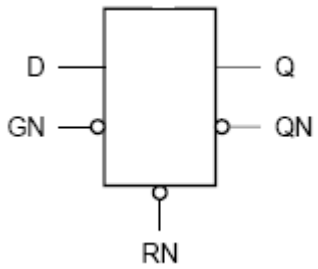
More details refer to doc/DATASHEET/*

LACLB

Cell Description

The LACLB cell is an active- low D-type transparent latch with asynchronous active-low reset (RN) and When the enable (GN) is low, data is transferred to the outputs (Q, QN)

Logic Symbol



Truth Table

INPUT			OUTPUT	
D	RN	GN	Q	QN
x	0	x	0	1
0	1	0	0	1
x	1	1	IQ	IQN
1	1	0	1	0

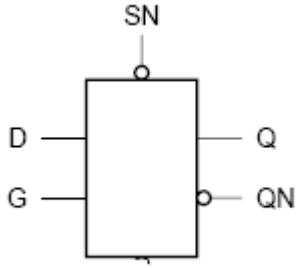
More details refer to doc/DATASHEET/*

LAPHB

Cell Description

The LAPHB cell is an active-high D-type transparent latch with asynchronous active-low set (RN) and When the enable (G) is high, data is transferred to the outputs (Q, QN)

Logic Symbol



Truth Table

INPUT			OUTPUT	
D	SN	G	Q	QN
x	0	x	1	0
x	1	0	IQ	IQN
0	1	1	0	1
1	1	1	1	0

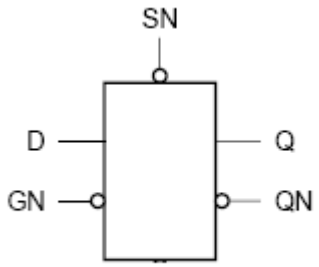
More details refer to doc/DATASHEET/*

LAPLB

Cell Description

The LAPLB cell is an active-low D-type transparent latch with asynchronous active-low set (SN) and When the enable (GN) is low, data is transferred to the outputs (Q, QN)

Logic Symbol



Truth Table

INPUT			OUTPUT	
D	SN	GN	Q	QN
x	0	x	1	0
0	1	0	0	1
x	1	1	IQ	IQN
1	1	0	1	0

More details refer to doc/DATASHEET/*

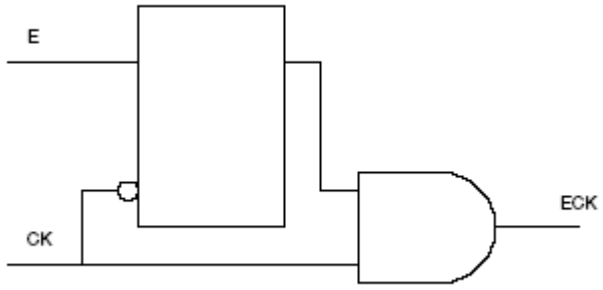
Clock Gating

TLATNCA

Cell Description

The TLATNCAD cell is clock gating cells with enable pin (E) .

Logic Symbol



Truth Table

INPUT		Internal pin	OUTPUT
E	CK	QN(n+1)	ECK
0	0	0	0
1	0	1	0
x	1	QN(n)	QN(n)

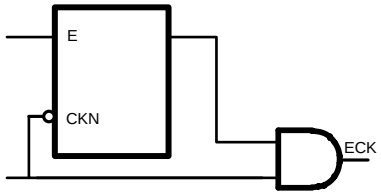
More details refer to doc/DATASHEET/*

TLATNFCA

Cell Description

The TLATNFCA cell is a Negative edge-triggered clock-gating latch.

Logic Symbol



Truth Table

INPUT		INTERNAL PIN	OUTPUT
E	CKN	QN(n+1)	ECK
x	0	QN(n)	QN(n)
0	1	1	1
1	1	0	1

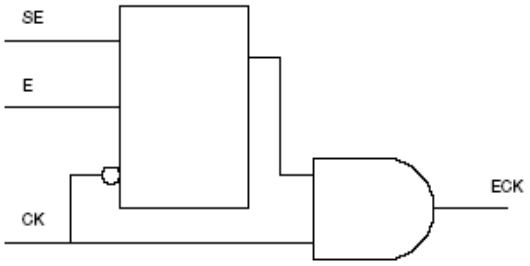
More details refer to doc/DATASHEET/*

TLATNTSCA

Cell Description

The TLATNTSCAD cell is clock gating cells with enable pin (E) and test enable pin (SE)

Logic Symbol



Function Table

INPUT			Internal Pin	OUTPUT
E	SE	CK	QN(n+1)	ECK
0	0	0	1	0
0	1	0	0	0
1	0	0	0	0
1	1	0	0	0
x	x	1	QN(n)	QN(n)

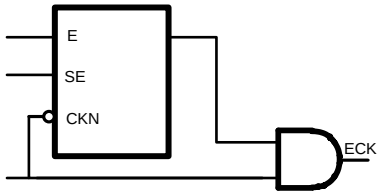
More details refer to doc/DATASHEET/*

TLATNFTSCA

Cell Description

The TLATNFTSCA cell is a Negative edge-triggered clock-gating latch.

Logic Symbol



Truth Table

INPUT			Internal Pin	OUTPUT
E	SE	CKN	QN(n+1)	ECK
0	0	1	0	1
0	1	1	1	1
1	0	1	1	1
1	1	1	1	1
x	x	0	QN(n)	QN(n)

More details refer to doc/DATASHEET/*

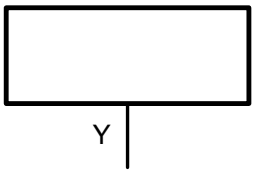
MISCELLANEOUS FUNCTIONS

ANTENNA

Cell Description

The library contains an antenna-fix cell which must be inserted manually. However, most place and route tools will indicate which nets require the antenna cell. The CSMC antenna effect prevention guideline, "CSMC 0.11µm eFlash 2P8M Salicide process," specifies a maximum wire length. During place and route, the router may connect wires to the input gates of cells that are longer than the maximum length allowable by the guideline. The antenna cell can be used in this case to add an optional diode on the net close to the input gates which do not meet the guideline. Pin A on the antenna cell connects to a diode, reverse biased to ground.

Logic Symbol



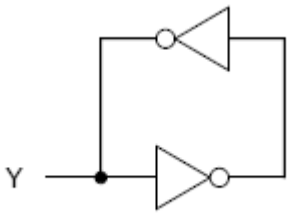
More details refer to doc/DATASHEET/*

BH01

Cell Description

The BH01 cell holds data at a known value. This cell is often used for holding data on a tri-state bus.

Logic Symbol



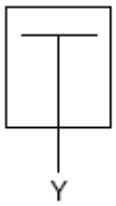
TIEHI

Cell Description

The TIEHI cell drives the output (Y) to a logic high. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:

$$Y = 1$$

Logic Symbol



More details refer to doc/DATASHEET/*

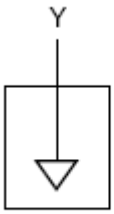
TIELO

Cell Description

The TIELO cell drives the output (Y) to a logic low. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:

$$Y = 0$$

Logic Symbol



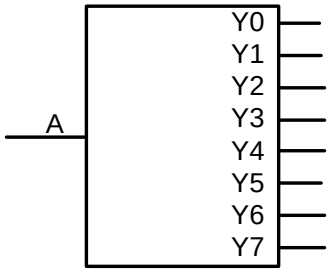
More details refer to doc/DATASHEET/*

INVOD8

Cell Description

The INVOD8 cell invertor with eight open drain pin

Logic Symbol



Function table

INPUT	OUTPUT							
A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
0	0	0	0	0	0	0	0	0
1	Hiz	Hiz	Hiz	Hiz	Hiz	Hiz	Hiz	Hiz

More details refer to doc/DATASHEET/*

ND02OD

Cell Description

The ND02OD cell with open drain

Logic Symbol

Truth Table

INPUT		OUTPUT
A	B	Y
0	x	Hiz
1	0	Hiz
1	1	-

More details refer to doc/DATASHEET/*

ND03OD

Cell Description

The ND03OD cell with open drain

Logic Symbol

Truth Table

INPUT			OUTPUT
A	B	C	Y
0	x	x	Hiz
1	0	x	Hiz
1	1	0	Hiz
1	1	1	0

More details refer to doc/DATASHEET/*

OR02OD

Cell Description

The OR02OD cell with open drain

Logic Symbol

Truth Table

INPUT		OUTPUT
A	B	Y
0	0	0
1	x	Hiz
x	1	Hiz

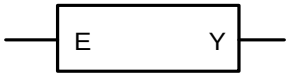
More details refer to doc/DATASHEET/*

PULLU

Cell Description

The PULLU cell is internal pull up with Enable pin (E)

Logic Symbol



Truth Table

INPUT	OUTPUT
E	Y
0	Hiz
1	1

More details refer to doc/DATASHEET/*

PULLD

Cell Description

The PULLU cell is internal pull down with Enable pin (EN)

Truth Table

INPUT	OUTPUT
EN	Y
0	0
1	Hiz

Logic Symbol :

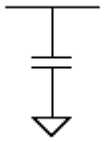
More details refer to doc/DATASHEET/*

FILLCAP

Cell Description

The FILLCAP cell is a filler cell that contains decoupling capacitors between VDD and GND rails to reduce ground bounce in the power grids.

Logic Symbol



FILLER

Cell Description

The library contains several FILLER cells:filler1, 2, 3,4,6,8,16,32,64. The number appended to "FILLER" in the cell name denotes the width of the cell in tracks.

During place and route, the FILLER cells are used to connect power and ground rails across an area containing no cells. The FILLER cells are also used to ensure gaps do not occur between well or implant layers which could cause design rule violations. Using wider cells where appropriate reduces the size of the layout database.

PMK

Library Description

CSMC 0.11um Power Management Kit Library is for CSMC 0.11um Eflash 2P8M process ,based on its 6-track layout .the library is a supplement of power switch cells and commonly used supporting features,such as always-on logic,isolation interface and levelshifters cells.

General Information

The pmk cells can be placed together with the cells in normal standard library .Please refer to PMK Power Rail Information on page 172.

Retention DFF

DRFCRB

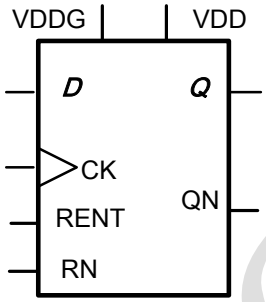
Cell description:

The DRFCRB cell is a positive edge-triggered ,static D Flip flop with asynchronous active-low reset RN.It will retain its stored state when VDD are powered down using power from VDDG.

Function Table

INPUT				OUTPUT	
D	RETN	RN	CK	Q	QN
0	x	1	R	0	1
1	0	1	R	0	1
1	1	1	R	1	0
x	x	0	x	0	1
x	x	1	x	IQ	IQN

Logic symbol



More details please ref to ../doc/DATASHEET

DRFNRB

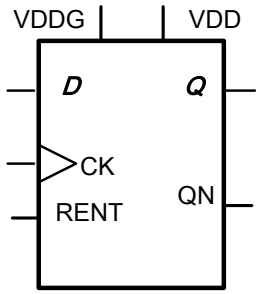
Cell description:

The DRFNRB cell is a positive edge-triggered ,static D Flip flop .It will retain its stored state when VDD are switch off. Power for this retention function comes from VDDG

Function Table

INPUT			OUTPUT	
CK	D	RETN	Q	QN
R	0	x	0	1
R	1	0	0	1
R	1	1	1	0
x	x	x	IQ	IQN

Logic symbol



More details please ref to ../doc/DATASHEET

DRFPRB

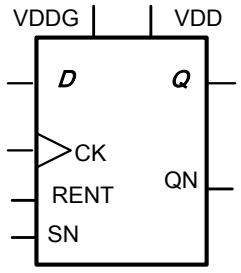
Cell description:

The DRFPRB cell is a positive edge-triggered ,static D Flip flop . with asynchronous active-low set SN . It will retain its stored state when VDD and/or GND are powered down using power from VDDG

Function Table

INPUT				OUTPUT	
D	RETN	SN	CK	Q	QN
0	x	1	R	0	1
1	0	1	R	0	1
1	1	1	R	1	0
x	x	0	x	0	1
x	x	1	x	IQ	IQN

Logic symbol



More details please ref to ../doc/DATASHEET

Always On

GPGBUFF

Cell description:

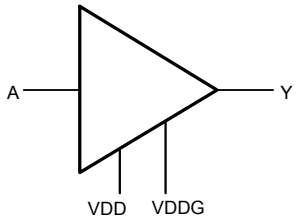
The GPGBUF cell is a non-inverting cell powered by VDDG pin rather than the VDD rails.Since it is powered by unswitched VDDG,the output Y can remain valid even when VDD are switched off .The output Y is represented by the logic equation:

$$Y = A$$

Function table

A	VDDG	Y
0	1	0
1	1	1

Logic symbol



More details please ref to ../doc/DATASHEET

GPGINV

Cell description:

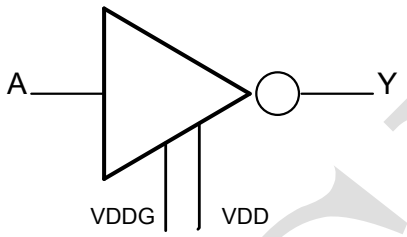
The GPGINV cell is an inverting cell powered by VDDG pin rather than the VDD rails.Since it is powered by unswitched VDDG,the output Y can remain valid even when VDD are switched off .The output Y is represented by the logic equation:

$$Y = ! A$$

Function table

A	VDDG	Y
0	1	1
1	1	0

Logic symbol



More details please ref to ../doc/DATASHEET

Power Gating

HEAD

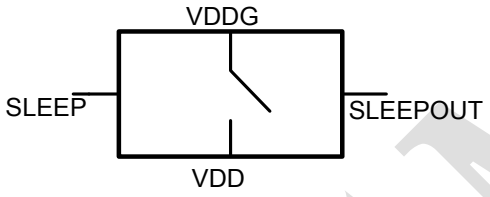
Cell description:

The HEAD cell is a power gating cell that connects local power (VDD) to global power (VDDG) when SLEEP is low .A buffer is included for SLEEP that is powered by VDDG so it will not power down if VDD is powered down.

Function table

SLEEP	VDDG	VDD	SLEEPOUT
0	1	1	0
1	1	Hi-z	1

Logic symbol



More details please ref to ../doc/DATASHEET

Isolation cell

ISOHD

Cell description:

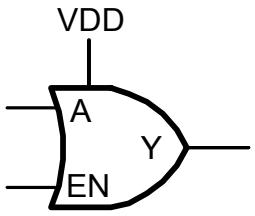
The ISOHD cell is a isolation cell.This cell is placed in a power domain (the sink domain)that receives input from a different power domain ,which may be powered down while the sink domain is still powered up.

Y= A + EN

Function table

A	EN	Y
0	0	0
X	1	1
1	X	1

Logic symbol



More details please ref to ../doc/DATASHEET

ISOLD

Cell description:

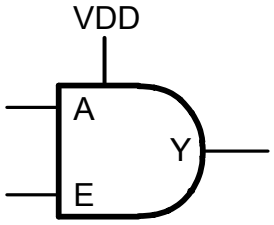
The ISOHD cell is a isolation cell.This cell is placed in a power domain (the sink domain)that receives input from a different power domain ,which may be powered down while the sink domain is still powered up.

Y= A & E

Function table

A	E	Y
0	X	0
1	0	0
1	1	1

Logic symbol



More details please ref to ../doc/DATASHEET

Retention DFF with Scan

SDRCRB

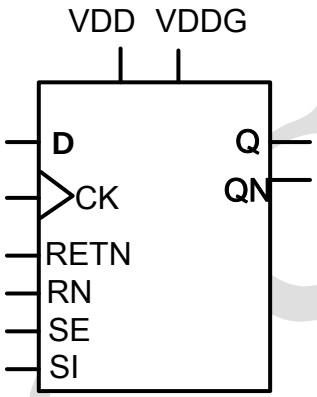
Cell description:

The SDRCRB cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) .it can retain its state when power are switched off .Power for this retention function comes from VDDG.

Function Table

INPUT						OUTPUT	
D	SE	SI	RETN	RN	CK	Q	QN
0	0	x	x	1	R	0	1
x	1	0	x	1	R	0	1
x	1	1	0	1	R	0	1
x	1	1	1	1	R	1	0
1	0	x	0	1	R	0	1
1	0	x	1	1	R	1	0
x	x	x	x	0	x	0	1
x	x	x	x	1	x	IQ	IQN

Logic symbol



More details please ref to ../doc/DATASHEET

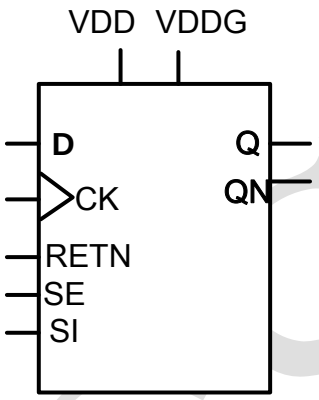
SDRNRB

Cell description:
The SDRNRB cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous reset (RN) .it can retain its state when power are switched off .Power for this retention function comes from VDDG.

Function Table

INPUT					OUTPUT	
D	RETN	SE	SI	CK	Q	QN
x	0	x	x	R	0	1
0	1	0	x	R	0	1
x	1	1	0	R	0	1
x	1	1	1	R	1	0
1	1	0	x	R	1	0
x	x	x	x	x	IQ	IQN

Logic symbol



More details please ref to ../doc/DATASHEET

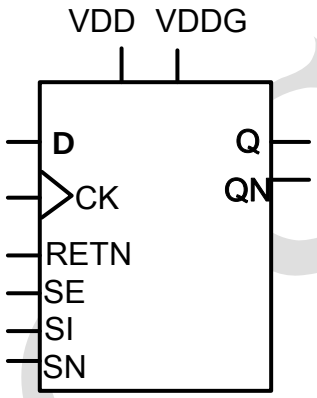
SDRPRB

Cell description:
The SDRPRB cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous set (SN) .it can retain its state when power are switched off .Power for this retention function comes from VDDG.

Function Table

INPUT						OUTPUT	
D	SE	SI	RETN	SN	CK	Q	QN
0	0	x	x	1	R	0	1
x	1	0	x	1	R	0	1
x	1	1	0	1	R	0	1
x	1	1	1	1	R	1	0
1	0	x	0	1	R	0	1
1	0	x	1	1	R	1	0
x	x	x	x	0	x	1	0
x	x	x	x	1	x	IQ	IQN

Logic symbol

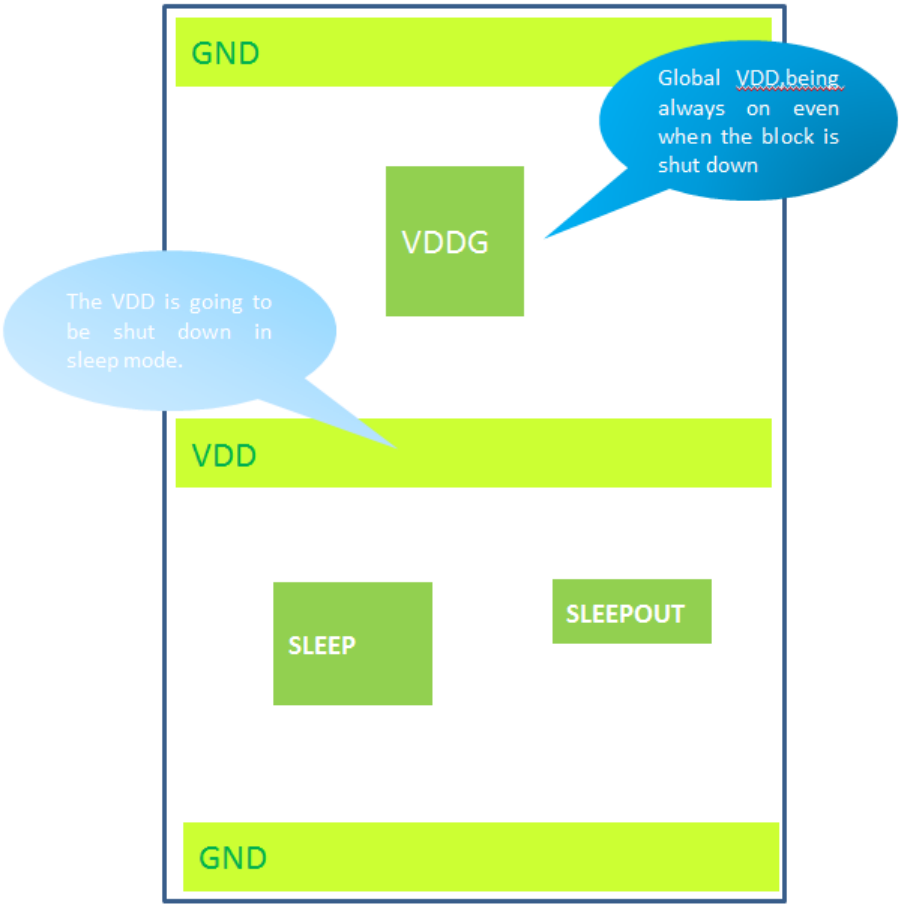


More details please ref to ../doc/DATASHEET

PMK Power Rail Information

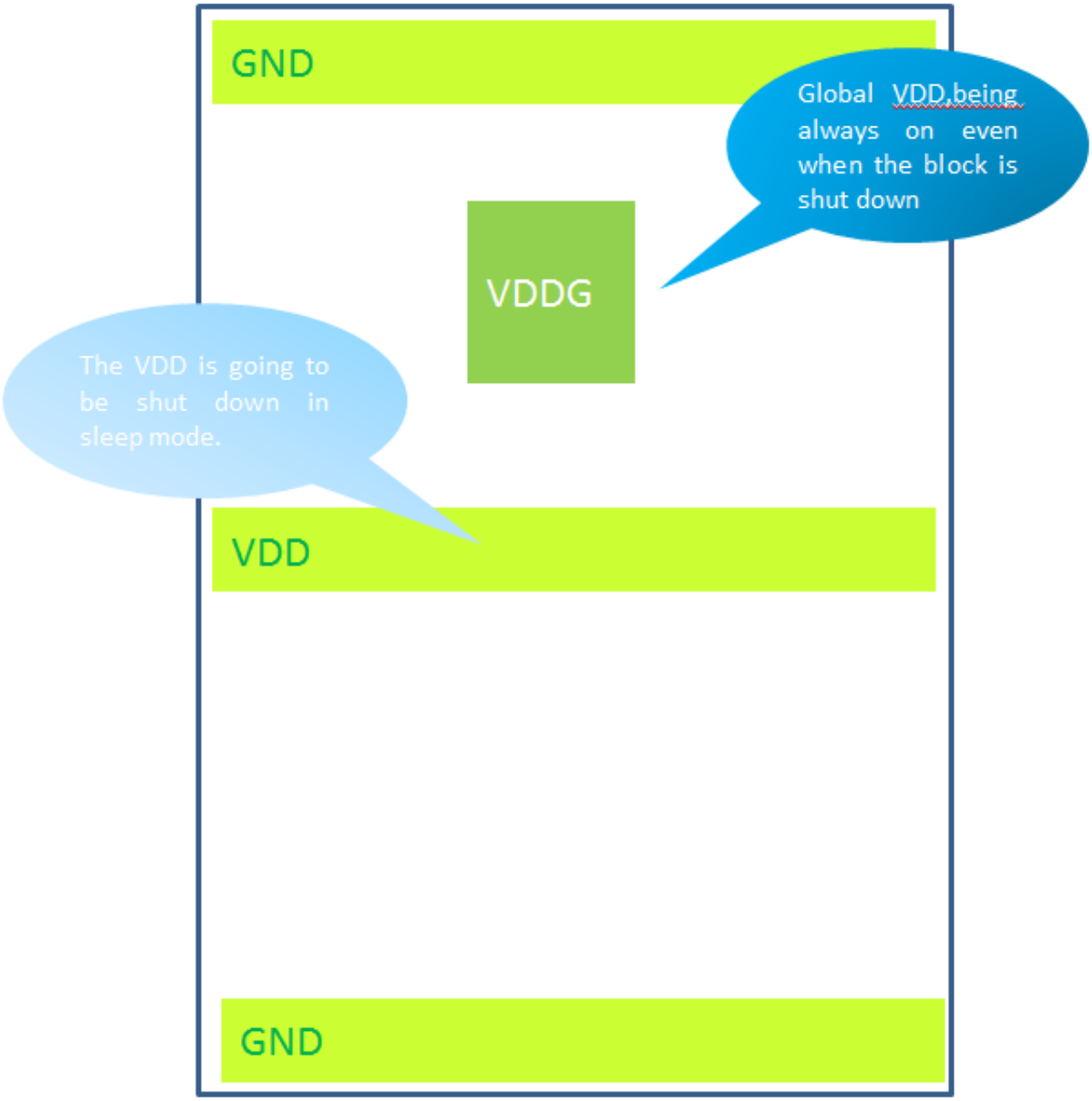
HEAD CELL power supply :

The cell layout is double height . The figure below shows there are 2 power pins in the cell.VDD should be connected to the primary power of the power-switchable block ;VDDG should be connected to the global power rail which remains when the block is power-off.



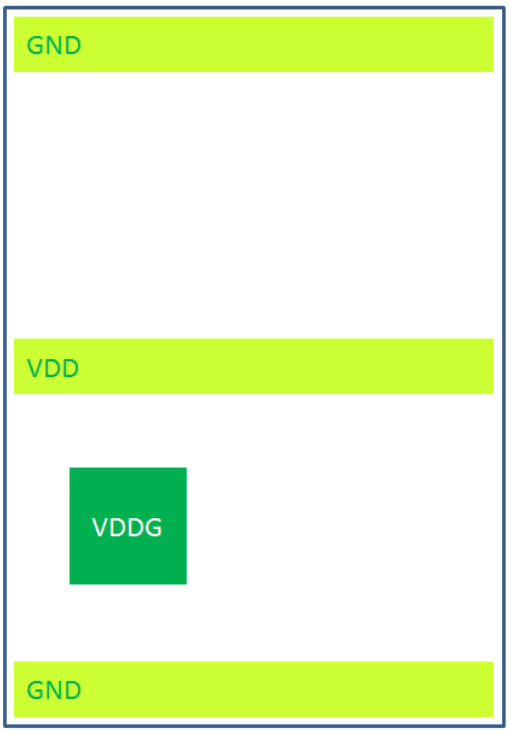
Always on cells' power supply :

The Figure below shows the PG is in always-on cell.The cell is double height,which have 2 power pins .VDD should be connected to the power of the power-switchable block which is usually gated by the power-switching header;VDDG should be connected to the global power rail which remains valid when the block is powered off .



Retention DFF power supply :

The cell layout is double height . It has two power pins ,one is VDD which should be connected to the power of the power-switchable block, which is usually gated by the power-switching header;the other is VDDG ,which should be connected to the global power rail which remains valid when the block is powered off.



Intergrating the Power Gating Function :

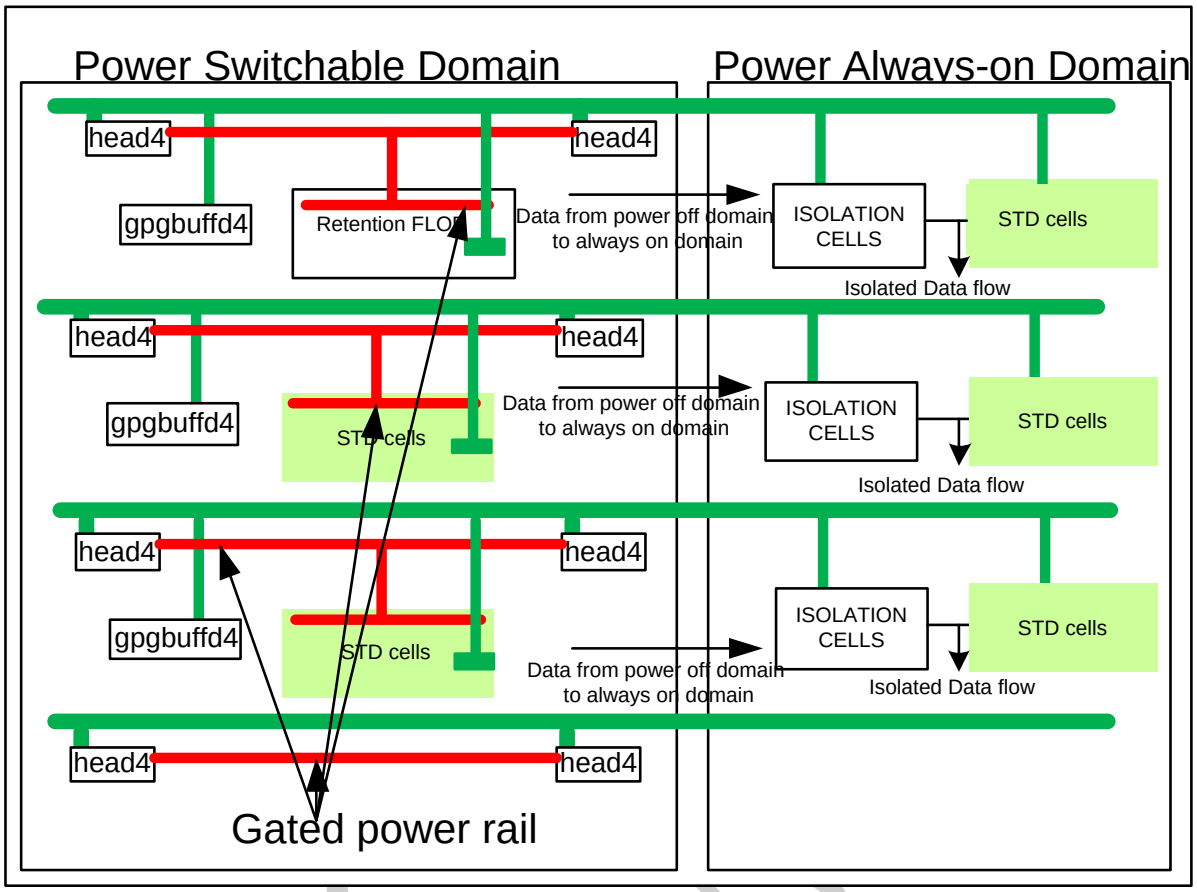
The figure below shows how the PMK cells work together in a design where one of its blocks has power-gating feature.And the followings are some guidelines for the intergration.

Head cells get their power from the global power rail (as the green line in the figure below) and gate out the switchable VDD rail (as the red line) to power the part of the block.

The head cells should be connected one after another by SLEEP and SLEEPOUT pins to form a power-switch-chain ,to ensure the gated VDD rail turns on and off gradually when switched .

A secondary supply grid for global power is needed within the power switchable domain to power the always-on cells and the always on domain of the retention flip flop cells .

Whenever signals flow from the power-switchable domain to the power-on domain,isolation cells are needed as the interface to ensure the validation of data in case the power-switchable domain is off ,isolation cells are required to get their power from the global power supply ,which is always on.


Power Switchable Domain
Power Always-on Domain
head4
head4
gpgbuffd4
Retention FLOP
Data from power off domain
to always on domain
ISOLATION
CELLS
STD cells
Isolated Data flow
head4
head4
gpgbuffd4
STD cells
Data from power off domain
to always on domain
ISOLATION
CELLS
STD cells
Isolated Data flow
head4
head4
gpgbuffd4
STD cells
Data from power off domain
to always on domain
ISOLATION
CELLS
STD cells
Isolated Data flow
head4
head4
Gated power rail