1.5V 6Track Standard Cell Library for CSMC 0.11um e-FLASH 2P8M Salicide Process

User's Guide

Version 0.2

Sep. 30th, 2019

Notice

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Revision History

Document Version	Date	Notes
1.0	Sep.25 ,2018	Production Build
2.0	Jan.2,2019	Improve pmk description
3.0	Sep.30,2019	EDR/Model updated ;1.2v corner Not provided ;

Introduction

This user'guide is intended to give users a general overview of the current 0.11um 1.5V Standard Cell Library for CSMC 0.11um Eflash Process details for the production release contents and structure.

Library Description

The 0.11um 1.5V Standard Cell Design Kit Library is for CSMC eFlash Process ,based on a 6 Track layout,including generic standard cell library .In order to satisfy the power and performance requirement,it also provides a set of power switch cells ,always on ,isolation ,retention cells and level shifters cells.

STD/PMK Library Operating Conditions

The recommended operating conditions for IC using the library as follows :

Recommended Operating Conditions 1				
Operating Conditions	TT	FF	FF	SS
Core DC supply Voltage	1.5V	1.65V	1.65V	1.35V
Junction Temperature	25℃	-40℃	125℃	125℃

Library Feature

- CSMC 0.11um EFLASH 2P8M Salicide 1.5V Process
- Support CSMC 0.11um e-FLASH 2P8M Salicide 1.5V process Version #:8A09 Design rule
  Note :when check lvs ,MOS width property magin < 0.5%
- Support CSMC 0.11um e-FLASH 2P8M Salicide 1.5V process **N1128X00V02** SPICE model
- 690 standard core cells:
  - STD :612
  - PMK:46
- Interval cells optimized for synthesis.
- Accurate timing characterization
- Support most of the EDA tools
- Optimized for Cadence and Synopsys place&route tools.
- High routing density, routability, high speed and low power .
- Routable for 4,5,6, 7, 8 metals
- Top metal thickness for 8K

Library Package Contents

- Optimum Silicon standard core cell library : CSMC011EFLASH2P8M6T

EDA Tool Environment

The library has been designed under Cadence and Synopsys software environment that consists of the following tools :

- Cadence Abstract 5.7
- Cadence ICFB 51
- Synopsys Astro 2007.03-SP9
- Synopsys HSPICE 2012.06
- Mentor LibComp v8.2009_1.10
- Synopsys StarRCXT B-2008.06-SP1
- Synopsys Design Compiler B-2008.09-SP5
- Synopsys Hercules B-2008.09
- Synopsys Milkyway G-2012.06-SP3
- Cadence Verilog_XL LDV5.1-QSR3
- Cadence encounter 10.12.002
- Mentor Calibre v2006.3_21.18
- Cadence Techgen 17.10.000

Library Shipping Database

- CSMC011EFLASH2P8M6T_FB --- Include GDSII and corresponding database.

What is CSMC FB Library Installation Directory

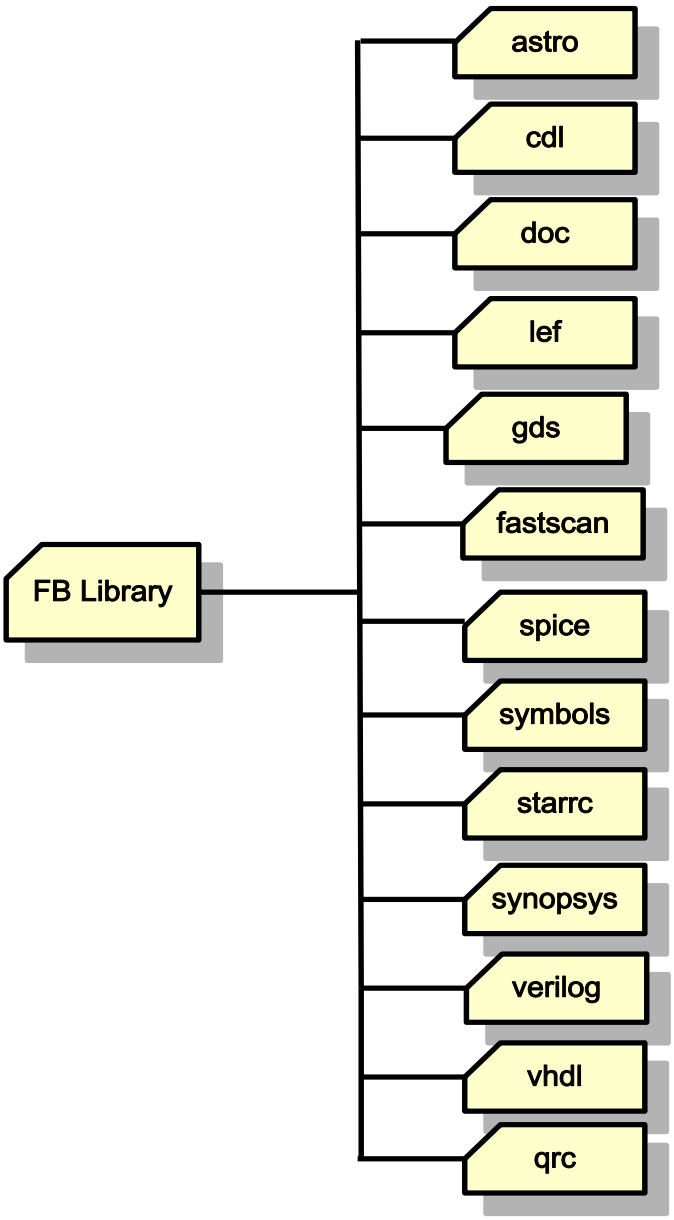

Figure 1 FB directory structure of CSMC library

FB Directory Major Structure Introduction

1. Astro

Content	Description
csmc011（Milkyway:std/pmk）	*CSMC 0.11um e-FLASH 1P8M standard CORE and PMK cells' FRAM, CELL, LM*
tf	*CSMC 0.11um e-FLASH 1P8M process Apollo and Astro technology file*
clf(std/pmk)	*CSMC 0.11um e-FLASH 1P8M standard CORE cells' timing model, including antenna information*
tcl	*Antenna tcl for icc*

2. cdl

Content	Description
csmc011.cdl	*CSMC 0.11um e-FLASH standard CORE cells' cdl netlist. It can be included to do lvs checking.*
csmc011_pmk.cdl	*CSMC 0.11um e-FLASH standard PMK cells' cdl netlist. It can be included to do lvs checking*

3. doc

Content	Description
CSMC0111P8M6T_DATASHEET	*0.11um e-FLASH 1P8M Salicide 1.5V Process standard CORE cells' descriptions.*
CSMC011_library_user_guide	*0.11um e-FLASH 1P8M Salicide 1.5V Process standard CORE cell library user guide*
libCellDataSheet	*0.11um e-FLASH1P8M Salicide 1.5V Process standard CORE cells' datasheet.*
DATASHEET/*	*0.11um e-FLASH1P8M Salicide 1.5V Process PMK/STD cells' details.*

4. fastscan

Content	Description
csmc011_ull_6T.atpglib	*0.11um e-FLASH 1P8M Salicide 1.5V Process standard CORE cells' ATPG library*
csmc011_ull_pmk.atpglib	*0.11um e-FLASH 1P8M Salicide 1.5V Process*

	standard PMK cells' ATPG library

5. **gds**

Content	Description
csmc011.gds	*0.11um e-FLASH 1P8M Salicide 1.5V process standard core cells' gds2 database*
csmc011_pmk.gds	*0.11um e-FLASH 1P8M Salicide 1.5V process standard PMK cells' gds2 database*

6. **symbols**

Content	Description
cadence	*0.11um e-FLASH 1P8M Salicide 1.5V process standard core cells' cadence symbol library*
	0.11um e-FLASH 1P8M Salicide 1.5V process standard PMK cells' cadence symbol library
edif	*0.11um e-FLASH 1P8M Salicide 1.5V process standard core cells' edif library*
	0.11um e-FLASH 1P8M Salicide 1.5V process standard PMK cells' edif library
Synopsys	*Core std cells'Synopsys symbol library*
	PMK cells'Synopsys symbol library

7. **lef (8k)**

Content	Description
csmc011_ull_4lm.lef	*0.11um e-FLASH 1P8M Salicide 1.5V process 4 metal technology lef file*
csmc011_ull_5lm.lef	*0.11um e-FLASH 1P8M Salicide 1.5V process 5 metal technology lef file*
csmc011_ull_6lm.lef	*0.11um e-FLASH 1P8M Salicide 1.5V process 6 metal technology lef file*
csmc011_ull_7lm.lef	*0.11um e-FLASH 1P8M Salicide 1.5V process 7 metal technology lef file*
csmc011_ull_8lm.lef	*0.11um e-FLASH 1P8M Salicide 1.5V process 8 metal technology lef file*

csmc011_ull.lef	*0.11um e-FLASH 1P8M Salicide 1.5V process standard core cells' Library Exchange Format description files*
csmc011_ull_pmk.lef	*0.11um e-FLASH 1P8M Salicide 1.5V process standard PMK cells' Library Exchange Format description files*

8. **spice (std/pmk)**

Content	Description
*.pex.netlist *.pex.netlist.*.pxi *.pex.netlist.pex	*0.11um e-FLASH 1P8M Salicide 1.5V process standard core and PMK cells' Hspice netlist*

9. **Starrc(8k)**

Content	Description
a4/a5/a6/a7/a8_gt_cell_8k_max.nxtgrd a4/a5/a6/a7/a8_gt_cell_8k_min.nxtgrd a4/a5/a6/a7/a8_gt_cell_8k_typ.nxtgrd	*0.11um e-FLASH 1P8M Salicide1.5Vprocess Star_RCXT technology files for TT, SS, FF corner*
a4/a5/a6/a7/a8_gt_cell_8k_max.itf a4/a5/a6/a7/a8_gt_cell_8k_min.itf a4/a5/a6/a7/a8_gt_cell_8k_typ.itf	*0.11um e-FLASH 1P8M Salicide 1.5V process itf files for TT, SS, FF corner*
a4/a5/a6/a7/a8_gt_cell_8k_max.tluplus a4/a5/a6/a7/a8_gt_cell_8k_min.tluplus a4/a5/a6/a7/a8_gt_cell_8k_typ.tluplus	*0.11um e-FLASH 1P8M Salicide 1.5V process TLUPlus files for TT, SS, FF corner*

10. **synopsys (std/pmk)**

Content	Description
csmc011_ull_6T_ff_1p65v_-40c.lib csmc011_ull_6T_ff_1p65v_125c.lib csmc011_ull_6T_ff_1p65v_0c.lib csmc011_ull_6T_ss_1p35v_125c.lib csmc011_ull_6T_ss_1p35v_85c.lib csmc011_ull_6T_tt_1p5v_25c.lib csmc011_ull_6T_ff_1p65v_-40c.db csmc011_ull_6T_ff_1p65v_125c.db csmc011_ull_6T_ff_1p65v_0c.db csmc011_ull_6T_ff_1p35v_125c.db csmc011_ull_6T_ff_1p35v_85c.db csmc011_ull_6T_tt_1p5v_25c.db	*0.11um e-FLASH 1P8M Salicide process standard core cells' synopsys timing models on 1.5V TT, SS125℃, SS85℃,FF_-40℃, FF_0℃, FF_125℃ corner*
csmc011_ull_6T_pmk_ff_1p65v_-40c.lib csmc011_ull_6T_pmk_ff_1p65v_125c.lib	*0.11um e-FLASH 1P8M Salicide process PMK cells'*

csmc011_ull_6T_pmk_ff_1p65v_0c.lib csmc011_ull_6T_pmk_ss_1p35v_125c.lib csmc011_ull_6T_pmk_ss_1p35v_85c.lib csmc011_ull_6T_pmk_tt_1p5v_25c.lib csmc011_ull_6T_pmk_ff_1p65v_-40c.db csmc011_ull_6T_pmk_ff_1p65v_125c.db csmc011_ull_6T_pmk_ff_1p65v_0c.db csmc011_ull_6T_pmk_ss_1p35v_125c.db csmc011_ull_6T_pmk_ss_1p35v_85c.db csmc011_ull_6T_pmk_tt_1p5v_25c.db	*synopsys timing models on 1.5V TT, SS125 ℃ , SS85 ℃ ,FF_-40 ℃ , FF_0 ℃,FF125 ℃ corner*

11. Verilog

std

Content	Description
csmc011_ull_6T.v	*0.11um e-FLASH 1P8M Salicide 1.5V process standard CORE cells' verilog format behavior model of Version 2.1*

pmk

Content	Description
csmc011_ull_6T_pmk.v	*0.11um e-FLASH 1P8M Salicide 1.5V process standard CORE cells' verilog format behavior model*
csmc011_ull_6T_pmk_be.v	*0.11um e-FLASH 1P8M Salicide 1.5V process standard CORE cells' verilog format behavior model with power information ;*

12. vhdl

Content	Description
*.vhd	*0.11um e-FLASH 1P8M Salicide 1.5V process standard core and PMK cells' VHDL format behavior models on TT, SS, FF_-40 ℃, FF_0 ℃,FF125 ℃ corner*

13. qrc(8k)

Content	Description
a4/a5/a6/a7/a8_gt_cell_8k_max.ict a4/a5/a6/a7/a8_gt_cell_8k_min.ict a4/a5/a6/a7/a8_gt_cell_8k_typ.ict a4/a5/a6/a7/a8_gt_cell_8k_max_captbl	*CSMC 0.11um e-FLASH Mixed Signal Salicide process 8K 4/5/6/7/8 metal qrc_RCXT gate level extraction technoMixed Signal files*

a4/a5/a6/a7/a8_gt_cell_8k_min_captbl **a4/a5/a6/a7/a8_gt_cell_8k_typ_captbl** ***/max/qrcTechFile** ***/min/qrcTechFile** ***/typ/qrcTechFile**	

Library Cell List For STD

The CSMC011 internal library supports a rich set of variable functions. It includes the following types of function cells:

ad …….. Full Adder GATES

ah …….. Half Adder GATES

an……AND GATES

antenna……ANTENNA-Fix CELL

aoi …….. AND-NOR GATES

aor…….. AND-OR GATES

bh…….. BUS HOLD CELL

buff……Buffer GATES

buft……..TRI-STATE BUFFER

ckan……Clock AND GATES

ckbuf……Clock BUFFER GATES

ckinv……Clock INVERT GATES

ckmx……Clock Multiplexer

cknd……Clock NAND GATES

cknr……Clock NOR GATES

ckor……Clock OR GATES

ckxn……Clock XNOR GATES

ckxr……Clock Exclusive OR GATES

df/dm…….D Flip-Flop

dl…….Delay GATES

fillcap…….Decoupling CELL

filler ……. Filler CELL GATES

inv0…….INVERTER GATES

invt…….TRI-STATE INVERTER GATES

la…….LATCH GATES

mi……Inverting MUX GATES

mx……MUX GATES

nd…….NAND GATES

nr…….NOR GATES

oai……OR-NAND GATES

or……OR GATES

ora……..OR-AND GATES

sd……Scan D Flip-Flop

se……Scan Enable D Flip-Flop

tie……..Drive Output to A Fixed State

tlat……Clock Gating CELL

xn……...XNOR GATES

xr……XOR GATES

STD Cells listed below:

Drive CAPABILITY :0<M<1<2<4 <P.. etc

Arithmetic Gates	
ad01dN	1-bit FULL ADDER (0,1,2,3,m)
adfh01dN	1-bit High-speed FULL ADDER (0,1,2)
ah01dN	1-bit Half Adder (0,1,2,3,m)

Buffers Gates

buffdN	Non Inverting(0,1,2,3,4,5,6,7,8,12,16,20,m)
buftdN	Non-inverting 3-state Buffer with active low enable (0,1,2,3,4,6,8,12,16,20,m)
ckbufdN	Clock Non Inverting (0,1,2,3,4,5,6,7,8,10,12,14,16,20,30,40,80,m)
ckanddN	Clock nand2 (0,1,2,4)
ckinvdN	Clock Inverting (0,1,2,3,4,5,6,7,8,10,12,14,16,20,30,40,80)
inv0dN	Inverter (0,1,2,3,4,5,6,7,8, 12, 16, 20,m,p)
invtldN	Inverter 3-state Buffer with active high enable (0,1,2,3,4,6,8,12,16,20,m)
dl01dN	Delay Gate(1,2,m)
dl02dN	Delay Gate(1,2)

COMPLEX Gates

aoi21dN	AND-NOR 2,1 (0,1,2,4,m)
aoi2m1dN	AND-NOR 2,1 1 inv(0,1,2,4)
aoi21mdN	AND-NOR 2,1 NOR1inv (0,1,2,4)
aoi31dN	AND-NOR 3,1 (0,1,2,4,m)
aoi32dN	AND-NOR 3,2 (0,1,2,4,m)
aoi33dN	AND-NOR 3,3 (0,1,2,4)
aoi22dN	AND-NOR2,2 (0,1,2,4,m)

aoi211dN	AND-NOR 2,1,1 (0,1,2,4)
aoi221dN	AND-NOR 2,2,1 (0,1,2,4)
aoi222dN	AND-NOR 2,2,2 (0,1,2,4)
aoim21dN	AND-NOR2,1 2 invt (0,1,2,3,m)
aoim22dN	AND-NOR2,2 2 invt (0,1,2,4,m)
oai21dN	OR-NAND2,1 (0,1,2,4,m)
oai2m1d0	OR-NAND2,1 or 1 inv(0,1,2,4)
oai21md0	OR-NAND2,1 nand 1inv (0,1,2,4)
oai31dN	OR-NAND3,1 (0,1,2,4)
oai32dN	OR-NAND3,2 (0,1,2,4)
oai33dN	OR-NAND3,3 (0,1,2,4)
oai22dN	OR-NAND2,2 (0,1,2,4,m)
oai211dN	OR-NAND2,1,1 (0,1,2,4)
oai221dN	OR-NAND2,2,1 (0,1,2,4)
oai222dN	OR-NAND2,2,2 (0,1,2,4)
oaim21dN	OR-NAND2,1 2 invt (0,1,2,4,m)
oaim22dN	OR-NAND2,2 2 invt (0,1,2,4,m)
aor21dN	AND-OR 2,1 (0,1,2,4)
aor22dN	AND-OR 2,2 (0,1,2,4)
aor211dN	AND-OR 2,1,1(0,1,2,4)
aor221dN	AND-OR 2,2,1 (0,1,2,4)
aor222dN	AND-OR 2,2,2(0,1,2,4)
aor31dN	AND-OR 3,1 (0,1,2,4)
ora211dN	OR -AND 2,1,1 (0,1,2,4)
ora221dN	OR -AND 2,2,1 (0,1,2,4)
ora222dN	OR -AND 2,2,2 (0,1,2,4)
ora21dN	OR -AND 2,1 (0,1,2,4)
ora22dN	OR -AND 2,2 (0,1,2,4)
ora31dN	OR -AND 3,1 (0,1,2,4)

Gates

an02dN	AND 2 input (0,1,1p5,2,2p5,3p5,4,m)
an03dN	AND 3 input (0,1,2,4,m)
an04dN	AND 4 input (0,1,2,4,m)
ckanddN	CLOCK AND 2 input (0,1,2,4)
cknd02dN	CLOCK NAND 2 input (0,1,2,4)
cknr02dN	CLOCK NOR 2 input (0,1,2,4)

ckor02dN	CLOCK OR 2 input (0,1,2,4)
ckxn02dN	CLOCK Excl-NOR 2 input (0,1,2,4)
ckxr02dN	CLOCK Excl-OR 2 input (0,1,2,4)
nd02dN	NAND 2 input (0,1,1.5,2,2.5,3,3.5,m)
nd12dN	NAND 2 input 1 invt (0,1,2,3,m)
nd03dN	NAND 3 input (0,1,2,3)
nd13dN	NAND 3 input 1 invt (0,1,2,3)
nd04dN	NAND 4 input (0,1,2,3)
nd14dN	NAND 4 input 1 invt (0,1,2,3)
nd24dN	NAND 4 input 2 invt (0,1,2,3)
nr02dN	NOR 2 input (0,1,2,4,m)
nr12dN	NOR 2 input 1 inv (0,1,1.5,2,2.5,4,m)
nr03dN	NOR 3 input (0,1,2,4)
nr13dN	NOR 3 input 1 inv (0,1,2,4)
nr04dN	NOR 4 input (0,1,2,4)
nr14dN	NOR 4 input 1 inv (0,1,2,4)
nr24dN	NOR 4 input 2 inv (0,1,2,4)
or02dN	OR 2 input (0,1,1.5,2,2.5,4,4.5,m)
or03dN	OR 3 input (0,1,2,4,m)
or04dN	OR 4 input (0,1,2,4)
xn02dN	Excl-NOR 2 input (0,1,2,4,m)
xn03dN	Excl-NOR 3 input (0,1,2,4,m)
xr02dN	Excl-OR 2 input (0,1,2,4,m)
xr03dN	Excl-OR 3 input (0,1,2,4,m)

MULTIPLEXERS

ckmx02dN	CLOCK Mux 2-to-1 (0,1,2,4)
mx02dN	Mux 2-to-1 (0,1,2,3,m)
mi02dN	Inverting Mux 2-to-1 (0,1,2,3,m)
mx03dN	Mux 3-to-1 (0,1,2,3)
mx04dN	Mux 4-to-1 (0,1,2,3,m)

FLIP FLOPS

denrqN	Pos. Edge Enable DFF, active-high enable , Q only (0,1,2)
dfanrq0	With input NAND2 D0,D1 Pos. Edge DFF, Q only(0,1,2)
dfbfbN	Neg. Edge DFF, preset & clear (0,1,2)
dfbrbN	Pos. Edge DFF, preset & clear (0,1,2,m)

dfbrqN	Pos. Edge DFF, preset & clear, Q only (0,1,2)
dfcfbN	Neg. Edge DFF, clear (0,1,2)
dfcrbN	Pos. Edge DFF, clear (0,1,2,m)
dfcrqN	Pos. Edge DFF, clear, Q only (0,1,2,m)
dfnfbN	Neg. Edge DFF(0,1,2)
dfnfqN	Neg. Edge DFF,Q only (0,1,2)
dfnrbN	Pos. Edge DFF(0,1,2)
dfnrqN	Pos. Edge DFF, Q only(0,1,2)
dfpfbN	Neg. Edge DFF, active-low preset(0,1,2)
dfprbN	Pos. Edge DFF, active-low preset(0,1,2)
dfprqN	Pos. Edge DFF, active-low preset,Q only(0,1,2,m)
dfscrqN	Pos. Edge synchronous DFF, clear, Q only (0,1,2)
dmnrqN	Pos. Edge DFF, Q only (0,1,2) with selected INPUT data D0,D1

LATCHES

labhbN	D latch, active-high enable, preset & clear (0,1,2,3)
lablbN	D latch, active-low enable, preset & clear (0,1,2,3)
lanhbN	D latch, active-high enable (0,1,2,3)
lanlbN	D latch, active-low enable (0,1,2,3)
lachbN	D latch, active-high enable, clear (0,1,2,3)
laclbN	D latch, active-low enable, clear (0,1,2,3)
laphbN	D latch, active-high enable, preset (0,1,2,3)
laplbN	D latch, active-low enable, preset (0,1,2,3)

SCAN FLIP FLOPS

sdanrqN	Pos.Edge Scan DFF, Q only (0,1,2,4,8) with NAND D0,D1 input data
sdbrbN	Pos.Edge Scan DFF, active-low set and clear (0,1,2,m)
sdbfbN	Neg.Edge Scan DFF, active-low set and clear (0,1,2)
sdbrqN	Pos.Edge Scan DFF, active-low set and clear, Q only (0,1,2)
sdcfbN	Neg.Edge Scan DFF, active-low clear (0,1,2)
sdcrbN	Pos.Edge Scan DFF, active-low clear (0,1,2,m)
sdcrqN	Pos.Edge Scan DFF, active-low clear, Q only (0,1,2,m)
sdmnrqN	Pos.Edge Scan DFF, Q only (0,1,2,4,8) With selected input Data D0,D1
sdnfbN	Neg.Edge Scan DFF(0,1,2)
sdnfqN	Neg.Edge Scan DFF, Q only (0,1,2)
sdnrbN	Pos.Edge Scan DFF (0,1,2)
sdnrqN	Pos.Edge Scan DFF, Q only (0,1,2)

sdpfbN	Neg.Edge Scan DFF, active-low preset (0,1,2)
sdprbN	Pos.Edge Scan DFF, active-low preset (0,1,2)
sdprqN	Pos.Edge Scan DFF, active-low preset ,Q only(0,1,2,m)
sdscrqN	Pos.Edge Scan synchronous DFF, clear, Q only (0,1,2)
senrqN	Pos.Edge Scan DFF, active-high enable ,Q only (0,1,2)

CLOCK GATE

tlatncadN	Positive edge-triggered clock-gating latch(0,1,2,4)
tlatnfcadN	Neg. edge-triggered clock-gating latch(0,1,2,4)
tlatntscadN	Positive edge-triggered clock-gating latch, with enable pin (0,1,2,4)
tlatnftscadN	Neg edge-triggered clock-gating latch, with enable pin (0,1,2,4)

MISCELLANEOUS

antenna	Antenna Diode
bh01dN	Three-state bus holder(1)
fillerN	Filler cell(1,2,3,4,6,8,16,32,64)
tiehi	Drives the output (Y) to Logic High
tielo	Drives the output (Y) to Logic Low
fillcapN	Decoupling cell(1,2,3,4,6,8,16,32,64)
fillersub	Tap cell
invod8d1	inv with 8 open drain
nd02od	Nand2 with open drain
nd03od	Nand3 with open drain
or02od	Or2 with open drain
pullu	Internal pull up with enable input pin E
pulld	Internal pull down with enable input pin EN

Library Cell List For PMK

drf…… Retention DFF

gpg……Always on

head……Power switch

iso……isolation cells

sdr……Retention Scan DFF

PMK Cells listed below:

Power Gating

headN	Power switch cells

Isolation cell

isohdN	h default “1” in isolation mode(1,2,4,m)
isoldN	l default “1” in isolation mode(1,2,4,m)

Always on

gpgbuffdN	Always on buffer (2,4,8,16,32)
gpgbuffdN	Always on inv (2,4,8,16,32)

Retention Flip Flop

drfcrbN	Pos. Edge retention DFF, with reset (0,1,2,m)
drfnrbN	Pos. Edge retention DFF(0,1,2,m)
drfprbN	Pos. Edge DFF, with set (0,1,2,m)

Retention Flip Flop with Scan

sdrcrbN	Pos. Edge retention DFF, with reset (0,1,2,m)
sdrnrbN	Pos. Edge retention DFF(0,1,2,m)
sdrprbN	Pos. Edge DFF, with set (0,1,2,m)

Appendix A: Techfile Layers

Layer Name	Cadence Layer Name	Cadence Purpose	GDS II Layer Number	GDS Data Type	Description
TB	TB	drawing	1	0	P-channel LV device substrate and symmetric HVNMOS drift region, Nwell layer
Active	TO	drawing	2	0	Diffusion and channel area
Poly	GT	drawing	3	0	Poly1
P+	SP	drawing	4	0	P+ implant
N+	SN	drawing	5	0	N+ implant
Contact	W1	drawing	6	0	Contact
A1	A1	drawing	7	0	Metal 1
W2	W2	drawing	8	0	Via1
A2	A2	drawing	9	0	Metal 2
W3	W3	drawing	40	0	Via2
A3	A3	drawing	41	0	Metal 3
W4	W4	drawing	61	0	Via3
A4	A4	drawing	62	0	Metal 4
W5	W5	drawing	91	0	Via4
A5	A5	drawing	92	0	Metal 5
Top Via	WT	drawing	93	0	Top via WT
Top Metal	AT	drawing	94	0	Top metal
VIA5	W6	drawing	95	0	VIA5
Metal6	A6	drawing	96	0	Metal6
VIA6	W7	drawing	97	0	VIA6
Metal7	A7	drawing	98	0	Metal7
DIODE	DIODE	mark	113	1	Diode marker
A1TEXT	A1TEXT	drawing	121	0	Metal 1 text
A2TEXT	A2TEXT	drawing	122	0	Metal 2 text
A3TEXT	A3TEXT	drawing	123	0	Metal 3 text
A4TEXT	A4TEXT	drawing	124	0	Metal 4 text
A5TEXT	A5TEXT	drawing	125	0	Metal 5 text
ATTEXT	ATTEXT	drawing	126	0	Top metal text