SMIC 40nm Low Leakage HS RVT Logic Process Standard Cell Library Databook V0.2

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Semiconductor Manufacturing International Corporation
No. 18 Zhangjiang Road
Pudong New Area
Shanghai, 201203
People's Republic of China

Revision History

This document contains the release history for SMIC 40nm low leakage HS RVT Process Standard Cell Library Databook.

IP Code	Release Version	Date of Release	Update Description
SCC40NLL_HS_RVT	0.0	Oct, 2010	Initial Release
SCC40NLL_HS_RVT	0.1	May, 2011	Update Release： New spice model
SCC40NLL_HS_RVT	0.2	Oct, 2012	Update Release： 1, Enrich cell functions 2, Improve cell performance 3,Optimize cell physical layout 4, New spice model (1.41r)

Table of Contents

Introduction

SMIC's standard cell library is custom-designed and tested to provide the optimum combination of high-performance and high-density cells. Cell optimization is derived from extensive internal and external custom designs and place-and-route analysis; whereas, library optimization is characterized by thorough simulation of library functions and of various drive strengths using leading simulation and place-and-route tools to produce superior GDSII results.

Organization of the databook

The introduction is organized into several sections:

1. Global Parameters provides library overview and some general specifications.
2. Timing Constraint describes what type of timing specification is measured from each cell.
3. Naming Conventions provides standard cells' name conventions.
4. Special Cells defines the various types of special cells in the library.
5. Standard Cell Library Interpretation explains the components in each of the datasheets.

Global Parameters

This section defines the general specifications for the SMIC 40nm Low Leakage HS RVT Process Standard Cell Library. It includes physical cell specifications, electrical specifications, propagation delay specifications, timing specifications, and power calculation.

Physical Cell Specifications

Table 1. shows the physical design cell specification for this standard cell library.

Table 1. Physical Cell Specification

Drawn Gate Length (um)	0.04
Number of Layers of Metal	6,7,8,9 or 10
Layout Grid (um)	0.005
Vertical Pin Grid (um)	0.14n+0.07
Horizontal Pin Grid (um)	0.14n+0.07
Cell power and Ground Rail Width (um)	0.14
Cell Height (um)	1.26
N-well and substrate distance	10.0

Where n is positive integer value. All pins are located with a 0.07um offset to vertical and horizontal pin grids, making place-and-route tools much more efficient.

Note

The library supports designs with six, seven, eight, nine, or ten layers of metal. For different layers of top-level metal, it is possible that a change in the design rules description within the technology file is required, because the top metal has greater minimum width, minimum spacing, and minimum area requirements. Please refer to "40nm Logic Salicide 0.9/1.1/1.2/1.8/2.5V Low Leakage and Generic Design Rule" for more information. It is crucial to define these rules correctly within the technology file for the place-and-route tool to function properly.

Table 2. lists the electrical specifications for this standard cell library.

Table 2. Electrical Specifications

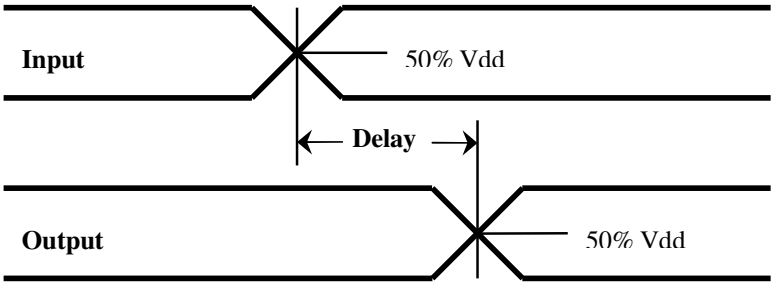
Corners	Best Low Temp	Best High Temp	Best: Zero Temp	Typical	Typical High Temp	Worst Low Temp	Worst High Temp
Supply Voltage (V)	1.21	1.21	1.21	1.10	1.10	0.99	0.99
Junction Temperature (°C)	-40	125	0	25	125	-40	125

Timing Constrains

Propagation Delay and Transition Time

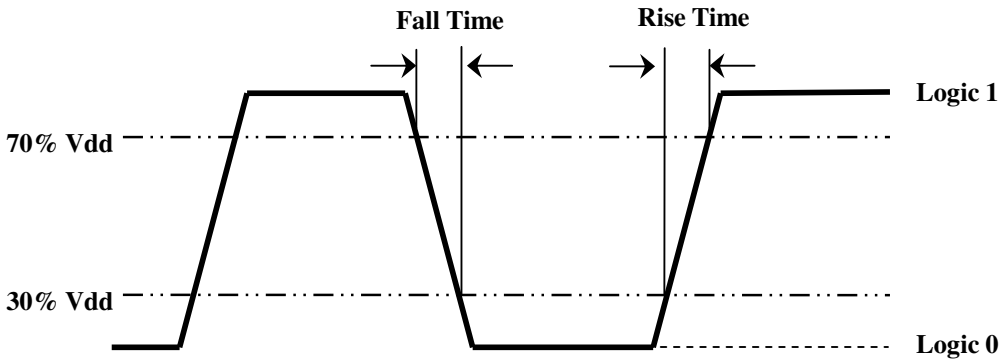
Propagation delay is the sum of the intrinsic delay, the load delay, and the input-slew delay of a cell. Delays are defined as the time interval between the input stimulus and output crossing 50% of the Vdd value. The propagation delay is illustrated in Figure 1. below.

Figure 1. Propagation Delay



Transition time or slew rate is defined as the time interval between crossings of 30% to 70% of Vdd value on a signal. Transition time is shown in Figure 2. for both rising and falling signals.

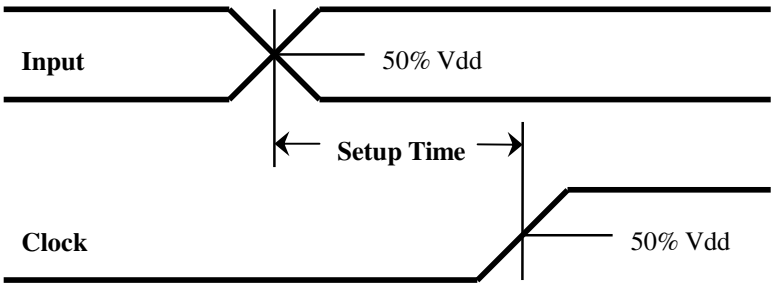
Figure 2. Transition Time



Setup Time

Setup time for a sequential cell is the minimum period of time the data signal must remain stable before the active edge of the clock (or another specified signal) to ensure correct function at the output. Setup constraint values are measured as the interval between the data signal crossing 50% of Vdd for rising or falling data and the clock signal crossing 50% of Vdd for rising or falling clocks. For measurement of setup time, the data signal is kept stable indefinitely after the clock edge. Definition of setup time for a positive-edge triggered sequential cell is shown in Figure 3.

Figure 3. Setup Time

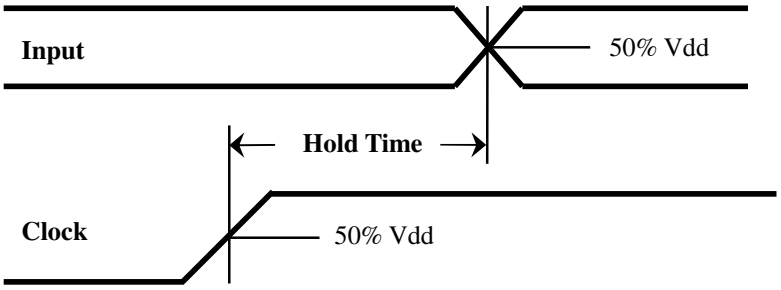


Hold Time

Hold time for a sequential cell is the minimum period of time the data signal must remain stable after the active edge of the clock (or another specified signal) to ensure correct function at the output. Hold constraint values are measured as the interval between the data signal crossing 50% of Vdd value and the clock signal crossing 50% of Vdd for either rise or fall transitions on both signals. For measurement of hold time, the data signal is kept stable indefinitely before the clock

edge. Definition of fall time for a positive-edge triggered sequential cell is shown in Figure 4.

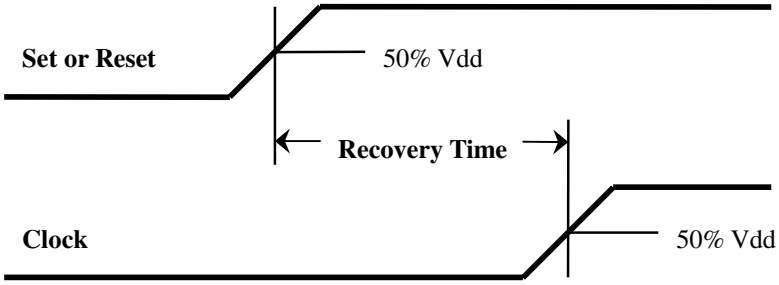
Figure 4. Hold Time



Recovery Time

Recovery time for sequential cell is the minimum length of time that the active-low set or reset signal must remain high before the active edge of the clock to ensure correct cell function. Recovery constraint value is measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd for rising or falling clocks. For measurement of recovery time, the set or reset signal is held stable indefinitely after the clock edge. Definition of recovery time is shown below in Figure 5.

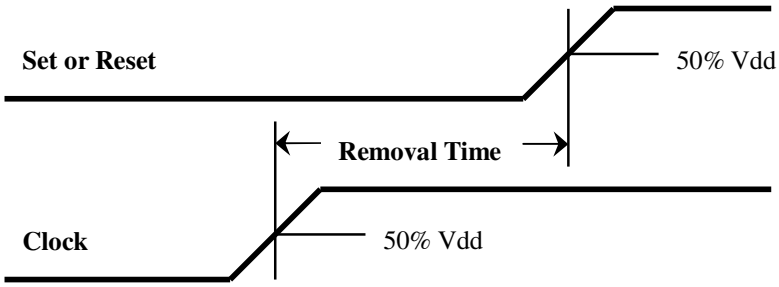
Figure 5. Recovery Time



Removal Time

Removal time for sequential cell is the minimum length of time that the set or reset signals must remain low after the active edge of the clock to ensure correct cell function. Removal constraint value is measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd for rising or falling clocks. For measurement of removal time, the set or reset signal is held stable indefinitely before the clock edge. Definition of removal time is shown in Figure 6.

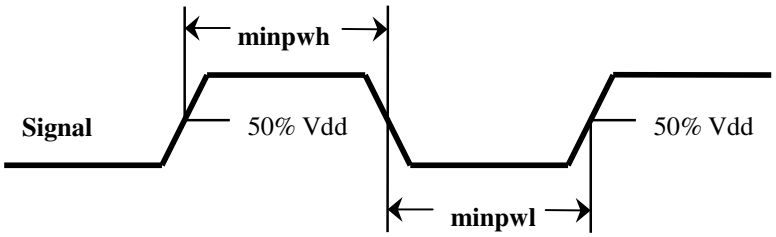
Figure 6. Removal Time



Minimum Pulse Width

Minimum pulse width is the minimum period of time between the leading the trailing edges of a pulse waveform. Minimum pulse width high (minpwh) is measured as the interval between the rising edge of signal crossing 50% of Vdd and the falling edge of signal crossing 50% of Vdd. Minimum pulse width low (minpwl) is measured as the interval between the falling edge of signal crossing 50% of Vdd and the rising edge of signal crossing 50% of Vdd. Minimum pulse width is illustrated in Figure 7.

Figure 7. Minimum Pulse Width



Naming Conventions

This section provides the naming convention for SMIC 40nm Low Leakage Process HS RVT Standard Cell Library.
The syntax is: **<Cell Type><Options> <library family> <Drive Selection>**

Example:

AND2HSV1: AND is Cell Type, 2 is the number of inputs, HS is High-Speed library and V1 is driving strength.

Cell Type	Description	Options
INV	Inverter cell	CKINV :Inverting Clock Inverter TINV: Tri-state inverter
BUF	Buffer cell	CLKBUF: Clock buffer TBUF: Tri-state buffer

AND	AND cell	2/3/4: The number of input pins
NAND	NAND cell	2/3/4: The number of input pins
I2NAND	NAND cell	3/4: with 2 Inverted Inputs
OR	OR cell	2/3/4: The number of input pins
NOR	NOR cell	2/3/4: The number of input pins
AO	AND-OR cell	21/211/221: The number of AND groups and additional inputs
OA	OR-AND cell	21/211/221: The number of OR groups and additional inputs
AOI	AND-OR-Inverter cell	21/211/221: The number of AND groups and additional inputs
OAI	OR-AND-Inverter cell	21/211/221: The number of OR groups and additional inputs
XOR	Exclusive OR cell	2/3:The number of input pins
XNOR	Exclusive NOR cell	2/3:The number of input pins
DEL	Delay cell	1/2/3/4: Delay class
AC	Full adder carry-generator	AC1CIN:with active low carry-in (CIN) AC1CON: with carry in (CI)
AD	Full adder cell	AD1CSCIN: with CO and CIN AD1CON: with CON and CI AD2 provides a carry-select adder function
ADH	Half adder cell	ADH1CIN with CO and CIN ADH1CON with CON and CI
MUX	Multiplexer cell	2/4:The number of input pins N: Inverted
D	Flip-Flop cell	SD: D flip-flop with scan ED: D flip-flop with enable SED: D flip-flop with scan enable DN: Negative edge clock trigger DQ: Output Q only DG: With synchronous (Reset/Set) S: Set R: Reset X: Mux Inputs
LA	Transparent Latch cell	L: Active low enable H: Active high enable CLKLA: Clock-gating latch R: Reset S: Set T: Tri-state transparent latch
HOLD	Weak bus holder	

All cells' names must be in upper case. For flip-flop cells, the default is:

Positive edge clock trigger

Asynchronous Set or Reset

With Q and QN

For latch cells, the default is:

Active high enable

Asynchronous Set or Reset

Special Cells

This section discusses the special cell types within the SMIC Standard Cell Library.

De-CAP Cells

The standard cell library includes 5 De-CAP cells: FDCAPHS4, FDCAPHS8, FDCAPHS16, FDCAPHS32 and FDCAPHS64. De-CAP is composed of a PMOS and NMOS device to form decoupling capacitors between V_{DD} and V_{SS} rails so as to reduce the voltage bounce on the power rails. The De-CAP functional schematic is shown in Figure 8. below.

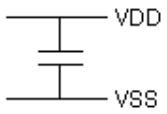


Figure 8. De-CAP Functional Schematic

FILL Cells

The standard cell library includes 5 FILL cells, namely: F_FILLHS1, F_FILLHS2, F_FILLHS4, F_FILLHS8 and F_FILLHS16. The number denoted at the end of the cell names represents the width of the cell measured in number of tracks.

The FILL cells are used to connect power and ground rails across an area with no cells during place and route. It is used to ensure that gaps do not occur between well or implant layers which in some cases can cause DRC violations.

PULL0/1 Cells

The PULLHS0 and PULLHS1 cells provide ESD protection of signal inputs from power and ground rails. These cells provide diffusion-driven inputs for signal pins. If these cells are not used and Via(s) are dropped on the power rails, DRC error or shorts may occur. Any input pin that will be preset to 0/1 need connect PULLHS0 / PULLHS1 cell rather than VSS/VDD.

NWELL and Substrate Tie Cells

The standard cell library contains one NWELL/Substrate Tie Cell: FILLTIEHS. This standard cell library does not have well or substrate ties inside the cells. It is required to tie NWell to VDD and substrate to VSS before place-and-route using the FILLTIEHS cells. It is also required to place the Tie cells as frequent as the design requires. Figures 9 and 10 illustrate the two FILLTIEHS cell orientations within the library.

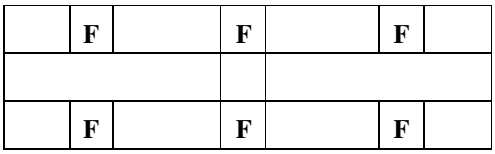


Figure 9. Normal placement of FILLTIE cells

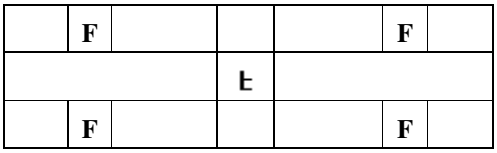


Figure 10. Flipped placement of FILLTIE cells

Figure 9 shows that normal placement of FILLTIEHS cells requires tie cells be placed every 20um. The accurate data please refer to "40nm Logic Salicide 0.9/1.0/1.1/1.2/1.8/2.5V Low leakage and generic ESD and Latch-up Guidelines". All rows except for the top and bottom two have their VDD and VSS shared between the adjacent rows, allowing for wider placement of FILLTIEHS cells when the cells of alternating rows are placed with an offset, as illustrated above in Figure 10. An example of this would be that the design rule specifies FILLTIEHS cells every 20um apart; however, with offset for alternating rows, FILLTIEHS cells can be placed every 40um apart with the exception of the top and bottom rows.

Antenna Cells

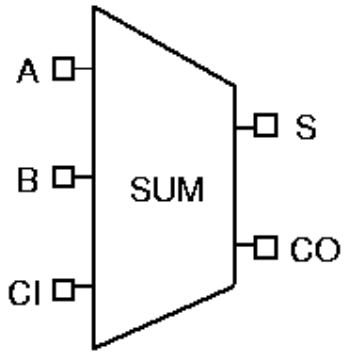
The standard cell library contains 3 F_DIODE cells: F_DIODEHS2, F_DIODEHS4 and F_DIODEHS8. The SMIC antenna effect prevention guideline within the "40nm LOGIC Antenna Ration Effect Generic Prevention Design Guide Rule" specifies the maximum length of wire allowed within the library. During place-and-route, the router may connect wires to the input gates of cells that are longer than the maximum length allowed. In this case, antenna cells can be placed on these inputs. Pin A on the antenna cell connects to two diodes, one reversed-biased from Pin A to ground and another from VDD to Pin A. The Antenna cells will need to be placed manually; fortunately, most place-and-route tools will indicate which nets will require the insertion of these cells.

Standard Cell Datasheet

AD1HS

Cell Description

1-Bit Full Adder
CO=((A&B)|(A&CI)|(B&CI))
S=(A^B^CI)



Function Table

A	B	CI	CO	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
AD1HSV1	1.26	5.04

Pin Power (uW/MHz)

Pin	V1
A	0.00309
B	0.00248
CI	0.00102

Pin Capacitance (pf)

Pin	V1
A	0.00119
B	0.00176
CI	0.00200

Max Leakage Power (uW)

V1
0.00099842

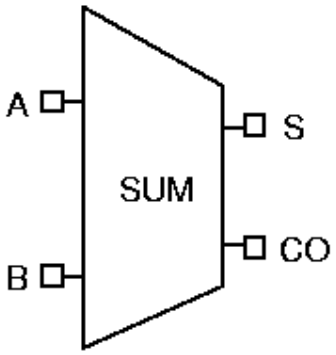
Delay Table (ns)

Description	V1
A→CO_FALL	0.09952
A→CO_RISE	0.08777
B→CO_FALL	0.08991
B→CO_RISE	0.07428
CI→CO_FALL	0.05180
CI→CO_RISE	0.04504
A→S_FALL	0.12773
A→S_RISE	0.12355
B→S_FALL	0.10390
B→S_RISE	0.09885
CI→S_FALL	0.04608
CI→S_RISE	0.04314

ADH1HS

Cell Description

1-Bit Half Adder
CO=(A&B)
S=(A^B)



Function Table

B	A	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Size

CellName	Height(um)	Width(um)
ADH1HSV1	1.26	2.94

Pin Power (uW/MHz)

Pin	V1
A	0.00159
B	0.00104

Pin Capacitance (pf)

Pin	V1
A	0.00112
B	0.00174

Max Leakage Power (uW)

V1
0.00077090

Delay Table (ns)

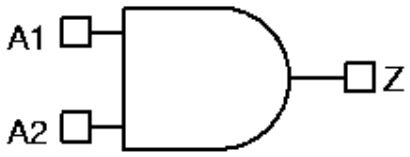
Description	V1
A→CO_FALL	0.02803
A→CO_RISE	0.03501

B→CO_FALL	0.02730
B→CO_RISE	0.03386
A→S_FALL	0.07637
A→S_RISE	0.06767
B→S_FALL	0.04859
B→S_RISE	0.04558

AND2HS

Cell Description

2-Input AND
Z=(A1&A2)



Function Table

A1	A2	Z
0	X	0
1	0	0
1	1	1

Cell Size

CellName	Height(um)	Width(um)
AND2HSV1	1.26	0.84
AND2HSV2	1.26	0.84
AND2HSV4	1.26	0.98
AND2HSV8	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2	V4	V8
A1	0.00062	0.00071	0.00103	0.00189
A2	0.00067	0.00076	0.00109	0.00197

Pin Capacitance (pf)

Pin	V1	V2	V4	V8
A1	0.00048	0.00048	0.00047	0.00066
A2	0.00047	0.00048	0.00047	0.00066

Max Leakage Power (uW)

V1	V2	V4	V8
0.00020273	0.00021474	0.00031150	0.00078619

Delay Table (ns)

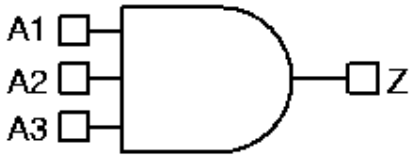
Description	V1	V2	V4	V8

A1→Z_FALL	0.03352	0.03402	0.04042	0.03706
A1→Z_RISE	0.04151	0.04207	0.04918	0.04435
A2→Z_FALL	0.03614	0.03668	0.04277	0.03840
A2→Z_RISE	0.04483	0.04556	0.05248	0.04696

AND3HS

Cell Description

3-Input AND
Z=(A1&A2&A3)



Function Table

A1	A2	A3	Z
0	X	X	0
1	0	X	0
1	1	0	0
1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
AND3HSV1	1.26	0.98
AND3HSV2	1.26	0.98
AND3HSV4	1.26	1.12
AND3HSV8	1.26	1.54

Pin Power (uW/MHz)

Pin	V1	V2	V4	V8
A1	0.00075	0.00083	0.00114	0.00201
A2	0.00080	0.00088	0.00120	0.00208
A3	0.00088	0.00096	0.00128	0.00217

Pin Capacitance (pf)

Pin	V1	V2	V4	V8
A1	0.00052	0.00052	0.00051	0.00064
A2	0.00054	0.00053	0.00054	0.00066
A3	0.00054	0.00053	0.00054	0.00068

Max Leakage Power (uW)

V1	V2	V4	V8
0.00029084	0.00030126	0.00039303	0.00089119

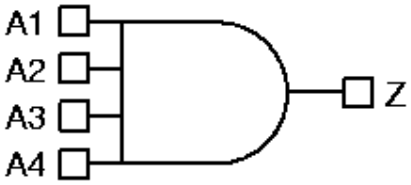
Delay Table (ns)

Description	V1	V2	V4	V8
A1→Z_FALL	0.03947	0.03985	0.04548	0.03908
A1→Z_RISE	0.04427	0.04404	0.04915	0.06214
A2→Z_FALL	0.04205	0.04181	0.04761	0.03988
A2→Z_RISE	0.04730	0.04697	0.05222	0.06529
A3→Z_FALL	0.04566	0.04528	0.05110	0.04193
A3→Z_RISE	0.05049	0.05002	0.05525	0.06828

AND4HS

Cell Description

4-Input AND
Z=(A1&A2&A3&A4)



Function Table

A1	A2	A3	A4	Z
0	X	X	X	0
1	0	X	X	0
1	1	0	X	0
1	1	1	0	0
1	1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
AND4HSV1	1.26	1.12
AND4HSV2	1.26	1.12
AND4HSV4	1.26	1.26
AND4HSV8	1.26	1.68

Pin Power (uW/MHz)

Pin	V1	V2	V4	V8
A1	0.00077	0.00086	0.00117	0.00211
A2	0.00085	0.00094	0.00125	0.00218
A3	0.00091	0.00100	0.00131	0.00224
A4	0.00100	0.00108	0.00139	0.00233

Pin Capacitance (pf)

Pin	V1	V2	V4	V8
A1	0.00053	0.00053	0.00053	0.00064
A2	0.00057	0.00057	0.00057	0.00069
A3	0.00055	0.00055	0.00054	0.00065
A4	0.00056	0.00056	0.00056	0.00068

Max Leakage Power (uW)

V1	V2	V4	V8
0.00036611	0.00038108	0.00046866	0.00109091

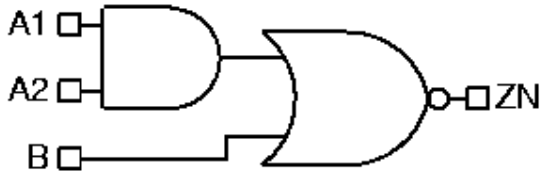
Delay Table (ns)

Description	V1	V2	V4	V8
A1→Z_FALL	0.04132	0.04179	0.04727	0.04021
A1→Z_RISE	0.05016	0.05061	0.05591	0.07994
A2→Z_FALL	0.04460	0.04496	0.04992	0.04143
A2→Z_RISE	0.05553	0.05594	0.06127	0.08534
A3→Z_FALL	0.04737	0.04778	0.05239	0.04254
A3→Z_RISE	0.05845	0.05889	0.06395	0.08800
A4→Z_FALL	0.05129	0.05176	0.05628	0.04445
A4→Z_RISE	0.06209	0.06245	0.06761	0.09177

AOI21HS

Cell Description

2-1 AOI
ZN=(!((A1&A2)|B))



Function Table

A1	A2	B	ZN
0	X	0	1
0	X	1	0
1	0	0	1
1	0	1	0
1	1	X	0

Cell Size

CellName	Height(um)	Width(um)
AOI21HSV1	1.26	0.84
AOI21HSV2	1.26	0.84

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00040	0.00050
A2	0.00045	0.00056
B	0.00026	0.00033

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00053	0.00064
A2	0.00056	0.00068
B	0.00051	0.00061

Max Leakage Power (uW)

V1	V2
0.00015243	0.00018216

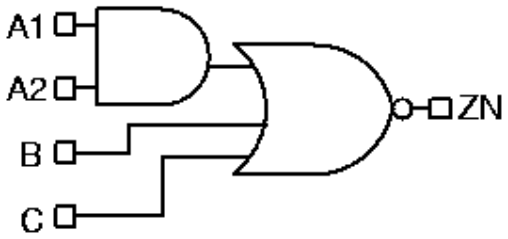
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.02131	0.01893
A1→ZN_RISE	0.03147	0.02792
A2→ZN_FALL	0.02298	0.02057
A2→ZN_RISE	0.03435	0.03102
B→ZN_FALL	0.01145	0.01028
B→ZN_RISE	0.02381	0.02112

AOI211HS

Cell Description

2-1-1 AOI
ZN=(!((A1&A2)|B|C))



Function Table

A1	A2	B	C	ZN
0	X	0	0	1
0	X	0	1	0
0	X	1	X	0
1	0	0	0	1
1	0	0	1	0
1	0	1	X	0
1	1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
AOI211HSV1	1.26	0.98
AOI211HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00052	0.00064
A2	0.00057	0.00071
B	0.00038	0.00047
C	0.00032	0.00038

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00053	0.00064
A2	0.00057	0.00069
B	0.00056	0.00066
C	0.00050	0.00059

Max Leakage Power (uW)

V1	V2
0.00022419	0.00026920

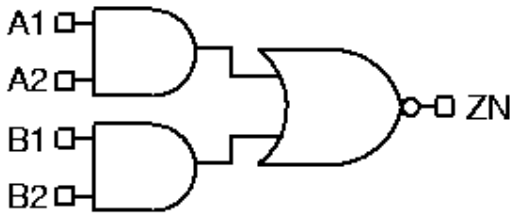
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.02364	0.02065
A1→ZN_RISE	0.05200	0.04589
A2→ZN_FALL	0.02535	0.02255
A2→ZN_RISE	0.05668	0.05119
B→ZN_FALL	0.01319	0.01183
B→ZN_RISE	0.04395	0.03908
C→ZN_FALL	0.01235	0.01093
C→ZN_RISE	0.03926	0.03384

AOI22HS

Cell Description

2-2 AOI
ZN=(!((A1&A2)|(B1&B2)))



Function Table

A1	A2	B1	B2	ZN
0	X	0	X	1
0	X	1	0	1
0	X	1	1	0
1	0	0	X	1
1	0	1	0	1
1	0	1	1	0
1	1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
AOI22HSV1	1.26	0.98
AOI22HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00051	0.00064
A2	0.00056	0.00071
B1	0.00028	0.00036
B2	0.00033	0.00042

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00053	0.00063
A2	0.00056	0.00067
B1	0.00052	0.00062
B2	0.00051	0.00061

Max Leakage Power (uW)

V1	V2
0.00024291	0.00032057

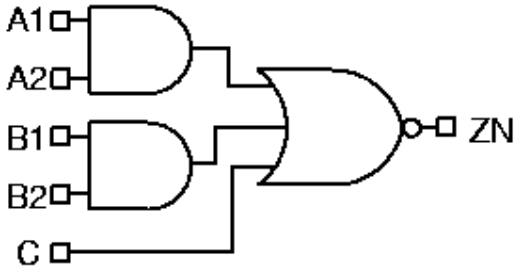
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.02380	0.02142
A1→ZN_RISE	0.03408	0.03070
A2→ZN_FALL	0.02553	0.02333
A2→ZN_RISE	0.03726	0.03409
B1→ZN_FALL	0.01793	0.01595
B1→ZN_RISE	0.02387	0.02117
B2→ZN_FALL	0.01957	0.01760
B2→ZN_RISE	0.02688	0.02416

AOI221HS

Cell Description

2-2-1 AOI
ZN=(!((A1&A2)|(B1&B2)|C))



Function Table

A1	A2	B1	B2	C	ZN
0	X	0	X	0	1
0	X	0	X	1	0
0	X	1	0	0	1
0	X	1	0	1	0
0	X	1	1	X	0
1	0	0	X	0	1
1	0	0	X	1	0
1	0	1	0	0	1
1	0	1	0	1	0
1	0	1	1	X	0
1	1	X	X	X	0

Cell Size

CellName	Height(um)	Width(um)
AOI221HSV1	1.26	1.26
AOI221HSV2	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00066	0.00083
A2	0.00070	0.00090
B1	0.00047	0.00060
B2	0.00053	0.00067
C	0.00034	0.00043

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00054	0.00064
A2	0.00056	0.00067

B1	0.00053	0.00063
B2	0.00052	0.00062
C	0.00051	0.00061

Max Leakage Power (uW)

V1	V2
0.00020423	0.00024605

Delay Table (ns)

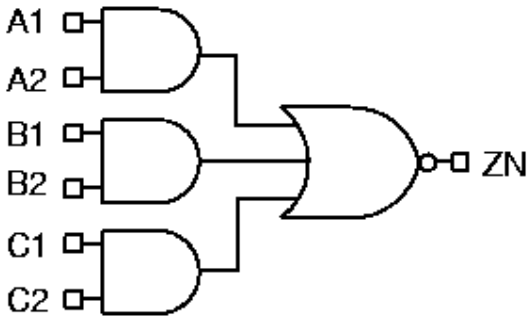
Description	V1	V2
A1→ZN_FALL	0.02552	0.02282
A1→ZN_RISE	0.06082	0.05539
A2→ZN_FALL	0.02721	0.02477
A2→ZN_RISE	0.06599	0.06110
B1→ZN_FALL	0.02320	0.02080
B1→ZN_RISE	0.05236	0.04728
B2→ZN_FALL	0.02534	0.02289
B2→ZN_RISE	0.05852	0.05343
C→ZN_FALL	0.01277	0.01154
C→ZN_RISE	0.03922	0.03492

AOI222HS

Cell Description

2-2-2 AOI

ZN=(!((A1&A2)|(B1&B2)|(C1&C2)))



Function Table

A1	A2	B1	B2	C1	C2	ZN
0	X	0	X	0	X	1
0	X	0	X	1	0	1
0	X	0	X	1	1	0
0	X	1	0	0	X	1
0	X	1	0	1	0	1
0	X	1	0	1	1	0
0	X	1	1	X	X	0
1	0	0	X	0	X	1
1	0	0	X	1	0	1
1	0	0	X	1	1	0
1	0	1	0	0	X	1
1	0	1	0	1	0	1
1	0	1	0	1	1	0
1	0	1	1	X	X	0
1	1	X	X	X	X	0

Cell Size

CellName	Height(um)	Width(um)
AOI222HSV1	1.26	1.54
AOI222HSV2	1.26	1.54

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00037	0.00046
A2	0.00041	0.00051
B1	0.00058	0.00073
B2	0.00063	0.00079
C1	0.00076	0.00095
C2	0.00081	0.00102

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00050	0.00060
A2	0.00050	0.00060
B1	0.00055	0.00065
B2	0.00052	0.00061
C1	0.00053	0.00062
C2	0.00055	0.00067

Max Leakage Power (uW)

V1	V2
0.00021177	0.00025473

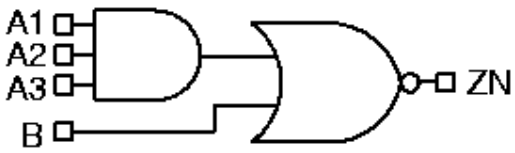
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.02047	0.01789
A1→ZN_RISE	0.03871	0.03387
A2→ZN_FALL	0.02159	0.01930
A2→ZN_RISE	0.04146	0.03730
B1→ZN_FALL	0.02625	0.02335
B1→ZN_RISE	0.05687	0.05124
B2→ZN_FALL	0.02802	0.02515
B2→ZN_RISE	0.06204	0.05659
C1→ZN_FALL	0.02835	0.02524
C1→ZN_RISE	0.06485	0.05897
C2→ZN_FALL	0.03016	0.02718
C2→ZN_RISE	0.06970	0.06421

AOI31HS

Cell Description

3-1 AOI
ZN=(!((A1&A2&A3)|B))



Function Table

A1	A2	A3	B	ZN
0	X	X	0	1
0	X	X	1	0
1	0	X	0	1
1	0	X	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	X	0

Cell Size

CellName	Height(um)	Width(um)
AOI31HSV1	1.26	0.98
AOI31HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00042	0.00051
A2	0.00046	0.00058
A3	0.00051	0.00064
B	0.00028	0.00033

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00056	0.00064
A2	0.00056	0.00066
A3	0.00056	0.00069
B	0.00051	0.00060

Max Leakage Power (uW)

V1	V2
0.00021034	0.00027524

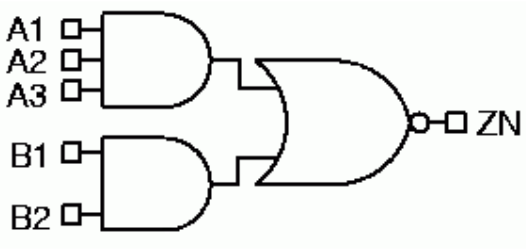
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.03021	0.02619
A1→ZN_RISE	0.03205	0.02796
A2→ZN_FALL	0.03296	0.02950
A2→ZN_RISE	0.03483	0.03122
A3→ZN_FALL	0.03437	0.03090
A3→ZN_RISE	0.03772	0.03399
B→ZN_FALL	0.01151	0.01020
B→ZN_RISE	0.02299	0.02003

AOI32HS

Cell Description

3-2 AOI
ZN=(!((A1&A2&A3)|(B1&B2)))



Function Table

A1	A2	A3	B1	B2	ZN
0	X	X	0	X	1
0	X	X	1	0	1
0	X	X	1	1	0
1	0	X	0	X	1
1	0	X	1	0	1
1	0	X	1	1	0
1	1	0	0	X	1
1	1	0	1	0	1
1	1	0	1	1	0
1	1	1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
AOI32HSV1	1.26	1.12
AOI32HSV2	1.26	1.12

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00050	0.00064
A2	0.00056	0.00072
A3	0.00060	0.00077
B1	0.00030	0.00037
B2	0.00035	0.00044

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00054	0.00064
A2	0.00060	0.00072
A3	0.00058	0.00069

B1	0.00052	0.00065
B2	0.00051	0.00059

Max Leakage Power (uW)

V1	V2
0.00023996	0.00032740

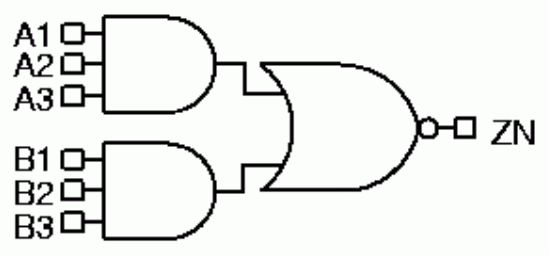
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.03346	0.02992
A1→ZN_RISE	0.03389	0.03046
A2→ZN_FALL	0.03686	0.03373
A2→ZN_RISE	0.03701	0.03386
A3→ZN_FALL	0.03818	0.03495
A3→ZN_RISE	0.04014	0.03675
B1→ZN_FALL	0.01793	0.01587
B1→ZN_RISE	0.02296	0.02031
B2→ZN_FALL	0.02011	0.01787
B2→ZN_RISE	0.02637	0.02338

AOI33HS

Cell Description

3-3 AOI
ZN=(!((A1&A2&A3)|(B1&B2&B3)))



Function Table

A1	A2	A3	B1	B2	B3	ZN
0	X	X	0	X	X	1
0	X	X	1	0	X	1
0	X	X	1	1	0	1
0	X	X	1	1	1	0
1	0	X	0	X	X	1
1	0	X	1	0	X	1
1	0	X	1	1	0	1
1	0	X	1	1	1	0
1	1	0	0	X	X	1
1	1	0	1	0	X	1
1	1	0	1	1	0	1
1	1	0	1	1	1	0
1	1	1	X	X	X	0

Cell Size

CellName	Height(um)	Width(um)
AOI33HSV1	1.26	1.40
AOI33HSV2	1.26	1.40

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00062	0.00078
A2	0.00067	0.00085
A3	0.00072	0.00091
B1	0.00038	0.00047
B2	0.00044	0.00055
B3	0.00049	0.00062

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00055	0.00065
A2	0.00061	0.00065
A3	0.00056	0.00067
B1	0.00052	0.00061
B2	0.00052	0.00061
B3	0.00052	0.00061

Max Leakage Power (uW)

V1	V2
0.00039042	0.00051250

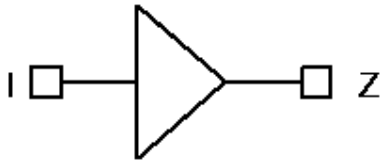
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.03913	0.03515
A1→ZN_RISE	0.03711	0.03342
A2→ZN_FALL	0.04221	0.03830
A2→ZN_RISE	0.03984	0.03623
A3→ZN_FALL	0.04354	0.03968
A3→ZN_RISE	0.04241	0.03876
B1→ZN_FALL	0.02777	0.02428
B1→ZN_RISE	0.02585	0.02283
B2→ZN_FALL	0.03198	0.02846
B2→ZN_RISE	0.02933	0.02626
B3→ZN_FALL	0.03354	0.03000
B3→ZN_RISE	0.03189	0.02873

BUFHS

Cell Description

Non-Inverting Buffer
Z=I



Function Table

I	Z
0	0
1	1

Cell Size

CellName	Height(um)	Width(um)
BUFHSV1	1.26	0.56
BUFHSV2	1.26	0.56
BUFHSV3	1.26	0.84
BUFHSV4	1.26	0.84
BUFHSV6	1.26	0.98
BUFHSV8	1.26	1.26
BUFHSV12	1.26	1.82
BUFHSV16	1.26	2.24
BUFHSV20	1.26	2.80
BUFHSV24	1.26	3.36

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
I	0.00061	0.00070	0.00091	0.00108	0.00154	0.00195	0.00293	0.00378

Pin	V20	V24
I	0.00468	0.00565

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
I	0.00049	0.00049	0.00053	0.00057	0.00067	0.00112	0.00155	0.00178

Pin	V20	V24
I	0.00239	0.00294

Max Leakage Power (uW)

V1	V2	V3	V4	V6	V8	V12	V16
0.00012705	0.00014264	0.00031998	0.00037610	0.00057425	0.00084329	0.00137394	0.00187471

V20	V24
0.00245036	0.00299142

Delay Table (ns)

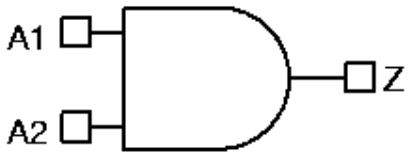
Description	V1	V2	V3	V4	V6	V8	V12	V16
I→Z_FALL	0.03340	0.03428	0.03198	0.03002	0.03250	0.02621	0.02624	0.02704
I→Z_RISE	0.02948	0.02943	0.02632	0.02537	0.02636	0.02225	0.02196	0.02218

Description	V20	V24
I→Z_FALL	0.02553	0.02529
I→Z_RISE	0.02115	0.02100

CLKAND2HS

Cell Description

2-Input Clock AND
Z=(A1&A2)



Function Table

A1	A2	Z
0	X	0
1	0	0
1	1	1

Cell Size

CellName	Height(um)	Width(um)
CLKAND2HSV1	1.26	0.84
CLKAND2HSV2	1.26	0.84
CLKAND2HSV4	1.26	1.12
CLKAND2HSV8	1.26	1.68

Pin Power (uW/MHz)

Pin	V1	V2	V4	V8
A1	0.00064	0.00074	0.00132	0.00238
A2	0.00073	0.00082	0.00140	0.00246

Pin Capacitance (pf)

Pin	V1	V2	V4	V8
A1	0.00056	0.00055	0.00054	0.00055
A2	0.00055	0.00055	0.00055	0.00055

Max Leakage Power (uW)

V1	V2	V4	V8
0.00019281	0.00022770	0.00054613	0.00115071

Delay Table (ns)

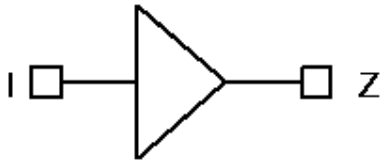
Description	V1	V2	V4	V8

A1→Z_FALL	0.03599	0.03662	0.04973	0.07277
A1→Z_RISE	0.02930	0.02903	0.03381	0.04697
A2→Z_FALL	0.04016	0.04099	0.05325	0.07563
A2→Z_RISE	0.03199	0.03170	0.03632	0.04945

CLKBUFHS

Cell Description

Clock Buffer with Balanced Rise/Fall Time
Z=I



Function Table

I	Z
0	0
1	1

Cell Size

CellName	Height(um)	Width(um)
CLKBUFHSV1	1.26	0.56
CLKBUFHSV2	1.26	0.56
CLKBUFHSV3	1.26	0.84
CLKBUFHSV4	1.26	0.84
CLKBUFHSV6	1.26	0.98
CLKBUFHSV8	1.26	1.26
CLKBUFHSV12	1.26	1.68
CLKBUFHSV16	1.26	2.24
CLKBUFHSV20	1.26	2.80
CLKBUFHSV24	1.26	3.08

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
I	0.00060	0.00068	0.00091	0.00106	0.00146	0.00175	0.00254	0.00328

Pin	V20	V24
I	0.00428	0.00492

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
I	0.00048	0.00049	0.00056	0.00061	0.00064	0.00092	0.00117	0.00154

Pin	V20	V24
I	0.00202	0.00220

Max Leakage Power (uW)

V1	V2	V3	V4	V6	V8	V12	V16
0.00012455	0.00014251	0.00034379	0.00040438	0.00057587	0.00075381	0.00130411	0.00169857

V20	V24
0.00220253	0.00266977

Delay Table (ns)

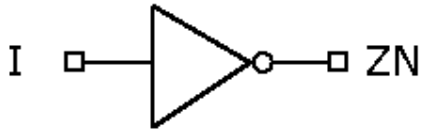
Description	V1	V2	V3	V4	V6	V8	V12	V16
I→Z_FALL	0.03447	0.03487	0.02925	0.02781	0.03202	0.02825	0.02790	0.02756
I→Z_RISE	0.02928	0.02892	0.02629	0.02406	0.02836	0.02588	0.02532	0.02677

Description	V20	V24
I→Z_FALL	0.02693	0.02789
I→Z_RISE	0.02640	0.02633

CLKNHS

Cell Description

Inverting Clock Buffer with Balanced Rise/Fall Time
ZN=(!I)



Function Table

I	ZN
0	1
1	0

Cell Size

CellName	Height(um)	Width(um)
CLKNHSV1	1.26	0.42
CLKNHSV2	1.26	0.42
CLKNHSV3	1.26	0.56
CLKNHSV4	1.26	0.56
CLKNHSV6	1.26	0.84
CLKNHSV8	1.26	0.98
CLKNHSV12	1.26	1.26
CLKNHSV16	1.26	1.68
CLKNHSV20	1.26	2.10
CLKNHSV24	1.26	2.38

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
I	0.00020	0.00024	0.00029	0.00033	0.00056	0.00063	0.00092	0.00117

Pin	V20	V24
I	0.00145	0.00179

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
I	0.00054	0.00062	0.00097	0.00110	0.00159	0.00200	0.00303	0.00401

Pin	V20	V24
I	0.00497	0.00596

Max Leakage Power (uW)

V1	V2	V3	V4	V6	V8	V12	V16
0.00007561	0.00009899	0.00020757	0.00023559	0.00045940	0.00061650	0.00097998	0.00144047

V20	V24
0.00185299	0.00228523

Delay Table (ns)

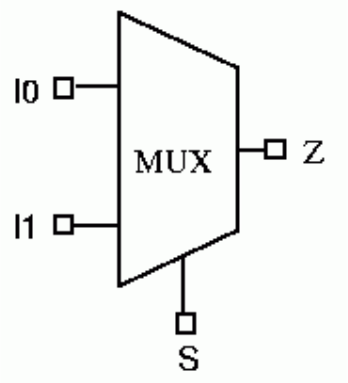
Description	V1	V2	V3	V4	V6	V8	V12	V16
I→ZN_FALL	0.01170	0.01052	0.00877	0.00842	0.00835	0.00819	0.00799	0.00768
I→ZN_RISE	0.01336	0.01174	0.00955	0.00896	0.00872	0.00799	0.00774	0.00748

Description	V20	V24
I→ZN_FALL	0.00775	0.00797
I→ZN_RISE	0.00764	0.00783

CKMUX2HS

Cell Description

2-to-1 Multiplexer
Z=((I0&(!S))|(I1&S))



Function Table

S	I0	I1	Z
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

Cell Size

CellName	Height(um)	Width(um)
CKMUX2HSV1	1.26	1.82
CKMUX2HSV2	1.26	1.82

Pin Power (uW/MHz)

Pin	V1	V2
I0	0.00101	0.00108
I1	0.00106	0.00113
S	0.00110	0.00117

Pin Capacitance (pf)

Pin	V1	V2
I0	0.00058	0.00058
I1	0.00061	0.00060
S	0.00095	0.00098

Max Leakage Power (uW)

V1	V2
0.00045727	0.00047267

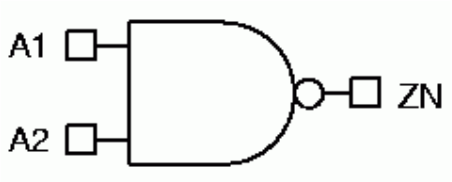
Delay Table (ns)

Description	V1	V2
I0→Z_FALL	0.05738	0.05696
I0→Z_RISE	0.04111	0.04093
I1→Z_FALL	0.06100	0.06050
I1→Z_RISE	0.04112	0.04095
S→Z_FALL	0.04872	0.04863
S→Z_RISE	0.03988	0.03988

CLKNAND2HS

Cell Description

2-Input NAND
ZN=(!(A1&A2))



Function Table

A1	A2	ZN
0	X	1
1	0	1
1	1	0

Cell Size

CellName	Height(um)	Width(um)
CLKNAND2HSV1	1.26	0.56
CLKNAND2HSV2	1.26	0.56
CLKNAND2HSV3	1.26	0.98
CLKNAND2HSV4	1.26	0.98
CLKNAND2HSV8	1.26	1.68

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V8
A1	0.00027	0.00031	0.00041	0.00056	0.00101
A2	0.00032	0.00037	0.00058	0.00076	0.00140

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V8
A1	0.00057	0.00064	0.00095	0.00113	0.00213
A2	0.00059	0.00067	0.00095	0.00112	0.00214

Max Leakage Power (uW)

V1	V2	V3	V4	V8
0.00018815	0.00023811	0.00051910	0.00061070	0.00142767

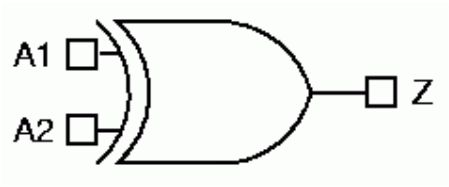
Delay Table (ns)

Description	V1	V2	V3	V4	V8
A1→ZN_FALL	0.01545	0.01540	0.01338	0.01322	0.01172
A1→ZN_RISE	0.01495	0.01292	0.01077	0.01073	0.00948
A2→ZN_FALL	0.01667	0.01684	0.01643	0.01616	0.01443
A2→ZN_RISE	0.01624	0.01406	0.01269	0.01254	0.01114

CLKXOR2HS

Cell Description

2-Input Exclusive OR
Z=(A1^A2)



Function Table

A2	A1	Z
0	0	0
0	1	1
1	0	1
1	1	0

Cell Size

CellName	Height(um)	Width(um)
CLKXOR2HSV1	1.26	1.96
CLKXOR2HSV2	1.26	1.96

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00116	0.00123
A2	0.00196	0.00204

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00111	0.00112
A2	0.00067	0.00066

Max Leakage Power (uW)

V1	V2
0.00044219	0.00043854

Delay Table (ns)

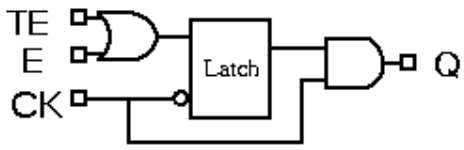
Description	V1	V2
A1→Z_FALL	0.04595	0.04648

A1→Z_RISE	0.04085	0.04060
A2→Z_FALL	0.07391	0.07502
A2→Z_RISE	0.06008	0.06015

CLKLANQHS

Cell Description

pre-controlled positiveedge triggered clock-gating latch for Low Power Design
IQ=!CK ? (TE|E)
Q=IQ&CK



Function Table

CK<1>	CK	TE	E	Q
0	1	0	0	0
0	1	0	1	1
0	1	1	X	1
0	0	X	X	0
1	1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
CLKLANQHSV1	1.26	2.94
CLKLANQHSV2	1.26	2.94
CLKLANQHSV3	1.26	3.08
CLKLANQHSV4	1.26	3.08
CLKLANQHSV6	1.26	3.36
CLKLANQHSV8	1.26	3.50
CLKLANQHSV12	1.26	3.92
CLKLANQHSV16	1.26	4.06
CLKLANQHSV20	1.26	4.48
CLKLANQHSV24	1.26	4.90

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
CK	0.00133	0.00134	0.00132	0.00131	0.00131	0.00133	0.00131	0.00133
E	0.00031	0.00031	0.00030	0.00030	0.00030	0.00031	0.00030	0.00030
Q	0.00109	0.00119	0.00135	0.00149	0.00191	0.00226	0.00308	0.00394
TE	0.00034	0.00034	0.00033	0.00033	0.00033	0.00034	0.00033	0.00033

Pin	V20	V24
CK	0.00133	0.00132
E	0.00030	0.00031
Q	0.00486	0.00591

TE	0.00033	0.00033

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
CK	0.00049	0.00050	0.00050	0.00050	0.00048	0.00048	0.00046	0.00048
E	0.00052	0.00052	0.00052	0.00052	0.00052	0.00052	0.00052	0.00053
TE	0.00051	0.00051	0.00051	0.00051	0.00053	0.00053	0.00052	0.00053

Pin	V20	V24
CK	0.00049	0.00050
E	0.00053	0.00052
TE	0.00053	0.00052

Max Leakage Power (uW)

V1	V2	V3	V4	V6	V8	V12	V16
0.00060208	0.00063152	0.00069526	0.00073225	0.00088344	0.00107927	0.00150172	0.00190859

V20	V24
0.00235408	0.00283105

Delay Table (ns)

Description	V1	V2	V3	V4	V6	V8	V12	V16
CK→Q_FALL	0.08147	0.08138	0.08158	0.08314	0.08738	0.09122	0.09958	0.11189
CK→Q_RISE	0.08231	0.08242	0.08252	0.08396	0.08840	0.09504	0.10551	0.11786

Description	V20	V24
CK→Q_FALL	0.12085	0.12679
CK→Q_RISE	0.12860	0.13811

Timing Constraints (ns)

Pin	Requirement	V1	V2	V3	V4	V6	V8
E	hold_FALL→CK	-0.04294	-0.04008	-0.04008	-0.03720	-0.03720	-0.03723
E	hold_RISE→CK	-0.02005	-0.02004	-0.01717	-0.01718	-0.02006	-0.02005
E	setup_FALL→CK	0.04866	0.04866	0.04866	0.04865	0.04867	0.04866
E	setup_RISE→CK	0.02292	0.02292	0.02292	0.02292	0.02292	0.02576
TE	hold_FALL→CK	-0.04579	-0.04294	-0.04294	-0.04294	-0.04293	-0.04292
TE	hold_RISE→CK	-0.02004	-0.02005	-0.02004	-0.02004	-0.02004	-0.02004
TE	setup_FALL→CK	0.05153	0.05151	0.05151	0.05153	0.05153	0.05439
TE	setup_RISE→CK	0.02577	0.02576	0.02576	0.02576	0.02576	0.02576
CK	minpwl	0.08155	0.08156	0.07982	0.07983	0.07978	0.08158

Pin	Requirement	V12	V16	V20	V24
E	hold_FALL→CK	-0.03723	-0.02861	-0.03147	-0.04008

E	hold_RISE→CK	-0.01718	-0.04008	-0.04008	-0.02005
E	setup_FALL→CK	0.04865	0.04293	0.04293	0.04865
E	setup_RISE→CK	0.02292	0.05152	0.04866	0.02289
TE	hold_FALL→CK	-0.04006	-0.03433	-0.03433	-0.04295
TE	hold_RISE→CK	-0.02005	-0.04582	-0.04580	-0.02005
TE	setup_FALL→CK	0.05152	0.04866	0.04866	0.05438
TE	setup_RISE→CK	0.02577	0.05440	0.05440	0.02578
CK	minpwl	0.07980	0.09304	0.09479	0.08337

DELHS

Cell Description

Delay cell
Z=I

Function Table

I	Z
0	0
1	1

Cell Size

CellName	Height(um)	Width(um)
DELHS2	1.26	1.54

Pin Power (uW/MHz)

Pin	DELHS2
I	0.00173

Pin Capacitance (pf)

Pin	DELHS2
I	0.00046

Max Leakage Power (uW)

DELHS2
0.00018496

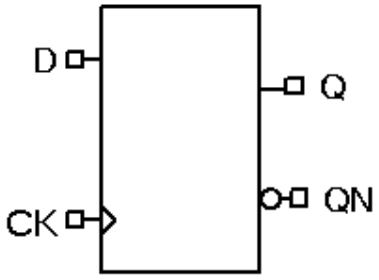
Delay Table (ns)

Description	DELHS2
I→Z_FALL	0.13000
I→Z_RISE	0.12888

DHS

Cell Description

D Flip-Flop
Q = rising (CK) ? D : pre_Q
QN = !Q



Function Table

CK<1>	CK	D	Q
0	0	X	Q<1>
0	1	0	0
0	1	1	1
1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
DHSV1	1.26	3.22
DHSV2	1.26	3.22

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00138	0.00138
D	0.00048	0.00048
Q	0.00090	0.00098
QN	0.00090	0.00099

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00044	0.00044
D	0.00053	0.00053

Max Leakage Power (uW)

V1	V2
0.00052176	0.00057897

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.11330	0.11316
CK→Q_RISE	0.11076	0.11257
CK→QN_FALL	0.08611	0.08453
CK→QN_RISE	0.08818	0.08718

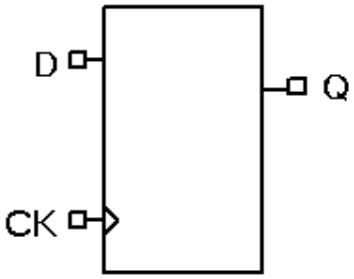
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	0.00573	0.00857
D	hold_RISE→CK	-0.00859	-0.00859
D	setup_FALL→CK	0.02005	0.02004
D	setup_RISE→CK	0.02005	0.02005
CK	minpwh	0.08818	0.09523
CK	minpwl	0.08995	0.08994

DQHS

Cell Description

D Flip-Flop, Single Output
Q = rising (CK) ? D : pre_Q



Function Table

CK<1>	CK	D	Q
0	0	X	Q<1>
0	1	0	0
0	1	1	1
1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
DQHSV1	1.26	2.94
DQHSV2	1.26	2.94

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00132	0.00132
D	0.00048	0.00048
Q	0.00136	0.00145

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00045	0.00045
D	0.00056	0.00056

Max Leakage Power (uW)

V1	V2
0.00044423	0.00045953

Delay Table (ns)

Description	V1	V2

CK→Q_FALL	0.10008	0.09954
CK→Q_RISE	0.09499	0.09484

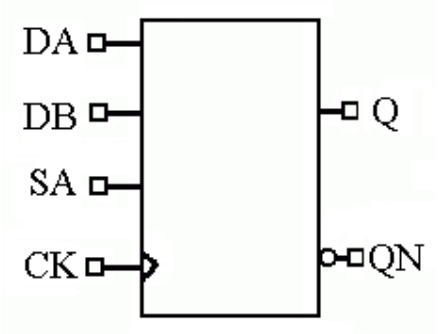
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	0.00286	0.00574
D	hold_RISE→CK	-0.00573	-0.00573
D	setup_FALL→CK	0.01719	0.01719
D	setup_RISE→CK	0.01433	0.01718
CK	minpwh	0.05648	0.06001
CK	minpwl	0.08552	0.08553

DXHS

Cell Description

D Flip-Flop with Mux Inputs
Q = rising (CK) ? (DA&SA|DB&!SA) : pre_Q
QN = !Q



Function Table

CK<1>	CK	SA	DB	DA	Q
0	0	X	X	X	Q<1>
0	1	0	0	X	0
0	1	0	1	X	1
0	1	1	X	0	0
0	1	1	X	1	1
1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
DXHSV1	1.26	4.20
DXHSV2	1.26	4.20

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00152	0.00152
DA	0.00035	0.00035
DB	0.00031	0.00031
Q	0.00090	0.00099
QN	0.00089	0.00098
SA	0.00064	0.00065

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00045	0.00045
DA	0.00041	0.00041
DB	0.00046	0.00047
SA	0.00092	0.00092

Max Leakage Power (uW)

V1	V2
0.00057504	0.00060788

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.11573	0.11648
CK→Q_RISE	0.11405	0.11740
CK→QN_FALL	0.08781	0.08893
CK→QN_RISE	0.09453	0.09359

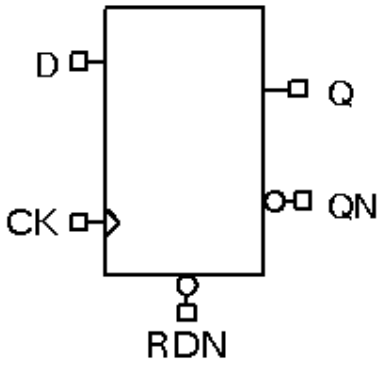
Timing Constraints (ns)

Pin	Requirement	V1	V2
DA	hold_FALL→CK	-0.01430	-0.00857
DA	hold_RISE→CK	-0.04008	-0.04007
DA	setup_FALL→CK	0.06010	0.06010
DA	setup_RISE→CK	0.06010	0.06296
DB	hold_FALL→CK	-0.00573	-0.00000
DB	hold_RISE→CK	-0.03434	-0.03435
DB	setup_FALL→CK	0.05439	0.05439
DB	setup_RISE→CK	0.05437	0.05726
SA	hold_FALL→CK	-0.05439	-0.05439
SA	hold_RISE→CK	-0.03149	-0.02576
SA	setup_FALL→CK	0.07442	0.07730
SA	setup_RISE→CK	0.08588	0.08301
CK	minpwh	0.09171	0.10226
CK	minpwl	0.10750	0.10751

DRNHS

Cell Description

D Flip-Flop with Async Clear
Q = !RDN ? 0 : rising (CK) ? D : pre_Q
QN = !Q



Function Table

RDN	CK<1>	CK	D	Q
0	X	X	X	0
1	0	0	X	Q<1>
1	0	1	0	0
1	0	1	1	1
1	1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
DRNHSV1	1.26	3.78
DRNHSV2	1.26	3.78

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00139	0.00139
D	0.00028	0.00028
Q	0.00115	0.00122
QN	0.00117	0.00125
RDN	0.00031	0.00031

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00043	0.00043
D	0.00042	0.00043
RDN	0.00162	0.00162

Max Leakage Power (uW)

V1	V2
0.00073888	0.00078291

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.11079	0.11177
CK→Q_RISE	0.12555	0.12777
RDN→Q_FALL	0.03221	0.03194
CK→QN_FALL	0.08496	0.08564
CK→QN_RISE	0.08713	0.08600
RDN→QN_RISE	0.09859	0.09922

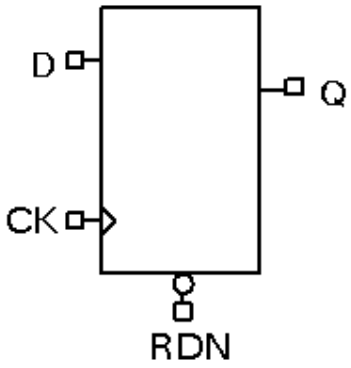
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.00000	0.00574
D	hold_RISE→CK	-0.02004	-0.01719
D	setup_FALL→CK	0.03435	0.03149
D	setup_RISE→CK	0.03436	0.03723
RDN	setup_RISE→CK	0.03722	0.04007
RDN	hold_RISE→CK	-0.02864	-0.02864
CK	minpwh	0.09171	0.09873
CK	minpwl	0.09875	0.09875
RDN	minpwl	0.05657	0.06011

DRNQHS

Cell Description

D Flip-Flop with Async Clear, Single Output
Q = !RDN ? 0 : rising (CK) ? D : pre_Q



Function Table

RDN	CK<1>	CK	D	Q
0	X	X	X	0
1	0	0	X	Q<1>
1	0	1	0	0
1	0	1	1	1
1	1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
DRNQHSV1	1.26	3.50
DRNQHSV2	1.26	3.50

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00140	0.00140
D	0.00027	0.00027
Q	0.00177	0.00185
RDN	0.00031	0.00031

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00045	0.00045
D	0.00042	0.00043
RDN	0.00158	0.00158

Max Leakage Power (uW)

V1	V2
0.00062509	0.00064666

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.10510	0.10494
CK→Q_RISE	0.10117	0.10089
RDN→Q_FALL	0.03923	0.03925

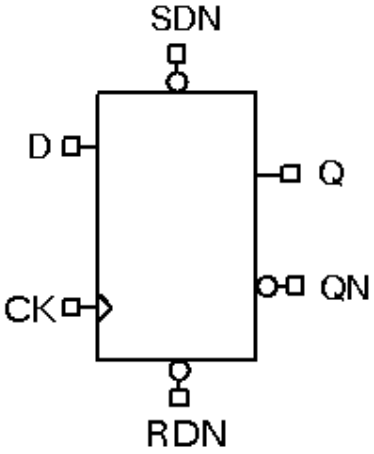
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.00287	-0.00000
D	hold_RISE→CK	-0.02004	-0.02004
D	setup_FALL→CK	0.03148	0.03148
D	setup_RISE→CK	0.03150	0.03435
RDN	setup_RISE→CK	0.03436	0.03723
RDN	hold_RISE→CK	-0.02864	-0.02864
CK	minpwh	0.05653	0.06007
CK	minpwl	0.09876	0.09876
RDN	minpwl	0.05654	0.06006

DRSNHS

Cell Description

D Flip-Flop with Async Clear and Set
Q = !SDN ? 1 : !RDN ? 0 : rising (CK) ? D : pre_Q
QN = !Q



Function Table

RDN	SDN	CK<1>	CK	D	Q
0	0	X	X	X	1
0	1	X	X	X	0
1	0	X	X	X	1
1	1	0	0	X	Q<1>
1	1	0	1	0	0
1	1	0	1	1	1
1	1	1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
DRSNHSV1	1.26	5.88
DRSNHSV2	1.26	5.88

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00203	0.00203
D	0.00028	0.00028
Q	0.00130	0.00139
QN	0.00130	0.00139
RDN	0.00097	0.00097
SDN	0.00017	0.00017

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00062	0.00062
D	0.00045	0.00045
RDN	0.00110	0.00110
SDN	0.00083	0.00083

Max Leakage Power (uW)

V1	V2
0.00065905	0.00070553

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.14930	0.15113
CK→Q_RISE	0.13590	0.13814
RDN→Q_FALL	0.13315	0.13506
SDN→Q_FALL	0.09544	0.09734
SDN→Q_RISE	0.09060	0.09186
CK→QN_FALL	0.11300	0.11187
CK→QN_RISE	0.12296	0.12108
RDN→QN_RISE	0.10633	0.10454
SDN→QN_FALL	0.06863	0.06694
SDN→QN_RISE	0.06863	0.06681

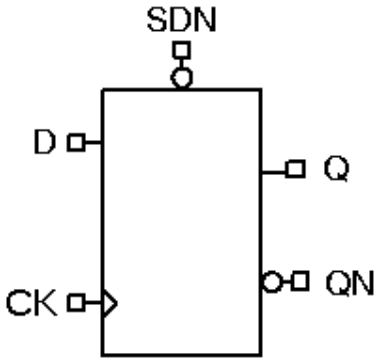
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	0.00288	0.00574
D	hold_RISE→CK	-0.03722	-0.03722
D	setup_FALL→CK	0.04865	0.05151
D	setup_RISE→CK	0.06297	0.06585
RDN	setup_RISE→CK	0.06584	0.06584
RDN	hold_RISE→CK	-0.05152	-0.05151
SDN	setup_RISE→CK	-0.06870	-0.06297
SDN	hold_RISE→CK	0.08588	0.08588
SDN	non_seq_hold_RISE→RDN	-0.04578	-0.04865
SDN	non_seq_setup_RISE→RDN	0.05724	0.06296
CK	minpwh	0.11627	0.12330
CK	minpwl	0.15585	0.15585
RDN	minpwl	0.09166	0.09869
SDN	minpwl	0.10575	0.11275

DSNHS

Cell Description

D Flip-Flop with Async Set
Q = !SDN ? 1 : rising (CK) ? D : pre_Q
QN = !Q



Function Table

SDN	CK<1>	CK	D	Q
0	X	X	X	1
1	0	0	X	Q<1>
1	0	1	0	0
1	0	1	1	1
1	1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
DSNHSV1	1.26	3.64
DSNHSV2	1.26	3.64

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00147	0.00147
D	0.00039	0.00039
Q	0.00117	0.00127
QN	0.00112	0.00120
SDN	0.00013	0.00013

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00046	0.00046
D	0.00049	0.00049
SDN	0.00100	0.00100

Max Leakage Power (uW)

V1	V2
0.00066451	0.00070792

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.12423	0.12626
CK→Q_RISE	0.12425	0.12556
SDN→Q_RISE	0.08269	0.08364
CK→QN_FALL	0.10040	0.10089
CK→QN_RISE	0.09970	0.09922
SDN→QN_FALL	0.06133	0.06158

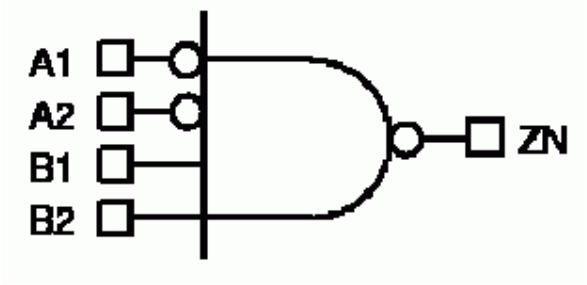
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	0.00573	0.00859
D	hold_RISE→CK	-0.01718	-0.01432
D	setup_FALL→CK	0.02576	0.02576
D	setup_RISE→CK	0.03149	0.03149
SDN	setup_RISE→CK	-0.04294	-0.04294
SDN	hold_RISE→CK	0.05439	0.05439
CK	minpwh	0.10925	0.11981
CK	minpwl	0.09872	0.09872
SDN	minpwl	0.09170	0.09872

I2NAND4HS

Cell Description

4-Input NAND with 2 Inverted Inputs
ZN=(!((!A1)&(!A2)&B1&B2))



Function Table

A1	A2	B1	B2	ZN
0	0	0	X	1
0	0	1	0	1
0	0	1	1	0
0	1	X	X	1
1	X	X	X	1

Cell Size

CellName	Height(um)	Width(um)
I2NAND4HSV1	1.26	1.54
I2NAND4HSV2	1.26	1.54

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00088	0.00094
A2	0.00087	0.00093
B1	0.00051	0.00055
B2	0.00057	0.00062

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00048	0.00049
A2	0.00049	0.00048
B1	0.00056	0.00060
B2	0.00057	0.00062

Max Leakage Power (uW)

V1	V2
0.00057633	0.00069433

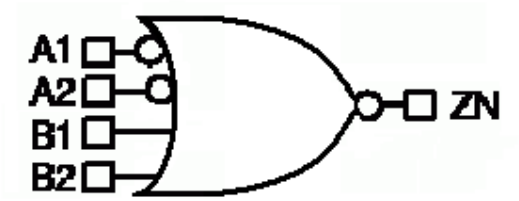
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.05306	0.05613
A1→ZN_RISE	0.03682	0.03507
A2→ZN_FALL	0.05689	0.06030
A2→ZN_RISE	0.03654	0.03468
B1→ZN_FALL	0.03607	0.03862
B1→ZN_RISE	0.01997	0.01705
B2→ZN_FALL	0.03786	0.04034
B2→ZN_RISE	0.02155	0.01821

I2NOR4HS

Cell Description

4-Input NOR with 2 Inverted Inputs
ZN=(!((!A1)|(!A2)|B1|B2))



Function Table

A1	A2	B1	B2	ZN
0	X	X	X	0
1	0	X	X	0
1	1	0	0	1
1	1	0	1	0
1	1	1	X	0

Cell Size

CellName	Height(um)	Width(um)
I2NOR4HSV1	1.26	1.54
I2NOR4HSV2	1.26	1.54

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00104	0.00109
A2	0.00096	0.00103
B1	0.00045	0.00049
B2	0.00036	0.00040

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00048	0.00048
A2	0.00047	0.00047
B1	0.00056	0.00060
B2	0.00054	0.00059

Max Leakage Power (uW)

V1	V2
0.00040394	0.00040143

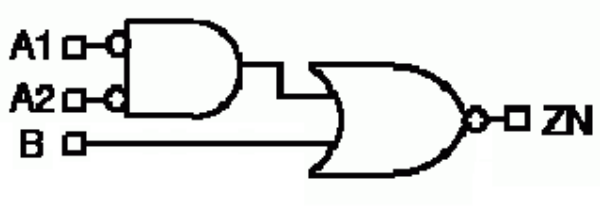
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.04192	0.04006
A1→ZN_RISE	0.07655	0.08131
A2→ZN_FALL	0.04002	0.03822
A2→ZN_RISE	0.07297	0.07810
B1→ZN_FALL	0.01461	0.01244
B1→ZN_RISE	0.05031	0.05481
B2→ZN_FALL	0.01354	0.01174
B2→ZN_RISE	0.04217	0.04669

IAO21HS

Cell Description

2-1 IAO with 2 Inverted Inputs
ZN=(!(((!A1)&(!A2))|B))



Function Table

A1	A2	B	ZN
0	0	X	0
0	1	0	1
0	1	1	0
1	X	0	1
1	X	1	0

Cell Size

CellName	Height(um)	Width(um)
IAO21HSV1	1.26	0.98
IAO21HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00076	0.00080
A2	0.00083	0.00087
B	0.00035	0.00037

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00050	0.00050
A2	0.00053	0.00053
B	0.00060	0.00064

Max Leakage Power (uW)

V1	V2
0.00024965	0.00024906

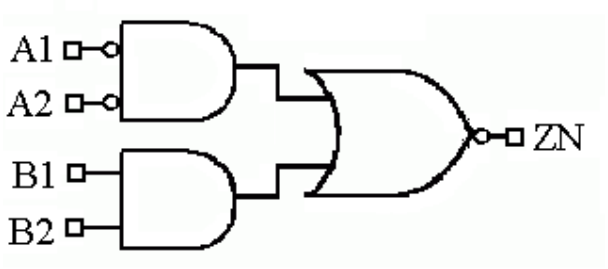
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.04852	0.04766
A1→ZN_RISE	0.03851	0.04029
A2→ZN_FALL	0.05165	0.05074
A2→ZN_RISE	0.04036	0.04213
B→ZN_FALL	0.01288	0.01092
B→ZN_RISE	0.02301	0.02418

IAO22HS

Cell Description

2-2 IAO with 2 Inverted Inputs
ZN=(!((!A1)&(!A2))|(B1&B2)))



Function Table

B1	B2	A1	A2	ZN
0	X	0	0	0
0	X	0	1	1
0	X	1	X	1
1	0	0	0	0
1	0	0	1	1
1	0	1	X	1
1	1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
IAO22HSV1	1.26	1.26
IAO22HSV2	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00083	0.00085
A2	0.00088	0.00090
B1	0.00050	0.00050
B2	0.00056	0.00056

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00048	0.00048
A2	0.00053	0.00054
B1	0.00070	0.00068
B2	0.00067	0.00068

Max Leakage Power (uW)

V1	V2
0.00025613	0.00025661

Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.05249	0.05060
A1→ZN_RISE	0.04060	0.04158
A2→ZN_FALL	0.05445	0.05253
A2→ZN_RISE	0.04198	0.04300
B1→ZN_FALL	0.01930	0.01924
B1→ZN_RISE	0.02922	0.02937
B2→ZN_FALL	0.02062	0.02067
B2→ZN_RISE	0.03221	0.03249

INAND2HS

Cell Description

2-Input NAND with 1 Inverted Input
ZN=(!((!A1)&B1))

Function Table

A1	B1	ZN
0	0	1
0	1	0
1	X	1

Cell Size

CellName	Height(um)	Width(um)
INAND2HSV1	1.26	0.84
INAND2HSV2	1.26	0.84

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00070	0.00074
B1	0.00032	0.00034

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00047	0.00049
B1	0.00059	0.00062

Max Leakage Power (uW)

V1	V2
0.00025052	0.00028868

Delay Table (ns)

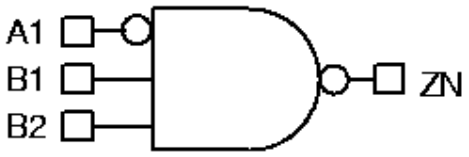
Description	V1	V2
A1→ZN_FALL	0.03701	0.03877
A1→ZN_RISE	0.03143	0.02992

B1→ZN_FALL	0.01595	0.01697
B1→ZN_RISE	0.01589	0.01364

INAND3HS

Cell Description

3-Input NAND with 1 Inverted Input
ZN=(!((!A1)&B1&B2))



Function Table

A1	B1	B2	ZN
0	0	X	1
0	1	0	1
0	1	1	0
1	X	X	1

Cell Size

CellName	Height(um)	Width(um)
INAND3HSV1	1.26	0.98
INAND3HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00080	0.00087
B1	0.00040	0.00044
B2	0.00046	0.00050

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00049	0.00049
B1	0.00057	0.00062
B2	0.00061	0.00066

Max Leakage Power (uW)

V1	V2
0.00038320	0.00041541

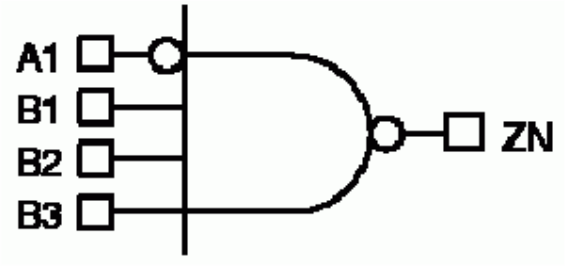
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.04520	0.04845
A1→ZN_RISE	0.03413	0.03267
B1→ZN_FALL	0.02448	0.02645
B1→ZN_RISE	0.01768	0.01482
B2→ZN_FALL	0.02640	0.02831
B2→ZN_RISE	0.01955	0.01622

INAND4HS

Cell Description

4-Input NAND with 1 Inverted Input
ZN=(!((!A1)&B1&B2&B3))



Function Table

A1	B1	B2	B3	ZN
0	0	X	X	1
0	1	0	X	1
0	1	1	0	1
0	1	1	1	0
1	X	X	X	1

Cell Size

CellName	Height(um)	Width(um)
INAND4HSV1	1.26	1.12
INAND4HSV2	1.26	1.12

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00087	0.00094
B1	0.00042	0.00047
B2	0.00050	0.00054
B3	0.00056	0.00060

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00050	0.00050
B1	0.00060	0.00064
B2	0.00059	0.00062
B3	0.00059	0.00062

Max Leakage Power (uW)

V1	V2
0.00050925	0.00059359

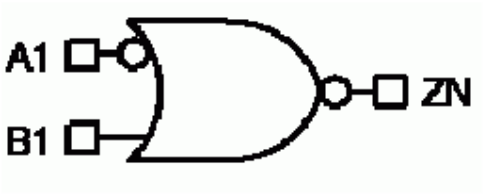
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.05360	0.05688
A1→ZN_RISE	0.03679	0.03535
B1→ZN_FALL	0.03161	0.03413
B1→ZN_RISE	0.01817	0.01581
B2→ZN_FALL	0.03556	0.03794
B2→ZN_RISE	0.02013	0.01729
B3→ZN_FALL	0.03708	0.03945
B3→ZN_RISE	0.02163	0.01841

INOR2HS

Cell Description

2-Input NOR with 1 Inverted Input
ZN=(!((!A1)|B1))



Function Table

A1	B1	ZN
0	X	0
1	0	1
1	1	0

Cell Size

CellName	Height(um)	Width(um)
INOR2HSV1	1.26	0.84
INOR2HSV2	1.26	0.84

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00071	0.00074
B1	0.00032	0.00037

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00047	0.00048
B1	0.00057	0.00064

Max Leakage Power (uW)

V1	V2
0.00022168	0.00021971

Delay Table (ns)

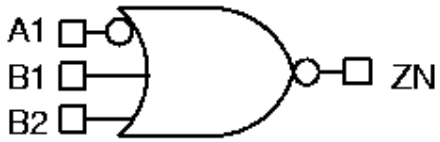
Description	V1	V2
A1→ZN_FALL	0.03358	0.03493
A1→ZN_RISE	0.04252	0.03793

B1→ZN_FALL	0.01050	0.01123
B1→ZN_RISE	0.02868	0.02443

INOR3HS

Cell Description

3-Input NOR with 1 Inverted Input
ZN=(!((!A1)|B1|B2))



Function Table

A1	B1	B2	ZN
0	X	X	0
1	0	0	1
1	0	1	0
1	1	X	0

Cell Size

CellName	Height(um)	Width(um)
INOR3HSV1	1.26	0.98
INOR3HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00081	0.00088
B1	0.00041	0.00046
B2	0.00051	0.00055

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00048	0.00049
B1	0.00059	0.00064
B2	0.00061	0.00066

Max Leakage Power (uW)

V1	V2
0.00028023	0.00028372

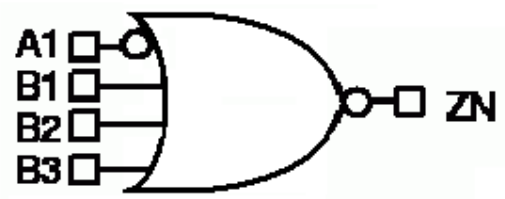
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.03907	0.03820
A1→ZN_RISE	0.04928	0.05304
B1→ZN_FALL	0.01397	0.01196
B1→ZN_RISE	0.03768	0.04072
B2→ZN_FALL	0.01481	0.01241
B2→ZN_RISE	0.04053	0.04347

INOR4HS

Cell Description

4-Input NOR with 1 Inverted Input
ZN=(!((!A1)|B1|B2|B3))



Function Table

A1	B1	B2	B3	ZN
0	X	X	X	0
1	0	0	0	1
1	0	0	1	0
1	0	1	X	0
1	1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
INOR4HSV1	1.26	1.12
INOR4HSV2	1.26	1.12

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00086	0.00093
B1	0.00044	0.00048
B2	0.00053	0.00058
B3	0.00062	0.00067

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00048	0.00049
B1	0.00057	0.00061
B2	0.00059	0.00064
B3	0.00060	0.00065

Max Leakage Power (uW)

V1	V2
0.00034756	0.00034899

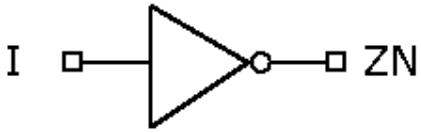
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.04096	0.03988
A1→ZN_RISE	0.06120	0.06653
B1→ZN_FALL	0.01452	0.01236
B1→ZN_RISE	0.05082	0.05559
B2→ZN_FALL	0.01536	0.01285
B2→ZN_RISE	0.05706	0.06187
B3→ZN_FALL	0.01542	0.01279
B3→ZN_RISE	0.05967	0.06450

INHS

Cell Description

Inverter
ZN=(!I)



Function Table

I	ZN
0	1
1	0

Cell Size

CellName	Height(um)	Width(um)
INHSV1	1.26	0.42
INHSV2	1.26	0.42
INHSV3	1.26	0.56
INHSV4	1.26	0.56
INHSV6	1.26	0.84
INHSV8	1.26	0.98
INHSV12	1.26	1.26
INHSV16	1.26	1.68
INHSV20	1.26	2.10
INHSV24	1.26	2.38

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
I	0.00020	0.00025	0.00031	0.00036	0.00059	0.00067	0.00092	0.00129

Pin	V20	V24
I	0.00163	0.00191

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
I	0.00056	0.00064	0.00102	0.00119	0.00170	0.00223	0.00300	0.00438

Pin	V20	V24
I	0.00542	0.00646

Max Leakage Power (uW)

V1	V2	V3	V4	V6	V8	V12	V16
0.00006480	0.00009265	0.00020757	0.00023811	0.00043081	0.00061938	0.00097998	0.00142363

V20	V24
0.00186733	0.00227777

Delay Table (ns)

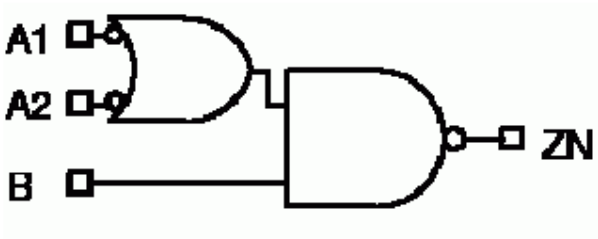
Description	V1	V2	V3	V4	V6	V8	V12	V16
I→ZN_FALL	0.01087	0.00980	0.00849	0.00797	0.00769	0.00716	0.00774	0.00708
I→ZN_RISE	0.01384	0.01215	0.00989	0.00933	0.00896	0.00824	0.00773	0.00801

Description	V20	V24
I→ZN_FALL	0.00734	0.00755
I→ZN_RISE	0.00821	0.00836

IOA21HS

Cell Description

2-1 IOA with 2 Inverted Inputs
ZN=(!(((!A1)|(!A2))&B))



Function Table

A1	A2	B	ZN
0	X	0	1
0	X	1	0
1	0	0	1
1	0	1	0
1	1	X	1

Cell Size

CellName	Height(um)	Width(um)
IOA21HSV1	1.26	0.98
IOA21HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00075	0.00082
A2	0.00082	0.00089
B	0.00032	0.00036

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00054	0.00054
A2	0.00055	0.00055
B	0.00056	0.00062

Max Leakage Power (uW)

V1	V2
0.00030048	0.00033669

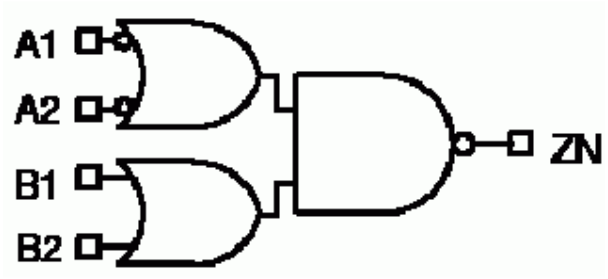
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.04014	0.04267
A1→ZN_RISE	0.03369	0.03232
A2→ZN_FALL	0.04288	0.04540
A2→ZN_RISE	0.03577	0.03435
B→ZN_FALL	0.01583	0.01710
B→ZN_RISE	0.01586	0.01348

IOA22HS

Cell Description

2-2 IOA with 2 Inverted Inputs
ZN=(!(((!A1)|(!A2))&(B1|B2)))



Function Table

B1	B2	A1	A2	ZN
0	0	X	X	1
0	1	0	X	0
0	1	1	0	0
0	1	1	1	1
1	X	0	X	0
1	X	1	0	0
1	X	1	1	1

Cell Size

CellName	Height(um)	Width(um)
IOA22HSV1	1.26	1.26
IOA22HSV2	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00082	0.00085
A2	0.00088	0.00090
B1	0.00044	0.00042
B2	0.00053	0.00051

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00054	0.00054
A2	0.00056	0.00055
B1	0.00060	0.00059
B2	0.00067	0.00067

Max Leakage Power (uW)

V1	V2
0.00030486	0.00034341

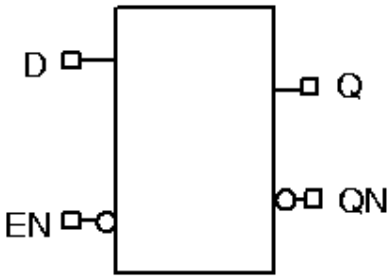
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.04271	0.04416
A1→ZN_RISE	0.03568	0.03374
A2→ZN_FALL	0.04568	0.04698
A2→ZN_RISE	0.03736	0.03528
B1→ZN_FALL	0.01988	0.01947
B1→ZN_RISE	0.02897	0.02800
B2→ZN_FALL	0.02221	0.02181
B2→ZN_RISE	0.03207	0.03101

LALHS

Cell Description

Low Enable Latch
Q = !EN ? D : pre_Q
QN = !Q



Function Table

EN	D	Q
0	0	0
0	1	1
1	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LALHSV1	1.26	2.24
LALHSV2	1.26	2.24

Pin Power (uW/MHz)

Pin	V1	V2
D	0.00002	0.00002
EN	0.00109	0.00109
Q	0.00091	0.00103
QN	0.00092	0.00102

Pin Capacitance (pf)

Pin	V1	V2
D	0.00064	0.00064
EN	0.00049	0.00048

Max Leakage Power (uW)

V1	V2
0.00044412	0.00045377

Delay Table (ns)

Description	V1	V2

D→Q_FALL	0.06189	0.06306
D→Q_RISE	0.05161	0.05142
EN→Q_FALL	0.10363	0.10467
EN→Q_RISE	0.08934	0.08907
D→QN_FALL	0.07299	0.07643
D→QN_RISE	0.08601	0.08924
EN→QN_FALL	0.11109	0.11444
EN→QN_RISE	0.12783	0.13090

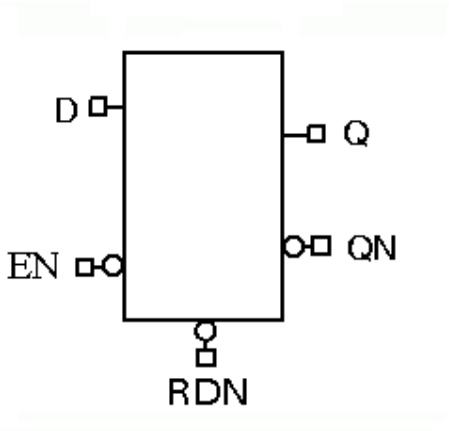
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→EN	-0.01716	-0.02003
D	hold_RISE→EN	-0.02290	-0.02577
D	setup_FALL→EN	0.03434	0.04292
D	setup_RISE→EN	0.03149	0.03437
EN	minpwl	0.07766	0.07766

LALRNHS

Cell Description

Latch
Q = !RDN ? 0 : !EN ? D : pre_Q
QN = !Q



Function Table

RDN	EN	D	Q
0	X	X	0
1	0	0	0
1	0	1	1
1	1	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LALRNHSV1	1.26	2.66
LALRNHSV2	1.26	2.66

Pin Power (uW/MHz)

Pin	V1	V2
D	0.00001	0.00001
EN	0.00116	0.00116
Q	0.00105	0.00119
QN	0.00108	0.00120
RDN	0.00000	0.00000

Pin Capacitance (pf)

Pin	V1	V2
D	0.00061	0.00062
EN	0.00049	0.00049
RDN	0.00088	0.00089

Max Leakage Power (uW)

V1	V2
0.00050496	0.00052935

Delay Table (ns)

Description	V1	V2
D→Q_FALL	0.06964	0.07054
D→Q_RISE	0.07246	0.07268
EN→Q_FALL	0.11250	0.11333
EN→Q_RISE	0.10694	0.10719
RDN→Q_FALL	0.06596	0.06657
RDN→Q_RISE	0.07652	0.07679
D→QN_FALL	0.09933	0.10373
D→QN_RISE	0.09337	0.09693
EN→QN_FALL	0.13413	0.13855
EN→QN_RISE	0.13626	0.13975
RDN→QN_RISE	0.09039	0.09375
RDN→QN_FALL	0.10343	0.10786

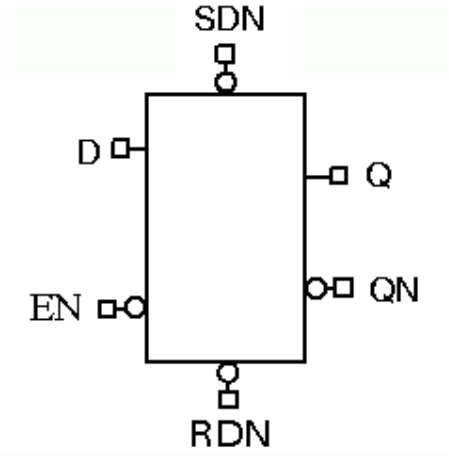
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→EN	-0.02289	-0.02575
D	hold_RISE→EN	-0.04294	-0.04580
D	setup_FALL→EN	0.04579	0.05152
D	setup_RISE→EN	0.05439	0.06012
RDN	setup_RISE→EN	0.05726	0.06299
RDN	hold_RISE→EN	-0.04583	-0.04866
EN	minpwl	0.09165	0.09522
RDN	minpwl	0.08465	0.09172

LALRSNHS

Cell Description

Low Enable Latch with Clear and Set
Q = !SDN ? 1 : !RDN ? 0 : !EN ? D : pre_Q
QN = !Q



Function Table

RDN	SDN	EN	D	Q
0	0	X	X	1
0	1	X	X	0
1	0	X	X	1
1	1	0	0	0
1	1	0	1	1
1	1	1	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LALRSNHSV1	1.26	3.92
LALRSNHSV2	1.26	4.06

Pin Power (uW/MHz)

Pin	V1	V2
D	0.00001	0.00001
EN	0.00129	0.00134
Q	0.00126	0.00133
QN	0.00125	0.00133
RDN	0.00001	0.00001
SDN	0.00057	0.00057

Pin Capacitance (pf)

Pin	V1	V2
D	0.00060	0.00061
EN	0.00048	0.00048
RDN	0.00094	0.00095
SDN	0.00048	0.00048

Max Leakage Power (uW)

V1	V2
0.00049770	0.00059618

Delay Table (ns)

Description	V1	V2
D→Q_FALL	0.11213	0.11029
D→Q_RISE	0.08242	0.07847
EN→Q_FALL	0.15423	0.15391
EN→Q_RISE	0.11357	0.11132
RDN→Q_FALL	0.13013	0.12734
RDN→Q_RISE	0.08719	0.08361
SDN→Q_FALL	0.14524	0.14163
SDN→Q_RISE	0.09351	0.09020
D→QN_FALL	0.10970	0.10897
D→QN_RISE	0.13561	0.13669
EN→QN_FALL	0.14131	0.14222
EN→QN_RISE	0.17788	0.18059
RDN→QN_RISE	0.15575	0.15720
RDN→QN_FALL	0.11454	0.11417
SDN→QN_FALL	0.11835	0.11726
SDN→QN_RISE	0.16949	0.16927

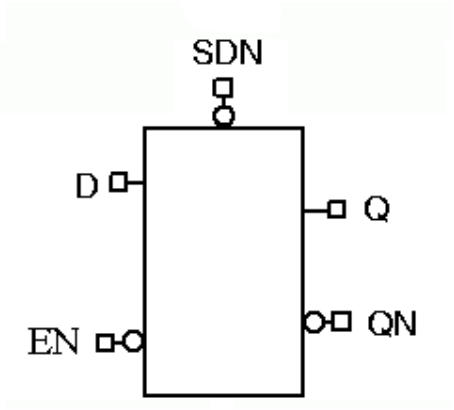
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→EN	-0.05152	-0.05724
D	hold_RISE→EN	-0.04868	-0.05151
D	setup_FALL→EN	0.08014	0.09159
D	setup_RISE→EN	0.06296	0.07443
RDN	setup_RISE→EN	0.06871	0.07730
RDN	hold_RISE→EN	-0.05439	-0.05726
SDN	setup_RISE→EN	0.10876	0.12021
SDN	hold_RISE→EN	-0.08302	-0.08872
SDN	non_seq_hold_RISE→RDN	-0.13166	-0.13740
SDN	non_seq_setup_RISE→RDN	0.16030	0.17174
EN	minpwl	0.09519	0.10573
RDN	minpwl	0.14445	0.15495
SDN	minpwl	0.07408	0.08115

LALSNHS

Cell Description

Latch
Q = !SDN ? 1 : !EN ? D : pre_Q
QN = !Q



Function Table

SDN	EN	D	Q
0	X	X	1
1	0	0	0
1	0	1	1
1	1	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LALSNHSV1	1.26	2.94
LALSNHSV2	1.26	2.94

Pin Power (uW/MHz)

Pin	V1	V2
D	0.00001	0.00001
EN	0.00117	0.00118
Q	0.00109	0.00121
QN	0.00109	0.00118
SDN	0.00050	0.00050

Pin Capacitance (pf)

Pin	V1	V2
D	0.00058	0.00059
EN	0.00049	0.00049
SDN	0.00064	0.00066

Max Leakage Power (uW)

V1	V2
0.00050985	0.00055848

Delay Table (ns)

Description	V1	V2
D→Q_FALL	0.09533	0.09566
D→Q_RISE	0.05764	0.05685
EN→Q_FALL	0.13424	0.13428
EN→Q_RISE	0.09733	0.09680
SDN→Q_FALL	0.12440	0.12447
SDN→Q_RISE	0.08519	0.08411
D→QN_FALL	0.08128	0.08369
D→QN_RISE	0.12116	0.12474
EN→QN_FALL	0.12127	0.12396
EN→QN_RISE	0.16018	0.16348
SDN→QN_FALL	0.10849	0.11050
SDN→QN_RISE	0.15020	0.15358

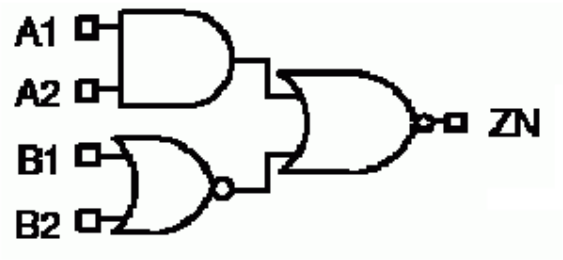
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→EN	-0.05153	-0.05440
D	hold_RISE→EN	-0.02577	-0.02862
D	setup_FALL→EN	0.08014	0.08873
D	setup_RISE→EN	0.03436	0.04007
SDN	setup_RISE→EN	0.10591	0.11450
SDN	hold_RISE→EN	-0.08016	-0.08301
EN	minpwl	0.08115	0.08467
SDN	minpwl	0.06705	0.07056

MAOI22HS

Cell Description

the logical NOR of one AND2 and one NOR2 block.
ZN=(!((A1&A2)|(!(B1|B2))))



Function Table

A1	A2	B1	B2	ZN
0	X	0	0	0
0	X	0	1	1
0	X	1	X	1
1	0	0	0	0
1	0	0	1	1
1	0	1	X	1
1	1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
MAOI22HSV1	1.26	1.26
MAOI22HSV2	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00056	0.00057
A2	0.00050	0.00051
B1	0.00083	0.00085
B2	0.00088	0.00090

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00069	0.00069
A2	0.00069	0.00069
B1	0.00051	0.00051
B2	0.00053	0.00054

Max Leakage Power (uW)

V1	V2
0.00025474	0.00025705

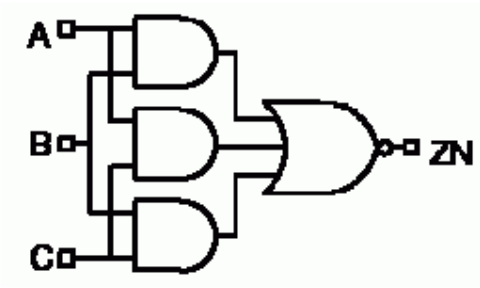
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.02080	0.02085
A1→ZN_RISE	0.03240	0.03268
A2→ZN_FALL	0.01934	0.01938
A2→ZN_RISE	0.02933	0.02963
B1→ZN_FALL	0.05290	0.05071
B1→ZN_RISE	0.04076	0.04166
B2→ZN_FALL	0.05440	0.05242
B2→ZN_RISE	0.04197	0.04300

MAOI222HS

Cell Description

Inverting 2 of 3 MAJORITY
ZN=(!((A&B)|(B&C)|(A&C)))



Function Table

A	B	C	ZN
0	0	X	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	X	0

Cell Size

CellName	Height(um)	Width(um)
MAOI222HSV1	1.26	1.54
MAOI222HSV2	1.26	1.54

Pin Power (uW/MHz)

Pin	V1	V2
A	0.00065	0.00083
B	0.00056	0.00072
C	0.00073	0.00094

Pin Capacitance (pf)

Pin	V1	V2
A	0.00114	0.00135
B	0.00102	0.00121
C	0.00103	0.00124

Max Leakage Power (uW)

V1	V2
0.00018402	0.00024194

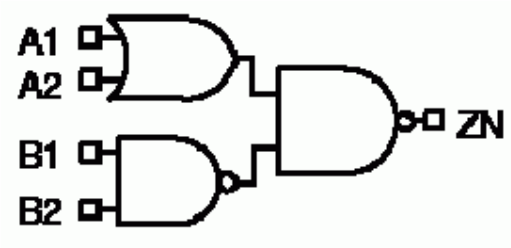
Delay Table (ns)

Description	V1	V2
A→ZN_FALL	0.02785	0.02533
A→ZN_RISE	0.05874	0.05407
B→ZN_FALL	0.02719	0.02500
B→ZN_RISE	0.05524	0.05113
C→ZN_FALL	0.02912	0.02660
C→ZN_RISE	0.06131	0.05675

MOAI22HS

Cell Description

the logical NAND of one OR2 and one NAND2 block.
ZN=(!((A1|A2)&(!(B1&B2))))



Function Table

A1	A2	B1	B2	ZN
0	0	X	X	1
0	1	0	X	0
0	1	1	0	0
0	1	1	1	1
1	X	0	X	0
1	X	1	0	0
1	X	1	1	1

Cell Size

CellName	Height(um)	Width(um)
MOAI22HSV1	1.26	1.26
MOAI22HSV2	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00043	0.00044
A2	0.00052	0.00053
B1	0.00083	0.00086
B2	0.00088	0.00091

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00060	0.00060
A2	0.00067	0.00067
B1	0.00071	0.00070
B2	0.00056	0.00055

Max Leakage Power (uW)

V1	V2
0.00030144	0.00034094

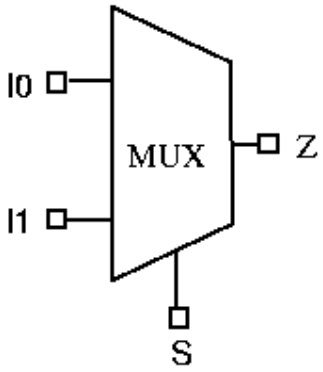
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.01981	0.02008
A1→ZN_RISE	0.02884	0.02889
A2→ZN_FALL	0.02233	0.02255
A2→ZN_RISE	0.03203	0.03203
B1→ZN_FALL	0.04332	0.04455
B1→ZN_RISE	0.03633	0.03413
B2→ZN_FALL	0.04584	0.04690
B2→ZN_RISE	0.03750	0.03527

MUX2HS

Cell Description

2-to-1 Multiplexer
Z=((I0&(!S))|(I1&S))



Function Table

S	I0	I1	Z
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

Cell Size

CellName	Height(um)	Width(um)
MUX2HSV1	1.26	1.68
MUX2HSV2	1.26	1.68

Pin Power (uW/MHz)

Pin	V1	V2
I0	0.00105	0.00112
I1	0.00089	0.00096
S	0.00111	0.00118

Pin Capacitance (pf)

Pin	V1	V2
I0	0.00056	0.00056
I1	0.00058	0.00058
S	0.00091	0.00091

Max Leakage Power (uW)

V1	V2
0.00056803	0.00058638

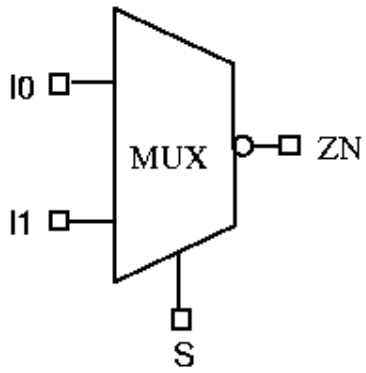
Delay Table (ns)

Description	V1	V2
I0→Z_FALL	0.05550	0.05614
I0→Z_RISE	0.04722	0.04704
I1→Z_FALL	0.04786	0.04822
I1→Z_RISE	0.03950	0.03912
S→Z_FALL	0.04378	0.04438
S→Z_RISE	0.04202	0.04176

MUX2NHS

Cell Description

2-to-1 Inverting Multiplexer
ZN=(!((I0&(!S))|(I1&S)))



Function Table

S	I0	I1	ZN
0	0	X	1
0	1	X	0
1	X	0	1
1	X	1	0

Cell Size

CellName	Height(um)	Width(um)
MUX2NHSV1	1.26	1.54
MUX2NHSV2	1.26	1.68

Pin Power (uW/MHz)

Pin	V1	V2
I0	0.00061	0.00068
I1	0.00065	0.00073
S	0.00066	0.00074

Pin Capacitance (pf)

Pin	V1	V2
I0	0.00056	0.00055
I1	0.00057	0.00057
S	0.00094	0.00100

Max Leakage Power (uW)

V1	V2
0.00037341	0.00039789

Delay Table (ns)

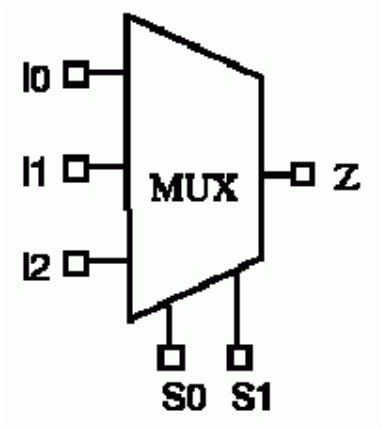
Description	V1	V2
I0→ZN_FALL	0.02657	0.02750
I0→ZN_RISE	0.03239	0.03388
I1→ZN_FALL	0.02600	0.02704
I1→ZN_RISE	0.03512	0.03723
S→ZN_FALL	0.02224	0.02241
S→ZN_RISE	0.02282	0.02393

MUX3HS

Cell Description

3-to-1 Multiplexer

Z=((I0&(!S0)&(!S1))|(I1&S0&(!S1))|(I2&S1))



Function Table

S1	S0	I0	I1	I2	Z
0	0	0	X	X	0
0	0	1	X	X	1
0	1	X	0	X	0
0	1	X	1	X	1
1	X	X	X	0	0
1	X	X	X	1	1

Cell Size

CellName	Height(um)	Width(um)
MUX3HSV1	1.26	3.50
MUX3HSV2	1.26	3.50

Pin Power (uW/MHz)

Pin	V1	V2
I0	0.00244	0.00255
I1	0.00217	0.00228
I2	0.00193	0.00204
S0	0.00278	0.00289
S1	0.00192	0.00202

Pin Capacitance (pf)

Pin	V1	V2
I0	0.00065	0.00065
I1	0.00060	0.00061
I2	0.00067	0.00067
S0	0.00151	0.00151
S1	0.00116	0.00115

Max Leakage Power (uW)

V1	V2
0.00083909	0.00082091

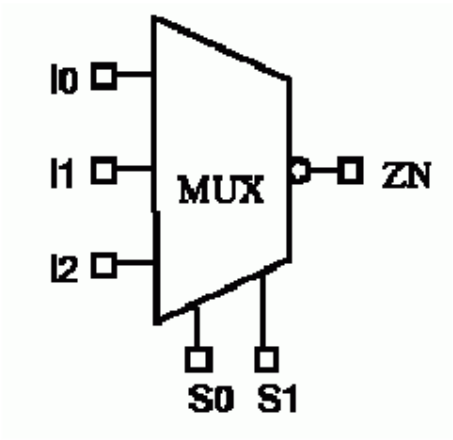
Delay Table (ns)

Description	V1	V2
I0→Z_FALL	0.10451	0.10565
I0→Z_RISE	0.10228	0.10314
I1→Z_FALL	0.09283	0.09403
I1→Z_RISE	0.09373	0.09480
I2→Z_FALL	0.07031	0.07197
I2→Z_RISE	0.07633	0.07774
S0→Z_FALL	0.10894	0.11017
S0→Z_RISE	0.10512	0.10611
S1→Z_FALL	0.06317	0.06408
S1→Z_RISE	0.07297	0.07388

MUX3NHS

Cell Description

3-to-1 Inverting Multiplexer
ZN=(!((I0&(!S0)&(!S1))|(I1&S0&(!S1))|(I2&S1)))



Function Table

S1	S0	I0	I1	I2	ZN
0	0	0	X	X	1
0	0	1	X	X	0
0	1	X	0	X	1
0	1	X	1	X	0
1	X	X	X	0	1
1	X	X	X	1	0

Cell Size

CellName	Height(um)	Width(um)
MUX3NHSV1	1.26	3.08
MUX3NHSV2	1.26	3.08

Pin Power (uW/MHz)

Pin	V1	V2
I0	0.00193	0.00200
I1	0.00166	0.00175
I2	0.00143	0.00150
S0	0.00228	0.00243
S1	0.00141	0.00147

Pin Capacitance (pf)

Pin	V1	V2
I0	0.00065	0.00066
I1	0.00061	0.00061
I2	0.00067	0.00068
S0	0.00151	0.00132
S1	0.00115	0.00115

Max Leakage Power (uW)

V1	V2
0.00074804	0.00085786

Delay Table (ns)

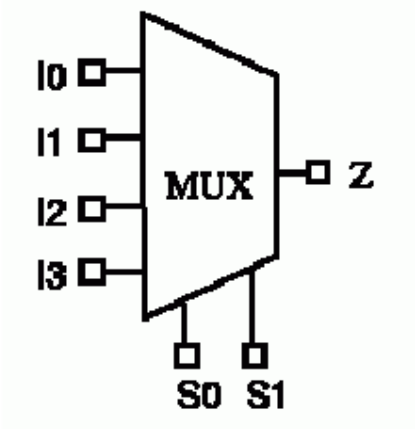
Description	V1	V2
I0→ZN_FALL	0.08498	0.08381
I0→ZN_RISE	0.08944	0.08725
I1→ZN_FALL	0.07646	0.07558
I1→ZN_RISE	0.07777	0.07625
I2→ZN_FALL	0.05910	0.05853
I2→ZN_RISE	0.05599	0.05458
S0→ZN_FALL	0.08801	0.08850
S0→ZN_RISE	0.09384	0.09285
S1→ZN_FALL	0.05493	0.05443
S1→ZN_RISE	0.04828	0.04684

MUX4HS

Cell Description

4-to-1 Multiplexer

Z=((I0&(!S0)&(!S1))|(I1&S0&(!S1))|(I2&(!S0)&S1)|(I3&S0&S1))



Function Table

S1	S0	I0	I1	I2	I3	Z
0	0	0	X	X	X	0
0	0	1	X	X	X	1
0	1	X	0	X	X	0
0	1	X	1	X	X	1
1	0	X	X	0	X	0
1	0	X	X	1	X	1
1	1	X	X	X	0	0
1	1	X	X	X	1	1

Cell Size

CellName	Height(um)	Width(um)
MUX4HSV1	1.26	4.06
MUX4HSV2	1.26	4.06

Pin Power (uW/MHz)

Pin	V1	V2
I0	0.00201	0.00210
I1	0.00230	0.00240
I2	0.00224	0.00233
I3	0.00247	0.00256
S0	0.00187	0.00197
S1	0.00334	0.00343

Pin Capacitance (pf)

Pin	V1	V2
I0	0.00066	0.00065
I1	0.00080	0.00078
I2	0.00062	0.00062
I3	0.00063	0.00063

S0	0.00141	0.00140
S1	0.00207	0.00206

Max Leakage Power (uW)

V1	V2
0.00091795	0.00089872

Delay Table (ns)

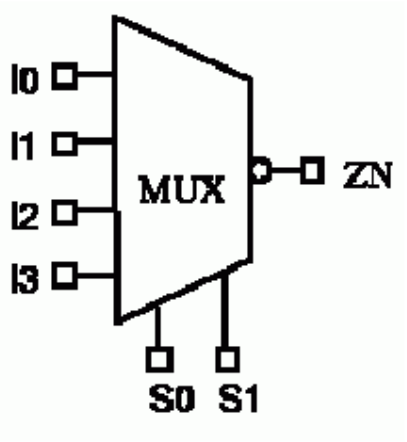
Description	V1	V2
I0→Z_FALL	0.08736	0.08805
I0→Z_RISE	0.08442	0.08428
I1→Z_FALL	0.09958	0.10061
I1→Z_RISE	0.10368	0.10376
I2→Z_FALL	0.09718	0.09776
I2→Z_RISE	0.09064	0.09044
I3→Z_FALL	0.10339	0.10441
I3→Z_RISE	0.10719	0.10724
S0→Z_FALL	0.06177	0.06280
S0→Z_RISE	0.07510	0.07538
S1→Z_FALL	0.10849	0.10930
S1→Z_RISE	0.10629	0.10622

MUX4NHS

Cell Description

4-to-1 Inverting Multiplexer

ZN=(!((I0&(!S0)&(!S1))|(I1&S0&(!S1))|(I2&(!S0)&S1)|(I3&S0&S1)))



Function Table

S1	S0	I0	I1	I2	I3	ZN
0	0	0	X	X	X	1
0	0	1	X	X	X	0
0	1	X	0	X	X	1
0	1	X	1	X	X	0
1	0	X	X	0	X	1
1	0	X	X	1	X	0
1	1	X	X	X	0	1
1	1	X	X	X	1	0

Cell Size

CellName	Height(um)	Width(um)
MUX4NHSV1	1.26	3.78
MUX4NHSV2	1.26	3.78

Pin Power (uW/MHz)

Pin	V1	V2
I0	0.00147	0.00157
I1	0.00178	0.00187
I2	0.00171	0.00180
I3	0.00194	0.00203
S0	0.00134	0.00143
S1	0.00281	0.00290

Pin Capacitance (pf)

Pin	V1	V2
I0	0.00065	0.00065
I1	0.00078	0.00079
I2	0.00062	0.00062
I3	0.00062	0.00063

S0	0.00141	0.00141
S1	0.00206	0.00206

Max Leakage Power (uW)

V1	V2
0.00082582	0.00087163

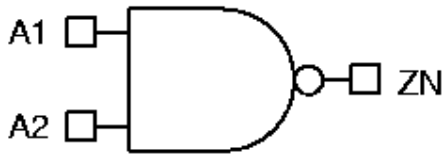
Delay Table (ns)

Description	V1	V2
I0→ZN_FALL	0.06630	0.06637
I0→ZN_RISE	0.07155	0.07150
I1→ZN_FALL	0.08385	0.08517
I1→ZN_RISE	0.08370	0.08341
I2→ZN_FALL	0.07143	0.07254
I2→ZN_RISE	0.08135	0.08121
I3→ZN_FALL	0.08718	0.08868
I3→ZN_RISE	0.08743	0.08732
S0→ZN_FALL	0.05507	0.05648
S0→ZN_RISE	0.04630	0.04594
S1→ZN_FALL	0.08711	0.08808
S1→ZN_RISE	0.09253	0.09246

NAND2HS

Cell Description

2-Input NAND
ZN=(!(A1&A2))



Function Table

A1	A2	ZN
0	X	1
1	0	1
1	1	0

Cell Size

CellName	Height(um)	Width(um)
NAND2HSV1	1.26	0.70
NAND2HSV2	1.26	0.70
NAND2HSV3	1.26	0.98
NAND2HSV8	1.26	1.68

Pin Power (uW/MHz)

Pin	V1	V2	V3	V8
A1	0.00027	0.00030	0.00045	0.00094
A2	0.00033	0.00036	0.00058	0.00139

Pin Capacitance (pf)

Pin	V1	V2	V3	V8
A1	0.00057	0.00064	0.00097	0.00219
A2	0.00059	0.00064	0.00115	0.00223

Max Leakage Power (uW)

V1	V2	V3	V8
0.00019670	0.00025660	0.00051499	0.00142525

Delay Table (ns)

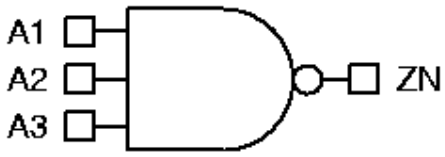
Description	V1	V2	V3	V8

A1→ZN_FALL	0.01430	0.01521	0.01351	0.01110
A1→ZN_RISE	0.01503	0.01265	0.01101	0.00925
A2→ZN_FALL	0.01592	0.01685	0.01592	0.01419
A2→ZN_RISE	0.01679	0.01382	0.01298	0.01114

NAND3HS

Cell Description

3-Input NAND
ZN=(!(A1&A2&A3))



Function Table

A1	A2	A3	ZN
0	X	X	1
1	0	X	1
1	1	0	1
1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
NAND3HSV1	1.26	0.84
NAND3HSV2	1.26	0.84
NAND3HSV3	1.26	1.26
NAND3HSV8	1.26	2.52

Pin Power (uW/MHz)

Pin	V1	V2	V3	V8
A1	0.00035	0.00040	0.00055	0.00125
A2	0.00041	0.00047	0.00068	0.00165
A3	0.00047	0.00053	0.00076	0.00195

Pin Capacitance (pf)

Pin	V1	V2	V3	V8
A1	0.00056	0.00062	0.00092	0.00217
A2	0.00058	0.00065	0.00110	0.00224
A3	0.00059	0.00065	0.00114	0.00221

Max Leakage Power (uW)

V1	V2	V3	V8
0.00031824	0.00041923	0.00052852	0.00197742

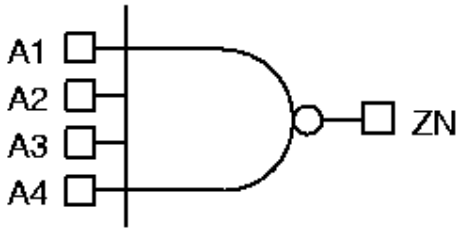
Delay Table (ns)

Description	V1	V2	V3	V8
A1→ZN_FALL	0.02145	0.02364	0.01969	0.01708
A1→ZN_RISE	0.01685	0.01428	0.01258	0.01051
A2→ZN_FALL	0.02424	0.02660	0.02374	0.02200
A2→ZN_RISE	0.01832	0.01532	0.01454	0.01230
A3→ZN_FALL	0.02577	0.02788	0.02486	0.02390
A3→ZN_RISE	0.02014	0.01652	0.01590	0.01348

NAND4HS

Cell Description

4-Input NAND
ZN=(!(A1&A2&A3&A4))



Function Table

A1	A2	A3	A4	ZN
0	X	X	X	1
1	0	X	X	1
1	1	0	X	1
1	1	1	0	1
1	1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
NAND4HSV1	1.26	0.98
NAND4HSV2	1.26	0.98
NAND4HSV3	1.26	1.68
NAND4HSV8	1.26	2.24

Pin Power (uW/MHz)

Pin	V1	V2	V3	V8
A1	0.00032	0.00044	0.00061	0.00290
A2	0.00038	0.00050	0.00075	0.00296
A3	0.00046	0.00058	0.00087	0.00303
A4	0.00052	0.00064	0.00094	0.00308

Pin Capacitance (pf)

Pin	V1	V2	V3	V8
A1	0.00052	0.00061	0.00092	0.00062
A2	0.00056	0.00065	0.00109	0.00067
A3	0.00054	0.00063	0.00118	0.00065
A4	0.00054	0.00064	0.00117	0.00066

Max Leakage Power (uW)

V1	V2	V3	V8
0.00026184	0.00061938	0.00076279	0.00148885

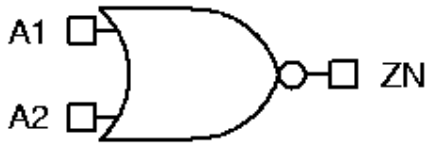
Delay Table (ns)

Description	V1	V2	V3	V8
A1→ZN_FALL	0.02477	0.03118	0.02543	0.08505
A1→ZN_RISE	0.02133	0.01495	0.01317	0.04869
A2→ZN_FALL	0.02877	0.03526	0.03125	0.08916
A2→ZN_RISE	0.02328	0.01578	0.01506	0.04947
A3→ZN_FALL	0.03227	0.03883	0.03515	0.09275
A3→ZN_RISE	0.02598	0.01705	0.01661	0.05127
A4→ZN_FALL	0.03364	0.04015	0.03564	0.09402
A4→ZN_RISE	0.02850	0.01805	0.01752	0.05337

NOR2HS

Cell Description

2-Input NOR
ZN=(!(A1|A2))



Function Table

A1	A2	ZN
0	0	1
0	1	0
1	X	0

Cell Size

CellName	Height(um)	Width(um)
NOR2HSV1	1.26	0.56
NOR2HSV2	1.26	0.56
NOR2HSV3	1.26	0.98
NOR2HSV8	1.26	1.68

Pin Power (uW/MHz)

Pin	V1	V2	V3	V8
A1	0.00028	0.00030	0.00041	0.00089
A2	0.00036	0.00038	0.00066	0.00146

Pin Capacitance (pf)

Pin	V1	V2	V3	V8
A1	0.00056	0.00061	0.00093	0.00204
A2	0.00063	0.00067	0.00100	0.00225

Max Leakage Power (uW)

V1	V2	V3	V8
0.00013698	0.00016259	0.00033955	0.00076427

Delay Table (ns)

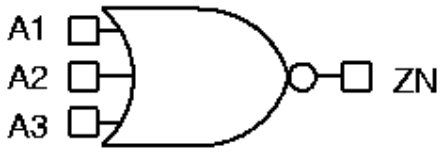
Description	V1	V2	V3	V8

A1→ZN_FALL	0.01240	0.01050	0.00911	0.00797
A1→ZN_RISE	0.02131	0.02249	0.01743	0.01435
A2→ZN_FALL	0.01341	0.01109	0.01030	0.00908
A2→ZN_RISE	0.02365	0.02471	0.02231	0.01877

NOR3HS

Cell Description

3-Input NOR
ZN=(!(A1|A2|A3))



Function Table

A1	A2	A3	ZN
0	0	0	1
0	0	1	0
0	1	X	0
1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
NOR3HSV1	1.26	0.84
NOR3HSV2	1.26	0.84
NOR3HSV3	1.26	1.26
NOR3HSV8	1.26	2.52

Pin Power (uW/MHz)

Pin	V1	V2	V3	V8
A1	0.00031	0.00039	0.00048	0.00111
A2	0.00037	0.00049	0.00066	0.00164
A3	0.00043	0.00057	0.00078	0.00209

Pin Capacitance (pf)

Pin	V1	V2	V3	V8
A1	0.00048	0.00058	0.00084	0.00200
A2	0.00054	0.00063	0.00107	0.00211
A3	0.00056	0.00068	0.00117	0.00228

Max Leakage Power (uW)

V1	V2	V3	V8
0.00023449	0.00028350	0.00047955	0.00106097

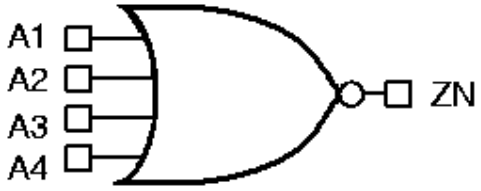
Delay Table (ns)

Description	V1	V2	V3	V8
A1→ZN_FALL	0.01242	0.01131	0.00952	0.00854
A1→ZN_RISE	0.04016	0.03593	0.02891	0.02221
A2→ZN_FALL	0.01328	0.01222	0.01080	0.00964
A2→ZN_RISE	0.04575	0.04181	0.03716	0.03099
A3→ZN_FALL	0.01358	0.01251	0.01110	0.00987
A3→ZN_RISE	0.04778	0.04418	0.03920	0.03433

NOR4HS

Cell Description

4-Input NOR
ZN=(!(A1|A2|A3|A4))



Function Table

A1	A2	A3	A4	ZN
0	0	0	0	1
0	0	0	1	0
0	0	1	X	0
0	1	X	X	0
1	X	X	X	0

Cell Size

CellName	Height(um)	Width(um)
NOR4HSV1	1.26	0.98
NOR4HSV2	1.26	0.98
NOR4HSV3	1.26	1.68
NOR4HSV8	1.26	2.10

Pin Power (uW/MHz)

Pin	V1	V2	V3	V8
A1	0.00036	0.00042	0.00060	0.00291
A2	0.00045	0.00051	0.00075	0.00300
A3	0.00055	0.00061	0.00092	0.00310
A4	0.00063	0.00069	0.00104	0.00319

Pin Capacitance (pf)

Pin	V1	V2	V3	V8
A1	0.00053	0.00057	0.00085	0.00060
A2	0.00057	0.00062	0.00106	0.00061
A3	0.00059	0.00062	0.00119	0.00064
A4	0.00061	0.00066	0.00121	0.00065

Max Leakage Power (uW)

V1	V2	V3	V8
0.00031362	0.00037670	0.00067853	0.00119549

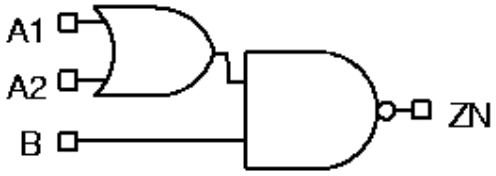
Delay Table (ns)

Description	V1	V2	V3	V8
A1→ZN_FALL	0.01349	0.01175	0.01037	0.04227
A1→ZN_RISE	0.04239	0.04809	0.04182	0.11663
A2→ZN_FALL	0.01470	0.01246	0.01139	0.04355
A2→ZN_RISE	0.05151	0.05699	0.05280	0.12662
A3→ZN_FALL	0.01557	0.01297	0.01211	0.04482
A3→ZN_RISE	0.05800	0.06357	0.06146	0.13316
A4→ZN_FALL	0.01568	0.01293	0.01206	0.04555
A4→ZN_RISE	0.06009	0.06558	0.06272	0.13711

OAI21HS

Cell Description

2-1 OAI
ZN=(!((A1|A2)&B))



Function Table

A1	A2	B	ZN
0	0	X	1
0	1	0	1
0	1	1	0
1	X	0	1
1	X	1	0

Cell Size

CellName	Height(um)	Width(um)
OAI21HSV1	1.26	0.84
OAI21HSV2	1.26	0.84

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00034	0.00046
A2	0.00041	0.00054
B	0.00025	0.00033

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00057	0.00066
A2	0.00057	0.00069
B	0.00054	0.00066

Max Leakage Power (uW)

V1	V2
0.00021683	0.00028581

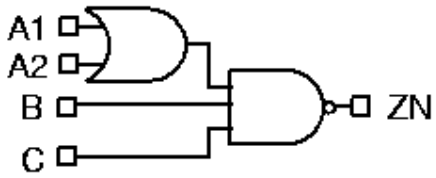
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.02090	0.01942
A1→ZN_RISE	0.03081	0.02838
A2→ZN_FALL	0.02293	0.02144
A2→ZN_RISE	0.03343	0.03107
B→ZN_FALL	0.01648	0.01517
B→ZN_RISE	0.01391	0.01269

OAI211HS

Cell Description

2-1-1 OAI
ZN=(!((A1|A2)&B&C))



Function Table

A1	A2	B	C	ZN
0	0	X	X	1
0	1	0	X	1
0	1	1	0	1
0	1	1	1	0
1	X	0	X	1
1	X	1	0	1
1	X	1	1	0

Cell Size

CellName	Height(um)	Width(um)
OAI211HSV1	1.26	0.98
OAI211HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00047	0.00060
A2	0.00053	0.00069
B	0.00034	0.00043
C	0.00039	0.00049

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00051	0.00061
A2	0.00058	0.00069
B	0.00057	0.00068
C	0.00057	0.00068

Max Leakage Power (uW)

V1	V2
0.00035325	0.00046589

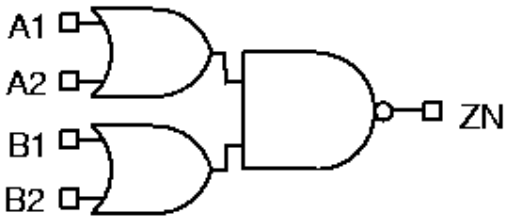
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.03353	0.03049
A1→ZN_RISE	0.03670	0.03311
A2→ZN_FALL	0.03649	0.03378
A2→ZN_RISE	0.03936	0.03599
B→ZN_FALL	0.02681	0.02404
B→ZN_RISE	0.01599	0.01428
C→ZN_FALL	0.02941	0.02683
C→ZN_RISE	0.01695	0.01533

OAI22HS

Cell Description

2-2 OAI
ZN=(!((A1|A2)&(B1|B2)))



Function Table

A1	A2	B1	B2	ZN
0	0	X	X	1
0	1	0	0	1
0	1	0	1	0
0	1	1	X	0
1	X	0	0	1
1	X	0	1	0
1	X	1	X	0

Cell Size

CellName	Height(um)	Width(um)
OAI22HSV1	1.26	0.98
OAI22HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00030	0.00037
A2	0.00037	0.00046
B1	0.00045	0.00057
B2	0.00051	0.00066

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00055	0.00065
A2	0.00053	0.00063
B1	0.00051	0.00061
B2	0.00057	0.00069

Max Leakage Power (uW)

V1	V2
0.00025506	0.00033674

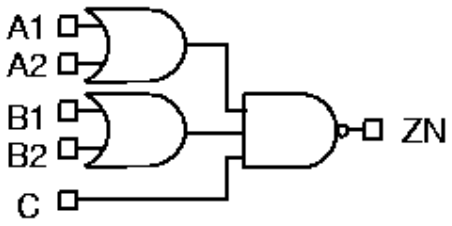
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.01769	0.01565
A1→ZN_RISE	0.02649	0.02295
A2→ZN_FALL	0.01979	0.01773
A2→ZN_RISE	0.02983	0.02620
B1→ZN_FALL	0.02318	0.02118
B1→ZN_RISE	0.03499	0.03153
B2→ZN_FALL	0.02486	0.02300
B2→ZN_RISE	0.03753	0.03446

OAI221HS

Cell Description

2-2-1 OAI
ZN=(!((A1|A2)&(B1|B2)&C))



Function Table

A1	A2	B1	B2	C	ZN
0	0	X	X	X	1
0	1	0	0	X	1
0	1	0	1	0	1
0	1	0	1	1	0
0	1	1	X	0	1
0	1	1	X	1	0
1	X	0	0	X	1
1	X	0	1	0	1
1	X	0	1	1	0
1	X	1	X	0	1
1	X	1	X	1	0

Cell Size

CellName	Height(um)	Width(um)
OAI221HSV1	1.26	1.26
OAI221HSV2	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00048	0.00060
A2	0.00054	0.00070
B1	0.00062	0.00078
B2	0.00067	0.00086
C	0.00040	0.00051

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00052	0.00062
A2	0.00057	0.00068

B1	0.00054	0.00063
B2	0.00058	0.00069
C	0.00070	0.00084

Max Leakage Power (uW)

V1	V2
0.00032033	0.00042232

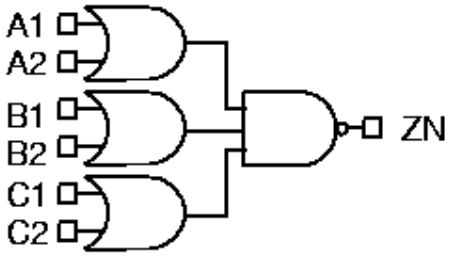
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.03433	0.03131
A1→ZN_RISE	0.03604	0.03229
A2→ZN_FALL	0.03785	0.03503
A2→ZN_RISE	0.03929	0.03560
B1→ZN_FALL	0.03998	0.03651
B1→ZN_RISE	0.04335	0.03897
B2→ZN_FALL	0.04279	0.03967
B2→ZN_RISE	0.04568	0.04157
C→ZN_FALL	0.02949	0.02676
C→ZN_RISE	0.01813	0.01625

OAI222HS

Cell Description

2-2-2 OAI
ZN=(!((A1|A2)&(B1|B2)&(C1|C2)))



Function Table

A1	A2	B1	B2	C1	C2	ZN
0	0	X	X	X	X	1
0	1	0	0	X	X	1
0	1	0	1	0	0	1
0	1	0	1	0	1	0
0	1	0	1	1	X	0
0	1	1	X	0	0	1
0	1	1	X	0	1	0
0	1	1	X	1	X	0
1	X	0	0	X	X	1
1	X	0	1	0	0	1
1	X	0	1	0	1	0
1	X	0	1	1	X	0
1	X	1	X	0	0	1
1	X	1	X	0	1	0
1	X	1	X	1	X	0

Cell Size

CellName	Height(um)	Width(um)
OAI222HSV1	1.26	1.54
OAI222HSV2	1.26	1.54

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00057	0.00072
A2	0.00062	0.00080
B1	0.00069	0.00090
B2	0.00075	0.00098
C1	0.00043	0.00053
C2	0.00047	0.00059

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00056	0.00066
A2	0.00055	0.00066
B1	0.00053	0.00061
B2	0.00058	0.00069
C1	0.00069	0.00083
C2	0.00052	0.00063

Max Leakage Power (uW)

V1	V2
0.00034373	0.00045343

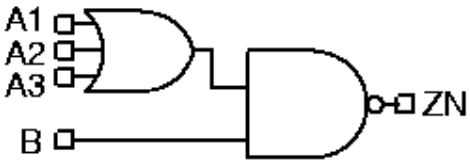
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.03709	0.03397
A1→ZN_RISE	0.04049	0.03649
A2→ZN_FALL	0.03950	0.03676
A2→ZN_RISE	0.04257	0.03889
B1→ZN_FALL	0.04200	0.03907
B1→ZN_RISE	0.04675	0.04284
B2→ZN_FALL	0.04445	0.04177
B2→ZN_RISE	0.04919	0.04557
C1→ZN_FALL	0.02961	0.02627
C1→ZN_RISE	0.03361	0.02933
C2→ZN_FALL	0.02966	0.02675
C2→ZN_RISE	0.03431	0.03049

OAI31HS

Cell Description

3-1 OAI
ZN=(!((A1|A2|A3)&B))



Function Table

A1	A2	A3	B	ZN
0	0	0	X	1
0	0	1	0	1
0	0	1	1	0
0	1	X	0	1
0	1	X	1	0
1	X	X	0	1
1	X	X	1	0

Cell Size

CellName	Height(um)	Width(um)
OAI31HSV1	1.26	0.98
OAI31HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00036	0.00048
A2	0.00043	0.00057
A3	0.00049	0.00065
B	0.00028	0.00036

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00052	0.00065
A2	0.00053	0.00063
A3	0.00057	0.00070
B	0.00054	0.00066

Max Leakage Power (uW)

V1	V2
0.00022951	0.00030280

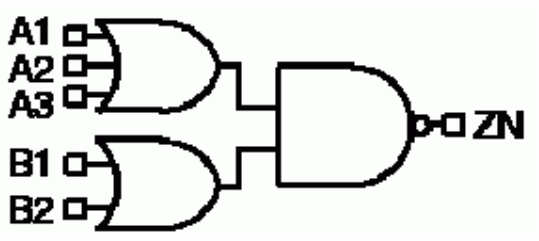
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.02159	0.02000
A1→ZN_RISE	0.04575	0.04212
A2→ZN_FALL	0.02365	0.02196
A2→ZN_RISE	0.05114	0.04750
A3→ZN_FALL	0.02471	0.02293
A3→ZN_RISE	0.05338	0.04984
B→ZN_FALL	0.01631	0.01479
B→ZN_RISE	0.01413	0.01271

OAI32HS

Cell Description

3-2 OAI
ZN=(!((A1|A2|A3)&(B1|B2)))



Function Table

A1	A2	A3	B1	B2	ZN
0	0	0	X	X	1
0	0	1	0	0	1
0	0	1	0	1	0
0	0	1	1	X	0
0	1	X	0	0	1
0	1	X	0	1	0
0	1	X	1	X	0
1	X	X	0	0	1
1	X	X	0	1	0
1	X	X	1	X	0

Cell Size

CellName	Height(um)	Width(um)
OAI32HSV1	1.26	1.12
OAI32HSV2	1.26	1.12

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00037	0.00046
A2	0.00044	0.00055
A3	0.00052	0.00065
B1	0.00054	0.00068
B2	0.00061	0.00078

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00052	0.00061
A2	0.00052	0.00062
A3	0.00056	0.00067

B1	0.00051	0.00060
B2	0.00058	0.00070

Max Leakage Power (uW)

V1	V2
0.00027200	0.00036015

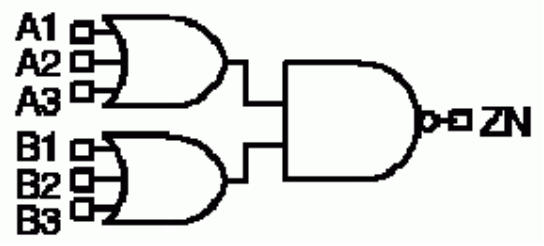
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.01943	0.01725
A1→ZN_RISE	0.04259	0.03691
A2→ZN_FALL	0.02150	0.01941
A2→ZN_RISE	0.04826	0.04301
A3→ZN_FALL	0.02381	0.02146
A3→ZN_RISE	0.05338	0.04755
B1→ZN_FALL	0.02475	0.02243
B1→ZN_RISE	0.03975	0.03546
B2→ZN_FALL	0.02659	0.02441
B2→ZN_RISE	0.04247	0.03854

OAI33HS

Cell Description

3-3 OAI
ZN=(!((A1|A2|A3)&(B1|B2|B3)))



Function Table

A1	A2	A3	B1	B2	B3	ZN
0	0	0	X	X	X	1
0	0	1	0	0	0	1
0	0	1	0	0	1	0
0	0	1	0	1	X	0
0	0	1	1	X	X	0
0	1	X	0	0	0	1
0	1	X	0	0	1	0
0	1	X	0	1	X	0
0	1	X	1	X	X	0
1	X	X	0	0	0	1
1	X	X	0	0	1	0
1	X	X	0	1	X	0
1	X	X	1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
OAI33HSV1	1.26	1.26
OAI33HSV2	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00056	0.00070
A2	0.00062	0.00079
A3	0.00069	0.00087
B1	0.00039	0.00047
B2	0.00045	0.00057
B3	0.00052	0.00066

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00051	0.00059
A2	0.00057	0.00067
A3	0.00059	0.00070
B1	0.00055	0.00064
B2	0.00054	0.00064
B3	0.00055	0.00064

Max Leakage Power (uW)

V1	V2
0.00028777	0.00038046

Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.02525	0.02272
A1→ZN_RISE	0.05950	0.05290
A2→ZN_FALL	0.02715	0.02477
A2→ZN_RISE	0.06505	0.05893
A3→ZN_FALL	0.02857	0.02601
A3→ZN_RISE	0.06767	0.06128
B1→ZN_FALL	0.01875	0.01672
B1→ZN_RISE	0.04245	0.03669
B2→ZN_FALL	0.02078	0.01874
B2→ZN_RISE	0.04849	0.04296
B3→ZN_FALL	0.02265	0.02035
B3→ZN_RISE	0.05253	0.04646

OR2HS

Cell Description

2-Input OR
Z=(A1|A2)

Function Table

A1	A2	Z
0	0	0
0	1	1
1	X	1

Cell Size

CellName	Height(um)	Width(um)
OR2HSV1	1.26	0.84
OR2HSV2	1.26	0.84
OR2HSV8	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2	V8
A1	0.00062	0.00071	0.00192
A2	0.00068	0.00077	0.00202

Pin Capacitance (pf)

Pin	V1	V2	V8
A1	0.00046	0.00046	0.00063
A2	0.00048	0.00048	0.00068

Max Leakage Power (uW)

V1	V2	V8
0.00018676	0.00020459	0.00087261

Delay Table (ns)

Description	V1	V2	V8
A1→Z_FALL	0.05262	0.05466	0.06441

A1→Z_RISE	0.02944	0.02929	0.02957
A2→Z_FALL	0.05798	0.05964	0.06811
A2→Z_RISE	0.03176	0.03139	0.03095

OR3HS

Cell Description

3-Input OR
Z=(A1|A2|A3)

Function Table

A1	A2	A3	Z
0	0	0	0
0	0	1	1
0	1	X	1
1	X	X	1

Cell Size

CellName	Height(um)	Width(um)
OR3HSV1	1.26	0.98
OR3HSV2	1.26	0.98
OR3HSV8	1.26	1.54

Pin Power (uW/MHz)

Pin	V1	V2	V8
A1	0.00075	0.00085	0.00210
A2	0.00084	0.00094	0.00218
A3	0.00095	0.00105	0.00229

Pin Capacitance (pf)

Pin	V1	V2	V8
A1	0.00053	0.00053	0.00061
A2	0.00055	0.00056	0.00064
A3	0.00059	0.00059	0.00067

Max Leakage Power (uW)

V1	V2	V8
0.00025938	0.00029354	0.00102500

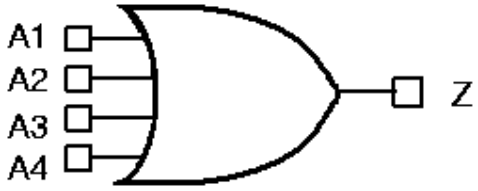
Delay Table (ns)

Description	V1	V2	V8
A1→Z_FALL	0.05483	0.05682	0.09619
A1→Z_RISE	0.03464	0.03465	0.03111
A2→Z_FALL	0.06080	0.06287	0.10211
A2→Z_RISE	0.03730	0.03733	0.03209
A3→Z_FALL	0.06517	0.06718	0.10607
A3→Z_RISE	0.04025	0.04023	0.03332

OR4HS

Cell Description

4-Input OR
Z=(A1|A2|A3|A4)



Function Table

A1	A2	A3	A4	Z
0	0	0	0	0
0	0	0	1	1
0	0	1	X	1
0	1	X	X	1
1	X	X	X	1

Cell Size

CellName	Height(um)	Width(um)
OR4HSV1	1.26	1.12
OR4HSV2	1.26	1.12
OR4HSV8	1.26	1.68

Pin Power (uW/MHz)

Pin	V1	V2	V8
A1	0.00078	0.00086	0.00216
A2	0.00089	0.00096	0.00226
A3	0.00097	0.00105	0.00235
A4	0.00107	0.00114	0.00245

Pin Capacitance (pf)

Pin	V1	V2	V8
A1	0.00052	0.00052	0.00061
A2	0.00057	0.00054	0.00062
A3	0.00054	0.00055	0.00063
A4	0.00058	0.00058	0.00066

Max Leakage Power (uW)

V1	V2	V8

0.00030253	0.00033775	0.00112182

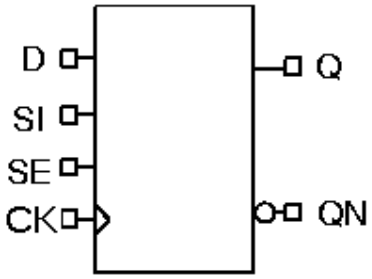
Delay Table (ns)

Description	V1	V2	V8
A1→Z_FALL	0.07026	0.07112	0.12402
A1→Z_RISE	0.03619	0.03518	0.03124
A2→Z_FALL	0.08134	0.08150	0.13433
A2→Z_RISE	0.03923	0.03810	0.03233
A3→Z_FALL	0.08624	0.08739	0.14015
A3→Z_RISE	0.04126	0.04065	0.03336
A4→Z_FALL	0.09138	0.09181	0.14492
A4→Z_RISE	0.04371	0.04263	0.03443

SDHS

Cell Description

Scan D Flip-Flop
Q = rising (CK) ? (SE&SI | !SE&D) : pre_Q
QN = !Q



Function Table

CK<1>	CK	SE	SI	D	Q
0	0	X	X	X	Q<1>
0	1	0	X	0	0
0	1	0	X	1	1
0	1	1	0	X	0
0	1	1	1	X	1
1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
SDHSV1	1.26	4.20
SDHSV2	1.26	4.06

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00155	0.00155
D	0.00032	0.00032
Q	0.00092	0.00101
QN	0.00090	0.00100
SE	0.00068	0.00068
SI	0.00036	0.00036

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00045	0.00045
D	0.00046	0.00046
SE	0.00098	0.00098
SI	0.00038	0.00038

Max Leakage Power (uW)

V1	V2
0.00057941	0.00061080

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.11752	0.11872
CK→Q_RISE	0.11308	0.11585
CK→QN_FALL	0.08659	0.08717
CK→QN_RISE	0.09555	0.09524

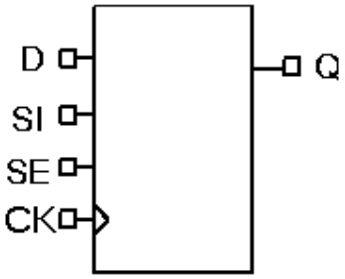
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.00857	-0.00573
D	hold_RISE→CK	-0.04008	-0.04007
D	setup_FALL→CK	0.04580	0.04867
D	setup_RISE→CK	0.06011	0.06298
SE	hold_FALL→CK	-0.01718	-0.01144
SE	hold_RISE→CK	-0.04866	-0.04865
SE	setup_FALL→CK	0.06298	0.06584
SE	setup_RISE→CK	0.07442	0.07728
SI	hold_FALL→CK	-0.04293	-0.03720
SI	hold_RISE→CK	-0.05439	-0.05153
SI	setup_FALL→CK	0.09159	0.09446
SI	setup_RISE→CK	0.07729	0.08016
CK	minpwh	0.09172	0.09875
CK	minpwl	0.13387	0.13829

SDQHS

Cell Description

Scan D Flip-Flop
Q = rising (CK) ? (SE&SI | !SE&D) : pre_Q



Function Table

CK<1>	CK	SE	D	SI	Q
0	0	X	X	X	Q<1>
0	1	0	0	X	0
0	1	0	1	X	1
0	1	1	X	0	0
0	1	1	X	1	1
1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
SDQHSV1	1.26	4.06
SDQHSV2	1.26	4.06

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00149	0.00149
D	0.00031	0.00031
Q	0.00139	0.00149
SE	0.00068	0.00068
SI	0.00035	0.00035

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00045	0.00045
D	0.00048	0.00048
SE	0.00098	0.00098
SI	0.00038	0.00039

Max Leakage Power (uW)

V1	V2
0.00046738	0.00048040

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.11014	0.11011
CK→Q_RISE	0.10362	0.10322

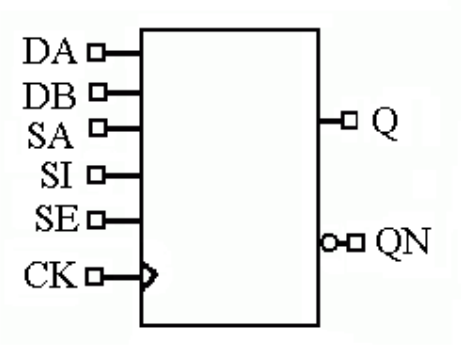
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.01144	-0.00858
D	hold_RISE→CK	-0.03721	-0.03721
D	setup_FALL→CK	0.04579	0.04579
D	setup_RISE→CK	0.05438	0.05726
SE	hold_FALL→CK	-0.01718	-0.01431
SE	hold_RISE→CK	-0.05153	-0.05153
SE	setup_FALL→CK	0.06011	0.06012
SE	setup_RISE→CK	0.07156	0.07442
SI	hold_FALL→CK	-0.04295	-0.04008
SI	hold_RISE→CK	-0.05726	-0.05726
SI	setup_FALL→CK	0.08588	0.08873
SI	setup_RISE→CK	0.07729	0.08015
CK	minpwh	0.06008	0.06008
CK	minpwl	0.12510	0.12510

SDXHS

Cell Description

Scan D Flip-Flop with Mux Inputs
Q = rising (CK) ? (SE&SI | !SE&(DA&SA|DB&!SA)) : pre_Q
QN = !Q



Function Table

CK<1>	CK	SA	DB	DA	SE	SI	Q
0	0	X	X	X	X	X	Q<1>
0	1	0	0	X	0	X	0
0	1	0	0	X	1	0	0
0	1	0	0	X	1	1	1
0	1	0	1	X	0	X	1
0	1	0	1	X	1	0	0
0	1	0	1	X	1	1	1
0	1	1	X	0	0	X	0
0	1	1	X	0	1	0	0
0	1	1	X	0	1	1	1
0	1	1	X	1	0	X	1
0	1	1	X	1	1	0	0
0	1	1	X	1	1	1	1
1	X	X	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
SDXHSV1	1.26	5.32
SDXHSV2	1.26	5.32

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00131	0.00131
DA	0.00018	0.00018
DB	0.00018	0.00018
Q	0.00091	0.00100
QN	0.00090	0.00100
SA	0.00052	0.00052
SE	0.00077	0.00077
SI	0.00041	0.00041

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00044	0.00044
DA	0.00045	0.00045
DB	0.00090	0.00090
SA	0.00091	0.00091
SE	0.00103	0.00103
SI	0.00041	0.00041

Max Leakage Power (uW)

V1	V2
0.00064975	0.00069959

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.11191	0.11340
CK→Q_RISE	0.10994	0.11224
CK→QN_FALL	0.08419	0.08429
CK→QN_RISE	0.09002	0.08876

Timing Constraints (ns)

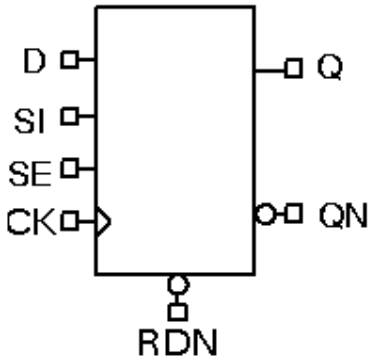
Pin	Requirement	V1	V2
DA	hold_FALL→CK	-0.02003	-0.01716
DA	hold_RISE→CK	-0.05152	-0.05152
DA	setup_FALL→CK	0.06010	0.06011
DA	setup_RISE→CK	0.06869	0.06869
DB	hold_FALL→CK	-0.02289	-0.02003
DB	hold_RISE→CK	-0.04866	-0.04866
DB	setup_FALL→CK	0.06010	0.06297
DB	setup_RISE→CK	0.06584	0.06870
SA	hold_FALL→CK	-0.05725	-0.05725
SA	hold_RISE→CK	-0.02576	-0.02289
SA	setup_FALL→CK	0.07441	0.07441
SA	setup_RISE→CK	0.06297	0.06583
SE	hold_FALL→CK	-0.01144	-0.00857
SE	hold_RISE→CK	-0.05438	-0.05438
SE	setup_FALL→CK	0.05724	0.06010
SE	setup_RISE→CK	0.07728	0.08014
SI	hold_FALL→CK	-0.04007	-0.03721
SI	hold_RISE→CK	-0.06012	-0.05726
SI	setup_FALL→CK	0.09159	0.09445
SI	setup_RISE→CK	0.08301	0.08588

CK	minpwh	0.08816	0.09515
CK	minpwl	0.12509	0.12509

SDRNHS

Cell Description

Scan D Flip-Flop with Async Clear
Q = !RDN ? 0 : rising (CK) ? (SE&SI | !SE&D) : pre_Q
QN = !Q



Function Table

RDN	CK<1>	CK	SE	SI	D	Q
0	X	X	X	X	X	0
1	0	0	X	X	X	Q<1>
1	0	1	0	X	0	0
1	0	1	0	X	1	1
1	0	1	1	0	X	0
1	0	1	1	1	X	1
1	1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
SDRNHSV1	1.26	5.04
SDRNHSV2	1.26	5.04

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00170	0.00170
D	0.00019	0.00019
Q	0.00114	0.00123
QN	0.00116	0.00125
RDN	0.00043	0.00043
SE	0.00049	0.00049
SI	0.00022	0.00022

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00045	0.00045
D	0.00039	0.00039
RDN	0.00174	0.00174
SE	0.00080	0.00080

SI	0.00035	0.00035

Max Leakage Power (uW)

V1	V2
0.00074428	0.00078784

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.11712	0.11850
CK→Q_RISE	0.12483	0.12823
RDN→Q_FALL	0.03120	0.03100
CK→QN_FALL	0.08647	0.08780
CK→QN_RISE	0.09512	0.09473
RDN→QN_RISE	0.09563	0.09698

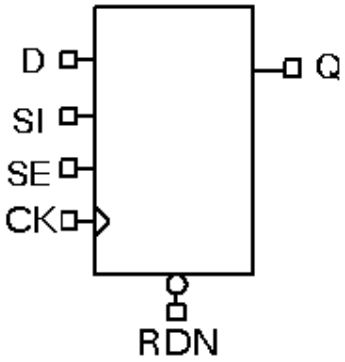
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.01717	-0.01432
D	hold_RISE→CK	-0.06298	-0.06012
D	setup_FALL→CK	0.08014	0.08302
D	setup_RISE→CK	0.10020	0.10306
RDN	setup_RISE→CK	0.12595	0.12881
RDN	hold_RISE→CK	-0.10877	-0.10877
SE	hold_FALL→CK	-0.02576	-0.01717
SE	hold_RISE→CK	-0.06583	-0.06299
SE	setup_FALL→CK	0.10590	0.10591
SE	setup_RISE→CK	0.10877	0.11164
SI	hold_FALL→CK	-0.04296	-0.04007
SI	hold_RISE→CK	-0.07730	-0.07443
SI	setup_FALL→CK	0.11737	0.12023
SI	setup_RISE→CK	0.11737	0.12310
CK	minpwh	0.09524	0.10227
CK	minpwl	0.15590	0.15587
RDN	minpwl	0.05301	0.05653

SDRNQHS

Cell Description

Scan D Flip-Flop with Async Clear
Q = !RDN ? 0 : rising (CK) ? (SE&SI | !SE&D) : pre_Q



Function Table

RDN	CK<1>	CK	SE	D	SI	Q
0	X	X	X	X	X	0
1	0	0	X	X	X	Q<1>
1	0	1	0	0	X	0
1	0	1	0	1	X	1
1	0	1	1	X	0	0
1	0	1	1	X	1	1
1	1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
SDRNQHSV1	1.26	4.76
SDRNQHSV2	1.26	4.76

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00166	0.00166
D	0.00018	0.00018
Q	0.00181	0.00188
RDN	0.00042	0.00042
SE	0.00054	0.00054
SI	0.00021	0.00021

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00045	0.00045
D	0.00041	0.00041
RDN	0.00161	0.00160
SE	0.00103	0.00103
SI	0.00035	0.00035

Max Leakage Power (uW)

V1	V2
0.00062457	0.00064639

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.11205	0.11177
CK→Q_RISE	0.10731	0.10688
RDN→Q_FALL	0.05383	0.05445

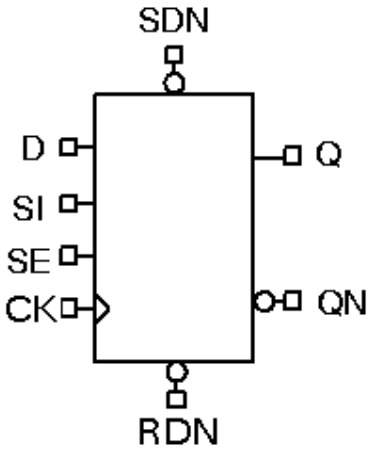
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.02576	-0.02003
D	hold_RISE→CK	-0.06012	-0.06012
D	setup_FALL→CK	0.06870	0.06870
D	setup_RISE→CK	0.09160	0.09447
RDN	setup_RISE→CK	0.12308	0.12595
RDN	hold_RISE→CK	-0.10878	-0.11164
SE	hold_FALL→CK	-0.03150	-0.02578
SE	hold_RISE→CK	-0.07730	-0.07730
SE	setup_FALL→CK	0.08302	0.08589
SE	setup_RISE→CK	0.11164	0.11450
SI	hold_FALL→CK	-0.05438	-0.05153
SI	hold_RISE→CK	-0.08302	-0.08302
SI	setup_FALL→CK	0.10591	0.10877
SI	setup_RISE→CK	0.11736	0.12024
CK	minpwh	0.06004	0.06004
CK	minpwl	0.14710	0.15148
RDN	minpwl	0.06709	0.07412

SDRSNHS

Cell Description

Scan D Flip-Flop with Async Clear and Set
Q = !SDN ? 1 : !RDN ? 0 : rising (CK) ? (SE&SI | !SE&D) : pre_Q
QN = !Q



Function Table

RDN	SDN	CK<1>	CK	SE	D	SI	Q
0	0	X	X	X	X	X	1
0	1	X	X	X	X	X	0
1	0	X	X	X	X	X	1
1	1	0	0	X	X	X	Q<1>
1	1	0	1	0	0	X	0
1	1	0	1	0	1	X	1
1	1	0	1	1	X	0	0
1	1	0	1	1	X	1	1
1	1	1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
SDRSNHSV1	1.26	7.14
SDRSNHSV2	1.26	7.14

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00213	0.00213
D	0.00018	0.00018
Q	0.00134	0.00142
QN	0.00133	0.00141
RDN	0.00105	0.00105
SDN	0.00018	0.00018
SE	0.00053	0.00053
SI	0.00020	0.00020

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00062	0.00062

D	0.00048	0.00048
RDN	0.00108	0.00108
SDN	0.00085	0.00085
SE	0.00093	0.00093
SI	0.00040	0.00040

Max Leakage Power (uW)

V1	V2
0.00069003	0.00075341

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.15417	0.15422
CK→Q_RISE	0.13839	0.13932
RDN→Q_FALL	0.13686	0.13680
SDN→Q_FALL	0.09900	0.09898
SDN→Q_RISE	0.09937	0.09973
CK→QN_FALL	0.11402	0.11132
CK→QN_RISE	0.12443	0.12255
RDN→QN_RISE	0.10716	0.10522
SDN→QN_FALL	0.07550	0.07239
SDN→QN_RISE	0.06926	0.06729

Timing Constraints (ns)

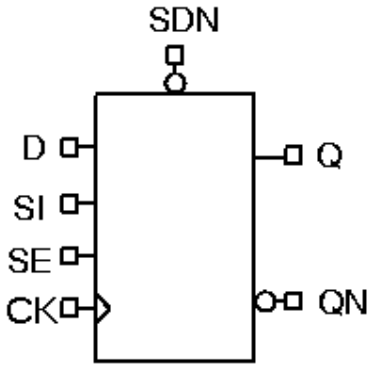
Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.00859	-0.00287
D	hold_RISE→CK	-0.08589	-0.08302
D	setup_FALL→CK	0.08016	0.08302
D	setup_RISE→CK	0.11737	0.12310
RDN	setup_RISE→CK	0.14025	0.14313
RDN	hold_RISE→CK	-0.12023	-0.12023
SDN	setup_RISE→CK	-0.06583	-0.06296
SDN	hold_RISE→CK	0.08587	0.08587
SDN	non_seq_hold_RISE→RDN	-0.04578	-0.04578
SDN	non_seq_setup_RISE→RDN	0.05723	0.06297
SE	hold_FALL→CK	-0.01143	-0.00574
SE	hold_RISE→CK	-0.08872	-0.08872
SE	setup_FALL→CK	0.09731	0.10018
SE	setup_RISE→CK	0.12880	0.13453
SI	hold_FALL→CK	-0.02290	-0.01717
SI	hold_RISE→CK	-0.10593	-0.10307
SI	setup_FALL→CK	0.09734	0.10020
SI	setup_RISE→CK	0.14314	0.14886

CK	minpwh	0.11981	0.12335
CK	minpwl	0.19102	0.19537
RDN	minpwl	0.09170	0.09874
SDN	minpwl	0.11279	0.11976

SDSNHS

Cell Description

Scan D Flip-Flop with Async Set
Q = !SDN ? 1 : rising (CK) ? (SE&SI | !SE&D) : pre_Q
QN = !Q



Function Table

SDN	CK<1>	CK	SE	SI	D	Q
0	X	X	X	X	X	1
1	0	0	X	X	X	Q<1>
1	0	1	0	X	0	0
1	0	1	0	X	1	1
1	0	1	1	0	X	0
1	0	1	1	1	X	1
1	1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
SDSNHSV1	1.26	4.76
SDSNHSV2	1.26	4.76

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00169	0.00170
D	0.00026	0.00026
Q	0.00117	0.00125
QN	0.00116	0.00123
SDN	0.00013	0.00013
SE	0.00058	0.00058
SI	0.00030	0.00030

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00045	0.00045
D	0.00047	0.00047
SDN	0.00090	0.00090
SE	0.00091	0.00091

SI	0.00038	0.00038

Max Leakage Power (uW)

V1	V2
0.00066984	0.00069407

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.13100	0.13193
CK→Q_RISE	0.12447	0.12662
SDN→Q_RISE	0.09562	0.09710
CK→QN_FALL	0.10132	0.09942
CK→QN_RISE	0.10455	0.10422
SDN→QN_FALL	0.07318	0.07087

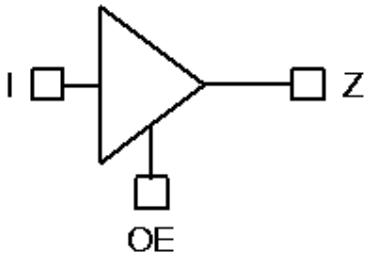
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.00857	-0.00574
D	hold_RISE→CK	-0.04007	-0.04007
D	setup_FALL→CK	0.05152	0.05437
D	setup_RISE→CK	0.06011	0.06297
SDN	setup_RISE→CK	-0.04867	-0.04581
SDN	hold_RISE→CK	0.05726	0.05725
SE	hold_FALL→CK	-0.01430	-0.00857
SE	hold_RISE→CK	-0.05153	-0.05153
SE	setup_FALL→CK	0.06869	0.06869
SE	setup_RISE→CK	0.07443	0.07729
SI	hold_FALL→CK	-0.04008	-0.03435
SI	hold_RISE→CK	-0.05725	-0.05725
SI	setup_FALL→CK	0.09161	0.09448
SI	setup_RISE→CK	0.08016	0.08302
CK	minpwh	0.10926	0.11629
CK	minpwl	0.14269	0.14708
SDN	minpwl	0.09873	0.10928

TBUFHS

Cell Description

3-State Buffer with High Enable
Z=!OE ? I:(1'bZ)



Function Table

OE	I	Z
0	X	Z
1	0	0
1	1	1

Cell Size

CellName	Height(um)	Width(um)
TBUFHSV1	1.26	1.26
TBUFHSV2	1.26	1.54
TBUFHSV3	1.26	1.54
TBUFHSV6	1.26	1.82
TBUFHSV8	1.26	2.10
TBUFHSV12	1.26	2.52
TBUFHSV16	1.26	2.94
TBUFHSV20	1.26	3.50
TBUFHSV24	1.26	4.06

Pin Power (uW/MHz)

Pin	V1	V2	V3	V6	V8	V12	V16	V20
I	0.00087	0.00108	0.00119	0.00184	0.00225	0.00304	0.00368	0.00455
OE	0.00059	0.00077	0.00087	0.00145	0.00182	0.00253	0.00312	0.00390

Pin	V24
I	0.00543
OE	0.00469

Pin Capacitance (pf)

Pin	V1	V2	V3	V6	V8	V12	V16	V20
I	0.00047	0.00044	0.00044	0.00045	0.00044	0.00047	0.00044	0.00046
OE	0.00086	0.00085	0.00085	0.00086	0.00085	0.00087	0.00086	0.00087

Pin	V24
I	0.00045
OE	0.00087

Max Leakage Power (uW)

V1	V2	V3	V6	V8	V12	V16	V20
0.00022816	0.00031271	0.00040206	0.00071552	0.00093530	0.00142210	0.00187713	0.00237431

V24
0.00295311

Delay Table (ns)

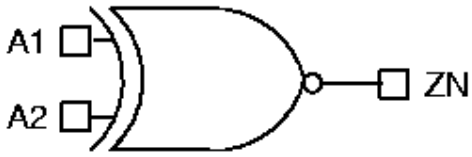
Description	V1	V2	V3	V6	V8	V12	V16	V20
I→Z_FALL	0.06581	0.06656	0.06816	0.08607	0.09596	0.12111	0.13910	0.16264
I→Z_RISE	0.05233	0.05106	0.05164	0.06363	0.07052	0.08786	0.09996	0.11639
OE→Z_FALL	0.03772	0.03736	0.03766	0.04443	0.04814	0.05751	0.06442	0.07337
OE→Z_RISE	0.03550	0.03495	0.03520	0.04083	0.04397	0.05175	0.05698	0.06387

Description	V24
I→Z_FALL	0.18791
I→Z_RISE	0.13348
OE→Z_FALL	0.08311
OE→Z_RISE	0.07141

XNOR2HS

Cell Description

2-Input Exclusive NOR
ZN=(!(A1^A2))



Function Table

A2	A1	ZN
0	0	1
0	1	0
1	0	0
1	1	1

Cell Size

CellName	Height(um)	Width(um)
XNOR2HSV1	1.26	1.96
XNOR2HSV2	1.26	1.96

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00109	0.00116
A2	0.00184	0.00192

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00097	0.00098
A2	0.00061	0.00061

Max Leakage Power (uW)

V1	V2
0.00037053	0.00038906

Delay Table (ns)

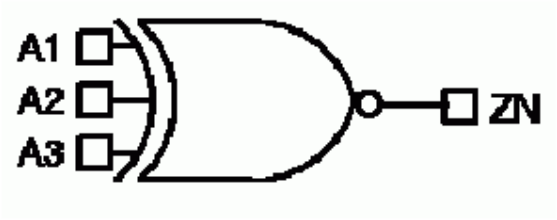
Description	V1	V2
A1→ZN_FALL	0.04563	0.04652

A1→ZN_RISE	0.04387	0.04350
A2→ZN_FALL	0.07359	0.07490
A2→ZN_RISE	0.06571	0.06566

XNOR3HS

Cell Description

3-Input Exclusive NOR
ZN=(!(A1^A2^A3))



Function Table

A2	A1	A3	ZN
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
XNOR3HSV1	1.26	3.08
XNOR3HSV2	1.26	3.08

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00295	0.00299
A2	0.00213	0.00217
A3	0.00102	0.00105

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00062	0.00062
A2	0.00098	0.00098
A3	0.00096	0.00096

Max Leakage Power (uW)

V1	V2

0.00082385	0.00084513

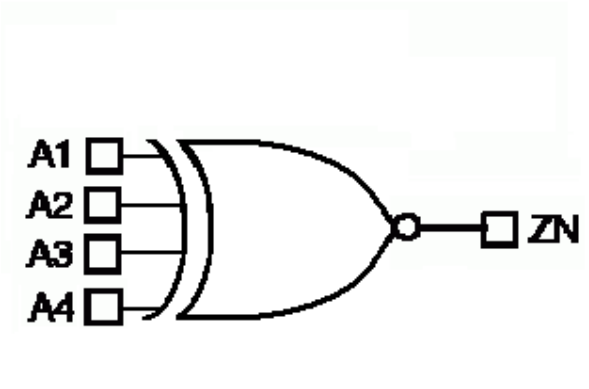
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.11887	0.12072
A1→ZN_RISE	0.11134	0.11027
A2→ZN_FALL	0.09367	0.09543
A2→ZN_RISE	0.08502	0.08391
A3→ZN_FALL	0.04600	0.04753
A3→ZN_RISE	0.03974	0.03878

XNOR4HS

Cell Description

4-Input Exclusive NOR
ZN=(!(A1^A2^A3^A4))



Function Table

A2	A1	A3	A4	ZN
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
XNOR4HSV1	1.26	5.46
XNOR4HSV2	1.26	5.46

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00316	0.00323
A2	0.00387	0.00393
A3	0.00271	0.00269
A4	0.00338	0.00334

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00097	0.00098
A2	0.00062	0.00062
A3	0.00101	0.00102
A4	0.00063	0.00062

Max Leakage Power (uW)

V1	V2
0.00107027	0.00112164

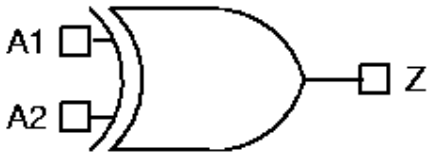
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.12370	0.12141
A1→ZN_RISE	0.11736	0.11613
A2→ZN_FALL	0.14916	0.14660
A2→ZN_RISE	0.14283	0.14132
A3→ZN_FALL	0.10305	0.10106
A3→ZN_RISE	0.10294	0.09971
A4→ZN_FALL	0.12793	0.12564
A4→ZN_RISE	0.12787	0.12433

XOR2HS

Cell Description

2-Input Exclusive OR
Z=(A1^A2)



Function Table

A2	A1	Z
0	0	0
0	1	1
1	0	1
1	1	0

Cell Size

CellName	Height(um)	Width(um)
XOR2HSV1	1.26	1.96
XOR2HSV2	1.26	1.96

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00108	0.00116
A2	0.00182	0.00189

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00097	0.00096
A2	0.00062	0.00061

Max Leakage Power (uW)

V1	V2
0.00038200	0.00039881

Delay Table (ns)

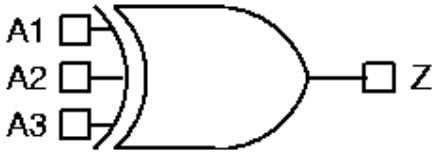
Description	V1	V2
A1→Z_FALL	0.04569	0.04682

A1→Z_RISE	0.04363	0.04348
A2→Z_FALL	0.07279	0.07382
A2→Z_RISE	0.06538	0.06520

XOR3HS

Cell Description

3-Input Exclusive OR
Z=(A1^A2^A3)



Function Table

A2	A1	A3	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
XOR3HSV1	1.26	3.08
XOR3HSV2	1.26	3.08

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00301	0.00305
A2	0.00218	0.00222
A3	0.00100	0.00103

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00062	0.00062
A2	0.00098	0.00098
A3	0.00094	0.00094

Max Leakage Power (uW)

V1	V2

0.00076373	0.00080602

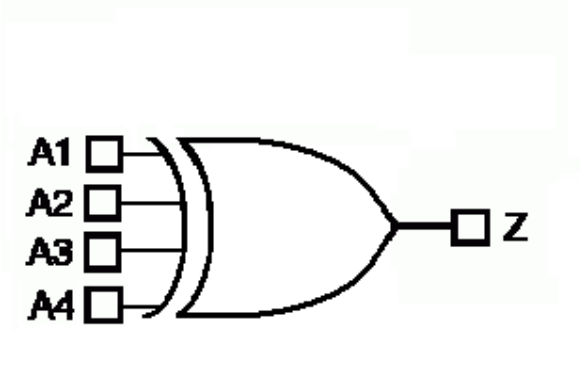
Delay Table (ns)

Description	V1	V2
A1→Z_FALL	0.12329	0.12503
A1→Z_RISE	0.11278	0.11134
A2→Z_FALL	0.09801	0.09976
A2→Z_RISE	0.08657	0.08512
A3→Z_FALL	0.04254	0.04426
A3→Z_RISE	0.03947	0.03803

XOR4HS

Cell Description

4-Input Exclusive OR
Z=(A1^A2^A3^A4)



Function Table

A2	A1	A3	A4	Z
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
XOR4HSV1	1.26	5.32
XOR4HSV2	1.26	5.32

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00326	0.00335
A2	0.00396	0.00405
A3	0.00281	0.00288
A4	0.00347	0.00354

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00098	0.00099
A2	0.00063	0.00062
A3	0.00098	0.00097
A4	0.00062	0.00062

Max Leakage Power (uW)

V1	V2
0.00117188	0.00120595

Delay Table (ns)

Description	V1	V2
A1→Z_FALL	0.12676	0.12799
A1→Z_RISE	0.12014	0.11951
A2→Z_FALL	0.15205	0.15317
A2→Z_RISE	0.14546	0.14472
A3→Z_FALL	0.10516	0.10568
A3→Z_RISE	0.10540	0.10414
A4→Z_FALL	0.13078	0.13108
A4→Z_RISE	0.13111	0.12962