

SMIC 65nm Low Leakage HS RVT
Logic Process
Standard Cell Library Databook
V2.0



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Revision History

This document contains the release history for SMIC 65nm Low Leakage HS RVT Process Standard Cell Library Databook.

| IP Code | Release Version | Date of Release | Update Description |
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| SCC65NLL_HS_RVT | 2.0 | Sep 2011 | Update Release |

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Introduction

SMIC's standard cell library is custom-designed and tested to provide the optimum combination of high-performance and high-density cells. Cell optimization is derived from extensive internal and external custom designs and place-and-route analysis; whereas, library optimization is characterized by thorough simulation of library functions and of various drive strengths using leading simulation and place-and-route tools to produce superior GDSII results.

Organization of the databook

The introduction is organized into several sections:

1. Global Parameters provides library overview and some general specifications.
2. Timing Constraint describes what type of timing specification is measured from each cell.
3. Special Cells defines the various types of special cells in the library.
4. Standard Cell Library Interpretation explains the components in each of the datasheets.

Global Parameters

This section defines the general specifications for the SMIC 65nm low leakage HS RVT Process Standard Cell Library. It includes physical cell specifications, electrical specifications, propagation delay specifications, timing specifications, and power calculation.

Physical Cell Specifications

Table 1. shows the physical design cell specification for this standard cell library.

Table 1. Physical Cell Specification

| | |
|---------------------------------------|----------------|
| Drawn Gate Length (um) | 0.06 |
| Number of Layers of Metal | 6,7,8,9, or 10 |
| Layout Grid (um) | 0.005 |
| Vertical Pin Grid (um) | 0.1+0.2n |
| Horizontal Pin Grid (um) | 0.1+0.2n |
| Cell power and Ground Rail Width (um) | 0.28 |
| Cell Height (um) | 1.8 |
| N-well and substrate distance | 10.0 |

Where n is positive integer value. All pins are located with a 0.1um offset to vertical and horizontal pin grids, making place-and-route tools much more efficient.

Note

The library supports designs with six, seven, eight, nine, or ten layers of metal. For different layers of top-level metal, it is possible that a change in the design rules description within the technology file is required, because the top metal has greater minimum width, minimum spacing, and minimum area requirements. Please refer to “65nm Logic 1P10M Salicide 1.2/1.8/2.5/3.3V Low Leakage and 1.0/1.8/2.5V Generic Design Rules” for more information. It is crucial to define these rules correctly within the technology file for the place-and-route tool to function properly.

Table 2. lists the electrical specifications for this standard cell library.

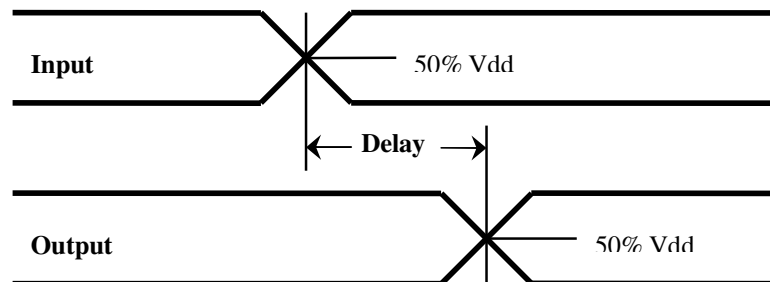
Table 2. Electrical Specifications

| Corners | Best | Best: High Temp | Best: Zero Temp | Typical | Worst: Low Temp | Worst |
|-----------------------------|-------------|----------------------------|----------------------------|----------------|----------------------------|--------------|
| Supply Voltage (V) | 1.32 | 1.32 | 1.32 | 1.20 | 1.08 | 1.08 |
| Junction Temperature (°C) | -40 | 125 | 0 | 25 | -40 | 125 |

Propagation Delay and Transition Time

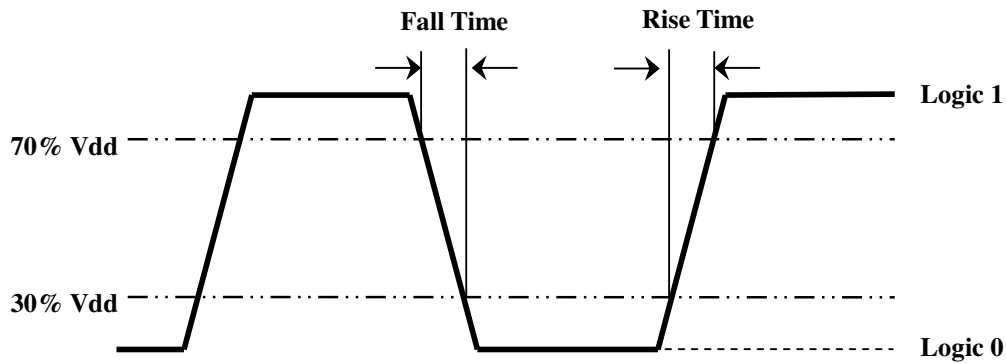
Propagation delay is the sum of the intrinsic delay, the load delay, and the input-slew delay of a cell. Delays are defined as the time interval between the input stimulus and output crossing 50% of the Vdd value. The propagation delay is illustrated in Figure 1. below.

Figure 1. Propagation Delay



Transition time or slew rate is defined as the time interval between crossings of 30% to 70% of Vdd value on a signal. Transition time is shown in Figure 2. for both rising and falling signals.

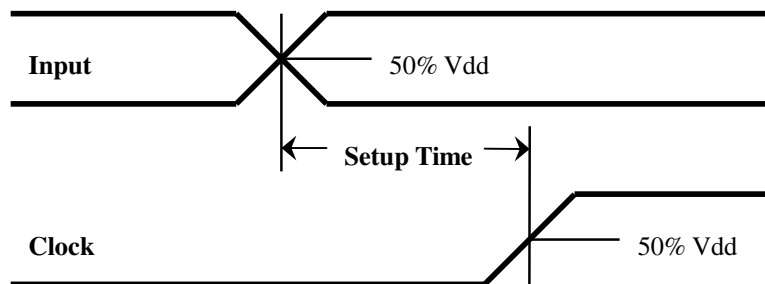
Figure 2. Transition Time



Setup Time

Setup time for a sequential cell is the minimum period of time the data signal must remain stable before the active edge of the clock (or another specified signal) to ensure correct function at the output. Setup constraint values are measured as the interval between the data signal crossing 50% of V_{dd} for rising or falling data and the clock signal crossing 50% of V_{dd} for rising or falling clocks. For measurement of setup time, the data signal is kept stable indefinitely after the clock edge. Definition of setup time for a positive-edge triggered sequential cell is shown in Figure 3.

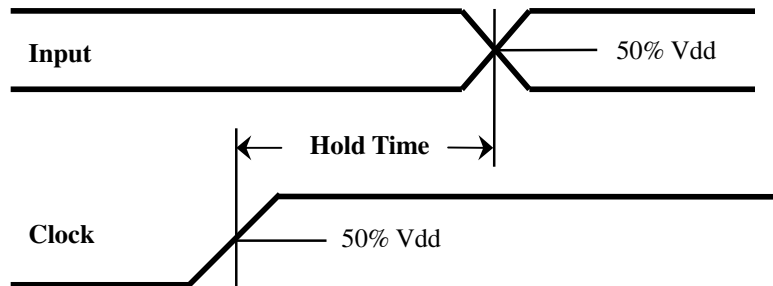
Figure 3. Setup Time



Hold Time

Hold time for a sequential cell is the minimum period of time the data signal must remain stable after the active edge of the clock (or another specified signal) to ensure correct function at the output. Hold constraint values are measured as the interval between the data signal crossing 50% of V_{dd} value and the clock signal crossing 50% of V_{dd} for either rise or fall transitions on both signals. For measurement of hold time, the data signal is kept stable indefinitely before the clock edge. Definition of fall time for a positive-edge triggered sequential cell is shown in Figure 4.

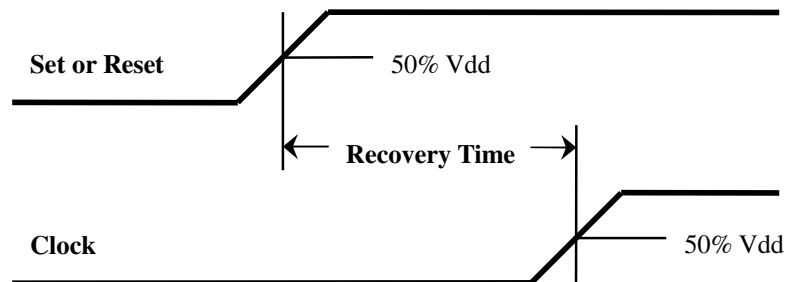
Figure 4. Hold Time



Recovery Time

Recovery time for sequential cell is the minimum length of time that the active-low set or reset signal must remain high before the active edge of the clock to ensure correct cell function. Recovery constraint value is measured as the interval between the set or reset signal crossing 50% of V_{dd} and the clock signal crossing 50% of V_{dd} for rising or falling clocks. For measurement of recovery time, the set or reset signal is held stable indefinitely after the clock edge. Definition of recovery time is shown below in Figure 5.

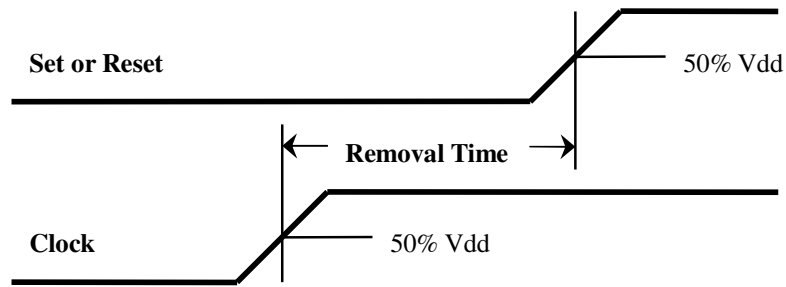
Figure 5. Recovery Time



Removal Time

Removal time for sequential cell is the minimum length of time that the set or reset signals must remain low after the active edge of the clock to ensure correct cell function. Removal constraint value is measured as the interval between the set or reset signal crossing 50% of V_{dd} and the clock signal crossing 50% of V_{dd} for rising or falling clocks. For measurement of removal time, the set or reset signal is held stable indefinitely before the clock edge. Definition of removal time is shown in Figure 6.

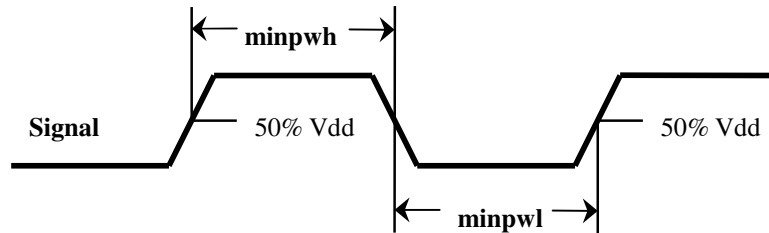
Figure 6. Removal Time



Minimum Pulse Width

Minimum pulse width is the minimum period of time between the leading and trailing edges of a pulse waveform. Minimum pulse width high (minpwh) is measured as the interval between the rising edge of signal crossing 50% of V_{DD} and the falling edge of signal crossing 50% of V_{DD}. Minimum pulse width low (minpwl) is measured as the interval between the falling edge of signal crossing 50% of V_{DD} and the rising edge of signal crossing 50% of V_{DD}. Minimum pulse width is illustrated in Figure 7.

Figure 7. Minimum Pulse Width



Special Cells

This section discusses the special cell types within the SMIC Standard Cell Library.

De-CAP Cells

The standard cell library includes 5 De-CAP cells: FDCAPHS4, FDCAPHS8, FDCAPHS16, FDCAPHS32 and FDCAPHS64. De-CAP is composed of a PMOS and NMOS device to form decoupling capacitors between V_{DD} and V_{SS} rails so as to reduce the voltage bounce on the power rails. The De-CAP functional schematic is shown in Figure 8. below.

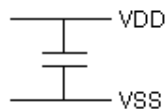


Figure 8. De-CAP Functional Schematic

FILL Cells

The standard cell library includes 5 FILL cells, namely: F_FILLHS1, F_FILLHS2, F_FILLHS4, F_FILLHS8 and F_FILLHS16. The number denoted at the end of the cell names represents the width of the cell measured in number of tracks.

The FILL cells are used to connect power and ground rails across an area with no cells during place and route. It is used to ensure that gaps do not occur between well or implant layers which in some cases can cause DRC violations.

PULL0/1 Cells

The two PULLHS0 and PULLHS1 cells provide ESD protection of signal inputs from power and ground rails. These cells provide diffusion-driven inputs for signal pins. If these cells are not used and Via(s) are dropped on the power rails, DRC error or shorts may occur. Any input pin that will be preset to 0/1 need connect PULLHS0 / PULLHS1 cell rather than VSS/VDD.

NWELL and Substrate Tie Cells

The standard cell library contains one NWELL/Substrate Tie Cell: FILLTIEHS. This standard cell library does not have well or substrate ties inside the cells. It is required to tie NWell to VDD and substrate to VSS before place-and-route using the FILLTIEHS cells. It is also required to place the Tie cells as frequent as the design requires. Figures 9 and 10 illustrate the two FILLTIEHS cell orientations within the library.

| | | | | | | |
|--|---|--|---|--|---|--|
| | F | | F | | F | |
| | | | | | | |
| | F | | F | | F | |

Figure 9. Normal placement of FILLTIE cells

| | | | | | | |
|--|---|--|---|--|---|--|
| | F | | | | F | |
| | | | T | | | |
| | F | | | | F | |

Figure 10. Flipped placement of FILLTIE cells

Figure 9 shows that normal placement of FILLTIEHS cells requires tie cells be placed every 20um. The accurate data please refer to "65nm Logic 1P7M 1.8V/2.5V ESD and Latch-up Guideline". All rows except for the top and bottom two have their VDD and VSS shared between the adjacent rows, allowing for wider placement of FILLTIEHS cells when the cells of alternating rows are placed with an offset, as illustrated above in Figure 10. An example of this would be that the design rule specifies FILLTIEHS cells every 20um apart; however, with offset for alternating rows, FILLTIEHS cells can be placed every 40um apart with the exception of the top and bottom rows.

Antenna Cells

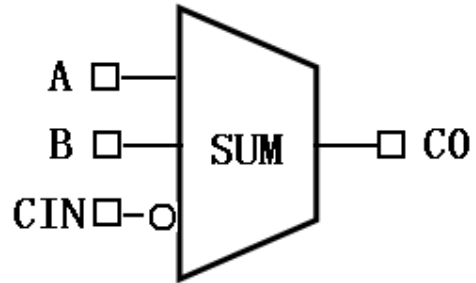
The standard cell library contains 3 F_DIODE cells: F_DIODEHS2, F_DIODEHS4 and F_DIODEHS8. The SMIC antenna effect prevention guideline within the "65nm LOGIC Antenna Ratio Effect Generic Prevention Design Guide Rule" specifies the maximum length of wire allowed within the library. During place-and-route, the router may connect wires to the input gates of cells that are longer than the maximum length allowed. In this case, antenna cells can be placed on these inputs. Pin A on the antenna cell connects to two diodes, one reversed-biased from Pin A to ground and another from VDD to Pin A. The Antenna cells will need to be placed manually; fortunately, most place-and-route tools will indicate which nets will require the insertion of these cells.

AC1CINHS

Cell Description

The AC1CIN cell is a full adder carry-generator that provides the arithmetic carryout (CO) of two operands (A,B) with active low carry-in (CIN).

$$CO = ((A \& B) | (A \& (!CIN)) | (B \& (!CIN)))$$



Function Table

| A | CIN | B | CO |
|---|-----|---|----|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | X | 0 |
| 1 | 0 | X | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| AC1CINHSV1 | 1.80 | 2.80 |
| AC1CINHSV2 | 1.80 | 2.80 |
| AC1CINHSV4 | 1.80 | 3.20 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00205 | 0.00227 | 0.00360 |
| B | 0.00212 | 0.00235 | 0.00373 |
| CIN | 0.00225 | 0.00249 | 0.00385 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00169 | 0.00176 | 0.00221 |
| B | 0.00149 | 0.00159 | 0.00212 |
| CIN | 0.00150 | 0.00164 | 0.00177 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|----|----|----|
|----|----|----|

| | | |
|------------|------------|------------|
| 0.00030013 | 0.00034547 | 0.00057732 |
|------------|------------|------------|

Delay Table (ns)

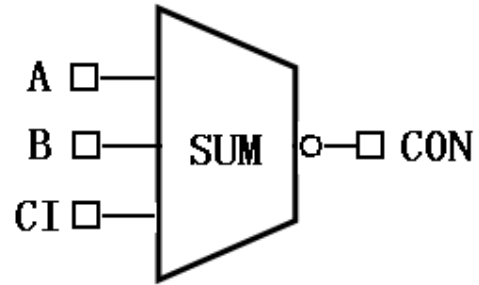
| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| A→CO_FALL | 0.10241 | 0.09873 | 0.09395 |
| A→CO_RISE | 0.07563 | 0.07434 | 0.07120 |
| B→CO_FALL | 0.10461 | 0.10121 | 0.09693 |
| B→CO_RISE | 0.07618 | 0.07518 | 0.07265 |
| CIN→CO_FALL | 0.07396 | 0.06993 | 0.06555 |
| CIN→CO_RISE | 0.06937 | 0.06799 | 0.06988 |

AC1CONHS

Cell Description

The AC1CON cell is a full adder carry-generator that provides the arithmetic activelow carry-out (CON) of two operands (A,B) with carryin (CI).

$$CON = \neg((A \& B) \mid (A \& CI) \mid (B \& CI))$$



Function Table

| B | A | CI | CON |
|---|---|----|-----|
| 0 | 0 | X | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| AC1CONHSV1 | 1.80 | 3.40 |
| AC1CONHSV2 | 1.80 | 3.40 |
| AC1CONHSV4 | 1.80 | 3.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00270 | 0.00297 | 0.00465 |
| B | 0.00277 | 0.00305 | 0.00478 |
| CI | 0.00229 | 0.00252 | 0.00389 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00167 | 0.00176 | 0.00229 |
| B | 0.00149 | 0.00158 | 0.00217 |
| CI | 0.00141 | 0.00153 | 0.00174 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00040834 | 0.00047184 | 0.00084706 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| A→CON_FALL | 0.10255 | 0.09737 | 0.08759 |
| A→CON_RISE | 0.10743 | 0.10215 | 0.08880 |
| B→CON_FALL | 0.10360 | 0.09840 | 0.08955 |
| B→CON_RISE | 0.10953 | 0.10439 | 0.09166 |
| CI→CON_FALL | 0.07112 | 0.06641 | 0.06098 |
| CI→CON_RISE | 0.06970 | 0.06545 | 0.06315 |

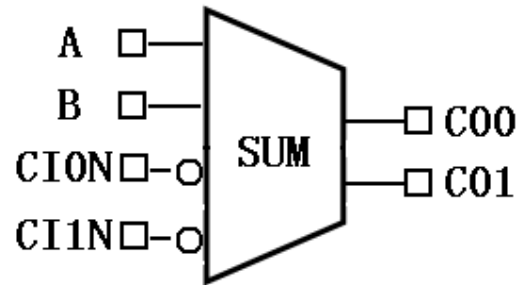
AC2CINHS

Cell Description

The AC2CIN cell provides a carry-select adder carry generation function with active-low carry inputs. The function produces the carryouts (CO0,CO1) of the operands (A,B) with active-low carry-ins (CI0N,CI1N).

$$CO0=((A\&B)|(A\&(!CI0N))|(B\&(!CI0N)))$$

$$CO1=((A\&B)|(A\&(!CI1N))|(B\&(!CI1N)))$$



Function Table

| CI0N | A | B | CO0 |
|------|---|---|-----|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | X | 1 |
| 1 | 0 | X | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |
| CI1N | A | B | CO1 |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | X | 1 |
| 1 | 0 | X | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| AC2CINHSV1 | 1.80 | 4.40 |
| AC2CINHSV2 | 1.80 | 4.40 |
| AC2CINHSV4 | 1.80 | 6.00 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|------|---------|---------|---------|
| A | 0.00245 | 0.00281 | 0.00464 |
| B | 0.00254 | 0.00294 | 0.00494 |
| CI0N | 0.00229 | 0.00254 | 0.00397 |
| CI1N | 0.00228 | 0.00254 | 0.00401 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|------|---------|---------|---------|
| A | 0.00171 | 0.00223 | 0.00430 |
| B | 0.00159 | 0.00216 | 0.00445 |
| CI0N | 0.00144 | 0.00157 | 0.00184 |
| CI1N | 0.00150 | 0.00164 | 0.00182 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00052408 | 0.00066075 | 0.00125210 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|---------------|---------|---------|---------|
| A→CO0_FALL | 0.11845 | 0.09660 | 0.08067 |
| A→CO0_RISE | 0.08388 | 0.06984 | 0.05910 |
| B→CO0_FALL | 0.12112 | 0.09958 | 0.08423 |
| B→CO0_RISE | 0.08131 | 0.07132 | 0.06121 |
| CI0N→CO0_FALL | 0.06872 | 0.05895 | 0.05510 |
| CI0N→CO0_RISE | 0.06791 | 0.06328 | 0.06155 |
| A→CO1_FALL | 0.12005 | 0.09805 | 0.08115 |
| A→CO1_RISE | 0.08480 | 0.07092 | 0.05973 |
| B→CO1_FALL | 0.12272 | 0.10102 | 0.08470 |
| B→CO1_RISE | 0.08235 | 0.07238 | 0.06186 |
| CI1N→CO1_FALL | 0.06893 | 0.05951 | 0.05588 |
| CI1N→CO1_RISE | 0.06741 | 0.06319 | 0.06227 |

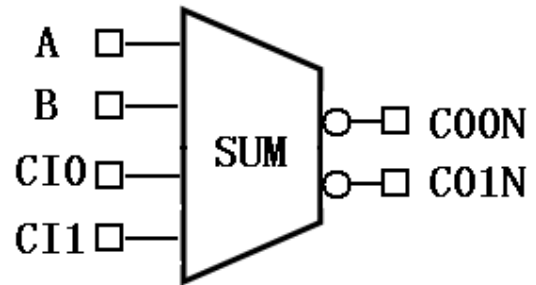
AC2CONHS

Cell Description

The AC2CON cell provides a carry-select addercarry generation function that produces active-low carryouts (CO0N,CO1N) of the operands (A,B) with carry-ins (CI0,CI1).

$CO0N = \neg((A \& B) | (A \& CI0) | (B \& CI0))$

$CO1N = \neg((A \& B) | (A \& CI1) | (B \& CI1))$



Function Table

| CI0 | A | B | CO0N |
|-----|---|---|------|
| 0 | 0 | X | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | X | 0 |
| CI1 | A | B | CO1N |
| 0 | 0 | X | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| AC2CONHSV1 | 1.80 | 5.00 |
| AC2CONHSV2 | 1.80 | 5.00 |
| AC2CONHSV4 | 1.80 | 6.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00318 | 0.00361 | 0.00586 |
| B | 0.00325 | 0.00373 | 0.00616 |
| CI0 | 0.00221 | 0.00246 | 0.00400 |
| CI1 | 0.00223 | 0.00247 | 0.00419 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00174 | 0.00232 | 0.00436 |
| B | 0.00155 | 0.00215 | 0.00448 |
| CI0 | 0.00148 | 0.00160 | 0.00166 |
| CI1 | 0.00152 | 0.00163 | 0.00174 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00061872 | 0.00077039 | 0.00149450 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|---------------|---------|---------|---------|
| A→CO0N_FALL | 0.11964 | 0.10808 | 0.09269 |
| A→CO0N_RISE | 0.11978 | 0.10573 | 0.08892 |
| B→CO0N_FALL | 0.11905 | 0.11039 | 0.09545 |
| B→CO0N_RISE | 0.12210 | 0.10866 | 0.08923 |
| CI0→CO0N_FALL | 0.06883 | 0.06478 | 0.06307 |
| CI0→CO0N_RISE | 0.06559 | 0.06191 | 0.06282 |
| A→CO1N_FALL | 0.11631 | 0.10713 | 0.09257 |
| A→CO1N_RISE | 0.11909 | 0.10514 | 0.08901 |
| B→CO1N_FALL | 0.11790 | 0.10946 | 0.09534 |
| B→CO1N_RISE | 0.12141 | 0.10808 | 0.08903 |
| CI1→CO1N_FALL | 0.06801 | 0.06404 | 0.06459 |
| CI1→CO1N_RISE | 0.06582 | 0.06209 | 0.06595 |

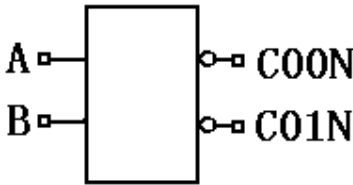
ACH2CONHS

Cell Description

The ACH2CON cell provides a carry-select addercarry generation function for the first stage of a carry-select adder block (i.e., there are no carry-inputs). The function produces active-low carryouts (CO0N,CO1N) of the operands (A,B).

$$CO0N=!(A\&B))$$

$$CO1N=!(A\mid B))$$



Function Table

| A | B | CO0N |
|---|---|------|
| 0 | X | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |
| A | B | CO1N |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| ACH2CONHSV1 | 1.80 | 1.20 |
| ACH2CONHSV2 | 1.80 | 1.20 |
| ACH2CONHSV4 | 1.80 | 2.60 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00058 | 0.00063 | 0.00120 |
| B | 0.00074 | 0.00082 | 0.00162 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00220 | 0.00237 | 0.00435 |
| B | 0.00220 | 0.00240 | 0.00457 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00016843 | 0.00021553 | 0.00047332 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| A→CO0N_FALL | 0.01459 | 0.01475 | 0.01378 |
| A→CO0N_RISE | 0.01600 | 0.01548 | 0.01317 |
| B→CO0N_FALL | 0.01661 | 0.01673 | 0.01669 |
| B→CO0N_RISE | 0.01893 | 0.01823 | 0.01624 |
| A→CO1N_FALL | 0.01290 | 0.01198 | 0.00983 |
| A→CO1N_RISE | 0.02243 | 0.02109 | 0.01926 |
| B→CO1N_FALL | 0.01404 | 0.01327 | 0.01101 |
| B→CO1N_RISE | 0.02549 | 0.02457 | 0.02449 |

AD142HS

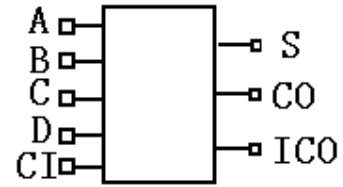
Cell Description

The AD142 cell takes in 4 bits of the partial product (A,B,C,D) and compresses them into 2-bits of partial product (S,CO). The cell requires an intermediate carry-in input (CI) from the n-1compressor and an intermediate carry-out output (CO) to the n+1compressor.

$$ICO=(A\&B)|(A\&C)|(B\&C)$$

$$CO=((A\wedge B\wedge C)\&D)|((A\wedge B\wedge C)\&CI)|(D\&CI)$$

$$S=((A\wedge B\wedge C)\wedge D\wedge CI)$$



Function Table

| B | A | C | CI | D | S | CO | ICO |
|---|---|---|----|---|---|----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| AD142HSV1 | 1.80 | 10.60 |
| AD142HSV2 | 1.80 | 10.60 |
| AD142HSV4 | 1.80 | 11.60 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00493 | 0.00550 | 0.00848 |
| B | 0.00491 | 0.00550 | 0.00846 |
| C | 0.00397 | 0.00436 | 0.00671 |
| CI | 0.00275 | 0.00305 | 0.00450 |
| D | 0.00564 | 0.00625 | 0.00957 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00165 | 0.00210 | 0.00210 |
| B | 0.00158 | 0.00210 | 0.00209 |
| C | 0.00104 | 0.00120 | 0.00155 |
| CI | 0.00096 | 0.00121 | 0.00155 |
| D | 0.00192 | 0.00224 | 0.00311 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00112620 | 0.00135010 | 0.00241930 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| A→CO_FALL | 0.30502 | 0.27646 | 0.29331 |
| A→CO_RISE | 0.29577 | 0.26851 | 0.28107 |
| B→CO_FALL | 0.30673 | 0.27868 | 0.29549 |
| B→CO_RISE | 0.29749 | 0.27075 | 0.28328 |
| C→CO_FALL | 0.26486 | 0.24297 | 0.22445 |
| C→CO_RISE | 0.26359 | 0.24253 | 0.22141 |
| CI→CO_FALL | 0.10526 | 0.08672 | 0.07974 |
| CI→CO_RISE | 0.08788 | 0.07292 | 0.06448 |
| D→CO_FALL | 0.16074 | 0.14316 | 0.13517 |
| D→CO_RISE | 0.14058 | 0.12642 | 0.11685 |

| | | | |
|------------|---------|---------|---------|
| A→ICO_FALL | 0.21139 | 0.19611 | 0.22947 |
| A→ICO_RISE | 0.17592 | 0.16174 | 0.17611 |
| B→ICO_FALL | 0.21416 | 0.19893 | 0.23213 |
| B→ICO_RISE | 0.17841 | 0.16508 | 0.17999 |
| C→ICO_FALL | 0.09565 | 0.08750 | 0.08415 |
| C→ICO_RISE | 0.07515 | 0.06954 | 0.06313 |
| A→S_FALL | 0.30301 | 0.27596 | 0.29312 |
| A→S_RISE | 0.29846 | 0.27157 | 0.28821 |
| B→S_FALL | 0.30470 | 0.27819 | 0.29531 |
| B→S_RISE | 0.30018 | 0.27381 | 0.29040 |
| C→S_FALL | 0.26650 | 0.24600 | 0.22862 |
| C→S_RISE | 0.26219 | 0.24177 | 0.22398 |
| CI→S_FALL | 0.12592 | 0.10658 | 0.09972 |
| CI→S_RISE | 0.11808 | 0.09946 | 0.09255 |
| D→S_FALL | 0.22456 | 0.20585 | 0.18940 |
| D→S_RISE | 0.22026 | 0.20166 | 0.18496 |

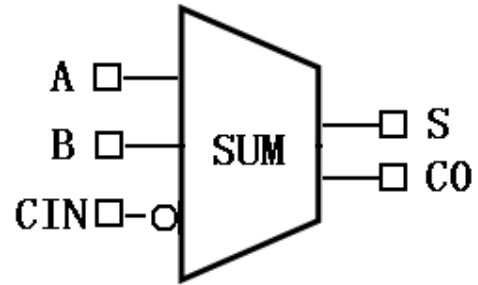
AD1CINHS

Cell Description

The AD1CIN cell is a full adder that provides the arithmetic sum(S)and carry-out (CO) of two operands (A,B) with active-low carry-in (CIN).

$$CO=((A\&B)|(A\&!CIN)|(B\&!CIN))$$

$$S=(A\wedge B\wedge (!CIN))$$



Function Table

| CIN | A | B | S | CO |
|-----|---|---|---|----|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| AD1CINHSV1 | 1.80 | 6.00 |
| AD1CINHSV2 | 1.80 | 6.00 |
| AD1CINHSV4 | 1.80 | 9.00 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| B | 0.00411 | 0.00447 | 0.00745 |
| CIN | 0.00223 | 0.00245 | 0.00406 |
| A | 0.00432 | 0.00471 | 0.00778 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00314 | 0.00339 | 0.00629 |
| B | 0.00353 | 0.00381 | 0.00718 |
| CIN | 0.00231 | 0.00252 | 0.00344 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00075445 | 0.00082878 | 0.00176860 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| A→CO_FALL | 0.10629 | 0.10020 | 0.08881 |
| A→CO_RISE | 0.08461 | 0.07839 | 0.06726 |
| B→CO_FALL | 0.11132 | 0.10517 | 0.09366 |
| B→CO_RISE | 0.08827 | 0.08185 | 0.06994 |
| CIN→CO_FALL | 0.08281 | 0.07757 | 0.07705 |
| CIN→CO_RISE | 0.07680 | 0.07188 | 0.07553 |
| A→S_FALL | 0.14458 | 0.13803 | 0.11731 |
| A→S_RISE | 0.13504 | 0.12947 | 0.10902 |
| B→S_FALL | 0.14692 | 0.14033 | 0.12001 |
| B→S_RISE | 0.13721 | 0.13161 | 0.11150 |
| CIN→S_FALL | 0.06681 | 0.06323 | 0.06296 |
| CIN→S_RISE | 0.06206 | 0.05895 | 0.06000 |

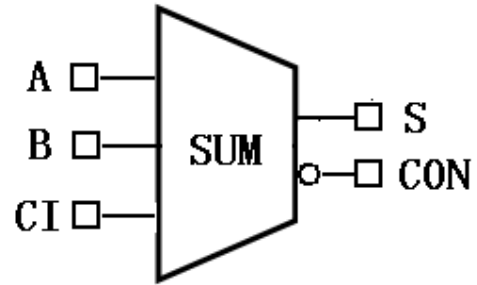
AD1CONHS

Cell Description

The AD1CON cell is a full adder that provides the arithmetic sum (S) and active-low carry-out (CON) of two operands (A,B) with carry-in (CI).

$$CON = \neg((A \& B) | (A \& CI) | (B \& CI))$$

$$S = (A \wedge B \wedge CI)$$



Function Table

| CI | A | B | S | CON |
|----|---|---|---|-----|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| AD1CONHSV1 | 1.80 | 6.80 |
| AD1CONHSV2 | 1.80 | 6.80 |
| AD1CONHSV4 | 1.80 | 9.40 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00429 | 0.00469 | 0.00760 |
| B | 0.00441 | 0.00482 | 0.00788 |
| CI | 0.00202 | 0.00226 | 0.00393 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00310 | 0.00338 | 0.00610 |
| B | 0.00356 | 0.00386 | 0.00706 |
| CI | 0.00230 | 0.00248 | 0.00316 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00083418 | 0.00092226 | 0.00189360 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| A→CON_FALL | 0.10929 | 0.10290 | 0.09123 |
| A→CON_RISE | 0.11878 | 0.11246 | 0.09379 |
| B→CON_FALL | 0.11310 | 0.10656 | 0.09504 |
| B→CON_RISE | 0.12487 | 0.11786 | 0.09861 |
| CI→CON_FALL | 0.07154 | 0.06756 | 0.06875 |
| CI→CON_RISE | 0.07635 | 0.07214 | 0.08274 |
| A→S_FALL | 0.13646 | 0.13061 | 0.11050 |
| A→S_RISE | 0.12640 | 0.12153 | 0.10257 |
| B→S_FALL | 0.13903 | 0.13304 | 0.11425 |
| B→S_RISE | 0.12880 | 0.12387 | 0.10618 |
| CI→S_FALL | 0.06229 | 0.05952 | 0.06273 |
| CI→S_RISE | 0.05793 | 0.05552 | 0.06034 |

AD2CSCINHS

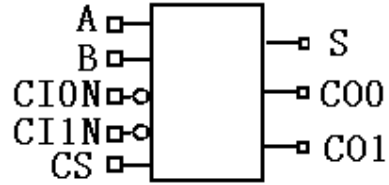
Cell Description

The AD2CSCIN cell provides a carry-select adder function that produces the arithmetic sum (S) and carryouts (CO0,CO1) of the operands (A,B) with active-low carry-ins (CI0N,CI1N).

$$CO0=((A\&B)|(A\&!CI0N)|(B\&!CI0N))$$

$$CO1=((A\&B)|(A\&!CI1N)|(B\&!CI1N))$$

$$S=((CS\&(A\wedge B\wedge (!CI1N)))(!CS\&(A\wedge B\wedge (!CI0N))))$$



Function Table

| CS | CI1N | CI0N | B | A | CO0 | CO1 | S |
|----|------|------|---|---|-----|-----|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|--------------|------------|-----------|
| AD2CSCINHSV1 | 1.80 | 11.60 |
| AD2CSCINHSV2 | 1.80 | 11.60 |
| AD2CSCINHSV4 | 1.80 | 16.20 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|------|---------|---------|---------|
| A | 0.00524 | 0.00569 | 0.00989 |
| B | 0.00532 | 0.00578 | 0.01012 |
| CI0N | 0.00297 | 0.00330 | 0.00585 |
| CI1N | 0.00288 | 0.00319 | 0.00565 |
| CS | 0.00192 | 0.00215 | 0.00384 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|------|---------|---------|---------|
| A | 0.00224 | 0.00243 | 0.00460 |
| B | 0.00225 | 0.00244 | 0.00535 |
| CI0N | 0.00459 | 0.00489 | 0.00628 |
| CI1N | 0.00375 | 0.00403 | 0.00538 |
| CS | 0.00173 | 0.00189 | 0.00252 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00133620 | 0.00144350 | 0.00293850 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|---------------|---------|---------|---------|
| A→CO0_FALL | 0.10544 | 0.10019 | 0.08489 |
| A→CO0_RISE | 0.07451 | 0.07477 | 0.06398 |
| B→CO0_FALL | 0.10856 | 0.10358 | 0.08877 |
| B→CO0_RISE | 0.07605 | 0.07286 | 0.06451 |
| CI0N→CO0_FALL | 0.05871 | 0.05694 | 0.05826 |
| CI0N→CO0_RISE | 0.06195 | 0.05863 | 0.06343 |
| A→CO1_FALL | 0.11644 | 0.11132 | 0.09662 |
| A→CO1_RISE | 0.08091 | 0.08249 | 0.07233 |
| B→CO1_FALL | 0.11948 | 0.11470 | 0.10050 |
| B→CO1_RISE | 0.08238 | 0.08403 | 0.07179 |

| | | | |
|---------------|---------|---------|---------|
| CI1N→CO1_FALL | 0.05602 | 0.05443 | 0.05765 |
| CI1N→CO1_RISE | 0.05881 | 0.05527 | 0.06328 |
| A→S_FALL | 0.24623 | 0.24104 | 0.21094 |
| A→S_RISE | 0.22592 | 0.22145 | 0.19640 |
| B→S_FALL | 0.24878 | 0.24371 | 0.21448 |
| B→S_RISE | 0.22840 | 0.22412 | 0.19987 |
| CI0N→S_FALL | 0.10433 | 0.10017 | 0.10375 |
| CI0N→S_RISE | 0.09147 | 0.08832 | 0.09627 |
| CI1N→S_FALL | 0.10625 | 0.10369 | 0.10429 |
| CI1N→S_RISE | 0.09263 | 0.08985 | 0.09524 |
| CS→S_FALL | 0.07212 | 0.06937 | 0.06726 |
| CS→S_RISE | 0.06129 | 0.05907 | 0.06200 |

AD2CSCONHS

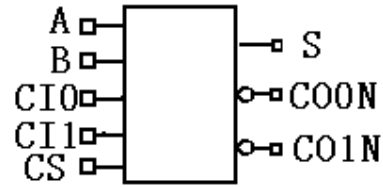
Cell Description

The AD2CSCON cell provides a carry-select adder function that produces the arithmetic sum (S) and active-low carryouts (CO0N,CO1N) of two operands (A,B) with carry-ins (CI0,CI1).

$$CO0N = \neg((A \& B) | (A \& CI0) | (B \& CI0))$$

$$CO1N = \neg((A \& B) | (A \& CI1) | (B \& CI1))$$

$$S = ((CS \& (A \wedge B \wedge CI1)) | (\neg CS \& (A \wedge B \wedge CI0)))$$



Function Table

| CS | CI1 | CI0 | B | A | CO0N | CO1N | S |
|----|-----|-----|---|---|------|------|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|--------------|------------|-----------|
| AD2CSCONHSV1 | 1.80 | 11.40 |
| AD2CSCONHSV2 | 1.80 | 11.40 |
| AD2CSCONHSV4 | 1.80 | 17.00 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00536 | 0.00584 | 0.01037 |
| B | 0.00544 | 0.00594 | 0.01059 |
| CI0 | 0.00298 | 0.00331 | 0.00574 |
| CI1 | 0.00299 | 0.00329 | 0.00572 |
| CS | 0.00192 | 0.00216 | 0.00384 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00224 | 0.00244 | 0.00465 |
| B | 0.00226 | 0.00247 | 0.00538 |
| CI0 | 0.00440 | 0.00469 | 0.00579 |
| CI1 | 0.00363 | 0.00391 | 0.00507 |
| CS | 0.00173 | 0.00189 | 0.00252 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00136080 | 0.00151950 | 0.00306190 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|---------------|---------|---------|---------|
| A→CO0N_FALL | 0.11916 | 0.11361 | 0.10398 |
| A→CO0N_RISE | 0.11614 | 0.10970 | 0.09597 |
| B→CO0N_FALL | 0.12135 | 0.11574 | 0.10689 |
| B→CO0N_RISE | 0.11975 | 0.11324 | 0.10000 |
| CI0→CO0N_FALL | 0.05982 | 0.05620 | 0.06004 |
| CI0→CO0N_RISE | 0.06643 | 0.06335 | 0.06800 |
| A→CO1N_FALL | 0.11423 | 0.10948 | 0.09931 |
| A→CO1N_RISE | 0.11290 | 0.10599 | 0.09216 |
| B→CO1N_FALL | 0.11627 | 0.11150 | 0.10221 |
| B→CO1N_RISE | 0.11641 | 0.10941 | 0.09621 |

| | | | |
|---------------|---------|---------|---------|
| CI1→COIN_FALL | 0.05504 | 0.05237 | 0.05777 |
| CI1→COIN_RISE | 0.06278 | 0.05896 | 0.06838 |
| A→S_FALL | 0.23561 | 0.22914 | 0.20435 |
| A→S_RISE | 0.21156 | 0.20691 | 0.18810 |
| B→S_FALL | 0.23847 | 0.23195 | 0.20783 |
| B→S_RISE | 0.21439 | 0.20972 | 0.19155 |
| CI0→S_FALL | 0.10596 | 0.10121 | 0.10505 |
| CI0→S_RISE | 0.09030 | 0.08719 | 0.09597 |
| CI1→S_FALL | 0.10691 | 0.10407 | 0.10389 |
| CI1→S_RISE | 0.09139 | 0.08850 | 0.09370 |
| CS→S_FALL | 0.07238 | 0.06963 | 0.06771 |
| CS→S_RISE | 0.06103 | 0.05885 | 0.06238 |

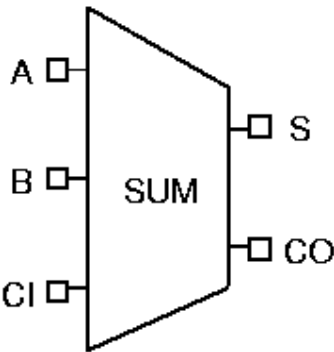
AD1HS

Cell Description

1-Bit Full Adder

$$CO=((A\&B)|(A\&CI)|(B\&CI))$$

$$S=(A\wedge B\wedge CI)$$



Function Table

| A | B | CI | CO | S |
|---|---|----|----|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| AD1HSV1 | 1.80 | 6.00 |
| AD1HSV1C | 1.80 | 4.40 |
| AD1HSV1R | 1.80 | 6.00 |
| AD1HSV1T | 1.80 | 5.80 |
| AD1HSV2 | 1.80 | 8.80 |
| AD1HSV2C | 1.80 | 4.40 |
| AD1HSV2R | 1.80 | 6.20 |
| AD1HSV2T | 1.80 | 6.60 |
| AD1HSV4 | 1.80 | 12.40 |
| AD1HSV4C | 1.80 | 6.00 |
| AD1HSV4R | 1.80 | 10.60 |
| AD1HSV4T | 1.80 | 9.80 |

Pin Power (uW/MHz)

| Pin | V1 | V1C | V1R | V1T | V2 | V2C | V2R | V2T |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A | 0.00468 | 0.00179 | 0.00330 | 0.00381 | 0.00734 | 0.00196 | 0.00374 | 0.00446 |

| | | | | | | | | |
|----|---------|---------|---------|---------|---------|---------|---------|---------|
| B | 0.00618 | 0.00178 | 0.00345 | 0.00513 | 0.00925 | 0.00196 | 0.00393 | 0.00601 |
| CI | 0.00212 | 0.00178 | 0.00212 | 0.00216 | 0.00305 | 0.00194 | 0.00233 | 0.00231 |

| Pin | V4 | V4C | V4R | V4T |
|-----|---------|---------|---------|---------|
| A | 0.01127 | 0.00318 | 0.00659 | 0.00721 |
| B | 0.01520 | 0.00319 | 0.00688 | 0.00967 |
| CI | 0.00521 | 0.00309 | 0.00401 | 0.00396 |

Pin Capacitance (pf)

| Pin | V1 | V1C | V1R | V1T | V2 | V2C | V2R | V2T |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A | 0.00157 | 0.00324 | 0.00320 | 0.00228 | 0.00241 | 0.00350 | 0.00355 | 0.00296 |
| B | 0.00127 | 0.00321 | 0.00384 | 0.00385 | 0.00157 | 0.00345 | 0.00446 | 0.00469 |
| CI | 0.00231 | 0.00262 | 0.00316 | 0.00216 | 0.00303 | 0.00279 | 0.00344 | 0.00255 |

| Pin | V4 | V4C | V4R | V4T |
|-----|---------|---------|---------|---------|
| A | 0.00307 | 0.00506 | 0.00719 | 0.00534 |
| B | 0.00307 | 0.00513 | 0.00778 | 0.00848 |
| CI | 0.00492 | 0.00382 | 0.00489 | 0.00413 |

Max Leakage Power (uW)

| V1 | V1C | V1R | V1T | V2 | V2C | V2R | V2T |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00103690 | 0.00033073 | 0.00075450 | 0.00075556 | 0.00170460 | 0.00038035 | 0.00083716 | 0.00088245 |

| V4 | V4C | V4R | V4T |
|------------|------------|------------|------------|
| 0.00300920 | 0.00072522 | 0.00165960 | 0.00168560 |

Delay Table (ns)

| Description | V1 | V1C | V1R | V1T | V2 | V2C | V2R | V2T |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A→CO_FALL | 0.15922 | 0.11051 | 0.09566 | 0.15645 | 0.15528 | 0.10813 | 0.09448 | 0.14813 |
| A→CO_RISE | 0.17359 | 0.07614 | 0.07287 | 0.15376 | 0.17383 | 0.07669 | 0.07103 | 0.14606 |
| B→CO_FALL | 0.15069 | 0.11510 | 0.10205 | 0.13564 | 0.15425 | 0.11225 | 0.09948 | 0.11593 |
| B→CO_RISE | 0.16670 | 0.08019 | 0.07841 | 0.10397 | 0.16437 | 0.08077 | 0.07505 | 0.09588 |
| CI→CO_FALL | 0.06980 | 0.10238 | 0.06596 | 0.08012 | 0.06799 | 0.09776 | 0.06217 | 0.07151 |
| CI→CO_RISE | 0.06817 | 0.07070 | 0.04267 | 0.06795 | 0.06344 | 0.06862 | 0.04007 | 0.06076 |
| A→S_FALL | 0.15477 | 0.12129 | 0.12210 | 0.14463 | 0.15551 | 0.12059 | 0.11983 | 0.14255 |
| A→S_RISE | 0.12989 | 0.11508 | 0.11460 | 0.13455 | 0.12498 | 0.11522 | 0.11329 | 0.13029 |
| B→S_FALL | 0.19143 | 0.12194 | 0.12668 | 0.14788 | 0.19107 | 0.12136 | 0.12329 | 0.14645 |
| B→S_RISE | 0.16387 | 0.11635 | 0.11918 | 0.13843 | 0.16052 | 0.11639 | 0.11671 | 0.13483 |
| CI→S_FALL | 0.06205 | 0.11710 | 0.06744 | 0.06203 | 0.06001 | 0.11497 | 0.06347 | 0.06038 |
| CI→S_RISE | 0.05673 | 0.10968 | 0.06307 | 0.05999 | 0.05537 | 0.10860 | 0.05983 | 0.05674 |

| Description | V4 | V4C | V4R | V4T |
|-------------|---------|---------|---------|---------|
| A→CO_FALL | 0.14703 | 0.09394 | 0.08499 | 0.12784 |

| | | | | |
|------------|---------|---------|---------|---------|
| A→CO_RISE | 0.17419 | 0.06664 | 0.06738 | 0.12757 |
| B→CO_FALL | 0.12771 | 0.09959 | 0.08715 | 0.11804 |
| B→CO_RISE | 0.15670 | 0.06989 | 0.06972 | 0.09192 |
| CI→CO_FALL | 0.06485 | 0.07584 | 0.05959 | 0.06183 |
| CI→CO_RISE | 0.06533 | 0.05602 | 0.03791 | 0.05503 |
| A→S_FALL | 0.15236 | 0.11703 | 0.10939 | 0.12623 |
| A→S_RISE | 0.11496 | 0.11209 | 0.09962 | 0.11322 |
| B→S_FALL | 0.17399 | 0.11765 | 0.11250 | 0.13102 |
| B→S_RISE | 0.13676 | 0.11456 | 0.10280 | 0.11865 |
| CI→S_FALL | 0.05713 | 0.10950 | 0.06622 | 0.05833 |
| CI→S_RISE | 0.05003 | 0.10181 | 0.06226 | 0.05336 |

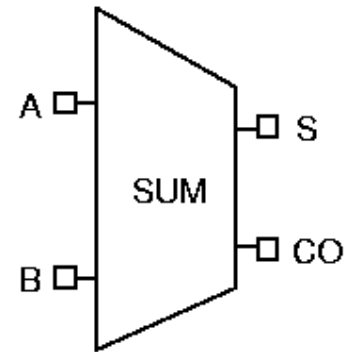
ADH1HS

Cell Description

1-Bit Half Adder

$CO=(A\&B)$

$S=(A\wedge B)$



Function Table

| B | A | S | CO |
|---|---|---|----|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| ADH1HSV1 | 1.80 | 3.40 |
| ADH1HSV1C | 1.80 | 2.40 |
| ADH1HSV2 | 1.80 | 4.20 |
| ADH1HSV2C | 1.80 | 2.40 |
| ADH1HSV4 | 1.80 | 5.20 |
| ADH1HSV4C | 1.80 | 3.40 |

Pin Power (uW/MHz)

| Pin | V1 | V1C | V2 | V2C | V4 | V4C |
|-----|---------|---------|---------|---------|---------|---------|
| A | 0.00220 | 0.00158 | 0.00292 | 0.00175 | 0.00468 | 0.00293 |
| B | 0.00143 | 0.00161 | 0.00197 | 0.00180 | 0.00296 | 0.00303 |

Pin Capacitance (pf)

| Pin | V1 | V1C | V2 | V2C | V4 | V4C |
|-----|---------|---------|---------|---------|---------|---------|
| A | 0.00307 | 0.00197 | 0.00324 | 0.00216 | 0.00541 | 0.00347 |
| B | 0.00339 | 0.00204 | 0.00463 | 0.00225 | 0.00744 | 0.00371 |

Max Leakage Power (uW)

| V1 | V1C | V2 | V2C | V4 | V4C |
|------------|------------|------------|------------|------------|------------|
| 0.00051437 | 0.00031086 | 0.00079301 | 0.00035404 | 0.00128190 | 0.00074455 |

Delay Table (ns)

| Description | V1 | V1C | V2 | V2C | V4 | V4C |
|-------------|---------|---------|---------|---------|---------|---------|
| A→CO_FALL | 0.03970 | 0.04805 | 0.04208 | 0.04429 | 0.04318 | 0.03602 |
| A→CO_RISE | 0.04372 | 0.04741 | 0.04661 | 0.04315 | 0.04641 | 0.03423 |
| B→CO_FALL | 0.03698 | 0.05185 | 0.03827 | 0.04819 | 0.03847 | 0.03985 |
| B→CO_RISE | 0.04145 | 0.04943 | 0.04287 | 0.04523 | 0.04166 | 0.03644 |
| A→S_FALL | 0.03729 | 0.07960 | 0.03665 | 0.07829 | 0.03583 | 0.07088 |
| A→S_RISE | 0.04016 | 0.06982 | 0.03996 | 0.06764 | 0.03783 | 0.06413 |
| B→S_FALL | 0.02157 | 0.08271 | 0.02166 | 0.08145 | 0.02230 | 0.07423 |
| B→S_RISE | 0.02267 | 0.07173 | 0.02288 | 0.06969 | 0.02060 | 0.06653 |

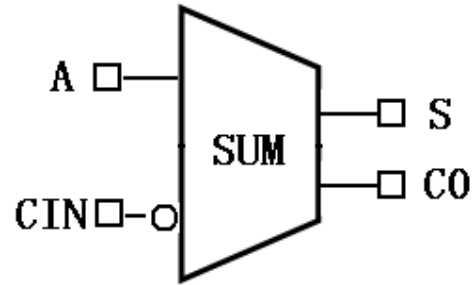
ADH1CINHS

Cell Description

The ADH1CIN cell is a half adder that provides the arithmetic sum (S) and carry-out (CO) of the input operand (A) with an active-low carry-in (CIN).

$$CO=(A\&!CIN)$$

$$S=(A\wedge !CIN)$$



Function Table

| CIN | A | CO | S |
|-----|---|----|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|--------------|------------|-----------|
| ADH1CINHSV1 | 1.80 | 3.00 |
| ADH1CINHSV1C | 1.80 | 3.00 |
| ADH1CINHSV2 | 1.80 | 3.00 |
| ADH1CINHSV2C | 1.80 | 3.00 |
| ADH1CINHSV4 | 1.80 | 4.40 |
| ADH1CINHSV4C | 1.80 | 3.40 |

Pin Power (uW/MHz)

| Pin | V1 | V1C | V2 | V2C | V4 | V4C |
|-----|---------|---------|---------|---------|---------|---------|
| CIN | 0.00176 | 0.00226 | 0.00198 | 0.00248 | 0.00330 | 0.00373 |
| A | 0.00233 | 0.00150 | 0.00267 | 0.00167 | 0.00481 | 0.00278 |

Pin Capacitance (pf)

| Pin | V1 | V1C | V2 | V2C | V4 | V4C |
|-----|---------|---------|---------|---------|---------|---------|
| A | 0.00257 | 0.00171 | 0.00285 | 0.00192 | 0.00483 | 0.00265 |
| CIN | 0.00223 | 0.00110 | 0.00233 | 0.00108 | 0.00333 | 0.00140 |

Max Leakage Power (uW)

| V1 | V1C | V2 | V2C | V4 | V4C |
|------------|------------|------------|------------|------------|------------|
| 0.00052131 | 0.00033434 | 0.00062071 | 0.00037139 | 0.00122720 | 0.00066980 |

Delay Table (ns)

| Description | V1 | V1C | V2 | V2C | V4 | V4C |
|-------------|---------|---------|---------|---------|---------|---------|
| A→CO_FALL | 0.04442 | 0.05886 | 0.04223 | 0.05530 | 0.03934 | 0.04786 |
| A→CO_RISE | 0.04552 | 0.05858 | 0.04252 | 0.05352 | 0.03810 | 0.04465 |
| CIN→CO_FALL | 0.07326 | 0.08682 | 0.07315 | 0.08539 | 0.06908 | 0.07315 |
| CIN→CO_RISE | 0.08605 | 0.09538 | 0.08603 | 0.09305 | 0.08153 | 0.07820 |
| A→S_FALL | 0.04093 | 0.08468 | 0.03874 | 0.08299 | 0.03581 | 0.07626 |
| A→S_RISE | 0.04675 | 0.07976 | 0.04430 | 0.07328 | 0.03960 | 0.07099 |
| CIN→S_FALL | 0.03110 | 0.11895 | 0.03113 | 0.11938 | 0.02965 | 0.10473 |
| CIN→S_RISE | 0.03191 | 0.11282 | 0.03161 | 0.10786 | 0.02907 | 0.09929 |

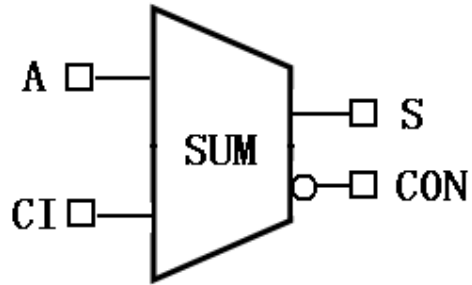
ADH1CONHS

Cell Description

The ADH1CON cell is a half adder that provides the arithmetic sum (S) and active-low carry-out (CON) of the input operand (A) with carry-in (CI).

$$\text{CON} = \neg(A \& \text{CI})$$

$$\text{S} = (A \wedge \text{CI})$$



Function Table

| CI | A | CON | S |
|----|---|-----|---|
| 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|--------------|------------|-----------|
| ADH1CONHSV1 | 1.80 | 2.40 |
| ADH1CONHSV1C | 1.80 | 2.20 |
| ADH1CONHSV2 | 1.80 | 2.40 |
| ADH1CONHSV2C | 1.80 | 2.20 |
| ADH1CONHSV4 | 1.80 | 4.40 |
| ADH1CONHSV4C | 1.80 | 2.80 |

Pin Power (uW/MHz)

| Pin | V1 | V1C | V2 | V2C | V4 | V4C |
|-----|---------|---------|---------|---------|---------|---------|
| A | 0.00197 | 0.00131 | 0.00220 | 0.00142 | 0.00411 | 0.00235 |
| CI | 0.00125 | 0.00135 | 0.00137 | 0.00147 | 0.00257 | 0.00245 |

Pin Capacitance (pf)

| Pin | V1 | V1C | V2 | V2C | V4 | V4C |
|-----|---------|---------|---------|---------|---------|---------|
| A | 0.00289 | 0.00186 | 0.00311 | 0.00205 | 0.00586 | 0.00340 |
| CI | 0.00309 | 0.00192 | 0.00324 | 0.00214 | 0.00624 | 0.00355 |

Max Leakage Power (uW)

| V1 | V1C | V2 | V2C | V4 | V4C |
|------------|------------|------------|------------|------------|------------|
| 0.00047538 | 0.00023172 | 0.00056196 | 0.00026051 | 0.00111310 | 0.00055621 |

Delay Table (ns)

| Description | V1 | V1C | V2 | V2C | V4 | V4C |
|-------------|---------|---------|---------|---------|---------|---------|
| A→CON_FALL | 0.01498 | 0.02303 | 0.01526 | 0.02033 | 0.01309 | 0.01593 |
| A→CON_RISE | 0.01630 | 0.02528 | 0.01578 | 0.02302 | 0.01292 | 0.01843 |
| CI→CON_FALL | 0.01691 | 0.02468 | 0.01715 | 0.02212 | 0.01602 | 0.01802 |
| CI→CON_RISE | 0.01930 | 0.02787 | 0.01860 | 0.02577 | 0.01606 | 0.02144 |
| A→S_FALL | 0.04176 | 0.23429 | 0.03878 | 0.20529 | 0.03599 | 0.13621 |
| A→S_RISE | 0.04588 | 0.23949 | 0.04295 | 0.21351 | 0.04025 | 0.14018 |
| CI→S_FALL | 0.02618 | 0.23717 | 0.02606 | 0.20835 | 0.02634 | 0.13937 |
| CI→S_RISE | 0.02719 | 0.23748 | 0.02688 | 0.21188 | 0.02660 | 0.14004 |

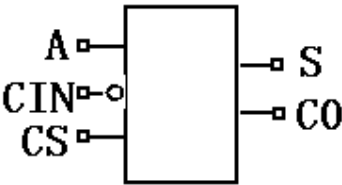
ADH1CSCINHS

Cell Description

The ADH1CSCIN cell provides a carry-select halfadder function that produces the arithmetic sum (S) and carryout (CO) of a single operand (A) with active-low carry-in (CIN).

$$CO=(A\&(!CIN))$$

$$S=(CS\&(A\^(!CIN)))+((!CS)\&A)$$



Function Table

| CS | CIN | A | CO | S |
|----|-----|---|----|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|---------------|------------|-----------|
| ADH1CSCINHSV1 | 1.80 | 3.80 |
| ADH1CSCINHSV2 | 1.80 | 3.80 |
| ADH1CSCINHSV4 | 1.80 | 4.20 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00282 | 0.00308 | 0.00394 |
| CIN | 0.00222 | 0.00245 | 0.00311 |
| CS | 0.00233 | 0.00256 | 0.00364 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00130 | 0.00147 | 0.00145 |
| CIN | 0.00315 | 0.00344 | 0.00350 |
| CS | 0.00200 | 0.00216 | 0.00220 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00066763 | 0.00077307 | 0.00096440 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| A→CO_FALL | 0.04911 | 0.04630 | 0.04740 |
| A→CO_RISE | 0.06388 | 0.06132 | 0.06389 |
| CIN→CO_FALL | 0.01252 | 0.01232 | 0.01220 |
| CIN→CO_RISE | 0.02580 | 0.02560 | 0.02478 |
| A→S_FALL | 0.11055 | 0.10593 | 0.11968 |
| A→S_RISE | 0.08960 | 0.08615 | 0.09563 |
| CIN→S_FALL | 0.10661 | 0.10396 | 0.12162 |
| CIN→S_RISE | 0.09003 | 0.08835 | 0.09983 |
| CS→S_FALL | 0.06844 | 0.06769 | 0.07944 |
| CS→S_RISE | 0.05840 | 0.05761 | 0.06470 |

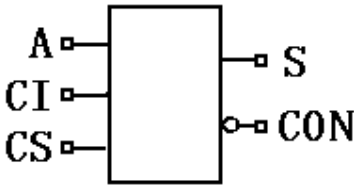
ADH1CSCONHS

Cell Description

The ADH1CSCON cell provides a carry-select halfadder function that produces the arithmetic sum (S) and active-low carryout (CON) of a single operand (A) with carry-in (CI).

$$CON = \neg(A \& CI)$$

$$S = ((CS \& (A \wedge CI)) | ((\neg CS) \& A))$$



Function Table

| CS | CI | A | CON | S |
|----|----|---|-----|---|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|---------------|------------|-----------|
| ADH1CSCONHSV1 | 1.80 | 3.60 |
| ADH1CSCONHSV2 | 1.80 | 3.80 |
| ADH1CSCONHSV4 | 1.80 | 4.20 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00259 | 0.00288 | 0.00377 |
| CI | 0.00244 | 0.00267 | 0.00337 |
| CS | 0.00218 | 0.00240 | 0.00352 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00237 | 0.00252 | 0.00271 |
| CI | 0.00293 | 0.00321 | 0.00335 |
| CS | 0.00207 | 0.00210 | 0.00209 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00066428 | 0.00076387 | 0.00092900 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| A→CON_FALL | 0.01986 | 0.01980 | 0.01759 |
| A→CON_RISE | 0.02151 | 0.02147 | 0.01964 |
| CI→CON_FALL | 0.01812 | 0.01831 | 0.01630 |
| CI→CON_RISE | 0.01927 | 0.01944 | 0.01782 |
| A→S_FALL | 0.10323 | 0.10075 | 0.11535 |
| A→S_RISE | 0.08307 | 0.08047 | 0.09302 |
| CI→S_FALL | 0.11519 | 0.11508 | 0.13254 |
| CI→S_RISE | 0.08392 | 0.08246 | 0.09625 |
| CS→S_FALL | 0.06380 | 0.06364 | 0.07855 |
| CS→S_RISE | 0.05457 | 0.05408 | 0.06426 |

ADH2CONHS

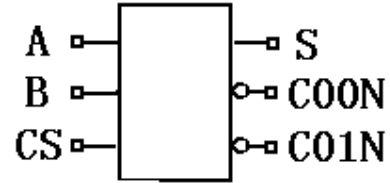
Cell Description

The ADH2CON cell provides a carry-select adder function for the initial stage of carry-select adder block. The function produces the arithmetic sum (S) and active low carryouts (CO0N,CO1N) of two operands (A,B).

$$CO0N = \neg(A \& B)$$

$$CO1N = \neg(A \mid B)$$

$$S = (A \wedge B \wedge CS)$$



Function Table

| CS | B | A | CO0N | CO1N | S |
|----|---|---|------|------|---|
| 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| ADH2CONHSV1 | 1.80 | 4.40 |
| ADH2CONHSV2 | 1.80 | 4.40 |
| ADH2CONHSV4 | 1.80 | 6.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00219 | 0.00236 | 0.00401 |
| B | 0.00223 | 0.00242 | 0.00417 |
| CS | 0.00211 | 0.00230 | 0.00350 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00316 | 0.00340 | 0.00658 |
| B | 0.00325 | 0.00353 | 0.00690 |
| CS | 0.00179 | 0.00189 | 0.00219 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00062690 | 0.00068899 | 0.00136400 |

Delay Table (ns)

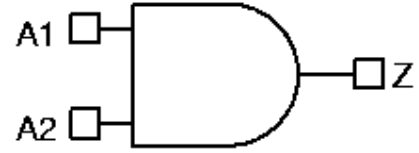
| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| A→CO0N_FALL | 0.02038 | 0.01831 | 0.01547 |
| A→CO0N_RISE | 0.02152 | 0.01983 | 0.01546 |
| B→CO0N_FALL | 0.02375 | 0.02130 | 0.01836 |
| B→CO0N_RISE | 0.02560 | 0.02363 | 0.01862 |
| A→CO1N_FALL | 0.01855 | 0.01730 | 0.01589 |
| A→CO1N_RISE | 0.03608 | 0.03390 | 0.02836 |
| B→CO1N_FALL | 0.01947 | 0.01846 | 0.01747 |
| B→CO1N_RISE | 0.03880 | 0.03685 | 0.03310 |
| A→S_FALL | 0.28064 | 0.25504 | 0.16979 |
| A→S_RISE | 0.26997 | 0.24514 | 0.15993 |
| B→S_FALL | 0.27938 | 0.25470 | 0.17100 |
| B→S_RISE | 0.26836 | 0.24452 | 0.16100 |
| CS→S_FALL | 0.06561 | 0.06154 | 0.05557 |
| CS→S_RISE | 0.05544 | 0.05193 | 0.04848 |

AND2HS

Cell Description

2-Input AND

$Z=(A1\&A2)$



Function Table

| A1 | A2 | Z |
|----|----|---|
| 0 | X | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| AND2HSV0 | 1.80 | 1.00 |
| AND2HSV0RD | 1.80 | 1.00 |
| AND2HSV1 | 1.80 | 1.00 |
| AND2HSV1RD | 1.80 | 1.00 |
| AND2HSV2 | 1.80 | 1.00 |
| AND2HSV2RD | 1.80 | 1.00 |
| AND2HSV4 | 1.80 | 1.40 |
| AND2HSV4RD | 1.80 | 1.80 |
| AND2HSV4RQ | 1.80 | 1.40 |
| AND2HSV8 | 1.80 | 2.40 |
| AND2HSV8RD | 1.80 | 3.40 |
| AND2HSV8RQ | 1.80 | 1.80 |
| AND2HSV12 | 1.80 | 3.40 |
| AND2HSV12RD | 1.80 | 4.40 |
| AND2HSV12RQ | 1.80 | 2.80 |
| AND2HSV16 | 1.80 | 4.40 |
| AND2HSV16RD | 1.80 | 5.80 |
| AND2HSV16RQ | 1.80 | 3.40 |
| AND2HSV20 | 1.80 | 5.40 |
| AND2HSV20RD | 1.80 | 6.80 |
| AND2HSV20RQ | 1.80 | 4.40 |

| | | |
|-------------|------|-------|
| AND2HSV24 | 1.80 | 6.40 |
| AND2HSV24RD | 1.80 | 8.40 |
| AND2HSV24RQ | 1.80 | 4.80 |
| AND2HSV32 | 1.80 | 8.40 |
| AND2HSV40 | 1.80 | 10.40 |
| AND2HSV48 | 1.80 | 12.40 |
| AND2HSV64 | 1.80 | 16.40 |

Pin Power (uW/MHz)

| Pin | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00107 | 0.00110 | 0.00123 | 0.00146 | 0.00146 | 0.00166 | 0.00251 | 0.00308 |
| A2 | 0.00120 | 0.00098 | 0.00135 | 0.00132 | 0.00158 | 0.00149 | 0.00267 | 0.00275 |

| Pin | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00242 | 0.00484 | 0.00603 | 0.00439 | 0.00749 | 0.00870 | 0.00648 | 0.00977 |
| A2 | 0.00227 | 0.00517 | 0.00540 | 0.00419 | 0.00693 | 0.00784 | 0.00616 | 0.00903 |

| Pin | V16RD | V16RQ | V20 | V20RD | V20RQ | V24 | V24RD | V24RQ |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.01158 | 0.00853 | 0.01232 | 0.01418 | 0.01066 | 0.01452 | 0.01722 | 0.01271 |
| A2 | 0.01035 | 0.00813 | 0.01140 | 0.01270 | 0.01017 | 0.01341 | 0.01542 | 0.01215 |

| Pin | V32 | V40 | V48 | V64 |
|-----|---------|---------|---------|---------|
| A1 | 0.01932 | 0.02421 | 0.02898 | 0.03892 |
| A2 | 0.01782 | 0.02237 | 0.02676 | 0.03594 |

Pin Capacitance (pf)

| Pin | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00107 | 0.00099 | 0.00107 | 0.00113 | 0.00103 | 0.00129 | 0.00146 | 0.00257 |
| A2 | 0.00112 | 0.00096 | 0.00111 | 0.00112 | 0.00108 | 0.00124 | 0.00152 | 0.00237 |

| Pin | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00116 | 0.00266 | 0.00500 | 0.00153 | 0.00418 | 0.00667 | 0.00261 | 0.00557 |
| A2 | 0.00107 | 0.00291 | 0.00488 | 0.00146 | 0.00416 | 0.00693 | 0.00233 | 0.00544 |

| Pin | V16RD | V16RQ | V20 | V20RD | V20RQ | V24 | V24RD | V24RQ |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00922 | 0.00305 | 0.00691 | 0.01059 | 0.00397 | 0.00830 | 0.01357 | 0.00442 |
| A2 | 0.00936 | 0.00279 | 0.00690 | 0.01103 | 0.00394 | 0.00820 | 0.01374 | 0.00440 |

| Pin | V32 | V40 | V48 | V64 |
|-----|---------|---------|---------|---------|
| A1 | 0.01106 | 0.01381 | 0.01655 | 0.02202 |
| A2 | 0.01099 | 0.01377 | 0.01657 | 0.02210 |

Max Leakage Power (uW)

| V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|----|------|----|------|----|------|----|------|
|----|------|----|------|----|------|----|------|

| | | | | | | | |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00015584 | 0.00014146 | 0.00017091 | 0.00018773 | 0.00019869 | 0.00021288 | 0.00037542 | 0.00046913 |
|------------|------------|------------|------------|------------|------------|------------|------------|

| | | | | | | | |
|------------|------------|------------|------------|------------|------------|------------|------------|
| V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
| 0.00032020 | 0.00081324 | 0.00099954 | 0.00065630 | 0.00123810 | 0.00138050 | 0.00108420 | 0.00168790 |

| | | | | | | | |
|------------|------------|------------|------------|------------|------------|------------|------------|
| V16RD | V16RQ | V20 | V20RD | V20RQ | V24 | V24RD | V24RQ |
| 0.00203880 | 0.00142480 | 0.00214080 | 0.00235340 | 0.00186380 | 0.00259500 | 0.00305990 | 0.00220870 |

| | | | |
|------------|------------|------------|------------|
| V32 | V40 | V48 | V64 |
| 0.00350380 | 0.00441270 | 0.00532340 | 0.00713940 |

Delay Table (ns)

| Description | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→Z_FALL | 0.03521 | 0.04359 | 0.03579 | 0.04084 | 0.03723 | 0.03883 | 0.03643 | 0.03523 |
| A1→Z_RISE | 0.04534 | 0.04665 | 0.04643 | 0.04290 | 0.05023 | 0.04064 | 0.04680 | 0.03567 |
| A2→Z_FALL | 0.03807 | 0.03969 | 0.03864 | 0.03714 | 0.03998 | 0.03506 | 0.03927 | 0.03134 |
| A2→Z_RISE | 0.04840 | 0.04376 | 0.04941 | 0.04027 | 0.05317 | 0.03791 | 0.04974 | 0.03289 |

| Description | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→Z_FALL | 0.05220 | 0.03412 | 0.03392 | 0.04988 | 0.03945 | 0.03333 | 0.04695 | 0.03857 |
| A1→Z_RISE | 0.05400 | 0.04291 | 0.03392 | 0.05783 | 0.03946 | 0.03298 | 0.05452 | 0.03844 |
| A2→Z_FALL | 0.04770 | 0.03692 | 0.03015 | 0.04643 | 0.03574 | 0.02991 | 0.04360 | 0.03491 |
| A2→Z_RISE | 0.05059 | 0.04597 | 0.03138 | 0.05480 | 0.03693 | 0.03079 | 0.05149 | 0.03592 |

| Description | V16RD | V16RQ | V20 | V20RD | V20RQ | V24 | V24RD | V24RQ |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→Z_FALL | 0.03290 | 0.04761 | 0.03873 | 0.03311 | 0.04687 | 0.03832 | 0.03293 | 0.04747 |
| A1→Z_RISE | 0.03251 | 0.05445 | 0.03853 | 0.03253 | 0.05361 | 0.03806 | 0.03231 | 0.05386 |
| A2→Z_FALL | 0.02930 | 0.04435 | 0.03510 | 0.02946 | 0.04376 | 0.03470 | 0.02929 | 0.04436 |
| A2→Z_RISE | 0.03009 | 0.05156 | 0.03608 | 0.03015 | 0.05104 | 0.03559 | 0.02994 | 0.05133 |

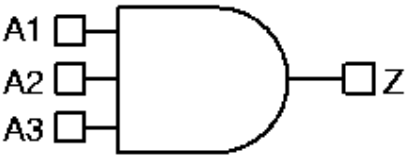
| Description | V32 | V40 | V48 | V64 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.03843 | 0.03837 | 0.03871 | 0.03839 |
| A1→Z_RISE | 0.03807 | 0.03797 | 0.03832 | 0.03812 |
| A2→Z_FALL | 0.03479 | 0.03476 | 0.03508 | 0.03481 |
| A2→Z_RISE | 0.03563 | 0.03557 | 0.03592 | 0.03573 |

AND3HS

Cell Description

3-Input AND

$$Z=(A1\&A2\&A3)$$



Function Table

| A1 | A2 | A3 | Z |
|----|----|----|---|
| 0 | X | X | 0 |
| 1 | 0 | X | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| AND3HSV0 | 1.80 | 1.40 |
| AND3HSV0RD | 1.80 | 1.40 |
| AND3HSV1 | 1.80 | 1.40 |
| AND3HSV1RD | 1.80 | 1.40 |
| AND3HSV2 | 1.80 | 1.40 |
| AND3HSV2RD | 1.80 | 1.40 |
| AND3HSV4 | 1.80 | 1.60 |
| AND3HSV4RD | 1.80 | 2.40 |
| AND3HSV4RQ | 1.80 | 1.60 |
| AND3HSV8 | 1.80 | 2.80 |
| AND3HSV8RD | 1.80 | 4.20 |
| AND3HSV8RQ | 1.80 | 2.20 |
| AND3HSV12 | 1.80 | 4.00 |
| AND3HSV12RD | 1.80 | 6.40 |
| AND3HSV12RQ | 1.80 | 3.20 |
| AND3HSV16 | 1.80 | 5.40 |
| AND3HSV16RD | 1.80 | 7.60 |
| AND3HSV16RQ | 1.80 | 3.80 |

Pin Power (uW/MHz)

| Pin | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00122 | 0.00113 | 0.00140 | 0.00152 | 0.00164 | 0.00168 | 0.00274 | 0.00304 |
| A2 | 0.00130 | 0.00120 | 0.00148 | 0.00169 | 0.00172 | 0.00186 | 0.00288 | 0.00342 |
| A3 | 0.00142 | 0.00132 | 0.00159 | 0.00186 | 0.00182 | 0.00204 | 0.00304 | 0.00386 |

| Pin | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00237 | 0.00518 | 0.00591 | 0.00445 | 0.00736 | 0.00898 | 0.00650 | 0.00970 |
| A2 | 0.00248 | 0.00549 | 0.00667 | 0.00462 | 0.00790 | 0.01013 | 0.00681 | 0.01046 |
| A3 | 0.00261 | 0.00587 | 0.00754 | 0.00480 | 0.00854 | 0.01137 | 0.00715 | 0.01132 |

| Pin | V16RD | V16RQ |
|-----|---------|---------|
| A1 | 0.01170 | 0.00869 |
| A2 | 0.01317 | 0.00908 |
| A3 | 0.01479 | 0.00953 |

Pin Capacitance (pf)

| Pin | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00109 | 0.00100 | 0.00108 | 0.00129 | 0.00108 | 0.00136 | 0.00146 | 0.00247 |
| A2 | 0.00104 | 0.00095 | 0.00104 | 0.00125 | 0.00105 | 0.00135 | 0.00144 | 0.00268 |
| A3 | 0.00110 | 0.00101 | 0.00107 | 0.00127 | 0.00107 | 0.00135 | 0.00145 | 0.00296 |

| Pin | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00110 | 0.00260 | 0.00501 | 0.00153 | 0.00417 | 0.00794 | 0.00230 | 0.00549 |
| A2 | 0.00106 | 0.00284 | 0.00502 | 0.00150 | 0.00417 | 0.00784 | 0.00249 | 0.00551 |
| A3 | 0.00109 | 0.00312 | 0.00545 | 0.00151 | 0.00463 | 0.00830 | 0.00281 | 0.00593 |

| Pin | V16RD | V16RQ |
|-----|---------|---------|
| A1 | 0.01016 | 0.00275 |
| A2 | 0.01004 | 0.00289 |
| A3 | 0.01053 | 0.00324 |

Max Leakage Power (uW)

| V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00021514 | 0.00018993 | 0.00022782 | 0.00024315 | 0.00026013 | 0.00028223 | 0.00045924 | 0.00060855 |

| V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00039956 | 0.00094784 | 0.00114780 | 0.00075611 | 0.00142680 | 0.00194730 | 0.00121360 | 0.00198410 |

| V16RD | V16RQ |
|------------|------------|
| 0.00246020 | 0.00162690 |

Delay Table (ns)

| Description | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-------------|----|------|----|------|----|------|----|------|
|-------------|----|------|----|------|----|------|----|------|

| | | | | | | | | |
|-----------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→Z_FALL | 0.03899 | 0.04444 | 0.03987 | 0.04247 | 0.04108 | 0.03897 | 0.03922 | 0.03442 |
| A1→Z_RISE | 0.06418 | 0.06135 | 0.06670 | 0.04494 | 0.07068 | 0.04570 | 0.06579 | 0.03949 |
| A2→Z_FALL | 0.04093 | 0.04718 | 0.04186 | 0.04729 | 0.04309 | 0.04313 | 0.04144 | 0.03885 |
| A2→Z_RISE | 0.06748 | 0.06463 | 0.07007 | 0.04900 | 0.07418 | 0.04984 | 0.06966 | 0.04421 |
| A3→Z_FALL | 0.04393 | 0.05143 | 0.04460 | 0.05207 | 0.04560 | 0.04714 | 0.04381 | 0.04350 |
| A3→Z_RISE | 0.07167 | 0.06895 | 0.07369 | 0.05187 | 0.07741 | 0.05264 | 0.07255 | 0.04784 |

| Description | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→Z_FALL | 0.04985 | 0.03630 | 0.03406 | 0.04847 | 0.03800 | 0.03303 | 0.04558 | 0.03735 |
| A1→Z_RISE | 0.06965 | 0.05947 | 0.03747 | 0.07514 | 0.05089 | 0.03753 | 0.07099 | 0.04891 |
| A2→Z_FALL | 0.05279 | 0.03877 | 0.03853 | 0.05123 | 0.04129 | 0.03723 | 0.04856 | 0.04073 |
| A2→Z_RISE | 0.07330 | 0.06415 | 0.04183 | 0.07930 | 0.05517 | 0.04186 | 0.07580 | 0.05331 |
| A3→Z_FALL | 0.05641 | 0.04161 | 0.04340 | 0.05400 | 0.04512 | 0.04166 | 0.05188 | 0.04451 |
| A3→Z_RISE | 0.07655 | 0.06803 | 0.04548 | 0.08185 | 0.05903 | 0.04530 | 0.07964 | 0.05687 |

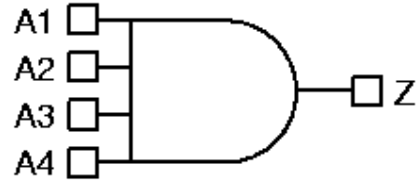
| Description | V16RD | V16RQ |
|-------------|---------|---------|
| A1→Z_FALL | 0.03288 | 0.04623 |
| A1→Z_RISE | 0.03676 | 0.07093 |
| A2→Z_FALL | 0.03697 | 0.04922 |
| A2→Z_RISE | 0.04086 | 0.07569 |
| A3→Z_FALL | 0.04140 | 0.05254 |
| A3→Z_RISE | 0.04413 | 0.07947 |

AND4HS

Cell Description

4-Input AND

$Z=(A1\&A2\&A3\&A4)$



Function Table

| A1 | A2 | A3 | A4 | Z |
|----|----|----|----|---|
| 0 | X | X | X | 0 |
| 1 | 0 | X | X | 0 |
| 1 | 1 | 0 | X | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| AND4HSV0 | 1.80 | 1.60 |
| AND4HSV0RD | 1.80 | 1.60 |
| AND4HSV1 | 1.80 | 1.60 |
| AND4HSV1RD | 1.80 | 1.60 |
| AND4HSV2 | 1.80 | 1.60 |
| AND4HSV2RD | 1.80 | 1.60 |
| AND4HSV4 | 1.80 | 1.80 |
| AND4HSV4RD | 1.80 | 2.80 |
| AND4HSV4RQ | 1.80 | 1.80 |
| AND4HSV8 | 1.80 | 4.00 |
| AND4HSV8RD | 1.80 | 6.20 |
| AND4HSV8RQ | 1.80 | 3.60 |
| AND4HSV12 | 1.80 | 7.00 |
| AND4HSV12RD | 1.80 | 9.20 |
| AND4HSV12RQ | 1.80 | 5.60 |
| AND4HSV16 | 1.80 | 9.40 |
| AND4HSV16RD | 1.80 | 11.80 |
| AND4HSV16RQ | 1.80 | 6.40 |

Pin Power (uW/MHz)

| Pin | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00142 | 0.00131 | 0.00153 | 0.00166 | 0.00177 | 0.00184 | 0.00286 | 0.00323 |
| A2 | 0.00153 | 0.00142 | 0.00163 | 0.00186 | 0.00187 | 0.00205 | 0.00302 | 0.00366 |
| A3 | 0.00162 | 0.00151 | 0.00174 | 0.00204 | 0.00197 | 0.00224 | 0.00318 | 0.00407 |
| A4 | 0.00174 | 0.00163 | 0.00184 | 0.00221 | 0.00207 | 0.00241 | 0.00334 | 0.00447 |

| Pin | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00253 | 0.00589 | 0.00621 | 0.00494 | 0.00815 | 0.00935 | 0.00733 | 0.01085 |
| A2 | 0.00274 | 0.00618 | 0.00698 | 0.00511 | 0.00895 | 0.01051 | 0.00772 | 0.01189 |
| A3 | 0.00293 | 0.00650 | 0.00761 | 0.00609 | 0.01000 | 0.01135 | 0.00914 | 0.01334 |
| A4 | 0.00313 | 0.00693 | 0.00835 | 0.00624 | 0.01075 | 0.01249 | 0.00952 | 0.01434 |

| Pin | V16RD | V16RQ |
|-----|---------|---------|
| A1 | 0.01241 | 0.00974 |
| A2 | 0.01393 | 0.01013 |
| A3 | 0.01494 | 0.01175 |
| A4 | 0.01641 | 0.01214 |

Pin Capacitance (pf)

| Pin | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00103 | 0.00094 | 0.00102 | 0.00122 | 0.00101 | 0.00129 | 0.00138 | 0.00243 |
| A2 | 0.00112 | 0.00103 | 0.00106 | 0.00125 | 0.00107 | 0.00135 | 0.00144 | 0.00263 |
| A3 | 0.00113 | 0.00103 | 0.00112 | 0.00131 | 0.00112 | 0.00140 | 0.00145 | 0.00290 |
| A4 | 0.00119 | 0.00109 | 0.00111 | 0.00131 | 0.00114 | 0.00142 | 0.00149 | 0.00305 |

| Pin | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00119 | 0.00330 | 0.00514 | 0.00167 | 0.00507 | 0.00790 | 0.00272 | 0.00690 |
| A2 | 0.00126 | 0.00328 | 0.00545 | 0.00167 | 0.00537 | 0.00816 | 0.00295 | 0.00708 |
| A3 | 0.00129 | 0.00322 | 0.00530 | 0.00170 | 0.00523 | 0.00806 | 0.00271 | 0.00710 |
| A4 | 0.00133 | 0.00365 | 0.00545 | 0.00158 | 0.00531 | 0.00810 | 0.00295 | 0.00710 |

| Pin | V16RD | V16RQ |
|-----|---------|---------|
| A1 | 0.01048 | 0.00303 |
| A2 | 0.01074 | 0.00325 |
| A3 | 0.01075 | 0.00300 |
| A4 | 0.01070 | 0.00331 |

Max Leakage Power (uW)

| V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00027481 | 0.00024599 | 0.00028723 | 0.00031057 | 0.00031869 | 0.00035172 | 0.00051658 | 0.00073063 |

| V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00046386 | 0.00110980 | 0.00183750 | 0.00124540 | 0.00233130 | 0.00291540 | 0.00206940 | 0.00316610 |

| | |
|------------|------------|
| V16RD | V16RQ |
| 0.00375710 | 0.00262490 |

Delay Table (ns)

| Description | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→Z_FALL | 0.04347 | 0.04968 | 0.04258 | 0.04549 | 0.04355 | 0.04199 | 0.04028 | 0.03635 |
| A1→Z_RISE | 0.08620 | 0.08165 | 0.08625 | 0.05674 | 0.09155 | 0.05820 | 0.08253 | 0.04915 |
| A2→Z_FALL | 0.04660 | 0.05397 | 0.04551 | 0.05136 | 0.04647 | 0.04711 | 0.04322 | 0.04136 |
| A2→Z_RISE | 0.09437 | 0.08967 | 0.09385 | 0.06439 | 0.09932 | 0.06588 | 0.09009 | 0.05688 |
| A3→Z_FALL | 0.04888 | 0.05718 | 0.04809 | 0.05604 | 0.04903 | 0.05105 | 0.04549 | 0.04565 |
| A3→Z_RISE | 0.09904 | 0.09448 | 0.09958 | 0.06926 | 0.10505 | 0.07073 | 0.09463 | 0.06242 |
| A4→Z_FALL | 0.05182 | 0.06134 | 0.05017 | 0.06009 | 0.05111 | 0.05437 | 0.04769 | 0.04941 |
| A4→Z_RISE | 0.10470 | 0.10012 | 0.10304 | 0.07218 | 0.10840 | 0.07352 | 0.09831 | 0.06609 |

| Description | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→Z_FALL | 0.05369 | 0.04103 | 0.03252 | 0.04857 | 0.03844 | 0.03214 | 0.04612 | 0.03836 |
| A1→Z_RISE | 0.06355 | 0.08103 | 0.03531 | 0.06574 | 0.03725 | 0.03510 | 0.05125 | 0.03685 |
| A2→Z_FALL | 0.06000 | 0.04331 | 0.03673 | 0.05105 | 0.04315 | 0.03621 | 0.04985 | 0.04286 |
| A2→Z_RISE | 0.07121 | 0.08669 | 0.03793 | 0.06803 | 0.03982 | 0.03764 | 0.05403 | 0.03936 |
| A3→Z_FALL | 0.06496 | 0.04567 | 0.03712 | 0.05352 | 0.04316 | 0.03621 | 0.05151 | 0.04317 |
| A3→Z_RISE | 0.07587 | 0.09101 | 0.04382 | 0.08004 | 0.04598 | 0.04325 | 0.06340 | 0.04571 |
| A4→Z_FALL | 0.06976 | 0.04623 | 0.04120 | 0.05571 | 0.04762 | 0.04035 | 0.05515 | 0.04770 |
| A4→Z_RISE | 0.07932 | 0.09657 | 0.04629 | 0.08223 | 0.04840 | 0.04576 | 0.06620 | 0.04809 |

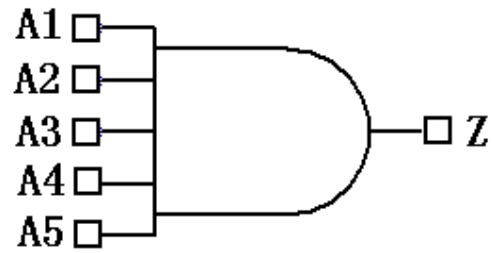
| Description | V16RD | V16RQ |
|-------------|---------|---------|
| A1→Z_FALL | 0.03233 | 0.04696 |
| A1→Z_RISE | 0.03476 | 0.06249 |
| A2→Z_FALL | 0.03644 | 0.04972 |
| A2→Z_RISE | 0.03724 | 0.06532 |
| A3→Z_FALL | 0.03638 | 0.05008 |
| A3→Z_RISE | 0.04260 | 0.07145 |
| A4→Z_FALL | 0.04040 | 0.05301 |
| A4→Z_RISE | 0.04498 | 0.07428 |

AND5HS

Cell Description

5-input AND

$Z=(A1\&A2\&A3\&A4\&A5)$



Function Table

| A1 | A2 | A3 | A4 | A5 | Z |
|----|----|----|----|----|---|
| 0 | X | X | X | X | 0 |
| 1 | 0 | X | X | X | 0 |
| 1 | 1 | 0 | X | X | 0 |
| 1 | 1 | 1 | 0 | X | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| AND5HSV0 | 1.80 | 2.20 |
| AND5HSV0RD | 1.80 | 2.20 |
| AND5HSV1 | 1.80 | 2.20 |
| AND5HSV1RD | 1.80 | 2.20 |
| AND5HSV2 | 1.80 | 2.20 |
| AND5HSV2RD | 1.80 | 2.20 |
| AND5HSV4 | 1.80 | 4.40 |
| AND5HSV4RD | 1.80 | 4.60 |
| AND5HSV4RQ | 1.80 | 3.20 |
| AND5HSV8 | 1.80 | 7.80 |
| AND5HSV8RD | 1.80 | 8.00 |
| AND5HSV8RQ | 1.80 | 4.00 |
| AND5HSV12 | 1.80 | 11.00 |
| AND5HSV12RD | 1.80 | 11.00 |
| AND5HSV12RQ | 1.80 | 6.40 |
| AND5HSV16 | 1.80 | 14.00 |
| AND5HSV16RD | 1.80 | 14.00 |
| AND5HSV16RQ | 1.80 | 7.40 |

Pin Power (uW/MHz)

| Pin | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00119 | 0.00120 | 0.00144 | 0.00155 | 0.00166 | 0.00178 | 0.00323 | 0.00357 |
| A2 | 0.00126 | 0.00128 | 0.00153 | 0.00171 | 0.00176 | 0.00193 | 0.00346 | 0.00396 |
| A3 | 0.00141 | 0.00139 | 0.00174 | 0.00192 | 0.00207 | 0.00218 | 0.00388 | 0.00430 |
| A4 | 0.00154 | 0.00152 | 0.00189 | 0.00210 | 0.00223 | 0.00237 | 0.00422 | 0.00479 |
| A5 | 0.00166 | 0.00164 | 0.00202 | 0.00229 | 0.00239 | 0.00254 | 0.00457 | 0.00523 |

| Pin | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00291 | 0.00552 | 0.00616 | 0.00474 | 0.00831 | 0.00862 | 0.00724 | 0.01065 |
| A2 | 0.00304 | 0.00614 | 0.00709 | 0.00488 | 0.00920 | 0.00995 | 0.00759 | 0.01189 |
| A3 | 0.00349 | 0.00739 | 0.00789 | 0.00627 | 0.01093 | 0.01134 | 0.00930 | 0.01465 |
| A4 | 0.00366 | 0.00826 | 0.00885 | 0.00643 | 0.01221 | 0.01274 | 0.00978 | 0.01633 |
| A5 | 0.00378 | 0.00898 | 0.00965 | 0.00659 | 0.01328 | 0.01392 | 0.01022 | 0.01774 |

| Pin | V16RD | V16RQ |
|-----|---------|---------|
| A1 | 0.01174 | 0.00934 |
| A2 | 0.01361 | 0.00981 |
| A3 | 0.01533 | 0.01211 |
| A4 | 0.01710 | 0.01259 |
| A5 | 0.01871 | 0.01298 |

Pin Capacitance (pf)

| Pin | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00098 | 0.00100 | 0.00105 | 0.00135 | 0.00117 | 0.00148 | 0.00220 | 0.00265 |
| A2 | 0.00090 | 0.00091 | 0.00098 | 0.00127 | 0.00107 | 0.00134 | 0.00202 | 0.00283 |
| A3 | 0.00101 | 0.00105 | 0.00111 | 0.00141 | 0.00125 | 0.00145 | 0.00232 | 0.00282 |
| A4 | 0.00104 | 0.00109 | 0.00117 | 0.00134 | 0.00123 | 0.00143 | 0.00231 | 0.00271 |
| A5 | 0.00105 | 0.00103 | 0.00108 | 0.00142 | 0.00126 | 0.00146 | 0.00251 | 0.00252 |

| Pin | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00131 | 0.00341 | 0.00492 | 0.00167 | 0.00520 | 0.00720 | 0.00277 | 0.00648 |
| A2 | 0.00119 | 0.00327 | 0.00479 | 0.00158 | 0.00514 | 0.00701 | 0.00289 | 0.00625 |
| A3 | 0.00130 | 0.00414 | 0.00497 | 0.00166 | 0.00609 | 0.00734 | 0.00277 | 0.00802 |
| A4 | 0.00135 | 0.00394 | 0.00475 | 0.00161 | 0.00587 | 0.00710 | 0.00265 | 0.00777 |
| A5 | 0.00122 | 0.00397 | 0.00478 | 0.00156 | 0.00593 | 0.00714 | 0.00268 | 0.00784 |

| Pin | V16RD | V16RQ |
|-----|---------|---------|
| A1 | 0.00961 | 0.00307 |
| A2 | 0.00953 | 0.00299 |
| A3 | 0.00969 | 0.00302 |
| A4 | 0.00918 | 0.00296 |
| A5 | 0.00941 | 0.00296 |

Max Leakage Power (uW)

| V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00034873 | 0.00034781 | 0.00040145 | 0.00045038 | 0.00046701 | 0.00051526 | 0.00100400 | 0.00107790 |

| V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00068900 | 0.00181130 | 0.00207180 | 0.00126230 | 0.00293810 | 0.00319360 | 0.00205630 | 0.00378280 |

| V16RD | V16RQ |
|------------|------------|
| 0.00413690 | 0.00266140 |

Delay Table (ns)

| Description | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→Z_FALL | 0.04591 | 0.04621 | 0.04685 | 0.03999 | 0.04458 | 0.03762 | 0.04198 | 0.03588 |
| A1→Z_RISE | 0.06171 | 0.05956 | 0.05310 | 0.04501 | 0.04966 | 0.04493 | 0.04401 | 0.04063 |
| A2→Z_FALL | 0.04852 | 0.04918 | 0.04994 | 0.04364 | 0.04783 | 0.04066 | 0.04546 | 0.03993 |
| A2→Z_RISE | 0.06304 | 0.06104 | 0.05476 | 0.04724 | 0.05144 | 0.04674 | 0.04583 | 0.04348 |
| A3→Z_FALL | 0.05212 | 0.05151 | 0.05341 | 0.04625 | 0.05208 | 0.04306 | 0.04707 | 0.04101 |
| A3→Z_RISE | 0.07486 | 0.07283 | 0.06701 | 0.06165 | 0.06453 | 0.06404 | 0.05799 | 0.05930 |
| A4→Z_FALL | 0.05761 | 0.05694 | 0.05904 | 0.05076 | 0.05721 | 0.04696 | 0.05247 | 0.04603 |
| A4→Z_RISE | 0.08018 | 0.07791 | 0.07222 | 0.06600 | 0.06897 | 0.06862 | 0.06259 | 0.06527 |
| A5→Z_FALL | 0.06160 | 0.06084 | 0.06275 | 0.05532 | 0.06193 | 0.05035 | 0.05761 | 0.04991 |
| A5→Z_RISE | 0.08250 | 0.07995 | 0.07389 | 0.06910 | 0.07147 | 0.07110 | 0.06589 | 0.06848 |

| Description | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→Z_FALL | 0.05390 | 0.03960 | 0.03280 | 0.04661 | 0.03703 | 0.03065 | 0.04550 | 0.03776 |
| A1→Z_RISE | 0.05404 | 0.03915 | 0.03538 | 0.06447 | 0.03861 | 0.03372 | 0.05173 | 0.03664 |
| A2→Z_FALL | 0.05705 | 0.04490 | 0.03761 | 0.04853 | 0.04174 | 0.03519 | 0.04883 | 0.04304 |
| A2→Z_RISE | 0.05565 | 0.04229 | 0.03867 | 0.06619 | 0.04157 | 0.03685 | 0.05428 | 0.03967 |
| A3→Z_FALL | 0.05822 | 0.04389 | 0.03713 | 0.05312 | 0.04279 | 0.03562 | 0.05145 | 0.04303 |
| A3→Z_RISE | 0.07960 | 0.05416 | 0.05451 | 0.10237 | 0.05401 | 0.05309 | 0.08271 | 0.05349 |
| A4→Z_FALL | 0.06246 | 0.05049 | 0.04197 | 0.05554 | 0.04940 | 0.04043 | 0.05579 | 0.04965 |
| A4→Z_RISE | 0.08417 | 0.06032 | 0.06064 | 0.10641 | 0.06009 | 0.05912 | 0.08885 | 0.05958 |
| A5→Z_FALL | 0.06562 | 0.05538 | 0.04547 | 0.05758 | 0.05413 | 0.04389 | 0.05935 | 0.05435 |
| A5→Z_RISE | 0.08596 | 0.06326 | 0.06359 | 0.10865 | 0.06293 | 0.06194 | 0.09222 | 0.06235 |

| Description | V16RD | V16RQ |
|-------------|---------|---------|
| A1→Z_FALL | 0.03113 | 0.04512 |
| A1→Z_RISE | 0.03413 | 0.06087 |
| A2→Z_FALL | 0.03597 | 0.04834 |
| A2→Z_RISE | 0.03738 | 0.06423 |
| A3→Z_FALL | 0.03618 | 0.05040 |
| A3→Z_RISE | 0.05385 | 0.09742 |
| A4→Z_FALL | 0.04189 | 0.05393 |
| A4→Z_RISE | 0.05943 | 0.10420 |

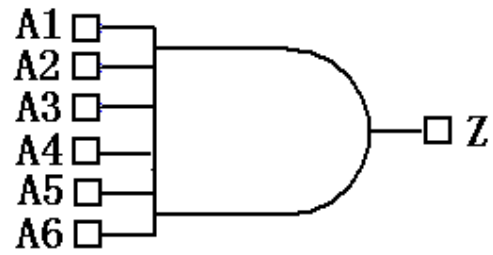
| | | |
|-----------|---------|---------|
| A5→Z_FALL | 0.04520 | 0.05647 |
| A5→Z_RISE | 0.06299 | 0.10723 |

AND6HS

Cell Description

6-input AND

$Z=(A1\&A2\&A3\&A4\&A5\&A6)$



Function Table

| A1 | A2 | A3 | A4 | A5 | A6 | Z |
|----|----|----|----|----|----|---|
| 0 | X | X | X | X | X | 0 |
| 1 | 0 | X | X | X | X | 0 |
| 1 | 1 | 0 | X | X | X | 0 |
| 1 | 1 | 1 | 0 | X | X | 0 |
| 1 | 1 | 1 | 1 | 0 | X | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| AND6HSV0 | 1.80 | 2.40 |
| AND6HSV0RD | 1.80 | 2.40 |
| AND6HSV1 | 1.80 | 2.40 |
| AND6HSV1RD | 1.80 | 2.40 |
| AND6HSV2 | 1.80 | 2.40 |
| AND6HSV2RD | 1.80 | 2.40 |
| AND6HSV4 | 1.80 | 4.20 |
| AND6HSV4RD | 1.80 | 4.80 |
| AND6HSV4RQ | 1.80 | 3.20 |
| AND6HSV8 | 1.80 | 8.40 |
| AND6HSV8RD | 1.80 | 9.00 |
| AND6HSV8RQ | 1.80 | 4.20 |
| AND6HSV12 | 1.80 | 12.80 |
| AND6HSV12RD | 1.80 | 12.80 |
| AND6HSV12RQ | 1.80 | 6.80 |
| AND6HSV16 | 1.80 | 16.80 |
| AND6HSV16RD | 1.80 | 16.80 |

| | | |
|-------------|------|------|
| AND6HSV16RQ | 1.80 | 7.80 |
|-------------|------|------|

Pin Power (uW/MHz)

| Pin | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00135 | 0.00134 | 0.00159 | 0.00176 | 0.00184 | 0.00196 | 0.00305 | 0.00347 |
| A2 | 0.00146 | 0.00148 | 0.00172 | 0.00194 | 0.00200 | 0.00215 | 0.00338 | 0.00385 |
| A3 | 0.00160 | 0.00161 | 0.00188 | 0.00214 | 0.00219 | 0.00235 | 0.00375 | 0.00427 |
| A4 | 0.00144 | 0.00142 | 0.00177 | 0.00195 | 0.00206 | 0.00219 | 0.00377 | 0.00411 |
| A5 | 0.00155 | 0.00155 | 0.00190 | 0.00212 | 0.00222 | 0.00237 | 0.00409 | 0.00447 |
| A6 | 0.00168 | 0.00167 | 0.00205 | 0.00233 | 0.00239 | 0.00258 | 0.00448 | 0.00489 |

| Pin | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00278 | 0.00603 | 0.00664 | 0.00507 | 0.00855 | 0.00953 | 0.00722 | 0.01132 |
| A2 | 0.00296 | 0.00682 | 0.00764 | 0.00525 | 0.00982 | 0.01091 | 0.00759 | 0.01299 |
| A3 | 0.00312 | 0.00760 | 0.00845 | 0.00544 | 0.01089 | 0.01209 | 0.00800 | 0.01442 |
| A4 | 0.00349 | 0.00736 | 0.00795 | 0.00630 | 0.01054 | 0.01142 | 0.00908 | 0.01388 |
| A5 | 0.00364 | 0.00813 | 0.00893 | 0.00648 | 0.01180 | 0.01280 | 0.00945 | 0.01554 |
| A6 | 0.00383 | 0.00891 | 0.00976 | 0.00668 | 0.01286 | 0.01398 | 0.00983 | 0.01695 |

| Pin | V16RD | V16RQ |
|-----|---------|---------|
| A1 | 0.01250 | 0.00945 |
| A2 | 0.01433 | 0.00992 |
| A3 | 0.01591 | 0.01035 |
| A4 | 0.01511 | 0.01186 |
| A5 | 0.01694 | 0.01232 |
| A6 | 0.01853 | 0.01276 |

Pin Capacitance (pf)

| Pin | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00096 | 0.00093 | 0.00103 | 0.00136 | 0.00118 | 0.00143 | 0.00203 | 0.00257 |
| A2 | 0.00098 | 0.00097 | 0.00105 | 0.00128 | 0.00120 | 0.00135 | 0.00212 | 0.00274 |
| A3 | 0.00102 | 0.00102 | 0.00108 | 0.00133 | 0.00122 | 0.00140 | 0.00238 | 0.00311 |
| A4 | 0.00097 | 0.00096 | 0.00105 | 0.00133 | 0.00118 | 0.00140 | 0.00203 | 0.00260 |
| A5 | 0.00097 | 0.00104 | 0.00104 | 0.00130 | 0.00116 | 0.00138 | 0.00215 | 0.00273 |
| A6 | 0.00103 | 0.00101 | 0.00111 | 0.00144 | 0.00123 | 0.00152 | 0.00246 | 0.00313 |

| Pin | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00121 | 0.00372 | 0.00494 | 0.00159 | 0.00575 | 0.00707 | 0.00258 | 0.00755 |
| A2 | 0.00125 | 0.00381 | 0.00479 | 0.00162 | 0.00554 | 0.00683 | 0.00271 | 0.00728 |
| A3 | 0.00125 | 0.00390 | 0.00490 | 0.00161 | 0.00560 | 0.00690 | 0.00304 | 0.00735 |
| A4 | 0.00133 | 0.00380 | 0.00502 | 0.00160 | 0.00578 | 0.00706 | 0.00256 | 0.00755 |
| A5 | 0.00124 | 0.00386 | 0.00483 | 0.00159 | 0.00553 | 0.00683 | 0.00275 | 0.00725 |
| A6 | 0.00131 | 0.00389 | 0.00489 | 0.00165 | 0.00556 | 0.00687 | 0.00293 | 0.00729 |

| Pin | V16RD | V16RQ |
|-----|-------|-------|
|-----|-------|-------|

| | | |
|----|---------|---------|
| A1 | 0.00939 | 0.00309 |
| A2 | 0.00906 | 0.00300 |
| A3 | 0.00916 | 0.00300 |
| A4 | 0.00941 | 0.00311 |
| A5 | 0.00905 | 0.00300 |
| A6 | 0.00920 | 0.00300 |

Max Leakage Power (uW)

| | | | | | | | |
|------------|------------|------------|------------|------------|------------|------------|------------|
| V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
| 0.00041834 | 0.00041397 | 0.00047449 | 0.00053940 | 0.00056286 | 0.00062353 | 0.00092430 | 0.00120360 |

| | | | | | | | |
|------------|------------|------------|------------|------------|------------|------------|------------|
| V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
| 0.00079342 | 0.00192960 | 0.00231050 | 0.00139360 | 0.00287040 | 0.00311120 | 0.00216180 | 0.00383290 |

| | |
|------------|------------|
| V16RD | V16RQ |
| 0.00449870 | 0.00280190 |

Delay Table (ns)

| | | | | | | | | |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| Description | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
| A1→Z_FALL | 0.05058 | 0.05030 | 0.05097 | 0.04386 | 0.04887 | 0.04061 | 0.04395 | 0.03616 |
| A1→Z_RISE | 0.07065 | 0.06909 | 0.06146 | 0.05583 | 0.05708 | 0.05738 | 0.04592 | 0.04950 |
| A2→Z_FALL | 0.05533 | 0.05604 | 0.05593 | 0.04851 | 0.05406 | 0.04448 | 0.04978 | 0.03997 |
| A2→Z_RISE | 0.07524 | 0.07449 | 0.06596 | 0.06016 | 0.06154 | 0.06168 | 0.05038 | 0.05412 |
| A3→Z_FALL | 0.06081 | 0.06138 | 0.06133 | 0.05308 | 0.05937 | 0.04818 | 0.05570 | 0.04407 |
| A3→Z_RISE | 0.07915 | 0.07818 | 0.06949 | 0.06339 | 0.06477 | 0.06489 | 0.05370 | 0.05795 |
| A4→Z_FALL | 0.05201 | 0.05152 | 0.05341 | 0.04633 | 0.05137 | 0.04303 | 0.04792 | 0.03822 |
| A4→Z_RISE | 0.07553 | 0.07340 | 0.06809 | 0.06214 | 0.06401 | 0.06420 | 0.05597 | 0.05770 |
| A5→Z_FALL | 0.05643 | 0.05706 | 0.05803 | 0.05071 | 0.05621 | 0.04663 | 0.05380 | 0.04200 |
| A5→Z_RISE | 0.07964 | 0.07867 | 0.07216 | 0.06627 | 0.06805 | 0.06834 | 0.06042 | 0.06212 |
| A6→Z_FALL | 0.06185 | 0.06164 | 0.06337 | 0.05577 | 0.06151 | 0.05078 | 0.06029 | 0.04618 |
| A6→Z_RISE | 0.08359 | 0.08139 | 0.07577 | 0.07002 | 0.07136 | 0.07206 | 0.06418 | 0.06587 |

| | | | | | | | | |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| Description | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
| A1→Z_FALL | 0.05301 | 0.04329 | 0.03480 | 0.04936 | 0.04027 | 0.03431 | 0.04992 | 0.04005 |
| A1→Z_RISE | 0.06673 | 0.04541 | 0.04661 | 0.08750 | 0.04289 | 0.04484 | 0.06586 | 0.04234 |
| A2→Z_FALL | 0.05787 | 0.04757 | 0.03994 | 0.05208 | 0.04716 | 0.03922 | 0.05362 | 0.04698 |
| A2→Z_RISE | 0.07203 | 0.05112 | 0.05308 | 0.09229 | 0.04876 | 0.05062 | 0.07054 | 0.04821 |
| A3→Z_FALL | 0.06174 | 0.05568 | 0.04346 | 0.05437 | 0.05216 | 0.04270 | 0.05749 | 0.05200 |
| A3→Z_RISE | 0.07494 | 0.05411 | 0.05587 | 0.09509 | 0.05146 | 0.05328 | 0.07413 | 0.05095 |
| A4→Z_FALL | 0.05717 | 0.04711 | 0.03804 | 0.05276 | 0.04395 | 0.03725 | 0.05368 | 0.04344 |
| A4→Z_RISE | 0.07928 | 0.05496 | 0.05573 | 0.10082 | 0.05220 | 0.05349 | 0.07896 | 0.05144 |
| A5→Z_FALL | 0.06105 | 0.05105 | 0.04299 | 0.05540 | 0.05103 | 0.04233 | 0.05755 | 0.05059 |
| A5→Z_RISE | 0.08326 | 0.06082 | 0.06243 | 0.10516 | 0.05824 | 0.05944 | 0.08356 | 0.05742 |
| A6→Z_FALL | 0.06577 | 0.05966 | 0.04680 | 0.05816 | 0.05620 | 0.04600 | 0.06125 | 0.05586 |

| | | | | | | | | |
|-----------|---------|---------|---------|---------|---------|---------|---------|---------|
| A6→Z_RISE | 0.08697 | 0.06385 | 0.06520 | 0.10845 | 0.06101 | 0.06217 | 0.08668 | 0.06024 |
|-----------|---------|---------|---------|---------|---------|---------|---------|---------|

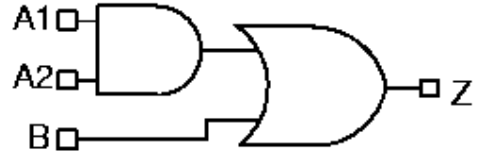
| Description | V16RD | V16RQ |
|-------------|---------|---------|
| A1→Z_FALL | 0.03320 | 0.04610 |
| A1→Z_RISE | 0.04395 | 0.08206 |
| A2→Z_FALL | 0.03805 | 0.04944 |
| A2→Z_RISE | 0.04970 | 0.08820 |
| A3→Z_FALL | 0.04140 | 0.05198 |
| A3→Z_RISE | 0.05243 | 0.09128 |
| A4→Z_FALL | 0.03631 | 0.04986 |
| A4→Z_RISE | 0.05297 | 0.09721 |
| A5→Z_FALL | 0.04127 | 0.05323 |
| A5→Z_RISE | 0.05884 | 0.10325 |
| A6→Z_FALL | 0.04496 | 0.05582 |
| A6→Z_RISE | 0.06167 | 0.10631 |

AO21HS

Cell Description

2-1 AO with Simple Gates

$$Z = ((A1 \& A2) | B)$$



Function Table

| A1 | A2 | B | Z |
|----|----|---|---|
| 0 | X | 0 | 0 |
| 0 | X | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| AO21HSV0 | 1.80 | 1.40 |
| AO21HSV1 | 1.80 | 1.40 |
| AO21HSV2 | 1.80 | 1.60 |
| AO21HSV4 | 1.80 | 1.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00131 | 0.00147 | 0.00176 | 0.00293 |
| A2 | 0.00138 | 0.00154 | 0.00184 | 0.00309 |
| B | 0.00110 | 0.00126 | 0.00154 | 0.00259 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00110 | 0.00109 | 0.00112 | 0.00140 |
| A2 | 0.00098 | 0.00098 | 0.00099 | 0.00138 |
| B | 0.00113 | 0.00118 | 0.00114 | 0.00153 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00016981 | 0.00018008 | 0.00020546 | 0.00039609 |

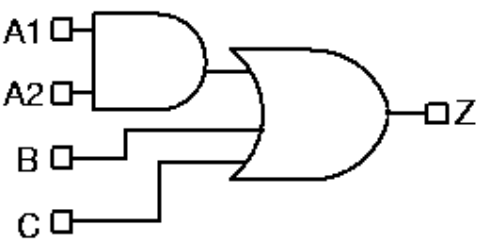
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.06088 | 0.06373 | 0.06828 | 0.06802 |
| A1→Z_RISE | 0.05242 | 0.05391 | 0.05724 | 0.05295 |
| A2→Z_FALL | 0.06519 | 0.06825 | 0.07293 | 0.07338 |
| A2→Z_RISE | 0.05382 | 0.05550 | 0.05876 | 0.05566 |
| B→Z_FALL | 0.05177 | 0.05493 | 0.05822 | 0.05772 |
| B→Z_RISE | 0.03254 | 0.03323 | 0.03423 | 0.03155 |

AO211HS

Cell Description

2-1-1 AO
 $Z=((A1\&A2)\|B)C$



Function Table

| A1 | A2 | B | C | Z |
|----|----|---|---|---|
| 0 | X | 0 | 0 | 0 |
| 0 | X | 0 | 1 | 1 |
| 0 | X | 1 | X | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | X | 1 |
| 1 | 1 | X | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| AO211HSV0 | 1.80 | 1.80 |
| AO211HSV1 | 1.80 | 1.80 |
| AO211HSV2 | 1.80 | 1.80 |
| AO211HSV4 | 1.80 | 2.00 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00156 | 0.00177 | 0.00198 | 0.00336 |
| A2 | 0.00168 | 0.00188 | 0.00209 | 0.00354 |
| B | 0.00133 | 0.00151 | 0.00173 | 0.00298 |
| C | 0.00121 | 0.00141 | 0.00162 | 0.00279 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00105 | 0.00108 | 0.00104 | 0.00142 |
| A2 | 0.00106 | 0.00105 | 0.00104 | 0.00145 |

| | | | | |
|---|---------|---------|---------|---------|
| B | 0.00105 | 0.00104 | 0.00105 | 0.00147 |
| C | 0.00106 | 0.00111 | 0.00108 | 0.00145 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00023008 | 0.00024281 | 0.00025750 | 0.00049343 |

Delay Table (ns)

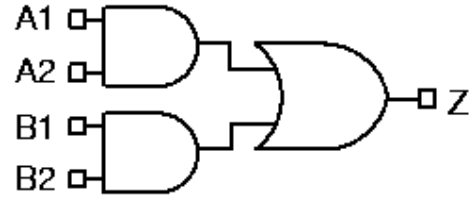
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.09509 | 0.10088 | 0.10546 | 0.10720 |
| A1→Z_RISE | 0.05834 | 0.06091 | 0.06224 | 0.05807 |
| A2→Z_FALL | 0.10434 | 0.10975 | 0.11427 | 0.11531 |
| A2→Z_RISE | 0.06152 | 0.06387 | 0.06535 | 0.06076 |
| B→Z_FALL | 0.08470 | 0.08883 | 0.09388 | 0.09615 |
| B→Z_RISE | 0.03681 | 0.03728 | 0.03778 | 0.03571 |
| C→Z_FALL | 0.07809 | 0.08356 | 0.08788 | 0.08849 |
| C→Z_RISE | 0.03538 | 0.03621 | 0.03663 | 0.03454 |

AO22HS

Cell Description

2-2 AO with Simple Gates

$$Z=((A1\&A2)|(B1\&B2))$$



Function Table

| A1 | A2 | B1 | B2 | Z |
|----|----|----|----|---|
| 0 | X | 0 | X | 0 |
| 0 | X | 1 | 0 | 0 |
| 0 | X | 1 | 1 | 1 |
| 1 | 0 | 0 | X | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | X | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| AO22HSV0 | 1.80 | 1.80 |
| AO22HSV1 | 1.80 | 1.80 |
| AO22HSV2 | 1.80 | 1.80 |
| AO22HSV4 | 1.80 | 2.00 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00154 | 0.00173 | 0.00199 | 0.00319 |
| A2 | 0.00164 | 0.00183 | 0.00209 | 0.00334 |
| B1 | 0.00118 | 0.00136 | 0.00163 | 0.00261 |
| B2 | 0.00131 | 0.00149 | 0.00176 | 0.00281 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00108 | 0.00108 | 0.00108 | 0.00144 |
| A2 | 0.00101 | 0.00101 | 0.00101 | 0.00134 |

| | | | | |
|----|---------|---------|---------|---------|
| B1 | 0.00109 | 0.00109 | 0.00108 | 0.00145 |
| B2 | 0.00106 | 0.00105 | 0.00109 | 0.00149 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00018495 | 0.00019828 | 0.00021288 | 0.00039802 |

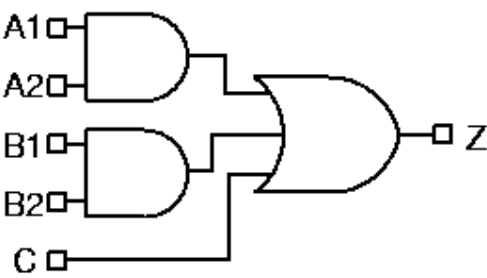
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.06741 | 0.06968 | 0.07376 | 0.07131 |
| A1→Z_RISE | 0.05911 | 0.06067 | 0.06402 | 0.05806 |
| A2→Z_FALL | 0.07186 | 0.07412 | 0.07812 | 0.07588 |
| A2→Z_RISE | 0.06154 | 0.06311 | 0.06644 | 0.06054 |
| B1→Z_FALL | 0.05455 | 0.05662 | 0.06068 | 0.05825 |
| B1→Z_RISE | 0.04767 | 0.04896 | 0.05207 | 0.04678 |
| B2→Z_FALL | 0.06053 | 0.06261 | 0.06709 | 0.06414 |
| B2→Z_RISE | 0.05123 | 0.05250 | 0.05595 | 0.05011 |

AO221HS

Cell Description

2-2-1 AO
 $Z=((A1\&A2)|(B1\&B2)|C)$



Function Table

| A1 | A2 | B1 | B2 | C | Z |
|----|----|----|----|---|---|
| 0 | X | 0 | X | 0 | 0 |
| 0 | X | 0 | X | 1 | 1 |
| 0 | X | 1 | 0 | 0 | 0 |
| 0 | X | 1 | 0 | 1 | 1 |
| 0 | X | 1 | 1 | X | 1 |
| 1 | 0 | 0 | X | 0 | 0 |
| 1 | 0 | 0 | X | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | X | 1 |
| 1 | 1 | X | X | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| AO221HSV0 | 1.80 | 2.00 |
| AO221HSV1 | 1.80 | 2.00 |
| AO221HSV2 | 1.80 | 2.00 |
| AO221HSV4 | 1.80 | 2.40 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00182 | 0.00199 | 0.00223 | 0.00371 |
| A2 | 0.00195 | 0.00211 | 0.00235 | 0.00390 |
| B1 | 0.00152 | 0.00169 | 0.00193 | 0.00327 |
| B2 | 0.00161 | 0.00178 | 0.00202 | 0.00344 |
| C | 0.00130 | 0.00147 | 0.00171 | 0.00291 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00109 | 0.00109 | 0.00109 | 0.00142 |
| A2 | 0.00112 | 0.00111 | 0.00109 | 0.00141 |
| B1 | 0.00107 | 0.00106 | 0.00106 | 0.00140 |
| B2 | 0.00102 | 0.00102 | 0.00101 | 0.00138 |
| C | 0.00108 | 0.00108 | 0.00107 | 0.00144 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00024430 | 0.00025668 | 0.00026666 | 0.00050665 |

Delay Table (ns)

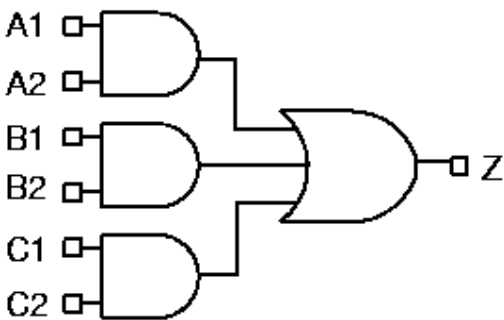
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.10558 | 0.10850 | 0.11360 | 0.11509 |
| A1→Z_RISE | 0.06444 | 0.06539 | 0.06817 | 0.06280 |
| A2→Z_FALL | 0.11507 | 0.11761 | 0.12201 | 0.12288 |
| A2→Z_RISE | 0.06781 | 0.06865 | 0.07102 | 0.06550 |
| B1→Z_FALL | 0.09567 | 0.09849 | 0.10358 | 0.10519 |
| B1→Z_RISE | 0.05804 | 0.05889 | 0.06139 | 0.05728 |
| B2→Z_FALL | 0.10244 | 0.10529 | 0.11024 | 0.11246 |
| B2→Z_RISE | 0.06016 | 0.06099 | 0.06346 | 0.05968 |
| C→Z_FALL | 0.07904 | 0.08172 | 0.08635 | 0.08664 |
| C→Z_RISE | 0.03718 | 0.03712 | 0.03819 | 0.03539 |

AO222HS

Cell Description

2-2-2 AO

$$Z=((A1\&A2)|(B1\&B2)|(C1\&C2))$$



Function Table

| A1 | A2 | B1 | B2 | C1 | C2 | Z |
|----|----|----|----|----|----|---|
| 0 | X | 0 | X | 0 | X | 0 |
| 0 | X | 0 | X | 1 | 0 | 0 |
| 0 | X | 0 | X | 1 | 1 | 1 |
| 0 | X | 1 | 0 | 0 | X | 0 |
| 0 | X | 1 | 0 | 1 | 0 | 0 |
| 0 | X | 1 | 0 | 1 | 1 | 1 |
| 0 | X | 1 | 1 | X | X | 1 |
| 1 | 0 | 0 | X | 0 | X | 0 |
| 1 | 0 | 0 | X | 1 | 0 | 0 |
| 1 | 0 | 0 | X | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | X | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | X | X | 1 |
| 1 | 1 | X | X | X | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| AO222HSV0 | 1.80 | 2.40 |
| AO222HSV1 | 1.80 | 2.40 |
| AO222HSV2 | 1.80 | 2.40 |
| AO222HSV4 | 1.80 | 2.60 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00209 | 0.00223 | 0.00250 | 0.00404 |
| A2 | 0.00216 | 0.00232 | 0.00259 | 0.00416 |

| | | | | |
|----|---------|---------|---------|---------|
| B1 | 0.00182 | 0.00193 | 0.00220 | 0.00358 |
| B2 | 0.00190 | 0.00207 | 0.00234 | 0.00374 |
| C1 | 0.00147 | 0.00162 | 0.00189 | 0.00309 |
| C2 | 0.00155 | 0.00170 | 0.00197 | 0.00323 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00107 | 0.00109 | 0.00108 | 0.00145 |
| A2 | 0.00103 | 0.00101 | 0.00101 | 0.00138 |
| B1 | 0.00123 | 0.00111 | 0.00111 | 0.00154 |
| B2 | 0.00109 | 0.00123 | 0.00123 | 0.00141 |
| C1 | 0.00108 | 0.00109 | 0.00108 | 0.00140 |
| C2 | 0.00105 | 0.00109 | 0.00109 | 0.00134 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00024079 | 0.00024757 | 0.00026273 | 0.00047828 |

Delay Table (ns)

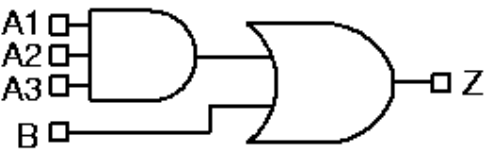
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.11867 | 0.11945 | 0.12433 | 0.12340 |
| A1→Z_RISE | 0.07607 | 0.07492 | 0.07820 | 0.07221 |
| A2→Z_FALL | 0.12386 | 0.12501 | 0.12986 | 0.12854 |
| A2→Z_RISE | 0.07729 | 0.07705 | 0.08032 | 0.07355 |
| B1→Z_FALL | 0.11025 | 0.10932 | 0.11400 | 0.11271 |
| B1→Z_RISE | 0.06903 | 0.06750 | 0.07031 | 0.06363 |
| B2→Z_FALL | 0.11562 | 0.12003 | 0.12460 | 0.11955 |
| B2→Z_RISE | 0.07077 | 0.07216 | 0.07499 | 0.06611 |
| C1→Z_FALL | 0.08737 | 0.09009 | 0.09472 | 0.09216 |
| C1→Z_RISE | 0.05762 | 0.05873 | 0.06153 | 0.05479 |
| C2→Z_FALL | 0.09355 | 0.09542 | 0.09999 | 0.09814 |
| C2→Z_RISE | 0.05955 | 0.06039 | 0.06319 | 0.05667 |

AO31HS

Cell Description

3-1 AO

$Z=((A1\&A2\&A3)|B)$



Function Table

| A1 | A2 | A3 | B | Z |
|----|----|----|---|---|
| 0 | X | X | 0 | 0 |
| 0 | X | X | 1 | 1 |
| 1 | 0 | X | 0 | 0 |
| 1 | 0 | X | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| AO31HSV0 | 1.80 | 1.60 |
| AO31HSV1 | 1.80 | 1.60 |
| AO31HSV2 | 1.80 | 1.60 |
| AO31HSV4 | 1.80 | 1.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00143 | 0.00158 | 0.00185 | 0.00299 |
| A2 | 0.00153 | 0.00168 | 0.00193 | 0.00315 |
| A3 | 0.00164 | 0.00179 | 0.00206 | 0.00332 |
| B | 0.00118 | 0.00133 | 0.00159 | 0.00259 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00108 | 0.00106 | 0.00105 | 0.00141 |
| A2 | 0.00106 | 0.00103 | 0.00103 | 0.00138 |

| | | | | |
|----|---------|---------|---------|---------|
| A3 | 0.00106 | 0.00106 | 0.00107 | 0.00139 |
| B | 0.00112 | 0.00104 | 0.00112 | 0.00142 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00016840 | 0.00018080 | 0.00019506 | 0.00035628 |

Delay Table (ns)

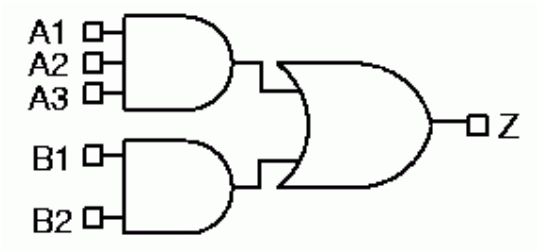
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.06595 | 0.06755 | 0.07151 | 0.06919 |
| A1→Z_RISE | 0.07248 | 0.07425 | 0.08083 | 0.07183 |
| A2→Z_FALL | 0.07166 | 0.07300 | 0.07665 | 0.07506 |
| A2→Z_RISE | 0.07741 | 0.07871 | 0.08466 | 0.07657 |
| A3→Z_FALL | 0.07693 | 0.07844 | 0.08210 | 0.08032 |
| A3→Z_RISE | 0.08064 | 0.08228 | 0.08851 | 0.07953 |
| B→Z_FALL | 0.05256 | 0.05326 | 0.05698 | 0.05478 |
| B→Z_RISE | 0.03443 | 0.03394 | 0.03614 | 0.03243 |

AO32HS

Cell Description

3-2 AO

$$Z=((A1\&A2\&A3)|(B1\&B2))$$



Function Table

| A1 | A2 | A3 | B1 | B2 | Z |
|----|----|----|----|----|---|
| 0 | X | X | 0 | X | 0 |
| 0 | X | X | 1 | 0 | 0 |
| 0 | X | X | 1 | 1 | 1 |
| 1 | 0 | X | 0 | X | 0 |
| 1 | 0 | X | 1 | 0 | 0 |
| 1 | 0 | X | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | X | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | X | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| AO32HSV0 | 1.80 | 1.80 |
| AO32HSV1 | 1.80 | 1.80 |
| AO32HSV2 | 1.80 | 2.00 |
| AO32HSV4 | 1.80 | 2.20 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00162 | 0.00178 | 0.00208 | 0.00337 |
| A2 | 0.00171 | 0.00187 | 0.00217 | 0.00353 |
| A3 | 0.00184 | 0.00199 | 0.00227 | 0.00369 |
| B1 | 0.00124 | 0.00141 | 0.00168 | 0.00276 |
| B2 | 0.00132 | 0.00149 | 0.00176 | 0.00290 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00105 | 0.00103 | 0.00103 | 0.00142 |
| A2 | 0.00104 | 0.00102 | 0.00103 | 0.00139 |
| A3 | 0.00107 | 0.00104 | 0.00103 | 0.00141 |
| B1 | 0.00113 | 0.00112 | 0.00110 | 0.00146 |
| B2 | 0.00103 | 0.00102 | 0.00103 | 0.00138 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00017625 | 0.00018880 | 0.00021891 | 0.00039593 |

Delay Table (ns)

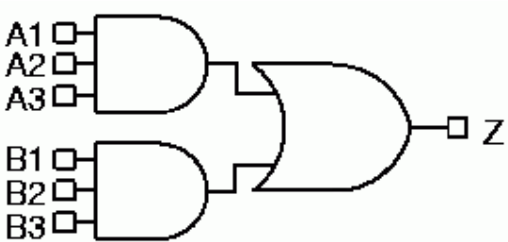
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.07071 | 0.07175 | 0.07625 | 0.07409 |
| A1→Z_RISE | 0.08138 | 0.08285 | 0.09065 | 0.07953 |
| A2→Z_FALL | 0.07567 | 0.07641 | 0.08087 | 0.07927 |
| A2→Z_RISE | 0.08559 | 0.08707 | 0.09511 | 0.08406 |
| A3→Z_FALL | 0.08106 | 0.08185 | 0.08562 | 0.08388 |
| A3→Z_RISE | 0.08971 | 0.09090 | 0.09813 | 0.08677 |
| B1→Z_FALL | 0.05515 | 0.05635 | 0.05966 | 0.05787 |
| B1→Z_RISE | 0.05077 | 0.05176 | 0.05593 | 0.04981 |
| B2→Z_FALL | 0.05873 | 0.05991 | 0.06321 | 0.06181 |
| B2→Z_RISE | 0.05253 | 0.05355 | 0.05788 | 0.05202 |

AO33HS

Cell Description

3-3 AO

$$Z=((A1\&A2\&A3)|(B1\&B2\&B3))$$



Function Table

| A1 | A2 | A3 | B1 | B2 | B3 | Z |
|----|----|----|----|----|----|---|
| 0 | X | X | 0 | X | X | 0 |
| 0 | X | X | 1 | 0 | X | 0 |
| 0 | X | X | 1 | 1 | 0 | 0 |
| 0 | X | X | 1 | 1 | 1 | 1 |
| 1 | 0 | X | 0 | X | X | 0 |
| 1 | 0 | X | 1 | 0 | X | 0 |
| 1 | 0 | X | 1 | 1 | 0 | 0 |
| 1 | 0 | X | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | X | X | 0 |
| 1 | 1 | 0 | 1 | 0 | X | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | X | X | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| AO33HSV0 | 1.80 | 2.20 |
| AO33HSV1 | 1.80 | 2.20 |
| AO33HSV2 | 1.80 | 2.20 |
| AO33HSV4 | 1.80 | 2.60 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00184 | 0.00199 | 0.00225 | 0.00363 |
| A2 | 0.00195 | 0.00210 | 0.00234 | 0.00380 |
| A3 | 0.00207 | 0.00219 | 0.00245 | 0.00395 |
| B1 | 0.00139 | 0.00153 | 0.00179 | 0.00296 |

| | | | | |
|----|---------|---------|---------|---------|
| B2 | 0.00149 | 0.00163 | 0.00189 | 0.00313 |
| B3 | 0.00156 | 0.00171 | 0.00197 | 0.00327 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00105 | 0.00101 | 0.00103 | 0.00136 |
| A2 | 0.00107 | 0.00105 | 0.00104 | 0.00142 |
| A3 | 0.00106 | 0.00105 | 0.00103 | 0.00141 |
| B1 | 0.00107 | 0.00111 | 0.00107 | 0.00143 |
| B2 | 0.00112 | 0.00109 | 0.00109 | 0.00144 |
| B3 | 0.00101 | 0.00100 | 0.00099 | 0.00139 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00021898 | 0.00023598 | 0.00026976 | 0.00046329 |

Delay Table (ns)

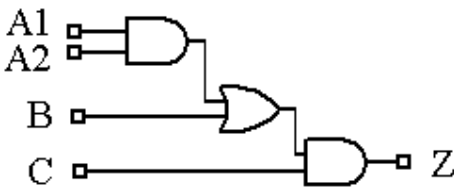
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.07604 | 0.07651 | 0.07920 | 0.07675 |
| A1→Z_RISE | 0.09176 | 0.09254 | 0.09875 | 0.08637 |
| A2→Z_FALL | 0.08109 | 0.08166 | 0.08376 | 0.08177 |
| A2→Z_RISE | 0.09700 | 0.09808 | 0.10378 | 0.09133 |
| A3→Z_FALL | 0.08581 | 0.08585 | 0.08885 | 0.08593 |
| A3→Z_RISE | 0.10023 | 0.10067 | 0.10706 | 0.09371 |
| B1→Z_FALL | 0.06028 | 0.06126 | 0.06390 | 0.06206 |
| B1→Z_RISE | 0.07136 | 0.07279 | 0.07835 | 0.06970 |
| B2→Z_FALL | 0.06525 | 0.06555 | 0.06849 | 0.06674 |
| B2→Z_RISE | 0.07691 | 0.07766 | 0.08354 | 0.07453 |
| B3→Z_FALL | 0.06770 | 0.06817 | 0.07099 | 0.07008 |
| B3→Z_RISE | 0.07765 | 0.07868 | 0.08450 | 0.07648 |

AOA211HS

Cell Description

2-1-1 AOA

$$Z = (((A1 \& A2) \mid B) \& C)$$



Function Table

| A1 | A2 | B | C | Z |
|----|----|---|---|---|
| 0 | X | 0 | X | 0 |
| 0 | X | 1 | 0 | 0 |
| 0 | X | 1 | 1 | 1 |
| 1 | 0 | 0 | X | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | X | 0 | 0 |
| 1 | 1 | X | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| AOA211HSV0 | 1.80 | 1.80 |
| AOA211HSV1 | 1.80 | 1.80 |
| AOA211HSV2 | 1.80 | 1.80 |
| AOA211HSV4 | 1.80 | 2.00 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| B | 0.00124 | 0.00152 | 0.00166 | 0.00277 |
| C | 0.00111 | 0.00138 | 0.00153 | 0.00253 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00094 | 0.00095 | 0.00095 | 0.00133 |
| A2 | 0.00096 | 0.00098 | 0.00099 | 0.00144 |
| B | 0.00098 | 0.00098 | 0.00098 | 0.00138 |

| | | | | |
|---|---------|---------|---------|---------|
| C | 0.00096 | 0.00096 | 0.00097 | 0.00137 |
|---|---------|---------|---------|---------|

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00014982 | 0.00018723 | 0.00020490 | 0.00038169 |

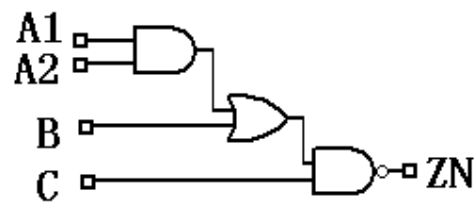
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.08628 | 0.09129 | 0.09023 | 0.08348 |
| A1→Z_RISE | 0.08086 | 0.08612 | 0.08946 | 0.07926 |
| A2→Z_FALL | 0.09246 | 0.09735 | 0.09615 | 0.08957 |
| A2→Z_RISE | 0.08445 | 0.08970 | 0.09322 | 0.08285 |
| B→Z_FALL | 0.07372 | 0.07799 | 0.07668 | 0.07074 |
| B→Z_RISE | 0.05560 | 0.05891 | 0.06060 | 0.05398 |
| C→Z_FALL | 0.04330 | 0.04515 | 0.04450 | 0.03966 |
| C→Z_RISE | 0.05293 | 0.05656 | 0.05852 | 0.05207 |

AOAI211HS

Cell Description

2-1-1 AOAI
 $ZN = \neg(((A1 \& A2) \mid B) \& C)$



Function Table

| A1 | A2 | B | C | ZN |
|----|----|---|---|----|
| 0 | X | 0 | X | 1 |
| 0 | X | 1 | 0 | 1 |
| 0 | X | 1 | 1 | 0 |
| 1 | 0 | 0 | X | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | X | 0 | 1 |
| 1 | 1 | X | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| AOAI211HSV0 | 1.80 | 1.40 |
| AOAI211HSV1 | 1.80 | 1.40 |
| AOAI211HSV2 | 1.80 | 1.40 |
| AOAI211HSV4 | 1.80 | 2.40 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00083 | 0.00121 | 0.00144 | 0.00261 |
| A2 | 0.00091 | 0.00134 | 0.00160 | 0.00295 |
| B | 0.00062 | 0.00089 | 0.00105 | 0.00192 |
| C | 0.00043 | 0.00062 | 0.00072 | 0.00125 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00101 | 0.00133 | 0.00142 | 0.00264 |

| | | | | |
|----|---------|---------|---------|---------|
| A2 | 0.00095 | 0.00128 | 0.00144 | 0.00282 |
| B | 0.00097 | 0.00129 | 0.00144 | 0.00259 |
| C | 0.00095 | 0.00128 | 0.00144 | 0.00284 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00011480 | 0.00014365 | 0.00015608 | 0.00035050 |

Delay Table (ns)

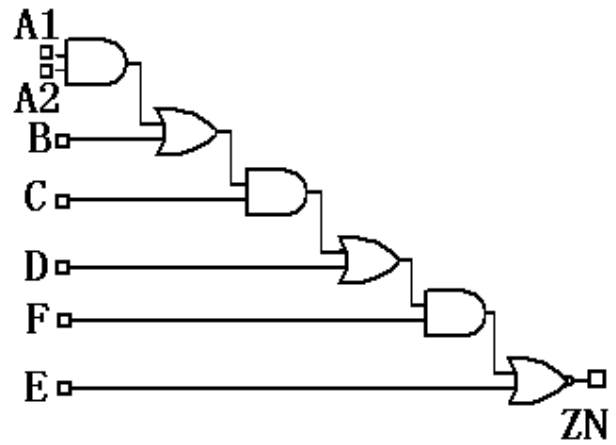
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.04644 | 0.03906 | 0.03749 | 0.03208 |
| A1→ZN_RISE | 0.04845 | 0.04347 | 0.04280 | 0.03762 |
| A2→ZN_FALL | 0.04843 | 0.04119 | 0.03988 | 0.03436 |
| A2→ZN_RISE | 0.05131 | 0.04671 | 0.04615 | 0.04142 |
| B→ZN_FALL | 0.02769 | 0.02330 | 0.02247 | 0.01932 |
| B→ZN_RISE | 0.03768 | 0.03295 | 0.03228 | 0.02842 |
| C→ZN_FALL | 0.02331 | 0.01934 | 0.01825 | 0.01504 |
| C→ZN_RISE | 0.01753 | 0.01507 | 0.01434 | 0.01215 |

AOAOAOI21111HS

Cell Description

2-1-1-1-1-1 AOAOAOI

$ZN = (!((((((A1 \& A2) | B) \& C) | D) \& F) | E))$



Function Table

| A1 | A2 | B | C | D | F | E | ZN |
|----|----|---|---|---|---|---|----|
| 0 | X | 0 | X | 0 | X | 0 | 1 |
| 0 | X | 0 | X | 0 | X | 1 | 0 |
| 0 | X | 0 | X | 1 | 0 | 0 | 1 |
| 0 | X | 0 | X | 1 | 0 | 1 | 0 |
| 0 | X | 0 | X | 1 | 1 | X | 0 |
| 0 | X | 1 | 0 | 0 | X | 0 | 1 |
| 0 | X | 1 | 0 | 0 | X | 1 | 0 |
| 0 | X | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | X | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | X | 1 | 0 | 1 | 1 | X | 0 |
| 0 | X | 1 | 1 | X | 0 | 0 | 1 |
| 0 | X | 1 | 1 | X | 0 | 1 | 0 |
| 0 | X | 1 | 1 | X | 1 | X | 0 |
| 1 | 0 | 0 | X | 0 | X | 0 | 1 |
| 1 | 0 | 0 | X | 0 | X | 1 | 0 |
| 1 | 0 | 0 | X | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | X | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | X | 1 | 1 | X | 0 |
| 1 | 0 | 1 | 0 | 0 | X | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | X | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | X | 0 |
| 1 | 0 | 1 | 1 | X | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | X | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | X | 1 | X | 0 |
| 1 | 1 | X | 0 | 0 | X | 0 | 1 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 1 | X | 0 | 0 | X | 1 | 0 |
| 1 | 1 | X | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | X | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | X | 0 | 1 | 1 | X | 0 |
| 1 | 1 | X | 1 | X | 0 | 0 | 1 |
| 1 | 1 | X | 1 | X | 0 | 1 | 0 |
| 1 | 1 | X | 1 | X | 1 | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------------|------------|-----------|
| AOAOAOI211111HSV0 | 1.80 | 2.60 |
| AOAOAOI211111HSV1 | 1.80 | 2.60 |
| AOAOAOI211111HSV2 | 1.80 | 2.60 |
| AOAOAOI211111HSV4 | 1.80 | 4.60 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00151 | 0.00218 | 0.00254 | 0.00490 |
| A2 | 0.00158 | 0.00230 | 0.00269 | 0.00530 |
| B | 0.00133 | 0.00191 | 0.00223 | 0.00427 |
| C | 0.00114 | 0.00164 | 0.00191 | 0.00362 |
| D | 0.00093 | 0.00132 | 0.00155 | 0.00291 |
| E | 0.00047 | 0.00065 | 0.00075 | 0.00139 |
| F | 0.00071 | 0.00102 | 0.00118 | 0.00224 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00101 | 0.00130 | 0.00145 | 0.00263 |
| A2 | 0.00090 | 0.00124 | 0.00140 | 0.00265 |
| B | 0.00096 | 0.00127 | 0.00143 | 0.00265 |
| C | 0.00097 | 0.00130 | 0.00146 | 0.00263 |
| D | 0.00096 | 0.00126 | 0.00142 | 0.00261 |
| E | 0.00098 | 0.00131 | 0.00147 | 0.00272 |
| F | 0.00101 | 0.00133 | 0.00150 | 0.00266 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00016026 | 0.00026326 | 0.00031038 | 0.00068049 |

Delay Table (ns)

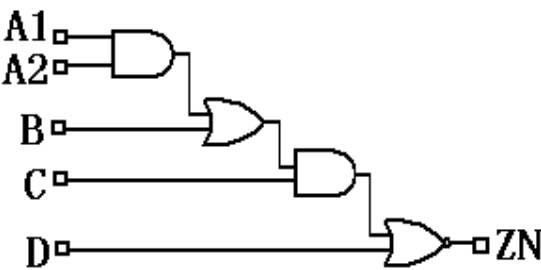
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.08552 | 0.06985 | 0.06680 | 0.05944 |
| A1→ZN_RISE | 0.14492 | 0.13354 | 0.13147 | 0.12229 |
| A2→ZN_FALL | 0.08629 | 0.07185 | 0.06889 | 0.06238 |

| | | | | |
|------------|---------|---------|---------|---------|
| A2→ZN_RISE | 0.15259 | 0.14046 | 0.13882 | 0.13222 |
| B→ZN_FALL | 0.06002 | 0.04977 | 0.04766 | 0.04213 |
| B→ZN_RISE | 0.13447 | 0.12262 | 0.12099 | 0.11237 |
| C→ZN_FALL | 0.05599 | 0.04609 | 0.04377 | 0.03800 |
| C→ZN_RISE | 0.08691 | 0.07820 | 0.07647 | 0.06974 |
| D→ZN_FALL | 0.03467 | 0.02880 | 0.02757 | 0.02455 |
| D→ZN_RISE | 0.08503 | 0.07603 | 0.07459 | 0.06774 |
| E→ZN_FALL | 0.01391 | 0.01159 | 0.01100 | 0.00962 |
| E→ZN_RISE | 0.03788 | 0.03192 | 0.03068 | 0.02665 |
| F→ZN_FALL | 0.02943 | 0.02412 | 0.02255 | 0.01973 |
| F→ZN_RISE | 0.04139 | 0.03607 | 0.03459 | 0.03093 |

AOAOI2111HS

Cell Description

2-1-1-1 AOAOI
 $ZN = (!(((A1 \& A2) | B) \& C) | D))$



Function Table

| A1 | A2 | B | C | D | ZN |
|----|----|---|---|---|----|
| 0 | X | 0 | X | 0 | 1 |
| 0 | X | 0 | X | 1 | 0 |
| 0 | X | 1 | 0 | 0 | 1 |
| 0 | X | 1 | 0 | 1 | 0 |
| 0 | X | 1 | 1 | X | 0 |
| 1 | 0 | 0 | X | 0 | 1 |
| 1 | 0 | 0 | X | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | X | 0 |
| 1 | 1 | X | 0 | 0 | 1 |
| 1 | 1 | X | 0 | 1 | 0 |
| 1 | 1 | X | 1 | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|---------------|------------|-----------|
| AOAOI2111HSV0 | 1.80 | 1.80 |
| AOAOI2111HSV1 | 1.80 | 1.80 |
| AOAOI2111HSV2 | 1.80 | 1.80 |
| AOAOI2111HSV4 | 1.80 | 3.20 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00110 | 0.00159 | 0.00184 | 0.00340 |
| A2 | 0.00118 | 0.00173 | 0.00201 | 0.00386 |
| B | 0.00093 | 0.00131 | 0.00152 | 0.00281 |
| C | 0.00076 | 0.00106 | 0.00122 | 0.00212 |

| | | | | |
|---|---------|---------|---------|---------|
| D | 0.00054 | 0.00073 | 0.00083 | 0.00137 |
|---|---------|---------|---------|---------|

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00093 | 0.00124 | 0.00141 | 0.00262 |
| A2 | 0.00086 | 0.00120 | 0.00140 | 0.00267 |
| B | 0.00091 | 0.00122 | 0.00141 | 0.00261 |
| C | 0.00092 | 0.00124 | 0.00141 | 0.00264 |
| D | 0.00097 | 0.00127 | 0.00146 | 0.00272 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00013103 | 0.00020308 | 0.00025857 | 0.00055865 |

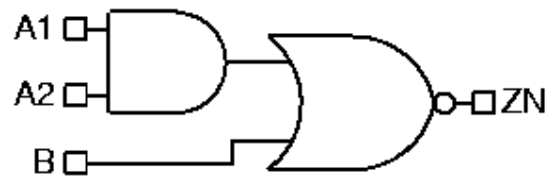
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.05247 | 0.04413 | 0.04076 | 0.03603 |
| A1→ZN_RISE | 0.08543 | 0.07729 | 0.07490 | 0.06707 |
| A2→ZN_FALL | 0.05452 | 0.04636 | 0.04309 | 0.03933 |
| A2→ZN_RISE | 0.09112 | 0.08343 | 0.08136 | 0.07574 |
| B→ZN_FALL | 0.03464 | 0.02930 | 0.02747 | 0.02418 |
| B→ZN_RISE | 0.07624 | 0.06797 | 0.06605 | 0.05911 |
| C→ZN_FALL | 0.02998 | 0.02480 | 0.02287 | 0.01906 |
| C→ZN_RISE | 0.04417 | 0.03819 | 0.03649 | 0.03034 |
| D→ZN_FALL | 0.01490 | 0.01236 | 0.01158 | 0.00970 |
| D→ZN_RISE | 0.03965 | 0.03326 | 0.03156 | 0.02563 |

AOI21HS

Cell Description

2-1 AOI
 $ZN = \neg((A1 \& A2) | B)$



Function Table

| A1 | A2 | B | ZN |
|----|----|---|----|
| 0 | X | 0 | 1 |
| 0 | X | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| AOI21HSV0 | 1.80 | 1.00 |
| AOI21HSV1 | 1.80 | 1.00 |
| AOI21HSV2 | 1.80 | 1.00 |
| AOI21HSV4 | 1.80 | 1.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00065 | 0.00086 | 0.00111 | 0.00206 |
| A2 | 0.00074 | 0.00098 | 0.00129 | 0.00248 |
| B | 0.00043 | 0.00054 | 0.00069 | 0.00124 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00104 | 0.00121 | 0.00151 | 0.00275 |
| A2 | 0.00099 | 0.00119 | 0.00152 | 0.00313 |
| B | 0.00099 | 0.00119 | 0.00152 | 0.00277 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00010375 | 0.00014026 | 0.00023351 | 0.00052808 |

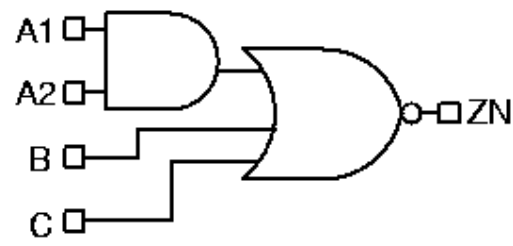
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.02694 | 0.02440 | 0.02090 | 0.01799 |
| A1→ZN_RISE | 0.03487 | 0.03231 | 0.02973 | 0.02666 |
| A2→ZN_FALL | 0.02905 | 0.02677 | 0.02343 | 0.02088 |
| A2→ZN_RISE | 0.03880 | 0.03640 | 0.03423 | 0.03148 |
| B→ZN_FALL | 0.01373 | 0.01231 | 0.01081 | 0.00946 |
| B→ZN_RISE | 0.02658 | 0.02359 | 0.02143 | 0.01844 |

AOI211HS

Cell Description

2-1-1 AOI
 $ZN = \neg((A1 \& A2) | B | C)$



Function Table

| A1 | A2 | B | C | ZN |
|----|----|---|---|----|
| 0 | X | 0 | 0 | 1 |
| 0 | X | 0 | 1 | 0 |
| 0 | X | 1 | X | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | X | 0 |
| 1 | 1 | X | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| AOI211HSV0 | 1.80 | 1.20 |
| AOI211HSV1 | 1.80 | 1.20 |
| AOI211HSV2 | 1.80 | 1.40 |
| AOI211HSV4 | 1.80 | 2.40 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00089 | 0.00113 | 0.00155 | 0.00397 |
| A2 | 0.00097 | 0.00125 | 0.00173 | 0.00406 |
| B | 0.00066 | 0.00085 | 0.00115 | 0.00376 |
| C | 0.00054 | 0.00067 | 0.00089 | 0.00366 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00099 | 0.00121 | 0.00150 | 0.00103 |
| A2 | 0.00095 | 0.00115 | 0.00153 | 0.00101 |

| | | | | |
|---|---------|---------|---------|---------|
| B | 0.00099 | 0.00123 | 0.00154 | 0.00104 |
| C | 0.00102 | 0.00123 | 0.00153 | 0.00106 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00016061 | 0.00024366 | 0.00037212 | 0.00047844 |

Delay Table (ns)

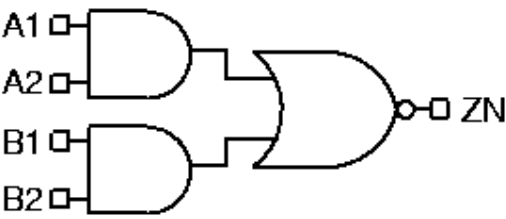
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.03108 | 0.02700 | 0.02424 | 0.09351 |
| A1→ZN_RISE | 0.05996 | 0.05477 | 0.05321 | 0.13869 |
| A2→ZN_FALL | 0.03325 | 0.02923 | 0.02681 | 0.09597 |
| A2→ZN_RISE | 0.06610 | 0.06141 | 0.06026 | 0.14695 |
| B→ZN_FALL | 0.01653 | 0.01476 | 0.01357 | 0.06491 |
| B→ZN_RISE | 0.05126 | 0.04705 | 0.04531 | 0.12785 |
| C→ZN_FALL | 0.01549 | 0.01358 | 0.01237 | 0.06345 |
| C→ZN_RISE | 0.04485 | 0.03963 | 0.03691 | 0.12182 |

AOI22HS

Cell Description

2-2 AOI

$$ZN = \neg((A1 \& A2) | (B1 \& B2))$$



Function Table

| A1 | A2 | B1 | B2 | ZN |
|----|----|----|----|----|
| 0 | X | 0 | X | 1 |
| 0 | X | 1 | 0 | 1 |
| 0 | X | 1 | 1 | 0 |
| 1 | 0 | 0 | X | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | X | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| AOI22HSV0 | 1.80 | 1.40 |
| AOI22HSV1 | 1.80 | 1.40 |
| AOI22HSV2 | 1.80 | 1.40 |
| AOI22HSV4 | 1.80 | 2.40 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00089 | 0.00117 | 0.00152 | 0.00289 |
| A2 | 0.00097 | 0.00129 | 0.00170 | 0.00327 |
| B1 | 0.00054 | 0.00069 | 0.00088 | 0.00166 |
| B2 | 0.00065 | 0.00084 | 0.00107 | 0.00207 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00103 | 0.00122 | 0.00150 | 0.00279 |
| A2 | 0.00097 | 0.00116 | 0.00150 | 0.00308 |

| | | | | |
|----|---------|---------|---------|---------|
| B1 | 0.00094 | 0.00118 | 0.00145 | 0.00276 |
| B2 | 0.00097 | 0.00119 | 0.00146 | 0.00300 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00011734 | 0.00017597 | 0.00026385 | 0.00056961 |

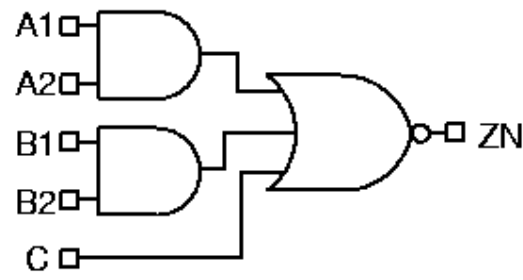
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.03209 | 0.02882 | 0.02556 | 0.02277 |
| A1→ZN_RISE | 0.04144 | 0.03858 | 0.03619 | 0.03295 |
| A2→ZN_FALL | 0.03391 | 0.03082 | 0.02781 | 0.02539 |
| A2→ZN_RISE | 0.04499 | 0.04228 | 0.04006 | 0.03735 |
| B1→ZN_FALL | 0.02392 | 0.02086 | 0.01826 | 0.01609 |
| B1→ZN_RISE | 0.02971 | 0.02664 | 0.02439 | 0.02192 |
| B2→ZN_FALL | 0.02687 | 0.02400 | 0.02101 | 0.01898 |
| B2→ZN_RISE | 0.03425 | 0.03143 | 0.02890 | 0.02662 |

AOI221HS

Cell Description

2-2-1 AOI
 $ZN = \neg((A1 \& A2) | (B1 \& B2) | C)$



Function Table

| A1 | A2 | B1 | B2 | C | ZN |
|----|----|----|----|---|----|
| 0 | X | 0 | X | 0 | 1 |
| 0 | X | 0 | X | 1 | 0 |
| 0 | X | 1 | 0 | 0 | 1 |
| 0 | X | 1 | 0 | 1 | 0 |
| 0 | X | 1 | 1 | X | 0 |
| 1 | 0 | 0 | X | 0 | 1 |
| 1 | 0 | 0 | X | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | X | 0 |
| 1 | 1 | X | X | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| AOI221HSV0 | 1.80 | 1.80 |
| AOI221HSV1 | 1.80 | 1.80 |
| AOI221HSV2 | 1.80 | 1.80 |
| AOI221HSV4 | 1.80 | 2.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00115 | 0.00149 | 0.00197 | 0.00419 |
| A2 | 0.00124 | 0.00161 | 0.00215 | 0.00431 |
| B1 | 0.00083 | 0.00106 | 0.00139 | 0.00384 |
| B2 | 0.00093 | 0.00119 | 0.00157 | 0.00393 |
| C | 0.00061 | 0.00076 | 0.00099 | 0.00363 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00099 | 0.00120 | 0.00151 | 0.00101 |
| A2 | 0.00095 | 0.00117 | 0.00151 | 0.00099 |
| B1 | 0.00095 | 0.00117 | 0.00149 | 0.00103 |
| B2 | 0.00096 | 0.00117 | 0.00150 | 0.00099 |
| C | 0.00097 | 0.00122 | 0.00154 | 0.00104 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00017282 | 0.00025504 | 0.00038397 | 0.00047255 |

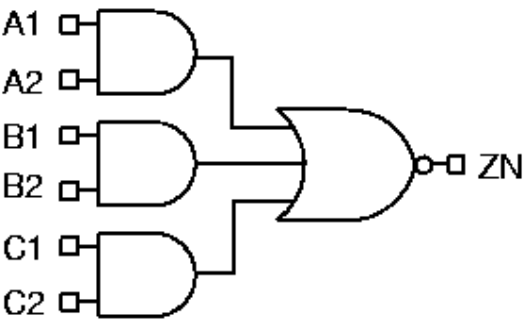
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.03464 | 0.03039 | 0.02688 | 0.09927 |
| A1→ZN_RISE | 0.07131 | 0.06665 | 0.06283 | 0.14761 |
| A2→ZN_FALL | 0.03676 | 0.03281 | 0.02933 | 0.10277 |
| A2→ZN_RISE | 0.07679 | 0.07268 | 0.06931 | 0.15698 |
| B1→ZN_FALL | 0.02994 | 0.02649 | 0.02349 | 0.09022 |
| B1→ZN_RISE | 0.06015 | 0.05579 | 0.05213 | 0.13599 |
| B2→ZN_FALL | 0.03262 | 0.02895 | 0.02590 | 0.09272 |
| B2→ZN_RISE | 0.06711 | 0.06248 | 0.05896 | 0.14403 |
| C→ZN_FALL | 0.01590 | 0.01412 | 0.01264 | 0.06366 |
| C→ZN_RISE | 0.04490 | 0.04034 | 0.03670 | 0.11865 |

AOI222HS

Cell Description

2-2-2 AOI
 $ZN = \neg((A1 \& A2) | (B1 \& B2) | (C1 \& C2))$



Function Table

| A1 | A2 | B1 | B2 | C1 | C2 | ZN |
|----|----|----|----|----|----|----|
| 0 | X | 0 | X | 0 | X | 1 |
| 0 | X | 0 | X | 1 | 0 | 1 |
| 0 | X | 0 | X | 1 | 1 | 0 |
| 0 | X | 1 | 0 | 0 | X | 1 |
| 0 | X | 1 | 0 | 1 | 0 | 1 |
| 0 | X | 1 | 0 | 1 | 1 | 0 |
| 0 | X | 1 | 1 | X | X | 0 |
| 1 | 0 | 0 | X | 0 | X | 1 |
| 1 | 0 | 0 | X | 1 | 0 | 1 |
| 1 | 0 | 0 | X | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | X | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | X | X | 0 |
| 1 | 1 | X | X | X | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| AOI222HSV0 | 1.80 | 2.00 |
| AOI222HSV1 | 1.80 | 2.00 |
| AOI222HSV2 | 1.80 | 2.20 |
| AOI222HSV4 | 1.80 | 3.00 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00079 | 0.00094 | 0.00117 | 0.00444 |
| A2 | 0.00087 | 0.00106 | 0.00135 | 0.00452 |

| | | | | |
|----|---------|---------|---------|---------|
| B1 | 0.00112 | 0.00137 | 0.00181 | 0.00416 |
| B2 | 0.00122 | 0.00150 | 0.00197 | 0.00423 |
| C1 | 0.00139 | 0.00174 | 0.00231 | 0.00382 |
| C2 | 0.00147 | 0.00186 | 0.00248 | 0.00391 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00100 | 0.00120 | 0.00144 | 0.00107 |
| A2 | 0.00097 | 0.00116 | 0.00144 | 0.00107 |
| B1 | 0.00108 | 0.00128 | 0.00170 | 0.00123 |
| B2 | 0.00102 | 0.00122 | 0.00149 | 0.00105 |
| C1 | 0.00098 | 0.00118 | 0.00151 | 0.00105 |
| C2 | 0.00101 | 0.00123 | 0.00154 | 0.00107 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00017539 | 0.00025939 | 0.00039567 | 0.00047616 |

Delay Table (ns)

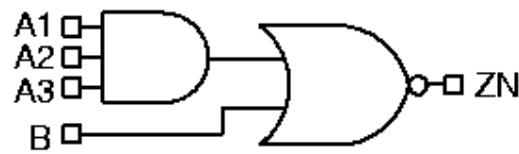
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.02964 | 0.02485 | 0.02099 | 0.11181 |
| A1→ZN_RISE | 0.05186 | 0.04481 | 0.03951 | 0.16142 |
| A2→ZN_FALL | 0.03155 | 0.02693 | 0.02349 | 0.11334 |
| A2→ZN_RISE | 0.05697 | 0.05026 | 0.04569 | 0.16758 |
| B1→ZN_FALL | 0.03721 | 0.03187 | 0.02852 | 0.10349 |
| B1→ZN_RISE | 0.07187 | 0.06451 | 0.06223 | 0.15295 |
| B2→ZN_FALL | 0.03995 | 0.03442 | 0.03057 | 0.10453 |
| B2→ZN_RISE | 0.07829 | 0.07073 | 0.06782 | 0.15747 |
| C1→ZN_FALL | 0.04267 | 0.03683 | 0.03251 | 0.09220 |
| C1→ZN_RISE | 0.08170 | 0.07456 | 0.07153 | 0.13007 |
| C2→ZN_FALL | 0.04447 | 0.03883 | 0.03456 | 0.09435 |
| C2→ZN_RISE | 0.08668 | 0.08008 | 0.07756 | 0.13723 |

AOI31HS

Cell Description

3-1 AOI

$$ZN = \neg((A1 \& A2 \& A3) | B)$$



Function Table

| A1 | A2 | A3 | B | ZN |
|----|----|----|---|----|
| 0 | X | X | 0 | 1 |
| 0 | X | X | 1 | 0 |
| 1 | 0 | X | 0 | 1 |
| 1 | 0 | X | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| AOI31HSV0 | 1.80 | 1.40 |
| AOI31HSV1 | 1.80 | 1.40 |
| AOI31HSV2 | 1.80 | 1.40 |
| AOI31HSV4 | 1.80 | 2.40 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00072 | 0.00092 | 0.00123 | 0.00370 |
| A2 | 0.00082 | 0.00105 | 0.00142 | 0.00379 |
| A3 | 0.00090 | 0.00116 | 0.00160 | 0.00392 |
| B | 0.00047 | 0.00058 | 0.00075 | 0.00348 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00097 | 0.00119 | 0.00151 | 0.00103 |
| A2 | 0.00098 | 0.00120 | 0.00152 | 0.00102 |

| | | | | |
|----|---------|---------|---------|---------|
| A3 | 0.00095 | 0.00116 | 0.00150 | 0.00106 |
| B | 0.00106 | 0.00129 | 0.00153 | 0.00116 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00010462 | 0.00015460 | 0.00024347 | 0.00039818 |

Delay Table (ns)

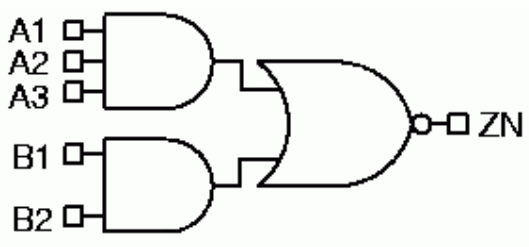
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.03959 | 0.03466 | 0.03028 | 0.10582 |
| A1→ZN_RISE | 0.03728 | 0.03384 | 0.03205 | 0.09707 |
| A2→ZN_FALL | 0.04405 | 0.03909 | 0.03452 | 0.11010 |
| A2→ZN_RISE | 0.04156 | 0.03831 | 0.03664 | 0.10249 |
| A3→ZN_FALL | 0.04587 | 0.04083 | 0.03703 | 0.11420 |
| A3→ZN_RISE | 0.04463 | 0.04136 | 0.04027 | 0.10930 |
| B→ZN_FALL | 0.01396 | 0.01232 | 0.01093 | 0.05965 |
| B→ZN_RISE | 0.02615 | 0.02332 | 0.02117 | 0.08233 |

AOI32HS

Cell Description

3-2 AOI

$$ZN = \neg((A1 \& A2 \& A3) | (B1 \& B2))$$



Function Table

| A1 | A2 | A3 | B1 | B2 | ZN |
|----|----|----|----|----|----|
| 0 | X | X | 0 | X | 1 |
| 0 | X | X | 1 | 0 | 1 |
| 0 | X | X | 1 | 1 | 0 |
| 1 | 0 | X | 0 | X | 1 |
| 1 | 0 | X | 1 | 0 | 1 |
| 1 | 0 | X | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | X | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | X | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| AOI32HSV0 | 1.80 | 1.60 |
| AOI32HSV1 | 1.80 | 1.60 |
| AOI32HSV2 | 1.80 | 1.60 |
| AOI32HSV4 | 1.80 | 2.60 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00093 | 0.00117 | 0.00157 | 0.00390 |
| A2 | 0.00102 | 0.00130 | 0.00175 | 0.00399 |
| A3 | 0.00110 | 0.00141 | 0.00192 | 0.00412 |
| B1 | 0.00054 | 0.00066 | 0.00090 | 0.00353 |
| B2 | 0.00064 | 0.00080 | 0.00110 | 0.00362 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00099 | 0.00120 | 0.00152 | 0.00109 |
| A2 | 0.00098 | 0.00119 | 0.00150 | 0.00103 |
| A3 | 0.00095 | 0.00115 | 0.00148 | 0.00106 |
| B1 | 0.00103 | 0.00124 | 0.00149 | 0.00108 |
| B2 | 0.00094 | 0.00116 | 0.00151 | 0.00102 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00011568 | 0.00016680 | 0.00027451 | 0.00040791 |

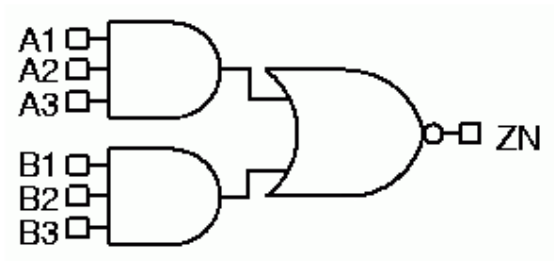
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.04692 | 0.04073 | 0.03580 | 0.11590 |
| A1→ZN_RISE | 0.04257 | 0.03864 | 0.03681 | 0.10263 |
| A2→ZN_FALL | 0.05097 | 0.04518 | 0.04014 | 0.12032 |
| A2→ZN_RISE | 0.04630 | 0.04267 | 0.04103 | 0.10769 |
| A3→ZN_FALL | 0.05288 | 0.04692 | 0.04241 | 0.12402 |
| A3→ZN_RISE | 0.04924 | 0.04550 | 0.04441 | 0.11358 |
| B1→ZN_FALL | 0.02342 | 0.02015 | 0.01797 | 0.08045 |
| B1→ZN_RISE | 0.02779 | 0.02470 | 0.02336 | 0.08536 |
| B2→ZN_FALL | 0.02613 | 0.02286 | 0.02084 | 0.08304 |
| B2→ZN_RISE | 0.03161 | 0.02856 | 0.02767 | 0.09008 |

AOI33HS

Cell Description

3-3 AOI
 $ZN = \neg((A1 \& A2 \& A3) | (B1 \& B2 \& B3))$



Function Table

| A1 | A2 | A3 | B1 | B2 | B3 | ZN |
|----|----|----|----|----|----|----|
| 0 | X | X | 0 | X | X | 1 |
| 0 | X | X | 1 | 0 | X | 1 |
| 0 | X | X | 1 | 1 | 0 | 1 |
| 0 | X | X | 1 | 1 | 1 | 0 |
| 1 | 0 | X | 0 | X | X | 1 |
| 1 | 0 | X | 1 | 0 | X | 1 |
| 1 | 0 | X | 1 | 1 | 0 | 1 |
| 1 | 0 | X | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | X | X | 1 |
| 1 | 1 | 0 | 1 | 0 | X | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | X | X | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| AOI33HSV0 | 1.80 | 1.80 |
| AOI33HSV1 | 1.80 | 1.80 |
| AOI33HSV2 | 1.80 | 1.80 |
| AOI33HSV4 | 1.80 | 2.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00112 | 0.00144 | 0.00192 | 0.00408 |
| A2 | 0.00120 | 0.00156 | 0.00210 | 0.00416 |
| A3 | 0.00129 | 0.00167 | 0.00227 | 0.00429 |
| B1 | 0.00067 | 0.00084 | 0.00111 | 0.00363 |

| | | | | |
|----|---------|---------|---------|---------|
| B2 | 0.00078 | 0.00099 | 0.00133 | 0.00373 |
| B3 | 0.00086 | 0.00110 | 0.00152 | 0.00380 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00100 | 0.00120 | 0.00148 | 0.00107 |
| A2 | 0.00098 | 0.00118 | 0.00151 | 0.00102 |
| A3 | 0.00093 | 0.00114 | 0.00147 | 0.00106 |
| B1 | 0.00101 | 0.00121 | 0.00147 | 0.00115 |
| B2 | 0.00099 | 0.00120 | 0.00151 | 0.00109 |
| B3 | 0.00094 | 0.00117 | 0.00149 | 0.00104 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00017101 | 0.00020333 | 0.00028640 | 0.00041407 |

Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.05448 | 0.04848 | 0.04245 | 0.12692 |
| A1→ZN_RISE | 0.04644 | 0.04301 | 0.04101 | 0.10766 |
| A2→ZN_FALL | 0.05840 | 0.05255 | 0.04707 | 0.13094 |
| A2→ZN_RISE | 0.04973 | 0.04655 | 0.04518 | 0.11201 |
| A3→ZN_FALL | 0.06033 | 0.05435 | 0.04922 | 0.13494 |
| A3→ZN_RISE | 0.05255 | 0.04937 | 0.04828 | 0.11783 |
| B1→ZN_FALL | 0.03678 | 0.03159 | 0.02712 | 0.10618 |
| B1→ZN_RISE | 0.03165 | 0.02842 | 0.02647 | 0.09136 |
| B2→ZN_FALL | 0.04237 | 0.03723 | 0.03280 | 0.11092 |
| B2→ZN_RISE | 0.03604 | 0.03288 | 0.03132 | 0.09608 |
| B3→ZN_FALL | 0.04379 | 0.03909 | 0.03549 | 0.11230 |
| B3→ZN_RISE | 0.03820 | 0.03537 | 0.03472 | 0.09929 |

BENCHS

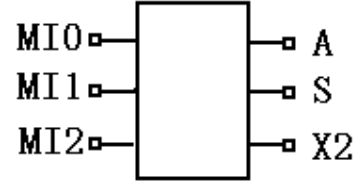
Cell Description

The booth encoder block, BENC, cell performs a 2bit multiplier recoding per a modified Booth's algorithm. Each BENC cell examines 3 bits of the multiplier (MI0,MI1,MI2) and generates the appropriate control signals to adjust the multiplicand for subsequent partial product reduction.

$A = (MI2)(\neg MI1 \& \neg MI0)$

$S = (\neg MI2)(MI1 \& MI0)$

$X2 = (\neg (MI1 \wedge MI0))$



Function Table

| MI2 | MI1 | MI0 | A | S | X2 |
|-----|-----|-----|---|---|----|
| 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| BENCHSV1 | 1.80 | 6.80 |
| BENCHSV2 | 1.80 | 6.80 |
| BENCHSV4 | 1.80 | 7.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| MI0 | 0.00367 | 0.00403 | 0.00564 |
| MI1 | 0.00294 | 0.00322 | 0.00471 |
| MI2 | 0.00259 | 0.00283 | 0.00432 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| MI0 | 0.00212 | 0.00232 | 0.00277 |
| MI1 | 0.00374 | 0.00402 | 0.00473 |
| MI2 | 0.00226 | 0.00244 | 0.00308 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00084726 | 0.00099839 | 0.00169800 |

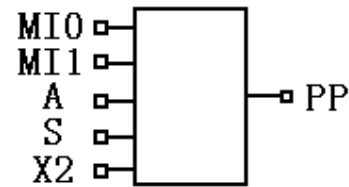
Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| MI0→A_FALL | 0.07288 | 0.07026 | 0.06648 |
| MI0→A_RISE | 0.10428 | 0.10374 | 0.08970 |
| MI1→A_FALL | 0.07692 | 0.07441 | 0.07166 |
| MI1→A_RISE | 0.10776 | 0.10753 | 0.09420 |
| MI2→A_FALL | 0.09245 | 0.08766 | 0.08418 |
| MI2→A_RISE | 0.08276 | 0.07889 | 0.07138 |
| MI0→S_FALL | 0.12111 | 0.11168 | 0.10337 |
| MI0→S_RISE | 0.14342 | 0.13786 | 0.11733 |
| MI1→S_FALL | 0.11305 | 0.10468 | 0.09855 |
| MI1→S_RISE | 0.13718 | 0.13196 | 0.11385 |
| MI2→S_FALL | 0.07247 | 0.06876 | 0.06004 |
| MI2→S_RISE | 0.06974 | 0.06649 | 0.05524 |
| MI0→X2_FALL | 0.11773 | 0.10839 | 0.10192 |
| MI0→X2_RISE | 0.13057 | 0.12061 | 0.11274 |
| MI1→X2_FALL | 0.08432 | 0.07814 | 0.07354 |
| MI1→X2_RISE | 0.08773 | 0.08282 | 0.07633 |

BMUXHS

Cell Description

The BMUX cell performs the shifting and 2's complement inversion of the multiplicand bits (MI1,MI0) based on the recode control signals (X2,A,S) from the booth encoder block cell.

$$PP=((X2\&((MI0\&!A)|(!MI0\&!S)))(!X2\&((MI1\&!A)|(!MI1\&!S))))$$


Function Table

| S | MI1 | A | X2 | MI0 | PP |
|---|-----|---|----|-----|----|
| 0 | 0 | 0 | X | X | 1 |
| 0 | 0 | 1 | 0 | X | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | X | X | 1 |
| 0 | 1 | 1 | 0 | X | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | X | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | X | X | 0 |
| 1 | 1 | 0 | 0 | X | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | X | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| BMUXHSV1 | 1.80 | 4.80 |
| BMUXHSV2 | 1.80 | 4.80 |
| BMUXHSV4 | 1.80 | 5.60 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00405 | 0.00462 | 0.00692 |
| MI0 | 0.00317 | 0.00362 | 0.00521 |

| | | | |
|-----|---------|---------|---------|
| MI1 | 0.00352 | 0.00400 | 0.00574 |
| S | 0.00414 | 0.00472 | 0.00693 |
| X2 | 0.00193 | 0.00220 | 0.00327 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| A | 0.00124 | 0.00138 | 0.00158 |
| MI0 | 0.00184 | 0.00204 | 0.00215 |
| MI1 | 0.00177 | 0.00199 | 0.00212 |
| S | 0.00127 | 0.00142 | 0.00164 |
| X2 | 0.00174 | 0.00190 | 0.00209 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00076781 | 0.00094286 | 0.00123600 |

Delay Table (ns)

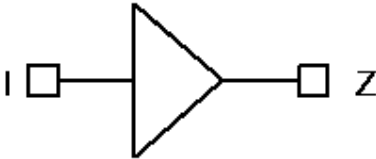
| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| A→PP_FALL | 0.11892 | 0.11272 | 0.11875 |
| A→PP_RISE | 0.12948 | 0.12451 | 0.13244 |
| MI0→PP_FALL | 0.10590 | 0.10044 | 0.10272 |
| MI0→PP_RISE | 0.10084 | 0.09658 | 0.09663 |
| MI1→PP_FALL | 0.11769 | 0.11097 | 0.11194 |
| MI1→PP_RISE | 0.11544 | 0.10940 | 0.10970 |
| S→PP_FALL | 0.12173 | 0.11570 | 0.12083 |
| S→PP_RISE | 0.12961 | 0.12468 | 0.13152 |
| X2→PP_FALL | 0.06030 | 0.05782 | 0.05878 |
| X2→PP_RISE | 0.05548 | 0.05362 | 0.05315 |

BUFHS

Cell Description

Non-Inverting Buffer

$Z=I$



Function Table

| | |
|---|---|
| I | Z |
| 0 | 0 |
| 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| BUFHSV0 | 1.80 | 0.80 |
| BUFHSV0RT | 1.80 | 0.80 |
| BUFHSV1 | 1.80 | 0.80 |
| BUFHSV1RT | 1.80 | 0.80 |
| BUFHSV2 | 1.80 | 0.80 |
| BUFHSV2RQ | 1.80 | 0.80 |
| BUFHSV2RT | 1.80 | 0.80 |
| BUFHSV3 | 1.80 | 1.00 |
| BUFHSV3RQ | 1.80 | 1.00 |
| BUFHSV3RT | 1.80 | 1.00 |
| BUFHSV4 | 1.80 | 1.00 |
| BUFHSV4RQ | 1.80 | 1.00 |
| BUFHSV4RT | 1.80 | 1.00 |
| BUFHSV6 | 1.80 | 1.40 |
| BUFHSV6RQ | 1.80 | 1.40 |
| BUFHSV6RT | 1.80 | 1.40 |
| BUFHSV8 | 1.80 | 1.80 |
| BUFHSV8RO | 1.80 | 1.60 |
| BUFHSV8RQ | 1.80 | 1.60 |
| BUFHSV8RT | 1.80 | 1.80 |
| BUFHSV12 | 1.80 | 2.60 |
| BUFHSV12RO | 1.80 | 2.00 |

| | | |
|------------|------|------|
| BUFHSV12RQ | 1.80 | 2.40 |
| BUFHSV12RT | 1.80 | 2.40 |
| BUFHSV16 | 1.80 | 3.00 |
| BUFHSV16RO | 1.80 | 2.60 |
| BUFHSV16RQ | 1.80 | 2.80 |
| BUFHSV16RT | 1.80 | 3.00 |
| BUFHSV20 | 1.80 | 3.80 |
| BUFHSV20RO | 1.80 | 3.40 |
| BUFHSV20RQ | 1.80 | 3.60 |
| BUFHSV20RT | 1.80 | 3.80 |
| BUFHSV24 | 1.80 | 4.60 |
| BUFHSV24RO | 1.80 | 3.80 |
| BUFHSV24RQ | 1.80 | 4.00 |
| BUFHSV24RT | 1.80 | 4.40 |
| BUFHSV32 | 1.80 | 6.40 |
| BUFHSV32RO | 1.80 | 4.80 |
| BUFHSV32RQ | 1.80 | 5.40 |
| BUFHSV32RT | 1.80 | 5.80 |
| BUFHSV40 | 1.80 | 7.80 |
| BUFHSV40RO | 1.80 | 6.00 |
| BUFHSV40RQ | 1.80 | 6.60 |
| BUFHSV40RT | 1.80 | 7.00 |
| BUFHSV48 | 1.80 | 9.40 |
| BUFHSV48RO | 1.80 | 7.00 |
| BUFHSV48RQ | 1.80 | 7.80 |

Pin Power (uW/MHz)

| Pin | V0 | V0RT | V1 | V1RT | V2 | V2RQ | V2RT | V3 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00107 | 0.00100 | 0.00122 | 0.00121 | 0.00146 | 0.00133 | 0.00135 | 0.00200 |

| Pin | V3RQ | V3RT | V4 | V4RQ | V4RT | V6 | V6RQ | V6RT |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00179 | 0.00184 | 0.00244 | 0.00213 | 0.00221 | 0.00351 | 0.00317 | 0.00323 |

| Pin | V8 | V8RO | V8RQ | V8RT | V12 | V12RO | V12RQ | V12RT |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00453 | 0.00407 | 0.00412 | 0.00410 | 0.00680 | 0.00602 | 0.00601 | 0.00617 |

| Pin | V16 | V16RO | V16RQ | V16RT | V20 | V20RO | V20RQ | V20RT |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00885 | 0.00786 | 0.00781 | 0.00804 | 0.01109 | 0.00973 | 0.00994 | 0.01008 |

| Pin | V24 | V24RO | V24RQ | V24RT | V32 | V32RO | V32RQ | V32RT |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.01318 | 0.01163 | 0.01183 | 0.01180 | 0.01703 | 0.01550 | 0.01558 | 0.01609 |

| Pin | V40 | V40RO | V40RQ | V40RT | V48 | V48RO | V48RQ |
|-----|---------|---------|---------|---------|---------|---------|---------|
| I | 0.02112 | 0.01945 | 0.01955 | 0.01988 | 0.02550 | 0.02332 | 0.02335 |

Pin Capacitance (pf)

| Pin | V0 | V0RT | V1 | V1RT | V2 | V2RQ | V2RT | V3 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00110 | 0.00098 | 0.00112 | 0.00101 | 0.00109 | 0.00098 | 0.00096 | 0.00123 |

| Pin | V3RQ | V3RT | V4 | V4RQ | V4RT | V6 | V6RQ | V6RT |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00101 | 0.00106 | 0.00147 | 0.00103 | 0.00126 | 0.00169 | 0.00133 | 0.00158 |

| Pin | V8 | V8RO | V8RQ | V8RT | V12 | V12RO | V12RQ | V12RT |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00258 | 0.00115 | 0.00161 | 0.00215 | 0.00390 | 0.00136 | 0.00241 | 0.00293 |

| Pin | V16 | V16RO | V16RQ | V16RT | V20 | V20RO | V20RQ | V20RT |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00466 | 0.00157 | 0.00297 | 0.00395 | 0.00614 | 0.00215 | 0.00377 | 0.00497 |

| Pin | V24 | V24RO | V24RQ | V24RT | V32 | V32RO | V32RQ | V32RT |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00727 | 0.00236 | 0.00427 | 0.00562 | 0.01108 | 0.00287 | 0.00566 | 0.00770 |

| Pin | V40 | V40RO | V40RQ | V40RT | V48 | V48RO | V48RQ |
|-----|---------|---------|---------|---------|---------|---------|---------|
| I | 0.01384 | 0.00369 | 0.00708 | 0.00951 | 0.01656 | 0.00424 | 0.00834 |

Max Leakage Power (uW)

| V0 | V0RT | V1 | V1RT | V2 | V2RQ | V2RT | V3 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00010730 | 0.00009988 | 0.00011476 | 0.00011381 | 0.00014721 | 0.00013686 | 0.00013927 | 0.00021492 |

| V3RQ | V3RT | V4 | V4RQ | V4RT | V6 | V6RQ | V6RT |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00018940 | 0.00020067 | 0.00028111 | 0.00025286 | 0.00027158 | 0.00044940 | 0.00041654 | 0.00043364 |

| V8 | V8RO | V8RQ | V8RT | V12 | V12RO | V12RQ | V12RT |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00064097 | 0.00054256 | 0.00059116 | 0.00060877 | 0.00101690 | 0.00086520 | 0.00094979 | 0.00098186 |

| V16 | V16RO | V16RQ | V16RT | V20 | V20RO | V20RQ | V20RT |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00138360 | 0.00121060 | 0.00129760 | 0.00133030 | 0.00178490 | 0.00156490 | 0.00167580 | 0.00169570 |

| V24 | V24RO | V24RQ | V24RT | V32 | V32RO | V32RQ | V32RT |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00217850 | 0.00189690 | 0.00202250 | 0.00207670 | 0.00306410 | 0.00259720 | 0.00276170 | 0.00287190 |

| V40 | V40RO | V40RQ | V40RT | V48 | V48RO | V48RQ |
|------------|------------|------------|------------|------------|------------|------------|
| 0.00386950 | 0.00328870 | 0.00350690 | 0.00362850 | 0.00467330 | 0.00399430 | 0.00423610 |

Delay Table (ns)

| Description | V0 | V0RT | V1 | V1RT | V2 | V2RQ | V2RT | V3 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| I→Z_FALL | 0.03454 | 0.03936 | 0.03516 | 0.04067 | 0.03633 | 0.04143 | 0.04159 | 0.03736 |
| I→Z_RISE | 0.03217 | 0.03354 | 0.03208 | 0.03318 | 0.03377 | 0.03454 | 0.03478 | 0.03329 |

| Description | V3RQ | V3RT | V4 | V4RQ | V4RT | V6 | V6RQ | V6RT |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| I→Z_FALL | 0.04881 | 0.04254 | 0.03564 | 0.04607 | 0.04003 | 0.03789 | 0.04592 | 0.03938 |

| | | | | | | | | |
|----------|---------|---------|---------|---------|---------|---------|---------|---------|
| I→Z_RISE | 0.03791 | 0.03522 | 0.03194 | 0.03891 | 0.03359 | 0.03290 | 0.03712 | 0.03185 |
|----------|---------|---------|---------|---------|---------|---------|---------|---------|

| | | | | | | | | |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| Description | V8 | V8RO | V8RQ | V8RT | V12 | V12RO | V12RQ | V12RT |
| I→Z_FALL | 0.03247 | 0.06746 | 0.04557 | 0.03618 | 0.03225 | 0.06907 | 0.04259 | 0.03663 |
| I→Z_RISE | 0.02848 | 0.05425 | 0.03618 | 0.03006 | 0.02813 | 0.05345 | 0.03405 | 0.02955 |

| | | | | | | | | |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| Description | V16 | V16RO | V16RQ | V16RT | V20 | V20RO | V20RQ | V20RT |
| I→Z_FALL | 0.03301 | 0.06853 | 0.04251 | 0.03626 | 0.03159 | 0.06362 | 0.04248 | 0.03592 |
| I→Z_RISE | 0.02841 | 0.05239 | 0.03359 | 0.02928 | 0.02719 | 0.04960 | 0.03369 | 0.02894 |

| | | | | | | | | |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| Description | V24 | V24RO | V24RQ | V24RT | V32 | V32RO | V32RQ | V32RT |
| I→Z_FALL | 0.03170 | 0.06539 | 0.04270 | 0.03587 | 0.03106 | 0.06651 | 0.04258 | 0.03653 |
| I→Z_RISE | 0.02713 | 0.05019 | 0.03363 | 0.02872 | 0.02615 | 0.05069 | 0.03377 | 0.02970 |

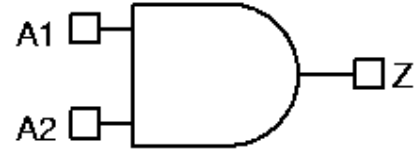
| | | | | | | | |
|-------------|---------|---------|---------|---------|---------|---------|---------|
| Description | V40 | V40RO | V40RQ | V40RT | V48 | V48RO | V48RQ |
| I→Z_FALL | 0.03106 | 0.06657 | 0.04299 | 0.03677 | 0.03122 | 0.06688 | 0.04254 |
| I→Z_RISE | 0.02619 | 0.05101 | 0.03396 | 0.02986 | 0.02627 | 0.05057 | 0.03359 |

CLKAND2HS

Cell Description

2-Input Clock AND

$$Z=(A1\&A2)$$



Function Table

| A1 | A2 | Z |
|----|----|---|
| 0 | X | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| CLKAND2HSV0 | 1.80 | 1.00 |
| CLKAND2HSV1 | 1.80 | 1.00 |
| CLKAND2HSV2 | 1.80 | 1.00 |
| CLKAND2HSV4 | 1.80 | 1.80 |
| CLKAND2HSV8 | 1.80 | 2.60 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 | V8 |
|-----|---------|---------|---------|---------|---------|
| A1 | 0.00113 | 0.00127 | 0.00160 | 0.00260 | 0.00496 |
| A2 | 0.00128 | 0.00143 | 0.00180 | 0.00290 | 0.00548 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 | V8 |
|-----|---------|---------|---------|---------|---------|
| A1 | 0.00114 | 0.00118 | 0.00142 | 0.00204 | 0.00381 |
| A2 | 0.00116 | 0.00123 | 0.00145 | 0.00218 | 0.00382 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 | V8 |
|------------|------------|------------|------------|------------|
| 0.00015326 | 0.00017019 | 0.00020665 | 0.00035334 | 0.00070024 |

Delay Table (ns)

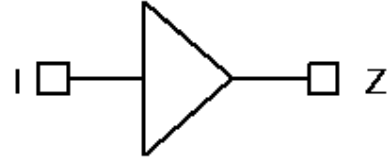
| Description | V0 | V1 | V2 | V4 | V8 |
|-------------|---------|---------|---------|---------|---------|
| A1→Z_FALL | 0.03780 | 0.03749 | 0.03547 | 0.03529 | 0.03380 |
| A1→Z_RISE | 0.03854 | 0.03733 | 0.03505 | 0.03175 | 0.03118 |
| A2→Z_FALL | 0.04164 | 0.04145 | 0.03923 | 0.03971 | 0.03748 |
| A2→Z_RISE | 0.04133 | 0.04023 | 0.03781 | 0.03462 | 0.03373 |

CLKBUFHS

Cell Description

Clock Buffer with Balanced Rise/Fall Time

Z=I



Function Table

| I | Z |
|---|---|
| 0 | 0 |
| 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|---------------|------------|-----------|
| CLKBUFHSV0 | 1.80 | 0.80 |
| CLKBUFHSV0P5 | 1.80 | 0.80 |
| CLKBUFHSV1 | 1.80 | 0.80 |
| CLKBUFHSV2 | 1.80 | 0.80 |
| CLKBUFHSV2RQ | 1.80 | 0.80 |
| CLKBUFHSV3 | 1.80 | 1.00 |
| CLKBUFHSV3RQ | 1.80 | 1.00 |
| CLKBUFHSV4 | 1.80 | 1.00 |
| CLKBUFHSV4RQ | 1.80 | 1.00 |
| CLKBUFHSV5 | 1.80 | 1.60 |
| CLKBUFHSV5RQ | 1.80 | 1.40 |
| CLKBUFHSV6 | 1.80 | 1.40 |
| CLKBUFHSV6RQ | 1.80 | 1.40 |
| CLKBUFHSV8 | 1.80 | 1.80 |
| CLKBUFHSV8RO | 1.80 | 1.60 |
| CLKBUFHSV8RQ | 1.80 | 1.60 |
| CLKBUFHSV12 | 1.80 | 2.40 |
| CLKBUFHSV12RO | 1.80 | 2.00 |
| CLKBUFHSV12RQ | 1.80 | 2.40 |
| CLKBUFHSV16 | 1.80 | 3.00 |
| CLKBUFHSV16RO | 1.80 | 2.60 |
| CLKBUFHSV16RQ | 1.80 | 2.80 |

| | | |
|---------------|------|------|
| CLKBUFHSV20 | 1.80 | 3.80 |
| CLKBUFHSV20RO | 1.80 | 3.40 |
| CLKBUFHSV20RQ | 1.80 | 3.60 |
| CLKBUFHSV24 | 1.80 | 4.40 |
| CLKBUFHSV24RO | 1.80 | 3.80 |
| CLKBUFHSV24RQ | 1.80 | 4.00 |
| CLKBUFHSV32 | 1.80 | 6.40 |
| CLKBUFHSV32RO | 1.80 | 4.80 |
| CLKBUFHSV32RQ | 1.80 | 5.40 |
| CLKBUFHSV40 | 1.80 | 7.80 |
| CLKBUFHSV40RO | 1.80 | 6.00 |
| CLKBUFHSV40RQ | 1.80 | 6.60 |
| CLKBUFHSV48 | 1.80 | 9.40 |
| CLKBUFHSV48RO | 1.80 | 7.40 |
| CLKBUFHSV48RQ | 1.80 | 7.80 |

Pin Power (uW/MHz)

| Pin | V0 | V0P5 | V1 | V2 | V2RQ | V3 | V3RQ | V4 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00104 | 0.00115 | 0.00120 | 0.00141 | 0.00138 | 0.00193 | 0.00183 | 0.00234 |

| Pin | V4RQ | V5 | V5RQ | V6 | V6RQ | V8 | V8RO | V8RQ |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00213 | 0.00297 | 0.00277 | 0.00323 | 0.00312 | 0.00411 | 0.00383 | 0.00392 |

| Pin | V12 | V12RO | V12RQ | V16 | V16RO | V16RQ | V20 | V20RO |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00588 | 0.00581 | 0.00584 | 0.00785 | 0.00772 | 0.00757 | 0.00998 | 0.00951 |

| Pin | V20RQ | V24 | V24RO | V24RQ | V32 | V32RO | V32RQ | V40 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00960 | 0.01151 | 0.01098 | 0.01126 | 0.01642 | 0.01478 | 0.01495 | 0.02093 |

| Pin | V40RO | V40RQ | V48 | V48RO | V48RQ |
|-----|---------|---------|---------|---------|---------|
| I | 0.01882 | 0.01912 | 0.02509 | 0.02255 | 0.02279 |

Pin Capacitance (pf)

| Pin | V0 | V0P5 | V1 | V2 | V2RQ | V3 | V3RQ | V4 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00113 | 0.00114 | 0.00118 | 0.00121 | 0.00113 | 0.00137 | 0.00113 | 0.00163 |

| Pin | V4RQ | V5 | V5RQ | V6 | V6RQ | V8 | V8RO | V8RQ |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00117 | 0.00212 | 0.00120 | 0.00163 | 0.00135 | 0.00222 | 0.00112 | 0.00157 |

| Pin | V12 | V12RO | V12RQ | V16 | V16RO | V16RQ | V20 | V20RO |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00292 | 0.00131 | 0.00235 | 0.00384 | 0.00159 | 0.00288 | 0.00492 | 0.00198 |

| Pin | V20RQ | V24 | V24RO | V24RQ | V32 | V32RO | V32RQ | V40 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00378 | 0.00551 | 0.00230 | 0.00426 | 0.01084 | 0.00283 | 0.00549 | 0.01367 |

| Pin | V40RO | V40RQ | V48 | V48RO | V48RQ |
|-----|---------|---------|---------|---------|---------|
| I | 0.00351 | 0.00693 | 0.01668 | 0.00447 | 0.00813 |

Max Leakage Power (uW)

| V0 | V0P5 | V1 | V2 | V2RQ | V3 | V3RQ | V4 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00010741 | 0.00011340 | 0.00011842 | 0.00013788 | 0.00012425 | 0.00020944 | 0.00017588 | 0.00025994 |

| V4RQ | V5 | V5RQ | V6 | V6RQ | V8 | V8RO | V8RQ |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00020720 | 0.00032274 | 0.00026267 | 0.00036212 | 0.00030510 | 0.00049914 | 0.00038948 | 0.00041431 |

| V12 | V12RO | V12RQ | V16 | V16RO | V16RQ | V20 | V20RO |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00072012 | 0.00060229 | 0.00066802 | 0.00103770 | 0.00089899 | 0.00098557 | 0.00139640 | 0.00108890 |

| V20RQ | V24 | V24RO | V24RQ | V32 | V32RO | V32RQ | V40 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00114180 | 0.00163920 | 0.00146360 | 0.00156540 | 0.00238040 | 0.00192700 | 0.00208610 | 0.00297980 |

| V40RO | V40RQ | V48 | V48RO | V48RQ |
|------------|------------|------------|------------|------------|
| 0.00245460 | 0.00261670 | 0.00362350 | 0.00300760 | 0.00318570 |

Delay Table (ns)

| Description | V0 | V0P5 | V1 | V2 | V2RQ | V3 | V3RQ | V4 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| I→Z_FALL | 0.03252 | 0.03311 | 0.03295 | 0.03482 | 0.03441 | 0.03295 | 0.03877 | 0.03197 |
| I→Z_RISE | 0.03075 | 0.03207 | 0.03149 | 0.03283 | 0.03422 | 0.03154 | 0.03805 | 0.02951 |

| Description | V4RQ | V5 | V5RQ | V6 | V6RQ | V8 | V8RO | V8RQ |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| I→Z_FALL | 0.04131 | 0.03073 | 0.04514 | 0.03726 | 0.04368 | 0.03470 | 0.05805 | 0.04220 |
| I→Z_RISE | 0.04050 | 0.02976 | 0.04434 | 0.03497 | 0.04293 | 0.03406 | 0.05659 | 0.04174 |

| Description | V12 | V12RO | V12RQ | V16 | V16RO | V16RQ | V20 | V20RO |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| I→Z_FALL | 0.03438 | 0.06376 | 0.04010 | 0.03379 | 0.06393 | 0.03961 | 0.03285 | 0.05990 |
| I→Z_RISE | 0.03306 | 0.06240 | 0.03938 | 0.03331 | 0.06250 | 0.03831 | 0.03329 | 0.06249 |

| Description | V20RQ | V24 | V24RO | V24RQ | V32 | V32RO | V32RQ | V40 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| I→Z_FALL | 0.03998 | 0.03412 | 0.05923 | 0.03994 | 0.02885 | 0.06095 | 0.03944 | 0.03031 |
| I→Z_RISE | 0.03862 | 0.03358 | 0.05799 | 0.03856 | 0.02756 | 0.05844 | 0.03767 | 0.02895 |

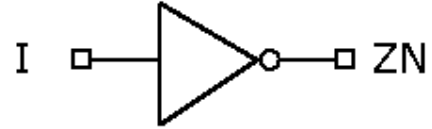
| Description | V40RO | V40RQ | V48 | V48RO | V48RQ |
|-------------|---------|---------|---------|---------|---------|
| I→Z_FALL | 0.06057 | 0.04091 | 0.03049 | 0.06015 | 0.04100 |
| I→Z_RISE | 0.06099 | 0.03900 | 0.02901 | 0.05789 | 0.03886 |

CLKNHS

Cell Description

Inverting Clock Buffer with Balanced Rise/Fall Time

$ZN = (!I)$



Function Table

| I | ZN |
|---|----|
| 0 | 1 |
| 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| CLKNHSV0 | 1.80 | 0.60 |
| CLKNHSV0P5 | 1.80 | 0.60 |
| CLKNHSV1 | 1.80 | 0.60 |
| CLKNHSV2 | 1.80 | 0.60 |
| CLKNHSV2P5 | 1.80 | 0.80 |
| CLKNHSV3 | 1.80 | 0.80 |
| CLKNHSV4 | 1.80 | 0.80 |
| CLKNHSV5 | 1.80 | 1.00 |
| CLKNHSV6 | 1.80 | 1.00 |
| CLKNHSV8 | 1.80 | 1.40 |
| CLKNHSV10 | 1.80 | 1.60 |
| CLKNHSV12 | 1.80 | 1.80 |
| CLKNHSV16 | 1.80 | 2.40 |
| CLKNHSV20 | 1.80 | 2.80 |
| CLKNHSV24 | 1.80 | 3.40 |
| CLKNHSV32 | 1.80 | 4.20 |
| CLKNHSV48 | 1.80 | 6.00 |
| CLKNHSV64 | 1.80 | 7.80 |

Pin Power (uW/MHz)

| Pin | V0 | V0P5 | V1 | V2 | V2P5 | V3 | V4 | V5 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00031 | 0.00036 | 0.00038 | 0.00049 | 0.00057 | 0.00073 | 0.00090 | 0.00107 |

| Pin | V6 | V8 | V10 | V12 | V16 | V20 | V24 | V32 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00123 | 0.00161 | 0.00189 | 0.00217 | 0.00281 | 0.00374 | 0.00427 | 0.00552 |

| Pin | V48 | V64 |
|-----|---------|---------|
| I | 0.00825 | 0.01262 |

Pin Capacitance (pf)

| Pin | V0 | V0P5 | V1 | V2 | V2P5 | V3 | V4 | V5 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00091 | 0.00102 | 0.00110 | 0.00142 | 0.00188 | 0.00220 | 0.00268 | 0.00333 |

| Pin | V6 | V8 | V10 | V12 | V16 | V20 | V24 | V32 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00387 | 0.00506 | 0.00618 | 0.00724 | 0.00957 | 0.01210 | 0.01418 | 0.01895 |

| Pin | V48 | V64 |
|-----|---------|---------|
| I | 0.02715 | 0.03462 |

Max Leakage Power (uW)

| V0 | V0P5 | V1 | V2 | V2P5 | V3 | V4 | V5 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00005173 | 0.00005613 | 0.00006369 | 0.00007308 | 0.00011439 | 0.00013454 | 0.00017042 | 0.00020795 |

| V6 | V8 | V10 | V12 | V16 | V20 | V24 | V32 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00025931 | 0.00035491 | 0.00043089 | 0.00055740 | 0.00079203 | 0.00106790 | 0.00126430 | 0.00166500 |

| V48 | V64 |
|------------|------------|
| 0.00269190 | 0.00369610 |

Delay Table (ns)

| Description | V0 | V0P5 | V1 | V2 | V2P5 | V3 | V4 | V5 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| I→ZN_FALL | 0.01258 | 0.01316 | 0.01199 | 0.01106 | 0.01078 | 0.01052 | 0.00984 | 0.00998 |
| I→ZN_RISE | 0.01328 | 0.01214 | 0.01231 | 0.01136 | 0.01039 | 0.01054 | 0.01015 | 0.00963 |

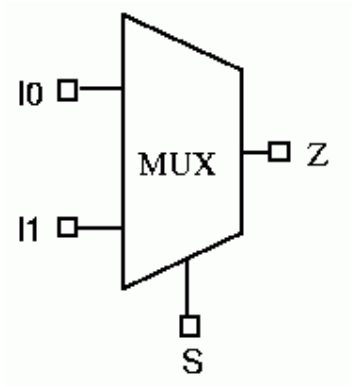
| Description | V6 | V8 | V10 | V12 | V16 | V20 | V24 | V32 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| I→ZN_FALL | 0.00936 | 0.00934 | 0.00913 | 0.00930 | 0.00888 | 0.00931 | 0.00964 | 0.00996 |
| I→ZN_RISE | 0.00952 | 0.00930 | 0.00905 | 0.00920 | 0.00880 | 0.00937 | 0.00977 | 0.01057 |

| Description | V48 | V64 |
|-------------|---------|---------|
| I→ZN_FALL | 0.01232 | 0.01572 |
| I→ZN_RISE | 0.01349 | 0.01724 |

CKMUX2HS

Cell Description

2-to-1 Multiplexer
 $Z=((I0\&(!S))|(I1\&S))$



Function Table

| S | I0 | I1 | Z |
|---|----|----|---|
| 0 | 0 | X | 0 |
| 0 | 1 | X | 1 |
| 1 | X | 0 | 0 |
| 1 | X | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| CKMUX2HSV0 | 1.80 | 2.60 |
| CKMUX2HSV1 | 1.80 | 2.60 |
| CKMUX2HSV2 | 1.80 | 2.60 |
| CKMUX2HSV4 | 1.80 | 3.00 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| I0 | 0.00200 | 0.00206 | 0.00245 | 0.00359 |
| I1 | 0.00191 | 0.00197 | 0.00236 | 0.00346 |
| S | 0.00207 | 0.00213 | 0.00254 | 0.00368 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| I0 | 0.00115 | 0.00118 | 0.00135 | 0.00159 |
| I1 | 0.00118 | 0.00119 | 0.00135 | 0.00158 |
| S | 0.00183 | 0.00181 | 0.00216 | 0.00274 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00033485 | 0.00034269 | 0.00040239 | 0.00061504 |

Delay Table (ns)

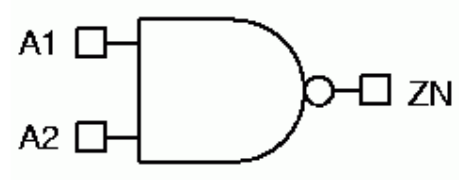
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| I0→Z_FALL | 0.06940 | 0.06744 | 0.06392 | 0.06281 |
| I0→Z_RISE | 0.06794 | 0.06512 | 0.06059 | 0.05894 |
| I1→Z_FALL | 0.06859 | 0.06668 | 0.06328 | 0.06208 |
| I1→Z_RISE | 0.06394 | 0.06108 | 0.05728 | 0.05681 |
| S→Z_FALL | 0.05994 | 0.05807 | 0.05427 | 0.05393 |
| S→Z_RISE | 0.05658 | 0.05510 | 0.05137 | 0.05092 |

CLKNAND2HS

Cell Description

2-Input NAND

$ZN = \neg(A1 \& A2)$



Function Table

| A1 | A2 | ZN |
|----|----|----|
| 0 | X | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|--------------|------------|-----------|
| CLKNAND2HSV0 | 1.80 | 0.80 |
| CLKNAND2HSV1 | 1.80 | 0.80 |
| CLKNAND2HSV2 | 1.80 | 1.20 |
| CLKNAND2HSV3 | 1.80 | 1.40 |
| CLKNAND2HSV4 | 1.80 | 1.60 |
| CLKNAND2HSV8 | 1.80 | 2.60 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V3 | V4 | V8 |
|-----|---------|---------|---------|---------|---------|---------|
| A1 | 0.00046 | 0.00057 | 0.00074 | 0.00101 | 0.00138 | 0.00267 |
| A2 | 0.00057 | 0.00073 | 0.00101 | 0.00137 | 0.00188 | 0.00362 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V3 | V4 | V8 |
|-----|---------|---------|---------|---------|---------|---------|
| A1 | 0.00110 | 0.00130 | 0.00174 | 0.00236 | 0.00309 | 0.00622 |
| A2 | 0.00105 | 0.00127 | 0.00194 | 0.00258 | 0.00332 | 0.00634 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V3 | V4 | V8 |
|----|----|----|----|----|----|
|----|----|----|----|----|----|

| | | | | | |
|------------|------------|------------|------------|------------|------------|
| 0.00011259 | 0.00012912 | 0.00015767 | 0.00026658 | 0.00029835 | 0.00065569 |
|------------|------------|------------|------------|------------|------------|

Delay Table (ns)

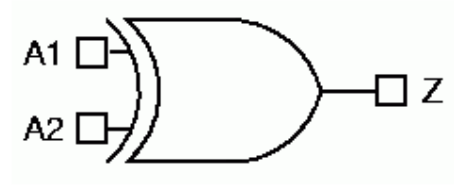
| Description | V0 | V1 | V2 | V3 | V4 | V8 |
|-------------|---------|---------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.01749 | 0.01612 | 0.01418 | 0.01400 | 0.01374 | 0.01284 |
| A1→ZN_RISE | 0.01630 | 0.01520 | 0.01407 | 0.01248 | 0.01284 | 0.01196 |
| A2→ZN_FALL | 0.01922 | 0.01809 | 0.01708 | 0.01686 | 0.01650 | 0.01536 |
| A2→ZN_RISE | 0.01834 | 0.01744 | 0.01716 | 0.01479 | 0.01547 | 0.01455 |

CLKXOR2HS

Cell Description

2-Input Exclusive OR

$$Z=(A1\wedge A2)$$



Function Table

| A2 | A1 | Z |
|----|----|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| CLKXOR2HSV0 | 1.80 | 2.20 |
| CLKXOR2HSV1 | 1.80 | 2.20 |
| CLKXOR2HSV2 | 1.80 | 2.20 |
| CLKXOR2HSV4 | 1.80 | 2.40 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00188 | 0.00203 | 0.00242 | 0.00327 |
| A2 | 0.00276 | 0.00291 | 0.00342 | 0.00451 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00195 | 0.00197 | 0.00228 | 0.00233 |
| A2 | 0.00118 | 0.00116 | 0.00134 | 0.00159 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00034263 | 0.00035144 | 0.00040984 | 0.00057332 |

Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.05235 | 0.05401 | 0.05044 | 0.05462 |
| A1→Z_RISE | 0.05063 | 0.05162 | 0.04885 | 0.05142 |
| A2→Z_FALL | 0.08187 | 0.08400 | 0.07766 | 0.07781 |
| A2→Z_RISE | 0.07833 | 0.07973 | 0.07512 | 0.07397 |

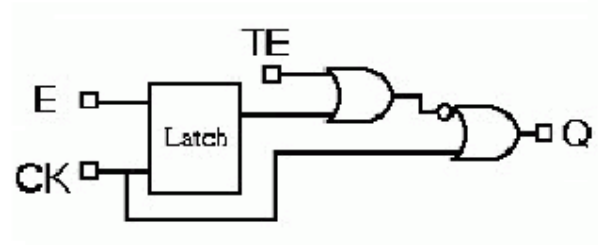
CLKLAHAQHS

Cell Description

Post-controlled negative-edge triggered clock-gating latch

$IQ = CK \ ? \ !E : \text{pre_IQ}$

$Q = CK \ ? \ 1 : (IQ \ \& \ !TE)$



Function Table

| CK<1> | CK | TE | E | Q |
|-------|----|----|---|------|
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | X | 0 |
| 1 | 1 | X | X | 1 |
| 0 | 0 | 0 | X | Q<1> |
| 0 | 0 | 1 | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|--------------|------------|-----------|
| CLKLAHAQHSV1 | 1.80 | 4.00 |
| CLKLAHAQHSV2 | 1.80 | 4.00 |
| CLKLAHAQHSV4 | 1.80 | 4.20 |
| CLKLAHAQHSV8 | 1.80 | 6.00 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 | V8 |
|-----|---------|---------|---------|---------|
| CK | 0.00234 | 0.00241 | 0.00243 | 0.00327 |
| E | 0.00126 | 0.00122 | 0.00134 | 0.00157 |
| Q | 0.00339 | 0.00365 | 0.00447 | 0.00741 |
| TE | 0.00072 | 0.00081 | 0.00077 | 0.00134 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 | V8 |
|-----|---------|---------|---------|---------|
| CK | 0.00114 | 0.00121 | 0.00114 | 0.00120 |
| E | 0.00113 | 0.00115 | 0.00121 | 0.00139 |
| TE | 0.00107 | 0.00119 | 0.00107 | 0.00127 |

Max Leakage Power (uW)

| V1 | V2 | V4 | V8 |
|------------|------------|------------|------------|
| 0.00044829 | 0.00054933 | 0.00058627 | 0.00112380 |

Delay Table (ns)

| Description | V1 | V2 | V4 | V8 |
|-------------|---------|---------|---------|---------|
| CK→Q_FALL | 0.11229 | 0.11367 | 0.12372 | 0.12395 |
| CK→Q_RISE | 0.10091 | 0.08449 | 0.10028 | 0.09215 |

Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 | V8 |
|-----|---------------|----------|----------|----------|----------|
| E | hold_FALL→CK | -0.03483 | -0.03980 | -0.02985 | -0.04476 |
| E | hold_RISE→CK | -0.00499 | 0.00498 | -0.00499 | 0.00498 |
| E | setup_FALL→CK | 0.04478 | 0.04974 | 0.03979 | 0.05970 |
| E | setup_RISE→CK | 0.01491 | 0.00499 | 0.01990 | 0.00994 |
| CK | minpwh | 0.06578 | 0.05586 | 0.07074 | 0.06081 |

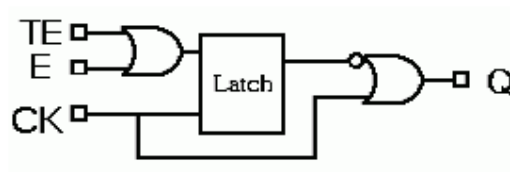
CLKLAHQHS

Cell Description

a pre-controlled negative-edge triggered clock-gating latch
for Low Power Design

$IQ = CK \text{ ? } !(TE|E) : \text{pre_IQ}$

$Q = IQ|CK$



Function Table

| CK<1> | CK | TE | E | Q |
|-------|----|----|---|------|
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | X | 0 |
| 0 | 0 | X | X | Q<1> |
| 1 | 1 | X | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| CLKLAHQHSV1 | 1.80 | 3.60 |
| CLKLAHQHSV2 | 1.80 | 3.40 |
| CLKLAHQHSV4 | 1.80 | 3.80 |
| CLKLAHQHSV8 | 1.80 | 5.00 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 | V8 |
|-----|---------|---------|---------|---------|
| CK | 0.00240 | 0.00229 | 0.00250 | 0.00306 |
| E | 0.00071 | 0.00063 | 0.00076 | 0.00079 |
| Q | 0.00221 | 0.00236 | 0.00321 | 0.00531 |
| TE | 0.00082 | 0.00072 | 0.00089 | 0.00090 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 | V8 |
|-----|---------|---------|---------|---------|
| CK | 0.00118 | 0.00123 | 0.00117 | 0.00122 |
| E | 0.00129 | 0.00119 | 0.00136 | 0.00134 |
| TE | 0.00130 | 0.00121 | 0.00138 | 0.00136 |

Max Leakage Power (uW)

| V1 | V2 | V4 | V8 |
|------------|------------|------------|------------|
| 0.00043956 | 0.00046265 | 0.00058000 | 0.00095310 |

Delay Table (ns)

| Description | V1 | V2 | V4 | V8 |
|-------------|---------|---------|---------|---------|
| CK→Q_FALL | 0.10289 | 0.09985 | 0.11192 | 0.11150 |
| CK→Q_RISE | 0.09394 | 0.08488 | 0.09737 | 0.09379 |

Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 | V8 |
|-----|---------------|----------|----------|----------|----------|
| E | hold_FALL→CK | -0.06467 | -0.07960 | -0.05970 | -0.07960 |
| E | hold_RISE→CK | -0.00000 | 0.00498 | -0.00000 | 0.00498 |
| E | setup_FALL→CK | 0.07462 | 0.08955 | 0.06964 | 0.09950 |
| E | setup_RISE→CK | 0.00994 | 0.00498 | 0.00994 | 0.00994 |
| TE | hold_FALL→CK | -0.06964 | -0.08457 | -0.06466 | -0.08457 |
| TE | hold_RISE→CK | -0.00000 | 0.00499 | -0.00000 | 0.00498 |
| TE | setup_FALL→CK | 0.07961 | 0.09452 | 0.07462 | 0.09950 |
| TE | setup_RISE→CK | 0.01492 | 0.00498 | 0.01493 | 0.00994 |
| CK | minpwh | 0.08548 | 0.09342 | 0.08554 | 0.08155 |

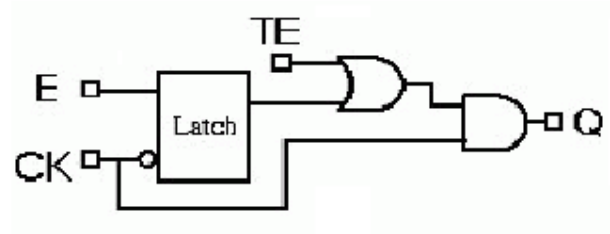
CLKLANAQHS

Cell Description

Post-controlled positive-edge triggered clock-gating latch

$IQ = !CK ? E : \text{pre_IQ}$

$Q = !CK ? 0 : (IQ \wedge TE)$



Function Table

| CK<1> | CK | TE | E | Q |
|-------|----|----|---|------|
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | X | 1 |
| 0 | 0 | X | X | 0 |
| 1 | 1 | 0 | X | Q<1> |
| 1 | 1 | 1 | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|--------------|------------|-----------|
| CLKLANAQHSV1 | 1.80 | 3.60 |
| CLKLANAQHSV2 | 1.80 | 3.80 |
| CLKLANAQHSV4 | 1.80 | 4.00 |
| CLKLANAQHSV8 | 1.80 | 5.60 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 | V8 |
|-----|---------|---------|---------|---------|
| CK | 0.00232 | 0.00252 | 0.00255 | 0.00341 |
| E | 0.00117 | 0.00122 | 0.00126 | 0.00167 |
| Q | 0.00307 | 0.00347 | 0.00445 | 0.00720 |
| TE | 0.00002 | 0.00002 | 0.00002 | 0.00007 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 | V8 |
|-----|---------|---------|---------|---------|
| CK | 0.00121 | 0.00121 | 0.00123 | 0.00120 |
| E | 0.00112 | 0.00128 | 0.00127 | 0.00143 |
| TE | 0.00118 | 0.00125 | 0.00140 | 0.00258 |

Max Leakage Power (uW)

| V1 | V2 | V4 | V8 |
|------------|------------|------------|------------|
| 0.00041253 | 0.00046262 | 0.00055609 | 0.00104070 |

Delay Table (ns)

| Description | V1 | V2 | V4 | V8 |
|-------------|---------|---------|---------|---------|
| CK→Q_FALL | 0.09503 | 0.09145 | 0.10073 | 0.10169 |
| CK→Q_RISE | 0.09691 | 0.09516 | 0.10202 | 0.10467 |

Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 | V8 |
|-----|---------------|----------|----------|----------|----------|
| E | hold_FALL→CK | -0.00994 | -0.00994 | -0.00498 | -0.00499 |
| E | hold_RISE→CK | -0.02487 | -0.01990 | -0.02486 | -0.01990 |
| E | setup_FALL→CK | 0.01990 | 0.01989 | 0.01492 | 0.01492 |
| E | setup_RISE→CK | 0.03481 | 0.02985 | 0.02985 | 0.02985 |
| CK | minpwl | 0.06086 | 0.06080 | 0.06083 | 0.06578 |

CLKLANQHS

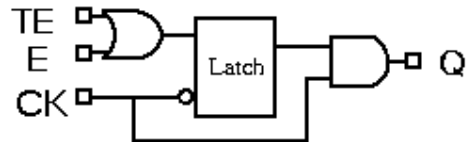
Cell Description

pre-controlled positiveedge triggered clock-gating latch for

Low Power Design

$IQ = !CK \ ? \ (TE|E)$

$Q = IQ \& CK$



Function Table

| CK<1> | CK | TE | E | Q |
|-------|----|----|---|------|
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | X | 1 |
| 0 | 0 | X | X | 0 |
| 1 | 1 | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|--------------|------------|-----------|
| CLKLANQHSV1 | 1.80 | 3.60 |
| CLKLANQHSV2 | 1.80 | 3.60 |
| CLKLANQHSV3 | 1.80 | 4.00 |
| CLKLANQHSV4 | 1.80 | 4.40 |
| CLKLANQHSV6 | 1.80 | 4.40 |
| CLKLANQHSV8 | 1.80 | 4.80 |
| CLKLANQHSV12 | 1.80 | 5.80 |
| CLKLANQHSV16 | 1.80 | 6.40 |
| CLKLANQHSV20 | 1.80 | 7.00 |
| CLKLANQHSV24 | 1.80 | 7.60 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V3 | V4 | V6 | V8 | V12 | V16 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| CK | 0.00237 | 0.00247 | 0.00244 | 0.00279 | 0.00301 | 0.00323 | 0.00247 | 0.00239 |
| E | 0.00066 | 0.00064 | 0.00065 | 0.00076 | 0.00077 | 0.00083 | 0.00068 | 0.00065 |
| Q | 0.00195 | 0.00218 | 0.00276 | 0.00296 | 0.00424 | 0.00525 | 0.00944 | 0.01151 |
| TE | 0.00074 | 0.00073 | 0.00074 | 0.00085 | 0.00089 | 0.00092 | 0.00076 | 0.00073 |

| Pin | V20 | V24 |
|-----|-----|-----|
|-----|-----|-----|

| | | |
|----|---------|---------|
| CK | 0.00245 | 0.00246 |
| E | 0.00065 | 0.00066 |
| Q | 0.01422 | 0.01621 |
| TE | 0.00073 | 0.00075 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V3 | V4 | V6 | V8 | V12 | V16 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| CK | 0.00121 | 0.00122 | 0.00123 | 0.00105 | 0.00134 | 0.00139 | 0.00123 | 0.00123 |
| E | 0.00122 | 0.00126 | 0.00122 | 0.00121 | 0.00140 | 0.00123 | 0.00127 | 0.00124 |
| TE | 0.00120 | 0.00125 | 0.00124 | 0.00129 | 0.00142 | 0.00122 | 0.00124 | 0.00121 |

| Pin | V20 | V24 |
|-----|---------|---------|
| CK | 0.00124 | 0.00124 |
| E | 0.00130 | 0.00119 |
| TE | 0.00119 | 0.00121 |

Max Leakage Power (uW)

| V1 | V2 | V3 | V4 | V6 | V8 | V12 | V16 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00042638 | 0.00043566 | 0.00054513 | 0.00056521 | 0.00079896 | 0.00108180 | 0.00139290 | 0.00176190 |

| V20 | V24 |
|------------|------------|
| 0.00211910 | 0.00249520 |

Delay Table (ns)

| Description | V1 | V2 | V3 | V4 | V6 | V8 | V12 | V16 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| CK→Q_FALL | 0.09442 | 0.09876 | 0.09844 | 0.09895 | 0.10481 | 0.09551 | 0.14648 | 0.15340 |
| CK→Q_RISE | 0.09461 | 0.10027 | 0.09909 | 0.09952 | 0.10219 | 0.09542 | 0.14593 | 0.15205 |

| Description | V20 | V24 |
|-------------|---------|---------|
| CK→Q_FALL | 0.15764 | 0.16241 |
| CK→Q_RISE | 0.15726 | 0.16134 |

Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V3 | V4 | V6 | V8 |
|-----|---------------|----------|----------|----------|----------|----------|----------|
| E | hold_FALL→CK | -0.04478 | -0.04478 | -0.03980 | -0.05472 | -0.02985 | -0.04975 |
| E | hold_RISE→CK | -0.02487 | -0.02487 | -0.02488 | -0.02985 | -0.02984 | -0.02984 |
| E | setup_FALL→CK | 0.05471 | 0.05472 | 0.05472 | 0.06965 | 0.03979 | 0.06467 |
| E | setup_RISE→CK | 0.03482 | 0.02985 | 0.02985 | 0.03981 | 0.03483 | 0.03979 |
| TE | hold_FALL→CK | -0.04975 | -0.04974 | -0.04477 | -0.05970 | -0.03483 | -0.05473 |
| TE | hold_RISE→CK | -0.02984 | -0.02984 | -0.02985 | -0.03483 | -0.03484 | -0.03482 |
| TE | setup_FALL→CK | 0.05970 | 0.05969 | 0.05473 | 0.07463 | 0.04479 | 0.06964 |
| TE | setup_RISE→CK | 0.03482 | 0.03482 | 0.03482 | 0.03981 | 0.03981 | 0.04478 |
| CK | minpwl | 0.06083 | 0.06083 | 0.06081 | 0.06576 | 0.06576 | 0.06575 |

| Pin | Requirement | V12 | V16 | V20 | V24 |
|-----|---------------|----------|----------|----------|----------|
| E | hold_FALL→CK | -0.04976 | -0.03979 | -0.04477 | -0.04478 |
| E | hold_RISE→CK | -0.02985 | -0.02487 | -0.02487 | -0.02488 |
| E | setup_FALL→CK | 0.05969 | 0.05472 | 0.05473 | 0.05473 |
| E | setup_RISE→CK | 0.03483 | 0.02985 | 0.02985 | 0.02985 |
| TE | hold_FALL→CK | -0.04974 | -0.04477 | -0.04477 | -0.04477 |
| TE | hold_RISE→CK | -0.02985 | -0.02985 | -0.02985 | -0.02985 |
| TE | setup_FALL→CK | 0.06466 | 0.05969 | 0.05473 | 0.05970 |
| TE | setup_RISE→CK | 0.03979 | 0.03484 | 0.03483 | 0.03483 |
| CK | minpwl | 0.06081 | 0.06083 | 0.06084 | 0.06085 |

DEL

Cell Description

Delay cell

$Z=I$



Function Table

| I | Z |
|---|---|
| 0 | 0 |
| 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| DELHS0 | 1.80 | 1.60 |
| DELHS1 | 1.80 | 1.60 |
| DELHS2 | 1.80 | 1.80 |
| DELHS3 | 1.80 | 1.80 |
| DELHS4 | 1.80 | 2.00 |

Pin Power (uW/MHz)

| Pin | DELHS0 | DELHS1 | DELHS2 | DELHS3 | DELHS4 |
|-----|---------|---------|---------|---------|---------|
| I | 0.00243 | 0.00263 | 0.00292 | 0.00324 | 0.00356 |

Pin Capacitance (pf)

| Pin | DELHS0 | DELHS1 | DELHS2 | DELHS3 | DELHS4 |
|-----|---------|---------|---------|---------|---------|
| I | 0.00112 | 0.00113 | 0.00112 | 0.00109 | 0.00107 |

Max Leakage Power (uW)

| DELHS0 | DELHS1 | DELHS2 | DELHS3 | DELHS4 |
|------------|------------|------------|------------|------------|
| 0.00020677 | 0.00022239 | 0.00014332 | 0.00014597 | 0.00015359 |

Delay Table (ns)

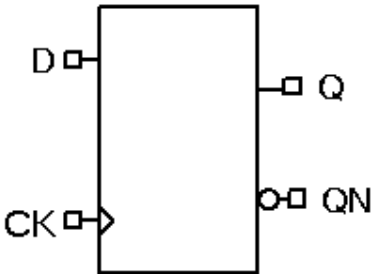
| Description | DELHS0 | DELHS1 | DELHS2 | DELHS3 | DELHS4 |
|-------------|--------|--------|--------|--------|--------|
|-------------|--------|--------|--------|--------|--------|

| | | | | | |
|----------|---------|---------|---------|---------|---------|
| I→Z_FALL | 0.07285 | 0.07420 | 0.10117 | 0.13255 | 0.16672 |
| I→Z_RISE | 0.07062 | 0.07146 | 0.09896 | 0.13273 | 0.17078 |

DHS

Cell Description

D Flip-Flop
Q = rising (CK) ? D : pre_Q
QN = !Q



Function Table

| CK<1> | CK | D | Q |
|-------|----|---|------|
| 0 | 0 | X | Q<1> |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| DHSV1 | 1.80 | 4.60 |
| DHSV2 | 1.80 | 4.80 |
| DHSV4 | 1.80 | 5.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00278 | 0.00320 | 0.00359 |
| D | 0.00134 | 0.00128 | 0.00137 |
| Q | 0.00190 | 0.00239 | 0.00332 |
| QN | 0.00192 | 0.00239 | 0.00327 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00111 | 0.00102 | 0.00132 |
| D | 0.00103 | 0.00107 | 0.00098 |

Max Leakage Power (uW)

| | | |
|----|----|----|
| V1 | V2 | V4 |
|----|----|----|

| | | |
|------------|------------|------------|
| 0.00052685 | 0.00062643 | 0.00090855 |
|------------|------------|------------|

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.09729 | 0.10323 | 0.08990 |
| CK→Q_RISE | 0.12130 | 0.11623 | 0.10913 |
| CK→QN_FALL | 0.15906 | 0.14700 | 0.13920 |
| CK→QN_RISE | 0.13716 | 0.13769 | 0.12176 |

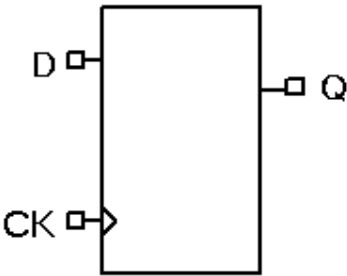
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.00995 | -0.00500 | -0.00499 |
| D | hold_RISE→CK | -0.02984 | -0.02488 | -0.02489 |
| D | setup_FALL→CK | 0.04976 | 0.04476 | 0.05473 |
| D | setup_RISE→CK | 0.03980 | 0.03483 | 0.03481 |
| CK | minpwh | 0.06970 | 0.06974 | 0.06578 |
| CK | minpwl | 0.08055 | 0.09045 | 0.08059 |

DQHS

Cell Description

D Flip-Flop, Single Output
Q = rising (CK) ? D : pre_Q



Function Table

| CK<1> | CK | D | Q |
|-------|----|---|------|
| 0 | 0 | X | Q<1> |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| DQHSV1 | 1.80 | 4.00 |
| DQHSV2 | 1.80 | 4.60 |
| DQHSV4 | 1.80 | 5.20 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00261 | 0.00336 | 0.00376 |
| D | 0.00112 | 0.00145 | 0.00162 |
| Q | 0.00251 | 0.00304 | 0.00414 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00116 | 0.00137 | 0.00134 |
| D | 0.00105 | 0.00126 | 0.00125 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00044751 | 0.00057792 | 0.00068266 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.09593 | 0.08983 | 0.08604 |
| CK→Q_RISE | 0.11515 | 0.10223 | 0.10933 |

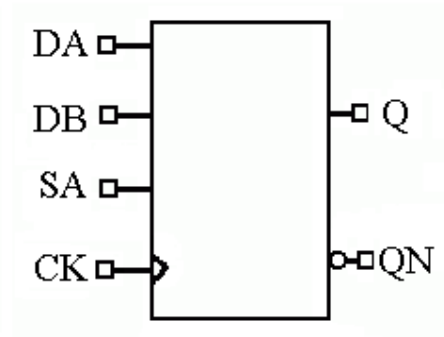
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.00994 | -0.00498 | -0.00000 |
| D | hold_RISE→CK | -0.01991 | -0.02488 | -0.02487 |
| D | setup_FALL→CK | 0.04478 | 0.04478 | 0.05471 |
| D | setup_RISE→CK | 0.02985 | 0.03483 | 0.03483 |
| CK | minpwh | 0.06576 | 0.06182 | 0.06578 |
| CK | minpwl | 0.08061 | 0.07564 | 0.08058 |

DXHS

Cell Description

D Flip-Flop with Mux Inputs
Q = rising (CK) ? (DA&SA|DB&!SA) : pre_Q
QN = !Q



Function Table

| CK<1> | CK | SA | DB | DA | Q |
|-------|----|----|----|----|------|
| 0 | 0 | X | X | X | Q<1> |
| 0 | 1 | 0 | 0 | X | 0 |
| 0 | 1 | 0 | 1 | X | 1 |
| 0 | 1 | 1 | X | 0 | 0 |
| 0 | 1 | 1 | X | 1 | 1 |
| 1 | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| DXHSV1 | 1.80 | 5.80 |
| DXHSV2 | 1.80 | 6.00 |
| DXHSV4 | 1.80 | 6.60 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00291 | 0.00306 | 0.00309 |
| DA | 0.00176 | 0.00183 | 0.00174 |
| DB | 0.00162 | 0.00170 | 0.00161 |
| Q | 0.00180 | 0.00205 | 0.00296 |
| QN | 0.00179 | 0.00202 | 0.00284 |
| SA | 0.00187 | 0.00195 | 0.00186 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00112 | 0.00113 | 0.00112 |
| DA | 0.00141 | 0.00140 | 0.00140 |

| | | | |
|----|---------|---------|---------|
| DB | 0.00140 | 0.00141 | 0.00141 |
| SA | 0.00204 | 0.00207 | 0.00204 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00085816 | 0.00094911 | 0.00116350 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.08879 | 0.08938 | 0.09790 |
| CK→Q_RISE | 0.09769 | 0.09812 | 0.10201 |
| CK→QN_FALL | 0.13066 | 0.12588 | 0.13600 |
| CK→QN_RISE | 0.12537 | 0.12191 | 0.13807 |

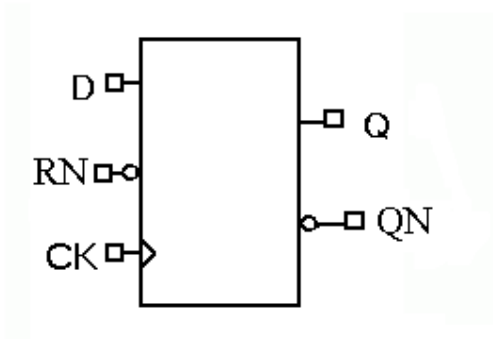
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| DA | hold_FALL→CK | -0.06964 | -0.06466 | -0.06964 |
| DA | hold_RISE→CK | -0.02488 | -0.01989 | -0.01989 |
| DA | setup_FALL→CK | 0.08954 | 0.08458 | 0.09451 |
| DA | setup_RISE→CK | 0.05969 | 0.05472 | 0.05969 |
| DB | hold_FALL→CK | -0.06467 | -0.06467 | -0.06467 |
| DB | hold_RISE→CK | -0.02984 | -0.01990 | -0.01989 |
| DB | setup_FALL→CK | 0.08456 | 0.07959 | 0.08954 |
| DB | setup_RISE→CK | 0.05970 | 0.05472 | 0.05969 |
| SA | hold_FALL→CK | -0.05471 | -0.05472 | -0.05472 |
| SA | hold_RISE→CK | -0.01988 | -0.00993 | -0.00993 |
| SA | setup_FALL→CK | 0.07462 | 0.07461 | 0.07959 |
| SA | setup_RISE→CK | 0.04973 | 0.04476 | 0.04973 |
| CK | minpwh | 0.06182 | 0.06183 | 0.06576 |
| CK | minpwl | 0.08555 | 0.08556 | 0.09047 |

DGRNHS

Cell Description

D Flip-Flop with Sync Clear
Q = rising (CK) ? D&RN : pre_Q
QN = !Q



Function Table

| CK<1> | CK | RN | D | Q |
|-------|----|----|---|------|
| 0 | 0 | X | X | Q<1> |
| 0 | 1 | 0 | X | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| DGRNHSV1 | 1.80 | 4.60 |
| DGRNHSV2 | 1.80 | 5.00 |
| DGRNHSV4 | 1.80 | 5.40 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00298 | 0.00312 | 0.00322 |
| D | 0.00063 | 0.00076 | 0.00080 |
| Q | 0.00122 | 0.00140 | 0.00224 |
| QN | 0.00126 | 0.00149 | 0.00237 |
| RN | 0.00066 | 0.00079 | 0.00083 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00140 | 0.00139 | 0.00153 |
| D | 0.00078 | 0.00098 | 0.00097 |
| RN | 0.00090 | 0.00096 | 0.00101 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00056948 | 0.00059438 | 0.00085729 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.12543 | 0.12258 | 0.13221 |
| CK→Q_RISE | 0.11653 | 0.10854 | 0.12245 |
| CK→QN_FALL | 0.08304 | 0.07597 | 0.08431 |
| CK→QN_RISE | 0.09381 | 0.09205 | 0.09754 |

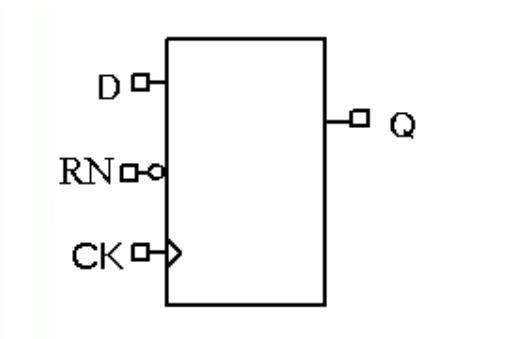
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.00000 | 0.00497 | 0.00499 |
| D | hold_RISE→CK | -0.03483 | -0.02985 | -0.03481 |
| D | setup_FALL→CK | 0.04478 | 0.04476 | 0.04974 |
| D | setup_RISE→CK | 0.06467 | 0.06466 | 0.06467 |
| RN | hold_FALL→CK | -0.00498 | -0.00000 | -0.00000 |
| RN | hold_RISE→CK | -0.03980 | -0.03482 | -0.03481 |
| RN | setup_FALL→CK | 0.04975 | 0.06466 | 0.06964 |
| RN | setup_RISE→CK | 0.06468 | 0.06469 | 0.06964 |
| CK | minpwh | 0.06581 | 0.06183 | 0.06973 |
| CK | minpwl | 0.08057 | 0.07567 | 0.07567 |

DGRNQHS

Cell Description

D Flip-Flop with Sync Clear
Q = rising (CK) ? D&RN : pre_Q



Function Table

| CK<1> | CK | RN | D | Q |
|-------|----|----|---|------|
| 0 | 0 | X | X | Q<1> |
| 0 | 1 | 0 | X | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| DGRNQHSV1 | 1.80 | 4.40 |
| DGRNQHSV2 | 1.80 | 4.60 |
| DGRNQHSV4 | 1.80 | 4.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00310 | 0.00313 | 0.00324 |
| D | 0.00068 | 0.00076 | 0.00076 |
| Q | 0.00347 | 0.00387 | 0.00473 |
| RN | 0.00071 | 0.00078 | 0.00078 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00139 | 0.00148 | 0.00149 |
| D | 0.00079 | 0.00089 | 0.00084 |
| RN | 0.00091 | 0.00095 | 0.00090 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00048637 | 0.00053011 | 0.00069898 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.11824 | 0.11403 | 0.11795 |
| CK→Q_RISE | 0.10144 | 0.09611 | 0.09706 |

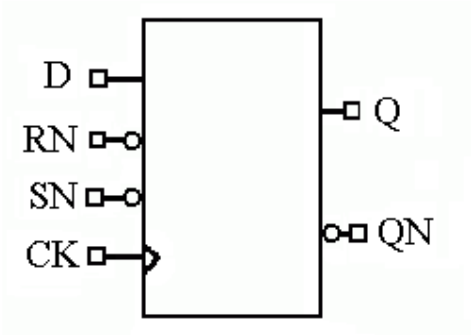
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.00499 | -0.00994 | -0.00498 |
| D | hold_RISE→CK | -0.04478 | -0.03981 | -0.03979 |
| D | setup_FALL→CK | 0.04977 | 0.05473 | 0.05472 |
| D | setup_RISE→CK | 0.06467 | 0.06965 | 0.07463 |
| RN | hold_FALL→CK | -0.00994 | -0.00994 | -0.00500 |
| RN | hold_RISE→CK | -0.04478 | -0.03979 | -0.03981 |
| RN | setup_FALL→CK | 0.05471 | 0.06466 | 0.06965 |
| RN | setup_RISE→CK | 0.06965 | 0.06965 | 0.07463 |
| CK | minpwh | 0.05781 | 0.05391 | 0.05391 |
| CK | minpwl | 0.09048 | 0.08555 | 0.08554 |

DGRSNHS

Cell Description

D Flip-Flop with Sync Clear and Set
Q = rising (CK) ? RN&(D!SN) : pre_Q
QN = !Q



Function Table

| CK<1> | CK | SN | D | RN | Q |
|-------|----|----|---|----|------|
| 0 | 0 | X | X | X | Q<1> |
| 0 | 1 | 0 | X | 0 | 0 |
| 0 | 1 | 0 | X | 1 | 1 |
| 0 | 1 | 1 | 0 | X | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| DGRSNHSV1 | 1.80 | 5.80 |
| DGRSNHSV2 | 1.80 | 6.00 |
| DGRSNHSV4 | 1.80 | 6.40 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00325 | 0.00351 | 0.00351 |
| D | 0.00035 | 0.00039 | 0.00039 |
| Q | 0.00146 | 0.00173 | 0.00255 |
| QN | 0.00148 | 0.00175 | 0.00270 |
| RN | 0.00116 | 0.00128 | 0.00128 |
| SN | 0.00118 | 0.00128 | 0.00128 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00136 | 0.00171 | 0.00171 |

| | | | |
|----|---------|---------|---------|
| D | 0.00086 | 0.00099 | 0.00100 |
| RN | 0.00111 | 0.00124 | 0.00124 |
| SN | 0.00139 | 0.00136 | 0.00136 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00065306 | 0.00077084 | 0.00099459 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.12870 | 0.12095 | 0.13327 |
| CK→Q_RISE | 0.11445 | 0.11251 | 0.13234 |
| CK→QN_FALL | 0.08215 | 0.07886 | 0.08796 |
| CK→QN_RISE | 0.09809 | 0.09108 | 0.09478 |

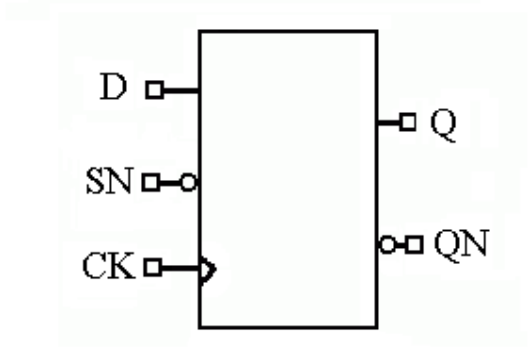
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.01991 | -0.01492 | -0.00994 |
| D | hold_RISE→CK | -0.04478 | -0.03980 | -0.03483 |
| D | setup_FALL→CK | 0.07961 | 0.07461 | 0.07960 |
| D | setup_RISE→CK | 0.07464 | 0.06467 | 0.06965 |
| RN | hold_FALL→CK | -0.00499 | -0.00994 | -0.00499 |
| RN | hold_RISE→CK | -0.05472 | -0.04478 | -0.04477 |
| RN | setup_FALL→CK | 0.05970 | 0.07463 | 0.07960 |
| RN | setup_RISE→CK | 0.08458 | 0.07959 | 0.07960 |
| SN | hold_FALL→CK | -0.06964 | -0.06467 | -0.05970 |
| SN | hold_RISE→CK | -0.03482 | -0.03482 | -0.02985 |
| SN | setup_FALL→CK | 0.09950 | 0.09453 | 0.09452 |
| SN | setup_RISE→CK | 0.09950 | 0.09453 | 0.09950 |
| CK | minpwh | 0.06574 | 0.06176 | 0.07763 |
| CK | minpwl | 0.09045 | 0.08059 | 0.08058 |

DGSNHS

Cell Description

D Flip-Flop with Sync Set
Q = rising (CK) ? (D!SN) : pre_Q
QN = !Q



Function Table

| CK<1> | CK | SN | D | Q |
|-------|----|----|---|------|
| 0 | 0 | X | X | Q<1> |
| 0 | 1 | 0 | X | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| DGSNHSV1 | 1.80 | 5.20 |
| DGSNHSV2 | 1.80 | 5.40 |
| DGSNHSV4 | 1.80 | 6.00 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00288 | 0.00331 | 0.00356 |
| D | 0.00059 | 0.00066 | 0.00066 |
| Q | 0.00111 | 0.00136 | 0.00223 |
| QN | 0.00109 | 0.00135 | 0.00224 |
| SN | 0.00141 | 0.00151 | 0.00151 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00111 | 0.00132 | 0.00175 |
| D | 0.00085 | 0.00088 | 0.00087 |
| SN | 0.00108 | 0.00109 | 0.00109 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00058532 | 0.00067927 | 0.00098312 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.14174 | 0.12802 | 0.13416 |
| CK→Q_RISE | 0.12944 | 0.12218 | 0.13020 |
| CK→QN_FALL | 0.09356 | 0.08721 | 0.08975 |
| CK→QN_RISE | 0.10908 | 0.09718 | 0.09200 |

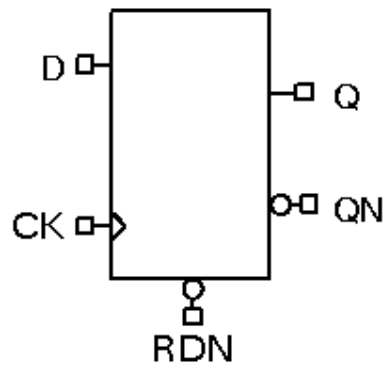
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.00000 | -0.00000 | -0.00499 |
| D | hold_RISE→CK | -0.01990 | -0.02487 | -0.02489 |
| D | setup_FALL→CK | 0.04975 | 0.05473 | 0.06965 |
| D | setup_RISE→CK | 0.03980 | 0.04478 | 0.04976 |
| SN | hold_FALL→CK | -0.05473 | -0.05970 | -0.05473 |
| SN | hold_RISE→CK | -0.01991 | -0.02488 | -0.02986 |
| SN | setup_FALL→CK | 0.07462 | 0.08458 | 0.08459 |
| SN | setup_RISE→CK | 0.07463 | 0.07961 | 0.09454 |
| CK | minpwh | 0.07368 | 0.06970 | 0.07766 |
| CK | minpwl | 0.08064 | 0.08554 | 0.07565 |

DRNHS

Cell Description

D Flip-Flop with Async Clear
Q = !RDN ? 0 : rising (CK) ? D : pre_Q
QN = !Q



Function Table

| RDN | CK<1> | CK | D | Q |
|-----|-------|----|---|------|
| 0 | X | X | X | 0 |
| 1 | 0 | 0 | X | Q<1> |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| DRNHSV1 | 1.80 | 5.20 |
| DRNHSV2 | 1.80 | 5.20 |
| DRNHSV4 | 1.80 | 6.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00288 | 0.00295 | 0.00376 |
| D | 0.00061 | 0.00065 | 0.00076 |
| Q | 0.00178 | 0.00223 | 0.00331 |
| QN | 0.00187 | 0.00230 | 0.00348 |
| RDN | 0.00066 | 0.00070 | 0.00083 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00112 | 0.00110 | 0.00140 |
| D | 0.00087 | 0.00084 | 0.00139 |
| RDN | 0.00260 | 0.00273 | 0.00376 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00068193 | 0.00078218 | 0.00125490 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.15072 | 0.15089 | 0.15057 |
| CK→Q_RISE | 0.14285 | 0.14006 | 0.14745 |
| RDN→Q_FALL | 0.04978 | 0.05456 | 0.07245 |
| CK→QN_FALL | 0.09790 | 0.09733 | 0.10665 |
| CK→QN_RISE | 0.11363 | 0.11560 | 0.10735 |
| RDN→QN_RISE | 0.11437 | 0.12313 | 0.15387 |

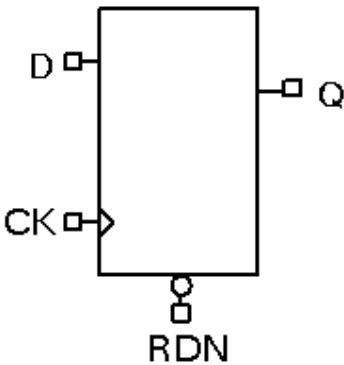
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | 0.00996 | 0.01493 | 0.01493 |
| D | hold_RISE→CK | -0.02985 | -0.02488 | -0.01989 |
| D | setup_FALL→CK | 0.03482 | 0.03980 | 0.03980 |
| D | setup_RISE→CK | 0.05472 | 0.05473 | 0.04974 |
| RDN | setup_RISE→CK | 0.05970 | 0.05970 | 0.05473 |
| RDN | hold_RISE→CK | -0.04477 | -0.04477 | -0.03980 |
| CK | minpwh | 0.08159 | 0.08157 | 0.08945 |
| CK | minpwl | 0.08554 | 0.08551 | 0.08059 |
| RDN | minpwl | 0.06576 | 0.07759 | 0.12112 |

DRNQHS

Cell Description

D Flip-Flop with Async Clear, Single Output
Q = !RDN ? 0 : rising (CK) ? D : pre_Q



Function Table

| RDN | CK<1> | CK | D | Q |
|-----|-------|----|---|------|
| 0 | X | X | X | 0 |
| 1 | 0 | 0 | X | Q<1> |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| DRNQHSV1 | 1.80 | 5.00 |
| DRNQHSV2 | 1.80 | 5.00 |
| DRNQHSV4 | 1.80 | 6.20 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00292 | 0.00299 | 0.00372 |
| D | 0.00062 | 0.00065 | 0.00075 |
| Q | 0.00423 | 0.00477 | 0.00632 |
| RDN | 0.00067 | 0.00071 | 0.00083 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00113 | 0.00113 | 0.00141 |
| D | 0.00078 | 0.00084 | 0.00140 |
| RDN | 0.00259 | 0.00270 | 0.00376 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00061613 | 0.00068953 | 0.00096400 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.14570 | 0.14150 | 0.13047 |
| CK→Q_RISE | 0.13180 | 0.12217 | 0.11671 |
| RDN→Q_FALL | 0.05001 | 0.05332 | 0.07001 |

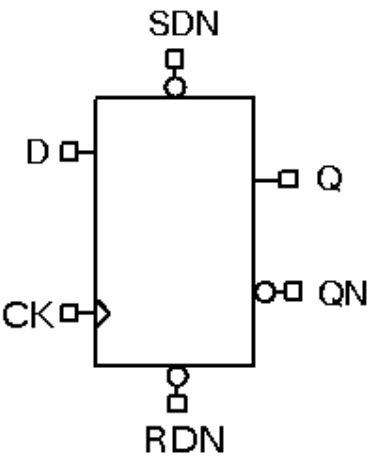
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | 0.00497 | 0.00497 | 0.00994 |
| D | hold_RISE→CK | -0.02986 | -0.02986 | -0.02487 |
| D | setup_FALL→CK | 0.03484 | 0.03979 | 0.03981 |
| D | setup_RISE→CK | 0.05474 | 0.05472 | 0.04974 |
| RDN | setup_RISE→CK | 0.05970 | 0.05969 | 0.05471 |
| RDN | hold_RISE→CK | -0.04478 | -0.04477 | -0.03979 |
| CK | minpwh | 0.07366 | 0.06977 | 0.06971 |
| CK | minpwl | 0.08557 | 0.08552 | 0.08058 |
| RDN | minpwl | 0.06177 | 0.06966 | 0.09739 |

DRSNHS

Cell Description

D Flip-Flop with Async Clear and Set
 $Q = \text{!SDN} \text{ ? } 1 : \text{!RDN} \text{ ? } 0 : \text{rising (CK) ? D : pre_Q}$
 $QN = \text{!Q}$



Function Table

| RDN | SDN | CK<1> | CK | D | Q |
|-----|-----|-------|----|---|------|
| 0 | 0 | X | X | X | 1 |
| 0 | 1 | X | X | X | 0 |
| 1 | 0 | X | X | X | 1 |
| 1 | 1 | 0 | 0 | X | Q<1> |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| DRSNHSV1 | 1.80 | 6.40 |
| DRSNHSV2 | 1.80 | 7.00 |
| DRSNHSV4 | 1.80 | 8.20 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00339 | 0.00359 | 0.00448 |
| D | 0.00089 | 0.00099 | 0.00104 |
| Q | 0.00254 | 0.00296 | 0.00396 |
| QN | 0.00255 | 0.00301 | 0.00407 |
| RDN | 0.00113 | 0.00145 | 0.00179 |
| SDN | 0.00046 | 0.00053 | 0.00061 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00103 | 0.00106 | 0.00182 |

| | | | |
|-----|---------|---------|---------|
| D | 0.00104 | 0.00106 | 0.00113 |
| RDN | 0.00102 | 0.00106 | 0.00099 |
| SDN | 0.00180 | 0.00192 | 0.00242 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00075638 | 0.00091770 | 0.00124250 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.17241 | 0.16673 | 0.14530 |
| CK→Q_RISE | 0.15562 | 0.14097 | 0.12741 |
| RDN→Q_FALL | 0.15925 | 0.14950 | 0.15077 |
| SDN→Q_FALL | 0.15370 | 0.13247 | 0.11735 |
| SDN→Q_RISE | 0.09745 | 0.10081 | 0.10671 |
| CK→QN_FALL | 0.11762 | 0.10728 | 0.09566 |
| CK→QN_RISE | 0.13665 | 0.13149 | 0.10240 |
| RDN→QN_RISE | 0.12176 | 0.11375 | 0.11034 |
| SDN→QN_FALL | 0.06564 | 0.06979 | 0.07670 |
| SDN→QN_RISE | 0.11618 | 0.09675 | 0.07697 |

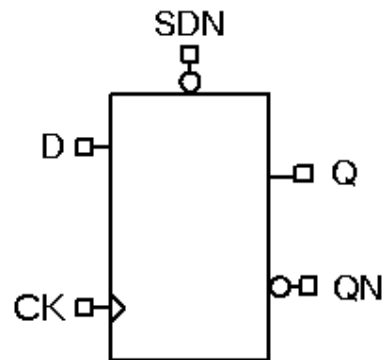
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|------------------------|----------|----------|----------|
| D | hold_FALL→CK | 0.00996 | 0.00994 | -0.00000 |
| D | hold_RISE→CK | -0.02985 | -0.02985 | -0.02985 |
| D | setup_FALL→CK | 0.04974 | 0.05471 | 0.07462 |
| D | setup_RISE→CK | 0.08457 | 0.08456 | 0.08457 |
| RDN | setup_RISE→CK | 0.06467 | 0.06964 | 0.06965 |
| RDN | hold_RISE→CK | -0.02487 | -0.02488 | -0.03483 |
| SDN | setup_RISE→CK | -0.02489 | -0.02986 | -0.00994 |
| SDN | hold_RISE→CK | 0.04479 | 0.05474 | 0.03979 |
| SDN | non_seq_hold_RISE→RDN | -0.09949 | -0.07462 | -0.05969 |
| SDN | non_seq_setup_RISE→RDN | 0.11443 | 0.09452 | 0.08456 |
| CK | minpwh | 0.09745 | 0.08559 | 0.07760 |
| CK | minpwl | 0.09546 | 0.10039 | 0.08062 |
| RDN | minpwl | 0.08948 | 0.08157 | 0.09348 |
| SDN | minpwl | 0.06579 | 0.06973 | 0.08159 |

DSNHS

Cell Description

D Flip-Flop with Async Set
Q = !SDN ? 1 : rising (CK) ? D : pre_Q
QN = !Q



Function Table

| SDN | CK<1> | CK | D | Q |
|-----|-------|----|---|------|
| 0 | X | X | X | 1 |
| 1 | 0 | 0 | X | Q<1> |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| DSNHSV1 | 1.80 | 5.20 |
| DSNHSV2 | 1.80 | 5.40 |
| DSNHSV4 | 1.80 | 7.00 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00297 | 0.00330 | 0.00412 |
| D | 0.00096 | 0.00111 | 0.00153 |
| Q | 0.00224 | 0.00265 | 0.00368 |
| QN | 0.00220 | 0.00261 | 0.00364 |
| SDN | 0.00040 | 0.00043 | 0.00057 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00113 | 0.00112 | 0.00136 |
| D | 0.00095 | 0.00117 | 0.00159 |
| SDN | 0.00168 | 0.00160 | 0.00208 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00068539 | 0.00089282 | 0.00117540 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.15159 | 0.13955 | 0.13786 |
| CK→Q_RISE | 0.14268 | 0.13272 | 0.12657 |
| SDN→Q_RISE | 0.09973 | 0.10177 | 0.11034 |
| CK→QN_FALL | 0.09895 | 0.09339 | 0.09181 |
| CK→QN_RISE | 0.11712 | 0.11227 | 0.10316 |
| SDN→QN_FALL | 0.05922 | 0.06230 | 0.07351 |

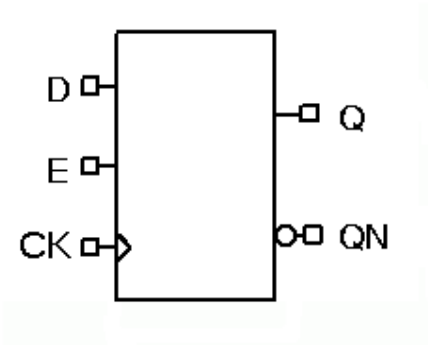
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | 0.00994 | 0.00994 | 0.00994 |
| D | hold_RISE→CK | -0.02489 | -0.01494 | -0.01990 |
| D | setup_FALL→CK | 0.03482 | 0.03482 | 0.03482 |
| D | setup_RISE→CK | 0.04975 | 0.03981 | 0.04477 |
| SDN | setup_RISE→CK | -0.03980 | -0.02984 | -0.03482 |
| SDN | hold_RISE→CK | 0.05970 | 0.05472 | 0.05970 |
| CK | minpwh | 0.08160 | 0.07766 | 0.07369 |
| CK | minpwl | 0.08064 | 0.08065 | 0.07563 |
| SDN | minpwl | 0.06573 | 0.06970 | 0.08158 |

EDHS

Cell Description

Enable D Flip-Flop
Q = rising (CK) ? (E ? D : pre_Q) : pre_Q
QN = !Q



Function Table

| CK<1> | CK | E | Q | D | Q |
|-------|----|---|---|---|------|
| 0 | 0 | X | X | X | Q<1> |
| 0 | 1 | 0 | 0 | X | 0 |
| 0 | 1 | 0 | 1 | X | 1 |
| 0 | 1 | 1 | X | 0 | 0 |
| 0 | 1 | 1 | X | 1 | 1 |
| 1 | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| EDHSV1 | 1.80 | 6.80 |
| EDHSV2 | 1.80 | 6.80 |
| EDHSV4 | 1.80 | 7.00 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00295 | 0.00298 | 0.00301 |
| D | 0.00118 | 0.00119 | 0.00124 |
| E | 0.00088 | 0.00088 | 0.00089 |
| Q | 0.00230 | 0.00259 | 0.00351 |
| QN | 0.00228 | 0.00257 | 0.00346 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00104 | 0.00104 | 0.00104 |
| D | 0.00090 | 0.00090 | 0.00090 |
| E | 0.00234 | 0.00234 | 0.00232 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00066799 | 0.00073396 | 0.00102720 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.10915 | 0.10405 | 0.11074 |
| CK→Q_RISE | 0.12086 | 0.11617 | 0.11990 |
| CK→QN_FALL | 0.16706 | 0.16302 | 0.17680 |
| CK→QN_RISE | 0.16254 | 0.16024 | 0.18156 |

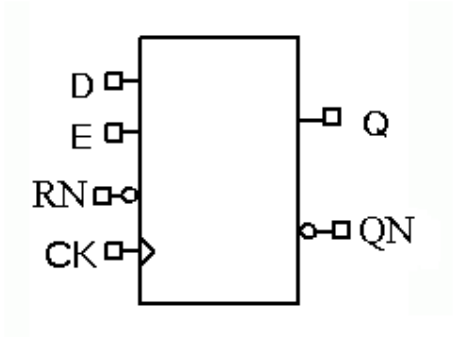
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.05472 | -0.05472 | -0.05970 |
| D | hold_RISE→CK | -0.05472 | -0.04974 | -0.04974 |
| D | setup_FALL→CK | 0.08955 | 0.09950 | 0.10446 |
| D | setup_RISE→CK | 0.06467 | 0.06467 | 0.06468 |
| E | hold_FALL→CK | -0.08456 | -0.08456 | -0.08456 |
| E | hold_RISE→CK | -0.08956 | -0.08956 | -0.09453 |
| E | setup_FALL→CK | 0.09452 | 0.09453 | 0.09452 |
| E | setup_RISE→CK | 0.11442 | 0.12437 | 0.12935 |
| CK | minpwh | 0.07368 | 0.06973 | 0.07371 |
| CK | minpwl | 0.07567 | 0.07568 | 0.08059 |

EDGRNHS

Cell Description

Enable D Flip-Flop with Sync Clear
 $Q = \text{rising}(\text{CK}) ? (!\text{RN} ? 0 : \text{E} ? \text{D} : \text{pre_Q}) : \text{pre_Q}$
 $\text{QN} = !Q$



Function Table

| CK<1> | CK | E | Q | D | RN | Q |
|-------|----|---|---|---|----|------|
| 0 | 0 | X | X | X | X | Q<1> |
| 0 | 1 | 0 | 0 | X | X | 0 |
| 0 | 1 | 0 | 1 | X | 0 | 0 |
| 0 | 1 | 0 | 1 | X | 1 | 1 |
| 0 | 1 | 1 | X | 0 | X | 0 |
| 0 | 1 | 1 | X | 1 | 0 | 0 |
| 0 | 1 | 1 | X | 1 | 1 | 1 |
| 1 | X | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| EDGRNHSV1 | 1.80 | 6.60 |
| EDGRNHSV2 | 1.80 | 6.80 |
| EDGRNHSV4 | 1.80 | 7.40 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00308 | 0.00326 | 0.00332 |
| D | 0.00068 | 0.00069 | 0.00064 |
| E | 0.00082 | 0.00081 | 0.00082 |
| Q | 0.00122 | 0.00161 | 0.00247 |
| QN | 0.00123 | 0.00160 | 0.00246 |
| RN | 0.00113 | 0.00115 | 0.00108 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|----|----|----|
|-----|----|----|----|

| | | | |
|----|---------|---------|---------|
| CK | 0.00107 | 0.00108 | 0.00109 |
| D | 0.00090 | 0.00091 | 0.00091 |
| E | 0.00232 | 0.00232 | 0.00231 |
| RN | 0.00100 | 0.00100 | 0.00100 |

Max Leakage Power (uW)

| | | |
|------------|------------|------------|
| V1 | V2 | V4 |
| 0.00067997 | 0.00075586 | 0.00096182 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.11690 | 0.11563 | 0.12200 |
| CK→Q_RISE | 0.12688 | 0.12585 | 0.13131 |
| CK→QN_FALL | 0.17112 | 0.17113 | 0.18611 |
| CK→QN_RISE | 0.16613 | 0.16823 | 0.18680 |

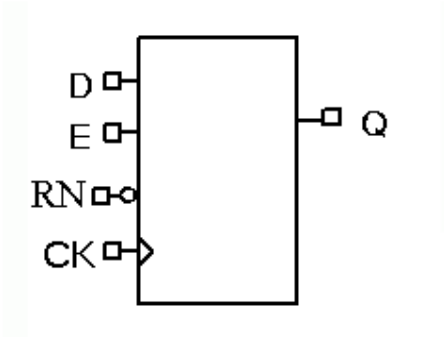
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.06466 | -0.06466 | -0.05472 |
| D | hold_RISE→CK | -0.06468 | -0.05969 | -0.05472 |
| D | setup_FALL→CK | 0.09949 | 0.09949 | 0.10447 |
| D | setup_RISE→CK | 0.07461 | 0.07461 | 0.06964 |
| E | hold_FALL→CK | -0.07461 | -0.06965 | -0.06466 |
| E | hold_RISE→CK | -0.06965 | -0.06964 | -0.06468 |
| E | setup_FALL→CK | 0.07960 | 0.07959 | 0.07462 |
| E | setup_RISE→CK | 0.07463 | 0.07463 | 0.07463 |
| RN | hold_FALL→CK | -0.06469 | -0.05971 | -0.05473 |
| RN | hold_RISE→CK | -0.07462 | -0.07461 | -0.06467 |
| RN | setup_FALL→CK | 0.08956 | 0.09452 | 0.09950 |
| RN | setup_RISE→CK | 0.07960 | 0.07960 | 0.07959 |
| CK | minpwh | 0.07764 | 0.07767 | 0.08157 |
| CK | minpwl | 0.08557 | 0.08556 | 0.09049 |

EDGRNQHS

Cell Description

Enable D Flip-Flop with Sync Clear
Q = rising (CK) ? (!RN ? 0 : E ? D : pre_Q) : pre_Q



Function Table

| CK<1> | CK | E | Q | D | RN | Q |
|-------|----|---|---|---|----|------|
| 0 | 0 | X | X | X | X | Q<1> |
| 0 | 1 | 0 | 0 | X | X | 0 |
| 0 | 1 | 0 | 1 | X | 0 | 0 |
| 0 | 1 | 0 | 1 | X | 1 | 1 |
| 0 | 1 | 1 | X | 0 | X | 0 |
| 0 | 1 | 1 | X | 1 | 0 | 0 |
| 0 | 1 | 1 | X | 1 | 1 | 1 |
| 1 | X | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| EDGRNQHSV1 | 1.80 | 6.20 |
| EDGRNQHSV2 | 1.80 | 6.40 |
| EDGRNQHSV4 | 1.80 | 6.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00301 | 0.00316 | 0.00324 |
| D | 0.00068 | 0.00068 | 0.00069 |
| E | 0.00089 | 0.00082 | 0.00091 |
| Q | 0.00371 | 0.00444 | 0.00532 |
| RN | 0.00113 | 0.00114 | 0.00115 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00107 | 0.00108 | 0.00108 |

| | | | |
|----|---------|---------|---------|
| D | 0.00089 | 0.00089 | 0.00090 |
| E | 0.00255 | 0.00232 | 0.00259 |
| RN | 0.00099 | 0.00099 | 0.00100 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00063366 | 0.00065351 | 0.00076269 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.11500 | 0.11446 | 0.12680 |
| CK→Q_RISE | 0.12425 | 0.12264 | 0.12904 |

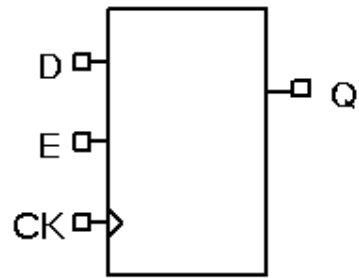
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.06964 | -0.06466 | -0.06466 |
| D | hold_RISE→CK | -0.06468 | -0.05970 | -0.05969 |
| D | setup_FALL→CK | 0.09949 | 0.10446 | 0.10448 |
| D | setup_RISE→CK | 0.07461 | 0.07462 | 0.07462 |
| E | hold_FALL→CK | -0.07461 | -0.06965 | -0.06966 |
| E | hold_RISE→CK | -0.06965 | -0.06966 | -0.06965 |
| E | setup_FALL→CK | 0.08456 | 0.07959 | 0.07959 |
| E | setup_RISE→CK | 0.07462 | 0.07463 | 0.07961 |
| RN | hold_FALL→CK | -0.06468 | -0.05970 | -0.05970 |
| RN | hold_RISE→CK | -0.07462 | -0.07463 | -0.06965 |
| RN | setup_FALL→CK | 0.08955 | 0.09452 | 0.09453 |
| RN | setup_RISE→CK | 0.07960 | 0.07959 | 0.07960 |
| CK | minpwh | 0.07372 | 0.07372 | 0.07765 |
| CK | minpwl | 0.08059 | 0.08553 | 0.08552 |

EDQHS

Cell Description

Enable D Flip-Flop, Single Output
Q = rising (CK) ? (E ? D : pre_Q) : pre_Q



Function Table

| CK<1> | CK | E | Q | D | Q |
|-------|----|---|---|---|------|
| 0 | 0 | X | X | X | Q<1> |
| 0 | 1 | 0 | 0 | X | 0 |
| 0 | 1 | 0 | 1 | X | 1 |
| 0 | 1 | 1 | X | 0 | 0 |
| 0 | 1 | 1 | X | 1 | 1 |
| 1 | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| EDQHSV1 | 1.80 | 6.20 |
| EDQHSV2 | 1.80 | 6.20 |
| EDQHSV4 | 1.80 | 6.60 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00294 | 0.00299 | 0.00304 |
| D | 0.00117 | 0.00119 | 0.00123 |
| E | 0.00088 | 0.00088 | 0.00089 |
| Q | 0.00471 | 0.00521 | 0.00629 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00103 | 0.00104 | 0.00106 |
| D | 0.00090 | 0.00090 | 0.00091 |
| E | 0.00234 | 0.00234 | 0.00234 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00060704 | 0.00065000 | 0.00077584 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.10610 | 0.10406 | 0.11322 |
| CK→Q_RISE | 0.11904 | 0.11545 | 0.12184 |

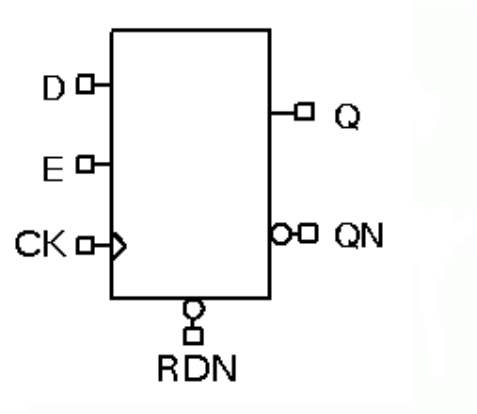
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.05473 | -0.05472 | -0.05472 |
| D | hold_RISE→CK | -0.05472 | -0.04974 | -0.04975 |
| D | setup_FALL→CK | 0.08955 | 0.09454 | 0.09950 |
| D | setup_RISE→CK | 0.06467 | 0.06466 | 0.06468 |
| E | hold_FALL→CK | -0.08954 | -0.08456 | -0.08459 |
| E | hold_RISE→CK | -0.08956 | -0.08956 | -0.08956 |
| E | setup_FALL→CK | 0.09451 | 0.09451 | 0.09454 |
| E | setup_RISE→CK | 0.11442 | 0.11940 | 0.12437 |
| CK | minpwh | 0.06973 | 0.06973 | 0.07368 |
| CK | minpwl | 0.07567 | 0.07567 | 0.07568 |

EDRNHS

Cell Description

Enable D Flip-Flop with Async Reset
 $Q = !RDN ? 0 : \text{rising}(CK) ? (E ? D : \text{pre_}Q) : \text{pre_}Q$
 $QN = !Q$



Function Table

| RDN | CK<1> | CK | E | Q | D | Q |
|-----|-------|----|---|---|---|------|
| 0 | X | X | X | X | X | 0 |
| 1 | 0 | 0 | X | X | X | Q<1> |
| 1 | 0 | 1 | 0 | 0 | X | 0 |
| 1 | 0 | 1 | 0 | 1 | X | 1 |
| 1 | 0 | 1 | 1 | X | 0 | 0 |
| 1 | 0 | 1 | 1 | X | 1 | 1 |
| 1 | 1 | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| EDRNHSV1 | 1.80 | 7.80 |
| EDRNHSV2 | 1.80 | 8.40 |
| EDRNHSV4 | 1.80 | 8.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00323 | 0.00341 | 0.00345 |
| D | 0.00088 | 0.00089 | 0.00090 |
| E | 0.00154 | 0.00155 | 0.00155 |
| Q | 0.00361 | 0.00413 | 0.00504 |
| QN | 0.00363 | 0.00415 | 0.00506 |
| RDN | 0.00066 | 0.00068 | 0.00069 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00108 | 0.00109 | 0.00109 |

| | | | |
|-----|---------|---------|---------|
| D | 0.00094 | 0.00097 | 0.00097 |
| E | 0.00226 | 0.00224 | 0.00224 |
| RDN | 0.00356 | 0.00383 | 0.00384 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00081440 | 0.00083065 | 0.00108540 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.12506 | 0.12450 | 0.13146 |
| CK→Q_RISE | 0.12464 | 0.12582 | 0.13200 |
| RDN→Q_FALL | 0.07585 | 0.08377 | 0.08762 |
| CK→QN_FALL | 0.17394 | 0.17953 | 0.19417 |
| CK→QN_RISE | 0.17813 | 0.18573 | 0.20291 |
| RDN→QN_RISE | 0.12322 | 0.13927 | 0.15099 |

Timing Constraints (ns)

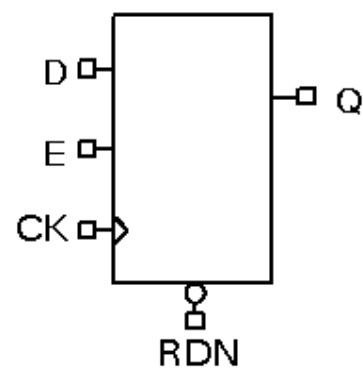
| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.06965 | -0.06965 | -0.06469 |
| D | hold_RISE→CK | -0.06466 | -0.06467 | -0.06466 |
| D | setup_FALL→CK | 0.09950 | 0.10945 | 0.10945 |
| D | setup_RISE→CK | 0.07461 | 0.07959 | 0.07960 |
| E | hold_FALL→CK | -0.07461 | -0.07461 | -0.06964 |
| E | hold_RISE→CK | -0.06966 | -0.06966 | -0.06966 |
| E | setup_FALL→CK | 0.08455 | 0.08456 | 0.07959 |
| E | setup_RISE→CK | 0.07462 | 0.07961 | 0.07961 |
| RDN | setup_RISE→CK | 0.08953 | 0.08954 | 0.08954 |
| RDN | hold_RISE→CK | -0.08457 | -0.08457 | -0.08458 |
| CK | minpwh | 0.07769 | 0.07769 | 0.08553 |
| CK | minpwl | 0.08559 | 0.09053 | 0.09051 |
| RDN | minpwl | 0.07370 | 0.08555 | 0.09741 |

EDRNQHS

Cell Description

Enable D Flip-Flop with Async Clear, Single Output

Q = !RDN ? 0 : rising (CK) ? (E ? D : pre_Q) : pre_Q



Function Table

| RDN | CK<1> | CK | E | Q | D | Q |
|-----|-------|----|---|---|---|------|
| 0 | X | X | X | X | X | 0 |
| 1 | 0 | 0 | X | X | X | Q<1> |
| 1 | 0 | 1 | 0 | 0 | X | 0 |
| 1 | 0 | 1 | 0 | 1 | X | 1 |
| 1 | 0 | 1 | 1 | X | 0 | 0 |
| 1 | 0 | 1 | 1 | X | 1 | 1 |
| 1 | 1 | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| EDRNQH1SV1 | 1.80 | 7.60 |
| EDRNQH1SV2 | 1.80 | 8.20 |
| EDRNQH1SV4 | 1.80 | 8.40 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00323 | 0.00342 | 0.00344 |
| D | 0.00089 | 0.00091 | 0.00091 |
| E | 0.00155 | 0.00157 | 0.00157 |
| Q | 0.00776 | 0.00871 | 0.00957 |
| RDN | 0.00067 | 0.00069 | 0.00069 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00114 | 0.00114 | 0.00114 |
| D | 0.00096 | 0.00096 | 0.00096 |

| | | | |
|-----|---------|---------|---------|
| E | 0.00231 | 0.00231 | 0.00231 |
| RDN | 0.00358 | 0.00385 | 0.00386 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00075351 | 0.00075500 | 0.00084286 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.12204 | 0.12328 | 0.13152 |
| CK→Q_RISE | 0.12273 | 0.12537 | 0.13119 |
| RDN→Q_FALL | 0.07467 | 0.08321 | 0.08818 |

Timing Constraints (ns)

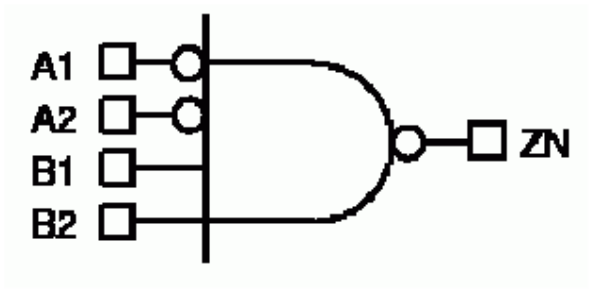
| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.06965 | -0.06965 | -0.06467 |
| D | hold_RISE→CK | -0.06468 | -0.06467 | -0.06467 |
| D | setup_FALL→CK | 0.09950 | 0.10448 | 0.10944 |
| D | setup_RISE→CK | 0.07959 | 0.07960 | 0.07959 |
| E | hold_FALL→CK | -0.07461 | -0.07461 | -0.07461 |
| E | hold_RISE→CK | -0.06965 | -0.06965 | -0.06965 |
| E | setup_FALL→CK | 0.08456 | 0.08456 | 0.08456 |
| E | setup_RISE→CK | 0.07960 | 0.07960 | 0.07960 |
| RDN | setup_RISE→CK | 0.08954 | 0.08954 | 0.08955 |
| RDN | hold_RISE→CK | -0.08457 | -0.08456 | -0.08457 |
| CK | minpwh | 0.07368 | 0.07764 | 0.08162 |
| CK | minpwl | 0.08553 | 0.09047 | 0.09047 |
| RDN | minpwl | 0.07366 | 0.08163 | 0.09347 |

I2NAND4HS

Cell Description

4-Input NAND with 2 Inverted Inputs

$$Z_N = \neg((\neg A_1) \& (\neg A_2) \& B_1 \& B_2)$$



Function Table

| A1 | A2 | B1 | B2 | ZN |
|----|----|----|----|----|
| 0 | 0 | 0 | X | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | X | X | 1 |
| 1 | X | X | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| I2NAND4HSV0 | 1.80 | 2.00 |
| I2NAND4HSV1 | 1.80 | 2.00 |
| I2NAND4HSV2 | 1.80 | 2.00 |
| I2NAND4HSV4 | 1.80 | 3.00 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00144 | 0.00162 | 0.00199 | 0.00396 |
| A2 | 0.00150 | 0.00183 | 0.00224 | 0.00429 |
| B1 | 0.00083 | 0.00108 | 0.00146 | 0.00284 |
| B2 | 0.00093 | 0.00120 | 0.00163 | 0.00317 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00114 | 0.00112 | 0.00109 | 0.00149 |
| A2 | 0.00113 | 0.00123 | 0.00106 | 0.00150 |
| B1 | 0.00101 | 0.00120 | 0.00152 | 0.00303 |
| B2 | 0.00101 | 0.00123 | 0.00155 | 0.00280 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00032221 | 0.00036966 | 0.00039195 | 0.00078076 |

Delay Table (ns)

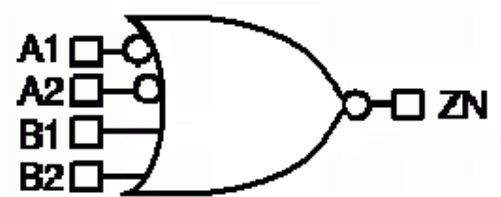
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.06940 | 0.06255 | 0.06038 | 0.06372 |
| A1→ZN_RISE | 0.03989 | 0.03810 | 0.03923 | 0.04198 |
| A2→ZN_FALL | 0.07554 | 0.07315 | 0.07108 | 0.07090 |
| A2→ZN_RISE | 0.04050 | 0.04112 | 0.04208 | 0.04346 |
| B1→ZN_FALL | 0.05861 | 0.05384 | 0.04960 | 0.04582 |
| B1→ZN_RISE | 0.02335 | 0.02155 | 0.02033 | 0.01874 |
| B2→ZN_FALL | 0.06123 | 0.05559 | 0.05214 | 0.04834 |
| B2→ZN_RISE | 0.02452 | 0.02230 | 0.02134 | 0.01983 |

I2NOR4HS

Cell Description

4-Input NOR with 2 Inverted Inputs

$$Z_N = \neg((\neg A_1) \vee (\neg A_2) \vee B_1 \vee B_2)$$



Function Table

| A1 | A2 | B1 | B2 | ZN |
|----|----|----|----|----|
| 0 | X | X | X | 0 |
| 1 | 0 | X | X | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| I2NOR4HSV0 | 1.80 | 2.00 |
| I2NOR4HSV1 | 1.80 | 2.00 |
| I2NOR4HSV2 | 1.80 | 2.00 |
| I2NOR4HSV4 | 1.80 | 3.20 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00164 | 0.00201 | 0.00261 | 0.00521 |
| A2 | 0.00169 | 0.00204 | 0.00257 | 0.00468 |
| B1 | 0.00071 | 0.00091 | 0.00122 | 0.00230 |
| B2 | 0.00058 | 0.00072 | 0.00094 | 0.00173 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00113 | 0.00112 | 0.00112 | 0.00151 |
| A2 | 0.00104 | 0.00103 | 0.00103 | 0.00146 |
| B1 | 0.00101 | 0.00123 | 0.00159 | 0.00302 |
| B2 | 0.00096 | 0.00118 | 0.00154 | 0.00277 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00033085 | 0.00038539 | 0.00059000 | 0.00124870 |

Delay Table (ns)

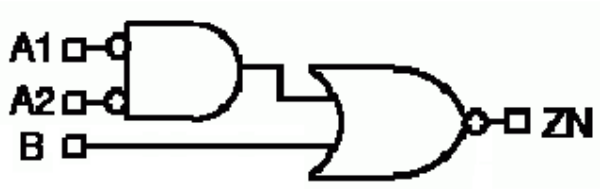
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.04001 | 0.04106 | 0.04308 | 0.04830 |
| A1→ZN_RISE | 0.10236 | 0.10075 | 0.10018 | 0.09924 |
| A2→ZN_FALL | 0.04482 | 0.04553 | 0.04695 | 0.04738 |
| A2→ZN_RISE | 0.10476 | 0.10225 | 0.09984 | 0.09223 |
| B1→ZN_FALL | 0.01785 | 0.01630 | 0.01456 | 0.01286 |
| B1→ZN_RISE | 0.07527 | 0.07029 | 0.06533 | 0.05738 |
| B2→ZN_FALL | 0.01622 | 0.01468 | 0.01311 | 0.01115 |
| B2→ZN_RISE | 0.06111 | 0.05501 | 0.04958 | 0.04165 |

IAO21HS

Cell Description

2-1 IAO with 2 Inverted Inputs

$$ZN = (!(((!A1) \& (!A2)) \mid B))$$



Function Table

| A1 | A2 | B | ZN |
|----|----|---|----|
| 0 | 0 | X | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | X | 0 | 1 |
| 1 | X | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| IAO21HSV0 | 1.80 | 1.40 |
| IAO21HSV1 | 1.80 | 1.40 |
| IAO21HSV2 | 1.80 | 1.40 |
| IAO21HSV4 | 1.80 | 1.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00121 | 0.00139 | 0.00163 | 0.00266 |
| A2 | 0.00134 | 0.00152 | 0.00178 | 0.00286 |
| B | 0.00053 | 0.00068 | 0.00087 | 0.00161 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00105 | 0.00104 | 0.00103 | 0.00145 |
| A2 | 0.00112 | 0.00113 | 0.00111 | 0.00141 |
| B | 0.00102 | 0.00124 | 0.00151 | 0.00287 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00017639 | 0.00021276 | 0.00028667 | 0.00052562 |

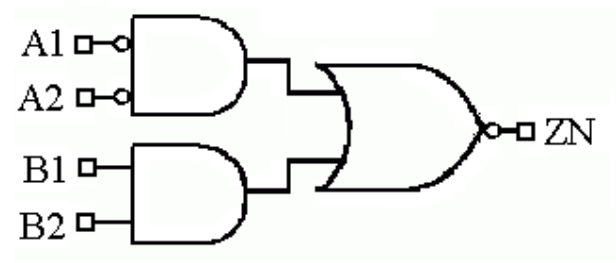
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.05792 | 0.05949 | 0.06284 | 0.06202 |
| A1→ZN_RISE | 0.04573 | 0.04414 | 0.04370 | 0.03930 |
| A2→ZN_FALL | 0.06184 | 0.06373 | 0.06805 | 0.06550 |
| A2→ZN_RISE | 0.04756 | 0.04612 | 0.04604 | 0.04067 |
| B→ZN_FALL | 0.01464 | 0.01337 | 0.01171 | 0.01161 |
| B→ZN_RISE | 0.03144 | 0.02893 | 0.02639 | 0.02476 |

IAO22HS

Cell Description

2-2 IAO with 2 Inverted Inputs
 $ZN = (((\neg A1) \& (\neg A2)) | (B1 \& B2))$



Function Table

| B1 | B2 | A1 | A2 | ZN |
|----|----|----|----|----|
| 0 | X | 0 | 0 | 0 |
| 0 | X | 0 | 1 | 1 |
| 0 | X | 1 | X | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | X | 1 |
| 1 | 1 | X | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| IAO22HSV0 | 1.80 | 1.80 |
| IAO22HSV1 | 1.80 | 1.80 |
| IAO22HSV2 | 1.80 | 1.80 |
| IAO22HSV4 | 1.80 | 2.60 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00127 | 0.00143 | 0.00172 | 0.00290 |
| A2 | 0.00138 | 0.00155 | 0.00185 | 0.00310 |
| B1 | 0.00068 | 0.00084 | 0.00115 | 0.00211 |
| B2 | 0.00076 | 0.00096 | 0.00132 | 0.00250 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00110 | 0.00116 | 0.00112 | 0.00144 |
| A2 | 0.00099 | 0.00109 | 0.00106 | 0.00142 |

| | | | | |
|----|---------|---------|---------|---------|
| B1 | 0.00106 | 0.00117 | 0.00151 | 0.00276 |
| B2 | 0.00097 | 0.00116 | 0.00151 | 0.00304 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00018136 | 0.00022964 | 0.00031234 | 0.00064903 |

Delay Table (ns)

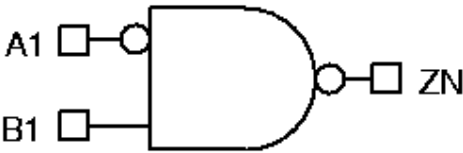
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.05759 | 0.05859 | 0.06245 | 0.06160 |
| A1→ZN_RISE | 0.04577 | 0.04409 | 0.04480 | 0.04010 |
| A2→ZN_FALL | 0.05992 | 0.06133 | 0.06523 | 0.06531 |
| A2→ZN_RISE | 0.04760 | 0.04538 | 0.04618 | 0.04158 |
| B1→ZN_FALL | 0.02761 | 0.02385 | 0.02154 | 0.01807 |
| B1→ZN_RISE | 0.03727 | 0.03386 | 0.03207 | 0.02876 |
| B2→ZN_FALL | 0.02876 | 0.02582 | 0.02363 | 0.02069 |
| B2→ZN_RISE | 0.04025 | 0.03764 | 0.03608 | 0.03385 |

INAND2HS

Cell Description

2-Input NAND with 1 Inverted Input

$$Z_N = \neg(\neg A_1 \& B_1)$$



Function Table

| A1 | B1 | ZN |
|----|----|----|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| INAND2HSV0 | 1.80 | 1.00 |
| INAND2HSV1 | 1.80 | 1.00 |
| INAND2HSV2 | 1.80 | 1.00 |
| INAND2HSV4 | 1.80 | 1.60 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00114 | 0.00136 | 0.00159 | 0.00277 |
| B1 | 0.00048 | 0.00067 | 0.00087 | 0.00154 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00108 | 0.00115 | 0.00101 | 0.00147 |
| B1 | 0.00094 | 0.00122 | 0.00152 | 0.00306 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00016331 | 0.00018861 | 0.00020394 | 0.00039781 |

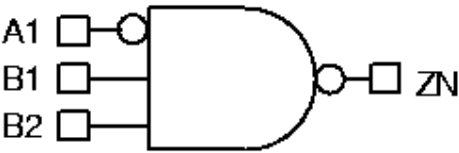
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.04257 | 0.04276 | 0.04248 | 0.04184 |
| A1→ZN_RISE | 0.03328 | 0.03386 | 0.03396 | 0.03333 |
| B1→ZN_FALL | 0.02336 | 0.02258 | 0.02047 | 0.01811 |
| B1→ZN_RISE | 0.01723 | 0.01629 | 0.01494 | 0.01323 |

INAND3HS

Cell Description

3-Input NAND with 1 Inverted Input
 $ZN = \neg((\neg A1) \& B1 \& B2)$



Function Table

| A1 | B1 | B2 | ZN |
|----|----|----|----|
| 0 | 0 | X | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | X | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| INAND3HSV0 | 1.80 | 1.40 |
| INAND3HSV1 | 1.80 | 1.40 |
| INAND3HSV2 | 1.80 | 1.40 |
| INAND3HSV4 | 1.80 | 2.00 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00131 | 0.00156 | 0.00188 | 0.00312 |
| B1 | 0.00068 | 0.00084 | 0.00112 | 0.00193 |
| B2 | 0.00079 | 0.00100 | 0.00132 | 0.00237 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00117 | 0.00115 | 0.00107 | 0.00146 |
| B1 | 0.00105 | 0.00124 | 0.00154 | 0.00300 |
| B2 | 0.00104 | 0.00131 | 0.00151 | 0.00328 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00021059 | 0.00024317 | 0.00025735 | 0.00054181 |

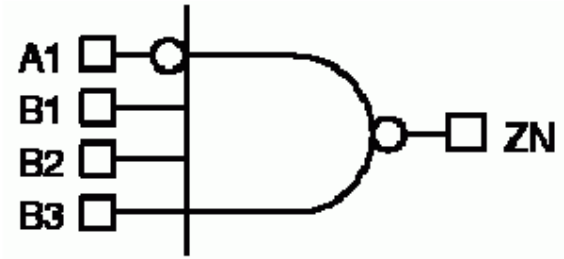
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.05645 | 0.05430 | 0.05303 | 0.04829 |
| A1→ZN_RISE | 0.03768 | 0.03771 | 0.03916 | 0.03536 |
| B1→ZN_FALL | 0.04136 | 0.03604 | 0.03326 | 0.02683 |
| B1→ZN_RISE | 0.02133 | 0.01881 | 0.01760 | 0.01498 |
| B2→ZN_FALL | 0.04497 | 0.04007 | 0.03643 | 0.03085 |
| B2→ZN_RISE | 0.02337 | 0.02103 | 0.01943 | 0.01722 |

INAND4HS

Cell Description

4-Input NAND with 1 Inverted Input
 $ZN = \neg((\neg A1) \& B1 \& B2 \& B3)$



Function Table

| A1 | B1 | B2 | B3 | ZN |
|----|----|----|----|----|
| 0 | 0 | X | X | 1 |
| 0 | 1 | 0 | X | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | X | X | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| INAND4HSV0 | 1.80 | 1.60 |
| INAND4HSV1 | 1.80 | 1.60 |
| INAND4HSV2 | 1.80 | 1.80 |
| INAND4HSV4 | 1.80 | 2.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00146 | 0.00167 | 0.00210 | 0.00395 |
| B1 | 0.00077 | 0.00095 | 0.00133 | 0.00249 |
| B2 | 0.00088 | 0.00110 | 0.00153 | 0.00285 |
| B3 | 0.00097 | 0.00121 | 0.00171 | 0.00318 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00116 | 0.00116 | 0.00111 | 0.00146 |
| B1 | 0.00102 | 0.00124 | 0.00154 | 0.00325 |
| B2 | 0.00107 | 0.00125 | 0.00154 | 0.00302 |
| B3 | 0.00104 | 0.00124 | 0.00153 | 0.00282 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00026606 | 0.00030724 | 0.00033261 | 0.00066066 |

Delay Table (ns)

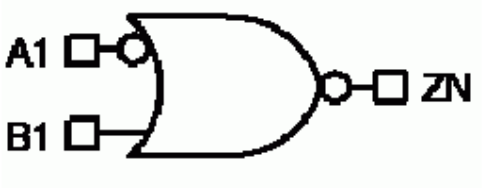
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.07104 | 0.06484 | 0.06363 | 0.06414 |
| A1→ZN_RISE | 0.04034 | 0.03935 | 0.04126 | 0.04264 |
| B1→ZN_FALL | 0.05602 | 0.04912 | 0.04635 | 0.04156 |
| B1→ZN_RISE | 0.02274 | 0.02035 | 0.01971 | 0.01780 |
| B2→ZN_FALL | 0.06255 | 0.05479 | 0.05137 | 0.04558 |
| B2→ZN_RISE | 0.02505 | 0.02234 | 0.02160 | 0.01938 |
| B3→ZN_FALL | 0.06465 | 0.05681 | 0.05438 | 0.04756 |
| B3→ZN_RISE | 0.02605 | 0.02324 | 0.02273 | 0.02027 |

INOR2HS

Cell Description

2-Input NOR with 1 Inverted Input

$$Z_N = \neg((\neg A_1) \vee B_1)$$



Function Table

| A1 | B1 | ZN |
|----|----|----|
| 0 | X | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| INOR2HSV0 | 1.80 | 1.00 |
| INOR2HSV1 | 1.80 | 1.00 |
| INOR2HSV2 | 1.80 | 1.20 |
| INOR2HSV4 | 1.80 | 1.60 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00111 | 0.00127 | 0.00158 | 0.00274 |
| B1 | 0.00050 | 0.00064 | 0.00088 | 0.00170 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00113 | 0.00113 | 0.00106 | 0.00148 |
| B1 | 0.00100 | 0.00117 | 0.00154 | 0.00313 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00015370 | 0.00019241 | 0.00026321 | 0.00058129 |

Delay Table (ns)

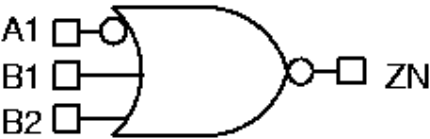
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.03513 | 0.03519 | 0.03799 | 0.03695 |
| A1→ZN_RISE | 0.04364 | 0.04164 | 0.04261 | 0.03930 |
| B1→ZN_FALL | 0.01445 | 0.01299 | 0.01189 | 0.01086 |
| B1→ZN_RISE | 0.03036 | 0.02773 | 0.02693 | 0.02483 |

INOR3HS

Cell Description

3-Input NOR with 1 Inverted Input

$$Z_N = \neg((\neg A_1) \vee B_1 \vee B_2)$$



Function Table

| A1 | B1 | B2 | ZN |
|----|----|----|----|
| 0 | X | X | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| INOR3HSV0 | 1.80 | 1.40 |
| INOR3HSV1 | 1.80 | 1.40 |
| INOR3HSV2 | 1.80 | 1.40 |
| INOR3HSV4 | 1.80 | 2.20 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00126 | 0.00147 | 0.00182 | 0.00302 |
| B1 | 0.00065 | 0.00083 | 0.00109 | 0.00200 |
| B2 | 0.00077 | 0.00100 | 0.00135 | 0.00253 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00115 | 0.00112 | 0.00104 | 0.00147 |
| B1 | 0.00099 | 0.00122 | 0.00155 | 0.00301 |
| B2 | 0.00102 | 0.00122 | 0.00155 | 0.00328 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00022680 | 0.00030021 | 0.00040247 | 0.00089668 |

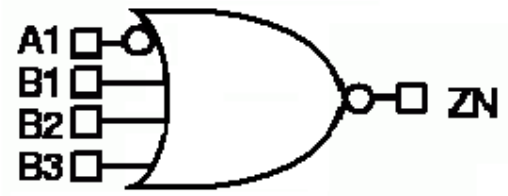
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.03802 | 0.03808 | 0.04140 | 0.03812 |
| A1→ZN_RISE | 0.06064 | 0.05691 | 0.05706 | 0.04904 |
| B1→ZN_FALL | 0.01658 | 0.01500 | 0.01326 | 0.01177 |
| B1→ZN_RISE | 0.05353 | 0.04990 | 0.04644 | 0.04123 |
| B2→ZN_FALL | 0.01702 | 0.01536 | 0.01391 | 0.01247 |
| B2→ZN_RISE | 0.05623 | 0.05233 | 0.05047 | 0.04563 |

INOR4HS

Cell Description

4-Input NOR with 1 Inverted Input
 $ZN = \neg((\neg A1) \vee B1 \vee B2 \vee B3)$



Function Table

| A1 | B1 | B2 | B3 | ZN |
|----|----|----|----|----|
| 0 | X | X | X | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | X | 0 |
| 1 | 1 | X | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| INOR4HSV0 | 1.80 | 1.60 |
| INOR4HSV1 | 1.80 | 1.60 |
| INOR4HSV2 | 1.80 | 1.60 |
| INOR4HSV4 | 1.80 | 2.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00139 | 0.00163 | 0.00191 | 0.00338 |
| B1 | 0.00072 | 0.00092 | 0.00117 | 0.00230 |
| B2 | 0.00085 | 0.00110 | 0.00145 | 0.00298 |
| B3 | 0.00096 | 0.00127 | 0.00168 | 0.00341 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00111 | 0.00116 | 0.00110 | 0.00150 |
| B1 | 0.00102 | 0.00121 | 0.00147 | 0.00304 |
| B2 | 0.00103 | 0.00123 | 0.00158 | 0.00313 |
| B3 | 0.00102 | 0.00126 | 0.00154 | 0.00285 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00029269 | 0.00039120 | 0.00055037 | 0.00121660 |

Delay Table (ns)

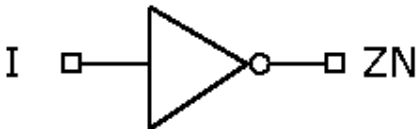
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.04027 | 0.04089 | 0.04200 | 0.03982 |
| A1→ZN_RISE | 0.07981 | 0.07345 | 0.06822 | 0.06125 |
| B1→ZN_FALL | 0.01763 | 0.01574 | 0.01380 | 0.01292 |
| B1→ZN_RISE | 0.07585 | 0.06950 | 0.06382 | 0.05933 |
| B2→ZN_FALL | 0.01843 | 0.01650 | 0.01460 | 0.01390 |
| B2→ZN_RISE | 0.08349 | 0.07806 | 0.07407 | 0.07221 |
| B3→ZN_FALL | 0.01814 | 0.01650 | 0.01449 | 0.01315 |
| B3→ZN_RISE | 0.08526 | 0.08146 | 0.07716 | 0.07426 |

INHS

Cell Description

Inverter

$ZN = (!I)$



Function Table

| I | ZN |
|---|----|
| 0 | 1 |
| 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| INHSV0 | 1.80 | 0.60 |
| INHSV0SR | 1.80 | 0.60 |
| INHSV0P5 | 1.80 | 0.60 |
| INHSV0P5SR | 1.80 | 0.60 |
| INHSV1 | 1.80 | 0.60 |
| INHSV1SR | 1.80 | 0.60 |
| INHSV2 | 1.80 | 0.60 |
| INHSV2P5 | 1.80 | 0.80 |
| INHSV2SR | 1.80 | 0.60 |
| INHSV3 | 1.80 | 0.80 |
| INHSV3SR | 1.80 | 0.80 |
| INHSV4 | 1.80 | 0.80 |
| INHSV4SR | 1.80 | 0.80 |
| INHSV5 | 1.80 | 1.00 |
| INHSV5SR | 1.80 | 1.00 |
| INHSV6 | 1.80 | 1.00 |
| INHSV6SR | 1.80 | 1.00 |
| INHSV8 | 1.80 | 1.40 |
| INHSV8SR | 1.80 | 1.40 |
| INHSV10 | 1.80 | 1.60 |
| INHSV10SR | 1.80 | 1.60 |
| INHSV12 | 1.80 | 1.80 |

| | | |
|-----------|------|------|
| INHSV12SR | 1.80 | 1.80 |
| INHSV16 | 1.80 | 2.40 |
| INHSV16SR | 1.80 | 2.40 |
| INHSV20 | 1.80 | 2.80 |
| INHSV20SR | 1.80 | 2.80 |
| INHSV24 | 1.80 | 3.40 |
| INHSV24SR | 1.80 | 3.40 |
| INHSV32 | 1.80 | 4.40 |
| INHSV32SR | 1.80 | 4.40 |
| INHSV48 | 1.80 | 6.40 |
| INHSV48SR | 1.80 | 6.40 |
| INHSV64 | 1.80 | 8.40 |
| INHSV64SR | 1.80 | 8.40 |

Pin Power (uW/MHz)

| Pin | V0 | V0SR | V0P5 | V0P5SR | V1 | V1SR | V2 | V2P5 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00031 | 0.00028 | 0.00034 | 0.00035 | 0.00039 | 0.00041 | 0.00050 | 0.00058 |

| Pin | V2SR | V3 | V3SR | V4 | V4SR | V5 | V5SR | V6 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00047 | 0.00068 | 0.00060 | 0.00083 | 0.00077 | 0.00113 | 0.00104 | 0.00127 |

| Pin | V6SR | V8 | V8SR | V10 | V10SR | V12 | V12SR | V16 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00118 | 0.00157 | 0.00146 | 0.00202 | 0.00188 | 0.00234 | 0.00215 | 0.00318 |

| Pin | V16SR | V20 | V20SR | V24 | V24SR | V32 | V32SR | V48 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00294 | 0.00390 | 0.00368 | 0.00465 | 0.00437 | 0.00604 | 0.00564 | 0.01103 |

| Pin | V48SR | V64 | V64SR |
|-----|---------|---------|---------|
| I | 0.00847 | 0.01518 | 0.01280 |

Pin Capacitance (pf)

| Pin | V0 | V0SR | V0P5 | V0P5SR | V1 | V1SR | V2 | V2P5 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00093 | 0.00084 | 0.00098 | 0.00101 | 0.00114 | 0.00120 | 0.00149 | 0.00199 |

| Pin | V2SR | V3 | V3SR | V4 | V4SR | V5 | V5SR | V6 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00139 | 0.00231 | 0.00212 | 0.00283 | 0.00260 | 0.00362 | 0.00337 | 0.00413 |

| Pin | V6SR | V8 | V8SR | V10 | V10SR | V12 | V12SR | V16 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00383 | 0.00547 | 0.00504 | 0.00675 | 0.00624 | 0.00811 | 0.00747 | 0.01082 |

| Pin | V16SR | V20 | V20SR | V24 | V24SR | V32 | V32SR | V48 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.01001 | 0.01345 | 0.01254 | 0.01598 | 0.01493 | 0.02122 | 0.01971 | 0.02936 |

| Pin | V48SR | V64 | V64SR |
|-----|---------|---------|---------|
| I | 0.02891 | 0.03838 | 0.03665 |

Max Leakage Power (uW)

| V0 | V0SR | V0P5 | V0P5SR | V1 | V1SR | V2 | V2P5 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00005414 | 0.00005037 | 0.00004961 | 0.00004861 | 0.00006292 | 0.00006398 | 0.00008558 | 0.00012319 |

| V2SR | V3 | V3SR | V4 | V4SR | V5 | V5SR | V6 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00008493 | 0.00015885 | 0.00015631 | 0.00020721 | 0.00020691 | 0.00027495 | 0.00025686 | 0.00033611 |

| V6SR | V8 | V8SR | V10 | V10SR | V12 | V12SR | V16 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00033068 | 0.00048991 | 0.00049230 | 0.00063450 | 0.00062275 | 0.00078843 | 0.00077514 | 0.00110900 |

| V16SR | V20 | V20SR | V24 | V24SR | V32 | V32SR | V48 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00110380 | 0.00141510 | 0.00141180 | 0.00175360 | 0.00172730 | 0.00239260 | 0.00238540 | 0.00372910 |

| V48SR | V64 | V64SR |
|------------|------------|------------|
| 0.00371380 | 0.00504380 | 0.00502310 |

Delay Table (ns)

| Description | V0 | V0SR | V0P5 | V0P5SR | V1 | V1SR | V2 | V2P5 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| I→ZN_FALL | 0.01262 | 0.01206 | 0.01214 | 0.01113 | 0.01134 | 0.01038 | 0.01009 | 0.00929 |
| I→ZN_RISE | 0.01403 | 0.01491 | 0.01331 | 0.01391 | 0.01268 | 0.01297 | 0.01152 | 0.01045 |

| Description | V2SR | V3 | V3SR | V4 | V4SR | V5 | V5SR | V6 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| I→ZN_FALL | 0.00975 | 0.00905 | 0.00856 | 0.00864 | 0.00829 | 0.00880 | 0.00843 | 0.00848 |
| I→ZN_RISE | 0.01234 | 0.01029 | 0.01070 | 0.00992 | 0.01046 | 0.00998 | 0.01053 | 0.00979 |

| Description | V6SR | V8 | V8SR | V10 | V10SR | V12 | V12SR | V16 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| I→ZN_FALL | 0.00814 | 0.00835 | 0.00796 | 0.00823 | 0.00790 | 0.00844 | 0.00800 | 0.00835 |
| I→ZN_RISE | 0.01030 | 0.00966 | 0.01007 | 0.00958 | 0.01003 | 0.00978 | 0.01008 | 0.00974 |

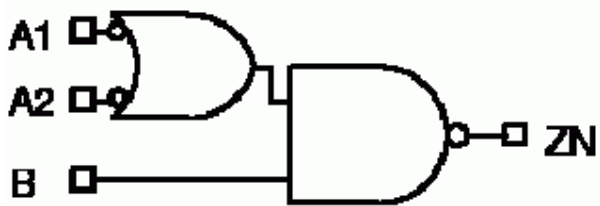
| Description | V16SR | V20 | V20SR | V24 | V24SR | V32 | V32SR | V48 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| I→ZN_FALL | 0.00798 | 0.00847 | 0.00799 | 0.00921 | 0.00824 | 0.00880 | 0.00840 | 0.01496 |
| I→ZN_RISE | 0.01012 | 0.00985 | 0.01004 | 0.01068 | 0.01033 | 0.01026 | 0.01061 | 0.01790 |

| Description | V48SR | V64 | V64SR |
|-------------|---------|---------|---------|
| I→ZN_FALL | 0.01054 | 0.01703 | 0.01349 |
| I→ZN_RISE | 0.01299 | 0.02037 | 0.01753 |

IOA21HS

Cell Description

2-1 IOA with 2 Inverted Inputs
 $ZN = (!(((!A1) | (!A2)) \& B))$



Function Table

| A1 | A2 | B | ZN |
|----|----|---|----|
| 0 | X | 0 | 1 |
| 0 | X | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| IOA21HSV0 | 1.80 | 1.40 |
| IOA21HSV1 | 1.80 | 1.40 |
| IOA21HSV2 | 1.80 | 1.40 |
| IOA21HSV4 | 1.80 | 1.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00125 | 0.00147 | 0.00172 | 0.00292 |
| A2 | 0.00133 | 0.00154 | 0.00182 | 0.00305 |
| B | 0.00051 | 0.00067 | 0.00087 | 0.00160 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00112 | 0.00117 | 0.00106 | 0.00150 |
| A2 | 0.00109 | 0.00109 | 0.00109 | 0.00146 |
| B | 0.00100 | 0.00124 | 0.00154 | 0.00312 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00016585 | 0.00018904 | 0.00020665 | 0.00041423 |

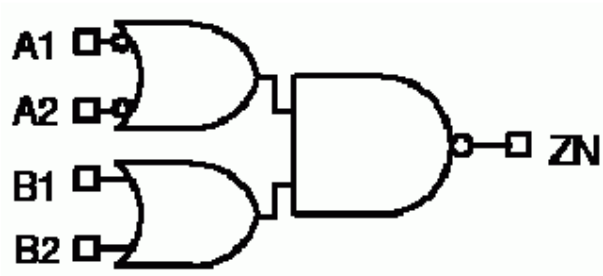
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.04607 | 0.04620 | 0.04648 | 0.04340 |
| A1→ZN_RISE | 0.04983 | 0.05162 | 0.05328 | 0.05062 |
| A2→ZN_FALL | 0.04820 | 0.04800 | 0.04931 | 0.04575 |
| A2→ZN_RISE | 0.05163 | 0.05297 | 0.05604 | 0.05269 |
| B→ZN_FALL | 0.02403 | 0.02211 | 0.01991 | 0.01761 |
| B→ZN_RISE | 0.01786 | 0.01638 | 0.01493 | 0.01339 |

IOA22HS

Cell Description

2-2 IOA with 2 Inverted Inputs
 $ZN = (!(((!A1)|(!A2))\&(B1|B2)))$



Function Table

| B1 | B2 | A1 | A2 | ZN |
|----|----|----|----|----|
| 0 | 0 | X | X | 1 |
| 0 | 1 | 0 | X | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | X | 0 | X | 0 |
| 1 | X | 1 | 0 | 0 |
| 1 | X | 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| IOA22HSV0 | 1.80 | 1.60 |
| IOA22HSV1 | 1.80 | 1.60 |
| IOA22HSV2 | 1.80 | 1.80 |
| IOA22HSV4 | 1.80 | 2.60 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00133 | 0.00156 | 0.00185 | 0.00324 |
| A2 | 0.00144 | 0.00167 | 0.00194 | 0.00338 |
| B1 | 0.00065 | 0.00081 | 0.00105 | 0.00196 |
| B2 | 0.00077 | 0.00097 | 0.00131 | 0.00251 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00105 | 0.00104 | 0.00107 | 0.00147 |
| A2 | 0.00103 | 0.00103 | 0.00105 | 0.00147 |

| | | | | |
|----|---------|---------|---------|---------|
| B1 | 0.00102 | 0.00123 | 0.00149 | 0.00274 |
| B2 | 0.00100 | 0.00121 | 0.00151 | 0.00307 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00015946 | 0.00018013 | 0.00020957 | 0.00044189 |

Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.04713 | 0.04712 | 0.04790 | 0.04665 |
| A1→ZN_RISE | 0.05298 | 0.05431 | 0.05559 | 0.05314 |
| A2→ZN_FALL | 0.04995 | 0.05026 | 0.05048 | 0.04910 |
| A2→ZN_RISE | 0.05605 | 0.05780 | 0.05808 | 0.05539 |
| B1→ZN_FALL | 0.02877 | 0.02547 | 0.02271 | 0.02084 |
| B1→ZN_RISE | 0.03798 | 0.03396 | 0.03095 | 0.02721 |
| B2→ZN_FALL | 0.03167 | 0.02866 | 0.02662 | 0.02467 |
| B2→ZN_RISE | 0.04033 | 0.03685 | 0.03493 | 0.03176 |

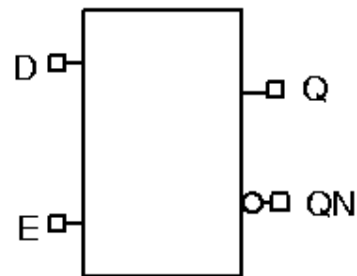
LAHHS

Cell Description

High Enable Latch

$Q = E ? D : \text{pre_}Q$

$QN = !Q$



Function Table

| E | D | Q |
|---|---|------|
| 0 | X | Q<1> |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| LAHHSV1 | 1.80 | 3.00 |
| LAHHSV2 | 1.80 | 3.40 |
| LAHHSV4 | 1.80 | 4.00 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| D | 0.00004 | 0.00005 | 0.00007 |
| E | 0.00202 | 0.00241 | 0.00248 |
| Q | 0.00186 | 0.00227 | 0.00319 |
| QN | 0.00187 | 0.00230 | 0.00318 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| D | 0.00121 | 0.00143 | 0.00149 |
| E | 0.00109 | 0.00134 | 0.00138 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00037144 | 0.00049911 | 0.00074876 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| D→Q_FALL | 0.08032 | 0.07390 | 0.07977 |
| D→Q_RISE | 0.05988 | 0.05746 | 0.06060 |
| E→Q_FALL | 0.10186 | 0.09024 | 0.09732 |
| E→Q_RISE | 0.10452 | 0.09496 | 0.09669 |
| D→QN_FALL | 0.09215 | 0.08833 | 0.09730 |
| D→QN_RISE | 0.11488 | 0.10830 | 0.12093 |
| E→QN_FALL | 0.13704 | 0.12602 | 0.13356 |
| E→QN_RISE | 0.13684 | 0.12503 | 0.13865 |

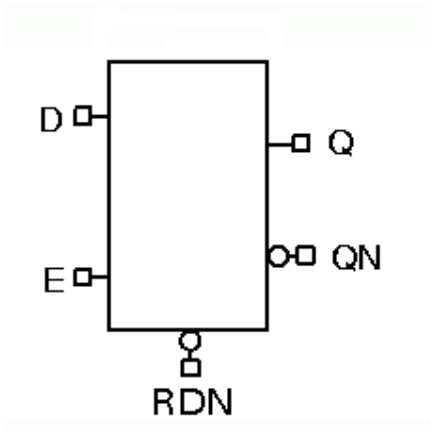
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|--------------|----------|----------|----------|
| D | hold_FALL→E | -0.04975 | -0.04974 | -0.05969 |
| D | hold_RISE→E | -0.00000 | -0.00499 | -0.00994 |
| D | setup_FALL→E | 0.07462 | 0.07960 | 0.08954 |
| D | setup_RISE→E | 0.01493 | 0.01991 | 0.03981 |
| E | minpwh | 0.06182 | 0.05386 | 0.05785 |

LAHRNHS

Cell Description

Latch
 $Q = \text{!RDN} ? 0 : E ? D : \text{pre_}Q$
 $QN = \text{!}Q$



Function Table

| RDN | E | D | Q |
|-----|---|---|------|
| 0 | X | X | 0 |
| 1 | 0 | X | Q<1> |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| LAHRNHSV1 | 1.80 | 3.80 |
| LAHRNHSV2 | 1.80 | 3.80 |
| LAHRNHSV4 | 1.80 | 4.40 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| D | 0.00002 | 0.00002 | 0.00002 |
| E | 0.00216 | 0.00250 | 0.00246 |
| Q | 0.00196 | 0.00223 | 0.00324 |
| QN | 0.00195 | 0.00222 | 0.00318 |
| RDN | 0.00004 | 0.00005 | 0.00008 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| D | 0.00141 | 0.00148 | 0.00162 |
| E | 0.00110 | 0.00135 | 0.00136 |
| RDN | 0.00185 | 0.00171 | 0.00182 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00043386 | 0.00051287 | 0.00074631 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| D→Q_FALL | 0.08080 | 0.08226 | 0.08661 |
| D→Q_RISE | 0.08485 | 0.07604 | 0.08717 |
| E→Q_FALL | 0.09927 | 0.09547 | 0.09525 |
| E→Q_RISE | 0.12521 | 0.10874 | 0.11765 |
| RDN→Q_FALL | 0.04234 | 0.05696 | 0.06418 |
| RDN→Q_RISE | 0.08372 | 0.07384 | 0.08453 |
| D→QN_FALL | 0.12142 | 0.11308 | 0.13105 |
| D→QN_RISE | 0.11567 | 0.12197 | 0.13195 |
| E→QN_FALL | 0.16210 | 0.14603 | 0.16169 |
| E→QN_RISE | 0.13461 | 0.13553 | 0.14095 |
| RDN→QN_RISE | 0.07377 | 0.09572 | 0.11021 |
| RDN→QN_FALL | 0.12039 | 0.11103 | 0.12851 |

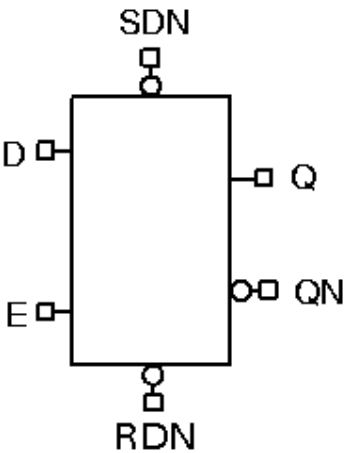
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|--------------|----------|----------|----------|
| D | hold_FALL→E | -0.05473 | -0.05970 | -0.07461 |
| D | hold_RISE→E | -0.01990 | -0.02488 | -0.03979 |
| D | setup_FALL→E | 0.08954 | 0.10446 | 0.10945 |
| D | setup_RISE→E | 0.03979 | 0.04477 | 0.06966 |
| RDN | setup_RISE→E | 0.04476 | 0.04974 | 0.06964 |
| RDN | hold_RISE→E | -0.02487 | -0.02486 | -0.03980 |
| E | minpwh | 0.07368 | 0.06575 | 0.08157 |
| RDN | minpwl | 0.04994 | 0.06573 | 0.07764 |

LAHRSNHS

Cell Description

High Enable Latch with Clear and Set
 $Q = !SDN ? 1 : !RDN ? 0 : E ? D : pre_Q$
 $QN = !Q$



Function Table

| RDN | SDN | E | D | Q |
|-----|-----|---|---|------|
| 0 | 0 | X | X | 1 |
| 0 | 1 | X | X | 0 |
| 1 | 0 | X | X | 1 |
| 1 | 1 | 0 | X | Q<1> |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| LAHRSNHSV1 | 1.80 | 5.20 |
| LAHRSNHSV2 | 1.80 | 5.20 |
| LAHRSNHSV4 | 1.80 | 5.60 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| D | 0.00005 | 0.00006 | 0.00006 |
| E | 0.00198 | 0.00236 | 0.00234 |
| Q | 0.00225 | 0.00259 | 0.00371 |
| QN | 0.00223 | 0.00257 | 0.00353 |
| RDN | 0.00003 | 0.00004 | 0.00003 |
| SDN | 0.00114 | 0.00119 | 0.00118 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| D | 0.00127 | 0.00151 | 0.00156 |
| E | 0.00114 | 0.00141 | 0.00114 |

| | | | |
|-----|---------|---------|---------|
| RDN | 0.00176 | 0.00185 | 0.00185 |
| SDN | 0.00112 | 0.00112 | 0.00112 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00046802 | 0.00059448 | 0.00081065 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| D→Q_FALL | 0.14618 | 0.13246 | 0.13769 |
| D→Q_RISE | 0.10228 | 0.09371 | 0.10315 |
| E→Q_FALL | 0.14782 | 0.12966 | 0.14368 |
| E→Q_RISE | 0.13080 | 0.11588 | 0.13140 |
| RDN→Q_FALL | 0.11032 | 0.11815 | 0.13153 |
| RDN→Q_RISE | 0.10014 | 0.09091 | 0.10013 |
| SDN→Q_FALL | 0.13880 | 0.14120 | 0.15034 |
| SDN→Q_RISE | 0.09687 | 0.10254 | 0.10790 |
| D→QN_FALL | 0.13978 | 0.12631 | 0.14928 |
| D→QN_RISE | 0.19154 | 0.17859 | 0.19359 |
| E→QN_FALL | 0.16872 | 0.14874 | 0.17775 |
| E→QN_RISE | 0.19308 | 0.17550 | 0.19923 |
| RDN→QN_RISE | 0.15546 | 0.16794 | 0.19420 |
| RDN→QN_FALL | 0.13789 | 0.12364 | 0.14629 |
| SDN→QN_FALL | 0.13076 | 0.13348 | 0.15085 |
| SDN→QN_RISE | 0.18086 | 0.18649 | 0.20648 |

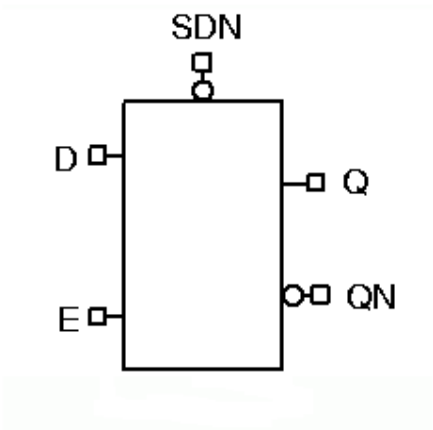
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|------------------------|----------|----------|----------|
| D | hold_FALL→E | -0.11939 | -0.10944 | -0.11939 |
| D | hold_RISE→E | -0.04476 | -0.03980 | -0.04974 |
| D | setup_FALL→E | 0.16417 | 0.15919 | 0.15919 |
| D | setup_RISE→E | 0.06965 | 0.07461 | 0.08954 |
| RDN | setup_RISE→E | 0.07461 | 0.07461 | 0.08954 |
| RDN | hold_RISE→E | -0.04476 | -0.03980 | -0.04975 |
| SDN | setup_RISE→E | 0.18407 | 0.17910 | 0.18407 |
| SDN | hold_RISE→E | -0.14926 | -0.13930 | -0.14926 |
| SDN | non_seq_hold_RISE→RDN | -0.12935 | -0.13433 | -0.15921 |
| SDN | non_seq_setup_RISE→RDN | 0.15423 | 0.16915 | 0.18906 |
| E | minpwh | 0.08555 | 0.07367 | 0.08945 |
| RDN | minpwl | 0.11322 | 0.12113 | 0.14483 |
| SDN | minpwl | 0.07767 | 0.08162 | 0.08952 |

LAHSNHS

Cell Description

Latch
Q = !SDN ? 1 : E ? D : pre_Q
QN = !Q



Function Table

| SDN | E | D | Q |
|-----|---|---|------|
| 0 | X | X | 1 |
| 1 | 0 | X | Q<1> |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| LAHSNHSV1 | 1.80 | 4.00 |
| LAHSNHSV2 | 1.80 | 4.40 |
| LAHSNHSV4 | 1.80 | 4.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| D | 0.00007 | 0.00009 | 0.00009 |
| E | 0.00211 | 0.00235 | 0.00245 |
| Q | 0.00174 | 0.00228 | 0.00328 |
| QN | 0.00173 | 0.00222 | 0.00313 |
| SDN | 0.00096 | 0.00098 | 0.00098 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| D | 0.00129 | 0.00146 | 0.00154 |
| E | 0.00113 | 0.00134 | 0.00135 |
| SDN | 0.00113 | 0.00103 | 0.00102 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00051773 | 0.00061705 | 0.00086545 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| D→Q_FALL | 0.11487 | 0.11212 | 0.12508 |
| D→Q_RISE | 0.06504 | 0.06550 | 0.06691 |
| E→Q_FALL | 0.12385 | 0.11507 | 0.12754 |
| E→Q_RISE | 0.11055 | 0.10118 | 0.10158 |
| SDN→Q_RISE | 0.07828 | 0.08653 | 0.09150 |
| SDN→Q_FALL | 0.13490 | 0.13494 | 0.14733 |
| D→QN_FALL | 0.09700 | 0.09836 | 0.10702 |
| D→QN_RISE | 0.15477 | 0.15348 | 0.17976 |
| E→QN_FALL | 0.14275 | 0.13424 | 0.14195 |
| E→QN_RISE | 0.16409 | 0.15637 | 0.18233 |
| SDN→QN_FALL | 0.10868 | 0.11863 | 0.13168 |
| SDN→QN_RISE | 0.17506 | 0.17613 | 0.20200 |

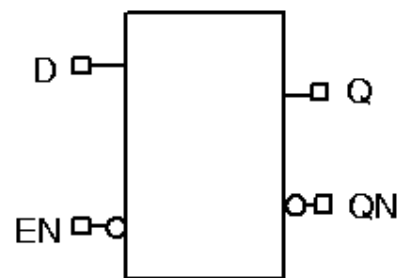
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|--------------|----------|----------|----------|
| D | hold_FALL→E | -0.08458 | -0.08458 | -0.10945 |
| D | hold_RISE→E | -0.00000 | -0.00994 | -0.01493 |
| D | setup_FALL→E | 0.10944 | 0.11940 | 0.13929 |
| D | setup_RISE→E | 0.01492 | 0.03482 | 0.04975 |
| SDN | setup_RISE→E | 0.12935 | 0.13929 | 0.15919 |
| SDN | hold_RISE→E | -0.10447 | -0.10945 | -0.12936 |
| E | minpwh | 0.06182 | 0.05783 | 0.06176 |
| SDN | minpwl | 0.06177 | 0.06574 | 0.07363 |

LALHS

Cell Description

Low Enable Latch
 $Q = !EN ? D : \text{pre_}Q$
 $QN = !Q$



Function Table

| EN | D | Q |
|----|---|------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| LALHSV1 | 1.80 | 3.20 |
| LALHSV2 | 1.80 | 3.40 |
| LALHSV4 | 1.80 | 3.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| D | 0.00003 | 0.00005 | 0.00006 |
| EN | 0.00188 | 0.00233 | 0.00244 |
| Q | 0.00034 | 0.00038 | 0.00112 |
| QN | 0.00036 | 0.00038 | 0.00112 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| D | 0.00117 | 0.00142 | 0.00154 |
| EN | 0.00109 | 0.00134 | 0.00137 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00037155 | 0.00048777 | 0.00071481 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| D→Q_FALL | 0.08087 | 0.07353 | 0.07903 |
| D→Q_RISE | 0.06246 | 0.05815 | 0.06157 |
| EN→Q_FALL | 0.12536 | 0.11189 | 0.11758 |
| EN→Q_RISE | 0.08896 | 0.08195 | 0.08614 |
| D→QN_FALL | 0.09429 | 0.08940 | 0.09794 |
| D→QN_RISE | 0.11527 | 0.10838 | 0.11932 |
| EN→QN_FALL | 0.12118 | 0.11363 | 0.12276 |
| EN→QN_RISE | 0.16005 | 0.14695 | 0.15805 |

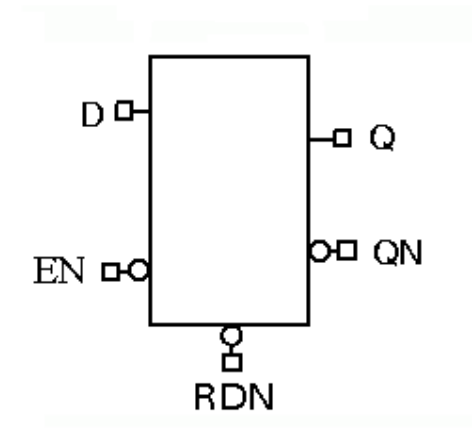
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→EN | -0.03482 | -0.02984 | -0.03979 |
| D | hold_RISE→EN | -0.03483 | -0.03482 | -0.03980 |
| D | setup_FALL→EN | 0.04974 | 0.05473 | 0.06468 |
| D | setup_RISE→EN | 0.04976 | 0.05472 | 0.06964 |
| EN | minpwl | 0.07369 | 0.06971 | 0.07367 |

LALRNHS

Cell Description

Latch
 $Q = \text{!RDN} ? 0 : \text{!EN} ? D : \text{pre_Q}$
 $QN = \text{!Q}$



Function Table

| RDN | EN | D | Q |
|-----|----|---|------|
| 0 | X | X | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| LALRNHSV1 | 1.80 | 3.60 |
| LALRNHSV2 | 1.80 | 3.60 |
| LALRNHSV4 | 1.80 | 4.20 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| D | 0.00001 | 0.00002 | 0.00003 |
| EN | 0.00194 | 0.00232 | 0.00249 |
| Q | 0.00104 | 0.00122 | 0.00216 |
| QN | 0.00104 | 0.00121 | 0.00209 |
| RDN | 0.00004 | 0.00004 | 0.00005 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| D | 0.00114 | 0.00135 | 0.00147 |
| EN | 0.00107 | 0.00132 | 0.00128 |
| RDN | 0.00155 | 0.00165 | 0.00158 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00040852 | 0.00050106 | 0.00075509 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| D→Q_FALL | 0.08465 | 0.07657 | 0.08055 |
| D→Q_RISE | 0.09999 | 0.09030 | 0.08814 |
| EN→Q_FALL | 0.12840 | 0.11311 | 0.11823 |
| EN→Q_RISE | 0.11359 | 0.10020 | 0.10423 |
| RDN→Q_FALL | 0.05182 | 0.05512 | 0.06082 |
| RDN→Q_RISE | 0.09918 | 0.08884 | 0.08487 |
| D→QN_FALL | 0.14188 | 0.13026 | 0.13241 |
| D→QN_RISE | 0.12347 | 0.11581 | 0.12426 |
| EN→QN_FALL | 0.15596 | 0.14053 | 0.14873 |
| EN→QN_RISE | 0.16767 | 0.15259 | 0.16226 |
| RDN→QN_RISE | 0.08783 | 0.09371 | 0.10459 |
| RDN→QN_FALL | 0.14131 | 0.12883 | 0.12925 |

Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→EN | -0.03979 | -0.03483 | -0.04478 |
| D | hold_RISE→EN | -0.07462 | -0.06964 | -0.06965 |
| D | setup_FALL→EN | 0.05971 | 0.06467 | 0.07463 |
| D | setup_RISE→EN | 0.09452 | 0.09452 | 0.09950 |
| RDN | setup_RISE→EN | 0.09451 | 0.09451 | 0.09950 |
| RDN | hold_RISE→EN | -0.07462 | -0.06965 | -0.06965 |
| EN | minpwl | 0.09742 | 0.08549 | 0.09340 |
| RDN | minpwl | 0.06183 | 0.06578 | 0.07764 |

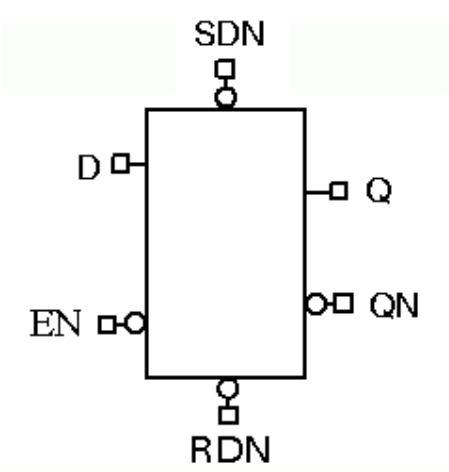
LALRSNHS

Cell Description

Low Enable Latch with Clear and Set

$Q = \text{!SDN} ? 1 : \text{!RDN} ? 0 : \text{!EN} ? D : \text{pre_Q}$

$QN = \text{!Q}$



Function Table

| RDN | SDN | EN | D | Q |
|-----|-----|----|---|------|
| 0 | 0 | X | X | 1 |
| 0 | 1 | X | X | 0 |
| 1 | 0 | X | X | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| LALRSNHSV1 | 1.80 | 5.00 |
| LALRSNHSV2 | 1.80 | 5.20 |
| LALRSNHSV4 | 1.80 | 5.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| D | 0.00004 | 0.00006 | 0.00006 |
| EN | 0.00191 | 0.00233 | 0.00233 |
| Q | 0.00185 | 0.00223 | 0.00335 |
| QN | 0.00183 | 0.00219 | 0.00315 |
| RDN | 0.00003 | 0.00004 | 0.00004 |
| SDN | 0.00112 | 0.00114 | 0.00114 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| D | 0.00123 | 0.00165 | 0.00153 |
| EN | 0.00111 | 0.00131 | 0.00105 |

| | | | |
|-----|---------|---------|---------|
| RDN | 0.00152 | 0.00167 | 0.00177 |
| SDN | 0.00112 | 0.00110 | 0.00109 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00052843 | 0.00059979 | 0.00082063 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| D→Q_FALL | 0.13713 | 0.13418 | 0.14814 |
| D→Q_RISE | 0.09238 | 0.09132 | 0.10271 |
| EN→Q_FALL | 0.16566 | 0.15669 | 0.17802 |
| EN→Q_RISE | 0.10652 | 0.09787 | 0.11731 |
| RDN→Q_FALL | 0.10742 | 0.12244 | 0.13220 |
| RDN→Q_RISE | 0.08971 | 0.08625 | 0.09702 |
| SDN→Q_FALL | 0.13212 | 0.14090 | 0.15093 |
| SDN→Q_RISE | 0.09041 | 0.10641 | 0.11274 |
| D→QN_FALL | 0.12925 | 0.12657 | 0.14912 |
| D→QN_RISE | 0.18119 | 0.18000 | 0.20622 |
| EN→QN_FALL | 0.14375 | 0.13347 | 0.16398 |
| EN→QN_RISE | 0.20929 | 0.20220 | 0.23583 |
| RDN→QN_RISE | 0.15146 | 0.17280 | 0.19531 |
| RDN→QN_FALL | 0.12663 | 0.12156 | 0.14350 |
| SDN→QN_FALL | 0.12345 | 0.14076 | 0.15714 |
| SDN→QN_RISE | 0.17322 | 0.18636 | 0.20809 |

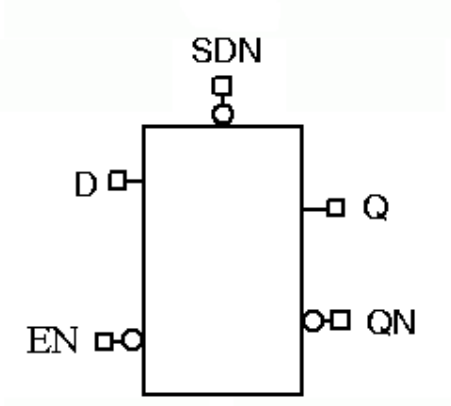
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|------------------------|----------|----------|----------|
| D | hold_FALL→EN | -0.08955 | -0.08954 | -0.10446 |
| D | hold_RISE→EN | -0.06964 | -0.06965 | -0.08456 |
| D | setup_FALL→EN | 0.11442 | 0.11941 | 0.13929 |
| D | setup_RISE→EN | 0.10945 | 0.12437 | 0.13431 |
| RDN | setup_RISE→EN | 0.10446 | 0.11940 | 0.12933 |
| RDN | hold_RISE→EN | -0.06964 | -0.06963 | -0.08456 |
| SDN | setup_RISE→EN | 0.14427 | 0.14926 | 0.16914 |
| SDN | hold_RISE→EN | -0.11940 | -0.11940 | -0.13432 |
| SDN | non_seq_hold_RISE→RDN | -0.12438 | -0.13931 | -0.15921 |
| SDN | non_seq_setup_RISE→RDN | 0.14926 | 0.17413 | 0.18905 |
| EN | minpwl | 0.09340 | 0.08555 | 0.10926 |
| RDN | minpwl | 0.10928 | 0.12905 | 0.14882 |
| SDN | minpwl | 0.07371 | 0.08558 | 0.09349 |

LALSNHS

Cell Description

Latch
Q = !SDN ? 1 : !EN ? D : pre_Q
QN = !Q



Function Table

| SDN | EN | D | Q |
|-----|----|---|------|
| 0 | X | X | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| LALSNHVS1 | 1.80 | 4.00 |
| LALSNHVS2 | 1.80 | 4.40 |
| LALSNHVS4 | 1.80 | 4.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| D | 0.00007 | 0.00009 | 0.00009 |
| EN | 0.00208 | 0.00233 | 0.00245 |
| Q | 0.00095 | 0.00129 | 0.00221 |
| QN | 0.00093 | 0.00124 | 0.00205 |
| SDN | 0.00090 | 0.00095 | 0.00096 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| D | 0.00124 | 0.00148 | 0.00158 |
| EN | 0.00113 | 0.00137 | 0.00136 |
| SDN | 0.00107 | 0.00102 | 0.00102 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00050296 | 0.00062339 | 0.00085114 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| D→Q_FALL | 0.11581 | 0.11051 | 0.11932 |
| D→Q_RISE | 0.06803 | 0.06434 | 0.06555 |
| EN→Q_FALL | 0.15318 | 0.13546 | 0.14413 |
| EN→Q_RISE | 0.09350 | 0.08712 | 0.09051 |
| SDN→Q_FALL | 0.13616 | 0.13292 | 0.14192 |
| SDN→Q_RISE | 0.07668 | 0.08473 | 0.08962 |
| D→QN_FALL | 0.09992 | 0.09664 | 0.10539 |
| D→QN_RISE | 0.15545 | 0.15089 | 0.17279 |
| EN→QN_FALL | 0.12628 | 0.11976 | 0.13058 |
| EN→QN_RISE | 0.19311 | 0.17594 | 0.19750 |
| SDN→QN_FALL | 0.10690 | 0.11636 | 0.12911 |
| SDN→QN_RISE | 0.17571 | 0.17333 | 0.19521 |

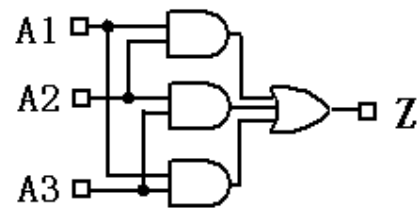
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→EN | -0.06467 | -0.06466 | -0.08457 |
| D | hold_RISE→EN | -0.03980 | -0.04476 | -0.04975 |
| D | setup_FALL→EN | 0.08458 | 0.08955 | 0.10945 |
| D | setup_RISE→EN | 0.06466 | 0.07463 | 0.08954 |
| SDN | setup_RISE→EN | 0.10944 | 0.11939 | 0.13930 |
| SDN | hold_RISE→EN | -0.08954 | -0.09453 | -0.10946 |
| EN | minpwl | 0.07767 | 0.07367 | 0.08153 |
| SDN | minpwl | 0.06177 | 0.06579 | 0.07372 |

MAJ23HS

Cell Description

3-input majority gate (2-out-of-3)
 $Z = ((A1 \& A2) | (A2 \& A3) | (A1 \& A3))$



Function Table

| A2 | A3 | A1 | Z |
|----|----|----|---|
| 0 | 0 | X | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| MAJ23HSV0 | 1.80 | 1.80 |
| MAJ23HSV1 | 1.80 | 1.80 |
| MAJ23HSV2 | 1.80 | 1.80 |
| MAJ23HSV4 | 1.80 | 2.00 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00146 | 0.00170 | 0.00186 | 0.00298 |
| A2 | 0.00144 | 0.00169 | 0.00186 | 0.00301 |
| A3 | 0.00122 | 0.00145 | 0.00158 | 0.00261 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00193 | 0.00199 | 0.00212 | 0.00280 |
| A2 | 0.00155 | 0.00162 | 0.00174 | 0.00240 |
| A3 | 0.00095 | 0.00096 | 0.00098 | 0.00134 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00017787 | 0.00019499 | 0.00020053 | 0.00040532 |

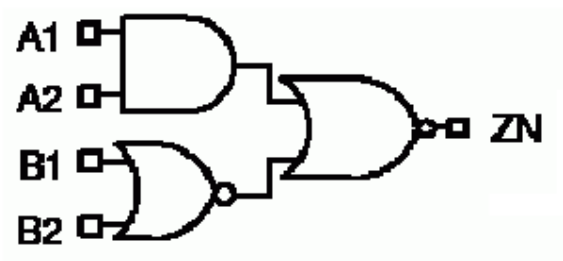
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.09003 | 0.08851 | 0.08681 | 0.07594 |
| A1→Z_RISE | 0.06018 | 0.06065 | 0.06131 | 0.05360 |
| A2→Z_FALL | 0.08694 | 0.08582 | 0.08437 | 0.07582 |
| A2→Z_RISE | 0.05837 | 0.05911 | 0.05975 | 0.05377 |
| A3→Z_FALL | 0.07097 | 0.06951 | 0.06662 | 0.06061 |
| A3→Z_RISE | 0.05068 | 0.05015 | 0.04900 | 0.04586 |

MAOI22HS

Cell Description

the logical NOR of one AND2 and one NOR2 block.
 $ZN = \neg((A1 \& A2) | (\neg(B1 \& B2)))$



Function Table

| A1 | A2 | B1 | B2 | ZN |
|----|----|----|----|----|
| 0 | X | 0 | 0 | 0 |
| 0 | X | 0 | 1 | 1 |
| 0 | X | 1 | X | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | X | 1 |
| 1 | 1 | X | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| MAOI22HSV0 | 1.80 | 1.80 |
| MAOI22HSV1 | 1.80 | 1.80 |
| MAOI22HSV2 | 1.80 | 1.80 |
| MAOI22HSV4 | 1.80 | 2.40 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00072 | 0.00090 | 0.00115 | 0.00212 |
| A2 | 0.00079 | 0.00100 | 0.00132 | 0.00252 |
| B1 | 0.00143 | 0.00161 | 0.00181 | 0.00309 |
| B2 | 0.00134 | 0.00152 | 0.00173 | 0.00292 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00107 | 0.00131 | 0.00153 | 0.00281 |
| A2 | 0.00098 | 0.00118 | 0.00151 | 0.00308 |

| | | | | |
|----|---------|---------|---------|---------|
| B1 | 0.00104 | 0.00102 | 0.00094 | 0.00138 |
| B2 | 0.00119 | 0.00116 | 0.00106 | 0.00148 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00018113 | 0.00022876 | 0.00030719 | 0.00064578 |

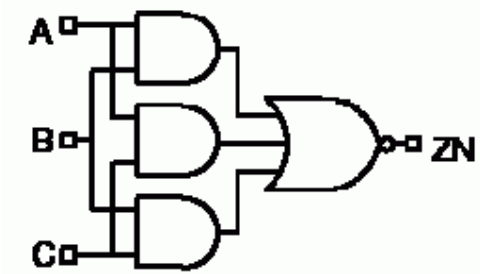
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.02871 | 0.02516 | 0.02152 | 0.01815 |
| A1→ZN_RISE | 0.03853 | 0.03490 | 0.03207 | 0.02847 |
| A2→ZN_FALL | 0.02995 | 0.02649 | 0.02361 | 0.02093 |
| A2→ZN_RISE | 0.04202 | 0.03852 | 0.03612 | 0.03355 |
| B1→ZN_FALL | 0.06156 | 0.06273 | 0.06404 | 0.06458 |
| B1→ZN_RISE | 0.04929 | 0.04713 | 0.04575 | 0.04208 |
| B2→ZN_FALL | 0.06003 | 0.06116 | 0.06269 | 0.06195 |
| B2→ZN_RISE | 0.04785 | 0.04548 | 0.04392 | 0.03964 |

MAOI222HS

Cell Description

Inverting 2 of 3 MAJORITY
 $ZN = \neg((A \& B) | (B \& C) | (A \& C))$



Function Table

| A | B | C | ZN |
|---|---|---|----|
| 0 | 0 | X | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| MAOI222HSV0 | 1.80 | 2.00 |
| MAOI222HSV1 | 1.80 | 2.00 |
| MAOI222HSV2 | 1.80 | 2.00 |
| MAOI222HSV4 | 1.80 | 3.60 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A | 0.00113 | 0.00137 | 0.00175 | 0.00323 |
| B | 0.00129 | 0.00161 | 0.00208 | 0.00388 |
| C | 0.00139 | 0.00175 | 0.00229 | 0.00446 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A | 0.00206 | 0.00243 | 0.00302 | 0.00564 |
| B | 0.00202 | 0.00245 | 0.00300 | 0.00600 |
| C | 0.00193 | 0.00231 | 0.00292 | 0.00562 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00014020 | 0.00019915 | 0.00030043 | 0.00052759 |

Delay Table (ns)

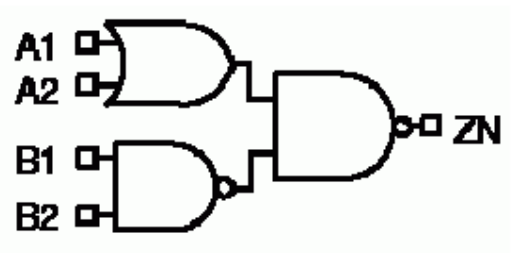
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A→ZN_FALL | 0.03925 | 0.03380 | 0.02921 | 0.02555 |
| A→ZN_RISE | 0.07355 | 0.06592 | 0.06056 | 0.05400 |
| B→ZN_FALL | 0.04232 | 0.03700 | 0.03233 | 0.02869 |
| B→ZN_RISE | 0.07781 | 0.07108 | 0.06635 | 0.06021 |
| C→ZN_FALL | 0.04330 | 0.03787 | 0.03342 | 0.03170 |
| C→ZN_RISE | 0.07918 | 0.07256 | 0.06865 | 0.06454 |

MOAI22HS

Cell Description

the logical NAND of one OR2 and one NAND2 block.

$$ZN = \neg((A1 \vee A2) \wedge \neg(B1 \wedge B2))$$



Function Table

| A1 | A2 | B1 | B2 | ZN |
|----|----|----|----|----|
| 0 | 0 | X | X | 1 |
| 0 | 1 | 0 | X | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | X | 0 | X | 0 |
| 1 | X | 1 | 0 | 0 |
| 1 | X | 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| MOAI22HSV0 | 1.80 | 1.60 |
| MOAI22HSV1 | 1.80 | 1.80 |
| MOAI22HSV2 | 1.80 | 1.80 |
| MOAI22HSV4 | 1.80 | 2.40 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00062 | 0.00082 | 0.00107 | 0.00194 |
| A2 | 0.00074 | 0.00098 | 0.00133 | 0.00250 |
| B1 | 0.00130 | 0.00158 | 0.00186 | 0.00306 |
| B2 | 0.00136 | 0.00164 | 0.00192 | 0.00315 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00099 | 0.00124 | 0.00155 | 0.00282 |
| A2 | 0.00097 | 0.00121 | 0.00151 | 0.00312 |

| | | | | |
|----|---------|---------|---------|---------|
| B1 | 0.00120 | 0.00119 | 0.00118 | 0.00157 |
| B2 | 0.00102 | 0.00104 | 0.00103 | 0.00134 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00016363 | 0.00018889 | 0.00022017 | 0.00043150 |

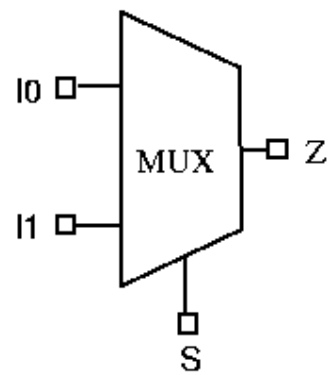
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.02871 | 0.02569 | 0.02342 | 0.02082 |
| A1→ZN_RISE | 0.03677 | 0.03404 | 0.03150 | 0.02729 |
| A2→ZN_FALL | 0.03204 | 0.02895 | 0.02708 | 0.02454 |
| A2→ZN_RISE | 0.03935 | 0.03682 | 0.03517 | 0.03186 |
| B1→ZN_FALL | 0.04680 | 0.04708 | 0.04721 | 0.04399 |
| B1→ZN_RISE | 0.05063 | 0.05325 | 0.05536 | 0.05218 |
| B2→ZN_FALL | 0.04807 | 0.04851 | 0.04873 | 0.04534 |
| B2→ZN_RISE | 0.05127 | 0.05412 | 0.05634 | 0.05318 |

MUX2HS

Cell Description

2-to-1 Multiplexer
 $Z=((I0\&(!S))|(I1\&S))$



Function Table

| S | I0 | I1 | Z |
|---|----|----|---|
| 0 | 0 | X | 0 |
| 0 | 1 | X | 1 |
| 1 | X | 0 | 0 |
| 1 | X | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| MUX2HSV0 | 1.80 | 2.00 |
| MUX2HSV1 | 1.80 | 2.00 |
| MUX2HSV2 | 1.80 | 2.00 |
| MUX2HSV4 | 1.80 | 3.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| I0 | 0.00161 | 0.00176 | 0.00221 | 0.00429 |
| I1 | 0.00155 | 0.00170 | 0.00218 | 0.00426 |
| S | 0.00185 | 0.00200 | 0.00245 | 0.00451 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| I0 | 0.00105 | 0.00105 | 0.00124 | 0.00242 |
| I1 | 0.00117 | 0.00116 | 0.00142 | 0.00235 |
| S | 0.00196 | 0.00196 | 0.00211 | 0.00339 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00034454 | 0.00035462 | 0.00042939 | 0.00093049 |

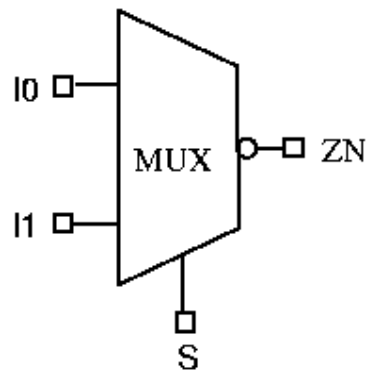
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| I0→Z_FALL | 0.06235 | 0.06301 | 0.05919 | 0.05399 |
| I0→Z_RISE | 0.05481 | 0.05515 | 0.05197 | 0.04900 |
| I1→Z_FALL | 0.06172 | 0.06239 | 0.05773 | 0.05502 |
| I1→Z_RISE | 0.05268 | 0.05299 | 0.04867 | 0.04692 |
| S→Z_FALL | 0.05542 | 0.05622 | 0.05333 | 0.05020 |
| S→Z_RISE | 0.05077 | 0.05107 | 0.04916 | 0.04610 |

MUX2NHS

Cell Description

2-to-1 Inverting Multiplexer
 $ZN = \neg((I0 \& \neg S) | (I1 \& S))$



Function Table

| S | I0 | I1 | ZN |
|---|----|----|----|
| 0 | 0 | X | 1 |
| 0 | 1 | X | 0 |
| 1 | X | 0 | 1 |
| 1 | X | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| MUX2NHSV0 | 1.80 | 1.60 |
| MUX2NHSV1 | 1.80 | 1.60 |
| MUX2NHSV2 | 1.80 | 2.00 |
| MUX2NHSV4 | 1.80 | 3.20 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| I0 | 0.00096 | 0.00119 | 0.00151 | 0.00270 |
| I1 | 0.00082 | 0.00106 | 0.00152 | 0.00268 |
| S | 0.00114 | 0.00137 | 0.00181 | 0.00306 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| I0 | 0.00098 | 0.00120 | 0.00159 | 0.00284 |
| I1 | 0.00107 | 0.00130 | 0.00160 | 0.00282 |
| S | 0.00198 | 0.00215 | 0.00288 | 0.00387 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00027261 | 0.00034314 | 0.00049494 | 0.00087282 |

Delay Table (ns)

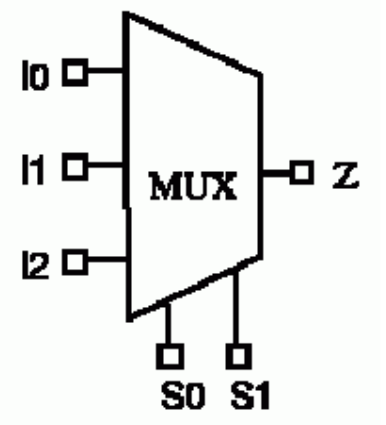
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| I0→ZN_FALL | 0.02990 | 0.02694 | 0.02366 | 0.02237 |
| I0→ZN_RISE | 0.03430 | 0.03046 | 0.02736 | 0.02654 |
| I1→ZN_FALL | 0.02653 | 0.02398 | 0.02286 | 0.02009 |
| I1→ZN_RISE | 0.03222 | 0.02960 | 0.02961 | 0.02883 |
| S→ZN_FALL | 0.02553 | 0.02504 | 0.02333 | 0.02458 |
| S→ZN_RISE | 0.02745 | 0.02643 | 0.02555 | 0.02588 |

MUX3HS

Cell Description

3-to-1 Multiplexer

$$Z=((I0\&(!S0)\&(!S1))|(I1\&S0\&(!S1))|(I2\&S1))$$



Function Table

| S1 | S0 | I0 | I1 | I2 | Z |
|----|----|----|----|----|---|
| 0 | 0 | 0 | X | X | 0 |
| 0 | 0 | 1 | X | X | 1 |
| 0 | 1 | X | 0 | X | 0 |
| 0 | 1 | X | 1 | X | 1 |
| 1 | X | X | X | 0 | 0 |
| 1 | X | X | X | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| MUX3HSV0 | 1.80 | 3.40 |
| MUX3HSV1 | 1.80 | 3.40 |
| MUX3HSV2 | 1.80 | 3.40 |
| MUX3HSV4 | 1.80 | 5.40 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| I0 | 0.00237 | 0.00273 | 0.00307 | 0.00570 |
| I1 | 0.00234 | 0.00272 | 0.00306 | 0.00581 |
| I2 | 0.00159 | 0.00189 | 0.00212 | 0.00372 |
| S0 | 0.00258 | 0.00297 | 0.00332 | 0.00607 |
| S1 | 0.00188 | 0.00221 | 0.00247 | 0.00410 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| I0 | 0.00111 | 0.00121 | 0.00134 | 0.00229 |
| I1 | 0.00103 | 0.00110 | 0.00124 | 0.00231 |

| | | | | |
|----|---------|---------|---------|---------|
| I2 | 0.00112 | 0.00119 | 0.00134 | 0.00178 |
| S0 | 0.00186 | 0.00196 | 0.00219 | 0.00356 |
| S1 | 0.00169 | 0.00188 | 0.00209 | 0.00285 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00052796 | 0.00060151 | 0.00073441 | 0.00130030 |

Delay Table (ns)

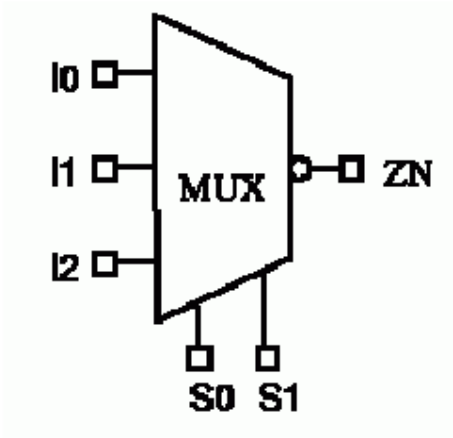
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| I0→Z_FALL | 0.11874 | 0.11398 | 0.10726 | 0.08809 |
| I0→Z_RISE | 0.09806 | 0.09412 | 0.08672 | 0.07899 |
| I1→Z_FALL | 0.11906 | 0.11500 | 0.10851 | 0.09060 |
| I1→Z_RISE | 0.09558 | 0.09343 | 0.08653 | 0.07943 |
| I2→Z_FALL | 0.06925 | 0.06666 | 0.06255 | 0.06319 |
| I2→Z_RISE | 0.05612 | 0.05387 | 0.04972 | 0.05170 |
| S0→Z_FALL | 0.11228 | 0.10820 | 0.10164 | 0.08681 |
| S0→Z_RISE | 0.09382 | 0.09091 | 0.08406 | 0.07864 |
| S1→Z_FALL | 0.06490 | 0.06296 | 0.05882 | 0.05625 |
| S1→Z_RISE | 0.06073 | 0.05905 | 0.05471 | 0.05275 |

MUX3NHS

Cell Description

3-to-1 Inverting Multiplexer

$$Z_N = \neg((I_0 \& \neg S_0) \& \neg S_1) \vee (I_1 \& S_0 \& \neg S_1) \vee (I_2 \& S_1))$$



Function Table

| S1 | S0 | I0 | I1 | I2 | ZN |
|----|----|----|----|----|----|
| 0 | 0 | 0 | X | X | 1 |
| 0 | 0 | 1 | X | X | 0 |
| 0 | 1 | X | 0 | X | 1 |
| 0 | 1 | X | 1 | X | 0 |
| 1 | X | X | X | 0 | 1 |
| 1 | X | X | X | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| MUX3NHSV0 | 1.80 | 4.20 |
| MUX3NHSV1 | 1.80 | 4.20 |
| MUX3NHSV2 | 1.80 | 4.20 |
| MUX3NHSV4 | 1.80 | 6.00 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| I0 | 0.00285 | 0.00363 | 0.00387 | 0.00694 |
| I1 | 0.00286 | 0.00364 | 0.00388 | 0.00685 |
| I2 | 0.00230 | 0.00284 | 0.00305 | 0.00589 |
| S0 | 0.00322 | 0.00398 | 0.00428 | 0.00727 |
| S1 | 0.00199 | 0.00240 | 0.00263 | 0.00480 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| I0 | 0.00111 | 0.00139 | 0.00139 | 0.00177 |
| I1 | 0.00103 | 0.00127 | 0.00127 | 0.00162 |

| | | | | |
|----|---------|---------|---------|---------|
| I2 | 0.00103 | 0.00105 | 0.00106 | 0.00152 |
| S0 | 0.00191 | 0.00205 | 0.00230 | 0.00308 |
| S1 | 0.00195 | 0.00211 | 0.00212 | 0.00345 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00069700 | 0.00083759 | 0.00085663 | 0.00154330 |

Delay Table (ns)

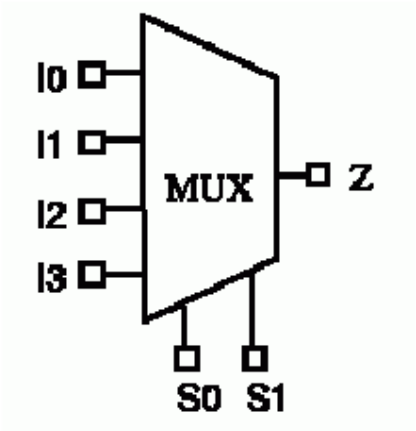
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| I0→ZN_FALL | 0.10385 | 0.09667 | 0.09763 | 0.09797 |
| I0→ZN_RISE | 0.10790 | 0.09999 | 0.10150 | 0.10688 |
| I1→ZN_FALL | 0.10311 | 0.09606 | 0.09755 | 0.09528 |
| I1→ZN_RISE | 0.10951 | 0.10169 | 0.10273 | 0.10687 |
| I2→ZN_FALL | 0.08046 | 0.07845 | 0.07937 | 0.07647 |
| I2→ZN_RISE | 0.07611 | 0.07482 | 0.07587 | 0.07653 |
| S0→ZN_FALL | 0.10178 | 0.09624 | 0.09533 | 0.09377 |
| S0→ZN_RISE | 0.10426 | 0.09757 | 0.09742 | 0.10064 |
| S1→ZN_FALL | 0.05851 | 0.05525 | 0.05660 | 0.05238 |
| S1→ZN_RISE | 0.05329 | 0.05079 | 0.05174 | 0.04956 |

MUX4HS

Cell Description

4-to-1 Multiplexer

$$Z=((I0\&(!S0)\&(!S1))|(I1\&S0\&(!S1))|(I2\&(!S0)\&S1)|(I3\&S0\&S1))$$



Function Table

| S1 | S0 | I0 | I1 | I2 | I3 | Z |
|----|----|----|----|----|----|---|
| 0 | 0 | 0 | X | X | X | 0 |
| 0 | 0 | 1 | X | X | X | 1 |
| 0 | 1 | X | 0 | X | X | 0 |
| 0 | 1 | X | 1 | X | X | 1 |
| 1 | 0 | X | X | 0 | X | 0 |
| 1 | 0 | X | X | 1 | X | 1 |
| 1 | 1 | X | X | X | 0 | 0 |
| 1 | 1 | X | X | X | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| MUX4HSV0 | 1.80 | 4.80 |
| MUX4HSV1 | 1.80 | 5.40 |
| MUX4HSV2 | 1.80 | 5.40 |
| MUX4HSV4 | 1.80 | 6.20 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| I0 | 0.00234 | 0.00320 | 0.00344 | 0.00504 |
| I1 | 0.00235 | 0.00316 | 0.00340 | 0.00499 |
| I2 | 0.00213 | 0.00305 | 0.00328 | 0.00484 |
| I3 | 0.00217 | 0.00294 | 0.00318 | 0.00484 |
| S0 | 0.00359 | 0.00458 | 0.00482 | 0.00665 |
| S1 | 0.00175 | 0.00230 | 0.00253 | 0.00382 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| I0 | 0.00108 | 0.00128 | 0.00128 | 0.00163 |
| I1 | 0.00104 | 0.00131 | 0.00131 | 0.00168 |
| I2 | 0.00112 | 0.00129 | 0.00129 | 0.00161 |
| I3 | 0.00104 | 0.00140 | 0.00139 | 0.00177 |
| S0 | 0.00306 | 0.00436 | 0.00436 | 0.00539 |
| S1 | 0.00195 | 0.00244 | 0.00243 | 0.00308 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00074434 | 0.00098193 | 0.00100580 | 0.00160070 |

Delay Table (ns)

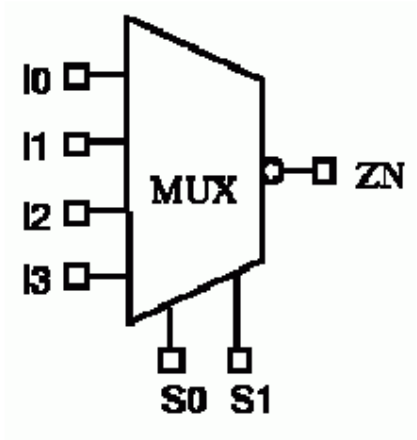
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| I0→Z_FALL | 0.10672 | 0.10465 | 0.10676 | 0.10507 |
| I0→Z_RISE | 0.08903 | 0.09096 | 0.09297 | 0.08713 |
| I1→Z_FALL | 0.10809 | 0.10514 | 0.10722 | 0.10578 |
| I1→Z_RISE | 0.08818 | 0.08789 | 0.08986 | 0.08450 |
| I2→Z_FALL | 0.09950 | 0.10115 | 0.10324 | 0.10181 |
| I2→Z_RISE | 0.08308 | 0.08533 | 0.08723 | 0.08167 |
| I3→Z_FALL | 0.10217 | 0.10009 | 0.10218 | 0.10290 |
| I3→Z_RISE | 0.08226 | 0.08323 | 0.08516 | 0.08245 |
| S0→Z_FALL | 0.10511 | 0.09868 | 0.10075 | 0.09908 |
| S0→Z_RISE | 0.09028 | 0.08470 | 0.08661 | 0.08131 |
| S1→Z_FALL | 0.06153 | 0.05907 | 0.06127 | 0.06312 |
| S1→Z_RISE | 0.05289 | 0.05475 | 0.05646 | 0.05470 |

MUX4NHS

Cell Description

4-to-1 Inverting Multiplexer

$$Z_N = \neg((I_0 \& \neg(S_0) \& \neg(S_1)) \vee (I_1 \& S_0 \& \neg(S_1)) \vee (I_2 \& \neg(S_0) \& S_1) \vee (I_3 \& S_0 \& S_1))$$



Function Table

| S1 | S0 | I0 | I1 | I2 | I3 | ZN |
|----|----|----|----|----|----|----|
| 0 | 0 | 0 | X | X | X | 1 |
| 0 | 0 | 1 | X | X | X | 0 |
| 0 | 1 | X | 0 | X | X | 1 |
| 0 | 1 | X | 1 | X | X | 0 |
| 1 | 0 | X | X | 0 | X | 1 |
| 1 | 0 | X | X | 1 | X | 0 |
| 1 | 1 | X | X | X | 0 | 1 |
| 1 | 1 | X | X | X | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| MUX4NHSV0 | 1.80 | 5.40 |
| MUX4NHSV1 | 1.80 | 5.40 |
| MUX4NHSV2 | 1.80 | 5.80 |
| MUX4NHSV4 | 1.80 | 7.60 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| I0 | 0.00304 | 0.00350 | 0.00491 | 0.00730 |
| I1 | 0.00306 | 0.00353 | 0.00492 | 0.00729 |
| I2 | 0.00290 | 0.00337 | 0.00447 | 0.00678 |
| I3 | 0.00293 | 0.00341 | 0.00445 | 0.00672 |
| S0 | 0.00458 | 0.00517 | 0.00675 | 0.00960 |
| S1 | 0.00190 | 0.00226 | 0.00298 | 0.00451 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| I0 | 0.00109 | 0.00109 | 0.00126 | 0.00163 |
| I1 | 0.00107 | 0.00107 | 0.00130 | 0.00165 |
| I2 | 0.00108 | 0.00108 | 0.00126 | 0.00170 |
| I3 | 0.00103 | 0.00103 | 0.00131 | 0.00176 |
| S0 | 0.00302 | 0.00327 | 0.00432 | 0.00571 |
| S1 | 0.00210 | 0.00225 | 0.00292 | 0.00343 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00087014 | 0.00096178 | 0.00130310 | 0.00198870 |

Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| I0→ZN_FALL | 0.11087 | 0.10830 | 0.10842 | 0.10589 |
| I0→ZN_RISE | 0.11868 | 0.11664 | 0.11474 | 0.11869 |
| I1→ZN_FALL | 0.11130 | 0.10932 | 0.10648 | 0.10382 |
| I1→ZN_RISE | 0.12017 | 0.11775 | 0.11619 | 0.11993 |
| I2→ZN_FALL | 0.10778 | 0.10590 | 0.09950 | 0.09478 |
| I2→ZN_RISE | 0.11116 | 0.11080 | 0.10304 | 0.10564 |
| I3→ZN_FALL | 0.10757 | 0.10591 | 0.09689 | 0.09351 |
| I3→ZN_RISE | 0.11339 | 0.11269 | 0.10358 | 0.10545 |
| S0→ZN_FALL | 0.11471 | 0.10917 | 0.10204 | 0.09680 |
| S0→ZN_RISE | 0.11716 | 0.11337 | 0.10554 | 0.10622 |
| S1→ZN_FALL | 0.05795 | 0.05398 | 0.04964 | 0.04999 |
| S1→ZN_RISE | 0.05238 | 0.04903 | 0.04526 | 0.04736 |

NAND2HS

Cell Description

2-Input NAND

$$Z_N = \neg(A_1 \& A_2)$$



Function Table

| A1 | A2 | ZN |
|----|----|----|
| 0 | X | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| NAND2HSV0 | 1.80 | 0.80 |
| NAND2HSV0P5 | 1.80 | 0.80 |
| NAND2HSV1 | 1.80 | 0.80 |
| NAND2HSV2 | 1.80 | 0.80 |
| NAND2HSV3 | 1.80 | 1.40 |
| NAND2HSV4 | 1.80 | 1.40 |
| NAND2HSV8 | 1.80 | 2.60 |
| NAND2HSV12 | 1.80 | 4.40 |
| NAND2HSV16 | 1.80 | 6.40 |
| NAND2HSV24 | 1.80 | 8.40 |

Pin Power (uW/MHz)

| Pin | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00041 | 0.00046 | 0.00054 | 0.00069 | 0.00104 | 0.00128 | 0.00240 | 0.00385 |
| A2 | 0.00048 | 0.00060 | 0.00065 | 0.00086 | 0.00136 | 0.00177 | 0.00320 | 0.00540 |

| Pin | V16 | V24 |
|-----|---------|---------|
| A1 | 0.00516 | 0.00754 |
| A2 | 0.00731 | 0.01069 |

Pin Capacitance (pf)

| Pin | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00096 | 0.00110 | 0.00120 | 0.00152 | 0.00231 | 0.00278 | 0.00545 | 0.00937 |
| A2 | 0.00091 | 0.00106 | 0.00116 | 0.00147 | 0.00252 | 0.00287 | 0.00590 | 0.00934 |

| Pin | V16 | V24 |
|-----|---------|---------|
| A1 | 0.01309 | 0.01865 |
| A2 | 0.01305 | 0.01877 |

Max Leakage Power (uW)

| V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00010362 | 0.00010406 | 0.00012738 | 0.00014426 | 0.00025252 | 0.00028534 | 0.00056395 | 0.00111540 |

| V16 | V24 |
|------------|------------|
| 0.00155080 | 0.00236760 |

Delay Table (ns)

| Description | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.02195 | 0.01534 | 0.01975 | 0.01726 | 0.01559 | 0.01463 | 0.01374 | 0.01154 |
| A1→ZN_RISE | 0.01615 | 0.01703 | 0.01486 | 0.01346 | 0.01265 | 0.01196 | 0.01127 | 0.01324 |
| A2→ZN_FALL | 0.02344 | 0.01738 | 0.02159 | 0.01929 | 0.01844 | 0.01825 | 0.01654 | 0.01397 |
| A2→ZN_RISE | 0.01749 | 0.01990 | 0.01637 | 0.01515 | 0.01476 | 0.01455 | 0.01351 | 0.01685 |

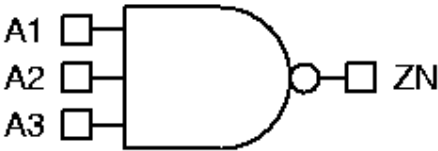
| Description | V16 | V24 |
|-------------|---------|---------|
| A1→ZN_FALL | 0.01142 | 0.01122 |
| A1→ZN_RISE | 0.01305 | 0.01294 |
| A2→ZN_FALL | 0.01391 | 0.01370 |
| A2→ZN_RISE | 0.01665 | 0.01659 |

NAND3HS

Cell Description

3-Input NAND

$$Z_N = \neg(A_1 \& A_2 \& A_3)$$



Function Table

| A1 | A2 | A3 | ZN |
|----|----|----|----|
| 0 | X | X | 1 |
| 1 | 0 | X | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| NAND3HSV0 | 1.80 | 1.00 |
| NAND3HSV0P5 | 1.80 | 1.00 |
| NAND3HSV1 | 1.80 | 1.00 |
| NAND3HSV2 | 1.80 | 1.00 |
| NAND3HSV3 | 1.80 | 1.80 |
| NAND3HSV4 | 1.80 | 2.00 |
| NAND3HSV8 | 1.80 | 2.60 |
| NAND3HSV12 | 1.80 | 5.00 |
| NAND3HSV16 | 1.80 | 5.60 |
| NAND3HSV24 | 1.80 | 8.60 |

Pin Power (uW/MHz)

| Pin | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00054 | 0.00055 | 0.00067 | 0.00089 | 0.00127 | 0.00152 | 0.00613 | 0.00343 |
| A2 | 0.00062 | 0.00071 | 0.00079 | 0.00107 | 0.00159 | 0.00193 | 0.00623 | 0.00528 |
| A3 | 0.00071 | 0.00085 | 0.00091 | 0.00125 | 0.00191 | 0.00232 | 0.00638 | 0.00678 |

| Pin | V16 | V24 |
|-----|---------|---------|
| A1 | 0.00446 | 0.00652 |
| A2 | 0.00680 | 0.01003 |

| | | |
|----|---------|---------|
| A3 | 0.00873 | 0.01296 |
|----|---------|---------|

Pin Capacitance (pf)

| Pin | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00103 | 0.00109 | 0.00125 | 0.00150 | 0.00227 | 0.00266 | 0.00131 | 0.00696 |
| A2 | 0.00101 | 0.00109 | 0.00123 | 0.00150 | 0.00250 | 0.00295 | 0.00127 | 0.00714 |
| A3 | 0.00095 | 0.00104 | 0.00118 | 0.00150 | 0.00271 | 0.00319 | 0.00130 | 0.00731 |

| Pin | V16 | V24 |
|-----|---------|---------|
| A1 | 0.00906 | 0.01329 |
| A2 | 0.00917 | 0.01346 |
| A3 | 0.00939 | 0.01409 |

Max Leakage Power (uW)

| V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00016618 | 0.00015156 | 0.00019728 | 0.00021520 | 0.00039830 | 0.00042429 | 0.00075584 | 0.00126660 |

| V16 | V24 |
|------------|------------|
| 0.00180650 | 0.00289660 |

Delay Table (ns)

| Description | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.03450 | 0.02171 | 0.02974 | 0.02619 | 0.02281 | 0.02133 | 0.10275 | 0.01289 |
| A1→ZN_RISE | 0.01861 | 0.02206 | 0.01655 | 0.01530 | 0.01393 | 0.01320 | 0.06642 | 0.01468 |
| A2→ZN_FALL | 0.03775 | 0.02589 | 0.03342 | 0.03052 | 0.02761 | 0.02656 | 0.10617 | 0.01868 |
| A2→ZN_RISE | 0.02011 | 0.02606 | 0.01827 | 0.01729 | 0.01602 | 0.01562 | 0.06876 | 0.02043 |
| A3→ZN_FALL | 0.04000 | 0.02825 | 0.03575 | 0.03300 | 0.03124 | 0.02994 | 0.11022 | 0.02126 |
| A3→ZN_RISE | 0.02139 | 0.02918 | 0.01951 | 0.01867 | 0.01791 | 0.01734 | 0.07202 | 0.02405 |

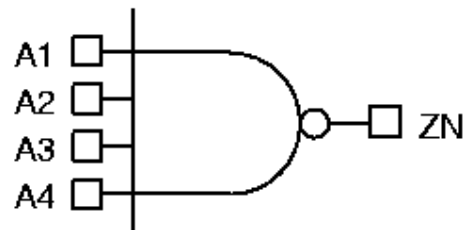
| Description | V16 | V24 |
|-------------|---------|---------|
| A1→ZN_FALL | 0.01261 | 0.01216 |
| A1→ZN_RISE | 0.01459 | 0.01412 |
| A2→ZN_FALL | 0.01791 | 0.01762 |
| A2→ZN_RISE | 0.02025 | 0.01990 |
| A3→ZN_FALL | 0.02036 | 0.01994 |
| A3→ZN_RISE | 0.02388 | 0.02337 |

NAND4HS

Cell Description

4-Input NAND

$$ZN = \neg(A1 \& A2 \& A3 \& A4)$$



Function Table

| A1 | A2 | A3 | A4 | ZN |
|----|----|----|----|----|
| 0 | X | X | X | 1 |
| 1 | 0 | X | X | 1 |
| 1 | 1 | 0 | X | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| NAND4HSV0 | 1.80 | 1.40 |
| NAND4HSV0P5 | 1.80 | 1.40 |
| NAND4HSV1 | 1.80 | 1.40 |
| NAND4HSV2 | 1.80 | 1.40 |
| NAND4HSV3 | 1.80 | 2.40 |
| NAND4HSV4 | 1.80 | 2.40 |
| NAND4HSV8 | 1.80 | 3.00 |
| NAND4HSV12 | 1.80 | 5.40 |
| NAND4HSV16 | 1.80 | 7.40 |
| NAND4HSV24 | 1.80 | 11.00 |

Pin Power (uW/MHz)

| Pin | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00066 | 0.00063 | 0.00077 | 0.00101 | 0.00158 | 0.00192 | 0.00629 | 0.00356 |
| A2 | 0.00077 | 0.00081 | 0.00091 | 0.00118 | 0.00189 | 0.00231 | 0.00643 | 0.00527 |
| A3 | 0.00087 | 0.00097 | 0.00103 | 0.00137 | 0.00224 | 0.00275 | 0.00655 | 0.00682 |
| A4 | 0.00097 | 0.00112 | 0.00114 | 0.00154 | 0.00255 | 0.00313 | 0.00668 | 0.00825 |

| Pin | V16 | V24 |
|-----|-----|-----|
|-----|-----|-----|

| | | |
|----|---------|---------|
| A1 | 0.00467 | 0.00693 |
| A2 | 0.00698 | 0.01053 |
| A3 | 0.00905 | 0.01355 |
| A4 | 0.01091 | 0.01647 |

Pin Capacitance (pf)

| Pin | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00093 | 0.00097 | 0.00119 | 0.00153 | 0.00233 | 0.00276 | 0.00116 | 0.00627 |
| A2 | 0.00100 | 0.00103 | 0.00122 | 0.00154 | 0.00255 | 0.00301 | 0.00122 | 0.00634 |
| A3 | 0.00105 | 0.00110 | 0.00125 | 0.00150 | 0.00274 | 0.00323 | 0.00122 | 0.00642 |
| A4 | 0.00104 | 0.00109 | 0.00116 | 0.00148 | 0.00294 | 0.00339 | 0.00127 | 0.00662 |

| Pin | V16 | V24 |
|-----|---------|---------|
| A1 | 0.00838 | 0.01227 |
| A2 | 0.00844 | 0.01263 |
| A3 | 0.00856 | 0.01261 |
| A4 | 0.00876 | 0.01314 |

Max Leakage Power (uW)

| V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00022063 | 0.00018917 | 0.00026183 | 0.00028534 | 0.00052944 | 0.00056168 | 0.00078468 | 0.00132380 |

| V16 | V24 |
|------------|------------|
| 0.00181940 | 0.00283990 |

Delay Table (ns)

| Description | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.04720 | 0.02712 | 0.04024 | 0.03494 | 0.03225 | 0.02968 | 0.12802 | 0.01451 |
| A1→ZN_RISE | 0.02039 | 0.02714 | 0.01770 | 0.01650 | 0.01551 | 0.01490 | 0.06922 | 0.01789 |
| A2→ZN_FALL | 0.05658 | 0.03528 | 0.04741 | 0.04091 | 0.03952 | 0.03680 | 0.13591 | 0.02227 |
| A2→ZN_RISE | 0.02324 | 0.03349 | 0.01998 | 0.01839 | 0.01782 | 0.01723 | 0.07244 | 0.02502 |
| A3→ZN_FALL | 0.06191 | 0.04045 | 0.05192 | 0.04559 | 0.04564 | 0.04266 | 0.14038 | 0.02727 |
| A3→ZN_RISE | 0.02504 | 0.03831 | 0.02136 | 0.01999 | 0.01993 | 0.01927 | 0.07487 | 0.03033 |
| A4→ZN_FALL | 0.06492 | 0.04319 | 0.05318 | 0.04791 | 0.04933 | 0.04617 | 0.14482 | 0.02988 |
| A4→ZN_RISE | 0.02622 | 0.04183 | 0.02179 | 0.02069 | 0.02117 | 0.02047 | 0.07768 | 0.03432 |

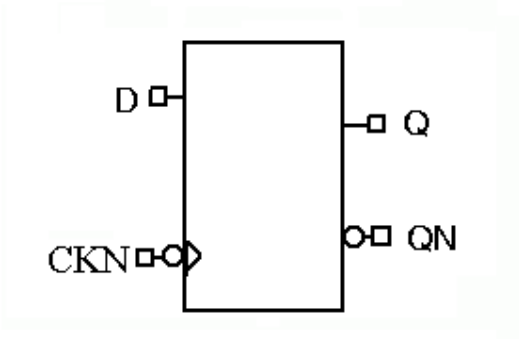
| Description | V16 | V24 |
|-------------|---------|---------|
| A1→ZN_FALL | 0.01438 | 0.01386 |
| A1→ZN_RISE | 0.01725 | 0.01716 |
| A2→ZN_FALL | 0.02219 | 0.02191 |
| A2→ZN_RISE | 0.02428 | 0.02451 |
| A3→ZN_FALL | 0.02724 | 0.02672 |
| A3→ZN_RISE | 0.02952 | 0.02966 |

| | | |
|------------|---------|---------|
| A4→ZN_FALL | 0.02968 | 0.02935 |
| A4→ZN_RISE | 0.03324 | 0.03377 |

NDHS

Cell Description

Negative Edge Trigger D Flip-Flop
Q = falling (CKN) ? D : pre_Q
QN = !Q



Function Table

| CKN<1> | CKN | D | Q |
|--------|-----|---|------|
| 0 | X | X | Q<1> |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| NDHSV1 | 1.80 | 4.60 |
| NDHSV2 | 1.80 | 4.60 |
| NDHSV4 | 1.80 | 5.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|----------|----------|----------|
| CKN | 0.00257 | 0.00300 | 0.00356 |
| D | 0.00124 | 0.00127 | 0.00133 |
| Q | -0.00106 | -0.00112 | -0.00082 |
| QN | -0.00107 | -0.00114 | -0.00094 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CKN | 0.00104 | 0.00104 | 0.00127 |
| D | 0.00099 | 0.00103 | 0.00104 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|----|----|----|
|----|----|----|

| | | |
|------------|------------|------------|
| 0.00048832 | 0.00058120 | 0.00085626 |
|------------|------------|------------|

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CKN→Q_FALL | 0.14218 | 0.13328 | 0.11706 |
| CKN→Q_RISE | 0.10261 | 0.12132 | 0.10320 |
| CKN→QN_FALL | 0.14276 | 0.15376 | 0.14227 |
| CKN→QN_RISE | 0.17324 | 0.16940 | 0.15464 |

Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|----------------|----------|----------|----------|
| D | hold_FALL→CKN | -0.02985 | -0.02488 | -0.02487 |
| D | hold_RISE→CKN | 0.00994 | 0.01492 | 0.00994 |
| D | setup_FALL→CKN | 0.03979 | 0.03979 | 0.03482 |
| D | setup_RISE→CKN | 0.02488 | 0.02487 | 0.03981 |
| CKN | minpwh | 0.07564 | 0.07564 | 0.07068 |
| CKN | minpwl | 0.08949 | 0.10136 | 0.08945 |

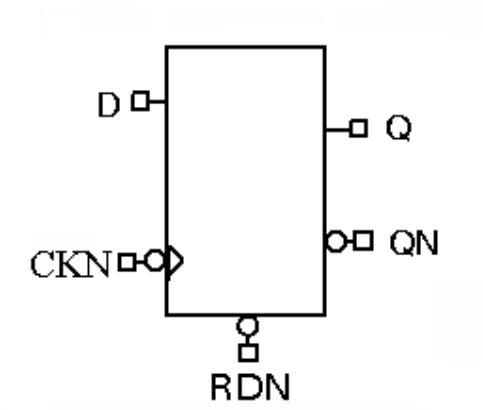
NDRNHS

Cell Description

Negative Edge Trigger D Flip-Flop with Async Clear

$Q = \neg RDN \text{ ? } 0 : \text{falling}(\text{CKN}) \text{ ? } D : \text{pre_}Q$

$QN = \neg Q$



Function Table

| RDN | CKN<1> | CKN | D | Q |
|-----|--------|-----|---|------|
| 0 | X | X | X | 0 |
| 1 | 0 | X | X | Q<1> |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| NDRNHSV1 | 1.80 | 5.20 |
| NDRNHSV2 | 1.80 | 5.20 |
| NDRNHSV4 | 1.80 | 5.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CKN | 0.00320 | 0.00332 | 0.00396 |
| D | 0.00057 | 0.00059 | 0.00062 |
| Q | 0.00080 | 0.00107 | 0.00185 |
| QN | 0.00084 | 0.00114 | 0.00201 |
| RDN | 0.00061 | 0.00064 | 0.00068 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CKN | 0.00110 | 0.00108 | 0.00172 |
| D | 0.00082 | 0.00078 | 0.00079 |
| RDN | 0.00251 | 0.00256 | 0.00295 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00063982 | 0.00071443 | 0.00115380 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CKN→Q_FALL | 0.14146 | 0.15354 | 0.13608 |
| CKN→Q_RISE | 0.17388 | 0.17566 | 0.14664 |
| RDN→Q_FALL | 0.04958 | 0.05249 | 0.06826 |
| CKN→QN_FALL | 0.13006 | 0.12716 | 0.10388 |
| CKN→QN_RISE | 0.10216 | 0.10837 | 0.09191 |
| RDN→QN_RISE | 0.12106 | 0.12921 | 0.15103 |

Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|----------------|----------|----------|----------|
| D | hold_FALL→CKN | -0.02985 | -0.02985 | -0.02489 |
| D | hold_RISE→CKN | 0.00994 | 0.01491 | -0.00000 |
| D | setup_FALL→CKN | 0.05969 | 0.06468 | 0.07464 |
| D | setup_RISE→CKN | 0.03482 | 0.03484 | 0.06469 |
| RDN | setup_RISE→CKN | 0.03980 | 0.03981 | 0.06965 |
| RDN | hold_RISE→CKN | -0.02487 | -0.02488 | -0.05471 |
| CKN | minpwh | 0.10531 | 0.10531 | 0.10033 |
| CKN | minpwl | 0.08554 | 0.08555 | 0.07366 |
| RDN | minpwl | 0.06574 | 0.06577 | 0.06581 |

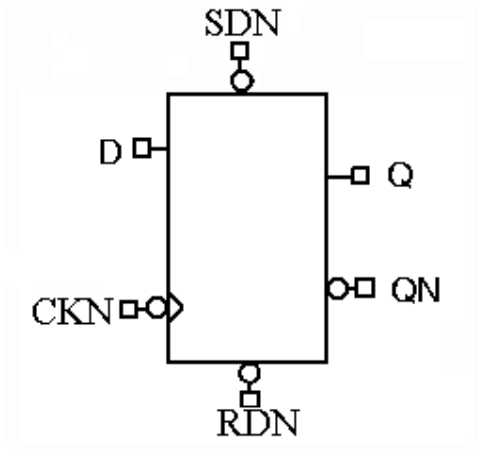
NDRSNHS

Cell Description

Negative Edge Trigger D Flip-Flop with Async Clear and Set

$Q = \neg SDN \text{ ? } 1 : \neg RDN \text{ ? } 0 : \text{falling}(CKN) \text{ ? } D : \text{pre_}Q$

$QN = \neg Q$



Function Table

| RDN | SDN | CKN<1> | CKN | D | Q |
|-----|-----|--------|-----|---|------|
| 0 | 0 | X | X | X | 1 |
| 0 | 1 | X | X | X | 0 |
| 1 | 0 | X | X | X | 1 |
| 1 | 1 | 0 | X | X | Q<1> |
| 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| NDRSNHSV1 | 1.80 | 6.40 |
| NDRSNHSV2 | 1.80 | 6.40 |
| NDRSNHSV4 | 1.80 | 6.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CKN | 0.00353 | 0.00393 | 0.00412 |
| D | 0.00081 | 0.00088 | 0.00087 |
| Q | 0.00192 | 0.00208 | 0.00299 |
| QN | 0.00195 | 0.00213 | 0.00317 |
| RDN | 0.00109 | 0.00113 | 0.00110 |
| SDN | 0.00041 | 0.00044 | 0.00043 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CKN | 0.00104 | 0.00184 | 0.00183 |

| | | | |
|-----|---------|---------|---------|
| D | 0.00088 | 0.00092 | 0.00092 |
| RDN | 0.00103 | 0.00102 | 0.00100 |
| SDN | 0.00168 | 0.00172 | 0.00167 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00070476 | 0.00083058 | 0.00107790 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CKN→Q_FALL | 0.18415 | 0.15401 | 0.17974 |
| CKN→Q_RISE | 0.18808 | 0.16770 | 0.17989 |
| RDN→Q_FALL | 0.17323 | 0.16740 | 0.19171 |
| SDN→Q_FALL | 0.17277 | 0.16311 | 0.18694 |
| SDN→Q_RISE | 0.09378 | 0.10145 | 0.10676 |
| CKN→QN_FALL | 0.15028 | 0.12067 | 0.12760 |
| CKN→QN_RISE | 0.14252 | 0.10477 | 0.12131 |
| RDN→QN_RISE | 0.13266 | 0.11993 | 0.13646 |
| SDN→QN_FALL | 0.06288 | 0.06287 | 0.06672 |
| SDN→QN_RISE | 0.13226 | 0.11571 | 0.13173 |

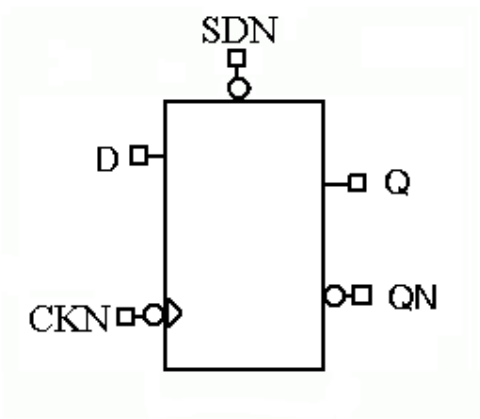
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|------------------------|----------|----------|----------|
| D | hold_FALL→CKN | -0.03484 | -0.03979 | -0.03482 |
| D | hold_RISE→CKN | 0.02985 | 0.00994 | 0.00994 |
| D | setup_FALL→CKN | 0.06964 | 0.08456 | 0.08955 |
| D | setup_RISE→CKN | 0.02986 | 0.05970 | 0.06469 |
| RDN | setup_RISE→CKN | 0.01492 | 0.03980 | 0.04478 |
| RDN | hold_RISE→CKN | 0.01493 | -0.00499 | -0.00994 |
| SDN | setup_RISE→CKN | 0.01491 | 0.02984 | 0.03483 |
| SDN | hold_RISE→CKN | 0.00499 | -0.00498 | -0.00499 |
| SDN | non_seq_hold_RISE→RDN | -0.11441 | -0.09950 | -0.11441 |
| SDN | non_seq_setup_RISE→RDN | 0.13432 | 0.12437 | 0.14428 |
| CKN | minpwh | 0.09050 | 0.09543 | 0.09048 |
| CKN | minpwl | 0.10930 | 0.09346 | 0.10923 |
| RDN | minpwl | 0.12905 | 0.11717 | 0.13297 |
| SDN | minpwl | 0.06976 | 0.07367 | 0.07766 |

NDSNHS

Cell Description

Negative Edge Trigger D Flip-Flop with Async Set
 $Q = \neg SDN \text{ ? } 1 \text{ : falling (CKN) ? } D \text{ : pre_Q}$
 $QN = \neg Q$



Function Table

| SDN | CKN<1> | CKN | D | Q |
|-----|--------|-----|---|------|
| 0 | X | X | X | 1 |
| 1 | 0 | X | X | Q<1> |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| NDSNHSV1 | 1.80 | 5.20 |
| NDSNHSV2 | 1.80 | 5.20 |
| NDSNHSV4 | 1.80 | 5.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CKN | 0.00307 | 0.00316 | 0.00403 |
| D | 0.00093 | 0.00098 | 0.00111 |
| Q | 0.00123 | 0.00157 | 0.00217 |
| QN | 0.00118 | 0.00152 | 0.00211 |
| SDN | 0.00034 | 0.00037 | 0.00043 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CKN | 0.00106 | 0.00106 | 0.00160 |
| D | 0.00100 | 0.00100 | 0.00100 |
| SDN | 0.00148 | 0.00155 | 0.00159 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00064837 | 0.00072690 | 0.00120070 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CKN→Q_FALL | 0.16231 | 0.15171 | 0.13595 |
| CKN→Q_RISE | 0.17015 | 0.16268 | 0.13790 |
| SDN→Q_RISE | 0.08856 | 0.09036 | 0.10512 |
| CKN→QN_FALL | 0.13174 | 0.12713 | 0.09947 |
| CKN→QN_RISE | 0.11836 | 0.11298 | 0.09655 |
| SDN→QN_FALL | 0.05552 | 0.05858 | 0.06690 |

Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|----------------|----------|----------|----------|
| D | hold_FALL→CKN | -0.01990 | -0.01990 | -0.02488 |
| D | hold_RISE→CKN | 0.01991 | 0.01991 | 0.00994 |
| D | setup_FALL→CKN | 0.03980 | 0.04476 | 0.05971 |
| D | setup_RISE→CKN | 0.01991 | 0.01991 | 0.03979 |
| SDN | setup_RISE→CKN | -0.01493 | -0.01492 | 0.00000 |
| SDN | hold_RISE→CKN | 0.02985 | 0.03483 | 0.01990 |
| CKN | minpwh | 0.08057 | 0.08062 | 0.07568 |
| CKN | minpwl | 0.08949 | 0.08552 | 0.06974 |
| SDN | minpwl | 0.06178 | 0.06972 | 0.08158 |

NOR2HS

Cell Description

2-Input NOR
 $ZN = \neg(A1 \vee A2)$



Function Table

| A1 | A2 | ZN |
|----|----|----|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| NOR2HSV0 | 1.80 | 0.80 |
| NOR2HSV0P5 | 1.80 | 0.80 |
| NOR2HSV1 | 1.80 | 0.80 |
| NOR2HSV2 | 1.80 | 0.80 |
| NOR2HSV3 | 1.80 | 1.40 |
| NOR2HSV4 | 1.80 | 1.40 |
| NOR2HSV8 | 1.80 | 2.40 |
| NOR2HSV12 | 1.80 | 3.40 |
| NOR2HSV16 | 1.80 | 4.40 |
| NOR2HSV24 | 1.80 | 6.40 |

Pin Power (uW/MHz)

| Pin | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00040 | 0.00042 | 0.00049 | 0.00066 | 0.00096 | 0.00115 | 0.00225 | 0.00310 |
| A2 | 0.00052 | 0.00055 | 0.00066 | 0.00091 | 0.00139 | 0.00171 | 0.00341 | 0.00486 |

| Pin | V16 | V24 |
|-----|---------|---------|
| A1 | 0.00413 | 0.00618 |
| A2 | 0.00648 | 0.00971 |

Pin Capacitance (pf)

| Pin | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00095 | 0.00097 | 0.00118 | 0.00154 | 0.00234 | 0.00281 | 0.00569 | 0.00806 |
| A2 | 0.00095 | 0.00098 | 0.00116 | 0.00153 | 0.00259 | 0.00308 | 0.00605 | 0.00846 |

| Pin | V16 | V24 |
|-----|---------|---------|
| A1 | 0.01081 | 0.01627 |
| A2 | 0.01126 | 0.01684 |

Max Leakage Power (uW)

| V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00008933 | 0.00009352 | 0.00012997 | 0.00020721 | 0.00037180 | 0.00048991 | 0.00110900 | 0.00143010 |

| V16 | V24 |
|------------|------------|
| 0.00196690 | 0.00305420 |

Delay Table (ns)

| Description | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.01396 | 0.01304 | 0.01238 | 0.01120 | 0.01006 | 0.00949 | 0.00904 | 0.00956 |
| A1→ZN_RISE | 0.02749 | 0.02798 | 0.02454 | 0.02252 | 0.01994 | 0.01872 | 0.01764 | 0.01629 |
| A2→ZN_FALL | 0.01543 | 0.01429 | 0.01371 | 0.01259 | 0.01188 | 0.01124 | 0.01061 | 0.01152 |
| A2→ZN_RISE | 0.03089 | 0.03144 | 0.02788 | 0.02642 | 0.02447 | 0.02346 | 0.02245 | 0.02113 |

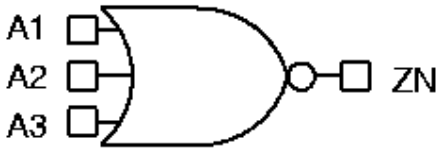
| Description | V16 | V24 |
|-------------|---------|---------|
| A1→ZN_FALL | 0.00951 | 0.00946 |
| A1→ZN_RISE | 0.01618 | 0.01601 |
| A2→ZN_FALL | 0.01141 | 0.01132 |
| A2→ZN_RISE | 0.02098 | 0.02081 |

NOR3HS

Cell Description

3-Input NOR

$$Z_N = \neg(A_1 \vee A_2 \vee A_3)$$



Function Table

| A1 | A2 | A3 | ZN |
|----|----|----|----|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | X | 0 |
| 1 | X | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| NOR3HSV0 | 1.80 | 1.00 |
| NOR3HSV0P5 | 1.80 | 1.00 |
| NOR3HSV1 | 1.80 | 1.00 |
| NOR3HSV2 | 1.80 | 1.00 |
| NOR3HSV3 | 1.80 | 1.80 |
| NOR3HSV4 | 1.80 | 1.80 |
| NOR3HSV8 | 1.80 | 2.80 |
| NOR3HSV12 | 1.80 | 5.00 |
| NOR3HSV16 | 1.80 | 6.60 |
| NOR3HSV24 | 1.80 | 9.60 |

Pin Power (uW/MHz)

| Pin | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00051 | 0.00048 | 0.00061 | 0.00082 | 0.00118 | 0.00143 | 0.00603 | 0.00335 |
| A2 | 0.00063 | 0.00062 | 0.00080 | 0.00109 | 0.00166 | 0.00205 | 0.00617 | 0.00541 |
| A3 | 0.00075 | 0.00075 | 0.00097 | 0.00134 | 0.00206 | 0.00256 | 0.00632 | 0.00714 |

| Pin | V16 | V24 |
|-----|---------|---------|
| A1 | 0.00442 | 0.00661 |
| A2 | 0.00714 | 0.01065 |

| | | |
|----|---------|---------|
| A3 | 0.00945 | 0.01404 |
|----|---------|---------|

Pin Capacitance (pf)

| Pin | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00102 | 0.00095 | 0.00117 | 0.00152 | 0.00224 | 0.00273 | 0.00130 | 0.00703 |
| A2 | 0.00102 | 0.00093 | 0.00124 | 0.00155 | 0.00261 | 0.00311 | 0.00124 | 0.00702 |
| A3 | 0.00093 | 0.00091 | 0.00114 | 0.00149 | 0.00274 | 0.00326 | 0.00117 | 0.00724 |

| Pin | V16 | V24 |
|-----|---------|---------|
| A1 | 0.00933 | 0.01369 |
| A2 | 0.00934 | 0.01370 |
| A3 | 0.00964 | 0.01403 |

Max Leakage Power (uW)

| V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00014627 | 0.00012695 | 0.00021471 | 0.00033512 | 0.00059635 | 0.00078843 | 0.00086587 | 0.00143660 |

| V16 | V24 |
|------------|------------|
| 0.00218950 | 0.00301070 |

Delay Table (ns)

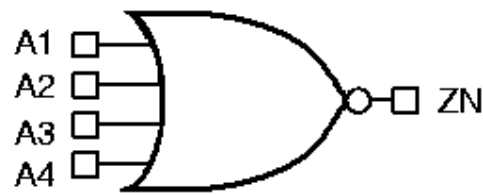
| Description | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.01567 | 0.01592 | 0.01355 | 0.01237 | 0.01093 | 0.01037 | 0.06108 | 0.01184 |
| A1→ZN_RISE | 0.04502 | 0.04162 | 0.03873 | 0.03619 | 0.03100 | 0.02940 | 0.12874 | 0.02218 |
| A2→ZN_FALL | 0.01674 | 0.01740 | 0.01496 | 0.01366 | 0.01288 | 0.01218 | 0.06259 | 0.01467 |
| A2→ZN_RISE | 0.05191 | 0.04942 | 0.04760 | 0.04543 | 0.04199 | 0.04059 | 0.13559 | 0.03428 |
| A3→ZN_FALL | 0.01755 | 0.01845 | 0.01553 | 0.01424 | 0.01374 | 0.01296 | 0.06510 | 0.01568 |
| A3→ZN_RISE | 0.05476 | 0.05267 | 0.05039 | 0.04890 | 0.04639 | 0.04499 | 0.13821 | 0.03872 |

| Description | V16 | V24 |
|-------------|---------|---------|
| A1→ZN_FALL | 0.01173 | 0.01241 |
| A1→ZN_RISE | 0.02202 | 0.02241 |
| A2→ZN_FALL | 0.01443 | 0.01496 |
| A2→ZN_RISE | 0.03407 | 0.03445 |
| A3→ZN_FALL | 0.01514 | 0.01613 |
| A3→ZN_RISE | 0.03849 | 0.03948 |

NOR4HS

Cell Description

4-Input NOR
 $ZN = \neg(A1 \vee A2 \vee A3 \vee A4)$



Function Table

| A1 | A2 | A3 | A4 | ZN |
|----|----|----|----|----|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | X | 0 |
| 0 | 1 | X | X | 0 |
| 1 | X | X | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| NOR4HSV0 | 1.80 | 1.40 |
| NOR4HSV0P5 | 1.80 | 1.40 |
| NOR4HSV1 | 1.80 | 1.40 |
| NOR4HSV2 | 1.80 | 1.40 |
| NOR4HSV3 | 1.80 | 2.40 |
| NOR4HSV4 | 1.80 | 2.40 |
| NOR4HSV8 | 1.80 | 3.00 |
| NOR4HSV12 | 1.80 | 6.80 |
| NOR4HSV16 | 1.80 | 8.80 |
| NOR4HSV24 | 1.80 | 12.80 |

Pin Power (uW/MHz)

| Pin | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00061 | 0.00058 | 0.00072 | 0.00095 | 0.00143 | 0.00172 | 0.00624 | 0.00385 |
| A2 | 0.00073 | 0.00072 | 0.00091 | 0.00123 | 0.00188 | 0.00228 | 0.00641 | 0.00588 |
| A3 | 0.00087 | 0.00085 | 0.00109 | 0.00149 | 0.00233 | 0.00287 | 0.00657 | 0.00768 |
| A4 | 0.00097 | 0.00098 | 0.00125 | 0.00172 | 0.00274 | 0.00339 | 0.00675 | 0.00936 |

| Pin | V16 | V24 |
|-----|-----|-----|
|-----|-----|-----|

| | | |
|----|---------|---------|
| A1 | 0.00506 | 0.00747 |
| A2 | 0.00772 | 0.01142 |
| A3 | 0.01010 | 0.01498 |
| A4 | 0.01231 | 0.01823 |

Pin Capacitance (pf)

| Pin | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00099 | 0.00100 | 0.00120 | 0.00152 | 0.00225 | 0.00276 | 0.00122 | 0.00685 |
| A2 | 0.00097 | 0.00094 | 0.00122 | 0.00159 | 0.00255 | 0.00301 | 0.00121 | 0.00684 |
| A3 | 0.00101 | 0.00094 | 0.00123 | 0.00155 | 0.00276 | 0.00329 | 0.00126 | 0.00686 |
| A4 | 0.00095 | 0.00094 | 0.00117 | 0.00150 | 0.00296 | 0.00345 | 0.00122 | 0.00704 |

| Pin | V16 | V24 |
|-----|---------|---------|
| A1 | 0.00901 | 0.01334 |
| A2 | 0.00900 | 0.01329 |
| A3 | 0.00903 | 0.01341 |
| A4 | 0.00925 | 0.01376 |

Max Leakage Power (uW)

| V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00021646 | 0.00020528 | 0.00032896 | 0.00048991 | 0.00083681 | 0.00110920 | 0.00103950 | 0.00192180 |

| V16 | V24 |
|------------|------------|
| 0.00259410 | 0.00395080 |

Delay Table (ns)

| Description | V0 | V0P5 | V1 | V2 | V3 | V4 | V8 | V12 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.01700 | 0.01757 | 0.01453 | 0.01317 | 0.01193 | 0.01125 | 0.06174 | 0.01378 |
| A1→ZN_RISE | 0.06438 | 0.05927 | 0.05427 | 0.05009 | 0.04397 | 0.04168 | 0.15994 | 0.02860 |
| A2→ZN_FALL | 0.01795 | 0.01908 | 0.01591 | 0.01452 | 0.01371 | 0.01289 | 0.06343 | 0.01729 |
| A2→ZN_RISE | 0.07558 | 0.07117 | 0.06873 | 0.06582 | 0.06018 | 0.05787 | 0.17388 | 0.04787 |
| A3→ZN_FALL | 0.01906 | 0.02003 | 0.01650 | 0.01496 | 0.01464 | 0.01371 | 0.06506 | 0.01858 |
| A3→ZN_RISE | 0.08501 | 0.07914 | 0.07699 | 0.07451 | 0.07066 | 0.06894 | 0.18133 | 0.05838 |
| A4→ZN_FALL | 0.01891 | 0.02060 | 0.01651 | 0.01499 | 0.01519 | 0.01409 | 0.06634 | 0.01876 |
| A4→ZN_RISE | 0.08570 | 0.08250 | 0.07909 | 0.07761 | 0.07612 | 0.07404 | 0.18620 | 0.06265 |

| Description | V16 | V24 |
|-------------|---------|---------|
| A1→ZN_FALL | 0.01359 | 0.01360 |
| A1→ZN_RISE | 0.02807 | 0.02766 |
| A2→ZN_FALL | 0.01705 | 0.01708 |
| A2→ZN_RISE | 0.04692 | 0.04659 |
| A3→ZN_FALL | 0.01834 | 0.01831 |
| A3→ZN_RISE | 0.05757 | 0.05725 |

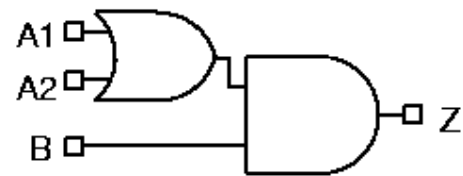
| | | |
|------------|---------|---------|
| A4→ZN_FALL | 0.01844 | 0.01843 |
| A4→ZN_RISE | 0.06175 | 0.06163 |

OA21HS

Cell Description

2-1 OA with Simple Gates

$Z=((A1\|A2)\&B)$



Function Table

| A1 | A2 | B | Z |
|----|----|---|---|
| 0 | 0 | X | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | X | 0 | 0 |
| 1 | X | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| OA21HSV0 | 1.80 | 1.60 |
| OA21HSV1 | 1.80 | 1.60 |
| OA21HSV2 | 1.80 | 1.60 |
| OA21HSV4 | 1.80 | 1.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00135 | 0.00149 | 0.00174 | 0.00281 |
| A2 | 0.00147 | 0.00161 | 0.00186 | 0.00301 |
| B | 0.00121 | 0.00135 | 0.00159 | 0.00257 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00108 | 0.00107 | 0.00107 | 0.00144 |
| A2 | 0.00104 | 0.00103 | 0.00102 | 0.00136 |
| B | 0.00113 | 0.00113 | 0.00110 | 0.00145 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00015236 | 0.00016809 | 0.00019904 | 0.00034465 |

Delay Table (ns)

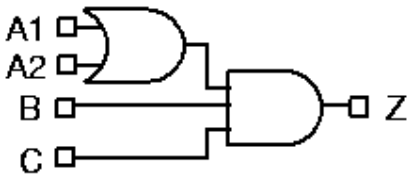
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.06770 | 0.06867 | 0.07209 | 0.07003 |
| A1→Z_RISE | 0.05321 | 0.05359 | 0.05648 | 0.05149 |
| A2→Z_FALL | 0.07124 | 0.07220 | 0.07551 | 0.07380 |
| A2→Z_RISE | 0.05774 | 0.05815 | 0.06107 | 0.05628 |
| B→Z_FALL | 0.03852 | 0.03827 | 0.03933 | 0.03694 |
| B→Z_RISE | 0.04709 | 0.04734 | 0.04970 | 0.04544 |

OA211HS

Cell Description

2-1-1 OA

$Z=((A1\|A2)\&B\&C)$



Function Table

| A1 | A2 | B | C | Z |
|----|----|---|---|---|
| 0 | 0 | X | X | 0 |
| 0 | 1 | 0 | X | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | X | 0 | X | 0 |
| 1 | X | 1 | 0 | 0 |
| 1 | X | 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| OA211HSV0 | 1.80 | 1.60 |
| OA211HSV1 | 1.80 | 1.60 |
| OA211HSV2 | 1.80 | 1.60 |
| OA211HSV4 | 1.80 | 1.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00130 | 0.00149 | 0.00161 | 0.00284 |
| A2 | 0.00142 | 0.00161 | 0.00172 | 0.00304 |
| B | 0.00153 | 0.00172 | 0.00183 | 0.00318 |
| C | 0.00163 | 0.00182 | 0.00193 | 0.00333 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00105 | 0.00105 | 0.00105 | 0.00138 |
| A2 | 0.00109 | 0.00108 | 0.00107 | 0.00140 |

| | | | | |
|---|---------|---------|---------|---------|
| B | 0.00108 | 0.00110 | 0.00107 | 0.00142 |
| C | 0.00107 | 0.00109 | 0.00108 | 0.00147 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00021719 | 0.00023330 | 0.00026105 | 0.00045113 |

Delay Table (ns)

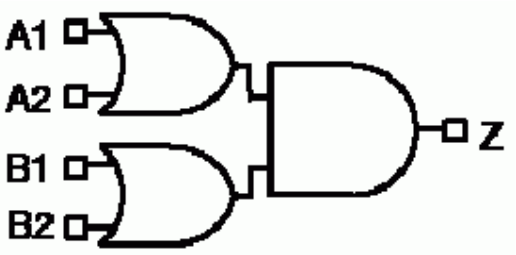
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.06483 | 0.06745 | 0.06630 | 0.06799 |
| A1→Z_RISE | 0.06756 | 0.07039 | 0.07470 | 0.06777 |
| A2→Z_FALL | 0.06840 | 0.07088 | 0.06947 | 0.07168 |
| A2→Z_RISE | 0.07253 | 0.07519 | 0.07927 | 0.07223 |
| B→Z_FALL | 0.04673 | 0.04768 | 0.04600 | 0.04558 |
| B→Z_RISE | 0.07630 | 0.07902 | 0.08286 | 0.07512 |
| C→Z_FALL | 0.04886 | 0.04986 | 0.04816 | 0.04777 |
| C→Z_RISE | 0.07941 | 0.08224 | 0.08608 | 0.07797 |

OA22HS

Cell Description

2-2 OA with Simple Gates

$$Z=((A1\text{I}A2)\&(B1\text{I}B2))$$



Function Table

| A1 | A2 | B1 | B2 | Z |
|----|----|----|----|---|
| 0 | 0 | X | X | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | X | 1 |
| 1 | X | 0 | 0 | 0 |
| 1 | X | 0 | 1 | 1 |
| 1 | X | 1 | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| OA22HSV0 | 1.80 | 1.80 |
| OA22HSV1 | 1.80 | 1.80 |
| OA22HSV2 | 1.80 | 1.80 |
| OA22HSV4 | 1.80 | 2.20 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00125 | 0.00143 | 0.00165 | 0.00281 |
| A2 | 0.00137 | 0.00154 | 0.00176 | 0.00301 |
| B1 | 0.00146 | 0.00164 | 0.00187 | 0.00313 |
| B2 | 0.00165 | 0.00183 | 0.00207 | 0.00344 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00108 | 0.00106 | 0.00101 | 0.00142 |
| A2 | 0.00103 | 0.00100 | 0.00098 | 0.00136 |

| | | | | |
|----|---------|---------|---------|---------|
| B1 | 0.00106 | 0.00104 | 0.00103 | 0.00146 |
| B2 | 0.00097 | 0.00096 | 0.00096 | 0.00136 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00017172 | 0.00018295 | 0.00020948 | 0.00040322 |

Delay Table (ns)

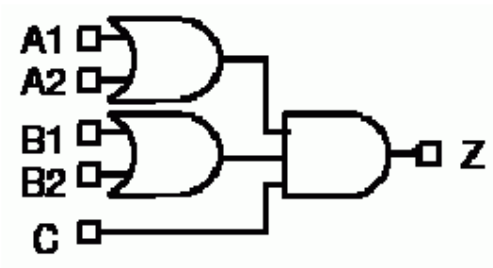
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.06042 | 0.06215 | 0.06502 | 0.06490 |
| A1→Z_RISE | 0.04822 | 0.04919 | 0.05175 | 0.04765 |
| A2→Z_FALL | 0.06306 | 0.06492 | 0.06745 | 0.06827 |
| A2→Z_RISE | 0.05170 | 0.05276 | 0.05514 | 0.05127 |
| B1→Z_FALL | 0.07270 | 0.07460 | 0.07788 | 0.07696 |
| B1→Z_RISE | 0.05511 | 0.05592 | 0.05884 | 0.05340 |
| B2→Z_FALL | 0.07783 | 0.07962 | 0.08331 | 0.08283 |
| B2→Z_RISE | 0.06027 | 0.06155 | 0.06491 | 0.05909 |

OA221HS

Cell Description

2-2-1 OA

$$Z=((A1\text{I}A2)\&(B1\text{I}B2)\&C)$$



Function Table

| A1 | A2 | B1 | B2 | C | Z |
|----|----|----|----|---|---|
| 0 | 0 | X | X | X | 0 |
| 0 | 1 | 0 | 0 | X | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | X | 0 | 0 |
| 0 | 1 | 1 | X | 1 | 1 |
| 1 | X | 0 | 0 | X | 0 |
| 1 | X | 0 | 1 | 0 | 0 |
| 1 | X | 0 | 1 | 1 | 1 |
| 1 | X | 1 | X | 0 | 0 |
| 1 | X | 1 | X | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| OA221HSV0 | 1.80 | 2.00 |
| OA221HSV1 | 1.80 | 2.00 |
| OA221HSV2 | 1.80 | 2.00 |
| OA221HSV4 | 1.80 | 2.20 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00148 | 0.00162 | 0.00189 | 0.00297 |
| A2 | 0.00159 | 0.00173 | 0.00200 | 0.00319 |
| B1 | 0.00170 | 0.00184 | 0.00211 | 0.00334 |
| B2 | 0.00184 | 0.00199 | 0.00225 | 0.00358 |
| C | 0.00195 | 0.00209 | 0.00234 | 0.00365 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00107 | 0.00106 | 0.00108 | 0.00135 |
| A2 | 0.00099 | 0.00099 | 0.00101 | 0.00136 |
| B1 | 0.00098 | 0.00098 | 0.00098 | 0.00138 |
| B2 | 0.00121 | 0.00121 | 0.00115 | 0.00164 |
| C | 0.00112 | 0.00111 | 0.00109 | 0.00146 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00021873 | 0.00023373 | 0.00026895 | 0.00045416 |

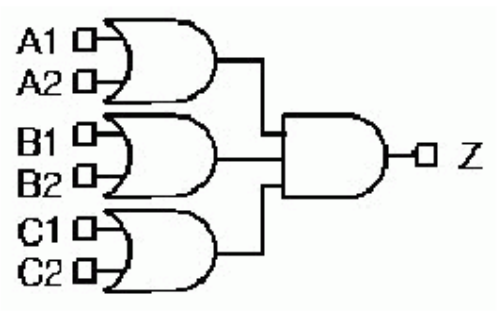
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.07199 | 0.07241 | 0.07532 | 0.06946 |
| A1→Z_RISE | 0.07198 | 0.07252 | 0.07765 | 0.06682 |
| A2→Z_FALL | 0.07486 | 0.07531 | 0.07785 | 0.07379 |
| A2→Z_RISE | 0.07688 | 0.07751 | 0.08249 | 0.07253 |
| B1→Z_FALL | 0.08360 | 0.08396 | 0.08687 | 0.08195 |
| B1→Z_RISE | 0.08266 | 0.08324 | 0.08885 | 0.07726 |
| B2→Z_FALL | 0.08889 | 0.08932 | 0.09154 | 0.08692 |
| B2→Z_RISE | 0.09185 | 0.09253 | 0.09739 | 0.08585 |
| C→Z_FALL | 0.05669 | 0.05612 | 0.05673 | 0.05159 |
| C→Z_RISE | 0.08949 | 0.08989 | 0.09454 | 0.08174 |

OA222HS

Cell Description

2-2-2 OA
 $Z=((A1\&A2)\&(B1\&B2)\&(C1\&C2))$



Function Table

| A1 | A2 | B1 | B2 | C1 | C2 | Z |
|----|----|----|----|----|----|---|
| 0 | 0 | X | X | X | X | 0 |
| 0 | 1 | 0 | 0 | X | X | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | X | 1 |
| 0 | 1 | 1 | X | 0 | 0 | 0 |
| 0 | 1 | 1 | X | 0 | 1 | 1 |
| 0 | 1 | 1 | X | 1 | X | 1 |
| 1 | X | 0 | 0 | X | X | 0 |
| 1 | X | 0 | 1 | 0 | 0 | 0 |
| 1 | X | 0 | 1 | 0 | 1 | 1 |
| 1 | X | 0 | 1 | 1 | X | 1 |
| 1 | X | 1 | X | 0 | 0 | 0 |
| 1 | X | 1 | X | 0 | 1 | 1 |
| 1 | X | 1 | X | 1 | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| OA222HSV0 | 1.80 | 2.40 |
| OA222HSV1 | 1.80 | 2.40 |
| OA222HSV2 | 1.80 | 2.40 |
| OA222HSV4 | 1.80 | 2.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00151 | 0.00168 | 0.00195 | 0.00312 |
| A2 | 0.00163 | 0.00181 | 0.00207 | 0.00331 |

| | | | | |
|----|---------|---------|---------|---------|
| B1 | 0.00201 | 0.00218 | 0.00245 | 0.00375 |
| B2 | 0.00211 | 0.00229 | 0.00256 | 0.00408 |
| C1 | 0.00180 | 0.00198 | 0.00224 | 0.00347 |
| C2 | 0.00189 | 0.00207 | 0.00234 | 0.00367 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00109 | 0.00108 | 0.00108 | 0.00143 |
| A2 | 0.00113 | 0.00109 | 0.00109 | 0.00139 |
| B1 | 0.00108 | 0.00107 | 0.00107 | 0.00138 |
| B2 | 0.00108 | 0.00108 | 0.00108 | 0.00134 |
| C1 | 0.00125 | 0.00125 | 0.00125 | 0.00138 |
| C2 | 0.00106 | 0.00106 | 0.00106 | 0.00134 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00020732 | 0.00022402 | 0.00025515 | 0.00042222 |

Delay Table (ns)

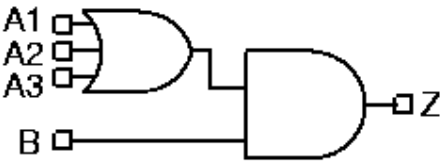
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.07464 | 0.07606 | 0.07903 | 0.07207 |
| A1→Z_RISE | 0.07034 | 0.07256 | 0.07604 | 0.07053 |
| A2→Z_FALL | 0.07821 | 0.07966 | 0.08259 | 0.07529 |
| A2→Z_RISE | 0.07603 | 0.07830 | 0.08177 | 0.07548 |
| B1→Z_FALL | 0.09955 | 0.10074 | 0.10357 | 0.09259 |
| B1→Z_RISE | 0.09099 | 0.09322 | 0.09663 | 0.08559 |
| B2→Z_FALL | 0.10188 | 0.10308 | 0.10591 | 0.09910 |
| B2→Z_RISE | 0.09456 | 0.09677 | 0.10016 | 0.09380 |
| C1→Z_FALL | 0.09011 | 0.09149 | 0.09424 | 0.08371 |
| C1→Z_RISE | 0.08520 | 0.08764 | 0.09107 | 0.08031 |
| C2→Z_FALL | 0.09185 | 0.09319 | 0.09592 | 0.08690 |
| C2→Z_RISE | 0.08765 | 0.08992 | 0.09333 | 0.08550 |

OA31HS

Cell Description

3-1 OA

$Z=((A1\&A2\&A3)\&B)$



Function Table

| A1 | A2 | A3 | B | Z |
|----|----|----|---|---|
| 0 | 0 | 0 | X | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | X | 0 | 0 |
| 0 | 1 | X | 1 | 1 |
| 1 | X | X | 0 | 0 |
| 1 | X | X | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| OA31HSV0 | 1.80 | 1.60 |
| OA31HSV1 | 1.80 | 1.60 |
| OA31HSV2 | 1.80 | 1.60 |
| OA31HSV4 | 1.80 | 1.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00133 | 0.00149 | 0.00171 | 0.00281 |
| A2 | 0.00145 | 0.00161 | 0.00183 | 0.00303 |
| A3 | 0.00157 | 0.00173 | 0.00195 | 0.00322 |
| B | 0.00164 | 0.00179 | 0.00200 | 0.00322 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00108 | 0.00110 | 0.00106 | 0.00144 |
| A2 | 0.00104 | 0.00105 | 0.00100 | 0.00139 |

| | | | | |
|----|---------|---------|---------|---------|
| A3 | 0.00101 | 0.00100 | 0.00096 | 0.00134 |
| B | 0.00114 | 0.00112 | 0.00112 | 0.00150 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00022361 | 0.00023617 | 0.00024652 | 0.00047672 |

Delay Table (ns)

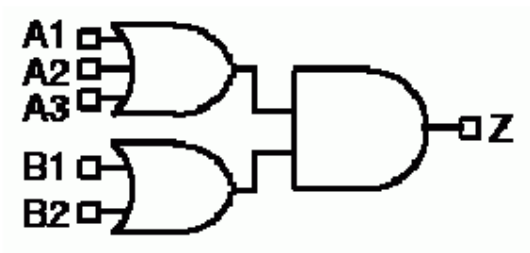
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.08788 | 0.09035 | 0.09380 | 0.09166 |
| A1→Z_RISE | 0.05269 | 0.05333 | 0.05495 | 0.04936 |
| A2→Z_FALL | 0.09522 | 0.09748 | 0.10159 | 0.10046 |
| A2→Z_RISE | 0.05700 | 0.05760 | 0.05961 | 0.05414 |
| A3→Z_FALL | 0.09878 | 0.10035 | 0.10435 | 0.10355 |
| A3→Z_RISE | 0.06118 | 0.06148 | 0.06351 | 0.05801 |
| B→Z_FALL | 0.04939 | 0.04915 | 0.04978 | 0.04636 |
| B→Z_RISE | 0.05816 | 0.05805 | 0.05961 | 0.05345 |

OA32HS

Cell Description

3-2 OA

$$Z=((A1\text{!}A2\text{!}A3)\&(B1\text{!}B2))$$



Function Table

| A1 | A2 | A3 | B1 | B2 | Z |
|----|----|----|----|----|---|
| 0 | 0 | 0 | X | X | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | X | 1 |
| 0 | 1 | X | 0 | 0 | 0 |
| 0 | 1 | X | 0 | 1 | 1 |
| 0 | 1 | X | 1 | X | 1 |
| 1 | X | X | 0 | 0 | 0 |
| 1 | X | X | 0 | 1 | 1 |
| 1 | X | X | 1 | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| OA32HSV0 | 1.80 | 2.00 |
| OA32HSV1 | 1.80 | 2.00 |
| OA32HSV2 | 1.80 | 2.00 |
| OA32HSV4 | 1.80 | 2.40 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00145 | 0.00160 | 0.00181 | 0.00297 |
| A2 | 0.00159 | 0.00173 | 0.00194 | 0.00318 |
| A3 | 0.00171 | 0.00185 | 0.00206 | 0.00337 |
| B1 | 0.00176 | 0.00190 | 0.00211 | 0.00339 |
| B2 | 0.00190 | 0.00204 | 0.00224 | 0.00365 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00103 | 0.00103 | 0.00103 | 0.00146 |
| A2 | 0.00108 | 0.00107 | 0.00107 | 0.00139 |
| A3 | 0.00101 | 0.00101 | 0.00101 | 0.00134 |
| B1 | 0.00111 | 0.00111 | 0.00110 | 0.00138 |
| B2 | 0.00110 | 0.00109 | 0.00108 | 0.00150 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00022569 | 0.00023805 | 0.00024786 | 0.00048015 |

Delay Table (ns)

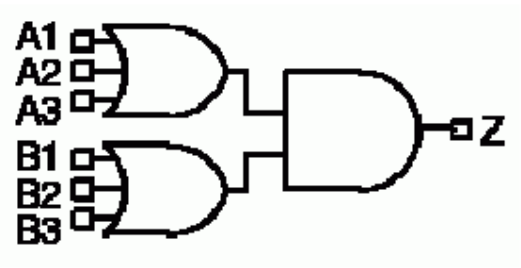
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.09541 | 0.09703 | 0.09941 | 0.09614 |
| A1→Z_RISE | 0.05373 | 0.05364 | 0.05504 | 0.04978 |
| A2→Z_FALL | 0.10414 | 0.10579 | 0.10818 | 0.10499 |
| A2→Z_RISE | 0.05834 | 0.05828 | 0.05970 | 0.05401 |
| A3→Z_FALL | 0.10719 | 0.10874 | 0.11108 | 0.10800 |
| A3→Z_RISE | 0.06209 | 0.06207 | 0.06356 | 0.05759 |
| B1→Z_FALL | 0.08760 | 0.08805 | 0.08899 | 0.08413 |
| B1→Z_RISE | 0.06157 | 0.06129 | 0.06252 | 0.05569 |
| B2→Z_FALL | 0.09247 | 0.09281 | 0.09348 | 0.09008 |
| B2→Z_RISE | 0.06701 | 0.06671 | 0.06781 | 0.06148 |

OA33HS

Cell Description

3-3 OA

$$Z=((A1|A2|A3)\&(B1|B2|B3))$$



Function Table

| A1 | A2 | A3 | B1 | B2 | B3 | Z |
|----|----|----|----|----|----|---|
| 0 | 0 | 0 | X | X | X | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | X | 1 |
| 0 | 0 | 1 | 1 | X | X | 1 |
| 0 | 1 | X | 0 | 0 | 0 | 0 |
| 0 | 1 | X | 0 | 0 | 1 | 1 |
| 0 | 1 | X | 0 | 1 | X | 1 |
| 0 | 1 | X | 1 | X | X | 1 |
| 1 | X | X | 0 | 0 | 0 | 0 |
| 1 | X | X | 0 | 0 | 1 | 1 |
| 1 | X | X | 0 | 1 | X | 1 |
| 1 | X | X | 1 | X | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| OA33HSV0 | 1.80 | 2.00 |
| OA33HSV1 | 1.80 | 2.00 |
| OA33HSV2 | 1.80 | 2.00 |
| OA33HSV4 | 1.80 | 2.40 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00143 | 0.00161 | 0.00187 | 0.00308 |
| A2 | 0.00158 | 0.00175 | 0.00201 | 0.00331 |
| A3 | 0.00171 | 0.00188 | 0.00213 | 0.00352 |
| B1 | 0.00180 | 0.00197 | 0.00221 | 0.00362 |

| | | | | |
|----|---------|---------|---------|---------|
| B2 | 0.00191 | 0.00209 | 0.00235 | 0.00385 |
| B3 | 0.00207 | 0.00225 | 0.00250 | 0.00406 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00106 | 0.00109 | 0.00109 | 0.00142 |
| A2 | 0.00111 | 0.00109 | 0.00107 | 0.00138 |
| A3 | 0.00106 | 0.00105 | 0.00105 | 0.00140 |
| B1 | 0.00115 | 0.00112 | 0.00108 | 0.00136 |
| B2 | 0.00104 | 0.00102 | 0.00106 | 0.00139 |
| B3 | 0.00107 | 0.00113 | 0.00108 | 0.00141 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00023912 | 0.00025053 | 0.00026202 | 0.00049201 |

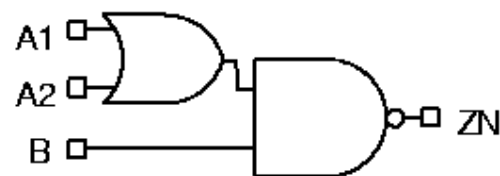
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.09150 | 0.09501 | 0.10018 | 0.09706 |
| A1→Z_RISE | 0.05028 | 0.05116 | 0.05324 | 0.04855 |
| A2→Z_FALL | 0.10222 | 0.10487 | 0.10962 | 0.10664 |
| A2→Z_RISE | 0.05525 | 0.05583 | 0.05782 | 0.05274 |
| A3→Z_FALL | 0.10573 | 0.10874 | 0.11341 | 0.11077 |
| A3→Z_RISE | 0.05897 | 0.05976 | 0.06190 | 0.05652 |
| B1→Z_FALL | 0.12144 | 0.12386 | 0.12765 | 0.12277 |
| B1→Z_RISE | 0.06138 | 0.06189 | 0.06340 | 0.05730 |
| B2→Z_FALL | 0.12844 | 0.13103 | 0.13678 | 0.13262 |
| B2→Z_RISE | 0.06481 | 0.06533 | 0.06776 | 0.06148 |
| B3→Z_FALL | 0.13366 | 0.13830 | 0.14231 | 0.13728 |
| B3→Z_RISE | 0.06861 | 0.06995 | 0.07171 | 0.06453 |

OAI21HS

Cell Description

2-1 OAI
 $ZN = \neg((A1 \mid A2) \& B)$



Function Table

| A1 | A2 | B | ZN |
|----|----|---|----|
| 0 | 0 | X | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | X | 0 | 1 |
| 1 | X | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| OAI21HSV0 | 1.80 | 1.00 |
| OAI21HSV1 | 1.80 | 1.00 |
| OAI21HSV2 | 1.80 | 1.00 |
| OAI21HSV4 | 1.80 | 1.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00062 | 0.00077 | 0.00103 | 0.00205 |
| A2 | 0.00074 | 0.00094 | 0.00127 | 0.00254 |
| B | 0.00046 | 0.00059 | 0.00079 | 0.00148 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00098 | 0.00119 | 0.00152 | 0.00306 |
| A2 | 0.00095 | 0.00117 | 0.00150 | 0.00289 |
| B | 0.00097 | 0.00122 | 0.00157 | 0.00282 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00011229 | 0.00013420 | 0.00015694 | 0.00036674 |

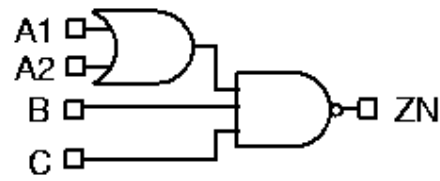
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.02783 | 0.02437 | 0.02173 | 0.02017 |
| A1→ZN_RISE | 0.03700 | 0.03298 | 0.03095 | 0.02889 |
| A2→ZN_FALL | 0.03086 | 0.02759 | 0.02493 | 0.02281 |
| A2→ZN_RISE | 0.03961 | 0.03599 | 0.03440 | 0.03231 |
| B→ZN_FALL | 0.02169 | 0.01928 | 0.01730 | 0.01511 |
| B→ZN_RISE | 0.01624 | 0.01457 | 0.01365 | 0.01214 |

OAI211HS

Cell Description

2-1-1 OAI
 $ZN = \neg((A1 \vee A2) \wedge B \wedge C)$



Function Table

| A1 | A2 | B | C | ZN |
|----|----|---|---|----|
| 0 | 0 | X | X | 1 |
| 0 | 1 | 0 | X | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | X | 0 | X | 1 |
| 1 | X | 1 | 0 | 1 |
| 1 | X | 1 | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| OAI211HSV0 | 1.80 | 1.20 |
| OAI211HSV1 | 1.80 | 1.20 |
| OAI211HSV2 | 1.80 | 1.40 |
| OAI211HSV4 | 1.80 | 2.40 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00083 | 0.00105 | 0.00141 | 0.00390 |
| A2 | 0.00095 | 0.00122 | 0.00166 | 0.00401 |
| B | 0.00057 | 0.00073 | 0.00098 | 0.00367 |
| C | 0.00065 | 0.00085 | 0.00116 | 0.00375 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00100 | 0.00123 | 0.00154 | 0.00103 |
| A2 | 0.00097 | 0.00118 | 0.00152 | 0.00097 |

| | | | | |
|---|---------|---------|---------|---------|
| B | 0.00103 | 0.00124 | 0.00151 | 0.00108 |
| C | 0.00099 | 0.00124 | 0.00153 | 0.00107 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00016581 | 0.00019923 | 0.00021795 | 0.00041537 |

Delay Table (ns)

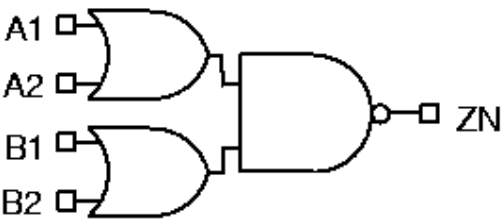
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.04364 | 0.03870 | 0.03536 | 0.11238 |
| A1→ZN_RISE | 0.04387 | 0.03988 | 0.03834 | 0.11255 |
| A2→ZN_FALL | 0.04904 | 0.04424 | 0.04057 | 0.11959 |
| A2→ZN_RISE | 0.04722 | 0.04340 | 0.04202 | 0.11557 |
| B→ZN_FALL | 0.03439 | 0.03006 | 0.02673 | 0.10185 |
| B→ZN_RISE | 0.01842 | 0.01646 | 0.01533 | 0.06821 |
| C→ZN_FALL | 0.03741 | 0.03378 | 0.03064 | 0.10566 |
| C→ZN_RISE | 0.01995 | 0.01835 | 0.01733 | 0.07067 |

OAI22HS

Cell Description

2-2 OAI

$$Z_N = \neg((A1 \vee A2) \wedge (B1 \vee B2))$$



Function Table

| A1 | A2 | B1 | B2 | ZN |
|----|----|----|----|----|
| 0 | 0 | X | X | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | X | 0 |
| 1 | X | 0 | 0 | 1 |
| 1 | X | 0 | 1 | 0 |
| 1 | X | 1 | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| OAI22HSV0 | 1.80 | 1.40 |
| OAI22HSV1 | 1.80 | 1.40 |
| OAI22HSV2 | 1.80 | 1.40 |
| OAI22HSV4 | 1.80 | 2.40 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00053 | 0.00067 | 0.00089 | 0.00172 |
| A2 | 0.00068 | 0.00087 | 0.00118 | 0.00227 |
| B1 | 0.00081 | 0.00101 | 0.00136 | 0.00260 |
| B2 | 0.00094 | 0.00119 | 0.00161 | 0.00313 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00097 | 0.00117 | 0.00149 | 0.00275 |
| A2 | 0.00099 | 0.00119 | 0.00154 | 0.00306 |

| | | | | |
|----|---------|---------|---------|---------|
| B1 | 0.00098 | 0.00112 | 0.00151 | 0.00278 |
| B2 | 0.00099 | 0.00116 | 0.00149 | 0.00302 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00011489 | 0.00015132 | 0.00024898 | 0.00056255 |

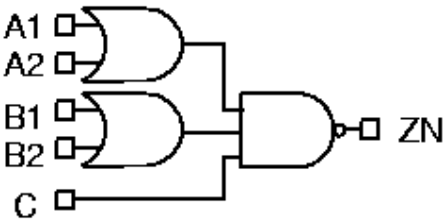
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.02235 | 0.02021 | 0.01768 | 0.01617 |
| A1→ZN_RISE | 0.03057 | 0.02725 | 0.02527 | 0.02280 |
| A2→ZN_FALL | 0.02681 | 0.02453 | 0.02164 | 0.01942 |
| A2→ZN_RISE | 0.03561 | 0.03213 | 0.03024 | 0.02752 |
| B1→ZN_FALL | 0.03080 | 0.02884 | 0.02427 | 0.02220 |
| B1→ZN_RISE | 0.04299 | 0.03937 | 0.03647 | 0.03348 |
| B2→ZN_FALL | 0.03445 | 0.03065 | 0.02766 | 0.02525 |
| B2→ZN_RISE | 0.04700 | 0.04329 | 0.04036 | 0.03762 |

OAI221HS

Cell Description

2-2-1 OAI
 $ZN = \neg((A1 \vee A2) \wedge (B1 \vee B2) \wedge C)$



Function Table

| A1 | A2 | B1 | B2 | C | ZN |
|----|----|----|----|---|----|
| 0 | 0 | X | X | X | 1 |
| 0 | 1 | 0 | 0 | X | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | X | 0 | 1 |
| 0 | 1 | 1 | X | 1 | 0 |
| 1 | X | 0 | 0 | X | 1 |
| 1 | X | 0 | 1 | 0 | 1 |
| 1 | X | 0 | 1 | 1 | 0 |
| 1 | X | 1 | X | 0 | 1 |
| 1 | X | 1 | X | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| OAI221HSV0 | 1.80 | 1.60 |
| OAI221HSV1 | 1.80 | 1.60 |
| OAI221HSV2 | 1.80 | 1.80 |
| OAI221HSV4 | 1.80 | 2.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00086 | 0.00106 | 0.00143 | 0.00390 |
| A2 | 0.00097 | 0.00123 | 0.00165 | 0.00401 |
| B1 | 0.00103 | 0.00130 | 0.00176 | 0.00409 |
| B2 | 0.00114 | 0.00146 | 0.00203 | 0.00421 |
| C | 0.00064 | 0.00081 | 0.00107 | 0.00372 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00113 | 0.00145 | 0.00179 | 0.00118 |
| A2 | 0.00105 | 0.00124 | 0.00151 | 0.00098 |
| B1 | 0.00102 | 0.00122 | 0.00143 | 0.00106 |
| B2 | 0.00102 | 0.00118 | 0.00150 | 0.00109 |
| C | 0.00100 | 0.00122 | 0.00152 | 0.00111 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00017042 | 0.00020135 | 0.00022567 | 0.00041534 |

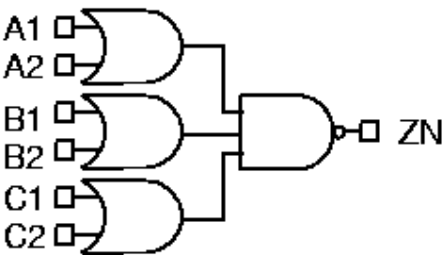
Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.04582 | 0.04018 | 0.03653 | 0.11293 |
| A1→ZN_RISE | 0.04471 | 0.03948 | 0.03798 | 0.11469 |
| A2→ZN_FALL | 0.04922 | 0.04379 | 0.03972 | 0.11948 |
| A2→ZN_RISE | 0.04751 | 0.04274 | 0.04096 | 0.11730 |
| B1→ZN_FALL | 0.04970 | 0.04405 | 0.04035 | 0.11891 |
| B1→ZN_RISE | 0.05027 | 0.04638 | 0.04391 | 0.12391 |
| B2→ZN_FALL | 0.05371 | 0.04946 | 0.04549 | 0.12544 |
| B2→ZN_RISE | 0.05251 | 0.04934 | 0.04822 | 0.12762 |
| C→ZN_FALL | 0.03307 | 0.02928 | 0.02603 | 0.10076 |
| C→ZN_RISE | 0.01882 | 0.01668 | 0.01550 | 0.07042 |

OAI222HS

Cell Description

2-2-2 OAI
 $ZN = \neg((A1 \vee A2) \wedge (B1 \vee B2) \wedge (C1 \vee C2))$



Function Table

| A1 | A2 | B1 | B2 | C1 | C2 | ZN |
|----|----|----|----|----|----|----|
| 0 | 0 | X | X | X | X | 1 |
| 0 | 1 | 0 | 0 | X | X | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | X | 0 |
| 0 | 1 | 1 | X | 0 | 0 | 1 |
| 0 | 1 | 1 | X | 0 | 1 | 0 |
| 0 | 1 | 1 | X | 1 | X | 0 |
| 1 | X | 0 | 0 | X | X | 1 |
| 1 | X | 0 | 1 | 0 | 0 | 1 |
| 1 | X | 0 | 1 | 0 | 1 | 0 |
| 1 | X | 0 | 1 | 1 | X | 0 |
| 1 | X | 1 | X | 0 | 0 | 1 |
| 1 | X | 1 | X | 0 | 1 | 0 |
| 1 | X | 1 | X | 1 | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| OAI222HSV0 | 1.80 | 2.00 |
| OAI222HSV1 | 1.80 | 2.20 |
| OAI222HSV2 | 1.80 | 2.00 |
| OAI222HSV4 | 1.80 | 2.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00108 | 0.00132 | 0.00172 | 0.00405 |
| A2 | 0.00120 | 0.00150 | 0.00196 | 0.00414 |

| | | | | |
|----|---------|---------|---------|---------|
| B1 | 0.00130 | 0.00155 | 0.00203 | 0.00425 |
| B2 | 0.00141 | 0.00184 | 0.00241 | 0.00437 |
| C1 | 0.00081 | 0.00102 | 0.00130 | 0.00376 |
| C2 | 0.00092 | 0.00119 | 0.00154 | 0.00387 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00109 | 0.00117 | 0.00150 | 0.00121 |
| A2 | 0.00103 | 0.00123 | 0.00150 | 0.00104 |
| B1 | 0.00099 | 0.00114 | 0.00148 | 0.00105 |
| B2 | 0.00104 | 0.00116 | 0.00149 | 0.00108 |
| C1 | 0.00101 | 0.00116 | 0.00144 | 0.00111 |
| C2 | 0.00101 | 0.00120 | 0.00149 | 0.00108 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00016897 | 0.00020385 | 0.00022747 | 0.00043284 |

Delay Table (ns)

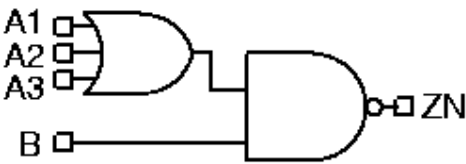
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.05033 | 0.04544 | 0.04014 | 0.11868 |
| A1→ZN_RISE | 0.05192 | 0.04492 | 0.04141 | 0.12396 |
| A2→ZN_FALL | 0.05408 | 0.05014 | 0.04448 | 0.12183 |
| A2→ZN_RISE | 0.05569 | 0.04844 | 0.04499 | 0.12637 |
| B1→ZN_FALL | 0.05761 | 0.05076 | 0.04518 | 0.12500 |
| B1→ZN_RISE | 0.06116 | 0.05175 | 0.04859 | 0.13453 |
| B2→ZN_FALL | 0.06085 | 0.05802 | 0.05180 | 0.12903 |
| B2→ZN_RISE | 0.06390 | 0.05833 | 0.05498 | 0.13740 |
| C1→ZN_FALL | 0.03771 | 0.03501 | 0.03035 | 0.10430 |
| C1→ZN_RISE | 0.03993 | 0.03453 | 0.03098 | 0.10870 |
| C2→ZN_FALL | 0.04169 | 0.03952 | 0.03479 | 0.10960 |
| C2→ZN_RISE | 0.04270 | 0.03815 | 0.03472 | 0.11146 |

OAI31HS

Cell Description

3-1 OAI

$$Z_N = \neg((A1 \vee A2 \vee A3) \wedge B)$$



Function Table

| A1 | A2 | A3 | B | ZN |
|----|----|----|---|----|
| 0 | 0 | 0 | X | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | X | 0 | 1 |
| 0 | 1 | X | 1 | 0 |
| 1 | X | X | 0 | 1 |
| 1 | X | X | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| OAI31HSV0 | 1.80 | 1.40 |
| OAI31HSV1 | 1.80 | 1.40 |
| OAI31HSV2 | 1.80 | 1.40 |
| OAI31HSV4 | 1.80 | 2.20 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00066 | 0.00084 | 0.00109 | 0.00366 |
| A2 | 0.00079 | 0.00102 | 0.00137 | 0.00378 |
| A3 | 0.00093 | 0.00120 | 0.00162 | 0.00393 |
| B | 0.00050 | 0.00064 | 0.00084 | 0.00350 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00097 | 0.00122 | 0.00149 | 0.00111 |
| A2 | 0.00095 | 0.00119 | 0.00151 | 0.00107 |

| | | | | |
|----|---------|---------|---------|---------|
| A3 | 0.00095 | 0.00116 | 0.00149 | 0.00108 |
| B | 0.00105 | 0.00126 | 0.00158 | 0.00106 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00012677 | 0.00017641 | 0.00024997 | 0.00042420 |

Delay Table (ns)

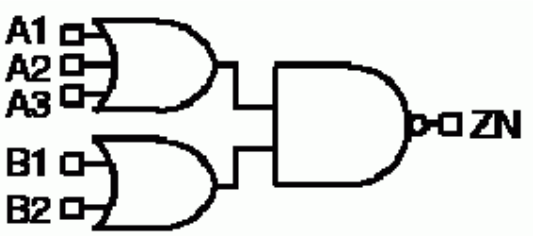
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.02768 | 0.02471 | 0.02200 | 0.08443 |
| A1→ZN_RISE | 0.05464 | 0.04993 | 0.04600 | 0.13736 |
| A2→ZN_FALL | 0.03147 | 0.02826 | 0.02568 | 0.08950 |
| A2→ZN_RISE | 0.06300 | 0.05828 | 0.05571 | 0.14512 |
| A3→ZN_FALL | 0.03396 | 0.03036 | 0.02755 | 0.09445 |
| A3→ZN_RISE | 0.06689 | 0.06168 | 0.05916 | 0.14983 |
| B→ZN_FALL | 0.02100 | 0.01851 | 0.01654 | 0.07376 |
| B→ZN_RISE | 0.01645 | 0.01465 | 0.01342 | 0.06468 |

OAI32HS

Cell Description

3-2 OAI

$$Z_N = \neg((A_1 \vee A_2 \vee A_3) \wedge (B_1 \vee B_2))$$



Function Table

| A1 | A2 | A3 | B1 | B2 | ZN |
|----|----|----|----|----|----|
| 0 | 0 | 0 | X | X | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | X | 0 |
| 0 | 1 | X | 0 | 0 | 1 |
| 0 | 1 | X | 0 | 1 | 0 |
| 0 | 1 | X | 1 | X | 0 |
| 1 | X | X | 0 | 0 | 1 |
| 1 | X | X | 0 | 1 | 0 |
| 1 | X | X | 1 | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| OAI32HSV0 | 1.80 | 1.60 |
| OAI32HSV1 | 1.80 | 1.60 |
| OAI32HSV2 | 1.80 | 1.60 |
| OAI32HSV4 | 1.80 | 2.60 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00069 | 0.00083 | 0.00104 | 0.00373 |
| A2 | 0.00084 | 0.00103 | 0.00132 | 0.00387 |
| A3 | 0.00097 | 0.00122 | 0.00160 | 0.00402 |
| B1 | 0.00103 | 0.00128 | 0.00166 | 0.00406 |
| B2 | 0.00115 | 0.00145 | 0.00190 | 0.00418 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00099 | 0.00119 | 0.00150 | 0.00103 |
| A2 | 0.00104 | 0.00121 | 0.00150 | 0.00105 |
| A3 | 0.00100 | 0.00120 | 0.00152 | 0.00109 |
| B1 | 0.00103 | 0.00120 | 0.00157 | 0.00103 |
| B2 | 0.00097 | 0.00118 | 0.00151 | 0.00099 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00017535 | 0.00024574 | 0.00039435 | 0.00047612 |

Delay Table (ns)

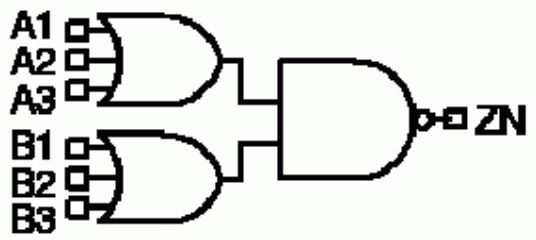
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.02562 | 0.02236 | 0.01912 | 0.08209 |
| A1→ZN_RISE | 0.05232 | 0.04533 | 0.03994 | 0.13339 |
| A2→ZN_FALL | 0.03006 | 0.02596 | 0.02265 | 0.08740 |
| A2→ZN_RISE | 0.06293 | 0.05472 | 0.04999 | 0.14316 |
| A3→ZN_FALL | 0.03283 | 0.02888 | 0.02534 | 0.09297 |
| A3→ZN_RISE | 0.06648 | 0.05934 | 0.05498 | 0.14888 |
| B1→ZN_FALL | 0.03361 | 0.02999 | 0.02619 | 0.08971 |
| B1→ZN_RISE | 0.05120 | 0.04598 | 0.04213 | 0.12141 |
| B2→ZN_FALL | 0.03677 | 0.03316 | 0.02940 | 0.09446 |
| B2→ZN_RISE | 0.05420 | 0.04916 | 0.04574 | 0.12485 |

OAI33HS

Cell Description

3-3 OAI

$$Z_N = \neg((A1 \vee A2 \vee A3) \wedge (B1 \vee B2 \vee B3))$$



Function Table

| A1 | A2 | A3 | B1 | B2 | B3 | ZN |
|----|----|----|----|----|----|----|
| 0 | 0 | 0 | X | X | X | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | X | 0 |
| 0 | 0 | 1 | 1 | X | X | 0 |
| 0 | 1 | X | 0 | 0 | 0 | 1 |
| 0 | 1 | X | 0 | 0 | 1 | 0 |
| 0 | 1 | X | 0 | 1 | X | 0 |
| 0 | 1 | X | 1 | X | X | 0 |
| 1 | X | X | 0 | 0 | 0 | 1 |
| 1 | X | X | 0 | 0 | 1 | 0 |
| 1 | X | X | 0 | 1 | X | 0 |
| 1 | X | X | 1 | X | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| OAI33HSV0 | 1.80 | 2.00 |
| OAI33HSV1 | 1.80 | 1.80 |
| OAI33HSV2 | 1.80 | 1.80 |
| OAI33HSV4 | 1.80 | 3.00 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00108 | 0.00132 | 0.00177 | 0.00416 |
| A2 | 0.00122 | 0.00151 | 0.00204 | 0.00428 |
| A3 | 0.00133 | 0.00167 | 0.00228 | 0.00440 |
| B1 | 0.00071 | 0.00087 | 0.00114 | 0.00380 |

| | | | | |
|----|---------|---------|---------|---------|
| B2 | 0.00086 | 0.00107 | 0.00143 | 0.00395 |
| B3 | 0.00100 | 0.00126 | 0.00170 | 0.00410 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00102 | 0.00117 | 0.00151 | 0.00105 |
| A2 | 0.00102 | 0.00121 | 0.00151 | 0.00102 |
| A3 | 0.00098 | 0.00119 | 0.00151 | 0.00097 |
| B1 | 0.00100 | 0.00120 | 0.00149 | 0.00099 |
| B2 | 0.00100 | 0.00120 | 0.00152 | 0.00108 |
| B3 | 0.00103 | 0.00122 | 0.00154 | 0.00106 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00018356 | 0.00024689 | 0.00039938 | 0.00048783 |

Delay Table (ns)

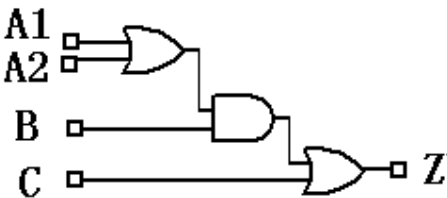
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.03457 | 0.03061 | 0.02742 | 0.09104 |
| A1→ZN_RISE | 0.07823 | 0.06905 | 0.06578 | 0.16411 |
| A2→ZN_FALL | 0.03780 | 0.03384 | 0.03055 | 0.09523 |
| A2→ZN_RISE | 0.08664 | 0.07792 | 0.07511 | 0.17215 |
| A3→ZN_FALL | 0.04019 | 0.03610 | 0.03270 | 0.09926 |
| A3→ZN_RISE | 0.08927 | 0.08054 | 0.07842 | 0.17487 |
| B1→ZN_FALL | 0.02429 | 0.02159 | 0.01889 | 0.07984 |
| B1→ZN_RISE | 0.05133 | 0.04479 | 0.04067 | 0.13334 |
| B2→ZN_FALL | 0.02800 | 0.02492 | 0.02231 | 0.08539 |
| B2→ZN_RISE | 0.06119 | 0.05404 | 0.05115 | 0.14497 |
| B3→ZN_FALL | 0.03129 | 0.02794 | 0.02487 | 0.09007 |
| B3→ZN_RISE | 0.06651 | 0.05913 | 0.05596 | 0.14973 |

OAO211HS

Cell Description

2-1-1 OAO

$$Z = (((A1A2) \& B) | C)$$



Function Table

| A1 | A2 | B | C | Z |
|----|----|---|---|---|
| 0 | 0 | X | 0 | 0 |
| 0 | 0 | X | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | X | 1 |
| 1 | X | 0 | 0 | 0 |
| 1 | X | 0 | 1 | 1 |
| 1 | X | 1 | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| OAO211HSV0 | 1.80 | 1.60 |
| OAO211HSV1 | 1.80 | 1.80 |
| OAO211HSV2 | 1.80 | 1.80 |
| OAO211HSV4 | 1.80 | 2.00 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00141 | 0.00170 | 0.00185 | 0.00320 |
| A2 | 0.00149 | 0.00178 | 0.00193 | 0.00335 |
| B | 0.00124 | 0.00152 | 0.00166 | 0.00286 |
| C | 0.00107 | 0.00135 | 0.00147 | 0.00254 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00088 | 0.00087 | 0.00089 | 0.00127 |

| | | | | |
|----|---------|---------|---------|---------|
| A2 | 0.00093 | 0.00093 | 0.00094 | 0.00133 |
| B | 0.00096 | 0.00095 | 0.00097 | 0.00136 |
| C | 0.00099 | 0.00099 | 0.00100 | 0.00141 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00018753 | 0.00020093 | 0.00020946 | 0.00042943 |

Delay Table (ns)

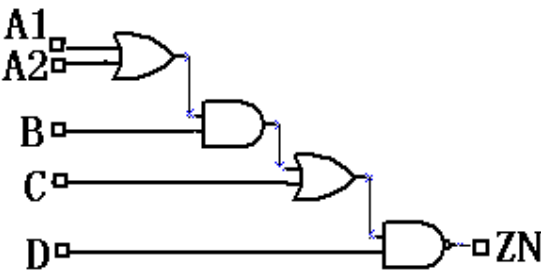
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.12049 | 0.12951 | 0.12692 | 0.12305 |
| A1→Z_RISE | 0.05932 | 0.06293 | 0.06521 | 0.05766 |
| A2→Z_FALL | 0.12275 | 0.13171 | 0.12931 | 0.12591 |
| A2→Z_RISE | 0.06000 | 0.06361 | 0.06610 | 0.05842 |
| B→Z_FALL | 0.07273 | 0.07804 | 0.07700 | 0.07365 |
| B→Z_RISE | 0.05048 | 0.05331 | 0.05545 | 0.04885 |
| C→Z_FALL | 0.06906 | 0.07531 | 0.07420 | 0.07042 |
| C→Z_RISE | 0.03445 | 0.03543 | 0.03617 | 0.03165 |

OAOAI2111HS

Cell Description

2-1-1-1 OAOAI

$$ZN = (!(((A1 \mid A2) \& B) \mid C) \& D))$$



Function Table

| A1 | A2 | B | C | D | ZN |
|----|----|---|---|---|----|
| 0 | 0 | X | 0 | X | 1 |
| 0 | 0 | X | 1 | 0 | 1 |
| 0 | 0 | X | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | X | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | X | 0 | 1 |
| 0 | 1 | 1 | X | 1 | 0 |
| 1 | X | 0 | 0 | X | 1 |
| 1 | X | 0 | 1 | 0 | 1 |
| 1 | X | 0 | 1 | 1 | 0 |
| 1 | X | 1 | X | 0 | 1 |
| 1 | X | 1 | X | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|---------------|------------|-----------|
| OAOAI2111HSV0 | 1.80 | 1.80 |
| OAOAI2111HSV1 | 1.80 | 1.80 |
| OAOAI2111HSV2 | 1.80 | 1.80 |
| OAOAI2111HSV4 | 1.80 | 3.20 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00108 | 0.00154 | 0.00182 | 0.00332 |
| A2 | 0.00118 | 0.00171 | 0.00202 | 0.00382 |
| B | 0.00091 | 0.00131 | 0.00155 | 0.00287 |
| C | 0.00067 | 0.00094 | 0.00112 | 0.00197 |

| | | | | |
|---|---------|---------|---------|---------|
| D | 0.00050 | 0.00069 | 0.00082 | 0.00137 |
|---|---------|---------|---------|---------|

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00093 | 0.00126 | 0.00141 | 0.00257 |
| A2 | 0.00099 | 0.00131 | 0.00147 | 0.00262 |
| B | 0.00096 | 0.00128 | 0.00143 | 0.00264 |
| C | 0.00101 | 0.00130 | 0.00149 | 0.00262 |
| D | 0.00097 | 0.00129 | 0.00146 | 0.00271 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00011664 | 0.00018879 | 0.00022163 | 0.00049849 |

Delay Table (ns)

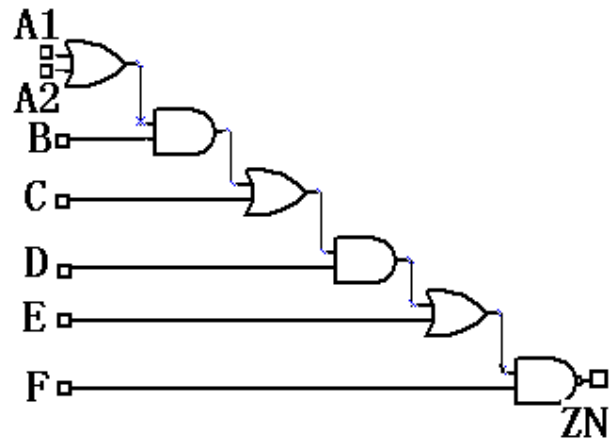
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.05442 | 0.04536 | 0.04381 | 0.03680 |
| A1→ZN_RISE | 0.09108 | 0.08206 | 0.08109 | 0.07129 |
| A2→ZN_FALL | 0.05626 | 0.04657 | 0.04512 | 0.03932 |
| A2→ZN_RISE | 0.09398 | 0.08504 | 0.08425 | 0.07574 |
| B→ZN_FALL | 0.04611 | 0.03817 | 0.03684 | 0.03159 |
| B→ZN_RISE | 0.05177 | 0.04603 | 0.04523 | 0.04020 |
| C→ZN_FALL | 0.02936 | 0.02394 | 0.02333 | 0.01914 |
| C→ZN_RISE | 0.04627 | 0.03945 | 0.03917 | 0.03299 |
| D→ZN_FALL | 0.02522 | 0.02035 | 0.01949 | 0.01527 |
| D→ZN_RISE | 0.01832 | 0.01530 | 0.01488 | 0.01225 |

OAOAOAI21111HS

Cell Description

2-1-1-1-1-1 OAOAOAI

$ZN = (!((((((A1 \wedge A2) \wedge B) \vee C) \wedge D) \vee E) \wedge F))$



Function Table

| A1 | A2 | B | C | D | E | F | ZN |
|----|----|---|---|---|---|---|----|
| 0 | 0 | X | 0 | X | 0 | X | 1 |
| 0 | 0 | X | 0 | X | 1 | 0 | 1 |
| 0 | 0 | X | 0 | X | 1 | 1 | 0 |
| 0 | 0 | X | 1 | 0 | 0 | X | 1 |
| 0 | 0 | X | 1 | 0 | 1 | 0 | 1 |
| 0 | 0 | X | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | X | 1 | 1 | X | 0 | 1 |
| 0 | 0 | X | 1 | 1 | X | 1 | 0 |
| 0 | 1 | 0 | 0 | X | 0 | X | 1 |
| 0 | 1 | 0 | 0 | X | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | X | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | X | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | X | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | X | 1 | 0 |
| 0 | 1 | 1 | X | 0 | 0 | X | 1 |
| 0 | 1 | 1 | X | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | X | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | X | 1 | X | 0 | 1 |
| 0 | 1 | 1 | X | 1 | X | 1 | 0 |
| 1 | X | 0 | 0 | X | 0 | X | 1 |
| 1 | X | 0 | 0 | X | 1 | 0 | 1 |
| 1 | X | 0 | 0 | X | 1 | 1 | 0 |
| 1 | X | 0 | 1 | 0 | 0 | X | 1 |
| 1 | X | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | X | 0 | 1 | 0 | 1 | 1 | 0 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | X | 0 | 1 | 1 | X | 0 | 1 |
| 1 | X | 0 | 1 | 1 | X | 1 | 0 |
| 1 | X | 1 | X | 0 | 0 | X | 1 |
| 1 | X | 1 | X | 0 | 1 | 0 | 1 |
| 1 | X | 1 | X | 0 | 1 | 1 | 0 |
| 1 | X | 1 | X | 1 | X | 0 | 1 |
| 1 | X | 1 | X | 1 | X | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------------|------------|-----------|
| OAOAOAI211111HSV0 | 1.80 | 2.40 |
| OAOAOAI211111HSV1 | 1.80 | 2.40 |
| OAOAOAI211111HSV2 | 1.80 | 2.40 |
| OAOAOAI211111HSV4 | 1.80 | 4.40 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00146 | 0.00214 | 0.00246 | 0.00464 |
| A2 | 0.00156 | 0.00230 | 0.00266 | 0.00514 |
| B | 0.00131 | 0.00192 | 0.00221 | 0.00422 |
| C | 0.00108 | 0.00158 | 0.00181 | 0.00343 |
| D | 0.00091 | 0.00134 | 0.00155 | 0.00292 |
| E | 0.00066 | 0.00095 | 0.00108 | 0.00204 |
| F | 0.00048 | 0.00067 | 0.00077 | 0.00138 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00094 | 0.00124 | 0.00139 | 0.00256 |
| A2 | 0.00101 | 0.00131 | 0.00146 | 0.00260 |
| B | 0.00098 | 0.00128 | 0.00143 | 0.00261 |
| C | 0.00102 | 0.00130 | 0.00145 | 0.00260 |
| D | 0.00094 | 0.00129 | 0.00145 | 0.00263 |
| E | 0.00094 | 0.00130 | 0.00145 | 0.00265 |
| F | 0.00097 | 0.00131 | 0.00148 | 0.00276 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00014593 | 0.00022860 | 0.00026618 | 0.00063220 |

Delay Table (ns)

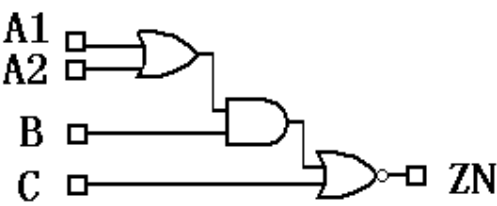
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.08634 | 0.07300 | 0.06944 | 0.05988 |
| A1→ZN_RISE | 0.15202 | 0.14164 | 0.13726 | 0.12669 |
| A2→ZN_FALL | 0.08749 | 0.07386 | 0.07023 | 0.06217 |

| | | | | |
|------------|---------|---------|---------|---------|
| A2→ZN_RISE | 0.15430 | 0.14475 | 0.14069 | 0.13101 |
| B→ZN_FALL | 0.07658 | 0.06465 | 0.06148 | 0.05379 |
| B→ZN_RISE | 0.09787 | 0.09055 | 0.08765 | 0.08099 |
| C→ZN_FALL | 0.05535 | 0.04698 | 0.04467 | 0.03819 |
| C→ZN_RISE | 0.09508 | 0.08719 | 0.08408 | 0.07717 |
| D→ZN_FALL | 0.05158 | 0.04336 | 0.04133 | 0.03505 |
| D→ZN_RISE | 0.05147 | 0.04636 | 0.04467 | 0.04029 |
| E→ZN_FALL | 0.02893 | 0.02428 | 0.02303 | 0.01935 |
| E→ZN_RISE | 0.04627 | 0.04100 | 0.03914 | 0.03500 |
| F→ZN_FALL | 0.02538 | 0.02074 | 0.01974 | 0.01575 |
| F→ZN_RISE | 0.01767 | 0.01498 | 0.01430 | 0.01231 |

OA0I211HS

Cell Description

2-1-1 OAOI
 $ZN = \neg(((A1 \mid A2) \& B) \mid C)$



Function Table

| A1 | A2 | B | C | ZN |
|----|----|---|---|----|
| 0 | 0 | X | 0 | 1 |
| 0 | 0 | X | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | X | 0 |
| 1 | X | 0 | 0 | 1 |
| 1 | X | 0 | 1 | 0 |
| 1 | X | 1 | X | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| OA0I211HSV0 | 1.80 | 1.40 |
| OA0I211HSV1 | 1.80 | 1.40 |
| OA0I211HSV2 | 1.80 | 1.40 |
| OA0I211HSV4 | 1.80 | 2.40 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00085 | 0.00127 | 0.00145 | 0.00263 |
| A2 | 0.00094 | 0.00142 | 0.00163 | 0.00306 |
| B | 0.00068 | 0.00100 | 0.00114 | 0.00205 |
| C | 0.00045 | 0.00064 | 0.00072 | 0.00122 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00092 | 0.00124 | 0.00140 | 0.00267 |

| | | | | |
|----|---------|---------|---------|---------|
| A2 | 0.00098 | 0.00131 | 0.00146 | 0.00292 |
| B | 0.00098 | 0.00131 | 0.00147 | 0.00293 |
| C | 0.00097 | 0.00131 | 0.00147 | 0.00268 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00012533 | 0.00022807 | 0.00027189 | 0.00065745 |

Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.03236 | 0.02730 | 0.02565 | 0.02196 |
| A1→ZN_RISE | 0.07569 | 0.07019 | 0.06721 | 0.05902 |
| A2→ZN_FALL | 0.03251 | 0.02725 | 0.02558 | 0.02281 |
| A2→ZN_RISE | 0.07819 | 0.07304 | 0.07025 | 0.06289 |
| B→ZN_FALL | 0.02439 | 0.01994 | 0.01865 | 0.01608 |
| B→ZN_RISE | 0.04039 | 0.03624 | 0.03443 | 0.02969 |
| C→ZN_FALL | 0.01402 | 0.01172 | 0.01101 | 0.00903 |
| C→ZN_RISE | 0.03482 | 0.03007 | 0.02827 | 0.02293 |

OR2HS

Cell Description

2-Input OR

$Z=(A1|A2)$



Function Table

| A1 | A2 | Z |
|----|----|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| OR2HSV0 | 1.80 | 1.00 |
| OR2HSV0RD | 1.80 | 1.00 |
| OR2HSV1 | 1.80 | 1.00 |
| OR2HSV1RD | 1.80 | 1.00 |
| OR2HSV2 | 1.80 | 1.20 |
| OR2HSV2RD | 1.80 | 1.20 |
| OR2HSV4 | 1.80 | 1.40 |
| OR2HSV4RD | 1.80 | 1.40 |
| OR2HSV4RQ | 1.80 | 1.40 |
| OR2HSV8 | 1.80 | 2.40 |
| OR2HSV8RD | 1.80 | 2.40 |
| OR2HSV8RQ | 1.80 | 1.80 |
| OR2HSV12 | 1.80 | 2.80 |
| OR2HSV12RD | 1.80 | 3.40 |
| OR2HSV12RQ | 1.80 | 2.80 |
| OR2HSV16 | 1.80 | 3.80 |
| OR2HSV16RD | 1.80 | 4.80 |
| OR2HSV16RQ | 1.80 | 3.40 |

Pin Power (uW/MHz)

| Pin | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-----|----|------|----|------|----|------|----|------|
|-----|----|------|----|------|----|------|----|------|

| | | | | | | | | |
|----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00106 | 0.00101 | 0.00122 | 0.00125 | 0.00147 | 0.00142 | 0.00253 | 0.00248 |
| A2 | 0.00119 | 0.00113 | 0.00136 | 0.00137 | 0.00160 | 0.00157 | 0.00274 | 0.00275 |

| | | | | | | | | |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| Pin | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
| A1 | 0.00225 | 0.00484 | 0.00473 | 0.00422 | 0.00643 | 0.00689 | 0.00630 | 0.00851 |
| A2 | 0.00240 | 0.00529 | 0.00527 | 0.00445 | 0.00697 | 0.00783 | 0.00667 | 0.00933 |

| | | |
|-----|---------|---------|
| Pin | V16RD | V16RQ |
| A1 | 0.00928 | 0.00838 |
| A2 | 0.01064 | 0.00886 |

Pin Capacitance (pf)

| | | | | | | | | |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| Pin | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
| A1 | 0.00108 | 0.00104 | 0.00108 | 0.00103 | 0.00108 | 0.00112 | 0.00146 | 0.00167 |
| A2 | 0.00108 | 0.00103 | 0.00108 | 0.00102 | 0.00107 | 0.00110 | 0.00146 | 0.00163 |

| | | | | | | | | |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| Pin | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
| A1 | 0.00101 | 0.00256 | 0.00299 | 0.00133 | 0.00288 | 0.00439 | 0.00210 | 0.00389 |
| A2 | 0.00112 | 0.00290 | 0.00322 | 0.00137 | 0.00318 | 0.00444 | 0.00240 | 0.00392 |

| | | |
|-----|---------|---------|
| Pin | V16RD | V16RQ |
| A1 | 0.00632 | 0.00244 |
| A2 | 0.00639 | 0.00279 |

Max Leakage Power (uW)

| | | | | | | | |
|------------|------------|------------|------------|------------|------------|------------|------------|
| V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
| 0.00016617 | 0.00015582 | 0.00017665 | 0.00016835 | 0.00017537 | 0.00017163 | 0.00036716 | 0.00038749 |

| | | | | | | | |
|------------|------------|------------|------------|------------|------------|------------|------------|
| V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
| 0.00027907 | 0.00072990 | 0.00078046 | 0.00058953 | 0.00098941 | 0.00120980 | 0.00093950 | 0.00137620 |

| | |
|------------|------------|
| V16RD | V16RQ |
| 0.00171090 | 0.00129460 |

Delay Table (ns)

| | | | | | | | | |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| Description | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
| A1→Z_FALL | 0.05347 | 0.05439 | 0.05585 | 0.05642 | 0.05983 | 0.05315 | 0.06029 | 0.05242 |
| A1→Z_RISE | 0.03207 | 0.03405 | 0.03240 | 0.03452 | 0.03442 | 0.03592 | 0.03178 | 0.03132 |
| A2→Z_FALL | 0.05710 | 0.05794 | 0.05958 | 0.05979 | 0.06333 | 0.05676 | 0.06450 | 0.05663 |
| A2→Z_RISE | 0.03386 | 0.03583 | 0.03422 | 0.03627 | 0.03620 | 0.03821 | 0.03355 | 0.03328 |

| | | | | | | | | |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| Description | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
| A1→Z_FALL | 0.07850 | 0.05578 | 0.04844 | 0.07736 | 0.05769 | 0.04539 | 0.07326 | 0.05576 |

| | | | | | | | | |
|-----------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→Z_RISE | 0.04282 | 0.02948 | 0.02887 | 0.04712 | 0.03431 | 0.02830 | 0.04333 | 0.03446 |
| A2→Z_FALL | 0.08315 | 0.06082 | 0.05320 | 0.08171 | 0.06260 | 0.05050 | 0.07815 | 0.06074 |
| A2→Z_RISE | 0.04483 | 0.03238 | 0.03192 | 0.04910 | 0.03771 | 0.03085 | 0.04709 | 0.03710 |

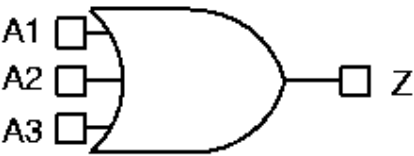
| Description | V16RD | V16RQ |
|-------------|---------|---------|
| A1→Z_FALL | 0.04413 | 0.07478 |
| A1→Z_RISE | 0.02808 | 0.04405 |
| A2→Z_FALL | 0.04925 | 0.07972 |
| A2→Z_RISE | 0.03079 | 0.04777 |

OR3HS

Cell Description

3-Input OR

$$Z=(A1|A2|A3)$$



Function Table

| A1 | A2 | A3 | Z |
|----|----|----|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | X | 1 |
| 1 | X | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| OR3HSV0 | 1.80 | 1.40 |
| OR3HSV0RD | 1.80 | 1.40 |
| OR3HSV1 | 1.80 | 1.40 |
| OR3HSV1RD | 1.80 | 1.40 |
| OR3HSV2 | 1.80 | 1.40 |
| OR3HSV2RD | 1.80 | 1.40 |
| OR3HSV4 | 1.80 | 1.60 |
| OR3HSV4RD | 1.80 | 1.60 |
| OR3HSV4RQ | 1.80 | 1.60 |
| OR3HSV8 | 1.80 | 2.80 |
| OR3HSV8RD | 1.80 | 2.80 |
| OR3HSV8RQ | 1.80 | 2.00 |
| OR3HSV12 | 1.80 | 3.40 |
| OR3HSV12RD | 1.80 | 4.00 |
| OR3HSV12RQ | 1.80 | 3.40 |
| OR3HSV16 | 1.80 | 4.60 |
| OR3HSV16RD | 1.80 | 6.00 |
| OR3HSV16RQ | 1.80 | 3.80 |

Pin Power (uW/MHz)

| Pin | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00119 | 0.00115 | 0.00137 | 0.00146 | 0.00162 | 0.00159 | 0.00265 | 0.00258 |
| A2 | 0.00131 | 0.00127 | 0.00148 | 0.00160 | 0.00174 | 0.00174 | 0.00286 | 0.00284 |
| A3 | 0.00146 | 0.00140 | 0.00162 | 0.00177 | 0.00187 | 0.00190 | 0.00306 | 0.00310 |

| Pin | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00241 | 0.00511 | 0.00485 | 0.00444 | 0.00669 | 0.00721 | 0.00668 | 0.00888 |
| A2 | 0.00253 | 0.00558 | 0.00542 | 0.00466 | 0.00726 | 0.00819 | 0.00706 | 0.00971 |
| A3 | 0.00266 | 0.00600 | 0.00598 | 0.00489 | 0.00783 | 0.00910 | 0.00745 | 0.01053 |

| Pin | V16RD | V16RQ |
|-----|---------|---------|
| A1 | 0.00963 | 0.00880 |
| A2 | 0.01098 | 0.00929 |
| A3 | 0.01224 | 0.00980 |

Pin Capacitance (pf)

| Pin | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00109 | 0.00103 | 0.00109 | 0.00111 | 0.00111 | 0.00110 | 0.00142 | 0.00151 |
| A2 | 0.00105 | 0.00107 | 0.00103 | 0.00115 | 0.00109 | 0.00114 | 0.00140 | 0.00142 |
| A3 | 0.00108 | 0.00104 | 0.00106 | 0.00111 | 0.00108 | 0.00111 | 0.00142 | 0.00148 |

| Pin | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00100 | 0.00254 | 0.00270 | 0.00129 | 0.00265 | 0.00413 | 0.00196 | 0.00359 |
| A2 | 0.00098 | 0.00277 | 0.00292 | 0.00127 | 0.00285 | 0.00400 | 0.00224 | 0.00346 |
| A3 | 0.00104 | 0.00292 | 0.00314 | 0.00134 | 0.00311 | 0.00411 | 0.00247 | 0.00353 |

| Pin | V16RD | V16RQ |
|-----|---------|---------|
| A1 | 0.00569 | 0.00232 |
| A2 | 0.00553 | 0.00255 |
| A3 | 0.00566 | 0.00279 |

Max Leakage Power (uW)

| V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00022965 | 0.00020771 | 0.00023788 | 0.00022897 | 0.00025385 | 0.00023249 | 0.00048450 | 0.00039305 |

| V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00031078 | 0.00102350 | 0.00091548 | 0.00057841 | 0.00104220 | 0.00130270 | 0.00093373 | 0.00143100 |

| V16RD | V16RQ |
|------------|------------|
| 0.00169520 | 0.00128550 |

Delay Table (ns)

| Description | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-------------|----|------|----|------|----|------|----|------|
|-------------|----|------|----|------|----|------|----|------|

| | | | | | | | | |
|-----------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→Z_FALL | 0.07964 | 0.08127 | 0.08350 | 0.07626 | 0.09018 | 0.07788 | 0.08687 | 0.07370 |
| A1→Z_RISE | 0.03512 | 0.03765 | 0.03548 | 0.03906 | 0.03689 | 0.03988 | 0.03297 | 0.03843 |
| A2→Z_FALL | 0.08667 | 0.08882 | 0.09008 | 0.08418 | 0.09699 | 0.08579 | 0.09570 | 0.08231 |
| A2→Z_RISE | 0.03662 | 0.03941 | 0.03682 | 0.04143 | 0.03822 | 0.04224 | 0.03449 | 0.04102 |
| A3→Z_FALL | 0.09156 | 0.09339 | 0.09456 | 0.08853 | 0.10076 | 0.09001 | 0.09977 | 0.08684 |
| A3→Z_RISE | 0.03853 | 0.04140 | 0.03867 | 0.04380 | 0.03992 | 0.04463 | 0.03592 | 0.04350 |

| Description | V4RQ | V8 | V8RD | V8RQ | V12 | V12RD | V12RQ | V16 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→Z_FALL | 0.11457 | 0.08038 | 0.06657 | 0.10989 | 0.08065 | 0.06251 | 0.10361 | 0.07801 |
| A1→Z_RISE | 0.04473 | 0.03029 | 0.03329 | 0.05443 | 0.04031 | 0.03423 | 0.04915 | 0.04162 |
| A2→Z_FALL | 0.12161 | 0.09090 | 0.07712 | 0.11858 | 0.09109 | 0.07343 | 0.11374 | 0.08889 |
| A2→Z_RISE | 0.04598 | 0.03289 | 0.03703 | 0.05671 | 0.04431 | 0.03775 | 0.05316 | 0.04493 |
| A3→Z_FALL | 0.12662 | 0.09518 | 0.08237 | 0.12324 | 0.09649 | 0.07794 | 0.11954 | 0.09348 |
| A3→Z_RISE | 0.04795 | 0.03492 | 0.04008 | 0.05949 | 0.04792 | 0.04000 | 0.05713 | 0.04762 |

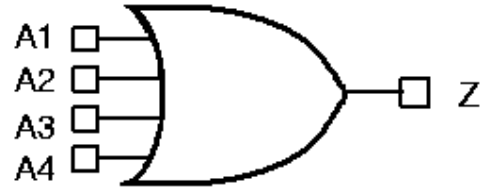
| Description | V16RD | V16RQ |
|-------------|---------|---------|
| A1→Z_FALL | 0.06106 | 0.10489 |
| A1→Z_RISE | 0.03403 | 0.05137 |
| A2→Z_FALL | 0.07210 | 0.11494 |
| A2→Z_RISE | 0.03768 | 0.05554 |
| A3→Z_FALL | 0.07654 | 0.12053 |
| A3→Z_RISE | 0.04023 | 0.05967 |

OR4HS

Cell Description

4-Input OR

$Z=(A1|A2|A3|A4)$



Function Table

| A1 | A2 | A3 | A4 | Z |
|----|----|----|----|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | X | 1 |
| 0 | 1 | X | X | 1 |
| 1 | X | X | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| OR4HSV0 | 1.80 | 1.60 |
| OR4HSV0RD | 1.80 | 1.60 |
| OR4HSV1 | 1.80 | 1.60 |
| OR4HSV1RD | 1.80 | 1.60 |
| OR4HSV2 | 1.80 | 1.60 |
| OR4HSV2RD | 1.80 | 1.60 |
| OR4HSV4 | 1.80 | 1.80 |
| OR4HSV4RD | 1.80 | 3.80 |
| OR4HSV4RQ | 1.80 | 1.80 |
| OR4HSV8 | 1.80 | 3.40 |
| OR4HSV8RD | 1.80 | 5.60 |
| OR4HSV8RQ | 1.80 | 4.20 |
| OR4HSV12RQ | 1.80 | 5.80 |
| OR4HSV16RQ | 1.80 | 8.40 |

Pin Power (uW/MHz)

| Pin | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00130 | 0.00126 | 0.00147 | 0.00151 | 0.00167 | 0.00159 | 0.00283 | 0.00358 |
| A2 | 0.00141 | 0.00139 | 0.00158 | 0.00164 | 0.00179 | 0.00173 | 0.00304 | 0.00383 |

| | | | | | | | | |
|----|---------|---------|---------|---------|---------|---------|---------|---------|
| A3 | 0.00154 | 0.00154 | 0.00171 | 0.00180 | 0.00191 | 0.00187 | 0.00323 | 0.00437 |
| A4 | 0.00169 | 0.00171 | 0.00185 | 0.00195 | 0.00206 | 0.00204 | 0.00348 | 0.00462 |

| Pin | V4RQ | V8 | V8RD | V8RQ | V12RQ | V16RQ |
|-----|---------|---------|---------|---------|---------|---------|
| A1 | 0.00256 | 0.00553 | 0.00589 | 0.00565 | 0.00837 | 0.01053 |
| A2 | 0.00268 | 0.00599 | 0.00646 | 0.00589 | 0.00873 | 0.01099 |
| A3 | 0.00278 | 0.00648 | 0.00715 | 0.00676 | 0.01013 | 0.01307 |
| A4 | 0.00294 | 0.00693 | 0.00770 | 0.00698 | 0.01049 | 0.01353 |

Pin Capacitance (pf)

| Pin | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00113 | 0.00116 | 0.00111 | 0.00114 | 0.00105 | 0.00108 | 0.00140 | 0.00148 |
| A2 | 0.00109 | 0.00111 | 0.00109 | 0.00112 | 0.00103 | 0.00106 | 0.00141 | 0.00142 |
| A3 | 0.00110 | 0.00113 | 0.00109 | 0.00111 | 0.00102 | 0.00105 | 0.00135 | 0.00149 |
| A4 | 0.00109 | 0.00112 | 0.00110 | 0.00112 | 0.00101 | 0.00104 | 0.00146 | 0.00145 |

| Pin | V4RQ | V8 | V8RD | V8RQ | V12RQ | V16RQ |
|-----|---------|---------|---------|---------|---------|---------|
| A1 | 0.00101 | 0.00248 | 0.00277 | 0.00123 | 0.00177 | 0.00212 |
| A2 | 0.00104 | 0.00270 | 0.00297 | 0.00125 | 0.00192 | 0.00224 |
| A3 | 0.00097 | 0.00294 | 0.00278 | 0.00125 | 0.00179 | 0.00213 |
| A4 | 0.00107 | 0.00313 | 0.00298 | 0.00127 | 0.00192 | 0.00234 |

Max Leakage Power (uW)

| V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00030087 | 0.00028281 | 0.00031412 | 0.00029869 | 0.00028504 | 0.00027912 | 0.00060559 | 0.00076066 |

| V4RQ | V8 | V8RD | V8RQ | V12RQ | V16RQ |
|------------|------------|------------|------------|------------|------------|
| 0.00037840 | 0.00128150 | 0.00141080 | 0.00113510 | 0.00183940 | 0.00217700 |

Delay Table (ns)

| Description | V0 | V0RD | V1 | V1RD | V2 | V2RD | V4 | V4RD |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→Z_FALL | 0.10580 | 0.09400 | 0.11001 | 0.09905 | 0.11529 | 0.09981 | 0.11444 | 0.06140 |
| A1→Z_RISE | 0.03738 | 0.04017 | 0.03710 | 0.04010 | 0.03823 | 0.04026 | 0.03428 | 0.05074 |
| A2→Z_FALL | 0.11622 | 0.10499 | 0.12065 | 0.11058 | 0.12639 | 0.11175 | 0.12896 | 0.06492 |
| A2→Z_RISE | 0.03852 | 0.04189 | 0.03836 | 0.04195 | 0.03960 | 0.04227 | 0.03583 | 0.05405 |
| A3→Z_FALL | 0.12443 | 0.11343 | 0.12937 | 0.11905 | 0.13392 | 0.11928 | 0.13601 | 0.07187 |
| A3→Z_RISE | 0.04014 | 0.04399 | 0.04002 | 0.04410 | 0.04118 | 0.04431 | 0.03695 | 0.05935 |
| A4→Z_FALL | 0.13032 | 0.11926 | 0.13432 | 0.12401 | 0.13956 | 0.12496 | 0.14263 | 0.07518 |
| A4→Z_RISE | 0.04146 | 0.04567 | 0.04121 | 0.04568 | 0.04261 | 0.04614 | 0.03812 | 0.06204 |

| Description | V4RQ | V8 | V8RD | V8RQ | V12RQ | V16RQ |
|-------------|---------|---------|---------|---------|---------|---------|
| A1→Z_FALL | 0.14918 | 0.10665 | 0.05094 | 0.08801 | 0.08175 | 0.08148 |
| A1→Z_RISE | 0.04558 | 0.03156 | 0.04281 | 0.07392 | 0.07573 | 0.07491 |

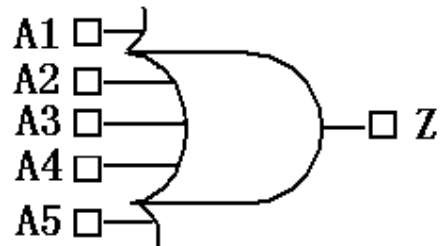
| | | | | | | |
|-----------|---------|---------|---------|---------|---------|---------|
| A2→Z_FALL | 0.16231 | 0.12242 | 0.05547 | 0.09218 | 0.08610 | 0.08553 |
| A2→Z_RISE | 0.04710 | 0.03401 | 0.04829 | 0.07896 | 0.08133 | 0.07998 |
| A3→Z_FALL | 0.16720 | 0.13377 | 0.05709 | 0.09849 | 0.09270 | 0.09373 |
| A3→Z_RISE | 0.04818 | 0.03612 | 0.04678 | 0.07852 | 0.08068 | 0.08222 |
| A4→Z_FALL | 0.17567 | 0.13984 | 0.06158 | 0.10275 | 0.09713 | 0.09797 |
| A4→Z_RISE | 0.05022 | 0.03758 | 0.05173 | 0.08176 | 0.08443 | 0.08754 |

OR5HS

Cell Description

5-input OR

$Z=(A1|A2|A3|A4|A5)$



Function Table

| A1 | A2 | A3 | A4 | A5 | Z |
|----|----|----|----|----|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | X | 1 |
| 0 | 0 | 1 | X | X | 1 |
| 0 | 1 | X | X | X | 1 |
| 1 | X | X | X | X | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| OR5HSV0RD | 1.80 | 2.20 |
| OR5HSV1RD | 1.80 | 2.20 |
| OR5HSV2RD | 1.80 | 2.60 |
| OR5HSV4RD | 1.80 | 3.20 |
| OR5HSV4RQ | 1.80 | 3.20 |
| OR5HSV8RD | 1.80 | 6.40 |
| OR5HSV8RQ | 1.80 | 4.20 |
| OR5HSV12RQ | 1.80 | 6.20 |
| OR5HSV16RQ | 1.80 | 8.00 |

Pin Power (uW/MHz)

| Pin | V0RD | V1RD | V2RD | V4RD | V4RQ | V8RD | V8RQ | V12RQ |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00121 | 0.00155 | 0.00186 | 0.00317 | 0.00291 | 0.00604 | 0.00557 | 0.00802 |
| A2 | 0.00131 | 0.00166 | 0.00200 | 0.00343 | 0.00302 | 0.00657 | 0.00580 | 0.00842 |
| A3 | 0.00151 | 0.00188 | 0.00227 | 0.00390 | 0.00369 | 0.00754 | 0.00705 | 0.00998 |
| A4 | 0.00166 | 0.00202 | 0.00241 | 0.00415 | 0.00380 | 0.00820 | 0.00725 | 0.01043 |
| A5 | 0.00181 | 0.00217 | 0.00255 | 0.00440 | 0.00394 | 0.00876 | 0.00748 | 0.01085 |

| Pin | V16RQ |
|-----|---------|
| A1 | 0.01032 |
| A2 | 0.01082 |
| A3 | 0.01306 |
| A4 | 0.01362 |
| A5 | 0.01412 |

Pin Capacitance (pf)

| Pin | V0RD | V1RD | V2RD | V4RD | V4RQ | V8RD | V8RQ | V12RQ |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | 0.00096 | 0.00105 | 0.00116 | 0.00160 | 0.00111 | 0.00290 | 0.00139 | 0.00208 |
| A2 | 0.00093 | 0.00100 | 0.00110 | 0.00158 | 0.00099 | 0.00292 | 0.00133 | 0.00199 |
| A3 | 0.00109 | 0.00109 | 0.00108 | 0.00148 | 0.00101 | 0.00277 | 0.00131 | 0.00179 |
| A4 | 0.00112 | 0.00110 | 0.00110 | 0.00143 | 0.00107 | 0.00267 | 0.00129 | 0.00182 |
| A5 | 0.00109 | 0.00107 | 0.00108 | 0.00147 | 0.00107 | 0.00274 | 0.00133 | 0.00191 |

| Pin | V16RQ |
|-----|---------|
| A1 | 0.00246 |
| A2 | 0.00249 |
| A3 | 0.00237 |
| A4 | 0.00232 |
| A5 | 0.00240 |

Max Leakage Power (uW)

| V0RD | V1RD | V2RD | V4RD | V4RQ | V8RD | V8RQ | V12RQ |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00034290 | 0.00037817 | 0.00044078 | 0.00073720 | 0.00061385 | 0.00163230 | 0.00121960 | 0.00191660 |

| V16RQ |
|------------|
| 0.00266010 |

Delay Table (ns)

| Description | V0RD | V1RD | V2RD | V4RD | V4RQ | V8RD | V8RQ | V12RQ |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| A1→Z_FALL | 0.07125 | 0.06362 | 0.06233 | 0.05945 | 0.08800 | 0.05612 | 0.08977 | 0.08294 |
| A1→Z_RISE | 0.03942 | 0.04081 | 0.04400 | 0.03795 | 0.05141 | 0.03502 | 0.05698 | 0.05334 |
| A2→Z_FALL | 0.07483 | 0.06692 | 0.06565 | 0.06365 | 0.09063 | 0.06064 | 0.09351 | 0.08737 |
| A2→Z_RISE | 0.04132 | 0.04315 | 0.04679 | 0.04108 | 0.05371 | 0.03791 | 0.06005 | 0.06122 |
| A3→Z_FALL | 0.08585 | 0.08754 | 0.09582 | 0.09055 | 0.14092 | 0.08633 | 0.14177 | 0.12590 |
| A3→Z_RISE | 0.04680 | 0.04682 | 0.04803 | 0.05011 | 0.05849 | 0.04580 | 0.07295 | 0.07292 |
| A4→Z_FALL | 0.09390 | 0.09533 | 0.10360 | 0.09928 | 0.14804 | 0.09873 | 0.14987 | 0.13795 |
| A4→Z_RISE | 0.04906 | 0.04896 | 0.05008 | 0.05259 | 0.05960 | 0.05029 | 0.07470 | 0.07821 |
| A5→Z_FALL | 0.09842 | 0.09949 | 0.10797 | 0.10378 | 0.15326 | 0.10327 | 0.15492 | 0.14327 |
| A5→Z_RISE | 0.05146 | 0.05097 | 0.05191 | 0.05522 | 0.06171 | 0.05280 | 0.07762 | 0.08181 |

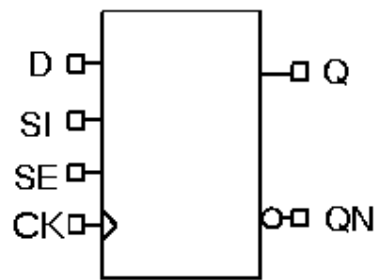
| Description | V16RQ |
|-------------|-------|
|-------------|-------|

| | |
|-----------|---------|
| A1→Z_FALL | 0.08292 |
| A1→Z_RISE | 0.05313 |
| A2→Z_FALL | 0.08768 |
| A2→Z_RISE | 0.05649 |
| A3→Z_FALL | 0.13014 |
| A3→Z_RISE | 0.06986 |
| A4→Z_FALL | 0.14194 |
| A4→Z_RISE | 0.07477 |
| A5→Z_FALL | 0.14688 |
| A5→Z_RISE | 0.07737 |

SDHS

Cell Description

Scan D Flip-Flop
Q = rising (CK) ? (SE&SI | !SE&D) : pre_Q
QN = !Q



Function Table

| CK<1> | CK | SE | SI | D | Q |
|-------|----|----|----|---|------|
| 0 | 0 | X | X | X | Q<1> |
| 0 | 1 | 0 | X | 0 | 0 |
| 0 | 1 | 0 | X | 1 | 1 |
| 0 | 1 | 1 | 0 | X | 0 |
| 0 | 1 | 1 | 1 | X | 1 |
| 1 | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| SDHSV1 | 1.80 | 6.20 |
| SDHSV2 | 1.80 | 6.60 |
| SDHSV4 | 1.80 | 6.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00292 | 0.00299 | 0.00305 |
| D | 0.00080 | 0.00090 | 0.00091 |
| Q | 0.00187 | 0.00216 | 0.00308 |
| QN | 0.00188 | 0.00215 | 0.00303 |
| SE | 0.00156 | 0.00168 | 0.00168 |
| SI | 0.00091 | 0.00101 | 0.00102 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00107 | 0.00109 | 0.00108 |
| D | 0.00160 | 0.00159 | 0.00161 |

| | | | |
|----|---------|---------|---------|
| SE | 0.00206 | 0.00209 | 0.00209 |
| SI | 0.00092 | 0.00093 | 0.00091 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00059692 | 0.00070158 | 0.00094785 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.11587 | 0.10597 | 0.11656 |
| CK→Q_RISE | 0.12617 | 0.12033 | 0.12635 |
| CK→QN_FALL | 0.16473 | 0.15881 | 0.16706 |
| CK→QN_RISE | 0.15952 | 0.15034 | 0.16413 |

Timing Constraints (ns)

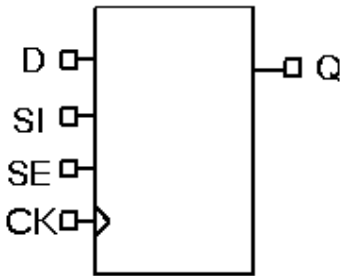
| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.03980 | -0.04478 | -0.03980 |
| D | hold_RISE→CK | -0.04476 | -0.04974 | -0.04476 |
| D | setup_FALL→CK | 0.07462 | 0.08459 | 0.08956 |
| D | setup_RISE→CK | 0.05472 | 0.05970 | 0.05970 |
| SE | hold_FALL→CK | -0.06466 | -0.06965 | -0.06965 |
| SE | hold_RISE→CK | -0.08456 | -0.09452 | -0.08955 |
| SE | setup_FALL→CK | 0.07462 | 0.07959 | 0.07960 |
| SE | setup_RISE→CK | 0.13431 | 0.14427 | 0.14426 |
| SI | hold_FALL→CK | -0.07461 | -0.07959 | -0.07462 |
| SI | hold_RISE→CK | -0.06964 | -0.07463 | -0.06965 |
| SI | setup_FALL→CK | 0.11939 | 0.13433 | 0.13434 |
| SI | setup_RISE→CK | 0.07959 | 0.08956 | 0.08456 |
| CK | minpwh | 0.07371 | 0.07362 | 0.07761 |
| CK | minpwl | 0.09051 | 0.09537 | 0.10036 |

SDQHS

Cell Description

Scan D Flip-Flop

Q = rising (CK) ? (SE&SI | !SE&D) : pre_Q



Function Table

| CK<1> | CK | SE | D | SI | Q |
|-------|----|----|---|----|------|
| 0 | 0 | X | X | X | Q<1> |
| 0 | 1 | 0 | 0 | X | 0 |
| 0 | 1 | 0 | 1 | X | 1 |
| 0 | 1 | 1 | X | 0 | 0 |
| 0 | 1 | 1 | X | 1 | 1 |
| 1 | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| SDQHVS1 | 1.80 | 5.80 |
| SDQHVS2 | 1.80 | 5.80 |
| SDQHVS4 | 1.80 | 6.00 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00290 | 0.00293 | 0.00302 |
| D | 0.00079 | 0.00086 | 0.00087 |
| Q | 0.00393 | 0.00457 | 0.00570 |
| SE | 0.00155 | 0.00159 | 0.00160 |
| SI | 0.00092 | 0.00098 | 0.00099 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00110 | 0.00102 | 0.00106 |
| D | 0.00148 | 0.00155 | 0.00155 |
| SE | 0.00207 | 0.00184 | 0.00184 |

| | | | |
|----|---------|---------|---------|
| SI | 0.00093 | 0.00092 | 0.00093 |
|----|---------|---------|---------|

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00054800 | 0.00057812 | 0.00072046 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.10897 | 0.11102 | 0.12342 |
| CK→Q_RISE | 0.12308 | 0.11949 | 0.12392 |

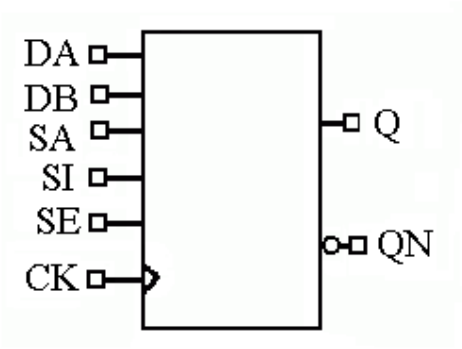
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.03483 | -0.03981 | -0.03485 |
| D | hold_RISE→CK | -0.04478 | -0.04479 | -0.03980 |
| D | setup_FALL→CK | 0.07959 | 0.07960 | 0.08459 |
| D | setup_RISE→CK | 0.05970 | 0.05473 | 0.05473 |
| SE | hold_FALL→CK | -0.06964 | -0.06467 | -0.06468 |
| SE | hold_RISE→CK | -0.07960 | -0.08955 | -0.08458 |
| SE | setup_FALL→CK | 0.07960 | 0.07960 | 0.07961 |
| SE | setup_RISE→CK | 0.13930 | 0.13931 | 0.13930 |
| SI | hold_FALL→CK | -0.06964 | -0.07960 | -0.07463 |
| SI | hold_RISE→CK | -0.07461 | -0.07461 | -0.06965 |
| SI | setup_FALL→CK | 0.12936 | 0.12437 | 0.12935 |
| SI | setup_RISE→CK | 0.08954 | 0.08955 | 0.08955 |
| CK | minpwh | 0.06975 | 0.06971 | 0.07365 |
| CK | minpwl | 0.08559 | 0.09544 | 0.10033 |

SDXHS

Cell Description

Scan D Flip-Flop with Mux Inputs
 $Q = \text{rising_}(CK) ? (SE \& SI \mid !SE \& (DA \& SA \mid DB \& !SA)) : \text{pre_}Q$
 $QN = !Q$



Function Table

| CK<1> | CK | SA | DB | DA | SE | SI | Q |
|-------|----|----|----|----|----|----|------|
| 0 | 0 | X | X | X | X | X | Q<1> |
| 0 | 1 | 0 | 0 | X | 0 | X | 0 |
| 0 | 1 | 0 | 0 | X | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | X | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | X | 0 | X | 1 |
| 0 | 1 | 0 | 1 | X | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | X | 1 | 1 | 1 |
| 0 | 1 | 1 | X | 0 | 0 | X | 0 |
| 0 | 1 | 1 | X | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | X | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | X | 1 | 0 | X | 1 |
| 0 | 1 | 1 | X | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | X | 1 | 1 | 1 | 1 |
| 1 | X | X | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| SDXHSV1 | 1.80 | 7.80 |
| SDXHSV2 | 1.80 | 7.80 |
| SDXHSV4 | 1.80 | 8.20 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00286 | 0.00292 | 0.00294 |
| DA | 0.00154 | 0.00163 | 0.00163 |
| DB | 0.00141 | 0.00150 | 0.00150 |
| Q | 0.00179 | 0.00202 | 0.00288 |

| | | | |
|----|---------|---------|---------|
| QN | 0.00177 | 0.00199 | 0.00280 |
| SA | 0.00165 | 0.00169 | 0.00169 |
| SE | 0.00164 | 0.00170 | 0.00170 |
| SI | 0.00162 | 0.00167 | 0.00166 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00111 | 0.00110 | 0.00113 |
| DA | 0.00137 | 0.00158 | 0.00158 |
| DB | 0.00143 | 0.00165 | 0.00165 |
| SA | 0.00203 | 0.00202 | 0.00202 |
| SE | 0.00239 | 0.00236 | 0.00238 |
| SI | 0.00138 | 0.00137 | 0.00136 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00103320 | 0.00112150 | 0.00134400 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.09049 | 0.08962 | 0.09790 |
| CK→Q_RISE | 0.09651 | 0.09584 | 0.09908 |
| CK→QN_FALL | 0.13036 | 0.12379 | 0.13277 |
| CK→QN_RISE | 0.12857 | 0.12232 | 0.13857 |

Timing Constraints (ns)

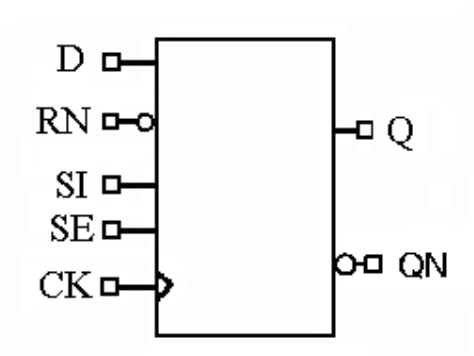
| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| DA | hold_FALL→CK | -0.09950 | -0.08954 | -0.08955 |
| DA | hold_RISE→CK | -0.05473 | -0.05472 | -0.04976 |
| DA | setup_FALL→CK | 0.12934 | 0.11939 | 0.11940 |
| DA | setup_RISE→CK | 0.11443 | 0.11939 | 0.12436 |
| DB | hold_FALL→CK | -0.09950 | -0.08956 | -0.08456 |
| DB | hold_RISE→CK | -0.05473 | -0.05471 | -0.04974 |
| DB | setup_FALL→CK | 0.12438 | 0.11443 | 0.11442 |
| DB | setup_RISE→CK | 0.11441 | 0.11939 | 0.12436 |
| SA | hold_FALL→CK | -0.08956 | -0.07960 | -0.07960 |
| SA | hold_RISE→CK | -0.04475 | -0.04476 | -0.03980 |
| SA | setup_FALL→CK | 0.11444 | 0.10945 | 0.10945 |
| SA | setup_RISE→CK | 0.10445 | 0.11440 | 0.11440 |
| SE | hold_FALL→CK | -0.01991 | -0.01991 | -0.01492 |
| SE | hold_RISE→CK | -0.05969 | -0.05970 | -0.05472 |
| SE | setup_FALL→CK | 0.08457 | 0.08956 | 0.09452 |
| SE | setup_RISE→CK | 0.08954 | 0.08954 | 0.09451 |

| | | | | |
|----|---------------|----------|----------|----------|
| SI | hold_FALL→CK | -0.07463 | -0.07462 | -0.07463 |
| SI | hold_RISE→CK | -0.05473 | -0.05472 | -0.04974 |
| SI | setup_FALL→CK | 0.10447 | 0.10945 | 0.10944 |
| SI | setup_RISE→CK | 0.12934 | 0.13929 | 0.13930 |
| CK | minpwh | 0.06185 | 0.06182 | 0.06182 |
| CK | minpwl | 0.11030 | 0.11527 | 0.12017 |

SDGRNHS

Cell Description

Scan D Flip-Flop with Sync Clear
Q = rising (CK) ? (SE&SI | !SE&(D&RN)) : pre_Q
QN = !Q



Function Table

| CK<1> | CK | D | SE | RN | SI | Q |
|-------|----|---|----|----|----|------|
| 0 | 0 | X | X | X | X | Q<1> |
| 0 | 1 | 0 | 0 | X | X | 0 |
| 0 | 1 | 0 | 1 | X | 0 | 0 |
| 0 | 1 | 0 | 1 | X | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | X | 0 |
| 0 | 1 | 1 | 0 | 1 | X | 1 |
| 0 | 1 | 1 | 1 | X | 0 | 0 |
| 0 | 1 | 1 | 1 | X | 1 | 1 |
| 1 | X | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| SDGRNHSV1 | 1.80 | 6.60 |
| SDGRNHSV2 | 1.80 | 6.60 |
| SDGRNHSV4 | 1.80 | 7.20 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00300 | 0.00311 | 0.00312 |
| D | 0.00070 | 0.00070 | 0.00072 |
| Q | 0.00145 | 0.00177 | 0.00260 |
| QN | 0.00147 | 0.00181 | 0.00274 |
| RN | 0.00073 | 0.00073 | 0.00075 |
| SE | 0.00210 | 0.00210 | 0.00214 |
| SI | 0.00133 | 0.00134 | 0.00137 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00134 | 0.00145 | 0.00151 |
| D | 0.00101 | 0.00101 | 0.00101 |
| RN | 0.00109 | 0.00109 | 0.00111 |
| SE | 0.00302 | 0.00302 | 0.00302 |
| SI | 0.00106 | 0.00105 | 0.00106 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00076423 | 0.00084999 | 0.00109100 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.12288 | 0.11914 | 0.13213 |
| CK→Q_RISE | 0.11482 | 0.11477 | 0.13532 |
| CK→QN_FALL | 0.08230 | 0.08290 | 0.09141 |
| CK→QN_RISE | 0.09231 | 0.08999 | 0.09391 |

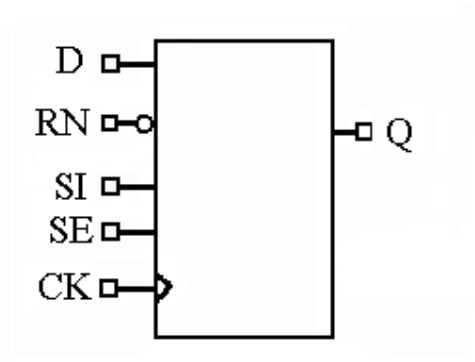
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.04478 | -0.04478 | -0.03979 |
| D | hold_RISE→CK | -0.05970 | -0.05970 | -0.06467 |
| D | setup_FALL→CK | 0.08955 | 0.08955 | 0.09453 |
| D | setup_RISE→CK | 0.08955 | 0.09453 | 0.09951 |
| RN | hold_FALL→CK | -0.08955 | -0.08456 | -0.07960 |
| RN | hold_RISE→CK | -0.06467 | -0.06467 | -0.06467 |
| RN | setup_FALL→CK | 0.15423 | 0.15422 | 0.15920 |
| RN | setup_RISE→CK | 0.09452 | 0.09453 | 0.10446 |
| SE | hold_FALL→CK | -0.06964 | -0.06964 | -0.06965 |
| SE | hold_RISE→CK | -0.05474 | -0.05474 | -0.05474 |
| SE | setup_FALL→CK | 0.09451 | 0.09950 | 0.10944 |
| SE | setup_RISE→CK | 0.10448 | 0.10946 | 0.11444 |
| SI | hold_FALL→CK | -0.05472 | -0.04975 | -0.04975 |
| SI | hold_RISE→CK | -0.05472 | -0.05472 | -0.05969 |
| SI | setup_FALL→CK | 0.10447 | 0.10447 | 0.10945 |
| SI | setup_RISE→CK | 0.08458 | 0.08456 | 0.08955 |
| CK | minpwh | 0.06575 | 0.06576 | 0.07762 |
| CK | minpwl | 0.07567 | 0.07068 | 0.07566 |

SDGRNQHS

Cell Description

Scan D Flip-Flop with Sync Clear
Q = rising (CK) ? (SE&SI | !SE&(D&RN)) : pre_Q



Function Table

| CK<1> | CK | D | SE | RN | SI | Q |
|-------|----|---|----|----|----|------|
| 0 | 0 | X | X | X | X | Q<1> |
| 0 | 1 | 0 | 0 | X | X | 0 |
| 0 | 1 | 0 | 1 | X | 0 | 0 |
| 0 | 1 | 0 | 1 | X | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | X | 0 |
| 0 | 1 | 1 | 0 | 1 | X | 1 |
| 0 | 1 | 1 | 1 | X | 0 | 0 |
| 0 | 1 | 1 | 1 | X | 1 | 1 |
| 1 | X | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| SDGRNQHSV1 | 1.80 | 6.20 |
| SDGRNQHSV2 | 1.80 | 6.20 |
| SDGRNQHSV4 | 1.80 | 6.60 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00315 | 0.00313 | 0.00309 |
| D | 0.00070 | 0.00071 | 0.00071 |
| Q | 0.00385 | 0.00420 | 0.00513 |
| RN | 0.00073 | 0.00073 | 0.00073 |
| SE | 0.00211 | 0.00211 | 0.00211 |
| SI | 0.00135 | 0.00136 | 0.00136 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00136 | 0.00144 | 0.00153 |
| D | 0.00098 | 0.00098 | 0.00099 |
| RN | 0.00107 | 0.00107 | 0.00108 |
| SE | 0.00301 | 0.00301 | 0.00300 |
| SI | 0.00106 | 0.00105 | 0.00106 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00070375 | 0.00074905 | 0.00088644 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.11415 | 0.11041 | 0.11448 |
| CK→Q_RISE | 0.10175 | 0.09813 | 0.10146 |

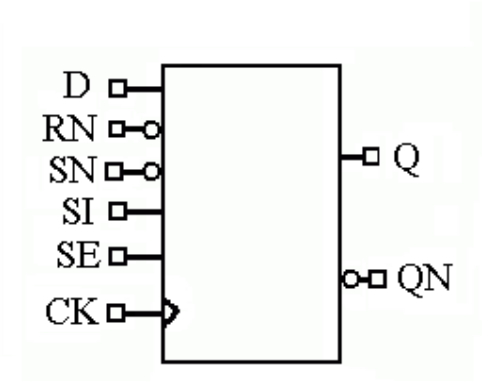
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.05473 | -0.04975 | -0.04478 |
| D | hold_RISE→CK | -0.06964 | -0.06964 | -0.06964 |
| D | setup_FALL→CK | 0.09453 | 0.09453 | 0.09949 |
| D | setup_RISE→CK | 0.08955 | 0.09452 | 0.10448 |
| RN | hold_FALL→CK | -0.09949 | -0.09453 | -0.07959 |
| RN | hold_RISE→CK | -0.06964 | -0.06964 | -0.06964 |
| RN | setup_FALL→CK | 0.15422 | 0.15422 | 0.15920 |
| RN | setup_RISE→CK | 0.09452 | 0.09949 | 0.10447 |
| SE | hold_FALL→CK | -0.07462 | -0.07463 | -0.07462 |
| SE | hold_RISE→CK | -0.06468 | -0.05970 | -0.05473 |
| SE | setup_FALL→CK | 0.09949 | 0.10447 | 0.10944 |
| SE | setup_RISE→CK | 0.10447 | 0.10946 | 0.10946 |
| SI | hold_FALL→CK | -0.05970 | -0.05970 | -0.04975 |
| SI | hold_RISE→CK | -0.05969 | -0.05969 | -0.05970 |
| SI | setup_FALL→CK | 0.10448 | 0.10945 | 0.10946 |
| SI | setup_RISE→CK | 0.07960 | 0.08456 | 0.08955 |
| CK | minpwh | 0.05788 | 0.05789 | 0.05786 |
| CK | minpwl | 0.08062 | 0.07563 | 0.07564 |

SDGRSNHS

Cell Description

Scan D Flip-Flop with Sync Clear and Set
Q = rising (CK) ? (SE ? SI : (!RN ? 0 : !SN ? 1 : D)) : pre_Q
QN = !Q



Function Table

| CK<1> | CK | RN | SE | SN | D | SI | Q |
|-------|----|----|----|----|---|----|------|
| 0 | 0 | X | X | X | X | X | Q<1> |
| 0 | 1 | 0 | 0 | X | X | X | 0 |
| 0 | 1 | 0 | 1 | X | X | 0 | 0 |
| 0 | 1 | 0 | 1 | X | X | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | X | X | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | X | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | X | 1 |
| 0 | 1 | 1 | 1 | X | X | 0 | 0 |
| 0 | 1 | 1 | 1 | X | X | 1 | 1 |
| 1 | X | X | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| SDGRSNHSV1 | 1.80 | 7.60 |
| SDGRSNHSV2 | 1.80 | 7.80 |
| SDGRSNHSV4 | 1.80 | 9.20 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00294 | 0.00300 | 0.00265 |
| D | 0.00048 | 0.00049 | 0.00053 |
| Q | 0.00166 | 0.00193 | 0.00302 |
| QN | 0.00169 | 0.00194 | 0.00313 |
| RN | 0.00142 | 0.00143 | 0.00156 |
| SE | 0.00233 | 0.00238 | 0.00258 |
| SI | 0.00139 | 0.00139 | 0.00165 |
| SN | 0.00130 | 0.00132 | 0.00136 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00117 | 0.00107 | 0.00102 |
| D | 0.00105 | 0.00104 | 0.00111 |
| RN | 0.00134 | 0.00131 | 0.00125 |
| SE | 0.00237 | 0.00236 | 0.00231 |
| SI | 0.00104 | 0.00101 | 0.00106 |
| SN | 0.00180 | 0.00169 | 0.00171 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00086916 | 0.00091236 | 0.00116650 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.16214 | 0.15896 | 0.15297 |
| CK→Q_RISE | 0.13074 | 0.13809 | 0.15650 |
| CK→QN_FALL | 0.09624 | 0.10215 | 0.11193 |
| CK→QN_RISE | 0.12890 | 0.12818 | 0.11513 |

Timing Constraints (ns)

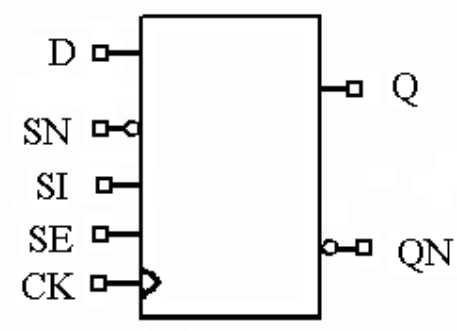
| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.11443 | -0.10945 | -0.12438 |
| D | hold_RISE→CK | -0.08457 | -0.08456 | -0.10448 |
| D | setup_FALL→CK | 0.12438 | 0.12436 | 0.14426 |
| D | setup_RISE→CK | 0.11940 | 0.12935 | 0.15424 |
| RN | hold_FALL→CK | -0.09452 | -0.09453 | -0.10945 |
| RN | hold_RISE→CK | -0.06965 | -0.06467 | -0.08457 |
| RN | setup_FALL→CK | 0.10446 | 0.10945 | 0.12935 |
| RN | setup_RISE→CK | 0.10447 | 0.10945 | 0.13433 |
| SE | hold_FALL→CK | -0.06963 | -0.06964 | -0.07961 |
| SE | hold_RISE→CK | -0.08955 | -0.08954 | -0.10448 |
| SE | setup_FALL→CK | 0.10446 | 0.11440 | 0.12934 |
| SE | setup_RISE→CK | 0.09950 | 0.09949 | 0.11941 |
| SI | hold_FALL→CK | -0.07960 | -0.07960 | -0.09454 |
| SI | hold_RISE→CK | -0.03483 | -0.03483 | -0.04974 |
| SI | setup_FALL→CK | 0.08955 | 0.08954 | 0.10945 |
| SI | setup_RISE→CK | 0.06965 | 0.07960 | 0.09951 |
| SN | hold_FALL→CK | -0.08458 | -0.08457 | -0.09951 |
| SN | hold_RISE→CK | -0.12437 | -0.12438 | -0.13931 |
| SN | setup_FALL→CK | 0.12438 | 0.12935 | 0.14926 |
| SN | setup_RISE→CK | 0.13432 | 0.13432 | 0.15421 |
| CK | minpwh | 0.07759 | 0.08555 | 0.09739 |

| | | | | |
|----|--------|---------|---------|---------|
| CK | minpwl | 0.08060 | 0.09540 | 0.08552 |
|----|--------|---------|---------|---------|

SDGSNHS

Cell Description

Scan D Flip-Flop with Sync Set
Q = rising (CK) ? (SE ? SI : (!SN ? 1 : D)) : pre_Q
QN = !Q



Function Table

| CK<1> | CK | SN | D | SE | SI | Q |
|-------|----|----|---|----|----|------|
| 0 | 0 | X | X | X | X | Q<1> |
| 0 | 1 | 0 | X | 0 | X | 1 |
| 0 | 1 | 0 | X | 1 | 0 | 0 |
| 0 | 1 | 0 | X | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | X | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | X | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | X | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| SDGSNHSV1 | 1.80 | 6.40 |
| SDGSNHSV2 | 1.80 | 6.80 |
| SDGSNHSV4 | 1.80 | 7.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00269 | 0.00322 | 0.00341 |
| D | 0.00062 | 0.00076 | 0.00086 |
| Q | 0.00152 | 0.00187 | 0.00273 |
| QN | 0.00155 | 0.00185 | 0.00273 |
| SE | 0.00184 | 0.00213 | 0.00229 |
| SI | 0.00110 | 0.00131 | 0.00144 |
| SN | 0.00136 | 0.00158 | 0.00171 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00115 | 0.00138 | 0.00142 |
| D | 0.00081 | 0.00102 | 0.00109 |
| SE | 0.00167 | 0.00179 | 0.00183 |
| SI | 0.00089 | 0.00087 | 0.00084 |
| SN | 0.00113 | 0.00111 | 0.00112 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00070460 | 0.00086771 | 0.00113560 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.13932 | 0.12560 | 0.13410 |
| CK→Q_RISE | 0.13712 | 0.12453 | 0.13895 |
| CK→QN_FALL | 0.10006 | 0.08940 | 0.09655 |
| CK→QN_RISE | 0.10550 | 0.09433 | 0.09686 |

Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.08457 | -0.06964 | -0.05970 |
| D | hold_RISE→CK | -0.05970 | -0.04974 | -0.04477 |
| D | setup_FALL→CK | 0.14426 | 0.13431 | 0.12935 |
| D | setup_RISE→CK | 0.08458 | 0.07960 | 0.07960 |
| SE | hold_FALL→CK | -0.08458 | -0.08458 | -0.07463 |
| SE | hold_RISE→CK | -0.06468 | -0.08459 | -0.06965 |
| SE | setup_FALL→CK | 0.11442 | 0.12438 | 0.11941 |
| SE | setup_RISE→CK | 0.12437 | 0.14925 | 0.15920 |
| SI | hold_FALL→CK | -0.05472 | -0.06965 | -0.05969 |
| SI | hold_RISE→CK | -0.06467 | -0.07462 | -0.06965 |
| SI | setup_FALL→CK | 0.10945 | 0.13432 | 0.13930 |
| SI | setup_RISE→CK | 0.09452 | 0.11442 | 0.12437 |
| SN | hold_FALL→CK | -0.09452 | -0.10447 | -0.09453 |
| SN | hold_RISE→CK | -0.10448 | -0.09453 | -0.07960 |
| SN | setup_FALL→CK | 0.12436 | 0.13930 | 0.13929 |
| SN | setup_RISE→CK | 0.16914 | 0.15919 | 0.15423 |
| CK | minpwh | 0.07769 | 0.06974 | 0.08160 |
| CK | minpwl | 0.08554 | 0.08060 | 0.08063 |

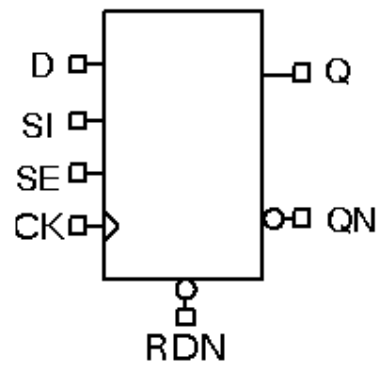
SDRNHS

Cell Description

Scan D Flip-Flop with Async Clear

$Q = \text{!RDN} ? 0 : \text{rising (CK)} ? (\text{SE\&SI} \mid \text{!SE\&D}) : \text{pre_Q}$

$QN = \text{!Q}$



Function Table

| RDN | CK<1> | CK | SE | SI | D | Q |
|-----|-------|----|----|----|---|------|
| 0 | X | X | X | X | X | 0 |
| 1 | 0 | 0 | X | X | X | Q<1> |
| 1 | 0 | 1 | 0 | X | 0 | 0 |
| 1 | 0 | 1 | 0 | X | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | X | 0 |
| 1 | 0 | 1 | 1 | 1 | X | 1 |
| 1 | 1 | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| SDRNHSV1 | 1.80 | 6.40 |
| SDRNHSV2 | 1.80 | 6.40 |
| SDRNHSV4 | 1.80 | 7.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00288 | 0.00291 | 0.00368 |
| D | 0.00063 | 0.00067 | 0.00082 |
| Q | 0.00169 | 0.00207 | 0.00295 |
| QN | 0.00180 | 0.00218 | 0.00311 |
| RDN | 0.00095 | 0.00102 | 0.00120 |
| SE | 0.00139 | 0.00143 | 0.00170 |
| SI | 0.00065 | 0.00068 | 0.00083 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|----|----|----|
|-----|----|----|----|

| | | | |
|-----|---------|---------|---------|
| CK | 0.00111 | 0.00111 | 0.00135 |
| D | 0.00089 | 0.00091 | 0.00107 |
| RDN | 0.00286 | 0.00296 | 0.00392 |
| SE | 0.00212 | 0.00214 | 0.00232 |
| SI | 0.00087 | 0.00090 | 0.00107 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00078065 | 0.00089467 | 0.00135520 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.15076 | 0.14593 | 0.14735 |
| CK→Q_RISE | 0.14461 | 0.13906 | 0.14537 |
| RDN→Q_FALL | 0.05185 | 0.05544 | 0.07116 |
| CK→QN_FALL | 0.09691 | 0.09554 | 0.10329 |
| CK→QN_RISE | 0.11047 | 0.10960 | 0.09969 |
| RDN→QN_RISE | 0.11371 | 0.11973 | 0.14506 |

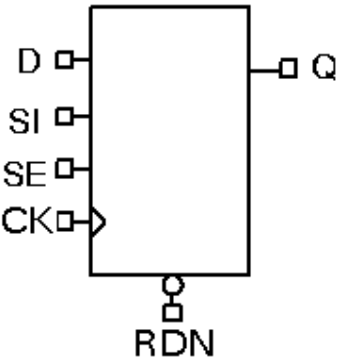
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.03980 | -0.03483 | -0.03482 |
| D | hold_RISE→CK | -0.06965 | -0.06468 | -0.05471 |
| D | setup_FALL→CK | 0.09949 | 0.09950 | 0.09950 |
| D | setup_RISE→CK | 0.09949 | 0.10447 | 0.09452 |
| RDN | setup_RISE→CK | 0.10943 | 0.10943 | 0.10448 |
| RDN | hold_RISE→CK | -0.08953 | -0.08954 | -0.08458 |
| SE | hold_FALL→CK | -0.08957 | -0.08458 | -0.07960 |
| SE | hold_RISE→CK | -0.05970 | -0.05472 | -0.05471 |
| SE | setup_FALL→CK | 0.11941 | 0.12438 | 0.11939 |
| SE | setup_RISE→CK | 0.11443 | 0.11939 | 0.11939 |
| SI | hold_FALL→CK | -0.04477 | -0.03980 | -0.03979 |
| SI | hold_RISE→CK | -0.06966 | -0.06468 | -0.05472 |
| SI | setup_FALL→CK | 0.09950 | 0.10448 | 0.10447 |
| SI | setup_RISE→CK | 0.10447 | 0.10447 | 0.09949 |
| CK | minpwh | 0.08161 | 0.07766 | 0.08558 |
| CK | minpwl | 0.09045 | 0.09049 | 0.08552 |
| RDN | minpwl | 0.06971 | 0.07764 | 0.11323 |

SDRNQHS

Cell Description

Scan D Flip-Flop with Async Clear
 $Q = \text{!RDN} ? 0 : \text{rising}(\text{CK}) ? (\text{SE} \& \text{SI} \mid \text{!SE} \& \text{D}) : \text{pre_Q}$



Function Table

| RDN | CK<1> | CK | SE | D | SI | Q |
|-----|-------|----|----|---|----|------|
| 0 | X | X | X | X | X | 0 |
| 1 | 0 | 0 | X | X | X | Q<1> |
| 1 | 0 | 1 | 0 | 0 | X | 0 |
| 1 | 0 | 1 | 0 | 1 | X | 1 |
| 1 | 0 | 1 | 1 | X | 0 | 0 |
| 1 | 0 | 1 | 1 | X | 1 | 1 |
| 1 | 1 | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| SDRNQHVS1 | 1.80 | 6.00 |
| SDRNQHVS2 | 1.80 | 6.00 |
| SDRNQHVS4 | 1.80 | 7.20 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00284 | 0.00290 | 0.00361 |
| D | 0.00063 | 0.00067 | 0.00083 |
| Q | 0.00417 | 0.00472 | 0.00607 |
| RDN | 0.00095 | 0.00101 | 0.00121 |
| SE | 0.00138 | 0.00143 | 0.00171 |
| SI | 0.00064 | 0.00068 | 0.00084 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00110 | 0.00109 | 0.00133 |

| | | | |
|-----|---------|---------|---------|
| D | 0.00089 | 0.00090 | 0.00107 |
| RDN | 0.00284 | 0.00297 | 0.00386 |
| SE | 0.00211 | 0.00213 | 0.00229 |
| SI | 0.00087 | 0.00089 | 0.00107 |

Max Leakage Power (uW)

| | | |
|------------|------------|------------|
| V1 | V2 | V4 |
| 0.00072110 | 0.00078403 | 0.00107910 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.14012 | 0.13613 | 0.12587 |
| CK→Q_RISE | 0.12658 | 0.12075 | 0.11464 |
| RDN→Q_FALL | 0.05022 | 0.05431 | 0.06871 |

Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.04975 | -0.04477 | -0.04477 |
| D | hold_RISE→CK | -0.06965 | -0.06468 | -0.05970 |
| D | setup_FALL→CK | 0.09452 | 0.09950 | 0.09950 |
| D | setup_RISE→CK | 0.09453 | 0.09452 | 0.09452 |
| RDN | setup_RISE→CK | 0.10446 | 0.10447 | 0.10446 |
| RDN | hold_RISE→CK | -0.08953 | -0.08457 | -0.08456 |
| SE | hold_FALL→CK | -0.08955 | -0.08459 | -0.08459 |
| SE | hold_RISE→CK | -0.06467 | -0.05969 | -0.06468 |
| SE | setup_FALL→CK | 0.11442 | 0.11941 | 0.11941 |
| SE | setup_RISE→CK | 0.11442 | 0.11443 | 0.11940 |
| SI | hold_FALL→CK | -0.04975 | -0.04477 | -0.04477 |
| SI | hold_RISE→CK | -0.06965 | -0.06468 | -0.05970 |
| SI | setup_FALL→CK | 0.09950 | 0.09949 | 0.09950 |
| SI | setup_RISE→CK | 0.09950 | 0.09950 | 0.09451 |
| CK | minpwh | 0.06976 | 0.06975 | 0.06976 |
| CK | minpwl | 0.09049 | 0.09046 | 0.08056 |
| RDN | minpwl | 0.06182 | 0.06973 | 0.09342 |

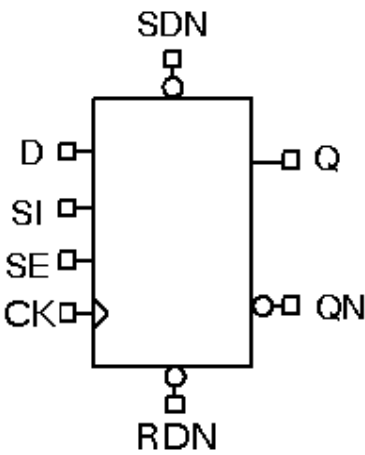
SDRSNHS

Cell Description

Scan D Flip-Flop with Async Clear and Set

$Q = !SDN ? 1 : !RDN ? 0 : \text{rising}(CK) ? (SE \& SI \mid !SE \& D) : \text{pre_}Q$

$QN = !Q$



Function Table

| RDN | SDN | CK<1> | CK | SE | D | SI | Q |
|-----|-----|-------|----|----|---|----|------|
| 0 | 0 | X | X | X | X | X | 1 |
| 0 | 1 | X | X | X | X | X | 0 |
| 1 | 0 | X | X | X | X | X | 1 |
| 1 | 1 | 0 | 0 | X | X | X | Q<1> |
| 1 | 1 | 0 | 1 | 0 | 0 | X | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | X | 1 |
| 1 | 1 | 0 | 1 | 1 | X | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | X | 1 | 1 |
| 1 | 1 | 1 | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| SDRSNHSV1 | 1.80 | 7.80 |
| SDRSNHSV2 | 1.80 | 7.80 |
| SDRSNHSV4 | 1.80 | 8.60 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00327 | 0.00334 | 0.00403 |
| D | 0.00090 | 0.00092 | 0.00120 |
| Q | 0.00238 | 0.00277 | 0.00374 |
| QN | 0.00241 | 0.00281 | 0.00387 |
| RDN | 0.00109 | 0.00119 | 0.00120 |
| SDN | 0.00045 | 0.00048 | 0.00049 |
| SE | 0.00150 | 0.00149 | 0.00186 |
| SI | 0.00088 | 0.00089 | 0.00118 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00108 | 0.00108 | 0.00133 |
| D | 0.00124 | 0.00123 | 0.00153 |
| RDN | 0.00103 | 0.00103 | 0.00103 |
| SDN | 0.00178 | 0.00186 | 0.00176 |
| SE | 0.00179 | 0.00171 | 0.00199 |
| SI | 0.00099 | 0.00095 | 0.00122 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00088235 | 0.00095999 | 0.00135510 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.17330 | 0.17043 | 0.17312 |
| CK→Q_RISE | 0.15635 | 0.15490 | 0.17486 |
| RDN→Q_FALL | 0.15293 | 0.14236 | 0.16337 |
| SDN→Q_FALL | 0.14518 | 0.13086 | 0.15330 |
| SDN→Q_RISE | 0.09315 | 0.09473 | 0.10902 |
| CK→QN_FALL | 0.11766 | 0.11847 | 0.12309 |
| CK→QN_RISE | 0.13508 | 0.13418 | 0.12634 |
| RDN→QN_RISE | 0.11441 | 0.10645 | 0.11849 |
| SDN→QN_FALL | 0.06144 | 0.06423 | 0.06875 |
| SDN→QN_RISE | 0.10661 | 0.09486 | 0.10844 |

Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|------------------------|----------|----------|----------|
| D | hold_FALL→CK | -0.03483 | -0.03979 | -0.03979 |
| D | hold_RISE→CK | -0.05473 | -0.06468 | -0.04478 |
| D | setup_FALL→CK | 0.10945 | 0.11441 | 0.10946 |
| D | setup_RISE→CK | 0.10448 | 0.11444 | 0.09453 |
| RDN | setup_RISE→CK | 0.05970 | 0.05473 | 0.05969 |
| RDN | hold_RISE→CK | -0.02488 | -0.01991 | -0.02487 |
| SDN | setup_RISE→CK | -0.01990 | -0.02986 | -0.00994 |
| SDN | hold_RISE→CK | 0.03981 | 0.04976 | 0.03483 |
| SDN | non_seq_hold_RISE→RDN | -0.08954 | -0.07462 | -0.09451 |
| SDN | non_seq_setup_RISE→RDN | 0.10446 | 0.09453 | 0.11940 |
| SE | hold_FALL→CK | -0.07463 | -0.08456 | -0.06467 |
| SE | hold_RISE→CK | -0.05473 | -0.05471 | -0.05473 |
| SE | setup_FALL→CK | 0.12436 | 0.13433 | 0.11939 |
| SE | setup_RISE→CK | 0.12439 | 0.12934 | 0.12936 |
| SI | hold_FALL→CK | -0.03482 | -0.03979 | -0.03980 |

| | | | | |
|-----|---------------|----------|----------|----------|
| SI | hold_RISE→CK | -0.05472 | -0.06468 | -0.04477 |
| SI | setup_FALL→CK | 0.10446 | 0.11442 | 0.10945 |
| SI | setup_RISE→CK | 0.10447 | 0.11441 | 0.09453 |
| CK | minpwh | 0.09345 | 0.09741 | 0.11322 |
| CK | minpwl | 0.09543 | 0.10039 | 0.08555 |
| RDN | minpwl | 0.08555 | 0.07763 | 0.09343 |
| SDN | minpwl | 0.06183 | 0.06577 | 0.07760 |

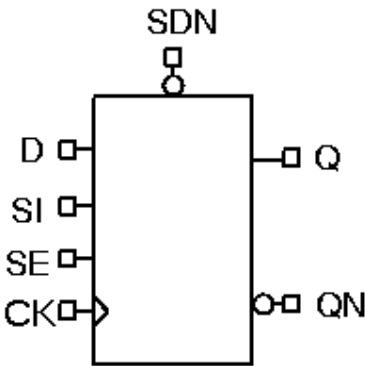
SDSNHS

Cell Description

Scan D Flip-Flop with Async Set

$Q = \neg SDN \text{ ? } 1 \text{ : rising (CK) ? (SE \& SI \mid \neg SE \& D) : pre_Q}$

$QN = \neg Q$



Function Table

| SDN | CK<1> | CK | SE | SI | D | Q |
|-----|-------|----|----|----|---|------|
| 0 | X | X | X | X | X | 1 |
| 1 | 0 | 0 | X | X | X | Q<1> |
| 1 | 0 | 1 | 0 | X | 0 | 0 |
| 1 | 0 | 1 | 0 | X | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | X | 0 |
| 1 | 0 | 1 | 1 | 1 | X | 1 |
| 1 | 1 | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| SDSNHSV1 | 1.80 | 6.80 |
| SDSNHSV2 | 1.80 | 6.80 |
| SDSNHSV4 | 1.80 | 7.40 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00309 | 0.00319 | 0.00323 |
| D | 0.00080 | 0.00084 | 0.00085 |
| Q | 0.00215 | 0.00259 | 0.00344 |
| QN | 0.00214 | 0.00254 | 0.00341 |
| SDN | 0.00039 | 0.00043 | 0.00042 |
| SE | 0.00136 | 0.00144 | 0.00144 |
| SI | 0.00074 | 0.00078 | 0.00079 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|----|----|----|
|-----|----|----|----|

| | | | |
|-----|---------|---------|---------|
| CK | 0.00108 | 0.00109 | 0.00110 |
| D | 0.00133 | 0.00135 | 0.00135 |
| SDN | 0.00169 | 0.00173 | 0.00173 |
| SE | 0.00187 | 0.00188 | 0.00183 |
| SI | 0.00092 | 0.00093 | 0.00090 |

Max Leakage Power (uW)

| | | |
|------------|------------|------------|
| V1 | V2 | V4 |
| 0.00076019 | 0.00090117 | 0.00112600 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.15224 | 0.14826 | 0.16230 |
| CK→Q_RISE | 0.14889 | 0.14446 | 0.15757 |
| SDN→Q_RISE | 0.09772 | 0.09725 | 0.10899 |
| CK→QN_FALL | 0.10481 | 0.10632 | 0.11192 |
| CK→QN_RISE | 0.11607 | 0.11648 | 0.12380 |
| SDN→QN_FALL | 0.05711 | 0.06197 | 0.06681 |

Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.01491 | -0.01492 | -0.00994 |
| D | hold_RISE→CK | -0.05971 | -0.05970 | -0.05473 |
| D | setup_FALL→CK | 0.08955 | 0.09949 | 0.10447 |
| D | setup_RISE→CK | 0.08456 | 0.09454 | 0.09451 |
| SDN | setup_RISE→CK | -0.03482 | -0.02986 | -0.02488 |
| SDN | hold_RISE→CK | 0.04974 | 0.04976 | 0.04974 |
| SE | hold_FALL→CK | -0.07464 | -0.07462 | -0.07464 |
| SE | hold_RISE→CK | -0.04974 | -0.04975 | -0.03980 |
| SE | setup_FALL→CK | 0.09950 | 0.10945 | 0.11442 |
| SE | setup_RISE→CK | 0.13431 | 0.14925 | 0.15424 |
| SI | hold_FALL→CK | -0.03483 | -0.03483 | -0.02488 |
| SI | hold_RISE→CK | -0.07462 | -0.07461 | -0.07462 |
| SI | setup_FALL→CK | 0.11940 | 0.13434 | 0.13930 |
| SI | setup_RISE→CK | 0.10447 | 0.11443 | 0.11939 |
| CK | minpwh | 0.08558 | 0.08556 | 0.09343 |
| CK | minpwl | 0.10531 | 0.11030 | 0.11025 |
| SDN | minpwl | 0.06179 | 0.06580 | 0.07764 |

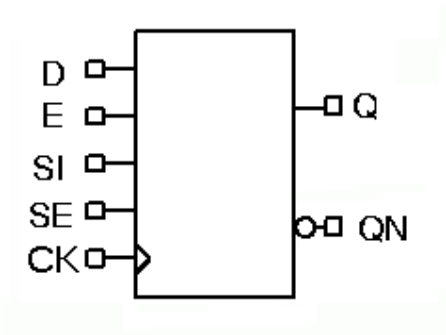
SEDHS

Cell Description

Scan Enable D Flip-Flop

Q = rising (CK) ? (SE ? SI : (E ? D : pre_Q)) : pre_Q

QN = !Q



Function Table

| CK<1> | CK | E | Q | D | SE | SI | Q |
|-------|----|---|---|---|----|----|------|
| 0 | 0 | X | X | X | X | X | Q<1> |
| 0 | 1 | 0 | 0 | X | 0 | X | 0 |
| 0 | 1 | 0 | 0 | X | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | X | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | X | 0 | X | 1 |
| 0 | 1 | 0 | 1 | X | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | X | 1 | 1 | 1 |
| 0 | 1 | 1 | X | 0 | 0 | X | 0 |
| 0 | 1 | 1 | X | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | X | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | X | 1 | 0 | X | 1 |
| 0 | 1 | 1 | X | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | X | 1 | 1 | 1 | 1 |
| 1 | X | X | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| SEDHSV1 | 1.80 | 8.00 |
| SEDHSV2 | 1.80 | 8.20 |
| SEDHSV4 | 1.80 | 8.60 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00322 | 0.00325 | 0.00326 |
| D | 0.00051 | 0.00053 | 0.00053 |
| E | 0.00074 | 0.00075 | 0.00076 |
| Q | 0.00254 | 0.00299 | 0.00388 |

| | | | |
|----|---------|---------|---------|
| QN | 0.00254 | 0.00300 | 0.00384 |
| SE | 0.00168 | 0.00171 | 0.00171 |
| SI | 0.00115 | 0.00119 | 0.00119 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00107 | 0.00109 | 0.00105 |
| D | 0.00102 | 0.00106 | 0.00105 |
| E | 0.00241 | 0.00245 | 0.00251 |
| SE | 0.00207 | 0.00212 | 0.00210 |
| SI | 0.00082 | 0.00083 | 0.00084 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00069124 | 0.00076647 | 0.00097964 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.12469 | 0.12251 | 0.13210 |
| CK→Q_RISE | 0.13262 | 0.12897 | 0.13640 |
| CK→QN_FALL | 0.18253 | 0.18104 | 0.19141 |
| CK→QN_RISE | 0.17698 | 0.18193 | 0.19101 |

Timing Constraints (ns)

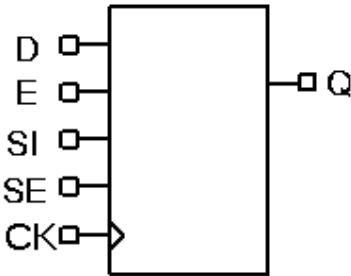
| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.07959 | -0.06964 | -0.06964 |
| D | hold_RISE→CK | -0.05970 | -0.06468 | -0.06467 |
| D | setup_FALL→CK | 0.12437 | 0.11939 | 0.12438 |
| D | setup_RISE→CK | 0.06965 | 0.07960 | 0.07960 |
| E | hold_FALL→CK | -0.08955 | -0.09452 | -0.08956 |
| E | hold_RISE→CK | -0.11442 | -0.10446 | -0.10447 |
| E | setup_FALL→CK | 0.09453 | 0.09950 | 0.09950 |
| E | setup_RISE→CK | 0.14924 | 0.14428 | 0.14925 |
| SE | hold_FALL→CK | -0.09452 | -0.09950 | -0.09949 |
| SE | hold_RISE→CK | -0.11941 | -0.12438 | -0.11939 |
| SE | setup_FALL→CK | 0.10446 | 0.10944 | 0.10944 |
| SE | setup_RISE→CK | 0.17910 | 0.18905 | 0.19401 |
| SI | hold_FALL→CK | -0.10448 | -0.10945 | -0.10945 |
| SI | hold_RISE→CK | -0.10447 | -0.10447 | -0.10447 |
| SI | setup_FALL→CK | 0.16419 | 0.17413 | 0.17910 |
| SI | setup_RISE→CK | 0.11939 | 0.12436 | 0.12437 |
| CK | minpwh | 0.08157 | 0.07762 | 0.08552 |
| CK | minpwl | 0.10531 | 0.11026 | 0.11025 |

SEDQHS

Cell Description

Scan Enable D Flip-Flop

Q = rising (CK) ? (SE ? SI : (E ? D : pre_Q)) : pre_Q



Function Table

| CK<1> | CK | E | Q | D | SE | SI | Q |
|-------|----|---|---|---|----|----|------|
| 0 | 0 | X | X | X | X | X | Q<1> |
| 0 | 1 | 0 | 0 | X | 0 | X | 0 |
| 0 | 1 | 0 | 0 | X | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | X | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | X | 0 | X | 1 |
| 0 | 1 | 0 | 1 | X | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | X | 1 | 1 | 1 |
| 0 | 1 | 1 | X | 0 | 0 | X | 0 |
| 0 | 1 | 1 | X | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | X | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | X | 1 | 0 | X | 1 |
| 0 | 1 | 1 | X | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | X | 1 | 1 | 1 | 1 |
| 1 | X | X | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| SEDQHSV1 | 1.80 | 7.60 |
| SEDQHSV2 | 1.80 | 7.60 |
| SEDQHSV4 | 1.80 | 8.00 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00317 | 0.00323 | 0.00326 |
| D | 0.00051 | 0.00052 | 0.00052 |
| E | 0.00075 | 0.00075 | 0.00075 |
| Q | 0.00516 | 0.00553 | 0.00671 |

| | | | |
|----|---------|---------|---------|
| SE | 0.00169 | 0.00171 | 0.00171 |
| SI | 0.00117 | 0.00119 | 0.00119 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00104 | 0.00105 | 0.00109 |
| D | 0.00105 | 0.00105 | 0.00105 |
| E | 0.00248 | 0.00248 | 0.00249 |
| SE | 0.00213 | 0.00212 | 0.00210 |
| SI | 0.00084 | 0.00085 | 0.00083 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00063533 | 0.00065259 | 0.00073486 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.12077 | 0.11363 | 0.13229 |
| CK→Q_RISE | 0.12922 | 0.12394 | 0.13474 |

Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.07462 | -0.06965 | -0.06964 |
| D | hold_RISE→CK | -0.06467 | -0.06466 | -0.06468 |
| D | setup_FALL→CK | 0.11442 | 0.12437 | 0.12437 |
| D | setup_RISE→CK | 0.07959 | 0.07959 | 0.07960 |
| E | hold_FALL→CK | -0.09453 | -0.09453 | -0.08955 |
| E | hold_RISE→CK | -0.10447 | -0.10447 | -0.10447 |
| E | setup_FALL→CK | 0.09949 | 0.09949 | 0.09950 |
| E | setup_RISE→CK | 0.13930 | 0.14428 | 0.14925 |
| SE | hold_FALL→CK | -0.09949 | -0.09949 | -0.09951 |
| SE | hold_RISE→CK | -0.12437 | -0.12437 | -0.11940 |
| SE | setup_FALL→CK | 0.10945 | 0.10946 | 0.10944 |
| SE | setup_RISE→CK | 0.17909 | 0.18905 | 0.19403 |
| SI | hold_FALL→CK | -0.10945 | -0.10945 | -0.10447 |
| SI | hold_RISE→CK | -0.10447 | -0.10447 | -0.10447 |
| SI | setup_FALL→CK | 0.16915 | 0.17911 | 0.17910 |
| SI | setup_RISE→CK | 0.12437 | 0.12436 | 0.12438 |
| CK | minpwh | 0.07764 | 0.07761 | 0.08156 |
| CK | minpwl | 0.10534 | 0.11022 | 0.11028 |

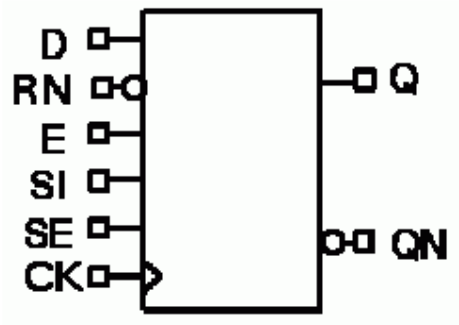
SEDGRNHS

Cell Description

Scan Enable D Flip-Flop with Sync Clear

$Q = \text{rising}(\text{CK}) ? (\text{SE} ? \text{SI} : (!\text{RN} ? 0 : \text{E} ? \text{D} : \text{pre_Q})) : \text{pre_Q}$

$\text{QN} = !Q$



Function Table

| CK<1> | CK | SE | RN | E | Q | D | SI | Q |
|-------|----|----|----|---|---|---|----|------|
| 0 | 0 | X | X | X | X | X | X | Q<1> |
| 0 | 1 | 0 | 0 | X | X | X | X | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | X | X | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | X | X | 1 |
| 0 | 1 | 0 | 1 | 1 | X | 0 | X | 0 |
| 0 | 1 | 0 | 1 | 1 | X | 1 | X | 1 |
| 0 | 1 | 1 | X | X | X | X | 0 | 0 |
| 0 | 1 | 1 | X | X | X | X | 1 | 1 |
| 1 | X | X | X | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| SEDGRNHSV1 | 1.80 | 8.20 |
| SEDGRNHSV2 | 1.80 | 8.20 |
| SEDGRNHSV4 | 1.80 | 8.60 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00292 | 0.00292 | 0.00301 |
| D | 0.00053 | 0.00053 | 0.00053 |
| E | 0.00106 | 0.00106 | 0.00105 |
| Q | 0.00188 | 0.00213 | 0.00294 |
| QN | 0.00192 | 0.00218 | 0.00310 |
| RN | 0.00089 | 0.00089 | 0.00090 |
| SE | 0.00264 | 0.00263 | 0.00262 |
| SI | 0.00152 | 0.00151 | 0.00151 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00110 | 0.00110 | 0.00110 |
| D | 0.00103 | 0.00103 | 0.00103 |
| E | 0.00254 | 0.00255 | 0.00254 |
| RN | 0.00099 | 0.00099 | 0.00099 |
| SE | 0.00320 | 0.00321 | 0.00321 |
| SI | 0.00087 | 0.00088 | 0.00088 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00078310 | 0.00084485 | 0.00107890 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.14559 | 0.14880 | 0.15740 |
| CK→Q_RISE | 0.14337 | 0.14711 | 0.16063 |
| CK→QN_FALL | 0.10991 | 0.10990 | 0.11647 |
| CK→QN_RISE | 0.11450 | 0.11446 | 0.11376 |

Timing Constraints (ns)

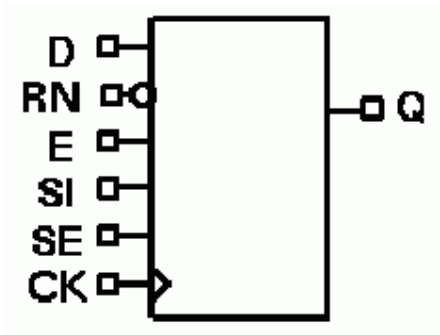
| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.11443 | -0.10945 | -0.10447 |
| D | hold_RISE→CK | -0.10446 | -0.10446 | -0.09950 |
| D | setup_FALL→CK | 0.19403 | 0.19403 | 0.19403 |
| D | setup_RISE→CK | 0.14924 | 0.15421 | 0.15422 |
| E | hold_FALL→CK | -0.11442 | -0.10447 | -0.10447 |
| E | hold_RISE→CK | -0.12934 | -0.12935 | -0.12934 |
| E | setup_FALL→CK | 0.14925 | 0.14925 | 0.14428 |
| E | setup_RISE→CK | 0.14924 | 0.15422 | 0.15422 |
| RN | hold_FALL→CK | -0.18408 | -0.17412 | -0.16915 |
| RN | hold_RISE→CK | -0.12438 | -0.12437 | -0.11941 |
| RN | setup_FALL→CK | 0.28357 | 0.28357 | 0.28359 |
| RN | setup_RISE→CK | 0.15920 | 0.16418 | 0.16418 |
| SE | hold_FALL→CK | -0.12438 | -0.12438 | -0.11941 |
| SE | hold_RISE→CK | -0.11941 | -0.11443 | -0.10945 |
| SE | setup_FALL→CK | 0.15424 | 0.15920 | 0.15920 |
| SE | setup_RISE→CK | 0.17413 | 0.17911 | 0.17911 |
| SI | hold_FALL→CK | -0.08458 | -0.07961 | -0.07463 |
| SI | hold_RISE→CK | -0.09453 | -0.08955 | -0.08955 |
| SI | setup_FALL→CK | 0.14927 | 0.14927 | 0.14927 |
| SI | setup_RISE→CK | 0.12438 | 0.12935 | 0.12935 |
| CK | minpwh | 0.08556 | 0.08951 | 0.09742 |

| | | | | |
|----|--------|---------|---------|---------|
| CK | minpwl | 0.08060 | 0.08062 | 0.08557 |
|----|--------|---------|---------|---------|

SEDGRNQHS

Cell Description

Scan Enable D Flip-Flop with Sync Clear
 $Q = \text{rising}(\text{CK}) ? (\text{SE} ? \text{SI} : (!\text{RN} ? 0 : \text{E} ? \text{D} : \text{pre_Q})) : \text{pre_Q}$



Function Table

| CK<1> | CK | SE | RN | E | Q | D | SI | Q |
|-------|----|----|----|---|---|---|----|------|
| 0 | 0 | X | X | X | X | X | X | Q<1> |
| 0 | 1 | 0 | 0 | X | X | X | X | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | X | X | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | X | X | 1 |
| 0 | 1 | 0 | 1 | 1 | X | 0 | X | 0 |
| 0 | 1 | 0 | 1 | 1 | X | 1 | X | 1 |
| 0 | 1 | 1 | X | X | X | X | 0 | 0 |
| 0 | 1 | 1 | X | X | X | X | 1 | 1 |
| 1 | X | X | X | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|-------------|------------|-----------|
| SEDGRNQHSV1 | 1.80 | 8.00 |
| SEDGRNQHSV2 | 1.80 | 8.00 |
| SEDGRNQHSV4 | 1.80 | 8.40 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00290 | 0.00290 | 0.00300 |
| D | 0.00054 | 0.00054 | 0.00054 |
| E | 0.00104 | 0.00105 | 0.00108 |
| Q | 0.00457 | 0.00485 | 0.00580 |
| RN | 0.00090 | 0.00089 | 0.00090 |
| SE | 0.00265 | 0.00263 | 0.00266 |
| SI | 0.00152 | 0.00151 | 0.00153 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00109 | 0.00110 | 0.00109 |
| D | 0.00102 | 0.00102 | 0.00103 |
| E | 0.00254 | 0.00246 | 0.00264 |
| RN | 0.00100 | 0.00099 | 0.00103 |
| SE | 0.00321 | 0.00321 | 0.00323 |
| SI | 0.00088 | 0.00088 | 0.00088 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00071132 | 0.00074362 | 0.00087922 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.14066 | 0.13943 | 0.13966 |
| CK→Q_RISE | 0.13506 | 0.13606 | 0.13887 |

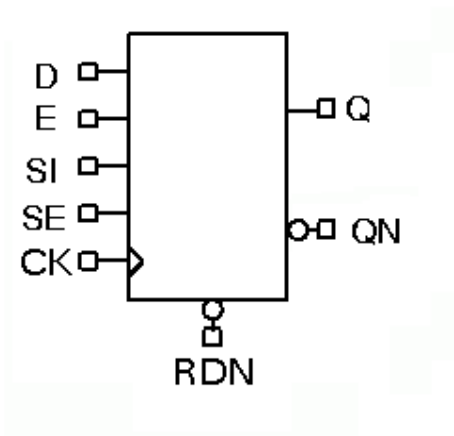
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.11940 | -0.11443 | -0.10944 |
| D | hold_RISE→CK | -0.10945 | -0.10446 | -0.10446 |
| D | setup_FALL→CK | 0.19403 | 0.19403 | 0.19403 |
| D | setup_RISE→CK | 0.14428 | 0.14925 | 0.15423 |
| E | hold_FALL→CK | -0.12437 | -0.11939 | -0.10945 |
| E | hold_RISE→CK | -0.12935 | -0.12935 | -0.12935 |
| E | setup_FALL→CK | 0.15422 | 0.15423 | 0.15422 |
| E | setup_RISE→CK | 0.14925 | 0.14924 | 0.15423 |
| RN | hold_FALL→CK | -0.19405 | -0.18408 | -0.17413 |
| RN | hold_RISE→CK | -0.12934 | -0.12436 | -0.12437 |
| RN | setup_FALL→CK | 0.27860 | 0.27862 | 0.28358 |
| RN | setup_RISE→CK | 0.15920 | 0.15919 | 0.16418 |
| SE | hold_FALL→CK | -0.12437 | -0.12438 | -0.12438 |
| SE | hold_RISE→CK | -0.12439 | -0.11941 | -0.11445 |
| SE | setup_FALL→CK | 0.15423 | 0.15423 | 0.15920 |
| SE | setup_RISE→CK | 0.17911 | 0.17911 | 0.17911 |
| SI | hold_FALL→CK | -0.08956 | -0.08458 | -0.07960 |
| SI | hold_RISE→CK | -0.09453 | -0.09453 | -0.08955 |
| SI | setup_FALL→CK | 0.14926 | 0.14925 | 0.15422 |
| SI | setup_RISE→CK | 0.12438 | 0.12934 | 0.12935 |
| CK | minpwh | 0.07765 | 0.08162 | 0.08159 |
| CK | minpwl | 0.08060 | 0.08061 | 0.08062 |

SEDRNHS

Cell Description

a high-speed, positive-edge triggered, static D-type Flip-Flop with a scan input (SI), active-high enable, active-high scan enable (SE), and asynchronous active-low reset (RDN).
Q = !RDN ? 0 : rising (CK) ? (SE ? SI : (E ? D : pre_Q)) : pre_Q
QN = !Q



Function Table

| RDN | CK<1> | CK | E | Q | D | SE | SI | Q |
|-----|-------|----|---|---|---|----|----|------|
| 0 | X | X | X | X | X | X | X | 0 |
| 1 | 0 | 0 | X | X | X | X | X | Q<1> |
| 1 | 0 | 1 | 0 | 0 | X | 0 | X | 0 |
| 1 | 0 | 1 | 0 | 0 | X | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | X | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | X | 0 | X | 1 |
| 1 | 0 | 1 | 0 | 1 | X | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | X | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | X | 0 | 0 | X | 0 |
| 1 | 0 | 1 | 1 | X | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | X | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | X | 1 | 0 | X | 1 |
| 1 | 0 | 1 | 1 | X | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | X | 1 | 1 | 1 | 1 |
| 1 | 1 | X | X | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| SEDRNHSV1 | 1.80 | 8.80 |
| SEDRNHSV2 | 1.80 | 9.00 |
| SEDRNHSV4 | 1.80 | 9.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00344 | 0.00358 | 0.00402 |
| D | 0.00028 | 0.00031 | 0.00031 |
| E | 0.00113 | 0.00115 | 0.00112 |

| | | | |
|-----|---------|---------|---------|
| Q | 0.00300 | 0.00333 | 0.00426 |
| QN | 0.00304 | 0.00337 | 0.00426 |
| RDN | 0.00086 | 0.00093 | 0.00094 |
| SE | 0.00128 | 0.00132 | 0.00136 |
| SI | 0.00057 | 0.00062 | 0.00063 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00095 | 0.00095 | 0.00147 |
| D | 0.00086 | 0.00086 | 0.00082 |
| E | 0.00249 | 0.00249 | 0.00246 |
| RDN | 0.00286 | 0.00288 | 0.00294 |
| SE | 0.00202 | 0.00202 | 0.00206 |
| SI | 0.00074 | 0.00074 | 0.00076 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00080248 | 0.00090525 | 0.00119820 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.12404 | 0.12833 | 0.12619 |
| CK→Q_RISE | 0.12976 | 0.13098 | 0.12691 |
| RDN→Q_FALL | 0.08118 | 0.08113 | 0.08597 |
| CK→QN_FALL | 0.17921 | 0.17673 | 0.17952 |
| CK→QN_RISE | 0.17703 | 0.18218 | 0.18848 |
| RDN→QN_RISE | 0.12873 | 0.12818 | 0.13999 |

Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.12935 | -0.13432 | -0.13931 |
| D | hold_RISE→CK | -0.10448 | -0.10946 | -0.11443 |
| D | setup_FALL→CK | 0.18407 | 0.18905 | 0.19901 |
| D | setup_RISE→CK | 0.12439 | 0.12936 | 0.14428 |
| E | hold_FALL→CK | -0.12437 | -0.12933 | -0.14426 |
| E | hold_RISE→CK | -0.11939 | -0.12437 | -0.13928 |
| E | setup_FALL→CK | 0.13929 | 0.14427 | 0.15918 |
| E | setup_RISE→CK | 0.12435 | 0.12934 | 0.14924 |
| RDN | setup_RISE→CK | 0.14925 | 0.15422 | 0.16915 |
| RDN | hold_RISE→CK | -0.14426 | -0.14925 | -0.15920 |
| SE | hold_FALL→CK | -0.13929 | -0.14427 | -0.15422 |
| SE | hold_RISE→CK | -0.12933 | -0.13929 | -0.14428 |
| SE | setup_FALL→CK | 0.16913 | 0.17412 | 0.18903 |

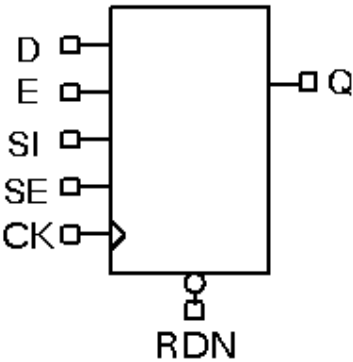
| | | | | |
|-----|---------------|----------|----------|----------|
| SE | setup_RISE→CK | 0.18903 | 0.19400 | 0.20398 |
| SI | hold_FALL→CK | -0.11443 | -0.11940 | -0.11939 |
| SI | hold_RISE→CK | -0.09950 | -0.09950 | -0.10947 |
| SI | setup_FALL→CK | 0.16916 | 0.17910 | 0.18406 |
| SI | setup_RISE→CK | 0.11941 | 0.12436 | 0.13434 |
| CK | minpwh | 0.08158 | 0.08158 | 0.08157 |
| CK | minpwl | 0.13004 | 0.13497 | 0.13003 |
| RDN | minpwl | 0.07368 | 0.07763 | 0.08950 |

SEDRNQHS

Cell Description

a high-speed, positive-edge triggered, static D-type Flip-Flop with a scan input (SI), active-high enable, active-high scan enable (SE), and asynchronous active-low reset (RDN) The cell has a single output (Q).

$$Q = \neg RDN ? 0 : \text{rising}(CK) ? (SE ? SI : (E ? D : \text{pre_Q})) : \text{pre_Q}$$



Function Table

| RDN | CK<1> | CK | E | Q | D | SE | SI | Q |
|-----|-------|----|---|---|---|----|----|------|
| 0 | X | X | X | X | X | X | X | 0 |
| 1 | 0 | 0 | X | X | X | X | X | Q<1> |
| 1 | 0 | 1 | 0 | 0 | X | 0 | X | 0 |
| 1 | 0 | 1 | 0 | 0 | X | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | X | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | X | 0 | X | 1 |
| 1 | 0 | 1 | 0 | 1 | X | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | X | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | X | 0 | 0 | X | 0 |
| 1 | 0 | 1 | 1 | X | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | X | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | X | 1 | 0 | X | 1 |
| 1 | 0 | 1 | 1 | X | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | X | 1 | 1 | 1 | 1 |
| 1 | 1 | X | X | X | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| SEDRNQHSV1 | 1.80 | 8.80 |
| SEDRNQHSV2 | 1.80 | 8.80 |
| SEDRNQHSV4 | 1.80 | 9.00 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00357 | 0.00357 | 0.00356 |
| D | 0.00032 | 0.00032 | 0.00032 |
| E | 0.00116 | 0.00116 | 0.00116 |

| | | | |
|-----|---------|---------|---------|
| Q | 0.00686 | 0.00714 | 0.00793 |
| RDN | 0.00095 | 0.00095 | 0.00095 |
| SE | 0.00134 | 0.00134 | 0.00135 |
| SI | 0.00063 | 0.00063 | 0.00063 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CK | 0.00094 | 0.00094 | 0.00094 |
| D | 0.00084 | 0.00085 | 0.00085 |
| E | 0.00250 | 0.00250 | 0.00250 |
| RDN | 0.00288 | 0.00288 | 0.00288 |
| SE | 0.00208 | 0.00204 | 0.00204 |
| SI | 0.00074 | 0.00075 | 0.00075 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00078926 | 0.00080878 | 0.00089308 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CK→Q_FALL | 0.12699 | 0.12566 | 0.13712 |
| CK→Q_RISE | 0.12730 | 0.12822 | 0.13309 |
| RDN→Q_FALL | 0.07954 | 0.07992 | 0.08428 |

Timing Constraints (ns)

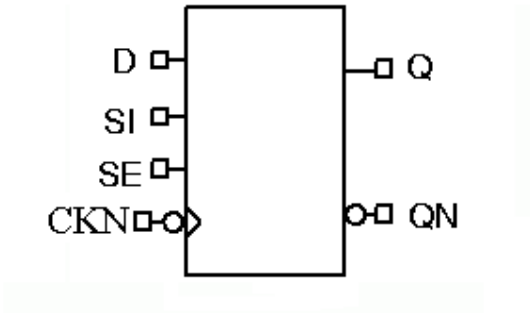
| Pin | Requirement | V1 | V2 | V4 |
|-----|---------------|----------|----------|----------|
| D | hold_FALL→CK | -0.13432 | -0.13432 | -0.12936 |
| D | hold_RISE→CK | -0.10945 | -0.10945 | -0.10946 |
| D | setup_FALL→CK | 0.18409 | 0.18905 | 0.18905 |
| D | setup_RISE→CK | 0.12936 | 0.12936 | 0.13434 |
| E | hold_FALL→CK | -0.13431 | -0.12933 | -0.12933 |
| E | hold_RISE→CK | -0.12437 | -0.12437 | -0.12437 |
| E | setup_FALL→CK | 0.14923 | 0.14427 | 0.14427 |
| E | setup_RISE→CK | 0.12934 | 0.13430 | 0.13430 |
| RDN | setup_RISE→CK | 0.15423 | 0.15423 | 0.15919 |
| RDN | hold_RISE→CK | -0.14925 | -0.14925 | -0.14925 |
| SE | hold_FALL→CK | -0.14924 | -0.14923 | -0.14428 |
| SE | hold_RISE→CK | -0.13929 | -0.13929 | -0.13432 |
| SE | setup_FALL→CK | 0.17410 | 0.17412 | 0.17410 |
| SE | setup_RISE→CK | 0.19400 | 0.19400 | 0.19898 |
| SI | hold_FALL→CK | -0.11941 | -0.11940 | -0.11442 |
| SI | hold_RISE→CK | -0.10946 | -0.10946 | -0.10448 |
| SI | setup_FALL→CK | 0.17412 | 0.17414 | 0.17911 |

| | | | | |
|-----|---------------|---------|---------|---------|
| SI | setup_RISE→CK | 0.12935 | 0.12936 | 0.13432 |
| CK | minpwh | 0.08158 | 0.08159 | 0.08159 |
| CK | minpwl | 0.13988 | 0.13991 | 0.13990 |
| RDN | minpwl | 0.06973 | 0.07369 | 0.08555 |

SNDHS

Cell Description

Negative Edge Trigger Scan D Flip-Flop
Q = falling (CKN) ? (SE&SI | !SE&D) : pre_Q
QN = !Q



Function Table

| CKN<1> | CKN | SE | SI | D | Q |
|--------|-----|----|----|---|------|
| 0 | X | X | X | X | Q<1> |
| 1 | 0 | 0 | X | 0 | 0 |
| 1 | 0 | 0 | X | 1 | 1 |
| 1 | 0 | 1 | 0 | X | 0 |
| 1 | 0 | 1 | 1 | X | 1 |
| 1 | 1 | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| SNDHSV1 | 1.80 | 6.40 |
| SNDHSV2 | 1.80 | 6.40 |
| SNDHSV4 | 1.80 | 6.80 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|----------|----------|----------|
| CKN | 0.00304 | 0.00312 | 0.00321 |
| D | 0.00093 | 0.00098 | 0.00100 |
| Q | -0.00139 | -0.00115 | -0.00049 |
| QN | -0.00140 | -0.00118 | -0.00058 |
| SE | 0.00190 | 0.00195 | 0.00198 |
| SI | 0.00095 | 0.00100 | 0.00102 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CKN | 0.00108 | 0.00108 | 0.00130 |
| D | 0.00148 | 0.00148 | 0.00149 |

| | | | |
|----|---------|---------|---------|
| SE | 0.00233 | 0.00233 | 0.00234 |
| SI | 0.00147 | 0.00148 | 0.00148 |

Max Leakage Power (uW)

| | | |
|------------|------------|------------|
| V1 | V2 | V4 |
| 0.00059891 | 0.00069005 | 0.00092830 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CKN→Q_FALL | 0.13782 | 0.13750 | 0.13516 |
| CKN→Q_RISE | 0.11679 | 0.12218 | 0.11817 |
| CKN→QN_FALL | 0.15250 | 0.15715 | 0.15807 |
| CKN→QN_RISE | 0.17210 | 0.17247 | 0.17493 |

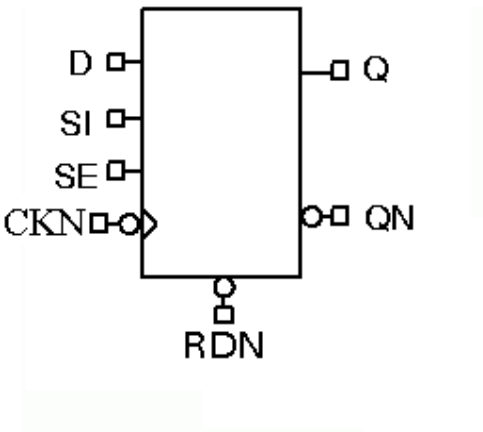
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|----------------|----------|----------|----------|
| D | hold_FALL→CKN | -0.05970 | -0.06469 | -0.06468 |
| D | hold_RISE→CKN | -0.00000 | -0.00498 | -0.01492 |
| D | setup_FALL→CKN | 0.07462 | 0.07462 | 0.07961 |
| D | setup_RISE→CKN | 0.05472 | 0.05473 | 0.06964 |
| SE | hold_FALL→CKN | -0.02986 | -0.03484 | -0.04478 |
| SE | hold_RISE→CKN | -0.08458 | -0.08458 | -0.08955 |
| SE | setup_FALL→CKN | 0.07961 | 0.07961 | 0.09950 |
| SE | setup_RISE→CKN | 0.09951 | 0.09951 | 0.10448 |
| SI | hold_FALL→CKN | -0.05969 | -0.06467 | -0.06467 |
| SI | hold_RISE→CKN | -0.00499 | -0.00994 | -0.01989 |
| SI | setup_FALL→CKN | 0.07462 | 0.07960 | 0.07959 |
| SI | setup_RISE→CKN | 0.05969 | 0.05969 | 0.07462 |
| CKN | minpwh | 0.08552 | 0.08556 | 0.08554 |
| CKN | minpwl | 0.09740 | 0.10134 | 0.10136 |

SNDRNHS

Cell Description

Negative Edge Trigger Scan D Flip-Flop with Async Clear
 $Q = \neg RDN \text{ ? } 0 \text{ : falling (CKN) ? (SE \& SI \mid \neg SE \& D) : pre_Q}$
 $QN = \neg Q$



Function Table

| RDN | CKN<1> | CKN | SE | SI | D | Q |
|-----|--------|-----|----|----|---|------|
| 0 | X | X | X | X | X | 0 |
| 1 | 0 | X | X | X | X | Q<1> |
| 1 | 1 | 0 | 0 | X | 0 | 0 |
| 1 | 1 | 0 | 0 | X | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | X | 0 |
| 1 | 1 | 0 | 1 | 1 | X | 1 |
| 1 | 1 | 1 | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| SNDRNHSV1 | 1.80 | 6.80 |
| SNDRNHSV2 | 1.80 | 6.80 |
| SNDRNHSV4 | 1.80 | 7.20 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CKN | 0.00351 | 0.00351 | 0.00363 |
| D | 0.00073 | 0.00073 | 0.00075 |
| Q | 0.00056 | 0.00080 | 0.00151 |
| QN | 0.00065 | 0.00090 | 0.00165 |
| RDN | 0.00107 | 0.00107 | 0.00108 |
| SE | 0.00161 | 0.00163 | 0.00164 |
| SI | 0.00073 | 0.00073 | 0.00074 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|----|----|----|
|-----|----|----|----|

| | | | |
|-----|---------|---------|---------|
| CKN | 0.00133 | 0.00134 | 0.00136 |
| D | 0.00103 | 0.00102 | 0.00107 |
| RDN | 0.00311 | 0.00307 | 0.00303 |
| SE | 0.00249 | 0.00247 | 0.00249 |
| SI | 0.00096 | 0.00095 | 0.00095 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00085578 | 0.00090033 | 0.00112380 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CKN→Q_FALL | 0.11945 | 0.12366 | 0.14693 |
| CKN→Q_RISE | 0.15034 | 0.15553 | 0.17240 |
| RDN→Q_FALL | 0.04648 | 0.04722 | 0.06145 |
| CKN→QN_FALL | 0.10927 | 0.11025 | 0.11465 |
| CKN→QN_RISE | 0.08401 | 0.08605 | 0.09463 |
| RDN→QN_RISE | 0.11295 | 0.11630 | 0.13443 |

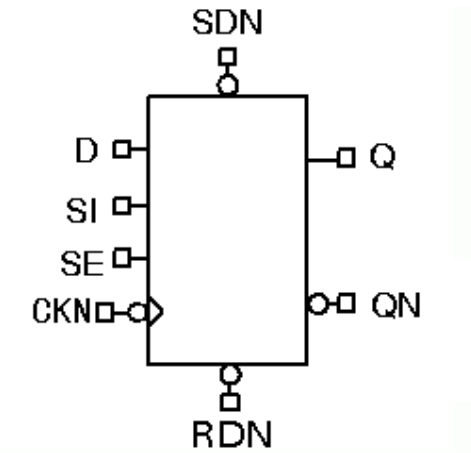
Timing Constraints (ns)

| Pin | Requirement | V1 | V2 | V4 |
|-----|----------------|----------|----------|----------|
| D | hold_FALL→CKN | -0.04975 | -0.04974 | -0.03483 |
| D | hold_RISE→CKN | -0.03979 | -0.03482 | -0.02985 |
| D | setup_FALL→CKN | 0.09949 | 0.10945 | 0.10945 |
| D | setup_RISE→CKN | 0.08955 | 0.08457 | 0.08954 |
| RDN | setup_RISE→CKN | 0.09950 | 0.09452 | 0.09452 |
| RDN | hold_RISE→CKN | -0.08457 | -0.07462 | -0.07959 |
| SE | hold_FALL→CKN | -0.05473 | -0.04974 | -0.04477 |
| SE | hold_RISE→CKN | -0.06965 | -0.05969 | -0.05472 |
| SE | setup_FALL→CKN | 0.10448 | 0.09950 | 0.10447 |
| SE | setup_RISE→CKN | 0.12437 | 0.12436 | 0.12935 |
| SI | hold_FALL→CKN | -0.05969 | -0.04975 | -0.04477 |
| SI | hold_RISE→CKN | -0.04478 | -0.03979 | -0.03482 |
| SI | setup_FALL→CKN | 0.10945 | 0.11443 | 0.11939 |
| SI | setup_RISE→CKN | 0.09451 | 0.09452 | 0.09949 |
| CKN | minpwh | 0.07567 | 0.07565 | 0.07566 |
| CKN | minpwl | 0.07368 | 0.07758 | 0.08555 |
| RDN | minpwl | 0.06181 | 0.06183 | 0.06181 |

SNDRSNHS

Cell Description

Negative Edge Trigger Scan D Flip-Flop with Async Clear and Set
 $Q = \text{!SDN} ? 1 : \text{!RDN} ? 0 : \text{falling}(\text{CKN}) ? (\text{SE} \& \text{SI} \mid \text{!SE} \& \text{D}) : \text{pre_Q}$
 $\text{QN} = \text{!Q}$



Function Table

| RDN | SDN | CKN<1> | CKN | SE | D | SI | Q |
|-----|-----|--------|-----|----|---|----|------|
| 0 | 0 | X | X | X | X | X | 1 |
| 0 | 1 | X | X | X | X | X | 0 |
| 1 | 0 | X | X | X | X | X | 1 |
| 1 | 1 | 0 | X | X | X | X | Q<1> |
| 1 | 1 | 1 | 0 | 0 | 0 | X | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | X | 1 |
| 1 | 1 | 1 | 0 | 1 | X | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | X | 1 | 1 |
| 1 | 1 | 1 | 1 | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|------------|------------|-----------|
| SNDRSNHSV1 | 1.80 | 8.20 |
| SNDRSNHSV2 | 1.80 | 8.20 |
| SNDRSNHSV4 | 1.80 | 8.60 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CKN | 0.00386 | 0.00386 | 0.00383 |
| D | 0.00108 | 0.00107 | 0.00109 |
| Q | 0.00195 | 0.00218 | 0.00306 |
| QN | 0.00199 | 0.00223 | 0.00317 |
| RDN | 0.00140 | 0.00140 | 0.00142 |
| SDN | 0.00051 | 0.00051 | 0.00052 |
| SE | 0.00181 | 0.00182 | 0.00182 |
| SI | 0.00105 | 0.00104 | 0.00105 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CKN | 0.00123 | 0.00125 | 0.00122 |
| D | 0.00141 | 0.00141 | 0.00144 |
| RDN | 0.00121 | 0.00121 | 0.00124 |
| SDN | 0.00169 | 0.00169 | 0.00170 |
| SE | 0.00223 | 0.00225 | 0.00221 |
| SI | 0.00116 | 0.00116 | 0.00116 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00103320 | 0.00106190 | 0.00129010 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CKN→Q_FALL | 0.13953 | 0.14332 | 0.16439 |
| CKN→Q_RISE | 0.15945 | 0.16462 | 0.18310 |
| RDN→Q_FALL | 0.15747 | 0.16113 | 0.18021 |
| SDN→Q_FALL | 0.14375 | 0.14737 | 0.16550 |
| SDN→Q_RISE | 0.09272 | 0.09571 | 0.10993 |
| CKN→QN_FALL | 0.12655 | 0.12606 | 0.13054 |
| CKN→QN_RISE | 0.09931 | 0.10102 | 0.10811 |
| RDN→QN_RISE | 0.11549 | 0.11734 | 0.12346 |
| SDN→QN_FALL | 0.06464 | 0.06387 | 0.06768 |
| SDN→QN_RISE | 0.10180 | 0.10360 | 0.10883 |

Timing Constraints (ns)

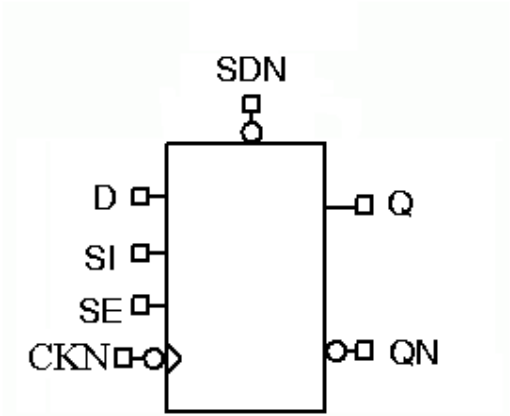
| Pin | Requirement | V1 | V2 | V4 |
|-----|------------------------|----------|----------|----------|
| D | hold_FALL→CKN | -0.05970 | -0.05970 | -0.05471 |
| D | hold_RISE→CKN | -0.01491 | -0.01492 | -0.00994 |
| D | setup_FALL→CKN | 0.10447 | 0.10448 | 0.10945 |
| D | setup_RISE→CKN | 0.08457 | 0.08954 | 0.08955 |
| RDN | setup_RISE→CKN | 0.03483 | 0.03980 | 0.04477 |
| RDN | hold_RISE→CKN | -0.00499 | -0.00500 | -0.00499 |
| SDN | setup_RISE→CKN | 0.00000 | 0.00499 | 0.00994 |
| SDN | hold_RISE→CKN | 0.01493 | 0.01493 | 0.01493 |
| SDN | non_seq_hold_RISE→RDN | -0.08457 | -0.08457 | -0.08954 |
| SDN | non_seq_setup_RISE→RDN | 0.10447 | 0.10945 | 0.11442 |
| SE | hold_FALL→CKN | -0.03482 | -0.02986 | -0.02487 |
| SE | hold_RISE→CKN | -0.08457 | -0.07959 | -0.07461 |
| SE | setup_FALL→CKN | 0.10449 | 0.10450 | 0.10447 |
| SE | setup_RISE→CKN | 0.12935 | 0.13433 | 0.13930 |
| SI | hold_FALL→CKN | -0.06966 | -0.06966 | -0.06468 |

| | | | | |
|-----|----------------|----------|----------|----------|
| SI | hold_RISE→CKN | -0.01493 | -0.01494 | -0.00995 |
| SI | setup_FALL→CKN | 0.11940 | 0.11941 | 0.12437 |
| SI | setup_RISE→CKN | 0.08458 | 0.08956 | 0.08956 |
| CKN | minpwh | 0.08058 | 0.08558 | 0.08059 |
| CKN | minpwl | 0.08557 | 0.08947 | 0.09741 |
| RDN | minpwl | 0.10923 | 0.10922 | 0.11712 |
| SDN | minpwl | 0.07763 | 0.08162 | 0.08558 |

SNDSNHS

Cell Description

Negative Edge Trigger Scan D Flip-Flop with Async Set
 $Q = \neg SDN \text{ ? } 1 \text{ : falling (CKN) ? (SE \& SI \mid \neg SE \& D) : pre_Q}$
 $QN = \neg Q$



Function Table

| SDN | CKN<1> | CKN | SE | SI | D | Q |
|-----|--------|-----|----|----|---|------|
| 0 | X | X | X | X | X | 1 |
| 1 | 0 | X | X | X | X | Q<1> |
| 1 | 1 | 0 | 0 | X | 0 | 0 |
| 1 | 1 | 0 | 0 | X | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | X | 0 |
| 1 | 1 | 0 | 1 | 1 | X | 1 |
| 1 | 1 | 1 | X | X | X | Q<1> |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| SNDSNHSV1 | 1.80 | 7.00 |
| SNDSNHSV2 | 1.80 | 7.00 |
| SNDSNHSV4 | 1.80 | 7.60 |

Pin Power (uW/MHz)

| Pin | V1 | V2 | V4 |
|-----|---------|---------|---------|
| CKN | 0.00361 | 0.00368 | 0.00388 |
| D | 0.00074 | 0.00075 | 0.00076 |
| Q | 0.00119 | 0.00140 | 0.00219 |
| QN | 0.00119 | 0.00137 | 0.00217 |
| SDN | 0.00042 | 0.00042 | 0.00044 |
| SE | 0.00141 | 0.00141 | 0.00144 |
| SI | 0.00075 | 0.00075 | 0.00076 |

Pin Capacitance (pf)

| Pin | V1 | V2 | V4 |
|-----|----|----|----|
|-----|----|----|----|

| | | | |
|-----|---------|---------|---------|
| CKN | 0.00101 | 0.00101 | 0.00122 |
| D | 0.00110 | 0.00110 | 0.00113 |
| SDN | 0.00154 | 0.00158 | 0.00169 |
| SE | 0.00198 | 0.00198 | 0.00200 |
| SI | 0.00111 | 0.00111 | 0.00113 |

Max Leakage Power (uW)

| V1 | V2 | V4 |
|------------|------------|------------|
| 0.00083460 | 0.00090989 | 0.00118820 |

Delay Table (ns)

| Description | V1 | V2 | V4 |
|-------------|---------|---------|---------|
| CKN→Q_FALL | 0.14750 | 0.14655 | 0.14551 |
| CKN→Q_RISE | 0.15466 | 0.15435 | 0.15287 |
| SDN→Q_RISE | 0.09670 | 0.09703 | 0.10788 |
| CKN→QN_FALL | 0.11736 | 0.11692 | 0.10812 |
| CKN→QN_RISE | 0.10670 | 0.10847 | 0.10115 |
| SDN→QN_FALL | 0.06003 | 0.06058 | 0.06581 |

Timing Constraints (ns)

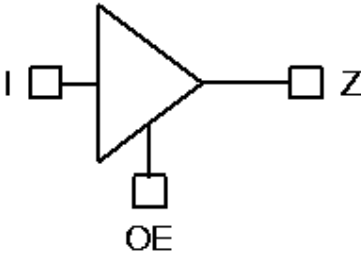
| Pin | Requirement | V1 | V2 | V4 |
|-----|----------------|----------|----------|----------|
| D | hold_FALL→CKN | -0.07462 | -0.06964 | -0.06964 |
| D | hold_RISE→CKN | -0.00000 | -0.00000 | -0.00000 |
| D | setup_FALL→CKN | 0.11441 | 0.11441 | 0.12437 |
| D | setup_RISE→CKN | 0.06965 | 0.07461 | 0.07961 |
| SDN | setup_RISE→CKN | 0.00499 | 0.00000 | 0.00000 |
| SDN | hold_RISE→CKN | 0.01990 | 0.02488 | 0.01989 |
| SE | hold_FALL→CKN | -0.02486 | -0.01989 | -0.02486 |
| SE | hold_RISE→CKN | -0.08956 | -0.08956 | -0.08955 |
| SE | setup_FALL→CKN | 0.09451 | 0.09451 | 0.10446 |
| SE | setup_RISE→CKN | 0.13431 | 0.13431 | 0.13929 |
| SI | hold_FALL→CKN | -0.07463 | -0.07463 | -0.07462 |
| SI | hold_RISE→CKN | -0.00498 | -0.00000 | -0.00000 |
| SI | setup_FALL→CKN | 0.11940 | 0.11940 | 0.12435 |
| SI | setup_RISE→CKN | 0.07461 | 0.07461 | 0.08457 |
| CKN | minpwh | 0.11031 | 0.11022 | 0.11028 |
| CKN | minpwl | 0.08155 | 0.08154 | 0.07765 |
| SDN | minpwl | 0.06973 | 0.07368 | 0.08156 |

TBUFHS

Cell Description

3-State Buffer with High Enable

$Z = OE ? I : (1'bZ)$



Function Table

| OE | I | Z |
|----|---|---|
| 0 | X | Z |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| TBUFHSV0 | 1.80 | 2.00 |
| TBUFHSV1 | 1.80 | 2.00 |
| TBUFHSV2 | 1.80 | 2.00 |
| TBUFHSV3 | 1.80 | 2.20 |
| TBUFHSV4 | 1.80 | 2.60 |
| TBUFHSV6 | 1.80 | 2.60 |
| TBUFHSV8 | 1.80 | 3.20 |
| TBUFHSV12 | 1.80 | 3.60 |
| TBUFHSV16 | 1.80 | 5.00 |
| TBUFHSV20 | 1.80 | 5.40 |
| TBUFHSV24 | 1.80 | 6.00 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V3 | V4 | V6 | V8 | V12 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00182 | 0.00198 | 0.00225 | 0.00266 | 0.00353 | 0.00443 | 0.00556 | 0.00753 |
| OE | 0.00128 | 0.00143 | 0.00168 | 0.00205 | 0.00258 | 0.00343 | 0.00414 | 0.00578 |

| Pin | V16 | V20 | V24 |
|-----|---------|---------|---------|
| I | 0.01053 | 0.01261 | 0.01445 |
| OE | 0.00817 | 0.00976 | 0.01140 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V3 | V4 | V6 | V8 | V12 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|
| I | 0.00108 | 0.00107 | 0.00108 | 0.00107 | 0.00192 | 0.00170 | 0.00264 | 0.00307 |
| OE | 0.00185 | 0.00185 | 0.00186 | 0.00186 | 0.00220 | 0.00211 | 0.00223 | 0.00254 |

| Pin | V16 | V20 | V24 |
|-----|---------|---------|---------|
| I | 0.00418 | 0.00568 | 0.00588 |
| OE | 0.00374 | 0.00357 | 0.00356 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V3 | V4 | V6 | V8 | V12 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 0.00022066 | 0.00023429 | 0.00026464 | 0.00032972 | 0.00042556 | 0.00055659 | 0.00076405 | 0.00110000 |

| V16 | V20 | V24 |
|------------|------------|------------|
| 0.00149740 | 0.00189490 | 0.00221190 |

Delay Table (ns)

| Description | V0 | V1 | V2 | V3 | V4 | V6 | V8 | V12 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| I→Z_FALL | 0.06702 | 0.06658 | 0.06831 | 0.07310 | 0.06378 | 0.06333 | 0.05556 | 0.06086 |
| I→Z_RISE | 0.05921 | 0.05891 | 0.06121 | 0.06400 | 0.04091 | 0.05243 | 0.04865 | 0.05350 |
| OE→Z_FALL | 0.04336 | 0.04269 | 0.04368 | 0.04589 | 0.04270 | 0.04557 | 0.04443 | 0.04444 |
| OE→Z_RISE | 0.04045 | 0.04017 | 0.04149 | 0.04276 | 0.03777 | 0.04274 | 0.04702 | 0.04680 |

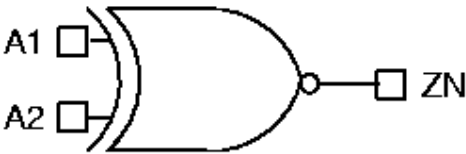
| Description | V16 | V20 | V24 |
|-------------|---------|---------|---------|
| I→Z_FALL | 0.05879 | 0.05488 | 0.05879 |
| I→Z_RISE | 0.04915 | 0.04764 | 0.05114 |
| OE→Z_FALL | 0.04590 | 0.04587 | 0.04972 |
| OE→Z_RISE | 0.04659 | 0.04685 | 0.05017 |

XNOR2HS

Cell Description

2-Input Exclusive NOR

$$ZN = \neg(A1 \oplus A2)$$



Function Table

| A2 | A1 | ZN |
|----|----|----|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| XNOR2HSV0 | 1.80 | 2.20 |
| XNOR2HSV1 | 1.80 | 2.20 |
| XNOR2HSV2 | 1.80 | 2.40 |
| XNOR2HSV4 | 1.80 | 2.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00188 | 0.00222 | 0.00276 | 0.00381 |
| A2 | 0.00271 | 0.00326 | 0.00376 | 0.00511 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00192 | 0.00209 | 0.00223 | 0.00265 |
| A2 | 0.00129 | 0.00153 | 0.00165 | 0.00243 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00034462 | 0.00039554 | 0.00046956 | 0.00074853 |

Delay Table (ns)

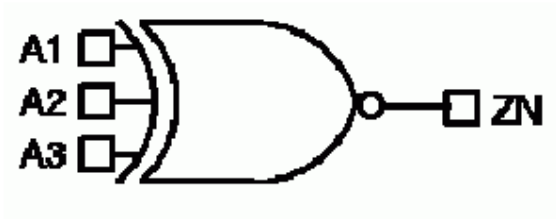
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.05584 | 0.05390 | 0.05366 | 0.05243 |
| A1→ZN_RISE | 0.05055 | 0.04941 | 0.04936 | 0.04718 |
| A2→ZN_FALL | 0.07823 | 0.07328 | 0.07270 | 0.06729 |
| A2→ZN_RISE | 0.07265 | 0.06823 | 0.06689 | 0.06096 |

XNOR3HS

Cell Description

3-Input Exclusive NOR

$$ZN = \neg(A1 \oplus A2 \oplus A3)$$



Function Table

| A2 | A1 | A3 | ZN |
|----|----|----|----|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| XNOR3HSV0 | 1.80 | 4.60 |
| XNOR3HSV1 | 1.80 | 4.60 |
| XNOR3HSV2 | 1.80 | 4.80 |
| XNOR3HSV4 | 1.80 | 7.00 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00503 | 0.00569 | 0.00688 | 0.00959 |
| A2 | 0.00395 | 0.00448 | 0.00526 | 0.00750 |
| A3 | 0.00182 | 0.00209 | 0.00250 | 0.00380 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00118 | 0.00132 | 0.00153 | 0.00220 |
| A2 | 0.00312 | 0.00345 | 0.00393 | 0.00563 |

| | | | | |
|----|---------|---------|---------|---------|
| A3 | 0.00193 | 0.00204 | 0.00219 | 0.00280 |
|----|---------|---------|---------|---------|

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00066307 | 0.00076289 | 0.00091455 | 0.00136220 |

Delay Table (ns)

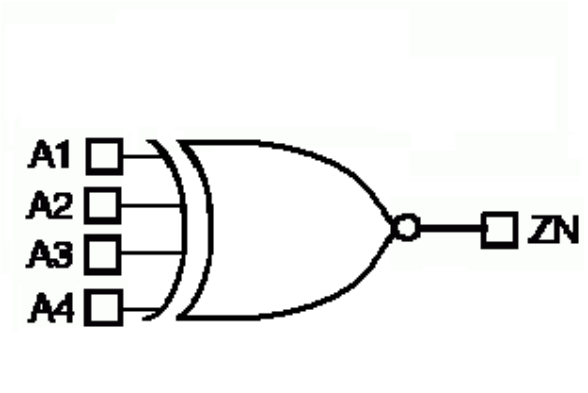
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.14005 | 0.13326 | 0.12713 | 0.12975 |
| A1→ZN_RISE | 0.12543 | 0.11947 | 0.11759 | 0.12168 |
| A2→ZN_FALL | 0.10396 | 0.09964 | 0.09502 | 0.09731 |
| A2→ZN_RISE | 0.08977 | 0.08582 | 0.08327 | 0.08697 |
| A3→ZN_FALL | 0.06206 | 0.06003 | 0.05868 | 0.06243 |
| A3→ZN_RISE | 0.05415 | 0.05200 | 0.05144 | 0.05634 |

XNOR4HS

Cell Description

4-Input Exclusive NOR

$$ZN = \neg(A1 \oplus A2 \oplus A3 \oplus A4)$$



Function Table

| A2 | A1 | A3 | A4 | ZN |
|----|----|----|----|----|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|-----------|------------|-----------|
| XNOR4HSV0 | 1.80 | 7.20 |
| XNOR4HSV1 | 1.80 | 7.40 |
| XNOR4HSV2 | 1.80 | 8.60 |
| XNOR4HSV4 | 1.80 | 12.40 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00509 | 0.00579 | 0.00693 | 0.00968 |

| | | | | |
|----|---------|---------|---------|---------|
| A2 | 0.00391 | 0.00448 | 0.00533 | 0.00755 |
| A3 | 0.00555 | 0.00622 | 0.00743 | 0.01091 |
| A4 | 0.00429 | 0.00481 | 0.00578 | 0.00835 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00120 | 0.00133 | 0.00158 | 0.00218 |
| A2 | 0.00314 | 0.00346 | 0.00377 | 0.00557 |
| A3 | 0.00121 | 0.00137 | 0.00156 | 0.00228 |
| A4 | 0.00319 | 0.00354 | 0.00379 | 0.00577 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00101700 | 0.00118410 | 0.00141200 | 0.00216100 |

Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→ZN_FALL | 0.14076 | 0.13481 | 0.13068 | 0.12823 |
| A1→ZN_RISE | 0.12752 | 0.12299 | 0.11912 | 0.11822 |
| A2→ZN_FALL | 0.10225 | 0.09880 | 0.09620 | 0.09429 |
| A2→ZN_RISE | 0.08958 | 0.08669 | 0.08510 | 0.08557 |
| A3→ZN_FALL | 0.13812 | 0.13202 | 0.12766 | 0.13385 |
| A3→ZN_RISE | 0.13858 | 0.13232 | 0.12876 | 0.13452 |
| A4→ZN_FALL | 0.10069 | 0.09650 | 0.09592 | 0.09840 |
| A4→ZN_RISE | 0.10107 | 0.09672 | 0.09670 | 0.09845 |

XOR2HS

Cell Description

2-Input Exclusive OR

$Z=(A1\wedge A2)$



Function Table

| A2 | A1 | Z |
|----|----|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| XOR2HSV0 | 1.80 | 2.00 |
| XOR2HSV1 | 1.80 | 2.20 |
| XOR2HSV2 | 1.80 | 2.20 |
| XOR2HSV4 | 1.80 | 3.00 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00182 | 0.00231 | 0.00264 | 0.00374 |
| A2 | 0.00239 | 0.00311 | 0.00353 | 0.00518 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00195 | 0.00204 | 0.00237 | 0.00256 |
| A2 | 0.00126 | 0.00145 | 0.00162 | 0.00234 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00033066 | 0.00039510 | 0.00049612 | 0.00074139 |

Delay Table (ns)

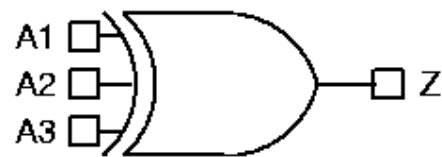
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.05133 | 0.05322 | 0.05202 | 0.05223 |
| A1→Z_RISE | 0.04926 | 0.05100 | 0.04957 | 0.04894 |
| A2→Z_FALL | 0.06988 | 0.07141 | 0.06928 | 0.06988 |
| A2→Z_RISE | 0.06536 | 0.06661 | 0.06487 | 0.06403 |

XOR3HS

Cell Description

3-Input Exclusive OR

$Z=(A1\wedge A2\wedge A3)$



Function Table

| A2 | A1 | A3 | Z |
|----|----|----|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| XOR3HSV0 | 1.80 | 4.20 |
| XOR3HSV1 | 1.80 | 4.20 |
| XOR3HSV2 | 1.80 | 4.40 |
| XOR3HSV4 | 1.80 | 6.80 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00502 | 0.00564 | 0.00668 | 0.00971 |
| A2 | 0.00389 | 0.00440 | 0.00514 | 0.00762 |
| A3 | 0.00182 | 0.00209 | 0.00248 | 0.00380 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00119 | 0.00133 | 0.00151 | 0.00220 |
| A2 | 0.00307 | 0.00339 | 0.00380 | 0.00566 |

| | | | | |
|----|---------|---------|---------|---------|
| A3 | 0.00192 | 0.00200 | 0.00216 | 0.00267 |
|----|---------|---------|---------|---------|

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00065226 | 0.00073167 | 0.00087938 | 0.00132480 |

Delay Table (ns)

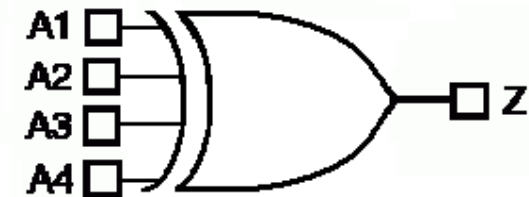
| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.14017 | 0.13309 | 0.12471 | 0.12961 |
| A1→Z_RISE | 0.12564 | 0.11986 | 0.11644 | 0.12223 |
| A2→Z_FALL | 0.10296 | 0.09899 | 0.09309 | 0.09718 |
| A2→Z_RISE | 0.08928 | 0.08600 | 0.08286 | 0.08750 |
| A3→Z_FALL | 0.06038 | 0.05872 | 0.05657 | 0.06093 |
| A3→Z_RISE | 0.05606 | 0.05429 | 0.05282 | 0.05565 |

XOR4HS

Cell Description

4-Input Exclusive OR

$Z=(A1^A2^A3^A4)$



Function Table

| A2 | A1 | A3 | A4 | Z |
|----|----|----|----|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |

Cell Size

| CellName | Height(um) | Width(um) |
|----------|------------|-----------|
| XOR4HSV0 | 1.80 | 7.00 |
| XOR4HSV1 | 1.80 | 7.00 |
| XOR4HSV2 | 1.80 | 8.20 |
| XOR4HSV4 | 1.80 | 12.00 |

Pin Power (uW/MHz)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00506 | 0.00570 | 0.00686 | 0.00956 |

| | | | | |
|----|---------|---------|---------|---------|
| A2 | 0.00388 | 0.00440 | 0.00530 | 0.00743 |
| A3 | 0.00550 | 0.00621 | 0.00738 | 0.01070 |
| A4 | 0.00424 | 0.00480 | 0.00571 | 0.00812 |

Pin Capacitance (pf)

| Pin | V0 | V1 | V2 | V4 |
|-----|---------|---------|---------|---------|
| A1 | 0.00119 | 0.00134 | 0.00156 | 0.00220 |
| A2 | 0.00311 | 0.00342 | 0.00376 | 0.00573 |
| A3 | 0.00123 | 0.00138 | 0.00163 | 0.00225 |
| A4 | 0.00311 | 0.00348 | 0.00371 | 0.00572 |

Max Leakage Power (uW)

| V0 | V1 | V2 | V4 |
|------------|------------|------------|------------|
| 0.00100900 | 0.00117690 | 0.00140290 | 0.00216270 |

Delay Table (ns)

| Description | V0 | V1 | V2 | V4 |
|-------------|---------|---------|---------|---------|
| A1→Z_FALL | 0.13995 | 0.13331 | 0.13024 | 0.12634 |
| A1→Z_RISE | 0.12713 | 0.12137 | 0.11818 | 0.11588 |
| A2→Z_FALL | 0.10131 | 0.09713 | 0.09627 | 0.09204 |
| A2→Z_RISE | 0.08893 | 0.08539 | 0.08435 | 0.08188 |
| A3→Z_FALL | 0.13695 | 0.13093 | 0.12776 | 0.13120 |
| A3→Z_RISE | 0.13807 | 0.13178 | 0.12823 | 0.13118 |
| A4→Z_FALL | 0.09999 | 0.09602 | 0.09653 | 0.09598 |
| A4→Z_RISE | 0.10058 | 0.09642 | 0.09657 | 0.09531 |