Data Sheet Summary

0.11µm 1.5V Standard Cell Library for CSMC 0.11µm
Eflash 2P8M Salicide Process

DESCRIPTION

As technologies advance into deep sub-micron, a “System-On-Chip (SOC)” design posts great challenge to designers that need high quality standard cell libraries to achieve their design goals.

CSMC’s 0.11µm cell library provides its customers with a cost effective SOC solutions to penetrate computer graphics, telecommunication, and consumer electronic markets. With the library development methodology, each core cell, input/output buffer, or memory macro is constructed from the most up-to-data design rules and electrical parameters.

CSMC offers almost all kinds of packages, including DIP, QFP, LQFP, TQFP, SOJ, SOP, SSOP and so on which can substantially reduce cost and turn-around time.

CSMC’s customers also receive DFT(Design-For-Test) service to ensure a high-quality library during mass production.

FEATURES

- CSMC 0.11um eflash 1P8M Salicide 1.5V Process
- 690 standard core cells – including 46 PMK cells
- Cell high : 2.196µm
- Interval cells optimized for synthesis.
- Accurate timing characterization
- Support most of the EDA tools
- Optimized for Cadence and Synopsys place&route tools.
- High routing density, routability, high speed and low power .
- Routable for 4,5,6, 7 or 8 metals

EDA TOOLS SUPPORT

- Verilog models
- VHDL models
- Synopsys synthesis models
- Composer schematic
- Cadence place & route tools
- Synopsys place & route
- GDSⅡ
- LVS spice netlist

Library Cell List

The CSMC011 internal library supports a rich set of variable functions. It includes the following types of function cells:

ad …….. Full Adder GATES
ah …….. Half Adder GATES
an……AND GATES
antenna……ANTENNA-Fix CELL
aoi …….. AND-NOR GATES
aor…….. AND-OR GATES
bh…….. BUS HOLD CELL
buff……Buffer GATES
buft……..TRI-STATE BUFFER
ckan……Clock AND GATES
ckbuf……Clock BUFFER GATES
ckinv……Clock INVERT GATES
ckmx……Clock Multiplexer
cknd……Clock NAND GATES
cknr……Clock NOR GATES
ckor……Clock OR GATES
ckxn……Clock XNOR GATES
ckxr……Clock Exclusive OR GATES
df/dm…….D Flip-Flop
dl…….Delay GATES
fillcap…….Decoupling CELL
filler ……. Filler CELL GATES
inv0…….INVERTER GATES
invt……..TRI-STATE INVERTER GATES
la……LATCH GATES
mi……Inverting MUX GATES
mx……MUX GATES
nd…….NAND GATES
nr……..NOR GATES
oai……OR-NAND GATES
or……OR GATES
ora……..OR-AND GATES
sd……Scan D Flip-Flop
se……Scan Enable D Flip-Flop
tie……..Drive Output to A Fixed State
tlat……Clock Gating CELL
xn……...XNOR GATES
xr……XOR GATES

STD Cells listed below:

Drive strength capabilites :0<M<1<2<4 <P.. etc

Arithmetic Gates	
ad01dN	1-bit FULL ADDER (0,1,2,3,m)
adfh01dN	1-bit High-speed FULL ADDER (0,1,2)
ah01dN	1-bit Half Adder (0,1,2,3,m)

Buffers Gates

buffdN	Non Inverting(0,1,2,3,4,5,6,7,8,12,16,20,m)
buftdN	Non-inverting 3-state Buffer with active low enable (0,1,2,3,4,6,8,12,16,20,m)
ckbufdN	Clock Non Inverting (0,1,2,3,4,5,6,7,8,10,12,14,16,20,30,40,80,m)
ckanddN	Clock nand2 (0,1,2,4)
ckinvdN	Clock Inverting (0,1,2,3,4,5,6,7,8,10,12,14,16,20,30,40,80)
inv0dN	Inverter (0,1,2,3,4,5,6,7,8, 12, 16, 20,m,p)
invtldN	Inverter 3-state Buffer with active high enable (0,1,2,3,4,6,8,12,16,20,m)
dl01dN	Delay Gate(1,2,m)
dl02dN	Delay Gate(1,2)

COMPLEX Gates

aoi21dN	AND-NOR 2,1 (0,1,2,4,m)
aoi2m1dN	AND-NOR 2,1 1 inv(0,1,2,4)
aoi21mdN	AND-NOR 2,1 NOR1inv (0,1,2,4)
aoi31dN	AND-NOR 3,1 (0,1,2,4,m)
aoi32dN	AND-NOR 3,2 (0,1,2,4,m)
aoi33dN	AND-NOR 3,3 (0,1,2,4)
aoi22dN	AND-NOR2,2 (0,1,2,4,m)
aoi211dN	AND-NOR 2,1,1 (0,1,2,4)
aoi221dN	AND-NOR 2,2,1 (0,1,2,4)
aoi222dN	AND-NOR 2,2,2 (0,1,2,4)
aoim21dN	AND-NOR2,1 2 invt (0,1,2,3,m)
aoim22dN	AND-NOR2,2 2 invt (0,1,2,4,m)
oai21dN	OR-NAND2,1 (0,1,2,4,m)
oai2m1d0	OR-NAND2,1 or 1 inv(0,1,2,4)
oai21md0	OR-NAND2,1 nand 1inv (0,1,2,4)
oai31dN	OR-NAND3,1 (0,1,2,4)
oai32dN	OR-NAND3,2 (0,1,2,4)
oai33dN	OR-NAND3,3 (0,1,2,4)
oai22dN	OR-NAND2,2 (0,1,2,4,m)
oai211dN	OR-NAND2,1,1 (0,1,2,4)

oai221dN	OR-NAND2,2,1 (0,1,2,4)
oai222dN	OR-NAND2,2,2 (0,1,2,4)
oaim21dN	OR-NAND2,1 2 invt (0,1,2,4,m)
oaim22dN	OR-NAND2,2 2 invt (0,1,2,4,m)
aor21dN	AND-OR 2,1 (0,1,2,4)
aor22dN	AND-OR 2,2 (0,1,2,4)
aor211dN	AND-OR 2,1,1(0,1,2,4)
aor221dN	AND-OR 2,2,1 (0,1,2,4)
aor222dN	AND-OR 2,2,2(0,1,2,4)
aor31dN	AND-OR 3,1 (0,1,2,4)
ora211dN	OR -AND 2,1,1 (0,1,2,4)
ora221dN	OR -AND 2,2,1 (0,1,2,4)
ora222dN	OR -AND 2,2,2 (0,1,2,4)
ora21dN	OR -AND 2,1 (0,1,2,4)
ora22dN	OR -AND 2,2 (0,1,2,4)
ora31dN	OR -AND 3,1 (0,1,2,4)

Gates

an02dN	AND 2 input (0,1,1p5,2,2p5,3p5,4,m)
an03dN	AND 3 input (0,1,2,4,m)
an04dN	AND 4 input (0,1,2,4,m)
ckanddN	CLOCK AND 2 input (0,1,2,4)
cknd02dN	CLOCK NAND 2 input (0,1,2,4)
cknr02dN	CLOCK NOR 2 input (0,1,2,4)
ckor02dN	CLOCK OR 2 input (0,1,2,4)
ckxn02dN	CLOCK Excl-NOR 2 input (0,1,2,4)
ckxr02dN	CLOCK Excl-OR 2 input (0,1,2,4)
nd02dN	NAND 2 input (0,1,1.5,2,2.5,3,3.5,m)
nd12dN	NAND 2 input 1 invt (0,1,2,3,m)
nd03dN	NAND 3 input (0,1,2,3)
nd13dN	NAND 3 input 1 invt (0,1,2,3)
nd04dN	NAND 4 input (0,1,2,3)
nd14dN	NAND 4 input 1 invt (0,1,2,3)
nd24dN	NAND 4 input 2 invt (0,1,2,3)
nr02dN	NOR 2 input (0,1,2,4,m)
nr12dN	NOR 2 input 1 inv (0,1,1.5,2,2.5,4,m)
nr03dN	NOR 3 input (0,1,2,4)
nr13dN	NOR 3 input 1 inv (0,1,2,4)
nr04dN	NOR 4 input (0,1,2,4)
nr14dN	NOR 4 input 1 inv (0,1,2,4)
nr24dN	NOR 4 input 2 inv (0,1,2,4)

or02dN	OR 2 input (0,1,1.5,2,2.5,4,4.5,m)
or03dN	OR 3 input (0,1,2,4,m)
or04dN	OR 4 input (0,1,2,4)
xn02dN	Excl-NOR 2 input (0,1,2,4,m)
xn03dN	Excl-NOR 3 input (0,1,2,4,m)
xr02dN	Excl-OR 2 input (0,1,2,4,m)
xr03dN	Excl-OR 3 input (0,1,2,4,m)

MULTIPLEXERS

ckmx02dN	CLOCK Mux 2-to-1 (0,1,2,4)
mx02dN	Mux 2-to-1 (0,1,2,3,m)
mi02dN	Inverting Mux 2-to-1 (0,1,2,3,m)
mx03dN	Mux 3-to-1 (0,1,2,3)
mx04dN	Mux 4-to-1 (0,1,2,3,m)

FLIP FLOPS

denrqN	Pos. Edge Enable DFF, active-high enable , Q only (0,1,2)
dfanrq0	With input NAND2 D0,D1 Pos. Edge DFF, Q only(0,1,2)
dfbfbN	Neg. Edge DFF, preset & clear (0,1,2)
dfbrbN	Pos. Edge DFF, preset & clear (0,1,2,m)
dfbrqN	Pos. Edge DFF, preset & clear, Q only (0,1,2)
dfcfbN	Neg. Edge DFF, clear (0,1,2)
dfcrbN	Pos. Edge DFF, clear (0,1,2,m)
dfcrqN	Pos. Edge DFF, clear, Q only (0,1,2,m)
dfnfbN	Neg. Edge DFF(0,1,2)
dfnfqN	Neg. Edge DFF,Q only (0,1,2)
dfnrbN	Pos. Edge DFF(0,1,2)
dfnrqN	Pos. Edge DFF, Q only(0,1,2)
dfpfbN	Neg. Edge DFF, active-low preset(0,1,2)
dfprbN	Pos. Edge DFF, active-low preset(0,1,2)
dfprqN	Pos. Edge DFF, active-low preset,Q only(0,1,2,m)
dfscrqN	Pos. Edge synchronous DFF, clear, Q only (0,1,2)
dmnrqN	Pos. Edge DFF, Q only (0,1,2) with selected INPUT data D0,D1

LATCHES

labhbN	D latch, active-high enable, preset & clear (0,1,2,3)
lablbN	D latch, active-low enable, preset & clear (0,1,2,3)
lanhbN	D latch, active-high enable (0,1,2,3)
lanlbN	D latch, active-low enable (0,1,2,3)
lachbN	D latch, active-high enable, clear (0,1,2,3)
laclbN	D latch, active-low enable, clear (0,1,2,3)

laphbN	D latch, active-high enable, preset (0,1,2,3)
laplbN	D latch, active-low enable, preset (0,1,2,3)

SCAN FLIP FLOPS

sdanrqN	Pos.Edge Scan DFF, Q only (0,1,2,4,8) with NAND D0,D1 input data
sdbrbN	Pos.Edge Scan DFF, active-low set and clear (0,1,2,m)
sdbfbN	Neg.Edge Scan DFF, active-low set and clear (0,1,2)
sdbrqN	Pos.Edge Scan DFF, active-low set and clear, Q only (0,1,2)
sdcfbN	Neg.Edge Scan DFF, active-low clear (0,1,2)
sdcrbN	Pos.Edge Scan DFF, active-low clear (0,1,2,m)
sdcrqN	Pos.Edge Scan DFF, active-low clear, Q only (0,1,2,m)
sdmnrqN	Pos.Edge Scan DFF, Q only (0,1,2,4,8) With selected input Data D0,D1
sdnfbN	Neg.Edge Scan DFF(0,1,2)
sdnfqN	Neg.Edge Scan DFF, Q only (0,1,2)
sdnrbN	Pos.Edge Scan DFF (0,1,2)
sdnrqN	Pos.Edge Scan DFF, Q only (0,1,2)
sdpfbN	Neg.Edge Scan DFF, active-low preset (0,1,2)
sdprbN	Pos.Edge Scan DFF, active-low preset (0,1,2)
sdprqN	Pos.Edge Scan DFF, active-low preset ,Q only(0,1,2,m)
sdscrqN	Pos.Edge Scan synchronous DFF, clear, Q only (0,1,2)
senrqN	Pos.Edge Scan DFF, active-high enable ,Q only (0,1,2)

CLOCK GATE

tlatncadN	Positive edge-triggered clock-gating latch(0,1,2,4)
tlatnfcadN	Neg. edge-triggered clock-gating latch(0,1,2,4)
tlatntscadN	Positive edge-triggered clock-gating latch, with enable pin (0,1,2,4)
tlatnftscadN	Neg edge-triggered clock-gating latch, with enable pin (0,1,2,4)

MISCELLANEOUS

antenna	Antenna Diode
bh01dN	Three-state bus holder(1)
fillerN	Filler cell(1,2,3,4,6,8,16,32,64)
tiehi	Dirves the output (Y) to Logic High
tielo	Dirves the output (Y) to Logic Low
fillcapN	Decoupling cell(1,2,3,4,6,8,16,32,64)
fillersub	Tap cell
invod8d1	inv with 8 open drain
nd02od	Nand2 with open drain
nd03od	Nand3 with open drain
or02od	Or2 with open drain
pullu	Internal pull up with an enble pin

pulld	Internal pull down with an enble pin

Library Cell List For PMK

drf…… Retention DFF
gpg……Always on
head……Power switch
iso……isolation cells
sdr……Retention Scan DFF

PMK Cells listed below:

Power Switch

headN	Power switch cells

Isolation cells

isohdN	h default “1” in isolation mode(1,2,4,m)
isoldN	l default “1” in isolation mode(1,2,4,m)

Always on

gpgbuffdN	Always on buffer (2,4,8,16,32)
gpgbuffdN	Always on inv (2,4,8,16,32)

Retention Flip Flop

drfcrbN	Pos. Edge retention DFF, with reset (0,1,2,m)
drfnrbN	Pos. Edge retention DFF(0,1,2,m)
drfprbN	Pos. Edge DFF, with set (0,1,2,m)

Retention Flip Flop with Scan

sdrcrbN	Pos. Edge retention DFF, with reset (0,1,2,m)
sdrnrbN	Pos. Edge retention DFF(0,1,2,m)
sdrprbN	Pos. Edge DFF, with set (0,1,2,m)