SMIC 40nm Low Leakage HS LVT Logic Process Standard Cell Library Databook V0.2

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Revision History

This document contains the release history for SMIC 40nm low leakage HS RVT Process Standard Cell Library Databook.

IP Code	Release Version	Date of Release	Update Description
SCC40NLL_HS_LVT	0.0	Oct, 2010	Initial Release
SCC40NLL_HS_LVT	0.1	May, 2011	Update Release： New spice model
SCC40NLL_HS_LVT	0.2	Oct, 2012	Update Release： 1, Enrich cell functions 2, Improve cell performance 3,Optimize cell physical layout 4, New spice model (1.41r)

Table of Contents

Introduction

SMIC's standard cell library is custom-designed and tested to provide the optimum combination of high-performance and high-density cells. Cell optimization is derived from extensive internal and external custom designs and place-and-route analysis; whereas, library optimization is characterized by thorough simulation of library functions and of various drive strengths using leading simulation and place-and-route tools to produce superior GDSII results.

Organization of the databook

The introduction is organized into several sections:

1. Global Parameters provides library overview and some general specifications.
2. Timing Constraint describes what type of timing specification is measured from each cell.
3. Naming Conventions provides standard cells' name conventions.
4. Special Cells defines the various types of special cells in the library.
5. Standard Cell Library Interpretation explains the components in each of the datasheets.

Global Parameters

This section defines the general specifications for the SMIC 40nm Low Leakage HS LVT Process Standard Cell Library. It includes physical cell specifications, electrical specifications, propagation delay specifications, timing specifications, and power calculation.

Physical Cell Specifications

Table 1. shows the physical design cell specification for this standard cell library.

Table 1. Physical Cell Specification

Drawn Gate Length (um)	0.04
Number of Layers of Metal	6,7,8,9 or 10
Layout Grid (um)	0.005
Vertical Pin Grid (um)	0.14n+0.07
Horizontal Pin Grid (um)	0.14n+0.07
Cell power and Ground Rail Width (um)	0.14
Cell Height (um)	1.26
N-well and substrate distance	10.0

Where n is positive integer value. All pins are located with a 0.07um offset to vertical and horizontal pin grids, making place-and-route tools much more efficient.

Note

The library supports designs with six, seven, eight, nine, or ten layers of metal. For different layers of top-level metal, it is possible that a change in the design rules description within the technology file is required, because the top metal has greater minimum width, minimum spacing, and minimum area requirements. Please refer to "40nm Logic Salicide 0.9/1.1/1.2/1.8/2.5V Low Leakage and Generic Design Rule" for more information. It is crucial to define these rules correctly within the technology file for the place-and-route tool to function properly.

Table 2. lists the electrical specifications for this standard cell library.

Table 2. Electrical Specifications

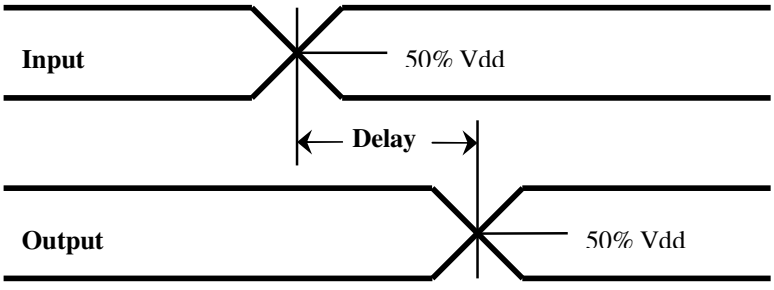
Corners	Best Low Temp	Best High Temp	Best: Zero Temp	Typical	Typical High Temp	Worst Low Temp	Worst High Temp
Supply Voltage (V)	1.21	1.21	1.21	1.10	1.10	0.99	0.99
Junction Temperature (°C)	-40	125	0	25	125	-40	125

Timing Constrains

Propagation Delay and Transition Time

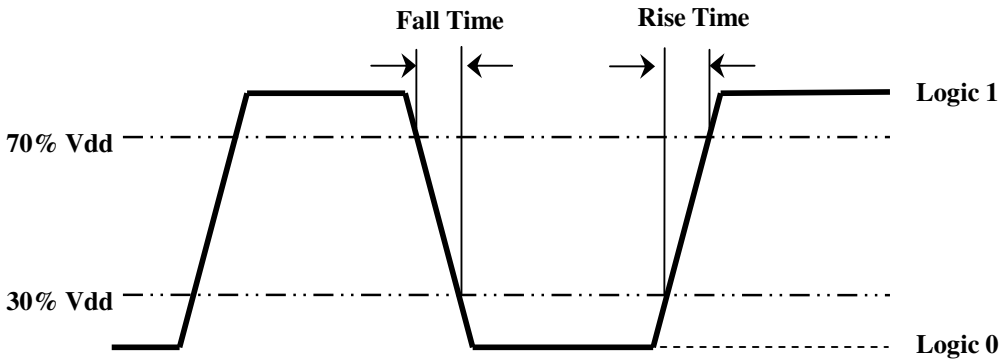
Propagation delay is the sum of the intrinsic delay, the load delay, and the input-slew delay of a cell. Delays are defined as the time interval between the input stimulus and output crossing 50% of the Vdd value. The propagation delay is illustrated in Figure 1. below.

Figure 1. Propagation Delay



Transition time or slew rate is defined as the time interval between crossings of 30% to 70% of Vdd value on a signal. Transition time is shown in Figure 2. for both rising and falling signals.

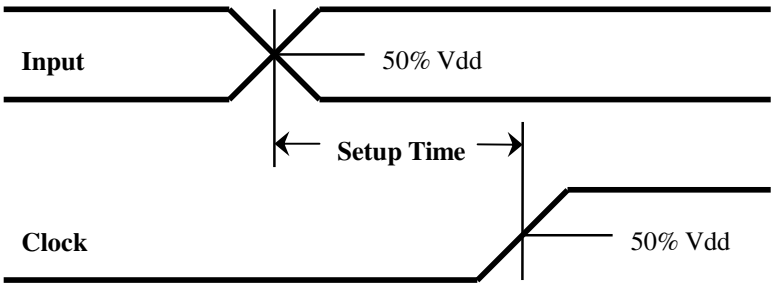
Figure 2. Transition Time



Setup Time

Setup time for a sequential cell is the minimum period of time the data signal must remain stable before the active edge of the clock (or another specified signal) to ensure correct function at the output. Setup constraint values are measured as the interval between the data signal crossing 50% of Vdd for rising or falling data and the clock signal crossing 50% of Vdd for rising or falling clocks. For measurement of setup time, the data signal is kept stable indefinitely after the clock edge. Definition of setup time for a positive-edge triggered sequential cell is shown in Figure 3.

Figure 3. Setup Time

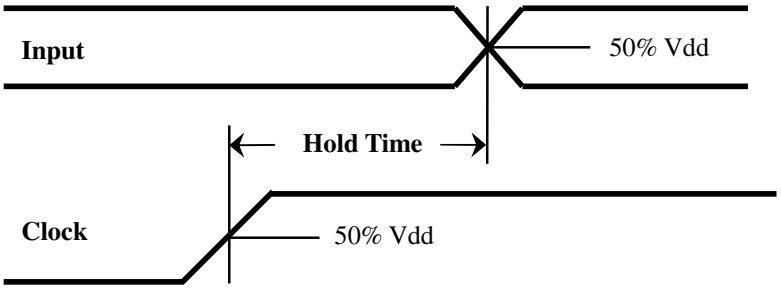


Hold Time

Hold time for a sequential cell is the minimum period of time the data signal must remain stable after the active edge of the clock (or another specified signal) to ensure correct function at the output. Hold constraint values are measured as the interval between the data signal crossing 50% of Vdd value and the clock signal crossing 50% of Vdd for either rise or fall transitions on both signals. For measurement of hold time, the data signal is kept stable indefinitely before the clock

edge. Definition of fall time for a positive-edge triggered sequential cell is shown in Figure 4.

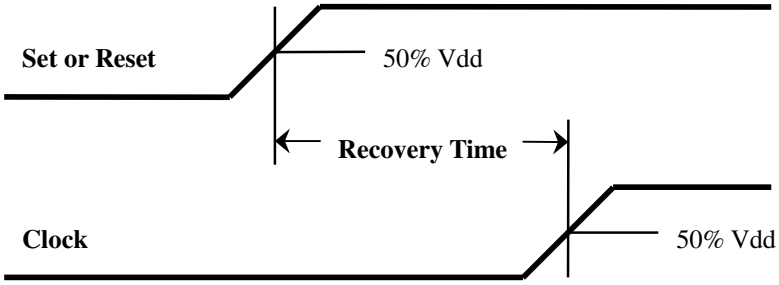
Figure 4. Hold Time



Recovery Time

Recovery time for sequential cell is the minimum length of time that the active-low set or reset signal must remain high before the active edge of the clock to ensure correct cell function. Recovery constraint value is measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd for rising or falling clocks. For measurement of recovery time, the set or reset signal is held stable indefinitely after the clock edge. Definition of recovery time is shown below in Figure 5.

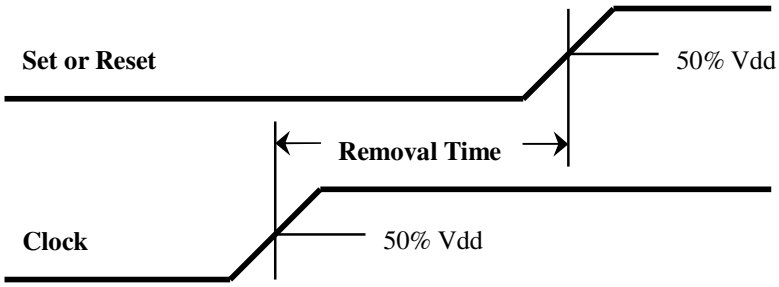
Figure 5. Recovery Time



Removal Time

Removal time for sequential cell is the minimum length of time that the set or reset signals must remain low after the active edge of the clock to ensure correct cell function. Removal constraint value is measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd for rising or falling clocks. For measurement of removal time, the set or reset signal is held stable indefinitely before the clock edge. Definition of removal time is shown in Figure 6.

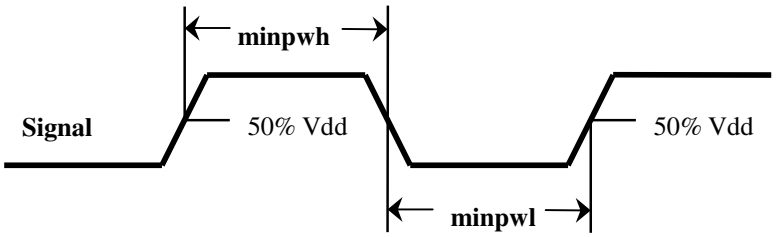
Figure 6. Removal Time



Minimum Pulse Width

Minimum pulse width is the minimum period of time between the leading the trailing edges of a pulse waveform. Minimum pulse width high (minpwh) is measured as the interval between the rising edge of signal crossing 50% of Vdd and the falling edge of signal crossing 50% of Vdd. Minimum pulse width low (minpwl) is measured as the interval between the falling edge of signal crossing 50% of Vdd and the rising edge of signal crossing 50% of Vdd. Minimum pulse width is illustrated in Figure 7.

Figure 7. Minimum Pulse Width



Naming Conventions

This section provides the naming convention for SMIC 40nm Low Leakage Process HS LVT Standard Cell Library.
The syntax is: **<Cell Type><Options> <library family> <Drive Selection>**

Example:

AND2HSV1: AND is Cell Type, 2 is the number of inputs, HS is High-Speed library and V1 is driving strength.

Cell Type	Description	Options
INV	Inverter cell	CKINV :Inverting Clock Inverter TINV: Tri-state inverter
BUF	Buffer cell	CLKBUF: Clock buffer TBUF: Tri-state buffer

AND	AND cell	2/3/4: The number of input pins
NAND	NAND cell	2/3/4: The number of input pins
I2NAND	NAND cell	3/4: with 2 Inverted Inputs
OR	OR cell	2/3/4: The number of input pins
NOR	NOR cell	2/3/4: The number of input pins
AO	AND-OR cell	21/211/221: The number of AND groups and additional inputs
OA	OR-AND cell	21/211/221: The number of OR groups and additional inputs
AOI	AND-OR-Inverter cell	21/211/221: The number of AND groups and additional inputs
OAI	OR-AND-Inverter cell	21/211/221: The number of OR groups and additional inputs
XOR	Exclusive OR cell	2/3:The number of input pins
XNOR	Exclusive NOR cell	2/3:The number of input pins
DEL	Delay cell	1/2/3/4: Delay class
AC	Full adder carry-generator	AC1CIN:with active low carry-in (CIN) AC1CON: with carry in (CI)
AD	Full adder cell	AD1CSCIN: with CO and CIN AD1CON: with CON and CI AD2 provides a carry-select adder function
ADH	Half adder cell	ADH1CIN with CO and CIN ADH1CON with CON and CI
MUX	Multiplexer cell	2/4:The number of input pins N: Inverted
D	Flip-Flop cell	SD: D flip-flop with scan ED: D flip-flop with enable SED: D flip-flop with scan enable DN: Negative edge clock trigger DQ: Output Q only DG: With synchronous (Reset/Set) S: Set R: Reset X: Mux Inputs
LA	Transparent Latch cell	L: Active low enable H: Active high enable CLKLA: Clock-gating latch R: Reset S: Set T: Tri-state transparent latch
HOLD	Weak bus holder	

All cells' names must be in upper case. For flip-flop cells, the default is:

Positive edge clock trigger

Asynchronous Set or Reset

With Q and QN

For latch cells, the default is:

Active high enable

Asynchronous Set or Reset

Special Cells

This section discusses the special cell types within the SMIC Standard Cell Library.

De-CAP Cells

The standard cell library includes 5 De-CAP cells: LVT_FDCAPHS4, LVT_FDCAPHS8, LVT_FDCAPHS16, LVT_FDCAPHS32 and LVT_FDCAPHS64. De-CAP is composed of a PMOS and NMOS device to form decoupling capacitors between V_{DD} and V_{SS} rails so as to reduce the voltage bounce on the power rails. The De-CAP functional schematic is shown in Figure 8. below.

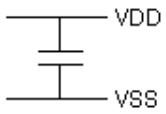


Figure 8. De-CAP Functional Schematic

FILL Cells

The standard cell library includes 5 FILL cells, namely: LVT_F_FILLHS1, LVT_F_FILLHS2, LVT_F_FILLHS4, LVT_F_FILLHS8 and LVT_F_FILLHS16. The number denoted at the end of the cell names represents the width of the cell measured in number of tracks.

The FILL cells are used to connect power and ground rails across an area with no cells during place and route. It is used to ensure that gaps do not occur between well or implant layers which in some cases can cause DRC violations.

PULL0/1 Cells

The LVT_PULLHS0 and LVT_PULLHS1 cells provide ESD protection of signal inputs from power and ground rails. These cells provide diffusion-driven inputs for signal pins. If these cells are not used and Via(s) are dropped on the power rails, DRC error or shorts may occur. Any input pin that will be preset to 0/1 need connect LVT_PULLHS0 / LVT_PULLHS1 cell rather than VSS/VDD.

NWELL and Substrate Tie Cells

The standard cell library contains one NWELL/Substrate Tie Cell: LVT_FILLTIEHS. This standard cell library does not have well or substrate ties inside the cells. It is required to tie NWell to VDD and substrate to VSS before place-and-route using the LVT_FILLTIEHS cells. It is also required to place the Tie cells as frequent as the design requires. Figures 9 and 10 illustrate the two LVT_FILLTIEHS cell orientations within the library.

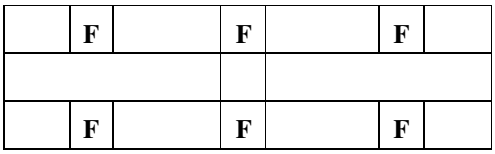


Figure 9. Normal placement of FILLTIE cells

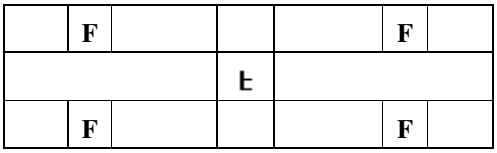


Figure 10. Flipped placement of FILLTIE cells

Figure 9 shows that normal placement of FILLTIEHS cells requires tie cells be placed every 20um. The accurate data please refer to "40nm Logic Salicide 0.9/1.0/1.1/1.2/1.8/2.5V Low leakage and generic ESD and Latch-up Guidelines". All rows except for the top and bottom two have their VDD and VSS shared between the adjacent rows, allowing for wider placement of LVT_FILLTIEHS cells when the cells of alternating rows are placed with an offset, as illustrated above in Figure 10. An example of this would be that the design rule specifies LVT_FILLTIEHS cells every 20um apart; however, with offset for alternating rows, LVT_FILLTIEHS cells can be placed every 40um apart with the exception of the top and bottom rows.

Antenna Cells

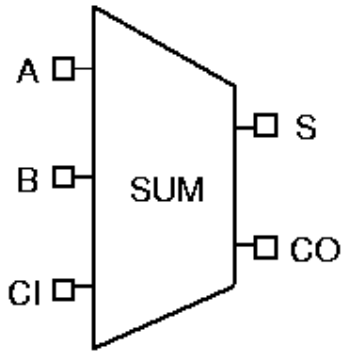
The standard cell library contains 3 F_DIODE cells: LVT_F_DIODEHS2, LVT_F_DIODEHS4 and LVT_F_DIODEHS8. The SMIC antenna effect prevention guideline within the "40nm LOGIC Antenna Ration Effect Generic Prevention Design Guide Rule" specifies the maximum length of wire allowed within the library. During place-and-route, the router may connect wires to the input gates of cells that are longer than the maximum length allowed. In this case, antenna cells can be placed on these inputs. Pin A on the antenna cell connects to two diodes, one reversed-biased from Pin A to ground and another from VDD to Pin A. The Antenna cells will need to be placed manually; fortunately, most place-and-route tools will indicate which nets will require the insertion of these cells.

Standard Cell Datasheet

LVT_AD1HS

Cell Description

1-Bit Full Adder
CO=((A&B)|(A&CI)|(B&CI))
S=(A^B^CI)



Function Table

A	B	CI	CO	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_AD1HSV1	1.26	5.04

Pin Power (uW/MHz)

Pin	V1
A	0.00322
B	0.00259
CI	0.00107

Pin Capacitance (pf)

Pin	V1
A	0.00126
B	0.00184
CI	0.00212

Max Leakage Power (uW)

V1
0.01172992

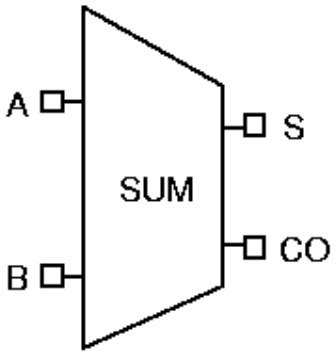
Delay Table (ns)

Description	V1
A→CO_FALL	0.07180
A→CO_RISE	0.06639
B→CO_FALL	0.06552
B→CO_RISE	0.05663
CI→CO_FALL	0.03828
CI→CO_RISE	0.03430
A→S_FALL	0.08817
A→S_RISE	0.08887
B→S_FALL	0.07081
B→S_RISE	0.07101
CI→S_FALL	0.03198
CI→S_RISE	0.03278

LVT_ADH1HS

Cell Description

1-Bit Half Adder
CO=(A&B)
S=(A^B)



Function Table

B	A	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Size

CellName	Height(um)	Width(um)
LVT_ADH1HSV1	1.26	2.94

Pin Power (uW/MHz)

Pin	V1
A	0.00165
B	0.00109

Pin Capacitance (pf)

Pin	V1
A	0.00121
B	0.00186

Max Leakage Power (uW)

V1
0.00914363

Delay Table (ns)

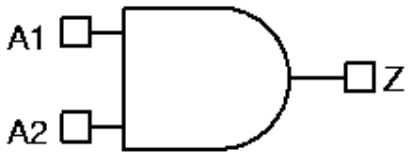
Description	V1
A→CO_FALL	0.02158
A→CO_RISE	0.02689

B→CO_FALL	0.02082
B→CO_RISE	0.02590
A→S_FALL	0.05370
A→S_RISE	0.05022
B→S_FALL	0.03408
B→S_RISE	0.03433

LVT_AND2HS

Cell Description

2-Input AND
Z=(A1&A2)



Function Table

A1	A2	Z
0	X	0
1	0	0
1	1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_AND2HSV1	1.26	0.84
LVT_AND2HSV2	1.26	0.84
LVT_AND2HSV4	1.26	0.98
LVT_AND2HSV8	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2	V4	V8
A1	0.00064	0.00073	0.00112	0.00211
A2	0.00070	0.00079	0.00118	0.00221

Pin Capacitance (pf)

Pin	V1	V2	V4	V8
A1	0.00051	0.00051	0.00050	0.00071
A2	0.00051	0.00051	0.00051	0.00072

Max Leakage Power (uW)

V1	V2	V4	V8
0.00248399	0.00253799	0.00377153	0.01001899

Delay Table (ns)

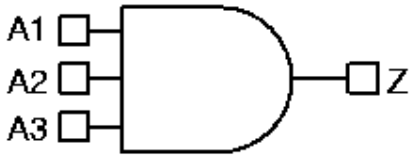
Description	V1	V2	V4	V8

A1→Z_FALL	0.02554	0.02595	0.03073	0.02809
A1→Z_RISE	0.03125	0.03143	0.03640	0.03310
A2→Z_FALL	0.02778	0.02827	0.03275	0.02925
A2→Z_RISE	0.03368	0.03397	0.03884	0.03510

LVT_AND3HS

Cell Description

3-Input AND
Z=(A1&A2&A3)



Function Table

A1	A2	A3	Z
0	X	X	0
1	0	X	0
1	1	0	0
1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_AND3HSV1	1.26	0.98
LVT_AND3HSV2	1.26	0.98
LVT_AND3HSV4	1.26	1.12
LVT_AND3HSV8	1.26	1.54

Pin Power (uW/MHz)

Pin	V1	V2	V4	V8
A1	0.00077	0.00086	0.00124	0.00234
A2	0.00084	0.00093	0.00132	0.00242
A3	0.00092	0.00101	0.00140	0.00252

Pin Capacitance (pf)

Pin	V1	V2	V4	V8
A1	0.00055	0.00055	0.00054	0.00068
A2	0.00058	0.00057	0.00057	0.00072
A3	0.00058	0.00057	0.00058	0.00074

Max Leakage Power (uW)

V1	V2	V4	V8
0.00353044	0.00357246	0.00484030	0.01201869

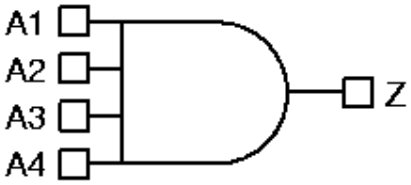
Delay Table (ns)

Description	V1	V2	V4	V8
A1→Z_FALL	0.02988	0.03022	0.03444	0.02951
A1→Z_RISE	0.03297	0.03259	0.03594	0.04570
A2→Z_FALL	0.03226	0.03221	0.03645	0.03027
A2→Z_RISE	0.03542	0.03492	0.03845	0.04828
A3→Z_FALL	0.03533	0.03510	0.03943	0.03200
A3→Z_RISE	0.03777	0.03721	0.04068	0.05051

LVT_AND4HS

Cell Description

4-Input AND
Z=(A1&A2&A3&A4)



Function Table

A1	A2	A3	A4	Z
0	X	X	X	0
1	0	X	X	0
1	1	0	X	0
1	1	1	0	0
1	1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_AND4HSV1	1.26	1.12
LVT_AND4HSV2	1.26	1.12
LVT_AND4HSV4	1.26	1.26
LVT_AND4HSV8	1.26	1.68

Pin Power (uW/MHz)

Pin	V1	V2	V4	V8
A1	0.00080	0.00090	0.00129	0.00253
A2	0.00089	0.00099	0.00138	0.00262
A3	0.00097	0.00107	0.00146	0.00270
A4	0.00106	0.00116	0.00156	0.00280

Pin Capacitance (pf)

Pin	V1	V2	V4	V8
A1	0.00056	0.00056	0.00056	0.00068
A2	0.00061	0.00061	0.00061	0.00073
A3	0.00059	0.00058	0.00058	0.00070
A4	0.00060	0.00060	0.00060	0.00074

Max Leakage Power (uW)

V1	V2	V4	V8
0.00437759	0.00447665	0.00569856	0.01484889

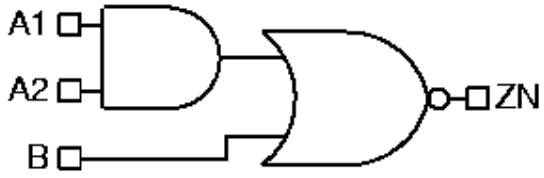
Delay Table (ns)

Description	V1	V2	V4	V8
A1→Z_FALL	0.03123	0.03162	0.03579	0.03032
A1→Z_RISE	0.03672	0.03680	0.04035	0.05840
A2→Z_FALL	0.03429	0.03456	0.03828	0.03140
A2→Z_RISE	0.04098	0.04103	0.04462	0.06271
A3→Z_FALL	0.03673	0.03707	0.04056	0.03241
A3→Z_RISE	0.04336	0.04338	0.04681	0.06488
A4→Z_FALL	0.04005	0.04042	0.04386	0.03400
A4→Z_RISE	0.04605	0.04604	0.04951	0.06767

LVT_AOI21HS

Cell Description

2-1 AOI
ZN=(!((A1&A2)|B))



Function Table

A1	A2	B	ZN
0	X	0	1
0	X	1	0
1	0	0	1
1	0	1	0
1	1	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_AOI21HSV1	1.26	0.84
LVT_AOI21HSV2	1.26	0.84

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00042	0.00052
A2	0.00048	0.00060
B	0.00027	0.00034

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00056	0.00067
A2	0.00061	0.00074
B	0.00054	0.00065

Max Leakage Power (uW)

V1	V2
0.00236669	0.00255267

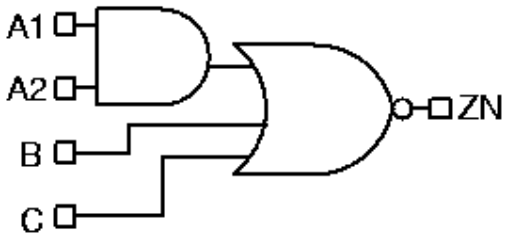
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.01612	0.01443
A1→ZN_RISE	0.02475	0.02171
A2→ZN_FALL	0.01742	0.01575
A2→ZN_RISE	0.02729	0.02443
B→ZN_FALL	0.00907	0.00821
B→ZN_RISE	0.01891	0.01664

LVT_AOI211HS

Cell Description

2-1-1 AOI
ZN=(!((A1&A2)|B|C))



Function Table

A1	A2	B	C	ZN
0	X	0	0	1
0	X	0	1	0
0	X	1	X	0
1	0	0	0	1
1	0	0	1	0
1	0	1	X	0
1	1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_AOI211HSV1	1.26	0.98
LVT_AOI211HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00054	0.00067
A2	0.00060	0.00076
B	0.00040	0.00050
C	0.00033	0.00040

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00055	0.00067
A2	0.00061	0.00075
B	0.00059	0.00071
C	0.00052	0.00063

Max Leakage Power (uW)

V1	V2
0.00345774	0.00375070

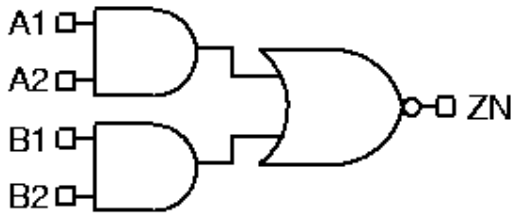
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.01790	0.01582
A1→ZN_RISE	0.04014	0.03490
A2→ZN_FALL	0.01924	0.01730
A2→ZN_RISE	0.04416	0.03939
B→ZN_FALL	0.01047	0.00951
B→ZN_RISE	0.03410	0.02994
C→ZN_FALL	0.00979	0.00878
C→ZN_RISE	0.03036	0.02589

LVT_AOI22HS

Cell Description

2-2 AOI
ZN=(!((A1&A2)|(B1&B2)))



Function Table

A1	A2	B1	B2	ZN
0	X	0	X	1
0	X	1	0	1
0	X	1	1	0
1	0	0	X	1
1	0	1	0	1
1	0	1	1	0
1	1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_AOI22HSV1	1.26	0.98
LVT_AOI22HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00053	0.00067
A2	0.00059	0.00076
B1	0.00030	0.00037
B2	0.00035	0.00045

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00056	0.00067
A2	0.00061	0.00073
B1	0.00055	0.00066
B2	0.00054	0.00065

Max Leakage Power (uW)

V1	V2
0.00274383	0.00391772

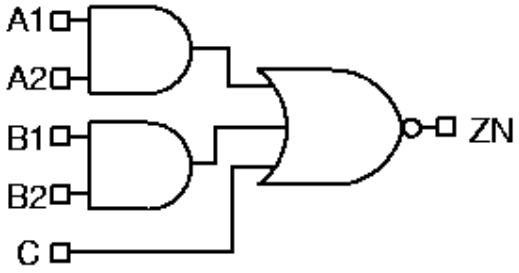
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.01807	0.01640
A1→ZN_RISE	0.02684	0.02391
A2→ZN_FALL	0.01945	0.01792
A2→ZN_RISE	0.02953	0.02677
B1→ZN_FALL	0.01357	0.01217
B1→ZN_RISE	0.01901	0.01669
B2→ZN_FALL	0.01488	0.01350
B2→ZN_RISE	0.02170	0.01934

LVT_AOI221HS

Cell Description

2-2-1 AOI
ZN=(!((A1&A2)|(B1&B2)|C))



Function Table

A1	A2	B1	B2	C	ZN
0	X	0	X	0	1
0	X	0	X	1	0
0	X	1	0	0	1
0	X	1	0	1	0
0	X	1	1	X	0
1	0	0	X	0	1
1	0	0	X	1	0
1	0	1	0	0	1
1	0	1	0	1	0
1	0	1	1	X	0
1	1	X	X	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_AOI221HSV1	1.26	1.26
LVT_AOI221HSV2	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00069	0.00088
A2	0.00075	0.00096
B1	0.00050	0.00063
B2	0.00056	0.00071
C	0.00036	0.00045

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00057	0.00067
A2	0.00061	0.00073

B1	0.00056	0.00067
B2	0.00056	0.00067
C	0.00054	0.00065

Max Leakage Power (uW)

V1	V2
0.00307180	0.00334228

Delay Table (ns)

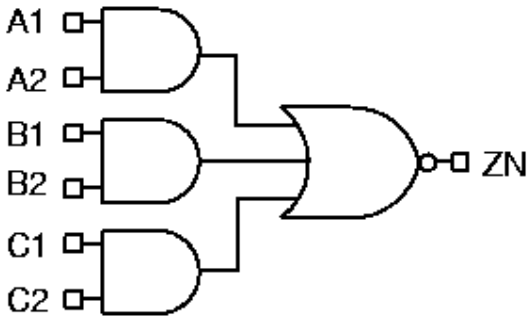
Description	V1	V2
A1→ZN_FALL	0.01945	0.01755
A1→ZN_RISE	0.04684	0.04210
A2→ZN_FALL	0.02079	0.01912
A2→ZN_RISE	0.05114	0.04679
B1→ZN_FALL	0.01776	0.01603
B1→ZN_RISE	0.04043	0.03606
B2→ZN_FALL	0.01943	0.01770
B2→ZN_RISE	0.04546	0.04104
C→ZN_FALL	0.01014	0.00928
C→ZN_RISE	0.03050	0.02693

LVT_AOI222HS

Cell Description

2-2-2 AOI

ZN=(!((A1&A2)|(B1&B2)|(C1&C2)))



Function Table

A1	A2	B1	B2	C1	C2	ZN
0	X	0	X	0	X	1
0	X	0	X	1	0	1
0	X	0	X	1	1	0
0	X	1	0	0	X	1
0	X	1	0	1	0	1
0	X	1	0	1	1	0
0	X	1	1	X	X	0
1	0	0	X	0	X	1
1	0	0	X	1	0	1
1	0	0	X	1	1	0
1	0	1	0	0	X	1
1	0	1	0	1	0	1
1	0	1	0	1	1	0
1	0	1	1	X	X	0
1	1	X	X	X	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_AOI222HSV1	1.26	1.54
LVT_AOI222HSV2	1.26	1.54

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00039	0.00048
A2	0.00044	0.00056
B1	0.00061	0.00077
B2	0.00067	0.00085
C1	0.00080	0.00101
C2	0.00086	0.00110

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00053	0.00063
A2	0.00052	0.00064
B1	0.00059	0.00070
B2	0.00055	0.00066
C1	0.00055	0.00066
C2	0.00060	0.00073

Max Leakage Power (uW)

V1	V2
0.00320322	0.00348049

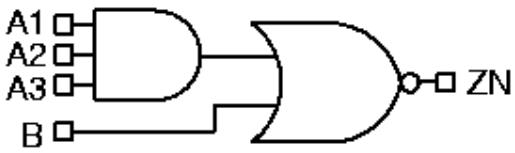
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.01561	0.01375
A1→ZN_RISE	0.03016	0.02615
A2→ZN_FALL	0.01652	0.01491
A2→ZN_RISE	0.03269	0.02916
B1→ZN_FALL	0.02015	0.01807
B1→ZN_RISE	0.04376	0.03888
B2→ZN_FALL	0.02156	0.01952
B2→ZN_RISE	0.04800	0.04325
C1→ZN_FALL	0.02175	0.01956
C1→ZN_RISE	0.04983	0.04464
C2→ZN_FALL	0.02317	0.02108
C2→ZN_RISE	0.05380	0.04891

LVT_AOI31HS

Cell Description

3-1 AOI
ZN=(!((A1&A2&A3)|B))



Function Table

A1	A2	A3	B	ZN
0	X	X	0	1
0	X	X	1	0
1	0	X	0	1
1	0	X	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_AOI31HSV1	1.26	0.98
LVT_AOI31HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00043	0.00053
A2	0.00049	0.00062
A3	0.00055	0.00069
B	0.00029	0.00035

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00058	0.00067
A2	0.00059	0.00070
A3	0.00061	0.00075
B	0.00054	0.00065

Max Leakage Power (uW)

V1	V2
0.00234694	0.00288472

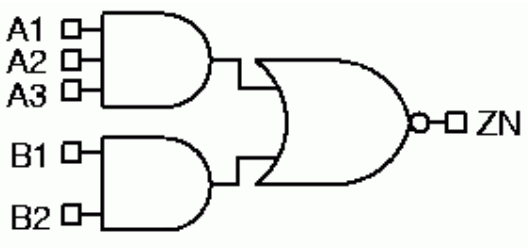
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.02239	0.01956
A1→ZN_RISE	0.02524	0.02179
A2→ZN_FALL	0.02467	0.02223
A2→ZN_RISE	0.02776	0.02466
A3→ZN_FALL	0.02576	0.02336
A3→ZN_RISE	0.03018	0.02697
B→ZN_FALL	0.00912	0.00816
B→ZN_RISE	0.01845	0.01599

LVT_AOI32HS

Cell Description

3-2 AOI
ZN=(!((A1&A2&A3)|(B1&B2)))



Function Table

A1	A2	A3	B1	B2	ZN
0	X	X	0	X	1
0	X	X	1	0	1
0	X	X	1	1	0
1	0	X	0	X	1
1	0	X	1	0	1
1	0	X	1	1	0
1	1	0	0	X	1
1	1	0	1	0	1
1	1	0	1	1	0
1	1	1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_AOI32HSV1	1.26	1.12
LVT_AOI32HSV2	1.26	1.12

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00053	0.00067
A2	0.00059	0.00076
A3	0.00064	0.00083
B1	0.00031	0.00039
B2	0.00038	0.00048

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00056	0.00067
A2	0.00063	0.00076
A3	0.00062	0.00074

B1	0.00055	0.00069
B2	0.00054	0.00063

Max Leakage Power (uW)

V1	V2
0.00268393	0.00402434

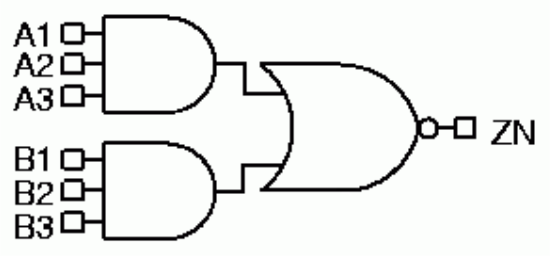
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.02498	0.02248
A1→ZN_RISE	0.02674	0.02378
A2→ZN_FALL	0.02769	0.02551
A2→ZN_RISE	0.02946	0.02668
A3→ZN_FALL	0.02877	0.02656
A3→ZN_RISE	0.03200	0.02905
B1→ZN_FALL	0.01360	0.01213
B1→ZN_RISE	0.01853	0.01625
B2→ZN_FALL	0.01526	0.01370
B2→ZN_RISE	0.02145	0.01891

LVT_AOI33HS

Cell Description

3-3 AOI
ZN=(!((A1&A2&A3)|(B1&B2&B3)))



Function Table

A1	A2	A3	B1	B2	B3	ZN
0	X	X	0	X	X	1
0	X	X	1	0	X	1
0	X	X	1	1	0	1
0	X	X	1	1	1	0
1	0	X	0	X	X	1
1	0	X	1	0	X	1
1	0	X	1	1	0	1
1	0	X	1	1	1	0
1	1	0	0	X	X	1
1	1	0	1	0	X	1
1	1	0	1	1	0	1
1	1	0	1	1	1	0
1	1	1	X	X	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_AOI33HSV1	1.26	1.40
LVT_AOI33HSV2	1.26	1.40

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00065	0.00082
A2	0.00071	0.00090
A3	0.00077	0.00098
B1	0.00040	0.00049
B2	0.00047	0.00059
B3	0.00053	0.00067

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00057	0.00068
A2	0.00064	0.00070
A3	0.00060	0.00073
B1	0.00054	0.00065
B2	0.00054	0.00065
B3	0.00054	0.00065

Max Leakage Power (uW)

V1	V2
0.00459800	0.00653072

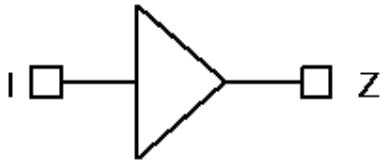
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.02920	0.02640
A1→ZN_RISE	0.02922	0.02600
A2→ZN_FALL	0.03175	0.02897
A2→ZN_RISE	0.03160	0.02843
A3→ZN_FALL	0.03276	0.03008
A3→ZN_RISE	0.03369	0.03051
B1→ZN_FALL	0.02054	0.01803
B1→ZN_RISE	0.02086	0.01825
B2→ZN_FALL	0.02379	0.02132
B2→ZN_RISE	0.02381	0.02116
B3→ZN_FALL	0.02500	0.02248
B3→ZN_RISE	0.02606	0.02332

LVT_BUFHS

Cell Description

Non-Inverting Buffer
Z=I



Function Table

I	Z
0	0
1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_BUFHSV1	1.26	0.56
LVT_BUFHSV2	1.26	0.56
LVT_BUFHSV3	1.26	0.84
LVT_BUFHSV4	1.26	0.84
LVT_BUFHSV6	1.26	0.98
LVT_BUFHSV8	1.26	1.26
LVT_BUFHSV12	1.26	1.82
LVT_BUFHSV16	1.26	2.24
LVT_BUFHSV20	1.26	2.80
LVT_BUFHSV24	1.26	3.36

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
I	0.00062	0.00072	0.00095	0.00113	0.00163	0.00205	0.00309	0.00403

Pin	V20	V24
I	0.00498	0.00602

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
I	0.00053	0.00053	0.00058	0.00063	0.00074	0.00123	0.00172	0.00200

Pin	V20	V24
I	0.00267	0.00331

Max Leakage Power (uW)

V1	V2	V3	V4	V6	V8	V12	V16
0.00149061	0.00163288	0.00376993	0.00453275	0.00706404	0.01083884	0.01836302	0.02542359

V20	V24
0.03380040	0.04152418

Delay Table (ns)

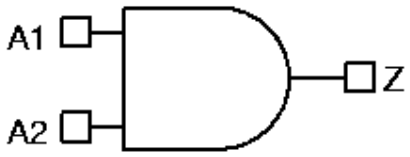
Description	V1	V2	V3	V4	V6	V8	V12	V16
I→Z_FALL	0.02549	0.02620	0.02439	0.02290	0.02465	0.02017	0.02019	0.02068
I→Z_RISE	0.02302	0.02286	0.02050	0.01976	0.02052	0.01742	0.01716	0.01738

Description	V20	V24
I→Z_FALL	0.01963	0.01945
I→Z_RISE	0.01665	0.01657

LVT_CLKAND2HS

Cell Description

2-Input Clock AND
Z=(A1&A2)



Function Table

A1	A2	Z
0	X	0
1	0	0
1	1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_CLKAND2HSV1	1.26	0.84
LVT_CLKAND2HSV2	1.26	0.84
LVT_CLKAND2HSV4	1.26	1.12
LVT_CLKAND2HSV8	1.26	1.68

Pin Power (uW/MHz)

Pin	V1	V2	V4	V8
A1	0.00066	0.00076	0.00143	0.00297
A2	0.00076	0.00086	0.00153	0.00307

Pin Capacitance (pf)

Pin	V1	V2	V4	V8
A1	0.00061	0.00059	0.00058	0.00059
A2	0.00059	0.00060	0.00059	0.00059

Max Leakage Power (uW)

V1	V2	V4	V8
0.00238998	0.00281620	0.00665239	0.01487073

Delay Table (ns)

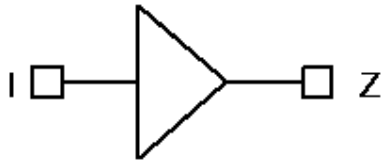
Description	V1	V2	V4	V8

A1→Z_FALL	0.02748	0.02797	0.03797	0.05629
A1→Z_RISE	0.02255	0.02216	0.02523	0.03504
A2→Z_FALL	0.03113	0.03177	0.04116	0.05895
A2→Z_RISE	0.02464	0.02421	0.02721	0.03699

LVT_CLKBUFHS

Cell Description

Clock Buffer with Balanced Rise/Fall Time
Z=I



Function Table

I	Z
0	0
1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_CLKBUFHSV1	1.26	0.56
LVT_CLKBUFHSV2	1.26	0.56
LVT_CLKBUFHSV3	1.26	0.84
LVT_CLKBUFHSV4	1.26	0.84
LVT_CLKBUFHSV6	1.26	0.98
LVT_CLKBUFHSV8	1.26	1.26
LVT_CLKBUFHSV12	1.26	1.68
LVT_CLKBUFHSV16	1.26	2.24
LVT_CLKBUFHSV20	1.26	2.80
LVT_CLKBUFHSV24	1.26	3.08

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
I	0.00062	0.00070	0.00094	0.00111	0.00153	0.00185	0.00270	0.00349

Pin	V20	V24
I	0.00455	0.00525

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
I	0.00053	0.00053	0.00062	0.00068	0.00070	0.00101	0.00130	0.00170

Pin	V20	V24
I	0.00225	0.00245

Max Leakage Power (uW)

V1	V2	V3	V4	V6	V8	V12	V16
0.00145588	0.00164282	0.00416781	0.00501393	0.00723452	0.00968382	0.01757344	0.02296167

V20	V24
0.03024714	0.03703531

Delay Table (ns)

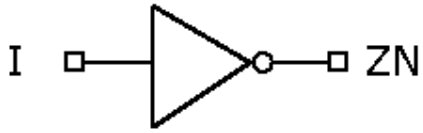
Description	V1	V2	V3	V4	V6	V8	V12	V16
I→Z_FALL	0.02628	0.02665	0.02228	0.02120	0.02428	0.02176	0.02128	0.02120
I→Z_RISE	0.02285	0.02242	0.02039	0.01871	0.02192	0.01994	0.01960	0.02071

Description	V20	V24
I→Z_FALL	0.02074	0.02138
I→Z_RISE	0.02047	0.02042

LVT_CLKNHS

Cell Description

Inverting Clock Buffer with Balanced Rise/Fall Time
ZN=(!I)



Function Table

I	ZN
0	1
1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_CLKNHSV1	1.26	0.42
LVT_CLKNHSV2	1.26	0.42
LVT_CLKNHSV3	1.26	0.56
LVT_CLKNHSV4	1.26	0.56
LVT_CLKNHSV6	1.26	0.84
LVT_CLKNHSV8	1.26	0.98
LVT_CLKNHSV12	1.26	1.26
LVT_CLKNHSV16	1.26	1.68
LVT_CLKNHSV20	1.26	2.10
LVT_CLKNHSV24	1.26	2.38

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
I	0.00020	0.00024	0.00030	0.00033	0.00057	0.00065	0.00095	0.00121

Pin	V20	V24
I	0.00150	0.00185

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
I	0.00057	0.00067	0.00105	0.00120	0.00173	0.00218	0.00331	0.00438

Pin	V20	V24
I	0.00541	0.00649

Max Leakage Power (uW)

V1	V2	V3	V4	V6	V8	V12	V16
0.00094292	0.00116272	0.00212648	0.00253653	0.00561979	0.00761807	0.01258146	0.01931775

V20	V24
0.02521548	0.03156305

Delay Table (ns)

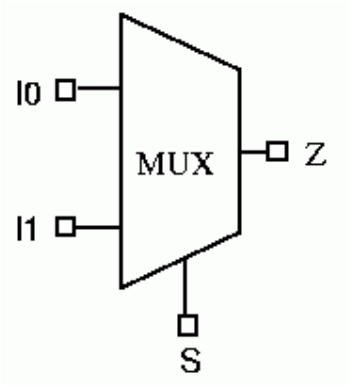
Description	V1	V2	V3	V4	V6	V8	V12	V16
I→ZN_FALL	0.00914	0.00829	0.00681	0.00651	0.00643	0.00631	0.00610	0.00586
I→ZN_RISE	0.01111	0.00974	0.00804	0.00746	0.00721	0.00650	0.00624	0.00604

Description	V20	V24
I→ZN_FALL	0.00596	0.00618
I→ZN_RISE	0.00623	0.00641

LVT_CKMUX2HS

Cell Description

2-to-1 Multiplexer
Z=((I0&(!S))|(I1&S))



Function Table

S	I0	I1	Z
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_CKMUX2HSV1	1.26	1.82
LVT_CKMUX2HSV2	1.26	1.82

Pin Power (uW/MHz)

Pin	V1	V2
I0	0.00105	0.00113
I1	0.00110	0.00118
S	0.00114	0.00122

Pin Capacitance (pf)

Pin	V1	V2
I0	0.00063	0.00063
I1	0.00065	0.00065
S	0.00102	0.00106

Max Leakage Power (uW)

V1	V2
0.00548702	0.00567911

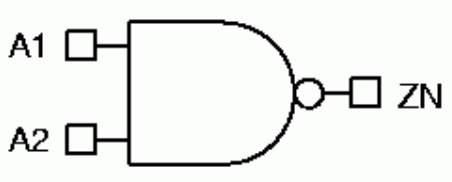
Delay Table (ns)

Description	V1	V2
I0→Z_FALL	0.04040	0.04001
I0→Z_RISE	0.03125	0.03093
I1→Z_FALL	0.04312	0.04269
I1→Z_RISE	0.03128	0.03096
S→Z_FALL	0.03405	0.03392
S→Z_RISE	0.03059	0.03043

LVT_CLKNAND2HS

Cell Description

2-Input NAND
ZN=(!(A1&A2))



Function Table

A1	A2	ZN
0	X	1
1	0	1
1	1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_CLKNAND2HSV1	1.26	0.56
LVT_CLKNAND2HSV2	1.26	0.56
LVT_CLKNAND2HSV3	1.26	0.98
LVT_CLKNAND2HSV4	1.26	0.98
LVT_CLKNAND2HSV8	1.26	1.68

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V8
A1	0.00027	0.00031	0.00042	0.00057	0.00103
A2	0.00034	0.00039	0.00062	0.00081	0.00148

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V8
A1	0.00060	0.00068	0.00100	0.00119	0.00226
A2	0.00064	0.00072	0.00102	0.00121	0.00234

Max Leakage Power (uW)

V1	V2	V3	V4	V8
0.00191825	0.00257743	0.00600634	0.00751379	0.01907642

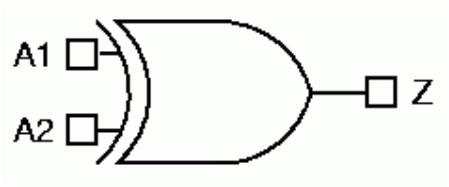
Delay Table (ns)

Description	V1	V2	V3	V4	V8
A1→ZN_FALL	0.01160	0.01155	0.01012	0.01004	0.00898
A1→ZN_RISE	0.01242	0.01071	0.00904	0.00895	0.00793
A2→ZN_FALL	0.01265	0.01275	0.01247	0.01234	0.01105
A2→ZN_RISE	0.01367	0.01181	0.01074	0.01053	0.00940

LVT_CLKXOR2HS

Cell Description

2-Input Exclusive OR
Z=(A1^A2)



Function Table

A2	A1	Z
0	0	0
0	1	1
1	0	1
1	1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_CLKXOR2HSV1	1.26	1.96
LVT_CLKXOR2HSV2	1.26	1.96

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00120	0.00128
A2	0.00202	0.00211

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00120	0.00120
A2	0.00072	0.00071

Max Leakage Power (uW)

V1	V2
0.00517060	0.00514396

Delay Table (ns)

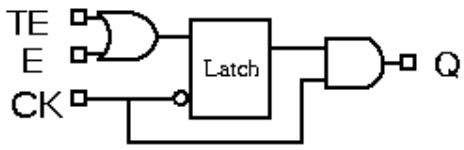
Description	V1	V2
A1→Z_FALL	0.03258	0.03288

A1→Z_RISE	0.03139	0.03087
A2→Z_FALL	0.05220	0.05285
A2→Z_RISE	0.04537	0.04506

LVT_CLKLANQHS

Cell Description

pre-controlled positiveedge triggered clock-gating latch for Low Power Design
IQ=!CK ? (TE|E)
Q=IQ&CK



Function Table

CK<1>	CK	TE	E	Q
0	1	0	0	0
0	1	0	1	1
0	1	1	X	1
0	0	X	X	0
1	1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_CLKLANQHSV1	1.26	2.94
LVT_CLKLANQHSV2	1.26	2.94
LVT_CLKLANQHSV3	1.26	3.08
LVT_CLKLANQHSV4	1.26	3.08
LVT_CLKLANQHSV6	1.26	3.36
LVT_CLKLANQHSV8	1.26	3.50
LVT_CLKLANQHSV12	1.26	3.92
LVT_CLKLANQHSV16	1.26	4.06
LVT_CLKLANQHSV20	1.26	4.48
LVT_CLKLANQHSV24	1.26	4.90

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
CK	0.00138	0.00139	0.00137	0.00136	0.00136	0.00138	0.00136	0.00138
E	0.00033	0.00033	0.00032	0.00032	0.00032	0.00033	0.00032	0.00032
Q	0.00113	0.00125	0.00143	0.00158	0.00205	0.00253	0.00370	0.00504
TE	0.00036	0.00036	0.00035	0.00035	0.00036	0.00036	0.00036	0.00036

Pin	V20	V24
CK	0.00138	0.00137
E	0.00032	0.00033
Q	0.00664	0.00857

TE	0.00036	0.00036

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
CK	0.00052	0.00053	0.00053	0.00054	0.00051	0.00052	0.00050	0.00052
E	0.00055	0.00055	0.00055	0.00055	0.00055	0.00055	0.00055	0.00056
TE	0.00054	0.00054	0.00054	0.00054	0.00056	0.00056	0.00056	0.00057

Pin	V20	V24
CK	0.00052	0.00053
E	0.00056	0.00056
TE	0.00057	0.00056

Max Leakage Power (uW)

V1	V2	V3	V4	V6	V8	V12	V16
0.00719259	0.00757311	0.00859963	0.00907673	0.01082110	0.01341251	0.01930878	0.02501019

V20	V24
0.03133542	0.03816639

Delay Table (ns)

Description	V1	V2	V3	V4	V6	V8	V12	V16
CK→Q_FALL	0.06091	0.06085	0.06096	0.06219	0.06533	0.06826	0.07474	0.08414
CK→Q_RISE	0.06174	0.06161	0.06160	0.06255	0.06580	0.07086	0.07904	0.08862

Description	V20	V24
CK→Q_FALL	0.09126	0.09624
CK→Q_RISE	0.09726	0.10507

Timing Constraints (ns)

Pin	Requirement	V1	V2	V3	V4	V6	V8
E	hold_FALL→CK	-0.03149	-0.02862	-0.02861	-0.02861	-0.02861	-0.02861
E	hold_RISE→CK	-0.01431	-0.01431	-0.01432	-0.01432	-0.01431	-0.01431
E	setup_FALL→CK	0.03436	0.03434	0.03434	0.03436	0.03721	0.03721
E	setup_RISE→CK	0.01718	0.01718	0.01720	0.01718	0.01717	0.01719
TE	hold_FALL→CK	-0.03434	-0.03149	-0.03149	-0.03148	-0.03149	-0.03149
TE	hold_RISE→CK	-0.01432	-0.01432	-0.01432	-0.01432	-0.01431	-0.01432
TE	setup_FALL→CK	0.03721	0.03722	0.03722	0.03720	0.04008	0.04008
TE	setup_RISE→CK	0.01717	0.02004	0.02005	0.02005	0.02004	0.02004
CK	minpwl	0.06103	0.06102	0.06103	0.06105	0.06104	0.06264

Pin	Requirement	V12	V16	V20	V24
E	hold_FALL→CK	-0.02575	-0.02289	-0.02289	-0.02861

E	hold_RISE→CK	-0.01432	-0.02578	-0.02578	-0.01432
E	setup_FALL→CK	0.03435	0.03148	0.03148	0.03722
E	setup_RISE→CK	0.01720	0.03149	0.03149	0.01719
TE	hold_FALL→CK	-0.02864	-0.02576	-0.02576	-0.03149
TE	hold_RISE→CK	-0.01432	-0.02864	-0.02864	-0.01432
TE	setup_FALL→CK	0.03721	0.03721	0.03722	0.04008
TE	setup_RISE→CK	0.02006	0.03436	0.03436	0.02004
CK	minpwl	0.06104	0.06901	0.07057	0.06420

LVT_DELHS

Cell Description

Delay cell
Z=I

Function Table

I	Z
0	0
1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_DELHS2	1.26	1.54

Pin Power (uW/MHz)

Pin	LVT_DELHS2
I	0.00181

Pin Capacitance (pf)

Pin	LVT_DELHS2
I	0.00050

Max Leakage Power (uW)

LVT_DELHS2
0.00212140

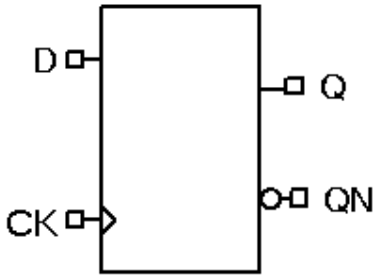
Delay Table (ns)

Description	LVT_DELHS2
I→Z_FALL	0.09654
I→Z_RISE	0.09597

LVT_DHS

Cell Description

D Flip-Flop
Q = rising (CK) ? D : pre_Q
QN = !Q



Function Table

CK<1>	CK	D	Q
0	0	X	Q<1>
0	1	0	0
0	1	1	1
1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_DHSV1	1.26	3.22
LVT_DHSV2	1.26	3.22

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00141	0.00141
D	0.00052	0.00052
Q	0.00092	0.00103
QN	0.00093	0.00104

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00047	0.00047
D	0.00056	0.00056

Max Leakage Power (uW)

V1	V2
0.00597979	0.00671760

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.08354	0.08367
CK→Q_RISE	0.08167	0.08282
CK→QN_FALL	0.06259	0.06167
CK→QN_RISE	0.06578	0.06478

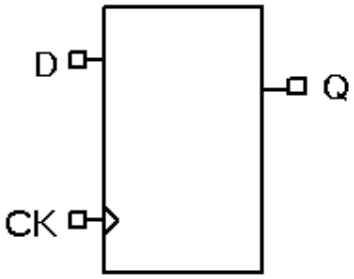
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.00000	0.00287
D	hold_RISE→CK	-0.00573	-0.00573
D	setup_FALL→CK	0.01432	0.01432
D	setup_RISE→CK	0.01146	0.01433
CK	minpwh	0.06501	0.06822
CK	minpwl	0.06975	0.06975

LVT_DQHS

Cell Description

D Flip-Flop, Single Output
Q = rising (CK) ? D : pre_Q



Function Table

CK<1>	CK	D	Q
0	0	X	Q<1>
0	1	0	0
0	1	1	1
1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_DQHSV1	1.26	2.94
LVT_DQHSV2	1.26	2.94

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00136	0.00136
D	0.00051	0.00052
Q	0.00141	0.00151

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00048	0.00048
D	0.00059	0.00060

Max Leakage Power (uW)

V1	V2
0.00529539	0.00541182

Delay Table (ns)

Description	V1	V2

CK→Q_FALL	0.07396	0.07357
CK→Q_RISE	0.07095	0.07066

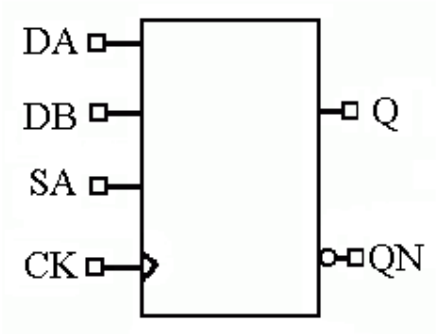
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.00000	-0.00000
D	hold_RISE→CK	-0.00287	-0.00287
D	setup_FALL→CK	0.01430	0.01430
D	setup_RISE→CK	0.01145	0.01145
CK	minpwh	0.04598	0.04598
CK	minpwl	0.06580	0.06581

LVT_DXHS

Cell Description

D Flip-Flop with Mux Inputs
Q = rising (CK) ? (DA&SA|DB&!SA) : pre_Q
QN = !Q



Function Table

CK<1>	CK	SA	DB	DA	Q
0	0	X	X	X	Q<1>
0	1	0	0	X	0
0	1	0	1	X	1
0	1	1	X	0	0
0	1	1	X	1	1
1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_DXHSV1	1.26	4.20
LVT_DXHSV2	1.26	4.20

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00155	0.00156
DA	0.00038	0.00038
DB	0.00034	0.00034
Q	0.00093	0.00103
QN	0.00094	0.00104
SA	0.00068	0.00068

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00047	0.00047
DA	0.00042	0.00042
DB	0.00049	0.00050
SA	0.00098	0.00098

Max Leakage Power (uW)

V1	V2
0.00684949	0.00713958

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.08535	0.08605
CK→Q_RISE	0.08399	0.08611
CK→QN_FALL	0.06391	0.06475
CK→QN_RISE	0.07043	0.06944

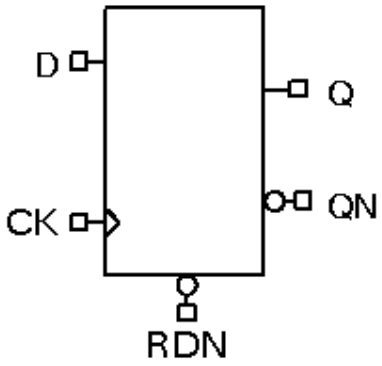
Timing Constraints (ns)

Pin	Requirement	V1	V2
DA	hold_FALL→CK	-0.01718	-0.01431
DA	hold_RISE→CK	-0.02864	-0.02864
DA	setup_FALL→CK	0.04294	0.04293
DA	setup_RISE→CK	0.04296	0.04580
DB	hold_FALL→CK	-0.01144	-0.00858
DB	hold_RISE→CK	-0.02577	-0.02577
DB	setup_FALL→CK	0.04007	0.04008
DB	setup_RISE→CK	0.03722	0.04009
SA	hold_FALL→CK	-0.04006	-0.04008
SA	hold_RISE→CK	-0.03148	-0.02575
SA	setup_FALL→CK	0.05439	0.05439
SA	setup_RISE→CK	0.06012	0.06012
CK	minpwh	0.06822	0.07142
CK	minpwl	0.08171	0.08171

LVT_DRNHS

Cell Description

D Flip-Flop with Async Clear
Q = !RDN ? 0 : rising (CK) ? D : pre_Q
QN = !Q



Function Table

RDN	CK<1>	CK	D	Q
0	X	X	X	0
1	0	0	X	Q<1>
1	0	1	0	0
1	0	1	1	1
1	1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_DRNHSV1	1.26	3.78
LVT_DRNHSV2	1.26	3.78

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00143	0.00143
D	0.00030	0.00030
Q	0.00119	0.00128
QN	0.00123	0.00133
RDN	0.00034	0.00034

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00046	0.00046
D	0.00044	0.00045
RDN	0.00167	0.00167

Max Leakage Power (uW)

V1	V2
0.00914844	0.00962504

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.08229	0.08314
CK→Q_RISE	0.09217	0.09343
RDN→Q_FALL	0.02448	0.02429
CK→QN_FALL	0.06190	0.06233
CK→QN_RISE	0.06520	0.06407
RDN→QN_RISE	0.07405	0.07419

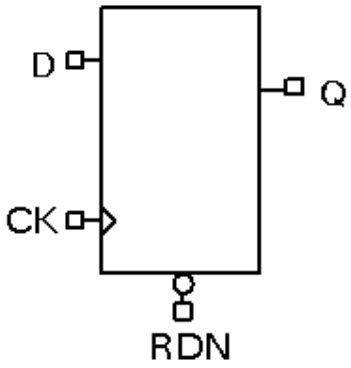
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.00287	-0.00000
D	hold_RISE→CK	-0.01430	-0.01431
D	setup_FALL→CK	0.02575	0.02290
D	setup_RISE→CK	0.02290	0.02577
RDN	setup_RISE→CK	0.02576	0.02576
RDN	hold_RISE→CK	-0.02004	-0.02004
CK	minpwh	0.06507	0.07141
CK	minpwl	0.07378	0.07378
RDN	minpwl	0.04599	0.04916

LVT_DRNQHS

Cell Description

D Flip-Flop with Async Clear, Single Output
Q = !RDN ? 0 : rising (CK) ? D : pre_Q



Function Table

RDN	CK<1>	CK	D	Q
0	X	X	X	0
1	0	0	X	Q<1>
1	0	1	0	0
1	0	1	1	1
1	1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_DRNQHSV1	1.26	3.50
LVT_DRNQHSV2	1.26	3.50

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00145	0.00144
D	0.00029	0.00029
Q	0.00185	0.00194
RDN	0.00034	0.00034

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00047	0.00047
D	0.00044	0.00044
RDN	0.00162	0.00163

Max Leakage Power (uW)

V1	V2
0.00745198	0.00765091

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.07810	0.07802
CK→Q_RISE	0.07536	0.07495
RDN→Q_FALL	0.02965	0.02972

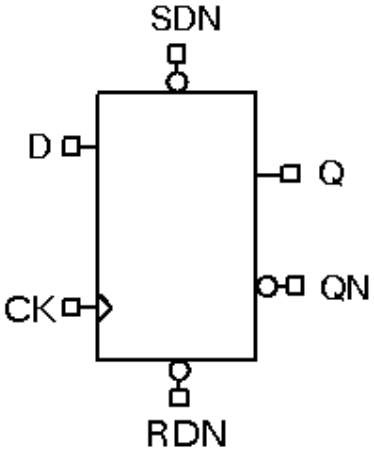
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.00574	-0.00574
D	hold_RISE→CK	-0.01431	-0.01431
D	setup_FALL→CK	0.02290	0.02290
D	setup_RISE→CK	0.02289	0.02289
RDN	setup_RISE→CK	0.02289	0.02576
RDN	hold_RISE→CK	-0.02004	-0.02004
CK	minpwh	0.04600	0.04600
CK	minpwl	0.07378	0.07378
RDN	minpwl	0.04601	0.04918

LVT_DRSNHS

Cell Description

D Flip-Flop with Async Clear and Set
Q = !SDN ? 1 : !RDN ? 0 : rising (CK) ? D : pre_Q
QN = !Q



Function Table

RDN	SDN	CK<1>	CK	D	Q
0	0	X	X	X	1
0	1	X	X	X	0
1	0	X	X	X	1
1	1	0	0	X	Q<1>
1	1	0	1	0	0
1	1	0	1	1	1
1	1	1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_DRSNHSV1	1.26	5.88
LVT_DRSNHSV2	1.26	5.88

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00208	0.00208
D	0.00030	0.00030
Q	0.00136	0.00146
QN	0.00137	0.00147
RDN	0.00101	0.00101
SDN	0.00018	0.00018

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00065	0.00065
D	0.00047	0.00047
RDN	0.00117	0.00117
SDN	0.00088	0.00088

Max Leakage Power (uW)

V1	V2
0.00725554	0.00769425

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.10898	0.11036
CK→Q_RISE	0.10050	0.10195
RDN→Q_FALL	0.09782	0.09923
SDN→Q_FALL	0.06951	0.07096
SDN→Q_RISE	0.06903	0.06985
CK→QN_FALL	0.08253	0.08203
CK→QN_RISE	0.09054	0.08894
RDN→QN_RISE	0.07907	0.07753
SDN→QN_FALL	0.05148	0.05049
SDN→QN_RISE	0.05076	0.04923

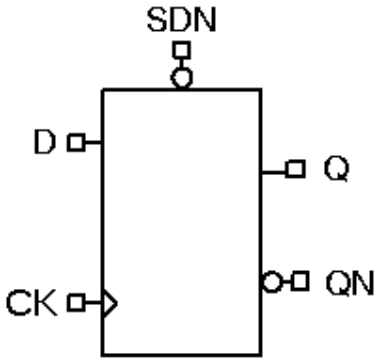
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.00574	-0.00287
D	hold_RISE→CK	-0.02863	-0.02577
D	setup_FALL→CK	0.03435	0.03435
D	setup_RISE→CK	0.04294	0.04581
RDN	setup_RISE→CK	0.04293	0.04579
RDN	hold_RISE→CK	-0.03720	-0.03721
SDN	setup_RISE→CK	-0.04866	-0.04580
SDN	hold_RISE→CK	0.06298	0.06297
SDN	non_seq_hold_RISE→RDN	-0.03434	-0.03434
SDN	non_seq_setup_RISE→RDN	0.04008	0.04581
CK	minpwh	0.08409	0.09042
CK	minpwl	0.11345	0.11345
RDN	minpwl	0.06818	0.07140
SDN	minpwl	0.08404	0.09039

LVT_DSNHS

Cell Description

D Flip-Flop with Async Set
Q = !SDN ? 1 : rising (CK) ? D : pre_Q
QN = !Q



Function Table

SDN	CK<1>	CK	D	Q
0	X	X	X	1
1	0	0	X	Q<1>
1	0	1	0	0
1	0	1	1	1
1	1	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_DSNHSV1	1.26	3.64
LVT_DSNHSV2	1.26	3.64

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00151	0.00151
D	0.00041	0.00041
Q	0.00124	0.00134
QN	0.00120	0.00128
SDN	0.00014	0.00014

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00048	0.00048
D	0.00052	0.00052
SDN	0.00105	0.00105

Max Leakage Power (uW)

V1	V2
0.00752625	0.00797839

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.09081	0.09234
CK→Q_RISE	0.08868	0.08933
SDN→Q_RISE	0.06208	0.06272
CK→QN_FALL	0.07061	0.07093
CK→QN_RISE	0.07412	0.07336
SDN→QN_FALL	0.04560	0.04595

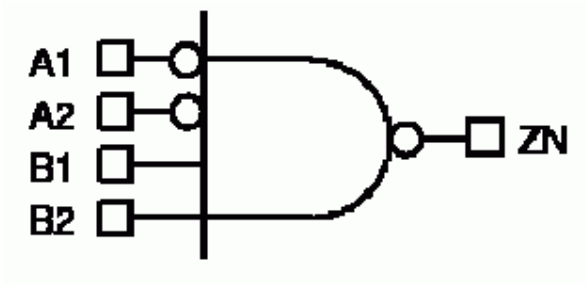
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.00000	0.00286
D	hold_RISE→CK	-0.01145	-0.01145
D	setup_FALL→CK	0.02003	0.02003
D	setup_RISE→CK	0.02291	0.02291
SDN	setup_RISE→CK	-0.03149	-0.03149
SDN	hold_RISE→CK	0.04007	0.04007
CK	minpwh	0.07771	0.08407
CK	minpwl	0.07770	0.07770
SDN	minpwl	0.07454	0.08088

LVT_I2NAND4HS

Cell Description

4-Input NAND with 2 Inverted Inputs
ZN=(!((!A1)&(!A2)&B1&B2))



Function Table

A1	A2	B1	B2	ZN
0	0	0	X	1
0	0	1	0	1
0	0	1	1	0
0	1	X	X	1
1	X	X	X	1

Cell Size

CellName	Height(um)	Width(um)
LVT_I2NAND4HSV1	1.26	1.54
LVT_I2NAND4HSV2	1.26	1.54

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00090	0.00097
A2	0.00090	0.00097
B1	0.00054	0.00059
B2	0.00062	0.00067

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00052	0.00052
A2	0.00052	0.00052
B1	0.00060	0.00065
B2	0.00061	0.00066

Max Leakage Power (uW)

V1	V2
0.00706466	0.00885360

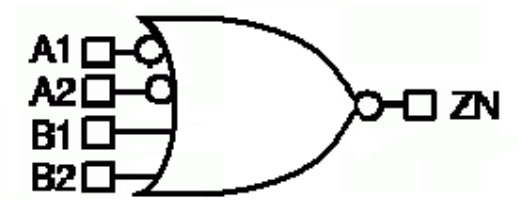
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.03943	0.04174
A1→ZN_RISE	0.02881	0.02723
A2→ZN_FALL	0.04229	0.04481
A2→ZN_RISE	0.02884	0.02712
B1→ZN_FALL	0.02648	0.02826
B1→ZN_RISE	0.01681	0.01424
B2→ZN_FALL	0.02794	0.02978
B2→ZN_RISE	0.01827	0.01528

LVT_I2NOR4HS

Cell Description

4-Input NOR with 2 Inverted Inputs
ZN=(!((!A1)|(!A2)|B1|B2))



Function Table

A1	A2	B1	B2	ZN
0	X	X	X	0
1	0	X	X	0
1	1	0	0	1
1	1	0	1	0
1	1	1	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_I2NOR4HSV1	1.26	1.54
LVT_I2NOR4HSV2	1.26	1.54

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00109	0.00115
A2	0.00101	0.00108
B1	0.00047	0.00052
B2	0.00037	0.00042

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00051	0.00051
A2	0.00051	0.00050
B1	0.00060	0.00066
B2	0.00057	0.00062

Max Leakage Power (uW)

V1	V2
0.00564795	0.00515887

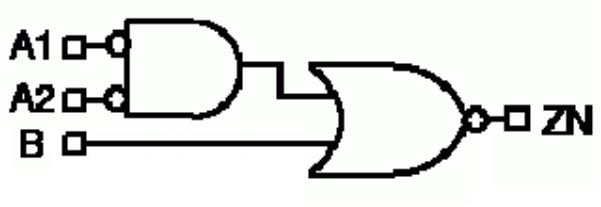
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.03243	0.03092
A1→ZN_RISE	0.05683	0.06056
A2→ZN_FALL	0.03101	0.02960
A2→ZN_RISE	0.05423	0.05828
B1→ZN_FALL	0.01165	0.00999
B1→ZN_RISE	0.03756	0.04109
B2→ZN_FALL	0.01075	0.00942
B2→ZN_RISE	0.03120	0.03481

LVT_IAO21HS

Cell Description

2-1 IAO with 2 Inverted Inputs
ZN=(!(((!A1)&(!A2))|B))



Function Table

A1	A2	B	ZN
0	0	X	0
0	1	0	1
0	1	1	0
1	X	0	1
1	X	1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_IAO21HSV1	1.26	0.98
LVT_IAO21HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00079	0.00084
A2	0.00086	0.00091
B	0.00036	0.00039

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00053	0.00053
A2	0.00057	0.00057
B	0.00063	0.00068

Max Leakage Power (uW)

V1	V2
0.00332033	0.00314674

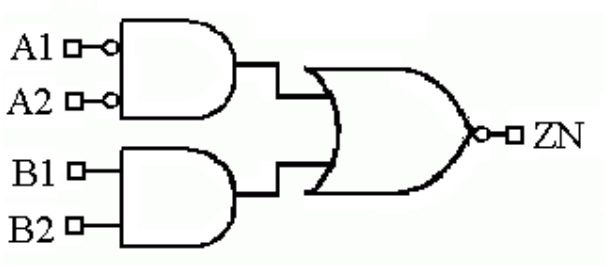
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.03576	0.03506
A1→ZN_RISE	0.02947	0.03092
A2→ZN_FALL	0.03805	0.03735
A2→ZN_RISE	0.03094	0.03238
B→ZN_FALL	0.01016	0.00870
B→ZN_RISE	0.01782	0.01878

LVT_IAO22HS

Cell Description

2-2 IAO with 2 Inverted Inputs
ZN=(!((!A1)&(!A2))|(B1&B2)))



Function Table

B1	B2	A1	A2	ZN
0	X	0	0	0
0	X	0	1	1
0	X	1	X	1
1	0	0	0	0
1	0	0	1	1
1	0	1	X	1
1	1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_IAO22HSV1	1.26	1.26
LVT_IAO22HSV2	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00086	0.00089
A2	0.00092	0.00095
B1	0.00052	0.00052
B2	0.00059	0.00060

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00051	0.00051
A2	0.00057	0.00057
B1	0.00073	0.00071
B2	0.00073	0.00074

Max Leakage Power (uW)

V1	V2
0.00302922	0.00316448

Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.03846	0.03696
A1→ZN_RISE	0.03123	0.03205
A2→ZN_FALL	0.03998	0.03851
A2→ZN_RISE	0.03237	0.03323
B1→ZN_FALL	0.01462	0.01461
B1→ZN_RISE	0.02263	0.02279
B2→ZN_FALL	0.01574	0.01581
B2→ZN_RISE	0.02534	0.02559

LVT_INAND2HS

Cell Description

2-Input NAND with 1 Inverted Input
ZN=(!((!A1)&B1))

Function Table

A1	B1	ZN
0	0	1
0	1	0
1	X	1

Cell Size

CellName	Height(um)	Width(um)
LVT_INAND2HSV1	1.26	0.84
LVT_INAND2HSV2	1.26	0.84

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00072	0.00077
B1	0.00034	0.00036

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00050	0.00052
B1	0.00063	0.00067

Max Leakage Power (uW)

V1	V2
0.00292209	0.00344456

Delay Table (ns)

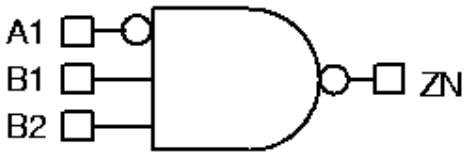
Description	V1	V2
A1→ZN_FALL	0.02808	0.02946
A1→ZN_RISE	0.02461	0.02324

B1→ZN_FALL	0.01201	0.01270
B1→ZN_RISE	0.01334	0.01137

LVT_INAND3HS

Cell Description

3-Input NAND with 1 Inverted Input
ZN=(!((!A1)&B1&B2))



Function Table

A1	B1	B2	ZN
0	0	X	1
0	1	0	1
0	1	1	0
1	X	X	1

Cell Size

CellName	Height(um)	Width(um)
LVT_INAND3HSV1	1.26	0.98
LVT_INAND3HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00082	0.00090
B1	0.00042	0.00046
B2	0.00050	0.00054

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00052	0.00053
B1	0.00062	0.00067
B2	0.00065	0.00071

Max Leakage Power (uW)

V1	V2
0.00453464	0.00519725

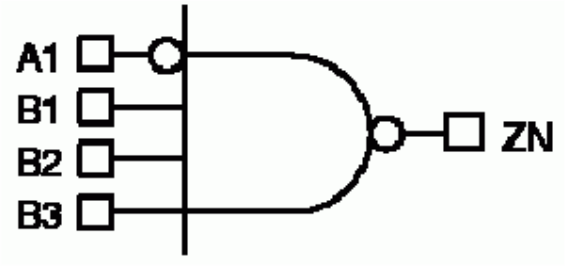
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.03396	0.03641
A1→ZN_RISE	0.02677	0.02533
B1→ZN_FALL	0.01803	0.01943
B1→ZN_RISE	0.01481	0.01230
B2→ZN_FALL	0.01961	0.02092
B2→ZN_RISE	0.01652	0.01352

LVT_INAND4HS

Cell Description

4-Input NAND with 1 Inverted Input
ZN=(!((!A1)&B1&B2&B3))



Function Table

A1	B1	B2	B3	ZN
0	0	X	X	1
0	1	0	X	1
0	1	1	0	1
0	1	1	1	0
1	X	X	X	1

Cell Size

CellName	Height(um)	Width(um)
LVT_INAND4HSV1	1.26	1.12
LVT_INAND4HSV2	1.26	1.12

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00090	0.00096
B1	0.00045	0.00049
B2	0.00053	0.00058
B3	0.00061	0.00065

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00053	0.00053
B1	0.00065	0.00069
B2	0.00062	0.00067
B3	0.00062	0.00067

Max Leakage Power (uW)

V1	V2
0.00606738	0.00742756

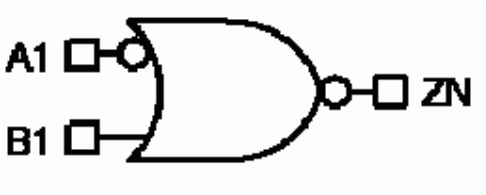
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.03986	0.04229
A1→ZN_RISE	0.02876	0.02742
B1→ZN_FALL	0.02305	0.02481
B1→ZN_RISE	0.01526	0.01315
B2→ZN_FALL	0.02615	0.02789
B2→ZN_RISE	0.01699	0.01444
B3→ZN_FALL	0.02741	0.02914
B3→ZN_RISE	0.01838	0.01547

LVT_INOR2HS

Cell Description

2-Input NOR with 1 Inverted Input
ZN=(!((!A1)|B1))



Function Table

A1	B1	ZN
0	X	0
1	0	1
1	1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_INOR2HSV1	1.26	0.84
LVT_INOR2HSV2	1.26	0.84

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00073	0.00077
B1	0.00033	0.00039

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00051	0.00051
B1	0.00061	0.00067

Max Leakage Power (uW)

V1	V2
0.00292510	0.00286834

Delay Table (ns)

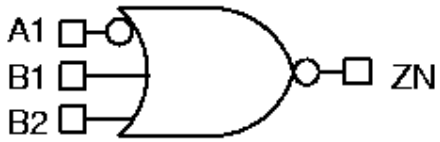
Description	V1	V2
A1→ZN_FALL	0.02562	0.02669
A1→ZN_RISE	0.03281	0.02902

B1→ZN_FALL	0.00838	0.00895
B1→ZN_RISE	0.02254	0.01894

LVT_INOR3HS

Cell Description

3-Input NOR with 1 Inverted Input
ZN=(!((!A1)|B1|B2))



Function Table

A1	B1	B2	ZN
0	X	X	0
1	0	0	1
1	0	1	0
1	1	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_INOR3HSV1	1.26	0.98
LVT_INOR3HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00083	0.00091
B1	0.00043	0.00048
B2	0.00053	0.00058

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00052	0.00052
B1	0.00064	0.00069
B2	0.00064	0.00069

Max Leakage Power (uW)

V1	V2
0.00399058	0.00372220

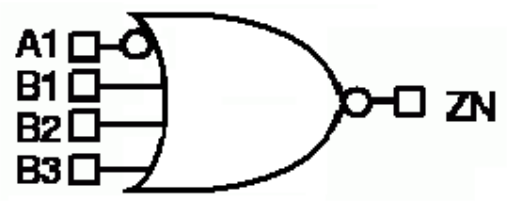
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.02985	0.02920
A1→ZN_RISE	0.03707	0.04004
B1→ZN_FALL	0.01106	0.00955
B1→ZN_RISE	0.02846	0.03088
B2→ZN_FALL	0.01173	0.00991
B2→ZN_RISE	0.03066	0.03302

LVT_INOR4HS

Cell Description

4-Input NOR with 1 Inverted Input
ZN=(!((!A1)|B1|B2|B3))



Function Table

A1	B1	B2	B3	ZN
0	X	X	X	0
1	0	0	0	1
1	0	0	1	0
1	0	1	X	0
1	1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_INOR4HSV1	1.26	1.12
LVT_INOR4HSV2	1.26	1.12

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00089	0.00096
B1	0.00046	0.00051
B2	0.00056	0.00061
B3	0.00066	0.00071

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00052	0.00052
B1	0.00061	0.00066
B2	0.00064	0.00069
B3	0.00064	0.00069

Max Leakage Power (uW)

V1	V2
0.00500010	0.00459946

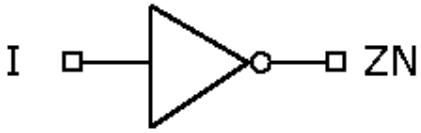
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.03129	0.03052
A1→ZN_RISE	0.04560	0.04969
B1→ZN_FALL	0.01152	0.00993
B1→ZN_RISE	0.03800	0.04157
B2→ZN_FALL	0.01222	0.01031
B2→ZN_RISE	0.04264	0.04648
B3→ZN_FALL	0.01227	0.01028
B3→ZN_RISE	0.04457	0.04847

LVT_INHS

Cell Description

Inverter
ZN=(!I)



Function Table

I	ZN
0	1
1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_INHSV1	1.26	0.42
LVT_INHSV2	1.26	0.42
LVT_INHSV3	1.26	0.56
LVT_INHSV4	1.26	0.56
LVT_INHSV6	1.26	0.84
LVT_INHSV8	1.26	0.98
LVT_INHSV12	1.26	1.26
LVT_INHSV16	1.26	1.68
LVT_INHSV20	1.26	2.10
LVT_INHSV24	1.26	2.38

Pin Power (uW/MHz)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
I	0.00020	0.00025	0.00032	0.00037	0.00060	0.00070	0.00095	0.00135

Pin	V20	V24
I	0.00170	0.00199

Pin Capacitance (pf)

Pin	V1	V2	V3	V4	V6	V8	V12	V16
I	0.00059	0.00071	0.00110	0.00130	0.00185	0.00244	0.00329	0.00478

Pin	V20	V24
I	0.00591	0.00704

Max Leakage Power (uW)

V1	V2	V3	V4	V6	V8	V12	V16
0.00098749	0.00110719	0.00217302	0.00257747	0.00509461	0.00764924	0.01258147	0.01898741

V20	V24
0.02544029	0.03141931

Delay Table (ns)

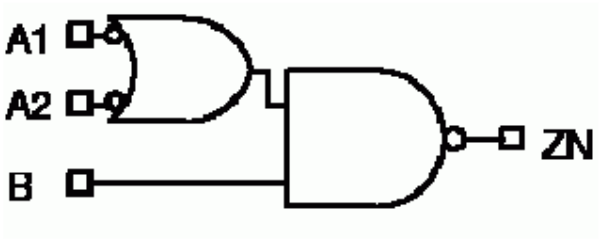
Description	V1	V2	V3	V4	V6	V8	V12	V16
I→ZN_FALL	0.00853	0.00775	0.00656	0.00611	0.00583	0.00536	0.00588	0.00536
I→ZN_RISE	0.01148	0.01009	0.00833	0.00782	0.00746	0.00679	0.00625	0.00658

Description	V20	V24
I→ZN_FALL	0.00563	0.00588
I→ZN_RISE	0.00683	0.00701

LVT_IOA21HS

Cell Description

2-1 IOA with 2 Inverted Inputs
ZN=(!(((!A1)|(!A2))&B))



Function Table

A1	A2	B	ZN
0	X	0	1
0	X	1	0
1	0	0	1
1	0	1	0
1	1	X	1

Cell Size

CellName	Height(um)	Width(um)
LVT_IOA21HSV1	1.26	0.98
LVT_IOA21HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00078	0.00085
A2	0.00086	0.00093
B	0.00034	0.00038

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00058	0.00058
A2	0.00059	0.00059
B	0.00061	0.00067

Max Leakage Power (uW)

V1	V2
0.00347796	0.00410970

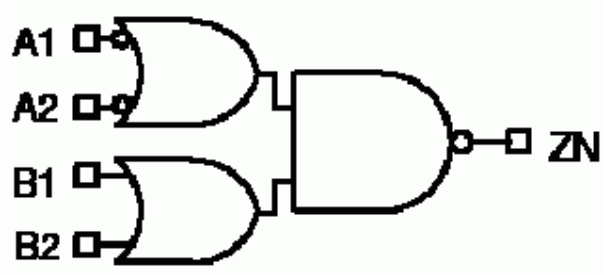
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.03045	0.03238
A1→ZN_RISE	0.02600	0.02464
A2→ZN_FALL	0.03301	0.03495
A2→ZN_RISE	0.02761	0.02621
B→ZN_FALL	0.01194	0.01282
B→ZN_RISE	0.01335	0.01121

LVT_IOA22HS

Cell Description

2-2 IOA with 2 Inverted Inputs
ZN=(!(((!A1)|(!A2))&(B1|B2)))



Function Table

B1	B2	A1	A2	ZN
0	0	X	X	1
0	1	0	X	0
0	1	1	0	0
0	1	1	1	1
1	X	0	X	0
1	X	1	0	0
1	X	1	1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_IOA22HSV1	1.26	1.26
LVT_IOA22HSV2	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00085	0.00088
A2	0.00092	0.00095
B1	0.00047	0.00045
B2	0.00056	0.00055

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00059	0.00059
A2	0.00060	0.00059
B1	0.00063	0.00063
B2	0.00072	0.00073

Max Leakage Power (uW)

V1	V2
0.00351071	0.00411521

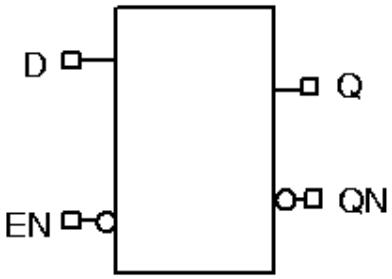
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.03243	0.03359
A1→ZN_RISE	0.02751	0.02571
A2→ZN_FALL	0.03514	0.03616
A2→ZN_RISE	0.02889	0.02699
B1→ZN_FALL	0.01502	0.01472
B1→ZN_RISE	0.02285	0.02206
B2→ZN_FALL	0.01685	0.01655
B2→ZN_RISE	0.02524	0.02441

LVT_LALHS

Cell Description

Low Enable Latch
Q = !EN ? D : pre_Q
QN = !Q



Function Table

EN	D	Q
0	0	0
0	1	1
1	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_LALHSV1	1.26	2.24
LVT_LALHSV2	1.26	2.24

Pin Power (uW/MHz)

Pin	V1	V2
D	0.00002	0.00002
EN	0.00113	0.00113
Q	0.00095	0.00108
QN	0.00096	0.00107

Pin Capacitance (pf)

Pin	V1	V2
D	0.00070	0.00070
EN	0.00052	0.00052

Max Leakage Power (uW)

V1	V2
0.00508670	0.00521508

Delay Table (ns)

Description	V1	V2

D→Q_FALL	0.04477	0.04564
D→Q_RISE	0.03900	0.03849
EN→Q_FALL	0.07518	0.07595
EN→Q_RISE	0.06715	0.06658
D→QN_FALL	0.05399	0.05665
D→QN_RISE	0.06346	0.06564
EN→QN_FALL	0.08242	0.08507
EN→QN_RISE	0.09390	0.09599

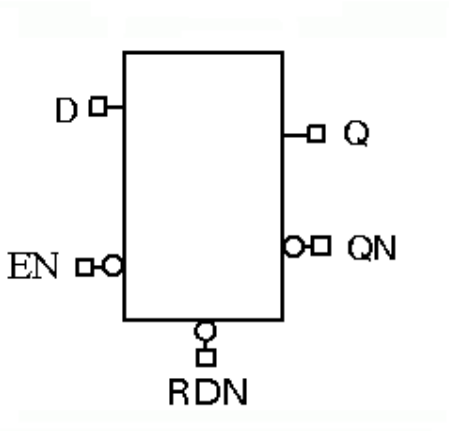
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→EN	-0.01145	-0.01432
D	hold_RISE→EN	-0.01718	-0.01719
D	setup_FALL→EN	0.02577	0.03148
D	setup_RISE→EN	0.02291	0.02577
EN	minpwl	0.05868	0.06186

LVT_LALRNHS

Cell Description

Latch
Q = !RDN ? 0 : !EN ? D : pre_Q
QN = !Q



Function Table

RDN	EN	D	Q
0	X	X	0
1	0	0	0
1	0	1	1
1	1	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_LALRNHSV1	1.26	2.66
LVT_LALRNHSV2	1.26	2.66

Pin Power (uW/MHz)

Pin	V1	V2
D	0.00002	0.00002
EN	0.00120	0.00120
Q	0.00112	0.00126
QN	0.00112	0.00125
RDN	0.00001	0.00001

Pin Capacitance (pf)

Pin	V1	V2
D	0.00065	0.00065
EN	0.00052	0.00053
RDN	0.00093	0.00094

Max Leakage Power (uW)

V1	V2
0.00576399	0.00602230

Delay Table (ns)

Description	V1	V2
D→Q_FALL	0.05020	0.05090
D→Q_RISE	0.05373	0.05333
EN→Q_FALL	0.08124	0.08188
EN→Q_RISE	0.07985	0.07950
RDN→Q_FALL	0.04959	0.05017
RDN→Q_RISE	0.05681	0.05643
D→QN_FALL	0.07235	0.07570
D→QN_RISE	0.06833	0.07074
EN→QN_FALL	0.09871	0.10214
EN→QN_RISE	0.09939	0.10178
RDN→QN_RISE	0.06828	0.07064
RDN→QN_FALL	0.07542	0.07878

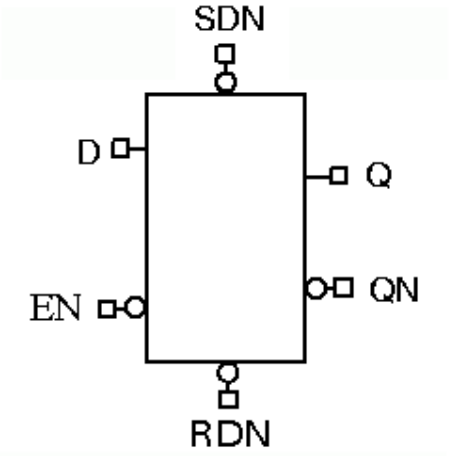
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→EN	-0.01433	-0.01718
D	hold_RISE→EN	-0.03150	-0.03149
D	setup_FALL→EN	0.03150	0.03721
D	setup_RISE→EN	0.03721	0.04294
RDN	setup_RISE→EN	0.04009	0.04580
RDN	hold_RISE→EN	-0.03435	-0.03436
EN	minpwl	0.07134	0.07453
RDN	minpwl	0.06819	0.07139

LVT_LALRSNHS

Cell Description

Low Enable Latch with Clear and Set
Q = !SDN ? 1 : !RDN ? 0 : !EN ? D : pre_Q
QN = !Q



Function Table

RDN	SDN	EN	D	Q
0	0	X	X	1
0	1	X	X	0
1	0	X	X	1
1	1	0	0	0
1	1	0	1	1
1	1	1	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_LALRSNHSV1	1.26	3.92
LVT_LALRSNHSV2	1.26	4.06

Pin Power (uW/MHz)

Pin	V1	V2
D	0.00002	0.00002
EN	0.00133	0.00137
Q	0.00135	0.00148
QN	0.00132	0.00141
RDN	0.00002	0.00002
SDN	0.00059	0.00059

Pin Capacitance (pf)

Pin	V1	V2
D	0.00065	0.00066
EN	0.00051	0.00051
RDN	0.00098	0.00099
SDN	0.00050	0.00051

Max Leakage Power (uW)

V1	V2
0.00524800	0.00661071

Delay Table (ns)

Description	V1	V2
D→Q_FALL	0.07925	0.07795
D→Q_RISE	0.06060	0.05795
EN→Q_FALL	0.10961	0.10951
EN→Q_RISE	0.08426	0.08300
RDN→Q_FALL	0.09422	0.09280
RDN→Q_RISE	0.06438	0.06216
SDN→Q_FALL	0.10470	0.10243
SDN→Q_RISE	0.07094	0.06866
D→QN_FALL	0.07970	0.07900
D→QN_RISE	0.09721	0.09770
EN→QN_FALL	0.10366	0.10416
EN→QN_RISE	0.12774	0.12946
RDN→QN_RISE	0.11334	0.11443
RDN→QN_FALL	0.08349	0.08316
SDN→QN_FALL	0.08847	0.08767
SDN→QN_RISE	0.12304	0.12282

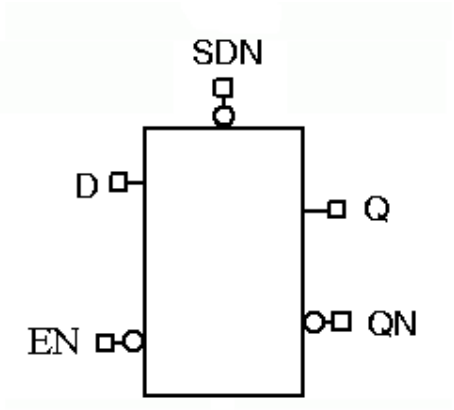
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→EN	-0.03435	-0.04006
D	hold_RISE→EN	-0.03435	-0.03722
D	setup_FALL→EN	0.05725	0.06582
D	setup_RISE→EN	0.04581	0.05153
RDN	setup_RISE→EN	0.04868	0.05727
RDN	hold_RISE→EN	-0.04009	-0.04008
SDN	setup_RISE→EN	0.07728	0.08587
SDN	hold_RISE→EN	-0.06011	-0.06297
SDN	non_seq_hold_RISE→RDN	-0.09732	-0.10304
SDN	non_seq_setup_RISE→RDN	0.12022	0.12881
EN	minpwl	0.07137	0.08090
RDN	minpwl	0.10947	0.11899
SDN	minpwl	0.05864	0.06184

LVT_LALSNHS

Cell Description

Latch
Q = !SDN ? 1 : !EN ? D : pre_Q
QN = !Q



Function Table

SDN	EN	D	Q
0	X	X	1
1	0	0	0
1	0	1	1
1	1	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_LALSNHSV1	1.26	2.94
LVT_LALSNHSV2	1.26	2.94

Pin Power (uW/MHz)

Pin	V1	V2
D	0.00001	0.00001
EN	0.00121	0.00121
Q	0.00116	0.00129
QN	0.00114	0.00125
SDN	0.00052	0.00051

Pin Capacitance (pf)

Pin	V1	V2
D	0.00063	0.00063
EN	0.00052	0.00052
SDN	0.00067	0.00069

Max Leakage Power (uW)

V1	V2
0.00577785	0.00631538

Delay Table (ns)

Description	V1	V2
D→Q_FALL	0.06747	0.06796
D→Q_RISE	0.04332	0.04242
EN→Q_FALL	0.09553	0.09579
EN→Q_RISE	0.07293	0.07221
SDN→Q_FALL	0.08832	0.08868
SDN→Q_RISE	0.06518	0.06403
D→QN_FALL	0.05986	0.06183
D→QN_RISE	0.08713	0.08956
EN→QN_FALL	0.08972	0.09188
EN→QN_RISE	0.11522	0.11747
SDN→QN_FALL	0.08163	0.08324
SDN→QN_RISE	0.10797	0.11030

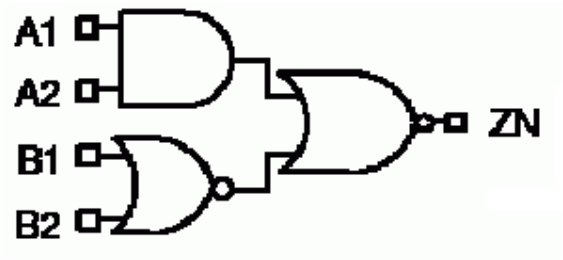
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→EN	-0.03435	-0.03722
D	hold_RISE→EN	-0.02004	-0.02004
D	setup_FALL→EN	0.05726	0.06298
D	setup_RISE→EN	0.02576	0.02864
SDN	setup_RISE→EN	0.07730	0.08302
SDN	hold_RISE→EN	-0.05724	-0.06012
EN	minpwl	0.06186	0.06505
SDN	minpwl	0.05231	0.05547

LVT_MAOI22HS

Cell Description

the logical NOR of one AND2 and one NOR2 block.
ZN=(!((A1&A2)|(!(B1|B2))))



Function Table

A1	A2	B1	B2	ZN
0	X	0	0	0
0	X	0	1	1
0	X	1	X	1
1	0	0	0	0
1	0	0	1	1
1	0	1	X	1
1	1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_MAOI22HSV1	1.26	1.26
LVT_MAOI22HSV2	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00060	0.00061
A2	0.00052	0.00053
B1	0.00086	0.00089
B2	0.00092	0.00095

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00075	0.00075
A2	0.00072	0.00072
B1	0.00054	0.00054
B2	0.00057	0.00057

Max Leakage Power (uW)

V1	V2
0.00300871	0.00317117

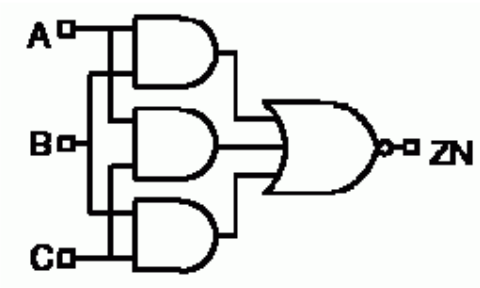
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.01587	0.01593
A1→ZN_RISE	0.02548	0.02573
A2→ZN_FALL	0.01465	0.01470
A2→ZN_RISE	0.02272	0.02296
B1→ZN_FALL	0.03873	0.03706
B1→ZN_RISE	0.03135	0.03211
B2→ZN_FALL	0.03994	0.03846
B2→ZN_RISE	0.03235	0.03321

LVT_MAOI222HS

Cell Description

Inverting 2 of 3 MAJORITY
ZN=(!((A&B)|(B&C)|(A&C)))



Function Table

A	B	C	ZN
0	0	X	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_MAOI222HSV1	1.26	1.54
LVT_MAOI222HSV2	1.26	1.54

Pin Power (uW/MHz)

Pin	V1	V2
A	0.00069	0.00089
B	0.00060	0.00077
C	0.00078	0.00100

Pin Capacitance (pf)

Pin	V1	V2
A	0.00121	0.00144
B	0.00107	0.00131
C	0.00110	0.00134

Max Leakage Power (uW)

V1	V2
0.00202534	0.00255523

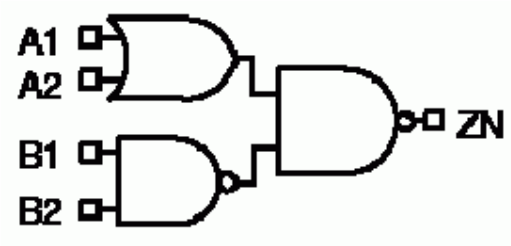
Delay Table (ns)

Description	V1	V2
A→ZN_FALL	0.02114	0.01938
A→ZN_RISE	0.04532	0.04116
B→ZN_FALL	0.02067	0.01914
B→ZN_RISE	0.04243	0.03880
C→ZN_FALL	0.02224	0.02048
C→ZN_RISE	0.04781	0.04369

LVT_MOAI22HS

Cell Description

the logical NAND of one OR2 and one NAND2 block.
ZN=(!((A1|A2)&(!(B1&B2))))



Function Table

A1	A2	B1	B2	ZN
0	0	X	X	1
0	1	0	X	0
0	1	1	0	0
0	1	1	1	1
1	X	0	X	0
1	X	1	0	0
1	X	1	1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_MOAI22HSV1	1.26	1.26
LVT_MOAI22HSV2	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00047	0.00047
A2	0.00056	0.00057
B1	0.00086	0.00089
B2	0.00092	0.00095

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00063	0.00063
A2	0.00073	0.00073
B1	0.00075	0.00075
B2	0.00059	0.00058

Max Leakage Power (uW)

V1	V2
0.00346092	0.00407492

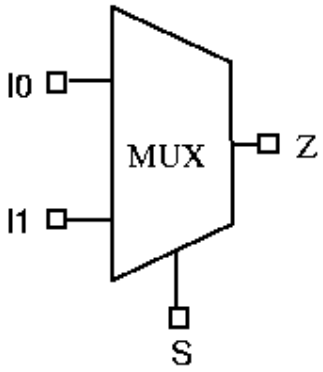
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.01497	0.01516
A1→ZN_RISE	0.02275	0.02276
A2→ZN_FALL	0.01693	0.01710
A2→ZN_RISE	0.02521	0.02521
B1→ZN_FALL	0.03289	0.03385
B1→ZN_RISE	0.02797	0.02602
B2→ZN_FALL	0.03524	0.03609
B2→ZN_RISE	0.02900	0.02700

LVT_MUX2HS

Cell Description

2-to-1 Multiplexer
Z=((I0&(!S))|(I1&S))



Function Table

S	I0	I1	Z
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_MUX2HSV1	1.26	1.68
LVT_MUX2HSV2	1.26	1.68

Pin Power (uW/MHz)

Pin	V1	V2
I0	0.00109	0.00117
I1	0.00093	0.00100
S	0.00115	0.00123

Pin Capacitance (pf)

Pin	V1	V2
I0	0.00060	0.00060
I1	0.00063	0.00063
S	0.00099	0.00099

Max Leakage Power (uW)

V1	V2
0.00728267	0.00749461

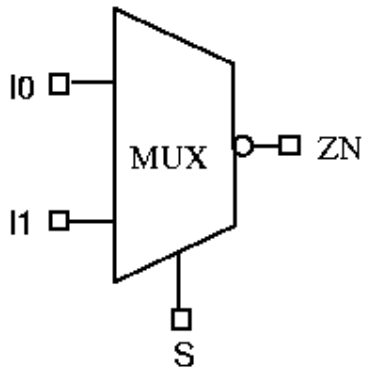
Delay Table (ns)

Description	V1	V2
I0→Z_FALL	0.03938	0.03976
I0→Z_RISE	0.03556	0.03522
I1→Z_FALL	0.03435	0.03458
I1→Z_RISE	0.03019	0.02970
S→Z_FALL	0.03127	0.03167
S→Z_RISE	0.03211	0.03173

LVT_MUX2NHS

Cell Description

2-to-1 Inverting Multiplexer
ZN=(!((I0&(!S))|(I1&S)))



Function Table

S	I0	I1	ZN
0	0	X	1
0	1	X	0
1	X	0	1
1	X	1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_MUX2NHSV1	1.26	1.54
LVT_MUX2NHSV2	1.26	1.68

Pin Power (uW/MHz)

Pin	V1	V2
I0	0.00063	0.00070
I1	0.00067	0.00075
S	0.00068	0.00077

Pin Capacitance (pf)

Pin	V1	V2
I0	0.00060	0.00059
I1	0.00061	0.00061
S	0.00102	0.00108

Max Leakage Power (uW)

V1	V2
0.00477412	0.00489836

Delay Table (ns)

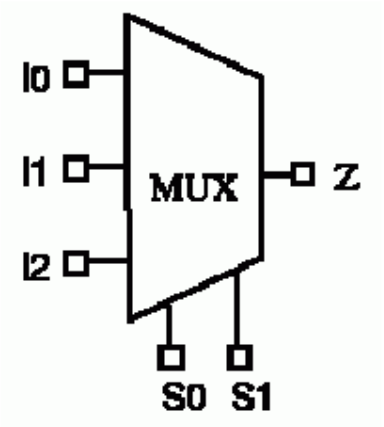
Description	V1	V2
I0→ZN_FALL	0.01971	0.02048
I0→ZN_RISE	0.02417	0.02530
I1→ZN_FALL	0.01931	0.02009
I1→ZN_RISE	0.02633	0.02796
S→ZN_FALL	0.01689	0.01708
S→ZN_RISE	0.01724	0.01799

LVT_MUX3HS

Cell Description

3-to-1 Multiplexer

Z=((I0&(!S0)&(!S1))|(I1&S0&(!S1))|(I2&S1))



Function Table

S1	S0	I0	I1	I2	Z
0	0	0	X	X	0
0	0	1	X	X	1
0	1	X	0	X	0
0	1	X	1	X	1
1	X	X	X	0	0
1	X	X	X	1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_MUX3HSV1	1.26	3.50
LVT_MUX3HSV2	1.26	3.50

Pin Power (uW/MHz)

Pin	V1	V2
I0	0.00257	0.00268
I1	0.00228	0.00239
I2	0.00202	0.00214
S0	0.00292	0.00303
S1	0.00201	0.00211

Pin Capacitance (pf)

Pin	V1	V2
I0	0.00069	0.00069
I1	0.00065	0.00065
I2	0.00075	0.00076
S0	0.00157	0.00157
S1	0.00120	0.00120

Max Leakage Power (uW)

V1	V2
0.00985828	0.00955149

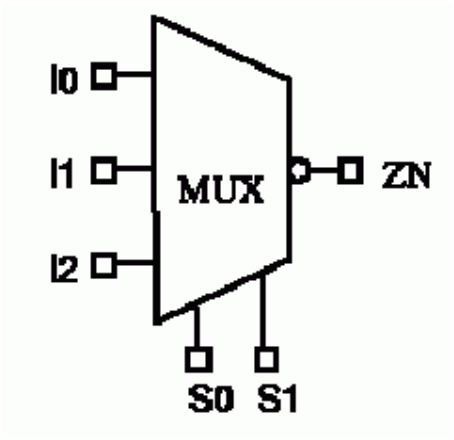
Delay Table (ns)

Description	V1	V2
I0→Z_FALL	0.07712	0.07799
I0→Z_RISE	0.07536	0.07583
I1→Z_FALL	0.06878	0.06971
I1→Z_RISE	0.06878	0.06938
I2→Z_FALL	0.05245	0.05371
I2→Z_RISE	0.05718	0.05811
S0→Z_FALL	0.08045	0.08140
S0→Z_RISE	0.07768	0.07824
S1→Z_FALL	0.04710	0.04780
S1→Z_RISE	0.05389	0.05441

LVT_MUX3NHS

Cell Description

3-to-1 Inverting Multiplexer
ZN=(!((I0&(!S0)&(!S1))|(I1&S0&(!S1))|(I2&S1)))



Function Table

S1	S0	I0	I1	I2	ZN
0	0	0	X	X	1
0	0	1	X	X	0
0	1	X	0	X	1
0	1	X	1	X	0
1	X	X	X	0	1
1	X	X	X	1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_MUX3NHSV1	1.26	3.08
LVT_MUX3NHSV2	1.26	3.08

Pin Power (uW/MHz)

Pin	V1	V2
I0	0.00204	0.00212
I1	0.00175	0.00184
I2	0.00149	0.00157
S0	0.00239	0.00255
S1	0.00147	0.00155

Pin Capacitance (pf)

Pin	V1	V2
I0	0.00069	0.00070
I1	0.00066	0.00066
I2	0.00076	0.00076
S0	0.00157	0.00139
S1	0.00119	0.00119

Max Leakage Power (uW)

V1	V2
0.00907689	0.01050280

Delay Table (ns)

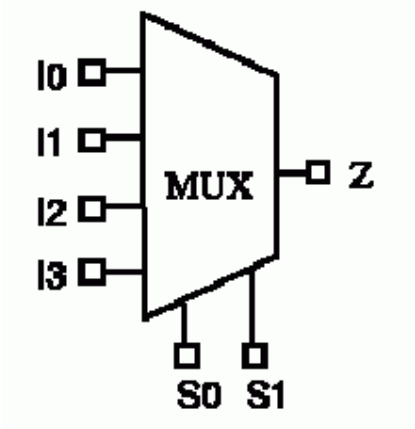
Description	V1	V2
I0→ZN_FALL	0.06181	0.06072
I0→ZN_RISE	0.06683	0.06518
I1→ZN_FALL	0.05528	0.05448
I1→ZN_RISE	0.05851	0.05728
I2→ZN_FALL	0.04368	0.04322
I2→ZN_RISE	0.04282	0.04148
S0→ZN_FALL	0.06429	0.06434
S0→ZN_RISE	0.07015	0.06951
S1→ZN_FALL	0.03985	0.03944
S1→ZN_RISE	0.03693	0.03555

LVT_MUX4HS

Cell Description

4-to-1 Multiplexer

Z=((I0&(!S0)&(!S1))|(I1&S0&(!S1))|(I2&(!S0)&S1)|(I3&S0&S1))



Function Table

S1	S0	I0	I1	I2	I3	Z
0	0	0	X	X	X	0
0	0	1	X	X	X	1
0	1	X	0	X	X	0
0	1	X	1	X	X	1
1	0	X	X	0	X	0
1	0	X	X	1	X	1
1	1	X	X	X	0	0
1	1	X	X	X	1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_MUX4HSV1	1.26	4.06
LVT_MUX4HSV2	1.26	4.06

Pin Power (uW/MHz)

Pin	V1	V2
I0	0.00210	0.00220
I1	0.00244	0.00254
I2	0.00235	0.00244
I3	0.00260	0.00270
S0	0.00195	0.00205
S1	0.00350	0.00360

Pin Capacitance (pf)

Pin	V1	V2
I0	0.00070	0.00070
I1	0.00084	0.00083
I2	0.00067	0.00067
I3	0.00067	0.00067

S0	0.00153	0.00153
S1	0.00222	0.00221

Max Leakage Power (uW)

V1	V2
0.01083365	0.01058576

Delay Table (ns)

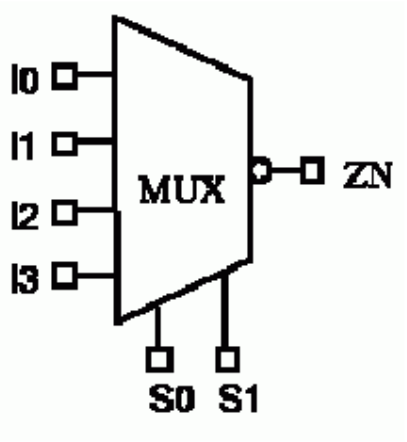
Description	V1	V2
I0→Z_FALL	0.06446	0.06502
I0→Z_RISE	0.06249	0.06226
I1→Z_FALL	0.07431	0.07515
I1→Z_RISE	0.07694	0.07689
I2→Z_FALL	0.07152	0.07202
I2→Z_RISE	0.06742	0.06714
I3→Z_FALL	0.07627	0.07709
I3→Z_RISE	0.07987	0.07980
S0→Z_FALL	0.04595	0.04678
S0→Z_RISE	0.05567	0.05575
S1→Z_FALL	0.08019	0.08086
S1→Z_RISE	0.07910	0.07893

LVT_MUX4NHS

Cell Description

4-to-1 Inverting Multiplexer

ZN=(!((I0&(!S0)&(!S1))|(I1&S0&(!S1))|(I2&(!S0)&S1)|(I3&S0&S1)))



Function Table

S1	S0	I0	I1	I2	I3	ZN
0	0	0	X	X	X	1
0	0	1	X	X	X	0
0	1	X	0	X	X	1
0	1	X	1	X	X	0
1	0	X	X	0	X	1
1	0	X	X	1	X	0
1	1	X	X	X	0	1
1	1	X	X	X	1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_MUX4NHSV1	1.26	3.78
LVT_MUX4NHSV2	1.26	3.78

Pin Power (uW/MHz)

Pin	V1	V2
I0	0.00154	0.00165
I1	0.00189	0.00200
I2	0.00179	0.00189
I3	0.00205	0.00216
S0	0.00140	0.00150
S1	0.00295	0.00305

Pin Capacitance (pf)

Pin	V1	V2
I0	0.00070	0.00070
I1	0.00083	0.00084
I2	0.00067	0.00067
I3	0.00067	0.00067

S0	0.00153	0.00153
S1	0.00221	0.00221

Max Leakage Power (uW)

V1	V2
0.01032741	0.01023227

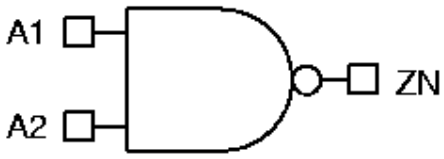
Delay Table (ns)

Description	V1	V2
I0→ZN_FALL	0.04824	0.04833
I0→ZN_RISE	0.05353	0.05329
I1→ZN_FALL	0.06138	0.06237
I1→ZN_RISE	0.06343	0.06297
I2→ZN_FALL	0.05233	0.05320
I2→ZN_RISE	0.06057	0.06029
I3→ZN_FALL	0.06420	0.06531
I3→ZN_RISE	0.06533	0.06499
S0→ZN_FALL	0.04000	0.04104
S0→ZN_RISE	0.03537	0.03484
S1→ZN_FALL	0.06406	0.06479
S1→ZN_RISE	0.06918	0.06892

LVT_NAND2HS

Cell Description

2-Input NAND
ZN=(!(A1&A2))



Function Table

A1	A2	ZN
0	X	1
1	0	1
1	1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_NAND2HSV1	1.26	0.70
LVT_NAND2HSV2	1.26	0.70
LVT_NAND2HSV3	1.26	0.98
LVT_NAND2HSV8	1.26	1.68

Pin Power (uW/MHz)

Pin	V1	V2	V3	V8
A1	0.00027	0.00030	0.00046	0.00097
A2	0.00035	0.00038	0.00061	0.00148

Pin Capacitance (pf)

Pin	V1	V2	V3	V8
A1	0.00060	0.00067	0.00103	0.00231
A2	0.00063	0.00069	0.00123	0.00244

Max Leakage Power (uW)

V1	V2	V3	V8
0.00203403	0.00284202	0.00592124	0.01901995

Delay Table (ns)

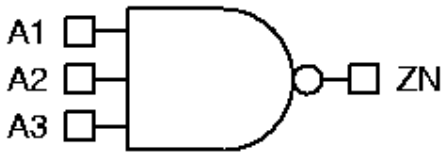
Description	V1	V2	V3	V8

A1→ZN_FALL	0.01079	0.01144	0.01020	0.00855
A1→ZN_RISE	0.01248	0.01046	0.00921	0.00776
A2→ZN_FALL	0.01209	0.01275	0.01203	0.01086
A2→ZN_RISE	0.01413	0.01156	0.01096	0.00942

LVT_NAND3HS

Cell Description

3-Input NAND
ZN=(!(A1&A2&A3))



Function Table

A1	A2	A3	ZN
0	X	X	1
1	0	X	1
1	1	0	1
1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_NAND3HSV1	1.26	0.84
LVT_NAND3HSV2	1.26	0.84
LVT_NAND3HSV3	1.26	1.26
LVT_NAND3HSV8	1.26	2.52

Pin Power (uW/MHz)

Pin	V1	V2	V3	V8
A1	0.00035	0.00040	0.00056	0.00128
A2	0.00044	0.00049	0.00071	0.00175
A3	0.00051	0.00056	0.00081	0.00210

Pin Capacitance (pf)

Pin	V1	V2	V3	V8
A1	0.00058	0.00065	0.00097	0.00228
A2	0.00062	0.00070	0.00118	0.00244
A3	0.00063	0.00070	0.00122	0.00242

Max Leakage Power (uW)

V1	V2	V3	V8
0.00344315	0.00489435	0.00668535	0.02563339

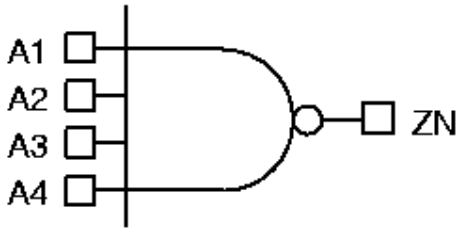
Delay Table (ns)

Description	V1	V2	V3	V8
A1→ZN_FALL	0.01566	0.01718	0.01442	0.01262
A1→ZN_RISE	0.01399	0.01183	0.01039	0.00879
A2→ZN_FALL	0.01803	0.01967	0.01756	0.01649
A2→ZN_RISE	0.01539	0.01274	0.01207	0.01036
A3→ZN_FALL	0.01920	0.02078	0.01861	0.01801
A3→ZN_RISE	0.01706	0.01386	0.01334	0.01141

LVT_NAND4HS

Cell Description

4-Input NAND
ZN=(!(A1&A2&A3&A4))



Function Table

A1	A2	A3	A4	ZN
0	X	X	X	1
1	0	X	X	1
1	1	0	X	1
1	1	1	0	1
1	1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_NAND4HSV1	1.26	0.98
LVT_NAND4HSV2	1.26	0.98
LVT_NAND4HSV3	1.26	1.68
LVT_NAND4HSV8	1.26	2.24

Pin Power (uW/MHz)

Pin	V1	V2	V3	V8
A1	0.00033	0.00045	0.00063	0.00312
A2	0.00041	0.00053	0.00078	0.00320
A3	0.00049	0.00062	0.00093	0.00328
A4	0.00057	0.00069	0.00102	0.00336

Pin Capacitance (pf)

Pin	V1	V2	V3	V8
A1	0.00054	0.00064	0.00096	0.00066
A2	0.00059	0.00070	0.00117	0.00071
A3	0.00058	0.00069	0.00125	0.00070
A4	0.00058	0.00069	0.00125	0.00071

Max Leakage Power (uW)

V1	V2	V3	V8
0.00277009	0.00764836	0.00998736	0.01883821

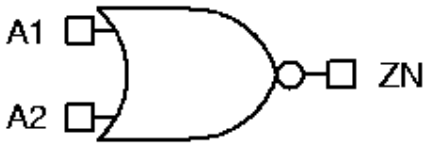
Delay Table (ns)

Description	V1	V2	V3	V8
A1→ZN_FALL	0.01775	0.02234	0.01833	0.06085
A1→ZN_RISE	0.01768	0.01235	0.01087	0.03698
A2→ZN_FALL	0.02112	0.02578	0.02287	0.06428
A2→ZN_RISE	0.01966	0.01314	0.01252	0.03783
A3→ZN_FALL	0.02383	0.02859	0.02584	0.06707
A3→ZN_RISE	0.02212	0.01425	0.01384	0.03940
A4→ZN_FALL	0.02506	0.02973	0.02650	0.06817
A4→ZN_RISE	0.02444	0.01517	0.01476	0.04109

LVT_NOR2HS

Cell Description

2-Input NOR
ZN=(!(A1|A2))



Function Table

A1	A2	ZN
0	0	1
0	1	0
1	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_NOR2HSV1	1.26	0.56
LVT_NOR2HSV2	1.26	0.56
LVT_NOR2HSV3	1.26	0.98
LVT_NOR2HSV8	1.26	1.68

Pin Power (uW/MHz)

Pin	V1	V2	V3	V8
A1	0.00028	0.00031	0.00043	0.00093
A2	0.00037	0.00040	0.00069	0.00151

Pin Capacitance (pf)

Pin	V1	V2	V3	V8
A1	0.00059	0.00065	0.00100	0.00220
A2	0.00066	0.00070	0.00106	0.00240

Max Leakage Power (uW)

V1	V2	V3	V8
0.00205445	0.00222182	0.00516162	0.01082784

Delay Table (ns)

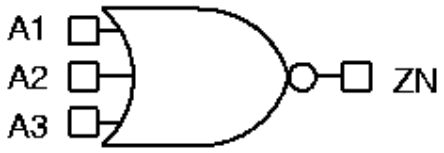
Description	V1	V2	V3	V8

A1→ZN_FALL	0.00975	0.00837	0.00721	0.00623
A1→ZN_RISE	0.01651	0.01745	0.01380	0.01141
A2→ZN_FALL	0.01058	0.00885	0.00823	0.00728
A2→ZN_RISE	0.01831	0.01918	0.01761	0.01475

LVT_NOR3HS

Cell Description

3-Input NOR
ZN=(!(A1|A2|A3))



Function Table

A1	A2	A3	ZN
0	0	0	1
0	0	1	0
0	1	X	0
1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_NOR3HSV1	1.26	0.84
LVT_NOR3HSV2	1.26	0.84
LVT_NOR3HSV3	1.26	1.26
LVT_NOR3HSV8	1.26	2.52

Pin Power (uW/MHz)

Pin	V1	V2	V3	V8
A1	0.00032	0.00041	0.00050	0.00117
A2	0.00039	0.00051	0.00068	0.00173
A3	0.00045	0.00060	0.00082	0.00221

Pin Capacitance (pf)

Pin	V1	V2	V3	V8
A1	0.00051	0.00062	0.00091	0.00215
A2	0.00058	0.00068	0.00115	0.00233
A3	0.00059	0.00072	0.00123	0.00243

Max Leakage Power (uW)

V1	V2	V3	V8
0.00366989	0.00401212	0.00718011	0.01460763

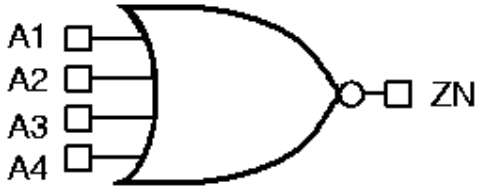
Delay Table (ns)

Description	V1	V2	V3	V8
A1→ZN_FALL	0.00981	0.00906	0.00764	0.00684
A1→ZN_RISE	0.03062	0.02713	0.02177	0.01698
A2→ZN_FALL	0.01052	0.00978	0.00866	0.00785
A2→ZN_RISE	0.03508	0.03155	0.02793	0.02365
A3→ZN_FALL	0.01077	0.01001	0.00898	0.00807
A3→ZN_RISE	0.03667	0.03339	0.02967	0.02619

LVT_NOR4HS

Cell Description

4-Input NOR
ZN=(!(A1|A2|A3|A4))



Function Table

A1	A2	A3	A4	ZN
0	0	0	0	1
0	0	0	1	0
0	0	1	X	0
0	1	X	X	0
1	X	X	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_NOR4HSV1	1.26	0.98
LVT_NOR4HSV2	1.26	0.98
LVT_NOR4HSV3	1.26	1.68
LVT_NOR4HSV8	1.26	2.10

Pin Power (uW/MHz)

Pin	V1	V2	V3	V8
A1	0.00037	0.00044	0.00063	0.00322
A2	0.00047	0.00054	0.00080	0.00333
A3	0.00058	0.00064	0.00097	0.00343
A4	0.00067	0.00073	0.00111	0.00354

Pin Capacitance (pf)

Pin	V1	V2	V3	V8
A1	0.00056	0.00061	0.00091	0.00064
A2	0.00061	0.00067	0.00114	0.00066
A3	0.00063	0.00067	0.00126	0.00069
A4	0.00064	0.00070	0.00127	0.00071

Max Leakage Power (uW)

V1	V2	V3	V8
0.00484253	0.00531252	0.01028217	0.01677953

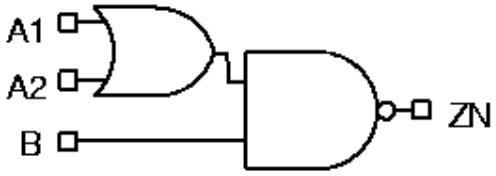
Delay Table (ns)

Description	V1	V2	V3	V8
A1→ZN_FALL	0.01072	0.00942	0.00835	0.03224
A1→ZN_RISE	0.03135	0.03584	0.03103	0.08274
A2→ZN_FALL	0.01171	0.01003	0.00917	0.03329
A2→ZN_RISE	0.03837	0.04259	0.03936	0.09029
A3→ZN_FALL	0.01240	0.01044	0.00974	0.03426
A3→ZN_RISE	0.04311	0.04743	0.04555	0.09511
A4→ZN_FALL	0.01250	0.01043	0.00978	0.03480
A4→ZN_RISE	0.04476	0.04915	0.04686	0.09792

LVT_OAI21HS

Cell Description

2-1 OAI
ZN=(!((A1|A2)&B))



Function Table

A1	A2	B	ZN
0	0	X	1
0	1	0	1
0	1	1	0
1	X	0	1
1	X	1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_OAI21HSV1	1.26	0.84
LVT_OAI21HSV2	1.26	0.84

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00037	0.00049
A2	0.00044	0.00058
B	0.00026	0.00034

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00060	0.00070
A2	0.00061	0.00074
B	0.00056	0.00069

Max Leakage Power (uW)

V1	V2
0.00234648	0.00333769

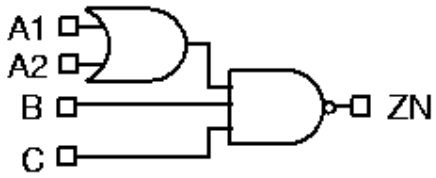
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.01582	0.01480
A1→ZN_RISE	0.02461	0.02240
A2→ZN_FALL	0.01743	0.01640
A2→ZN_RISE	0.02665	0.02452
B→ZN_FALL	0.01243	0.01149
B→ZN_RISE	0.01155	0.01053

LVT_OAI211HS

Cell Description

2-1-1 OAI
ZN=(!((A1|A2)&B&C))



Function Table

A1	A2	B	C	ZN
0	0	X	X	1
0	1	0	X	1
0	1	1	0	1
0	1	1	1	0
1	X	0	X	1
1	X	1	0	1
1	X	1	1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_OAI211HSV1	1.26	0.98
LVT_OAI211HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00051	0.00065
A2	0.00057	0.00074
B	0.00035	0.00044
C	0.00040	0.00052

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00053	0.00064
A2	0.00062	0.00075
B	0.00059	0.00071
C	0.00061	0.00074

Max Leakage Power (uW)

V1	V2
0.00402503	0.00574641

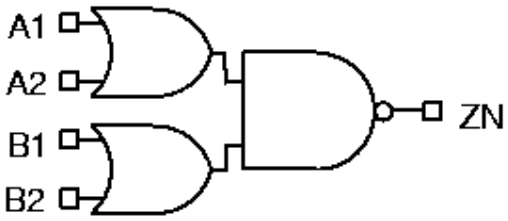
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.02497	0.02286
A1→ZN_RISE	0.02944	0.02630
A2→ZN_FALL	0.02729	0.02541
A2→ZN_RISE	0.03148	0.02851
B→ZN_FALL	0.01960	0.01764
B→ZN_RISE	0.01329	0.01183
C→ZN_FALL	0.02176	0.01995
C→ZN_RISE	0.01422	0.01277

LVT_OAI22HS

Cell Description

2-2 OAI
ZN=(!((A1|A2)&(B1|B2)))



Function Table

A1	A2	B1	B2	ZN
0	0	X	X	1
0	1	0	0	1
0	1	0	1	0
0	1	1	X	0
1	X	0	0	1
1	X	0	1	0
1	X	1	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_OAI22HSV1	1.26	0.98
LVT_OAI22HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00031	0.00038
A2	0.00038	0.00048
B1	0.00048	0.00062
B2	0.00055	0.00071

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00058	0.00069
A2	0.00055	0.00066
B1	0.00054	0.00065
B2	0.00061	0.00075

Max Leakage Power (uW)

V1	V2
0.00297488	0.00425719

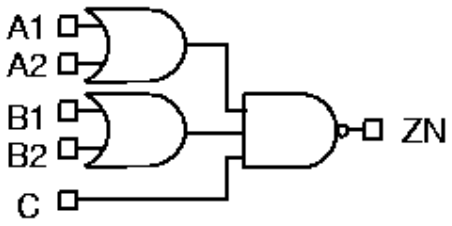
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.01344	0.01200
A1→ZN_RISE	0.02085	0.01790
A2→ZN_FALL	0.01505	0.01360
A2→ZN_RISE	0.02339	0.02039
B1→ZN_FALL	0.01766	0.01626
B1→ZN_RISE	0.02822	0.02523
B2→ZN_FALL	0.01898	0.01771
B2→ZN_RISE	0.03022	0.02749

LVT_OAI221HS

Cell Description

2-2-1 OAI
ZN=(!((A1|A2)&(B1|B2)&C))



Function Table

A1	A2	B1	B2	C	ZN
0	0	X	X	X	1
0	1	0	0	X	1
0	1	0	1	0	1
0	1	0	1	1	0
0	1	1	X	0	1
0	1	1	X	1	0
1	X	0	0	X	1
1	X	0	1	0	1
1	X	0	1	1	0
1	X	1	X	0	1
1	X	1	X	1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_OAI221HSV1	1.26	1.26
LVT_OAI221HSV2	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00050	0.00064
A2	0.00057	0.00074
B1	0.00067	0.00085
B2	0.00073	0.00094
C	0.00041	0.00052

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00055	0.00065
A2	0.00061	0.00073

B1	0.00057	0.00067
B2	0.00062	0.00074
C	0.00072	0.00088

Max Leakage Power (uW)

V1	V2
0.00354444	0.00505340

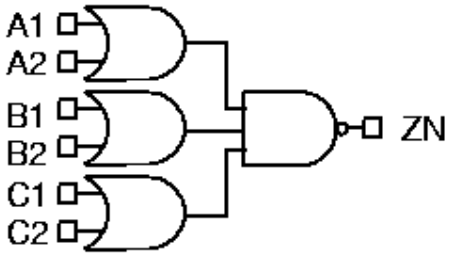
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.02547	0.02339
A1→ZN_RISE	0.02879	0.02554
A2→ZN_FALL	0.02816	0.02623
A2→ZN_RISE	0.03127	0.02808
B1→ZN_FALL	0.02984	0.02746
B1→ZN_RISE	0.03505	0.03120
B2→ZN_FALL	0.03203	0.02991
B2→ZN_RISE	0.03688	0.03322
C→ZN_FALL	0.02161	0.01971
C→ZN_RISE	0.01509	0.01346

LVT_OAI222HS

Cell Description

2-2-2 OAI
ZN=(!((A1|A2)&(B1|B2)&(C1|C2)))



Function Table

A1	A2	B1	B2	C1	C2	ZN
0	0	X	X	X	X	1
0	1	0	0	X	X	1
0	1	0	1	0	0	1
0	1	0	1	0	1	0
0	1	0	1	1	X	0
0	1	1	X	0	0	1
0	1	1	X	0	1	0
0	1	1	X	1	X	0
1	X	0	0	X	X	1
1	X	0	1	0	0	1
1	X	0	1	0	1	0
1	X	0	1	1	X	0
1	X	1	X	0	0	1
1	X	1	X	0	1	0
1	X	1	X	1	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_OAI222HSV1	1.26	1.54
LVT_OAI222HSV2	1.26	1.54

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00061	0.00078
A2	0.00067	0.00086
B1	0.00076	0.00098
B2	0.00082	0.00108
C1	0.00044	0.00055
C2	0.00048	0.00062

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00059	0.00069
A2	0.00058	0.00070
B1	0.00055	0.00065
B2	0.00061	0.00074
C1	0.00073	0.00088
C2	0.00054	0.00066

Max Leakage Power (uW)

V1	V2
0.00384486	0.00548614

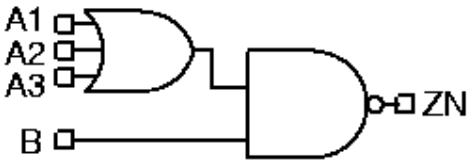
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.02758	0.02542
A1→ZN_RISE	0.03266	0.02918
A2→ZN_FALL	0.02948	0.02761
A2→ZN_RISE	0.03429	0.03105
B1→ZN_FALL	0.03141	0.02943
B1→ZN_RISE	0.03817	0.03469
B2→ZN_FALL	0.03336	0.03154
B2→ZN_RISE	0.04006	0.03677
C1→ZN_FALL	0.02186	0.01948
C1→ZN_RISE	0.02640	0.02284
C2→ZN_FALL	0.02201	0.01998
C2→ZN_RISE	0.02701	0.02377

LVT_OAI31HS

Cell Description

3-1 OAI
ZN=(!((A1|A2|A3)&B))



Function Table

A1	A2	A3	B	ZN
0	0	0	X	1
0	0	1	0	1
0	0	1	1	0
0	1	X	0	1
0	1	X	1	0
1	X	X	0	1
1	X	X	1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_OAI31HSV1	1.26	0.98
LVT_OAI31HSV2	1.26	0.98

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00039	0.00052
A2	0.00046	0.00061
A3	0.00053	0.00070
B	0.00029	0.00037

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00055	0.00069
A2	0.00056	0.00068
A3	0.00061	0.00075
B	0.00056	0.00069

Max Leakage Power (uW)

V1	V2
0.00253953	0.00362056

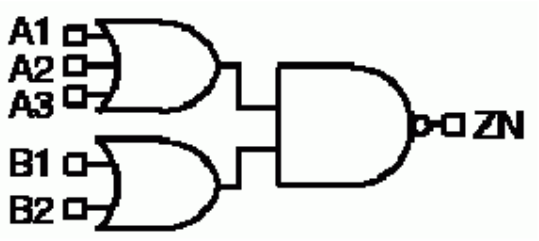
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.01642	0.01533
A1→ZN_RISE	0.03586	0.03255
A2→ZN_FALL	0.01805	0.01688
A2→ZN_RISE	0.04004	0.03667
A3→ZN_FALL	0.01884	0.01763
A3→ZN_RISE	0.04178	0.03847
B→ZN_FALL	0.01237	0.01131
B→ZN_RISE	0.01178	0.01054

LVT_OAI32HS

Cell Description

3-2 OAI
ZN=(!((A1|A2|A3)&(B1|B2)))



Function Table

A1	A2	A3	B1	B2	ZN
0	0	0	X	X	1
0	0	1	0	0	1
0	0	1	0	1	0
0	0	1	1	X	0
0	1	X	0	0	1
0	1	X	0	1	0
0	1	X	1	X	0
1	X	X	0	0	1
1	X	X	0	1	0
1	X	X	1	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_OAI32HSV1	1.26	1.12
LVT_OAI32HSV2	1.26	1.12

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00039	0.00048
A2	0.00045	0.00057
A3	0.00054	0.00068
B1	0.00059	0.00074
B2	0.00066	0.00084

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00055	0.00065
A2	0.00055	0.00066
A3	0.00058	0.00070

B1	0.00054	0.00064
B2	0.00062	0.00075

Max Leakage Power (uW)

V1	V2
0.00345505	0.00465868

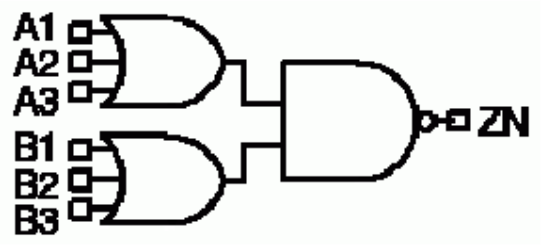
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.01481	0.01327
A1→ZN_RISE	0.03290	0.02810
A2→ZN_FALL	0.01642	0.01498
A2→ZN_RISE	0.03734	0.03275
A3→ZN_FALL	0.01813	0.01650
A3→ZN_RISE	0.04110	0.03610
B1→ZN_FALL	0.01892	0.01732
B1→ZN_RISE	0.03220	0.02855
B2→ZN_FALL	0.02034	0.01887
B2→ZN_RISE	0.03431	0.03088

LVT_OAI33HS

Cell Description

3-3 OAI
ZN=(!((A1|A2|A3)&(B1|B2|B3)))



Function Table

A1	A2	A3	B1	B2	B3	ZN
0	0	0	X	X	X	1
0	0	1	0	0	0	1
0	0	1	0	0	1	0
0	0	1	0	1	X	0
0	0	1	1	X	X	0
0	1	X	0	0	0	1
0	1	X	0	0	1	0
0	1	X	0	1	X	0
0	1	X	1	X	X	0
1	X	X	0	0	0	1
1	X	X	0	0	1	0
1	X	X	0	1	X	0
1	X	X	1	X	X	0

Cell Size

CellName	Height(um)	Width(um)
LVT_OAI33HSV1	1.26	1.26
LVT_OAI33HSV2	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00061	0.00076
A2	0.00068	0.00086
A3	0.00075	0.00095
B1	0.00040	0.00050
B2	0.00047	0.00059
B3	0.00055	0.00070

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00053	0.00063
A2	0.00061	0.00073
A3	0.00062	0.00074
B1	0.00057	0.00068
B2	0.00056	0.00067
B3	0.00057	0.00068

Max Leakage Power (uW)

V1	V2
0.00349411	0.00502011

Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.01933	0.01760
A1→ZN_RISE	0.04750	0.04179
A2→ZN_FALL	0.02082	0.01920
A2→ZN_RISE	0.05180	0.04640
A3→ZN_FALL	0.02188	0.02015
A3→ZN_RISE	0.05384	0.04819
B1→ZN_FALL	0.01438	0.01295
B1→ZN_RISE	0.03284	0.02797
B2→ZN_FALL	0.01595	0.01453
B2→ZN_RISE	0.03753	0.03273
B3→ZN_FALL	0.01734	0.01574
B3→ZN_RISE	0.04054	0.03533

LVT_OR2HS

Cell Description

2-Input OR
Z=(A1|A2)

Function Table

A1	A2	Z
0	0	0
0	1	1
1	X	1

Cell Size

CellName	Height(um)	Width(um)
LVT_OR2HSV1	1.26	0.84
LVT_OR2HSV2	1.26	0.84
LVT_OR2HSV8	1.26	1.26

Pin Power (uW/MHz)

Pin	V1	V2	V8
A1	0.00064	0.00074	0.00224
A2	0.00071	0.00080	0.00234

Pin Capacitance (pf)

Pin	V1	V2	V8
A1	0.00049	0.00048	0.00068
A2	0.00051	0.00051	0.00074

Max Leakage Power (uW)

V1	V2	V8
0.00254751	0.00271990	0.01120697

Delay Table (ns)

Description	V1	V2	V8
A1→Z_FALL	0.03846	0.04009	0.04721

A1→Z_RISE	0.02305	0.02284	0.02291
A2→Z_FALL	0.04246	0.04381	0.04989
A2→Z_RISE	0.02482	0.02444	0.02402

LVT_OR3HS

Cell Description

3-Input OR
Z=(A1|A2|A3)

Function Table

A1	A2	A3	Z
0	0	0	0
0	0	1	1
0	1	X	1
1	X	X	1

Cell Size

CellName	Height(um)	Width(um)
LVT_OR3HSV1	1.26	0.98
LVT_OR3HSV2	1.26	0.98
LVT_OR3HSV8	1.26	1.54

Pin Power (uW/MHz)

Pin	V1	V2	V8
A1	0.00078	0.00089	0.00262
A2	0.00088	0.00099	0.00272
A3	0.00099	0.00110	0.00283

Pin Capacitance (pf)

Pin	V1	V2	V8
A1	0.00056	0.00057	0.00065
A2	0.00060	0.00060	0.00070
A3	0.00063	0.00064	0.00072

Max Leakage Power (uW)

V1	V2	V8
0.00371385	0.00417243	0.01355793

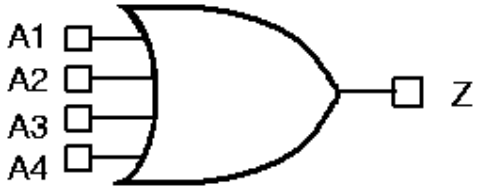
Delay Table (ns)

Description	V1	V2	V8
A1→Z_FALL	0.03860	0.04006	0.06958
A1→Z_RISE	0.02689	0.02667	0.02407
A2→Z_FALL	0.04307	0.04459	0.07405
A2→Z_RISE	0.02903	0.02881	0.02487
A3→Z_FALL	0.04624	0.04764	0.07685
A3→Z_RISE	0.03132	0.03106	0.02585

LVT_OR4HS

Cell Description

4-Input OR
Z=(A1|A2|A3|A4)



Function Table

A1	A2	A3	A4	Z
0	0	0	0	0
0	0	0	1	1
0	0	1	X	1
0	1	X	X	1
1	X	X	X	1

Cell Size

CellName	Height(um)	Width(um)
LVT_OR4HSV1	1.26	1.12
LVT_OR4HSV2	1.26	1.12
LVT_OR4HSV8	1.26	1.68

Pin Power (uW/MHz)

Pin	V1	V2	V8
A1	0.00082	0.00091	0.00286
A2	0.00093	0.00102	0.00296
A3	0.00102	0.00111	0.00307
A4	0.00113	0.00122	0.00318

Pin Capacitance (pf)

Pin	V1	V2	V8
A1	0.00056	0.00056	0.00065
A2	0.00061	0.00058	0.00068
A3	0.00059	0.00060	0.00068
A4	0.00062	0.00062	0.00072

Max Leakage Power (uW)

V1	V2	V8

0.00439931	0.00489348	0.01498753

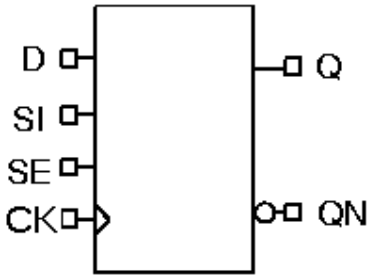
Delay Table (ns)

Description	V1	V2	V8
A1→Z_FALL	0.04841	0.04921	0.08932
A1→Z_RISE	0.02803	0.02708	0.02422
A2→Z_FALL	0.05655	0.05695	0.09706
A2→Z_RISE	0.03047	0.02943	0.02512
A3→Z_FALL	0.06025	0.06129	0.10138
A3→Z_RISE	0.03211	0.03142	0.02592
A4→Z_FALL	0.06402	0.06450	0.10480
A4→Z_RISE	0.03394	0.03291	0.02673

LVT_SDHS

Cell Description

Scan D Flip-Flop
Q = rising (CK) ? (SE&SI | !SE&D) : pre_Q
QN = !Q



Function Table

CK<1>	CK	SE	SI	D	Q
0	0	X	X	X	Q<1>
0	1	0	X	0	0
0	1	0	X	1	1
0	1	1	0	X	0
0	1	1	1	X	1
1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_SDHSV1	1.26	4.20
LVT_SDHSV2	1.26	4.06

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00158	0.00158
D	0.00035	0.00035
Q	0.00095	0.00105
QN	0.00096	0.00106
SE	0.00073	0.00073
SI	0.00040	0.00040

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00047	0.00047
D	0.00050	0.00050
SE	0.00105	0.00105
SI	0.00039	0.00039

Max Leakage Power (uW)

V1	V2
0.00670136	0.00705864

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.08662	0.08767
CK→Q_RISE	0.08397	0.08575
CK→QN_FALL	0.06365	0.06416
CK→QN_RISE	0.07119	0.07058

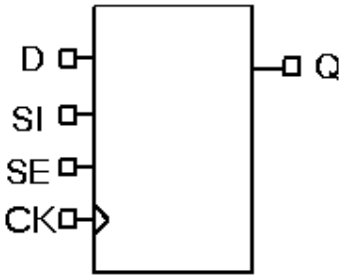
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.00857	-0.00857
D	hold_RISE→CK	-0.03150	-0.02863
D	setup_FALL→CK	0.03148	0.03148
D	setup_RISE→CK	0.04295	0.04295
SE	hold_FALL→CK	-0.01716	-0.01431
SE	hold_RISE→CK	-0.03721	-0.03721
SE	setup_FALL→CK	0.04294	0.04294
SE	setup_RISE→CK	0.05152	0.05439
SI	hold_FALL→CK	-0.03721	-0.03434
SI	hold_RISE→CK	-0.04294	-0.04009
SI	setup_FALL→CK	0.06583	0.06583
SI	setup_RISE→CK	0.05439	0.05726
CK	minpwh	0.06502	0.07137
CK	minpwl	0.10155	0.10555

LVT_SDQHS

Cell Description

Scan D Flip-Flop
Q = rising (CK) ? (SE&SI | !SE&D) : pre_Q



Function Table

CK<1>	CK	SE	D	SI	Q
0	0	X	X	X	Q<1>
0	1	0	0	X	0
0	1	0	1	X	1
0	1	1	X	0	0
0	1	1	X	1	1
1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_SDQHSV1	1.26	4.06
LVT_SDQHSV2	1.26	4.06

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00152	0.00152
D	0.00034	0.00034
Q	0.00144	0.00155
SE	0.00072	0.00072
SI	0.00039	0.00039

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00047	0.00047
D	0.00051	0.00051
SE	0.00104	0.00105
SI	0.00039	0.00040

Max Leakage Power (uW)

V1	V2
0.00555794	0.00565766

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.08117	0.08120
CK→Q_RISE	0.07740	0.07688

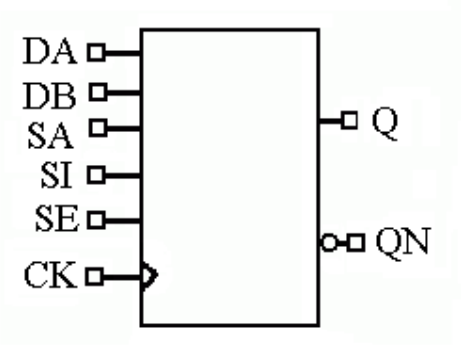
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.01144	-0.01144
D	hold_RISE→CK	-0.02863	-0.02863
D	setup_FALL→CK	0.03148	0.03148
D	setup_RISE→CK	0.03722	0.04009
SE	hold_FALL→CK	-0.01717	-0.01431
SE	hold_RISE→CK	-0.04007	-0.04006
SE	setup_FALL→CK	0.04008	0.04293
SE	setup_RISE→CK	0.05153	0.05438
SI	hold_FALL→CK	-0.04007	-0.03720
SI	hold_RISE→CK	-0.04294	-0.04294
SI	setup_FALL→CK	0.06298	0.06583
SI	setup_RISE→CK	0.05439	0.05726
CK	minpwh	0.04602	0.04602
CK	minpwl	0.09362	0.09362

LVT_SDXHS

Cell Description

Scan D Flip-Flop with Mux Inputs
Q = rising (CK) ? (SE&SI | !SE&(DA&SA|DB&!SA)) : pre_Q
QN = !Q



Function Table

CK<1>	CK	SA	DB	DA	SE	SI	Q
0	0	X	X	X	X	X	Q<1>
0	1	0	0	X	0	X	0
0	1	0	0	X	1	0	0
0	1	0	0	X	1	1	1
0	1	0	1	X	0	X	1
0	1	0	1	X	1	0	0
0	1	0	1	X	1	1	1
0	1	1	X	0	0	X	0
0	1	1	X	0	1	0	0
0	1	1	X	0	1	1	1
0	1	1	X	1	0	X	1
0	1	1	X	1	1	0	0
0	1	1	X	1	1	1	1
1	X	X	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_SDXHSV1	1.26	5.32
LVT_SDXHSV2	1.26	5.32

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00134	0.00134
DA	0.00020	0.00020
DB	0.00020	0.00020
Q	0.00094	0.00104
QN	0.00094	0.00105
SA	0.00054	0.00054
SE	0.00082	0.00082
SI	0.00045	0.00045

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00046	0.00046
DA	0.00046	0.00046
DB	0.00104	0.00104
SA	0.00097	0.00097
SE	0.00110	0.00110
SI	0.00042	0.00042

Max Leakage Power (uW)

V1	V2
0.00772587	0.00828107

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.08211	0.08336
CK→Q_RISE	0.08087	0.08236
CK→QN_FALL	0.06114	0.06129
CK→QN_RISE	0.06675	0.06550

Timing Constraints (ns)

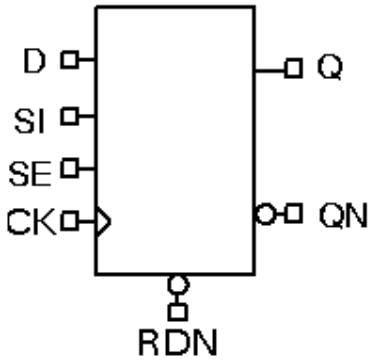
Pin	Requirement	V1	V2
DA	hold_FALL→CK	-0.02003	-0.02003
DA	hold_RISE→CK	-0.03720	-0.03720
DA	setup_FALL→CK	0.04292	0.04579
DA	setup_RISE→CK	0.04578	0.04866
DB	hold_FALL→CK	-0.02290	-0.02005
DB	hold_RISE→CK	-0.03721	-0.03433
DB	setup_FALL→CK	0.04580	0.04580
DB	setup_RISE→CK	0.04579	0.04579
SA	hold_FALL→CK	-0.04292	-0.04292
SA	hold_RISE→CK	-0.02290	-0.02290
SA	setup_FALL→CK	0.05439	0.05438
SA	setup_RISE→CK	0.04581	0.04865
SE	hold_FALL→CK	-0.01431	-0.01144
SE	hold_RISE→CK	-0.04293	-0.04007
SE	setup_FALL→CK	0.04293	0.04293
SE	setup_RISE→CK	0.05725	0.05725
SI	hold_FALL→CK	-0.04006	-0.03720
SI	hold_RISE→CK	-0.04581	-0.04581
SI	setup_FALL→CK	0.06869	0.06869
SI	setup_RISE→CK	0.06011	0.06302

CK	minpwh	0.06501	0.06819
CK	minpwl	0.09357	0.09355

LVT_SDRNHS

Cell Description

Scan D Flip-Flop with Async Clear
Q = !RDN ? 0 : rising (CK) ? (SE&SI | !SE&D) : pre_Q
QN = !Q



Function Table

RDN	CK<1>	CK	SE	SI	D	Q
0	X	X	X	X	X	0
1	0	0	X	X	X	Q<1>
1	0	1	0	X	0	0
1	0	1	0	X	1	1
1	0	1	1	0	X	0
1	0	1	1	1	X	1
1	1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_SDRNHSV1	1.26	5.04
LVT_SDRNHSV2	1.26	5.04

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00176	0.00176
D	0.00021	0.00021
Q	0.00119	0.00129
QN	0.00123	0.00133
RDN	0.00048	0.00048
SE	0.00052	0.00052
SI	0.00025	0.00025

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00047	0.00047
D	0.00041	0.00040
RDN	0.00180	0.00180
SE	0.00084	0.00084

SI	0.00035	0.00036

Max Leakage Power (uW)

V1	V2
0.00903607	0.00948114

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.08683	0.08798
CK→Q_RISE	0.09246	0.09466
RDN→Q_FALL	0.02375	0.02362
CK→QN_FALL	0.06369	0.06467
CK→QN_RISE	0.07097	0.07039
RDN→QN_RISE	0.07195	0.07264

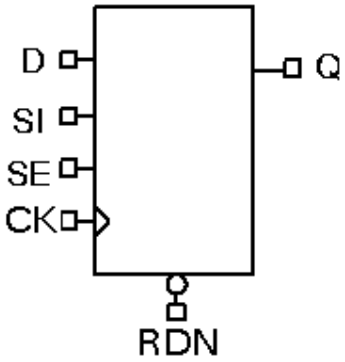
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.02005	-0.01719
D	hold_RISE→CK	-0.04867	-0.04579
D	setup_FALL→CK	0.05440	0.05726
D	setup_RISE→CK	0.07157	0.07156
RDN	setup_RISE→CK	0.08874	0.09159
RDN	hold_RISE→CK	-0.08015	-0.08016
SE	hold_FALL→CK	-0.02576	-0.02290
SE	hold_RISE→CK	-0.05152	-0.04867
SE	setup_FALL→CK	0.07156	0.07443
SE	setup_RISE→CK	0.07728	0.07729
SI	hold_FALL→CK	-0.04008	-0.03723
SI	hold_RISE→CK	-0.05725	-0.05724
SI	setup_FALL→CK	0.08302	0.08303
SI	setup_RISE→CK	0.08303	0.08588
CK	minpwh	0.06826	0.07140
CK	minpwl	0.11744	0.11741
RDN	minpwl	0.04602	0.04604

LVT_SDRNQHS

Cell Description

Scan D Flip-Flop with Async Clear
Q = !RDN ? 0 : rising (CK) ? (SE&SI | !SE&D) : pre_Q



Function Table

RDN	CK<1>	CK	SE	D	SI	Q
0	X	X	X	X	X	0
1	0	0	X	X	X	Q<1>
1	0	1	0	0	X	0
1	0	1	0	1	X	1
1	0	1	1	X	0	0
1	0	1	1	X	1	1
1	1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_SDRNQHSV1	1.26	4.76
LVT_SDRNQHSV2	1.26	4.76

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00172	0.00172
D	0.00021	0.00021
Q	0.00189	0.00197
RDN	0.00047	0.00047
SE	0.00057	0.00057
SI	0.00024	0.00024

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00048	0.00048
D	0.00042	0.00042
RDN	0.00166	0.00166
SE	0.00109	0.00109
SI	0.00036	0.00036

Max Leakage Power (uW)

V1	V2
0.00699163	0.00720967

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.08295	0.08279
CK→Q_RISE	0.08037	0.07979
RDN→Q_FALL	0.04032	0.04091

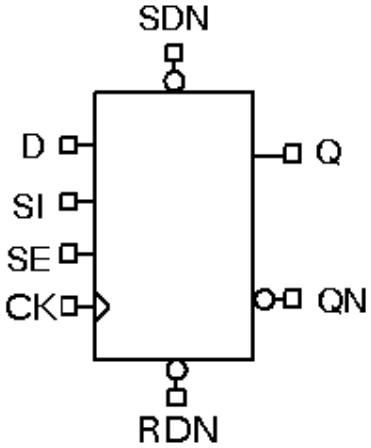
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.02291	-0.02005
D	hold_RISE→CK	-0.04580	-0.04580
D	setup_FALL→CK	0.04867	0.04867
D	setup_RISE→CK	0.06297	0.06583
RDN	setup_RISE→CK	0.08586	0.08875
RDN	hold_RISE→CK	-0.08015	-0.08016
SE	hold_FALL→CK	-0.02863	-0.02577
SE	hold_RISE→CK	-0.05727	-0.05727
SE	setup_FALL→CK	0.05726	0.06011
SE	setup_RISE→CK	0.07730	0.08016
SI	hold_FALL→CK	-0.04867	-0.04579
SI	hold_RISE→CK	-0.06299	-0.06299
SI	setup_FALL→CK	0.07729	0.07730
SI	setup_RISE→CK	0.08017	0.08303
CK	minpwh	0.04600	0.04600
CK	minpwl	0.10950	0.11342
RDN	minpwl	0.05555	0.05870

LVT_SDRSNHS

Cell Description

Scan D Flip-Flop with Async Clear and Set
Q = !SDN ? 1 : !RDN ? 0 : rising (CK) ? (SE&SI | !SE&D) : pre_Q
QN = !Q



Function Table

RDN	SDN	CK<1>	CK	SE	D	SI	Q
0	0	X	X	X	X	X	1
0	1	X	X	X	X	X	0
1	0	X	X	X	X	X	1
1	1	0	0	X	X	X	Q<1>
1	1	0	1	0	0	X	0
1	1	0	1	0	1	X	1
1	1	0	1	1	X	0	0
1	1	0	1	1	X	1	1
1	1	1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_SDRSNHSV1	1.26	7.14
LVT_SDRSNHSV2	1.26	7.14

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00220	0.00220
D	0.00019	0.00019
Q	0.00140	0.00148
QN	0.00140	0.00150
RDN	0.00110	0.00110
SDN	0.00019	0.00019
SE	0.00055	0.00055
SI	0.00022	0.00022

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00065	0.00065

D	0.00050	0.00050
RDN	0.00114	0.00114
SDN	0.00089	0.00089
SE	0.00099	0.00099
SI	0.00041	0.00041

Max Leakage Power (uW)

V1	V2
0.00758988	0.00830893

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.11238	0.11257
CK→Q_RISE	0.10200	0.10259
RDN→Q_FALL	0.10055	0.10067
SDN→Q_FALL	0.07214	0.07229
SDN→Q_RISE	0.07530	0.07549
CK→QN_FALL	0.08304	0.08153
CK→QN_RISE	0.09148	0.08988
RDN→QN_RISE	0.07967	0.07806
SDN→QN_FALL	0.05649	0.05451
SDN→QN_RISE	0.05119	0.04957

Timing Constraints (ns)

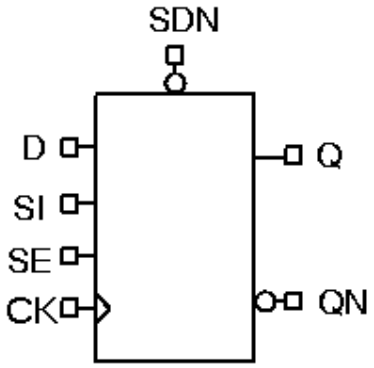
Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.01432	-0.01145
D	hold_RISE→CK	-0.06298	-0.06012
D	setup_FALL→CK	0.05727	0.05727
D	setup_RISE→CK	0.08301	0.08589
RDN	setup_RISE→CK	0.10018	0.10305
RDN	hold_RISE→CK	-0.08873	-0.08873
SDN	setup_RISE→CK	-0.04865	-0.04580
SDN	hold_RISE→CK	0.06296	0.06296
SDN	non_seq_hold_RISE→RDN	-0.03436	-0.03436
SDN	non_seq_setup_RISE→RDN	0.04009	0.04580
SE	hold_FALL→CK	-0.01715	-0.01429
SE	hold_RISE→CK	-0.06584	-0.06584
SE	setup_FALL→CK	0.06868	0.07155
SE	setup_RISE→CK	0.09161	0.09445
SI	hold_FALL→CK	-0.02864	-0.02577
SI	hold_RISE→CK	-0.07727	-0.07727
SI	setup_FALL→CK	0.06870	0.07157
SI	setup_RISE→CK	0.10017	0.10305

CK	minpwh	0.08725	0.09044
CK	minpwl	0.13727	0.14122
RDN	minpwl	0.06820	0.07139
SDN	minpwl	0.09038	0.09672

LVT_SDSNHS

Cell Description

Scan D Flip-Flop with Async Set
Q = !SDN ? 1 : rising (CK) ? (SE&SI | !SE&D) : pre_Q
QN = !Q



Function Table

SDN	CK<1>	CK	SE	SI	D	Q
0	X	X	X	X	X	1
1	0	0	X	X	X	Q<1>
1	0	1	0	X	0	0
1	0	1	0	X	1	1
1	0	1	1	0	X	0
1	0	1	1	1	X	1
1	1	X	X	X	X	Q<1>

Cell Size

CellName	Height(um)	Width(um)
LVT_SDSNHSV1	1.26	4.76
LVT_SDSNHSV2	1.26	4.76

Pin Power (uW/MHz)

Pin	V1	V2
CK	0.00173	0.00174
D	0.00028	0.00028
Q	0.00123	0.00132
QN	0.00123	0.00134
SDN	0.00014	0.00014
SE	0.00060	0.00061
SI	0.00032	0.00032

Pin Capacitance (pf)

Pin	V1	V2
CK	0.00048	0.00048
D	0.00050	0.00051
SDN	0.00093	0.00094
SE	0.00097	0.00097

SI	0.00038	0.00038

Max Leakage Power (uW)

V1	V2
0.00776924	0.00803439

Delay Table (ns)

Description	V1	V2
CK→Q_FALL	0.09616	0.09695
CK→Q_RISE	0.09150	0.09281
SDN→Q_RISE	0.07264	0.07364
CK→QN_FALL	0.07340	0.07222
CK→QN_RISE	0.07759	0.07705
SDN→QN_FALL	0.05491	0.05347

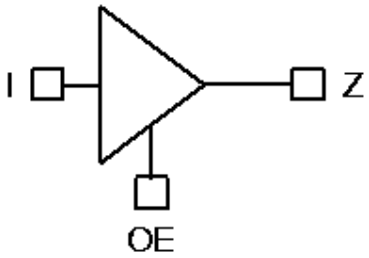
Timing Constraints (ns)

Pin	Requirement	V1	V2
D	hold_FALL→CK	-0.01145	-0.00858
D	hold_RISE→CK	-0.02864	-0.02864
D	setup_FALL→CK	0.03720	0.03721
D	setup_RISE→CK	0.04295	0.04295
SDN	setup_RISE→CK	-0.03722	-0.03435
SDN	hold_RISE→CK	0.04294	0.04294
SE	hold_FALL→CK	-0.01431	-0.01431
SE	hold_RISE→CK	-0.04007	-0.03722
SE	setup_FALL→CK	0.04578	0.04866
SE	setup_RISE→CK	0.05438	0.05439
SI	hold_FALL→CK	-0.03722	-0.03436
SI	hold_RISE→CK	-0.04295	-0.04294
SI	setup_FALL→CK	0.06585	0.06871
SI	setup_RISE→CK	0.06012	0.06012
CK	minpwh	0.07774	0.08408
CK	minpwl	0.10949	0.10949
SDN	minpwl	0.08090	0.08725

LVT_TBUFHS

Cell Description

3-State Buffer with High Enable
Z=!OE ? I:(1'bZ)



Function Table

OE	I	Z
0	X	Z
1	0	0
1	1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_TBUFHSV1	1.26	1.26
LVT_TBUFHSV2	1.26	1.54
LVT_TBUFHSV3	1.26	1.54
LVT_TBUFHSV6	1.26	1.82
LVT_TBUFHSV8	1.26	2.10
LVT_TBUFHSV12	1.26	2.52
LVT_TBUFHSV16	1.26	2.94
LVT_TBUFHSV20	1.26	3.50
LVT_TBUFHSV24	1.26	4.06

Pin Power (uW/MHz)

Pin	V1	V2	V3	V6	V8	V12	V16	V20
I	0.00089	0.00110	0.00123	0.00192	0.00237	0.00330	0.00411	0.00528
OE	0.00060	0.00079	0.00091	0.00152	0.00191	0.00270	0.00338	0.00430

Pin	V24
I	0.00657
OE	0.00530

Pin Capacitance (pf)

Pin	V1	V2	V3	V6	V8	V12	V16	V20
I	0.00050	0.00047	0.00047	0.00048	0.00047	0.00050	0.00047	0.00049
OE	0.00093	0.00091	0.00091	0.00092	0.00091	0.00093	0.00092	0.00093

Pin	V24
I	0.00048
OE	0.00093

Max Leakage Power (uW)

V1	V2	V3	V6	V8	V12	V16	V20
0.00267368	0.00393795	0.00496000	0.00877629	0.01166890	0.01796069	0.02412397	0.03079030

V24
0.03866697

Delay Table (ns)

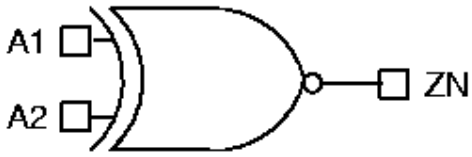
Description	V1	V2	V3	V6	V8	V12	V16	V20
I→Z_FALL	0.04645	0.04606	0.04707	0.05878	0.06525	0.08178	0.09375	0.11001
I→Z_RISE	0.03931	0.03787	0.03803	0.04642	0.05137	0.06346	0.07208	0.08367
OE→Z_FALL	0.02763	0.02710	0.02730	0.03210	0.03478	0.04157	0.04655	0.05319
OE→Z_RISE	0.02797	0.02749	0.02757	0.03175	0.03417	0.03986	0.04367	0.04886

Description	V24
I→Z_FALL	0.12742
I→Z_RISE	0.09570
OE→Z_FALL	0.06042
OE→Z_RISE	0.05443

LVT_XNOR2HS

Cell Description

2-Input Exclusive NOR
ZN=(!(A1^A2))



Function Table

A2	A1	ZN
0	0	1
0	1	0
1	0	0
1	1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_XNOR2HSV1	1.26	1.96
LVT_XNOR2HSV2	1.26	1.96

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00113	0.00120
A2	0.00189	0.00199

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00104	0.00105
A2	0.00067	0.00066

Max Leakage Power (uW)

V1	V2
0.00455746	0.00461396

Delay Table (ns)

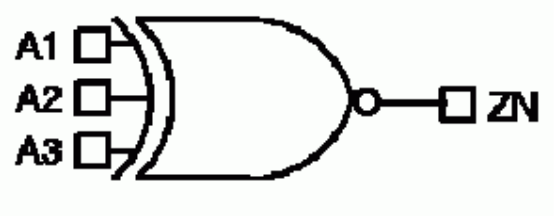
Description	V1	V2
A1→ZN_FALL	0.03211	0.03262

A1→ZN_RISE	0.03351	0.03297
A2→ZN_FALL	0.05161	0.05246
A2→ZN_RISE	0.04912	0.04878

LVT_XNOR3HS

Cell Description

3-Input Exclusive NOR
ZN=(!(A1^A2^A3))



Function Table

A2	A1	A3	ZN
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_XNOR3HSV1	1.26	3.08
LVT_XNOR3HSV2	1.26	3.08

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00311	0.00315
A2	0.00225	0.00229
A3	0.00106	0.00109

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00067	0.00067
A2	0.00105	0.00105
A3	0.00103	0.00104

Max Leakage Power (uW)

V1	V2

0.00999257	0.01011306

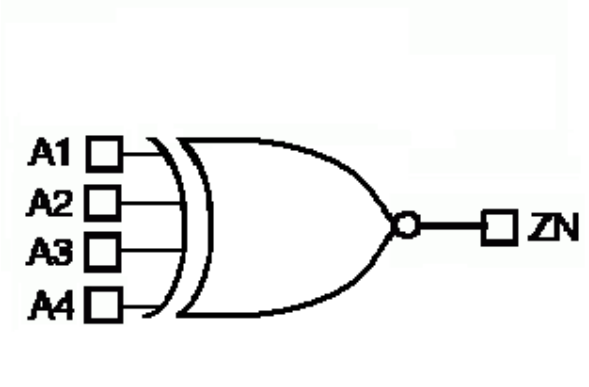
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.08144	0.08306
A1→ZN_RISE	0.08020	0.07909
A2→ZN_FALL	0.06316	0.06468
A2→ZN_RISE	0.06121	0.06007
A3→ZN_FALL	0.03149	0.03263
A3→ZN_RISE	0.03047	0.02956

LVT_XNOR4HS

Cell Description

4-Input Exclusive NOR
ZN=(!(A1^A2^A3^A4))



Function Table

A2	A1	A3	A4	ZN
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_XNOR4HSV1	1.26	5.46
LVT_XNOR4HSV2	1.26	5.46

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00327	0.00335
A2	0.00400	0.00407
A3	0.00281	0.00280
A4	0.00350	0.00346

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00104	0.00106
A2	0.00067	0.00068
A3	0.00109	0.00109
A4	0.00067	0.00067

Max Leakage Power (uW)

V1	V2
0.01249909	0.01304464

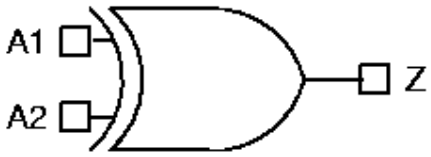
Delay Table (ns)

Description	V1	V2
A1→ZN_FALL	0.08784	0.08637
A1→ZN_RISE	0.08604	0.08490
A2→ZN_FALL	0.10612	0.10446
A2→ZN_RISE	0.10432	0.10298
A3→ZN_FALL	0.07401	0.07259
A3→ZN_RISE	0.07595	0.07353
A4→ZN_FALL	0.09188	0.09024
A4→ZN_RISE	0.09389	0.09121

LVT_XOR2HS

Cell Description

2-Input Exclusive OR
Z=(A1^A2)



Function Table

A2	A1	Z
0	0	0
0	1	1
1	0	1
1	1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_XOR2HSV1	1.26	1.96
LVT_XOR2HSV2	1.26	1.96

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00112	0.00120
A2	0.00187	0.00195

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00104	0.00103
A2	0.00067	0.00067

Max Leakage Power (uW)

V1	V2
0.00483773	0.00483708

Delay Table (ns)

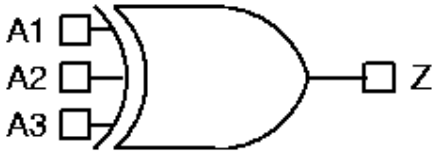
Description	V1	V2
A1→Z_FALL	0.03218	0.03285

A1→Z_RISE	0.03327	0.03292
A2→Z_FALL	0.05140	0.05205
A2→Z_RISE	0.04908	0.04866

LVT_XOR3HS

Cell Description

3-Input Exclusive OR
Z=(A1^A2^A3)



Function Table

A2	A1	A3	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Cell Size

CellName	Height(um)	Width(um)
LVT_XOR3HSV1	1.26	3.08
LVT_XOR3HSV2	1.26	3.08

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00317	0.00322
A2	0.00230	0.00235
A3	0.00104	0.00108

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00067	0.00067
A2	0.00105	0.00105
A3	0.00102	0.00102

Max Leakage Power (uW)

V1	V2

0.01023824	0.01023774

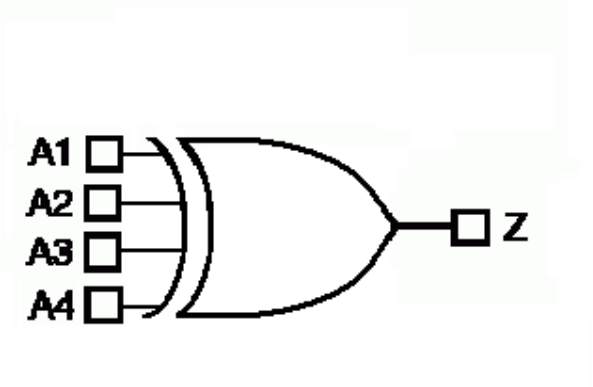
Delay Table (ns)

Description	V1	V2
A1→Z_FALL	0.08410	0.08567
A1→Z_RISE	0.08115	0.07973
A2→Z_FALL	0.06571	0.06722
A2→Z_RISE	0.06224	0.06082
A3→Z_FALL	0.02968	0.03090
A3→Z_RISE	0.03032	0.02903

LVT_XOR4HS

Cell Description

4-Input Exclusive OR
Z=(A1^A2^A3^A4)



Function Table

A2	A1	A3	A4	Z
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Cell Size

CellName	Height(um)	Width(um)
LVT_XOR4HSV1	1.26	5.32
LVT_XOR4HSV2	1.26	5.32

Pin Power (uW/MHz)

Pin	V1	V2
A1	0.00338	0.00348
A2	0.00410	0.00420
A3	0.00291	0.00300
A4	0.00359	0.00367

Pin Capacitance (pf)

Pin	V1	V2
A1	0.00106	0.00106
A2	0.00068	0.00067
A3	0.00105	0.00105
A4	0.00068	0.00067

Max Leakage Power (uW)

V1	V2
0.01390013	0.01414299

Delay Table (ns)

Description	V1	V2
A1→Z_FALL	0.08971	0.09063
A1→Z_RISE	0.08773	0.08711
A2→Z_FALL	0.10787	0.10872
A2→Z_RISE	0.10590	0.10521
A3→Z_FALL	0.07523	0.07555
A3→Z_RISE	0.07748	0.07646
A4→Z_FALL	0.09357	0.09375
A4→Z_RISE	0.09591	0.09474