CSMC 0.153um CMOS EN Process 5V

High Density 7-track

Standard Cell Library

Version 1.0

2019

CSMC Corp.

Notice

Disclaimer

CSMC CORPORATION RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS DESCRIBED HEREIN. CSMC CORPORATION MAKES NO WARRANTY, REPRESENTATION, OR GUARANTEE REGARDING THE SUITABILITY OF ITS PRODUCTS FOR ANY PARTICULAR PURPOSE, NOR DOES CSMC CORPORATION ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT, AND SPECIFICALLY DISCLAIMS ANY AND ALL LIABILITY, INCLUDING WITHOUT LIMITATION, CONSEQUENTIAL OR INCIDENTAL DAMAGES.

Proprietary Rights Notice

This document contains information of a proprietary nature. No part of this manual may be copied or distributed without the prior written consent of CSMC corporation. This document and the software described herein is only provided under a written license agreement or a type of written non-disclosure agreement with CSMC corporation or its subsidiaries. ALL INFORMATION CONTAINED HEREIN SHALL BE KEPT IN CONFIDENCE AND USED STRICTLY IN ACCORDANCE WITH THE TERMS OF THE WRITTEN NON-DISCLOSURE AGREEMENT OR WRITTEN LICENSE AGREEMENT WITH CSMC CORPORATION OR ITS SUBSIDIARIES.

Trademark/Service-Mark Notice

Planet, Planet-PL, Planet-RTL, Solar, Star-Sim, Star-Hspice, HSPICE, Star-HspiceLink, HSPICE-LINK, AvanWaves, Sirius, Star-DC, Star-RC, Star-Power, Star-MTB, MASTER Toolbox, Hercules, LTL, Passport, V- Formal, Lynx-VHDL, laybool, Lynx-LB, Datapath Compiler, Chip Compiler, PathFinder, ChipPlanner, DesignVP, Optimum Silicone, QTV, Polaris, Polaris-CBS, Polaris-MT, Device Model Builder (DMB), Avan Test-chip, ArcCell, ArcChip, ArcUtil, ADM, ATEM, Evaccess, Explorer, Pure Speed, CycleLink, BaseLine, SimLine, DriveLine, Dynamic Model Switcher, Base Line Software Accelerator, Smart Extraction, VeriView, VeriCheck, Chips Crunch, and Time are trademarks of CSMC Corporation and its subsidiaries.

CSMC Corporation, CSMC logo, and AvanLabs are trademarks and service-marks of CSMC Corporation.

All other trademarks are the property of their respective owners.

Revision History

Document Version Number	Date	Notes
1.0	July.25th,2019	Initial Production Release

Table of content

Introduction

This manual addresses the design engineer who is doing a preliminary feasibility evaluation and wishes to make comparisons among the available technologies. Additionally, you can use this library manual while designing a chip, to see which cells are available, and to check the power consumption, critical timing values, propagation delay equations, and functions of a cell.

The datasheets only show individual pin-to-pin timings for the storage elements. For other cells, the delays in the datasheets are combined as typical-case delays for the purpose of readability.

Product Description

The Synthesis Standard Cell Library is a new set of standard cells that replaces the current high-density and high-performance standard cell sets. The cell set functionality and drive strengths are optimized for industry standard synthesis design entry using Verilog or VHDL driving Synopsys or the ASIC Synthesizer. The cell layout is optimized for industry-leading, area-based routers.

The CSMC0153 Library is a high-performance, standard cell library in CSMC 0.153- micron CMOS EN process.

Contents of This Manual

This introduction contains the following sections:

- The *General Information* section of this book gives basic information on the conditions under which this library was characterized and offers assistance in using derating factors and estimating propagation delay.
- The *Cells* section describes the contents of the datasheets and how to interpret them. It also explains how to decode the cell names.
- The tables in the *Cell Matrices* section give a quick reference to the features of storage elements in the library.

Following this introduction, there are three sections:

- Simple Logic Gates - AND, AND-OR-Invert, NAND, NOR, OR, OR-AND- Invert, exclusive-OR, and exclusive-NOR gates; buffers, clock buffers and 3- state buffers with both active-high and active-low enables.
- Storage Elements - D flip-flops, JK flip-flops, latches, multiplexed flip-flops, latches, scan latches, and scan flip-flops.
- Special Functions - Adders, adder/subtractors, carry generators, multiplexers, and symbolic cells.

Within these divisions, the library cells are listed in alphabetical order where possible. Cells of a similar type have been combined. For example, the information for all the 2-input NAND gates - ND02D0, ND02D1, ND02D2, and ND02D4 - has been combined into one datasheet.

For storage elements, there is a cover page listing the common information for all cells of that type, then the following pages give information specific to individual cells in the grouping. For example, there is a cover page for D flip-flops with set and clear, then a page each on DFBRB1 and DFBRB2.

Buffers have been grouped together by type with different drive capabilities. For example, INV0D0, INV0D1, INV0D2, IN0VD4 and IN0VD8 have been combined on a single datasheet.

General Information

Recommended Operating Conditions

Table 1 shows the physical design specifications of this library.

Drawn Gate Length (um)	0.42/0.5
Layers of Metal	3,4, 5 or 6
Layout Grid (um)	0.001
Vertical Pin Grid (um)	0.476
Horizontal Pin Grid (um)	0.476
Cell height (um)	3.332
Cell Power and Ground Rail Width (um)	0.52

Table 1. Physical Specifications

In this library, all pins are located on the vertical and horizontal pin grids. Most
place-and-route tools work more efficiently with all pins on grids, and some tools
even require it.
The library also supports designs with four, five or six layers of metal. You may need to change the design rules in the technology file, because the top-level metal has a greater minimum width and greater minimum spacing requirement.

Table 2 describes the electrical specifications for this library.

Conner	**Minimum(0C)**	**Minimum(-40C)**	**TYPICAL**	**Maximum**
DC Supply Voltage (Vdd)	5.5v	5.5v	5v	2. 7v/1.8v/4.5v
Junction Temperature	$0^{o}C$	$-40^{o}C$	$25^{o}C$	$125^{o}C$

Table 2. Electrical Specifications

AC Characteristics

Timing Measurement Conditions

Unless otherwise specified:

VDD = 5volts

Junction Temperature = 25 degrees C

Process = typical case

AC Timing Definitions

Propagation Delay and Transition Time

The propagation delay through a cell is the sum of the intrinsic delay, theload dependent delay, and the input-slew dependent delay. Delays are defined as thetime interval between the input stimulus crossing 50% of Vdd and the output rossing 50% of Vdd. Figure 1 illustrates the propagation delay.

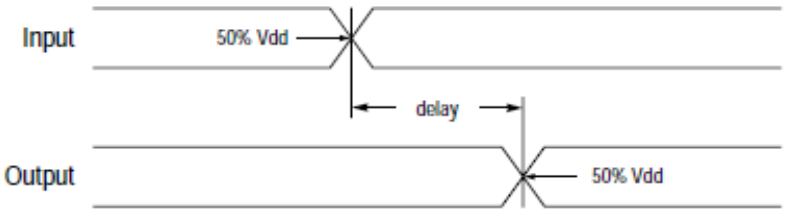


Figure 1. Propagation Delay

The transition times (slews) on input and output pins are defined as the timeinterval between the signal crossing 10% of Vdd and 90% of Vdd. Figure 2 llustrates transition time measurements for rising and falling signals.

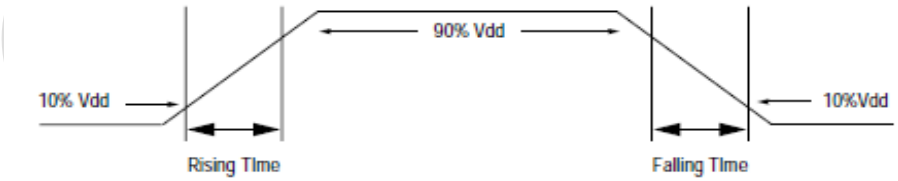


Figure 2. Transition Time

Timing Constraints

Timing constraints define minimum time intervals during which specific signals must be held steady in order to ensure the correct functioning of any given cell. Timing constraints include: setup time, hold time, recovery time, and minimum pulse width.

The sequential-cell timing models provided with this library include the effects of input-transition time and data-signal and clock-signal polarity on timing constraints.

Timing constraints can affect propagation delays. The intrinsic delays given in the datasheets are measured with relaxed timing constraints (longer

than necessary setup times, hold times, recovery times, and pulse widths). The use of shorter timing constraint intervals may increase delay. Each cell is considered functional as long as the actual delay does not exceed the delay given in the datasheets by more than 10%.

Setup Time

The setup time for a sequential cell is the minimum length of time the data-input signal must remain stable before the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large setup time) by more than 10%.

Setup constraint values are measured as the interval between the data signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd. For the measurement of setup time, the data input signal is kept stable after the active clock edge for an infinite hold time. Figure 3 illustrates setup time for a positive-edge-triggered sequential cell.

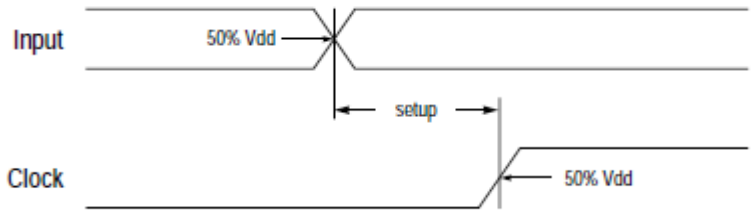


Figure 3. Setup Time

Hold Time

The hold time for a sequential cell is the minimum length of time the data-input signal must remain stable after the active edge of the clock (or other specified signal) to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large hold time) by more than 10%.

Hold-constraint values are measured as the interval between the data signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd. For the measurement of hold time, the data input signal is held stable before the active clock edge for an infinite setup time. Figure 4 illustrates hold time for a positive-edge-triggered sequential cell.

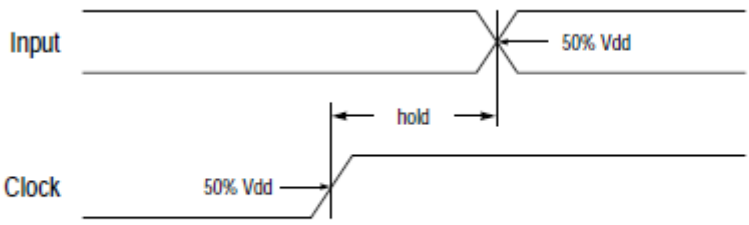


Figure 4. Hold Time

Recovery Time

Recovery time for sequential cells is the minimum length of time that the active low set or reset signal must remain high before the active edge of the clock to ensure correct functioning of the cell. The cell is considered functional as long as the delay for the output reaching its expected value does not exceed the reference delay (measured with a large recovery time) by more than 10%.

Recovery constraint values are measured as the interval between the set or reset signal crossing 50% of Vdd and the clock signal crossing 50% of Vdd. For the measurement of recovery time, the set or reset signal is held stable after the active clock edge for an infinite hold time.Figure 5 illustrates recovery time.

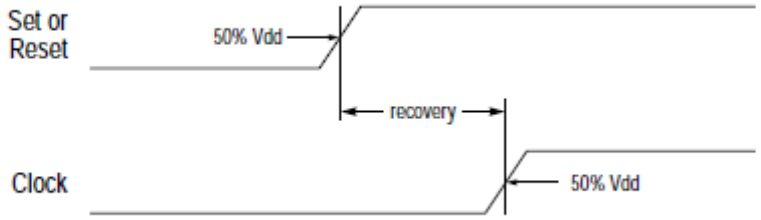


Figure 5. Recovery Time

Minimum Pulse Width

Minimum pulse width is the minimum length of time between the leading and trailing edges of a pulse waveform. Minimum pulse width high (minpwh) is measured as the interval between the rising edge of the signal crossing 50% of Vdd and the falling edge of the signal crossing 50% of Vdd. Minimum pulse width low (minpwl) is measured as the interval between the falling edge of the signal crossing 50% of Vdd and the rising edge of the signal crossing 50% of Vdd. Figure 6 illustrates minimum pulse width.

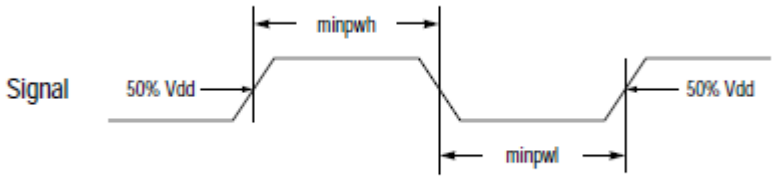


Figure 6. Minimum Pulse Width

The value in this datasheet is just for customer reference.

Cells

Buffers and Gates

Name Decoding Scheme: *aaaa*D*n*

aaaa = Name of the cell:

AN = AND Gate
AOI = AND-OR-Invert Gate
AOR = AND-OR Gate
BUFF = Non-Inverting Buffer
BUFT = Non-Inverting 3-State Buffer
DL = Non Inverting Delay Buffer
INV0 = Inverter
INVT = Inverting 3-State Buffer
ND = NAND Gate
NR = NOR Gate
OAI = OR-AND-Invert Gate
OR = OR Gate
ORA = OR-AND Gate
XN = Exclusive NOR Gate
XR = Exclusive OR Gate

n = Drive Strength

0 = Minimum drive
1 = Basic drive speed
2 = 2 times basic drive speed
4 = 4 times basic drive speed

Multiplexers

Name Decoding Scheme: *aabc*D*n*

aa = Name of the Cell:

MX = Multiplexer
MI = Inverting Multiplexer

b = Number of Inversions in the Input

c = Number of Inputs

n = Drive Strength

Flip-Flops

Name Decoding Scheme: *aabcdn*

aa = Name of the Cell
- DF = D Flip-Flop

b = Preset and Clear Notation
- B = Both Preset and Clear
- C = Clear
- P = Preset
- N = None

c = Clock Edge
- R = Positive Rising Edge
- F = Negative Falling Edge

d = Number of Output Pins:
- B = Both Q and QN
- Q = Q Only
- N = QN Only

n = Drive Strength

Scan Flip-Flops

Name Decoding Scheme: *aabcdn*

aa = Name of the Cell:
- SD = Multiplexed Scan D Flip-Flop

b = Preset and Clear Notation:
- B = Both Preset and Clear
- C = Clear
- P = Preset
- N = None

c = Enable:
- H = Active High Enable
- L = Active Low Enable

d = Number of Output Pins:
- B = Both Q and QN
- Q = Q Only
- N = QN Only

n = Drive Strength

Latches

Name Decoding Scheme: *aabcdn*

aa = Name of the Cell:
- LA = D Latch

b = Preset and Clear Notation:
- B = Both Preset and Clear
- C = Clear
- P = Preset
- N = None

c = Enable:
- H = Active High Enable
- L = Active Low Enable

d = Number of Output Pins:
- B = Both Q and QN
- Q = Q Only
- N = QN Only
- T = Z Only

n = Drive Strength

Adders/Subtractors

Name Decoding Scheme: *aabc*D*n*

aa = Name of the Cell
- AD = Adder
- AH = Half Adder

b = Number of Inversions in the Input

c = Number of Bits

n = Drive Strength

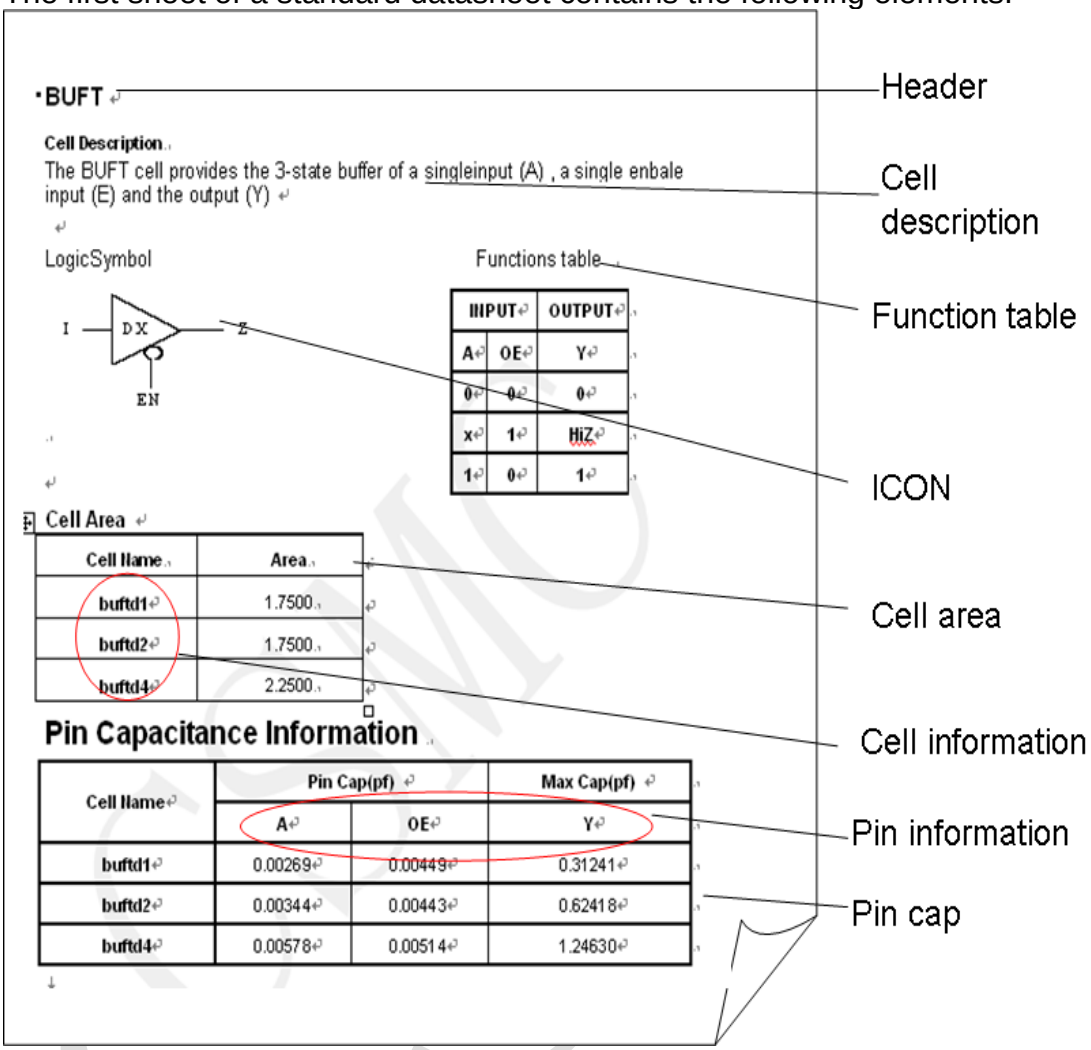
Decoding the Cell Name

This section describes the naming conventions for the cells in the CSMC0153 . Each cell name begins with either a two-, three-, or four-letter code that defines the type of cell. These codes are listed in the following table; the sections that follow give the detailed naming conventions for each cell type.

Code	Description
AD	Adder
AH	Half Adder
AN	AND Gate
AOI	AND-OR-Invert Gate
AOR	AND-OR Gate
BUFF	Non-Inverting Buffer
BUFT	Non-Inverting 3-State Buffer
DF	D Flip-Flop
INV0	Inverter
INVT	Inverting 3-State Buffer
LA	D Latch
MI	Inverting Multiplexer
MX	Multiplexer
ND	NAND Gate
NR	NOR Gate
OAI	OR-AND-Invert Gate
OR	OR Gate
ORA	OR-AND Gate
SD	Multiplexed Scan D Flip-Flop
XN	Exclusive NOR Gate
XR	Exclusive OR Gate

Reading the Datasheet

The first sheet of a standard datasheet contains the following elements:



Header and cell Description

The cell header in the large font describes the cell type, such as Clock Buffer with Positive Clock Input. Under the header is a list of the cells included in the category, in a smaller font. The text block following the headers gives a brief description of the cells included in this datasheet.

Icon

The icon pictured on the datasheet is the one you will see in the DC_vision Tools when you place a schematic element.

Function Table

The function table gives all the possible combinations of input and output signals for this cell type. The following symbols are used in the function tables on the datasheets

0	=	Low level	Q	=	Current Q
1	=	High level	Qn	=	Current QN, also complement of Q
	=	Low to High transition	Q0	=	Previous level of Q
	=	High to Low transition	QN0	=	Previous level of QN, also complement of Q0
X	=	Any level (Don't Care)	HiZ	=	High impedance state
U	=	Unknown	Zrl	=	3-state output with resistive pull down
Rh	=	Resistive High	Zrh	=	3-state output with resistive pullup
Rl	=	Resistive Low	Z	=	3-state output

Cell Information and Cell Area

This information is listed under the icon and function table for the cell; not all categories will be included for all cell types and libraries:

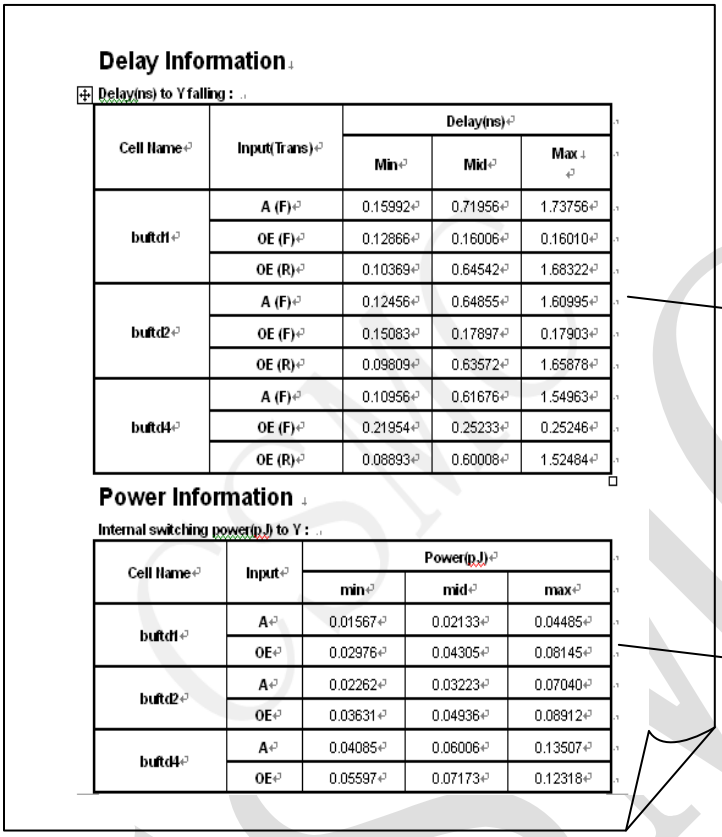
- Gate Equivalents - One gate is the equivalent in terms of area of one 2-input NAND. The Gate Equivalent is the ratio between the area of a cell and the one of the 2-input NAND gate. This is an indication of the area required by a cell.

Pin Iinformation and Pin capcacitance

The Pin Description table gives:

- The name of the pin.
- The total capacitance that a signal driving in to that pin will have to drive; this includes gate capacitance as well as interconnect capacitance within the cell.For outputs, the pin capacitance is not specified, only the maximum output load capacitance on that pin is given
- A description of the pin's usage.

The second page of a standard datasheet contains the following information:



Delay Information

Delay(ns) to Y falling :

Cell Name	Input(Trans)	Delay(ns)		
		Min	Mid	Max
buftd1	A (F)	0.15992	0.71956	1.73756
	OE (F)	0.12866	0.16006	0.16010
	OE (R)	0.10369	0.64542	1.68322
buftd2	A (F)	0.12456	0.64855	1.60995
	OE (F)	0.15083	0.17897	0.17903
	OE (R)	0.09809	0.63572	1.65878
buftd4	A (F)	0.10956	0.61676	1.54963
	OE (F)	0.21954	0.25233	0.25246
	OE (R)	0.08893	0.60008	1.52484

Power Information

Internal switching power(pJ) to Y :

Cell Name	Input	Power(pJ)		
		min	mid	max
buftd1	A	0.01567	0.02133	0.04485
	OE	0.02976	0.04305	0.08145
buftd2	A	0.02262	0.03223	0.07040
	OE	0.03631	0.04936	0.08912
buftd4	A	0.04085	0.06006	0.13507
	OE	0.05597	0.07173	0.12318

Propagation Delays for Sample Loads

The Propagation Cell Delays e Loads table are extrapolated from the characterized look-up table values using the max , middle , min load and skew input. The value can be used for reference.

Pin Power Table

The pin power table gives for each pin of the table a dissipated power from the Synopsys look-up table models.This power is given for a standard load and a standard input transition.The power data provided are the internal power for input pin when outputs doesn't switch, and the internal power for output pins.

The power data for output pins is defined as defined in the synopsys power models

$$\text{internal power} = \text{total switching power} - C*Vdd^2/2 - \text{input power}$$

In this equation, the input power is the internal power of the relative input that create the switching of the output.

Note that due to the fact that C includes both the output pin load and the external load, the output pin internal power may be negative for some cells; this is a modelisation effect.

The complete switching power when pin I makes the pin OUT switching is:

total switching power = internal power(OUT) + $C(OUT)*Vdd^2/2$ + input power(I)

The internal power has been modelised for all output. The input power of the cells
for which the input switching always create an output switching (i.e. buffer) is not modelised. Therefore only the internal power of output pin for this type of cells appears in the datasheet and includes the input power of the input pin.
In this case, the complete switching power when the input pin makes the output pin switching is:

total switching power = internal power + $C(OUT)*Vdd^2/2$

Note:

The RISE and FALL times represent the total delay time from the change of the input pin to the corresponding response on the output pin. Actual interconnect length and load cannot be determined until a design has completed placement and routing. When using these tables, you must estimate the interconnect load in units of standard loads and add that to the fanout. A rough rule of thumb is that, for every input load, there is a corresponding interconnect load approximately equal to it. For example, to estimate the delay of a NAND gate driving a fanout of two, use the column in the datasheet specifying four standard loads: two for fanout and two for the interconnect loading.

Arithmetic Gates

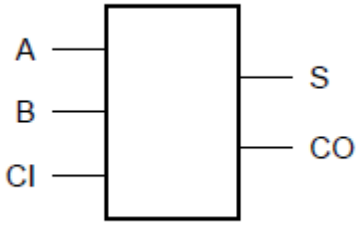
AD01

Cell Description

The AD01 cell provides the arithmetic sum (S) and carry out (CO) of two operands (A, B) with carry in (CI). The two outputs (S, CO) are represented by the logic equations:

$$S = (A \oplus B \oplus CI)$$
$$CO = (A \oplus B) \bullet CI + (A \bullet B)$$

Logic Symbol



Functions table

CI	A	B	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

ad01dN datasheet details refer to ../doc/DATASHEET/html/

AH01

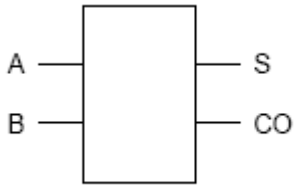
Cell Description

The AH01 cell provides the arithmetic sum (S) and carry out (CO) of two operands (A, B). The two outputs (S, CO) are represented by the logic equations:

$$S=(A•B)+(A•B)$$

$$CO = A • B$$

Logic Symbol



Functions

INPUT		OUTPUT	
A	B	CO	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

ah01dN datasheet details refer to ../doc/DATASHEET/html/

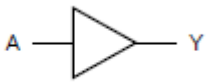
BUFF

Cell Description

The BUFF cell provides the logical buffer of a singleinput (A). The output (Y) is represented by the logicequation:

$$Y = A$$

LogicSymbol



Functions table

A	Y
0	0
1	1

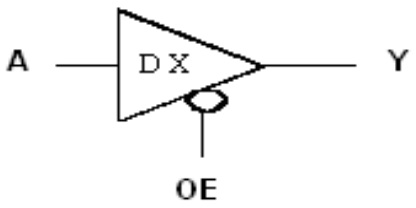
buffdN datasheet details refer to ../doc/DATASHEET/html/

BUFT

Cell Description

The BUFT cell provides the 3-state buffer of a single input (A) , a single low enable input (OE) and the output (Y)

LogicSymbol



Functions table

INPUT		OUTPUT
A	OE	Y
0	0	0
x	1	HiZ
1	0	1

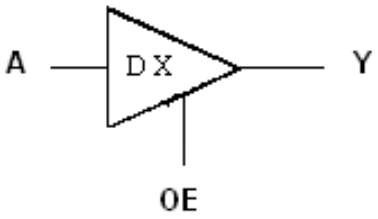
buftdN datasheet Details refer to doc/DATASHEET/html/

BUFTL

Cell Description

The BUFTL cell provides the 3-state buffer of a single input (A) , a single high enable input (OE) and the output (Y)

Logic Symbol



Functions table

INPUT		OUTPUT
A	OE	Y
x	0	HiZ
0	1	0
1	1	1

buftldN datasheet Details refer to doc/DATASHEET/html/

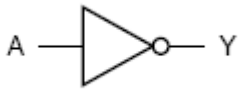
INV0

Cell Description

The INV0 cell provides the logical inversion of a single input (A). The output (Y) is represented by the logic equation:

$$Y = !A$$

Logic Symbol



Functions

INPUT	OUTPUT
A	Y
0	1
1	0

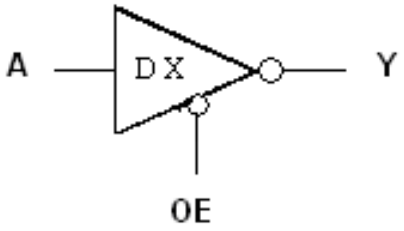
inv0dN datasheet Details refer to doc/DATASHEET/html/

INVT

Cell Description

The INVT cell provides the 3-state inverter of a singleinput (A) , a single low enable input (OE) and the output (Y)

LogicSymbol



Functions table

INPUT		OUTPUT
A	OE	Y
0	0	1
x	1	HiZ
1	0	0

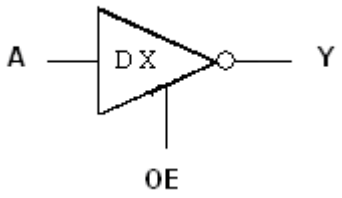
InvtdN datasheet Details refer to doc/DATASHEET/html/

INVTL

Cell Description

The INVTL cell provides the 3-state inverter of a singleinput (A) , a single high enable input (OE) and the output (Y)

LogicSymbol



Functions table

INPUT		OUTPUT
A	OE	Y
x	0	HiZ
0	1	1
1	1	0

invtldN datasheet Details refer to doc/DATASHEET/html/

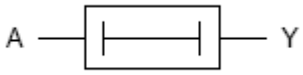
DL01

Cell Description

The DL01 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$$Y = A$$

Logic Symbol



Functions table

INPUT	OUTPUT
A	Y
0	0
1	1

dl01dN datasheet details refer to doc/DATASHEET/html/

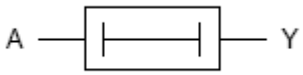
DL02

Cell Description

The DL02 cell provides the logical delay of a single input (A). The output (Y) is represented by the logic equation:

$$Y = A$$

Logic Symbol



Functions table

INPUT	OUTPUT
A	Y
0	0
1	1

dl02dN datasheet details refer to doc/DATASHEET/html/

COMPLEX Gates

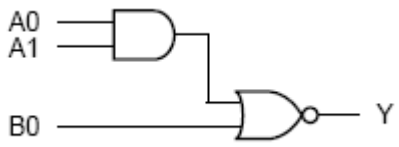
AOI21

Cell Description

The AOI21 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = !（(A0 \bullet A1) + B0）$$

Logic Symbol



Functions table

INPUT			OUTPUT
A0	A1	B0	Y
0	x	0	1
x	x	1	0
1	0	0	1
1	1	x	0

aoi21dN datasheet details refer to doc/DATASHEET/html/

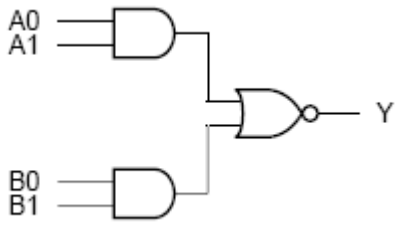
AOI22

Cell Description

The AOI22 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = ! ((A0 \bullet A1)+(B0 \bullet B1))$$

Logic Symbol



Functions table

INPUT				OUTPUT
A0	A1	B0	B1	Y
0	x	0	x	1
0	x	1	0	1
x	x	1	1	0
1	0	0	x	1
1	0	1	0	1
1	1	x	x	0

aoi22dN datasheet details refer to doc/DATASHEET/html/

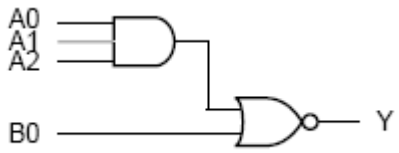
AOI31

Cell Description

The AOI31 cell provides the logical inverted OR of one AND group and an additional input. The output (Y) is represented by the logic equation:

$$Y = \ ! \ （ \ (A0 \bullet A1 \bullet A2) + B0 \ ）$$

Logic Symbol



Functions table

INPUT				OUTPUT
A0	A1	A2	B0	Y
0	x	x	0	1
x	x	x	1	0
1	0	x	0	1
1	1	0	0	1
1	1	1	x	0

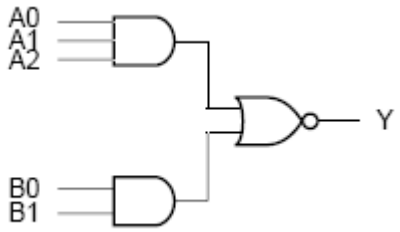
aoi31dN datasheet details refer to doc/DATASHEET/html/

AOI32

The AOI32 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = !\ (\ (A0 \bullet A1 \bullet A2)+(B0 \bullet B1)\ )$$

Logic Symbol



Functions table

INPUT					OUTPUT
A0	A1	A2	B0	B1	Y
0	x	x	0	x	1
0	x	x	1	0	1
x	x	x	1	1	0
1	0	x	0	x	1
1	0	x	1	0	1
1	1	0	0	x	1
1	1	0	1	0	1
1	1	1	x	x	0

aoi32dN datasheet details refer to doc/DATASHEET/html/

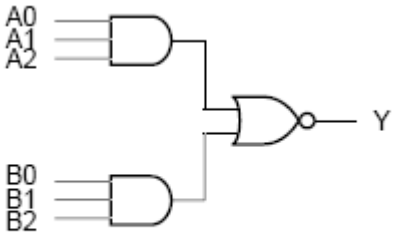
AOI33

Cell Description

The AOI33 cell provides the logical inverted OR of two AND groups. The output (Y) is represented by the logic equation:

$$Y = \ !\ (\ (\ A0 \bullet A1 \bullet A2) + (B0 \bullet B1 \bullet B2)\ )$$

Logic Symbol



Functions table

INPUT						OUTPUT
A0	A1	A2	B0	B1	B2	Y
0	x	x	0	x	x	1
0	x	x	1	0	x	1
0	x	x	1	1	0	1
x	x	x	1	1	1	0
1	0	x	0	x	x	1
1	0	x	1	0	x	1
1	0	x	1	1	0	1
1	1	0	0	x	x	1
1	1	0	1	0	x	1
1	1	0	1	1	0	1
1	1	1	x	x	x	0

aoi33dN datasheet details refer to doc/DATASHEET/html/

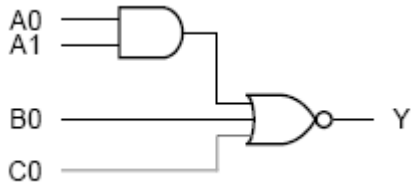
AOI211

Cell Description

The AOI211 cell provides the logical inverted OR of one AND groups and two addition inputs. The output (Y) is represented by the logic equation:

Y = (!(C0|B0|(A1&A0)))

Logic Symbol



Functions table

INPUT				OUTPUT
A0	A1	B0	C0	Y
0	x	0	0	1
0	x	x	1	0
x	x	1	x	0
1	0	0	0	1
1	0	x	1	0
1	1	x	x	0

aoi211dN datasheet details refer to doc/DATASHEET/html/

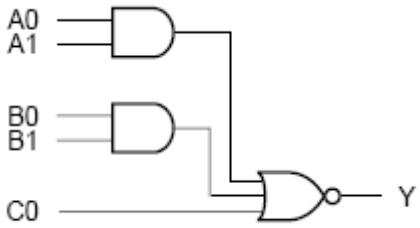
AOI221

Cell Description

The AOI221 cell provides the logical inverted OR of two AND groups and a third input. The output (Y) is represented by the logic equation:

$$Y = !((A0 \bullet A1)+(B0 \bullet B1)+C0)$$

Logic Symbol



Functions table

INPUT					OUTPUT
A0	A1	B0	B1	C0	Y
0	x	0	x	0	1
0	x	x	x	1	0
0	x	1	0	0	1
x	x	1	1	x	0
1	0	0	x	0	1
1	0	x	x	1	0
1	0	1	0	0	1
1	1	x	x	x	0

aoi221dN datasheet details refer to doc/DATASHEET/html/

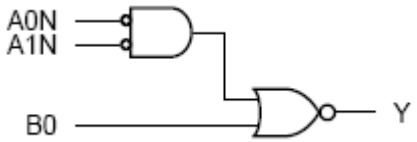
AOIM21

Cell Description

The AOIM21 cell provides the logical inverted OR of one AND group of two inverted inputs (A0N, A1N) and an additional non-inverted input (B0).The output (Y) is represented by the logic equation:

Y = ((!B0)&(A0N|A1N))

Logic Symbol



Functions table

INPUT			OUTPUT
A0N	A1N	B0	Y
0	0	x	0
x	1	0	1
x	1	1	0
1	x	0	1
1	x	1	0

aoim21dN datasheet details refer to doc/DATASHEET/html/

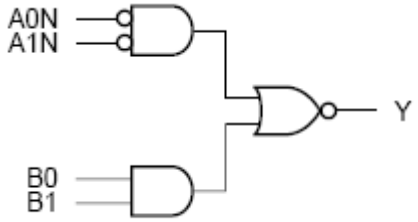
AOIM22

Cell Description

The AOIM22 cell provides the logical inverted OR of one AND group of two inverted inputs (A0N, A1N)and one AND group of two non-inverted inputs (B0,B1).The output (Y) is represented by the logic equation:

Y = (!(((!A1N)&(!A0N))|(B1&B0)))

Logic Symbol



Functions table

INPUT				OUTPUT
A0N	A1N	B0	B1	Y
0	0	x	x	0
x	1	0	x	1
x	1	1	0	1
x	1	1	1	0
1	x	0	x	1
1	x	1	0	1
1	x	1	1	0

aoim22dN datasheet details refer to doc/DATASHEET/html/

AOIM31

Cell Description

The AOIM31 cell provides the logical inverted OR of one AND group of three inverted inputs (A0N, A1N , A2N) and an additional non-inverted input (B0).The output (Y) is represented by the logic equation:

$$Y = ((!B0)\&(A1N|A0N|A2N))$$

Logic Symbol

Functions table

INPUT				OUTPUT
A0N	A1N	A2N	B0	Y
0	0	0	x	0
0	x	1	0	1
0	x	1	1	0
x	1	x	0	1
x	1	x	1	0
1	x	x	0	1
1	x	x	1	0

aoim31dN datasheet details refer to doc/DATASHEET/html/

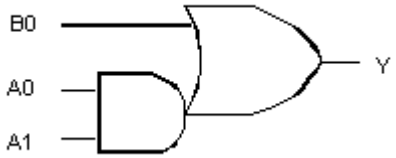
AOR21

Cell Description

The AOR21 cell provides the logical OR of one AND group of two inputs (A0, A1) and an additional inputs (B0).The output (Y) is represented by the logic equation:

Y =((A0&A1)|B0)

Logic Symbol



Functions table

INPUT			OUTPUT
A0	A1	B0	Y
0	x	0	0
x	x	1	1
1	0	0	0
1	1	x	1

aor21dN datasheet details refer to doc/DATASHEET/html/

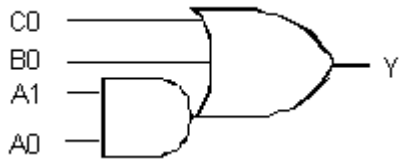
AOR211

Cell Description

The AOR211 cell provides the logical OR of one AND group of two inputs（A0,A1）and two addition inputs(B0 C0) .The output (Y) is represented by the logic equation:

Y = (B0|C0|(A1&A0))

Logic Symbol



Functions table

INPUT				OUTPUT
A0	A1	B0	C0	Y
0	x	0	0	0
0	x	x	1	1
x	x	1	x	1
1	0	0	0	0
1	0	x	1	1
1	1	x	x	1

aor211dN datasheet details refer to doc/DATASHEET/html/

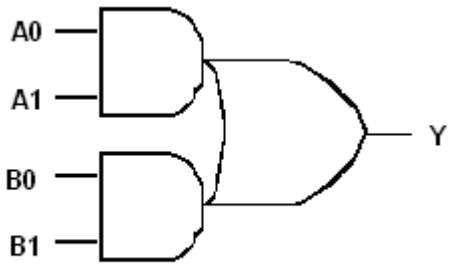
AOR22

Cell Description

The AOR22 cell provides the logical OR of two AND group of two inputs The output (Y) is represented by the logic equation:

Y= ((A1&A0)|(B1&B0))

Logic Symbol



Functions table

INPUT				OUTPUT
A0	A1	B0	B1	Y
0	x	0	x	0
0	x	1	0	0
x	x	1	1	1
1	0	0	x	0
1	0	1	0	0
1	1	x	x	1

aor22dN datasheet details refer to doc/DATASHEET/html/

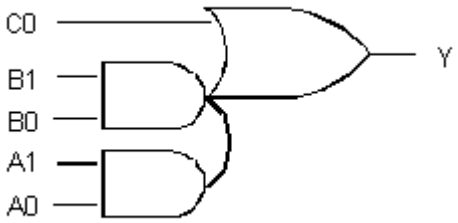
AOR221

Cell Description

The AOR221 cell provides the logical OR of two AND group of two inputs and an addition input .The output (Y) is represented by the logic equation:

Y = ((A0&A1)|(B1&B0)|C0)

Logic Symbol



Functions table

INPUT					OUTPUT
A0	A1	B0	B1	C0	Y
0	x	0	x	0	0
0	x	x	x	1	1
0	x	1	0	0	0
x	x	1	1	x	1
1	0	0	x	0	0
1	0	x	x	1	1
1	0	1	0	0	0
1	1	x	x	x	1

aor221dN datasheet details refer to doc/DATASHEET/html/

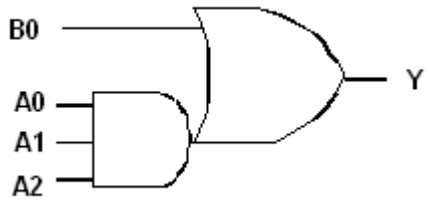
AOR31

Cell Description

The AOR31 cell provides the logical OR of one AND group of three inputs and an addition input .The output (Y) is represented by the logic equation:

Y = ((A1&A0&A2)|B0)

Logic Symbol



Functions table

INPUT				OUTPUT
A0	A1	A2	B0	Y
0	x	x	0	0
x	x	x	1	1
1	0	x	0	0
1	1	0	0	0
1	1	1	x	1

aor31dN datasheet details refer to doc/DATASHEET/html/

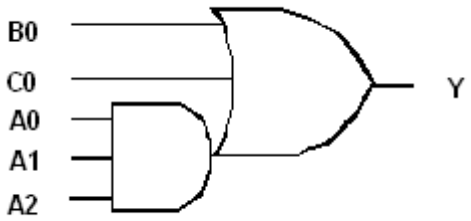
AOR311

Cell Description

The AOR311 cell provides the logical OR of one AND group of three inputs and two addition inputs .The output (Y) is represented by the logic equation:

Y = ((A0&A2&A1)|B0|C0)

Logic Symbol



Functions table

INPUT					OUTPUT
A0	A1	A2	B0	C0	Y
0	x	x	0	0	0
0	x	x	x	1	1
x	x	x	1	x	1
1	0	x	0	0	0
1	0	x	x	1	1
1	1	0	0	0	0
1	1	0	x	1	1
1	1	1	x	x	1

aor311dN datasheet details refer to doc/DATASHEET/html/

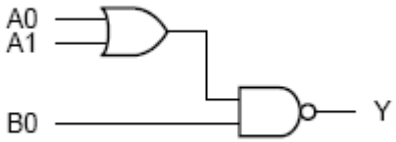
OAI21

Cell Description

The OAI21 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

Y = (!(B0&(A0|A1)))

Logic Symbol



Functions table

INPUT			OUTPUT
A0	A1	B0	Y
0	0	x	1
x	1	0	1
x	1	1	0
1	x	0	1
1	x	1	0

oai21dN datasheet details refer to doc/DATASHEET/html/

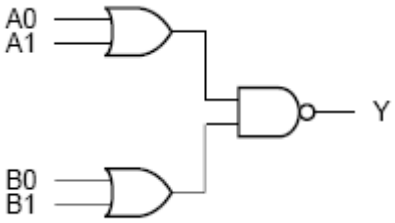
OAI22

Cell Description

The OAI22 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

Y = (!((B1|B0)&(A1|A0)))

Logic Symbol



Functions table

INPUT				OUTPUT
A0	A1	B0	B1	Y
0	0	x	x	1
x	1	0	0	1
x	1	x	1	0
x	1	1	x	0
1	x	0	0	1
1	x	x	1	0
1	x	1	x	0

oai22dN datasheet details refer to doc/DATASHEET/html/

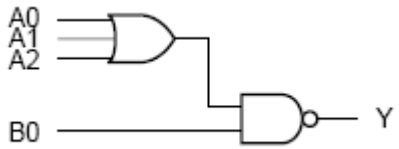
OAI31

Cell Description

The OAI31 cell provides the logical inverted AND of one OR group and an additional input. The output (Y) is represented by the logic equation:

Y = (!(B0&(A1|A0|A2)))

Logic Symbol



Functions table

INPUT				OUTPUT
A0	A1	A2	B0	Y
0	0	0	x	1
0	x	1	0	1
0	x	1	1	0
x	1	x	0	1
x	1	x	1	0
1	x	x	0	1
1	x	x	1	0

oai31dN datasheet details refer to doc/DATASHEET/html/

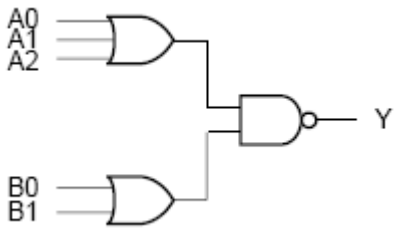
OAI32

Cell Description

The OAI32 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation:

Y = (!((B0|B1)&(A0|A2|A1)))

Logic Symbol



Functions table

INPUT					OUTPUT
A0	A1	A2	B0	B1	Y
0	0	0	x	x	1
0	x	1	0	0	1
0	x	1	x	1	0
0	x	1	1	x	0
x	1	x	0	0	1
x	1	x	x	1	0
x	1	x	1	x	0
1	x	x	0	0	1
1	x	x	x	1	0
1	x	x	1	x	0

oai32dN datasheet details refer to doc/DATASHEET/html/

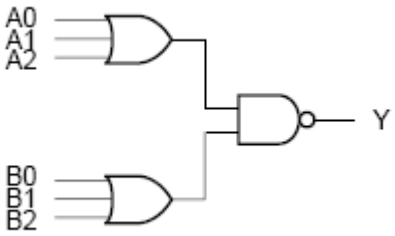
OAI33

Cell Description

The OAI33 cell provides the logical inverted AND of two OR groups. The output (Y) is represented by the logic equation

Y = (!((A2&A1&A0)|(B2&B1&B0)))

Logic Symbol



Functions table

INPUT						OUTPUT
A0	A1	A2	B0	B1	B2	Y
0	0	0	x	x	x	1
0	x	1	0	0	0	1
0	x	1	0	x	1	0
0	x	1	x	1	x	0
0	x	1	1	x	x	0
x	1	x	0	0	0	1
x	1	x	0	x	1	0
x	1	x	x	1	x	0
x	1	x	1	x	x	0
1	x	x	0	0	0	1
1	x	x	0	x	1	0
1	x	x	x	1	x	0
1	x	x	1	x	x	0

oai33dN datasheet details refer to doc/DATASHEET/html/

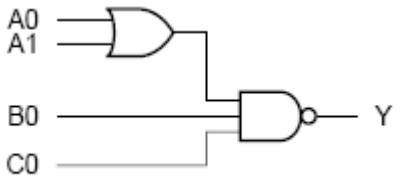
OAI211

Cell description

The OAI211 cell provides the logical inverted OR of one OR group and two additional inputs. The output (Y) is represented by the logic equation:

$$Y = (!(C0|B0|(A1\&A0)))$$

Logic Symbol



Functions table

INPUT				OUTPUT
A0	A1	B0	C0	Y
0	0	x	x	1
x	1	0	x	1
x	1	1	0	1
x	1	1	1	0
1	x	0	x	1
1	x	1	0	1
1	x	1	1	0

oai211dN datasheet details refer to doc/DATASHEET/html/

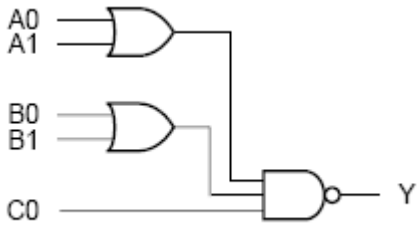
OAI221

Cell Description

The OAI221 cell provides the logical inverted AND of two OR groups and an additional input. The output (Y) is represented by the logic equation:

Y = (!(C0&(A1|A0)&(B0|B1)))

Logic Symbol



Functions table

INPUT					OUTPUT
A0	A1	B0	B1	C0	Y
0	0	x	x	x	1
x	1	0	0	x	1
x	1	x	1	0	1
x	1	x	1	1	0
x	1	1	x	0	1
x	1	1	x	1	0
1	x	0	0	x	1
1	x	x	1	0	1
1	x	x	1	1	0
1	x	1	x	0	1
1	x	1	x	1	0

oai221dN datasheet details refer to doc/DATASHEET/html/

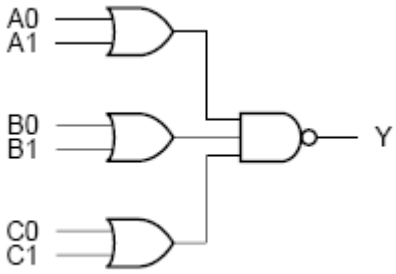
OAI222

Cell Description

The OAI222 cell provides the logical inverted AND of three OR groups. The output (Y) is represented by the logic equation:

Y = !((C1|C0)&(A1|A0)&(B1|B0))

Logic Symbol



Functions table

INPUT						OUTPUT
A0	A1	B0	B1	C0	C1	Y
0	0	x	x	x	x	1
x	1	0	0	x	x	1
x	1	x	1	0	0	1
x	1	x	1	x	1	0
x	1	x	1	1	x	0
x	1	1	x	0	0	1
x	1	1	x	x	1	0
x	1	1	x	1	x	0
1	x	0	0	x	x	1
1	x	x	1	0	0	1
1	x	x	1	x	1	0
1	x	x	1	1	x	0
1	x	1	x	0	0	1
1	x	1	x	x	1	0
1	x	1	x	1	x	0

oai222dN datasheet details refer to doc/DATASHEET/html/

OAI311

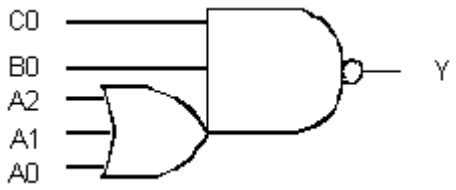
Cell Description

The OAI321 cell provides the logical inverted AND of one OR groups with two addition input.

The output (Y) is represented by the logic equation:

Y = (!(B0&C0&(A0|A2|A1)))

Logic Symbol



Functions table

INPUT					OUTPUT
A0	A1	A2	B0	C0	Y
0	0	0	x	x	1
0	x	1	0	x	1
0	x	1	1	0	1
0	x	1	1	1	0
x	1	x	0	x	1
x	1	x	1	0	1
x	1	x	1	1	0
1	x	x	0	x	1
1	x	x	1	0	1
1	x	x	1	1	0

oai311dN datasheet details refer to doc/DATASHEET/html/

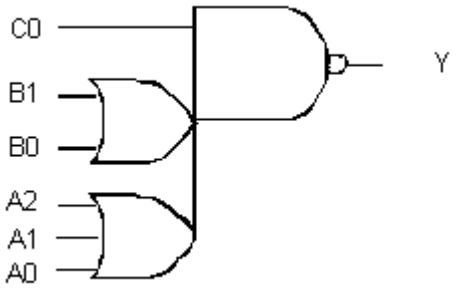
OAI321

Cell Description

The OAI321 cell provides the logical inverted AND of two OR groups with an addition input.
The output (Y) is represented by the logic equation:

Y = (!(C0&(A2|A1|A0)&(B0|B1)))

Logic Symbol



Functions table

INPUT						OUTPUT
A0	A1	A2	B0	B1	C0	Y
0	0	0	x	x	x	1
0	x	1	0	0	x	1
0	x	1	x	1	0	1
0	x	1	x	1	1	0
0	x	1	1	x	0	1
0	x	1	1	x	1	0
x	1	x	0	0	x	1
x	1	x	x	1	0	1
x	1	x	x	1	1	0
x	1	x	1	x	0	1
x	1	x	1	x	1	0
1	x	x	0	0	x	1
1	x	x	x	1	0	1
1	x	x	x	1	1	0
1	x	x	1	x	0	1
1	x	x	1	x	1	0

oai321dN datasheet details refer to doc/DATASHEET/html/

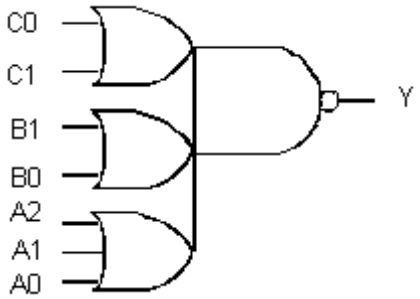
OAI322

Cell Description

The OAI322 cell provides the logical inverted AND of three OR groups. The output (Y) is represented by the logic equation:

Y = (!((B1|B0)&(C1|C0)&(A1|A0|A2)))

Logic Symbol



Functions table

INPUT							OUTPUT
A0	A1	A2	B0	B1	C0	C1	Y
0	0	0	x	x	x	x	1
0	x	1	0	0	x	x	1
0	x	1	x	1	0	0	1
0	x	1	x	1	x	1	0
0	x	1	x	1	1	x	0
0	x	1	1	x	0	0	1
0	x	1	1	x	x	1	0
0	x	1	1	x	1	x	0
x	1	x	0	0	x	x	1
x	1	x	x	1	0	0	1
x	1	x	x	1	x	1	0
x	1	x	x	1	1	x	0
x	1	x	1	x	0	0	1
x	1	x	1	x	x	1	0
x	1	x	1	x	1	x	0
1	x	x	0	0	x	x	1
1	x	x	x	1	0	0	1
1	x	x	x	1	x	1	0
1	x	x	x	1	1	x	0
1	x	x	1	x	0	0	1
1	x	x	1	x	x	1	0
1	x	x	1	x	1	x	0

oai322dN datasheet details refer to doc/DATASHEET/html/

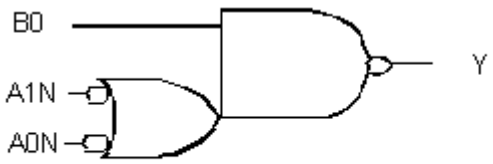
OAIM21

Cell Description

The OAIM21 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N, A1N) and an additional non-inverted input (B0).The output (Y) is represented by the logic equation:

$$Y = ((!B0)|(A0N\&A1N))$$

Logic Symbol



Functions table

INPUT			OUTPUT
A0N	A1N	B0	Y
x	x	0	1
0	x	1	0
1	0	1	0
1	1	1	1

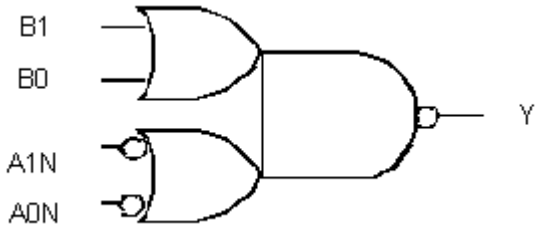
oaim21dN datasheet details refer to doc/DATASHEET/html/

OAIM22

Cell Description

The OAIM22 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N, A1N) and one OR group of two additional non-inverted input (B0 , B1).The output (Y) is represented by the logic equation:

Logic Symbol



Functions table

INPUT				OUTPUT
A0N	A1N	B0	B1	Y
x	x	0	0	1
0	x	x	1	0
0	x	1	x	0
1	0	x	1	0
1	0	1	x	0
1	1	x	1	1
1	1	1	x	1

oaim22dN datasheet details refer to doc/DATASHEET/html/

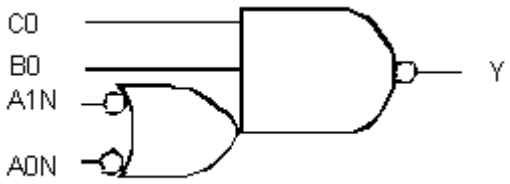
OAIM211

Cell Description

The OAIM211 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N, A1N) and two additional non-inverted input (B0, C0).The output (Y) is represented by the logic equation:

Y =(!(B0&C0&((!A1N)|(!A0N))))

Logic Symbol



Functions table

INPUT				OUTPUT
A0N	A1N	B0	C0	Y
x	x	0	x	1
x	x	1	0	1
0	x	1	1	0
1	0	1	1	0
1	1	1	1	1

oaim211dN datasheet details refer to doc/DATASHEET/html/

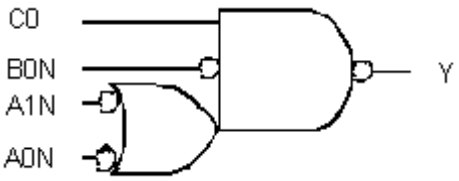
OAIM2M11

Cell Description

The OAIM2M11 cell provides the logical inverted AND of one OR group of two inverted inputs (A0N, A1N) and an inverter inputs(B0N) and an additional non-inverted input (C0).The output (Y) is represented by the logic equation:

$$Y = (B0N|(!C0)|(A1N\&A0N))$$

Logic Symbol



Functions table

INPUT				OUTPUT
A0N	A1N	B0N	C0	Y
0	x	x	0	1
0	x	0	1	0
x	x	1	1	1
1	0	x	0	1
1	0	0	1	0
1	1	x	x	1

oaim2m11dN datasheet details refer to doc/DATASHEET/html/

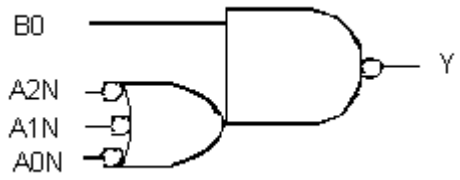
OAIM31

Cell Description

The AOIM31 cell provides the logical inverted AND of one OR group of three inverted inputs (A0N, A1N , A2N) and an additional non-inverted input (B0).The output (Y) is represented by the logic equation:

$$Y = ((!B0)\&(A1N|A0N|A2N))$$

Logic Symbol



Functions table

INPUT				OUTPUT
A0N	A1N	A2N	B0	Y
x	x	x	0	1
0	x	x	1	0
1	0	x	1	0
1	1	0	1	0
1	1	1	1	1

oaim31dN datasheet details refer to doc/DATASHEET/html/

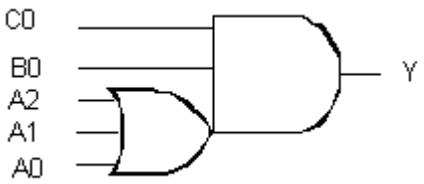
ORA211

Cell Description

The ORA211 cell provides the logical AND of one OR group of two inputs（A0,A1）and two addition inputs(B0 C0) .The output (Y) is represented by the logic equation

Y = (B0&C0&(A1|A0))

Logic Symbol



Functions table

INPUT				OUTPUT
A0	A1	B0	C0	Y
0	0	x	x	0
x	1	0	x	0
x	1	1	0	0
x	1	1	1	1
1	x	0	x	0
1	x	1	0	0
1	x	1	1	1

ora211dN datasheet details refer to doc/DATASHEET/html/

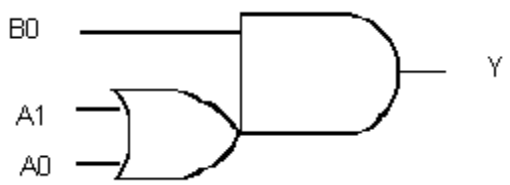
ORA21

Cell Description

The ORA21 cell provides the logical AND of one OR group of two inputs (A0, A1) and an additional inputs (B0).The output (Y) is represented by the logic equation:

Y = (B0&(A0|A1))

Logic Symbol



Functions table

INPUT			OUTPUT
A0	A1	B0	Y
0	0	x	0
x	1	0	0
x	1	1	1
1	x	0	0
1	x	1	1

ora21dN datasheet details refer to doc/DATASHEET/html/

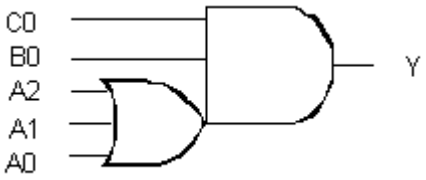
ORA311

Cell Description

The ORA311 cell provides the logical AND of one OR group of three inputs（A0,A1,A2）and two addition inputs(B0 C0) .The output (Y) is represented by the logic equation

Y = (B0&C0&(A1|A0|A2))

Logic Symbol



Functions table

INPUT					OUTPUT
A0	A1	A2	B0	C0	Y
0	0	0	x	x	0
0	x	1	0	x	0
0	x	1	1	0	0
0	x	1	1	1	1
x	1	x	0	x	0
x	1	x	1	0	0
x	1	x	1	1	1
1	x	x	0	x	0
1	x	x	1	0	0
1	x	x	1	1	1

ora311dN datasheet details refer to doc/DATASHEET/html/

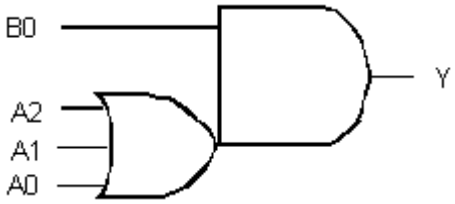
● ORA31

Cell Description

The ORA31 cell provides the logical AND of one OR group of three inputs（A0,A1,A2）and an addition inputs(B0) .The output (Y) is represented by the logic equation

Y = (B0&(A1|A0|A2))

Logic Symbol



Functions table

INPUT				OUTPUT
A0	A1	A2	B0	Y
0	0	0	x	0
0	x	1	0	0
0	x	1	1	1
x	1	x	0	0
x	1	x	1	1
1	x	x	0	0
1	x	x	1	1

ora31dN datasheet details refer to doc/DATASHEET/html/

Gates

AN02

Cell Description

The AND2 cell provides the logical AND of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = A \,\&\, B$$

Logic Symbol

Functions table

INPUT		OUTPUT
A	B	Y
0	x	0
1	0	0
1	1	1

an02dN datasheet details refer to doc/DATASHEET/html/

AN03

Cell Description

The AND3 cell provides the logical AND of three inputs (A, B, C). The output (Y) is represented by the logic equation:

Y =(C&B&A)

Logic Symbol

Functions table

INPUT			OUTPUT
A	B	C	Y
0	x	x	0
1	0	x	0
1	1	0	0
1	1	1	1

an03dN datasheet details refer to doc/DATASHEET/html/

AN04

Cell Description

The AND4 cell provides the logical AND of four inputs (A, B, C, D).The output (Y) is represented by the logic equation:

Y = (D&C&B&A)

Logic Symbol

Functions table

INPUT				OUTPUT
A	B	C	D	Y
0	x	x	x	0
1	0	x	x	0
1	1	0	x	0
1	1	1	0	0
1	1	1	1	1

an04dN datasheet details refer to doc/DATASHEET/html/

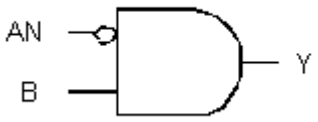
AN12

Cell Description

The AN12 cell provides the logical AND of one inverted input (AN) and one non-inverted input (B).The output (Y) is represented by the logic equation:

Y = (B&(!AN))

Logic Symbol



Functions table

INPUT		OUTPUT
AN	B	Y
x	0	0
0	1	1
1	1	0

an12dN datasheet details refer to doc/DATASHEET/html/

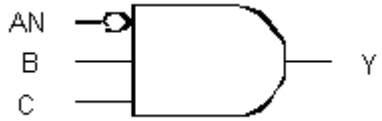
AN13

Cell Description

The AN13 cell provides the logical AND of one inverted input (AN) and two non-inverted inputs (B,C). The output (Y) is represented by the logic equation:

Y = (C&B&(!AN))

Logic Symbol



Functions table

INPUT			OUTPUT
AN	B	C	Y
x	0	x	0
x	1	0	0
0	1	1	1
1	1	1	0

an13dN datasheet details refer to doc/DATASHEET/html/

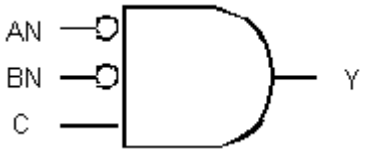
AN23

Cell Description

The AN23 cell provides the logical AND of two inverted input (AN,BN) and one non-inverted inputs (C). The output (Y) is represented by the logic equation:

Y = (C&(!BN)&(!AN))

Logic Symbol



Functions table

INPUT			OUTPUT
AN	BN	C	Y
0	x	0	0
0	0	1	1
x	1	1	0
1	x	x	0

an23dN datasheet details refer to doc/DATASHEET/html/

ND02

Cell Description

The NAND2 cell provides the logical NAND of two inputs (A, B). The output (Y) is represented by the logic equation:

Y = (!(B&A))

Logic Symbol

Functions table

INPUT		OUTPUT
A	B	Y
0	x	1
1	0	1
1	1	0

nd02dN datasheet details refer to doc/DATASHEET/html/

ND03

Cell Description

The NAND3 cell provides the logical NAND of three inputs (A, B, C). The output (Y) is represented by the logic equation:

Y = (!(C&B&A))

Logic Symbol

Functions table

INPUT			OUTPUT
A	B	C	Y
0	x	x	1
1	0	x	1
1	1	0	1
1	1	1	0

nd03dN datasheet details refer to doc/DATASHEET/html/

ND04

Cell Description

The NAND4 cell provides a logical NAND of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

Y = (!(D&C&B&A))

Logic Symbol

Functions table

INPUT				OUTPUT
A	B	C	D	Y
0	x	x	x	1
1	0	x	x	1
1	1	0	x	1
1	1	1	0	1
1	1	1	1	0

nd04dN datasheet details refer to doc/DATASHEET/html/

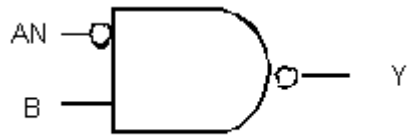
ND12

Cell Description

The ND12 cell provides the logical NAND of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

Y = ((!B)|AN)

Logic Symbol



Functions table

INPUT		OUTPUT
AN	B	Y
x	0	1
0	1	0
1	1	1

nd12dN datasheet details refer to doc/DATASHEET/html/

ND13

Cell Description

The ND13 cell provides the logical NAND of one inverted input (AN) and two non-inverted inputs (B,C). The output (Y) is represented by the logic equation:

Y = ((!C)|(!B)|AN)

Logic Symbol

Functions table

INPUT			OUTPUT
AN	B	C	Y
x	0	x	1
x	1	0	1
0	1	1	0
1	1	1	1

nd13dN datasheet details refer to doc/DATASHEET/html/

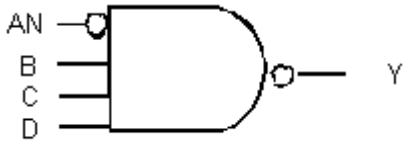
ND14

Cell Description

The ND14 cell provides a logical NAND of one inverted input (AN) and three non-inverted inputs (B,C, D). The output (Y) is represented by the logic equation:

Y =((!D)|(!C)|(!B)|AN)

Logic Symbol



Functions table

INPUT				OUTPUT
AN	B	C	D	Y
x	0	x	x	1
x	1	0	x	1
x	1	1	0	1
0	1	1	1	0
1	1	1	1	1

nd14dN datasheet details refer to doc/DATASHEET/html/

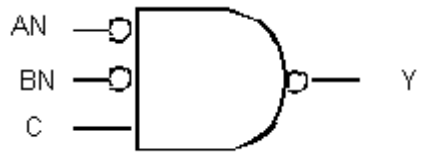
ND23

Cell Description

The ND23 cell provides a logical NAND of two inverted input (AN , BN) and one non-inverted inputs (C). The output (Y) is represented by the logic equation:

Y = ((!C)|BN|AN)

Logic Symbol



Functions table

INPUT			OUTPUT
AN	BN	C	Y
0	x	0	1
0	0	1	0
x	1	1	1
1	x	x	1

nd23dN datasheet details refer to doc/DATASHEET/html/

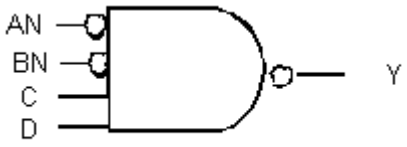
ND24

Cell Description

The ND24 cell provides a logical NAND of two inverted input (AN , BN) and two non-inverted inputs (C, D). The output (Y) is represented by the logic equation:

Y = ((!D)|(!C)|BN|AN)

Logic Symbol



Functions table

INPUT				OUTPUT
AN	BN	C	D	Y
0	x	0	x	1
0	x	1	0	1
0	0	1	1	0
x	1	1	1	1
1	x	x	x	1

nd24dN datasheet details refer to doc/DATASHEET/html/

NR02

Cell Description

The NR02 cell provides a logical NOR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (!(B|A))$$

Logic Symbol

Functions table

INPUT		OUTPUT
A	B	Y
0	0	1
x	1	0
1	x	0

nr02dN datasheet details refer to doc/DATASHEET/html/

NR03

Cell Description

The NR03 cell provides a logical NOR of three inputs (A, B, C). The output (Y) is represented by the logic equation:

Y = (!(C|B|A))

Logic Symbol

Functions table

INPUT			OUTPUT
A	B	C	Y
0	0	0	1
0	x	1	0
x	1	x	0
1	x	x	0

nr03dN datasheet details refer to doc/DATASHEET/html/

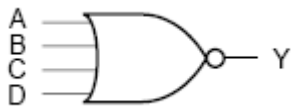
NR04

Cell Description

The NR04 cell provides a logical NOR of four inputs (A, B, C, D). The output (Y) is represented by the logic equation:

$$Y = (!(D|C|B|A))$$

Logic Symbol



Functions table

INPUT				OUTPUT
A	B	C	D	Y
0	0	0	0	1
0	0	x	1	0
0	x	1	x	0
x	1	x	x	0
1	x	x	x	0

nr04dN datasheet details refer to doc/DATASHEET/html/

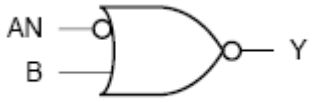
NR12

Cell Description

The NR12 cell provides a logical NOR of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

Y = ((!B)&AN)

Logic Symbol



Functions table

INPUT		OUTPUT
AN	B	Y
0	x	0
1	0	1
1	1	0

nr12dN datasheet details refer to doc/DATASHEET/html/

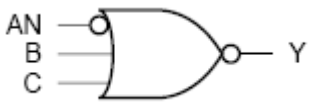
NR13

Cell Description

The NR13 cell provides a logical NOR of one inverted input (AN) and two non-inverted inputs (B, C). The output (Y) is represented by the logic equation:

Y = ((!C)&(!B)&AN)

Logic Symbol



Functions table

INPUT			OUTPUT
AN	B	C	Y
0	x	x	0
1	0	0	1
1	x	1	0
1	1	x	0

nr13dN datasheet details refer to doc/DATASHEET/html/

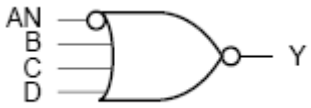
NR14

Cell Description

The NR14 cell provides a logical NOR of one inverted input (AN) and three non-inverted inputs (B, C, D). The output (Y) is represented by the logic equation:

Y = ((!D)&(!C)&(!B)&AN)

Logic Symbol



Functions table

INPUT				OUTPUT
AN	B	C	D	Y
0	x	x	x	0
1	0	0	0	1
1	0	x	1	0
1	x	1	x	0
1	1	x	x	0

nr14dN datasheet details refer to doc/DATASHEET/html/

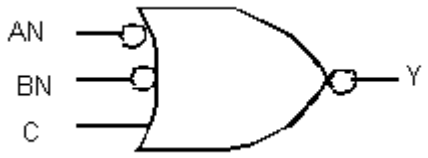
NR23

Cell Description

The NR23 cell provides a logical NOR of two inverted input (AN, BN) and one non-inverted input (C). The output (Y) is represented by the logic equation:

Y = ((!C)&BN&AN)

Logic Symbol



Functions table

INPUT			OUTPUT
AN	BN	C	Y
0	x	x	0
1	0	x	0
1	1	0	1
1	1	1	0

nr23dN datasheet details refer to doc/DATASHEET/html/

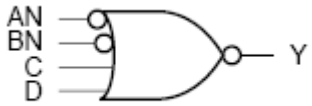
NR24

Cell Description

The NR24 cell provides a logical NOR of two inverted inputs (AN,BN)and two non-inverted inputs (C, D). The output (Y) is represented by the logic equation:

Y = ((!D)&(!C)&BN&AN)

Logic Symbol



Functions table

INPUT				OUTPUT
AN	BN	C	D	Y
0	x	x	x	0
1	0	x	x	0
1	1	0	0	1
1	1	x	1	0
1	1	1	x	0

nr24dN datasheet details refer to doc/DATASHEET/html/

OR02

Cell Description

The OR2 cell provides the logical OR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (B|A)$$

Logic Symbol

Functions table

INPUT		OUTPUT
A	B	Y
0	0	0
x	1	1
1	x	1

or02dN datasheet details refer to doc/DATASHEET/html/

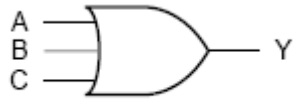
OR03

Cell Description

The OR3 cell provides the logical OR of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = (C|B|A)$$

Logic Symbol



Functions table

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	x	1	1
x	1	x	1
1	x	x	1

or03dN datasheet details refer to doc/DATASHEET/html/

OR04

Cell Description

The OR4 cell provides the logical OR of four inputs (A, B, C, D).The output (Y) is represented by the logic equation:

$$Y = (D|C|B|A)$$

Logic Symbol

Functions table

INPUT				OUTPUT
A	B	C	D	Y
0	0	0	0	0
0	0	x	1	1
0	x	1	x	1
x	1	x	x	1
1	x	x	x	1

or04dN datasheet details refer to doc/DATASHEET/html/

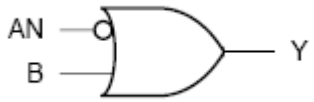
OR12

Cell Description

The NR12 cell provides a logical OR of one inverted input (AN) and one non-inverted input (B). The output (Y) is represented by the logic equation:

$$Y = (B|(!AN))$$

Logic Symbol



Functions table

INPUT		OUTPUT
AN	B	Y
0	x	1
1	0	0
1	1	1

or12dN datasheet details refer to doc/DATASHEET/html/

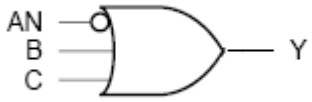
OR13

Cell Description

The OR13 cell provides a logical OR of one inverted input (AN) and two non-inverted inputs (B, C). The output (Y) is represented by the logic equation:

$$Y = (C|B|(!AN))$$

Logic Symbol



Functions table

INPUT			OUTPUT
AN	B	C	Y
0	x	x	1
1	0	0	0
1	x	1	1
1	1	x	1

or13dN datasheet details refer to doc/DATASHEET/html/

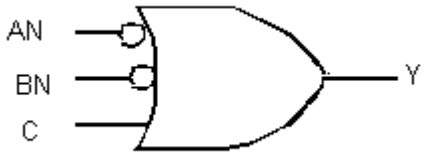
OR23

Cell Description

The OR23 cell provides a logical OR of two inverted input (AN, BN) and one non-inverted input (C). The output (Y) is represented by the logic equation:

Y = (C|(!BN)|(!AN))

Logic Symbol



Functions table

INPUT			OUTPUT
AN	BN	C	Y
0	x	x	1
1	0	x	1
1	1	0	0
1	1	1	1

or23dN datasheet details refer to doc/DATASHEET/html/

XN02

Cell Description

The XN02 cell provides a logical EXCLUSIVE NOR of two inputs (A, B). The output (Y) is represented by the logic equation:

Y = (!(B^A))

Logic Symbol

Functions table

INPUT		OUTPUT
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

xn02dN datasheet details refer to doc/DATASHEET/html/

XN03

Cell Description

The XN03 cell provides a logical EXCLUSIVE NOR of three inputs (A, B, C). The output (Y) is represented by the logic equation:

Y = (!(C^B^A))

Logic Symbol

Functions table

INPUT			OUTPUT
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

xn03dN datasheet details refer to doc/DATASHEET/html/

XR02

Cell Description

The XR02 cell provides a logical EXCLUSIVE OR of two inputs (A, B). The output (Y) is represented by the logic equation:

$$Y = (B \hat{} A)$$

Logic Symbol

Functions table

INPUT		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

xr02dN datasheet details refer to doc/DATASHEET/html/

XR03

Cell Description

The XR03 cell provides a logical EXCLUSIVE OR of three inputs (A, B, C). The output (Y) is represented by the logic equation:

$$Y = (C \hat{} B \hat{} A)$$

Logic Symbol

Functions table

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

xr03dN datasheet details refer to doc/DATASHEET/html/

MULTIPLEXERS

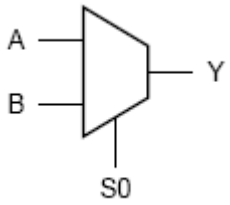
MX02

Cell Description

The MX02 cell is a 2-to-1 multiplexer. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y).The output (Y) is represented by the logic equation:

Y = ((A&(!S0))|(B&S0))

Logic Symbol



Functions table

INPUT			OUTPUT
A	B	S0	Y
0	0	x	0
0	1	0	0
x	1	1	1
1	x	0	1
1	0	1	0

mx02dN datasheet details refer to doc/DATASHEET/html/

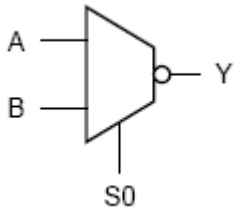
MI02

Cell Description

The MI02 cell is a 2-to-1 multiplexer with inverted output. The state of the select input (S0) determines which data input (A, B) is presented to the output (Y). The output (Y) is represented by the logic equation:

Y =(!((A&(!S0))|(B&S0)))

Logic Symbol



Functions table

INPUT			OUTPUT
A	B	S0	Y
0	0	x	1
0	1	0	1
x	1	1	0
1	x	0	0
1	0	1	1

mi02dN datasheet details refer to doc/DATASHEET/html/

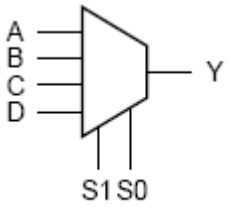
MX04

Cell Description

The MX04 cell is a 4-to-1 multiplexer. The state of the select inputs (S1, S0) determines which data input (A, B, C, D) is presented to the output (Y). The output (Y) is represented by the logic equation:

$$Y = ((A\&(!S1)\&(!S0))|(B\&(!S1)\&S0)|(D\&S1\&S0)|(C\&S1\&(!S0)))$$

Logic Symbol



Functions table

INPUT						OUTPUT
A	B	C	D	S0	S1	Y
0	0	0	0	x	x	0
0	x	0	1	0	x	0
x	0	x	1	1	0	0
x	x	x	1	1	1	1
0	0	1	x	x	0	0
0	x	1	x	0	1	1
0	x	1	0	1	1	0
0	1	0	x	0	x	0
0	1	x	x	1	0	1
0	1	x	0	1	1	0
0	1	1	x	0	0	0
1	0	0	x	0	0	1
1	x	0	0	x	1	0
1	0	x	0	1	x	0
1	x	0	1	0	1	0
1	x	1	x	0	x	1
1	1	0	x	x	0	1
1	1	1	x	1	0	1
1	1	1	0	1	1	0

mx04dN datasheet details refer to doc/DATASHEET/html/

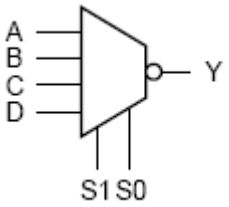
MI04

Cell Description

The MI04 cell is a 4-to-1 multiplexer with inverted output. The state of the select inputs (S1, S0) determines which data input (A, B, C, D) is presented to the output (Y). The output (Y) is represented by the logic equation:

Y = (!((A&(!S1)&(!S0))|(B&(!S1)&S0)|(D&S1&S0)|(C&S1&(!S0))))

Logic Symbol



mi04dN datasheet details refer to doc/DATASHEET/html/

Functions table

INPUT						OUTPUT
A	B	C	D	S0	S1	Y
0	0	0	0	x	x	1
0	x	0	1	0	x	1
x	0	x	1	1	0	1
x	x	x	1	1	1	0
0	0	1	x	x	0	1
0	x	1	x	0	1	0
0	x	1	0	1	1	1
0	1	0	x	0	x	1
0	1	x	x	1	0	0
0	1	x	0	1	1	1
0	1	1	x	0	0	1
1	0	0	x	0	0	0
1	x	0	0	x	1	1
1	0	x	0	1	x	1
1	x	0	1	0	1	1
1	x	1	x	0	x	0
1	1	0	x	x	0	0
1	1	1	x	1	0	0
1	1	1	0	1	1	1

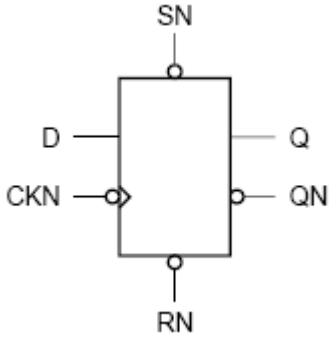
FLIP-FLOPS

DFBFB

Cell Description

The DFBFB cell is a negative-edge triggered, asynchronous active-low reset (RN) and set (SN), static D-type flip-flop.

Logic Symbol



Functions table

INPUT				OUTPUT	
D	RN	SN	CKN	Q	QN
0	1	1	F	0	1
1	1	1	F	1	0
x	x	0	x	1	0
x	0	1	x	0	1
x	1	1	x	IQ	IQN

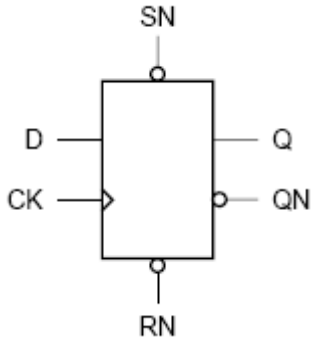
dfbfbN datasheet details refer to doc/DATASHEET/html/

DFBRB

Cell Description

The DFBRB cell is a positive-edge triggered, asynchronous active-low reset (RN) and set (SN), static D-type flip-flop.

Logic Symbol



Functions table

INPUT				OUTPUT	
D	RN	SN	CK	Q	QN
0	1	1	R	0	1
1	1	1	R	1	0
x	x	0	x	1	0
x	0	1	x	0	1
x	1	1	x	IQ	IQN

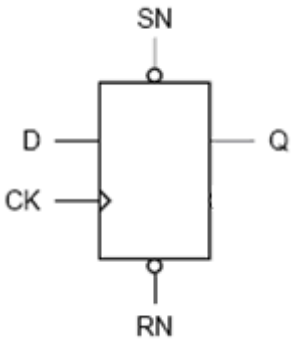
dfbrbN datasheet details refer to doc/DATASHEET/html/

DFBRQ

Cell Description

The DFBRQ cell is a positive-edge triggered, asynchronous active-low reset (RN) and set (SN), static D-type flip-flop.

Logic Symbol



Functions table

INPUT				OUTPUT
D	RN	SN	CK	Q
0	1	1	R	0
1	1	1	R	1
x	x	0	x	1
x	0	1	x	0
x	1	1	x	IQ

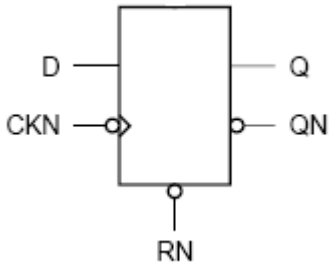
dfbrqN datasheet details refer to doc/DATASHEET/html/

DFCFB

Cell Description

The DFCFB cell is a negative-edge triggered, asynchronous active-low reset (RN) and static D-type flip-flop.

Logic Symbol



Functions table

INPUT			OUTPUT	
D	RN	CKN	Q	QN
0	1	F	0	1
1	1	F	1	0
x	0	x	0	1
x	1	x	IQ	IQN

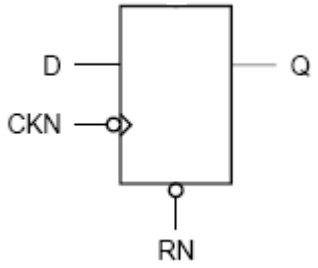
dfcfbN datasheet details refer to doc/DATASHEET/html/

DFCFQ

Cell Description

The DFCFQ cell is a negative-edge triggered, asynchronous active-low reset (RN) with a single output Q, static D-type flip-flop.

Logic Symbol



Functions table

INPUT			OUTPUT
D	RN	CKN	Q
0	1	F	0
1	1	F	1
x	0	x	0
x	1	x	IQ

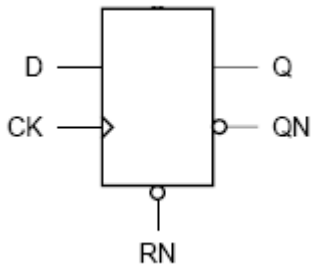
dfcfqN datasheet details refer to doc/DATASHEET/html/

DFCRB

Cell Description

The DFCRB cell is a positive-edge triggered, asynchronous active-low reset (RN), static D-type flip-flop.

Logic Symbol



Functions table

INPUT			OUTPUT	
D	RN	CK	Q	QN
0	1	R	0	1
1	1	R	1	0
x	0	x	0	1
x	1	x	IQ	IQN

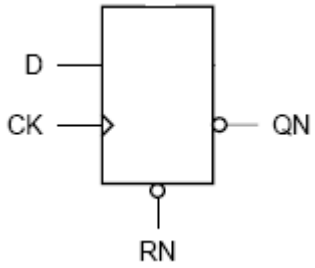
dfcrbN datasheet details refer to doc/DATASHEET/html/

DFCRN

Cell Description

The DFCRN cell is a positive-edge triggered, asynchronous active-low reset (RN) with a single output QN, static D-type flip-flop.

Logic Symbol



Functions table

INPUT			OUTPUT
D	RN	CK	QN
0	1	R	1
1	1	R	0
x	0	x	1
x	1	x	IQN

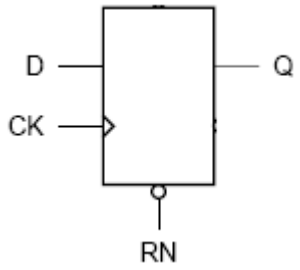
dfcrnN datasheet details refer to doc/DATASHEET/html/

DFCRQ

Cell Description

The DFCRQ cell is a positive-edge triggered, asynchronous active-low reset (RN) with a single output Q, static D-type flip-flop.

Logic Symbol



Functions table

INPUT			OUTPUT
D	RN	CK	Q
0	1	R	0
1	1	R	1
x	0	x	0
x	1	x	IQ

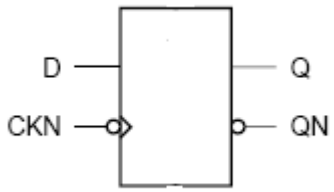
dfcrqN datasheet details refer to doc/DATASHEET/html/

DFNFB

Cell Description

The DFNFB cell is a negative-edge triggered, static D-type flip-flop.

Logic Symbol



Functions table

INPUT		OUTPUT	
D	CKN	Q	QN
0	F	0	1
1	F	1	0
x	x	IQ	IQN

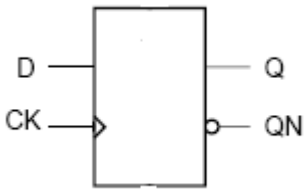
dfnfbN datasheet details refer to doc/DATASHEET/html/

DFNRB

Cell Description

The DFNRB cell is a positive-edge triggered, static D-type flip-flop.

Logic Symbol



Functions table

INPUT		OUTPUT	
D	CK	Q	QN
0	R	0	1
1	R	1	0
x	x	IQ	IQN

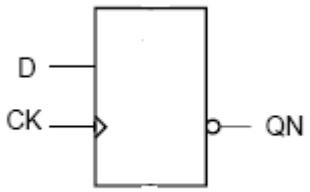
dfnrbN datasheet details refer to doc/DATASHEET/html/

DFNRN

Cell Description

The DFNRN cell is a positive-edge triggered, with a single output QN, static D-type flip-flop.

Logic Symbol



Functions table

INPUT		OUTPUT
D	CK	QN
0	R	1
1	R	0
x	x	IQN

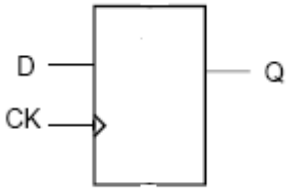
dfnrnN datasheet details refer to doc/DATASHEET/html/

DFNRQ

Cell Description

The DFNRQ cell is a positive-edge triggered, with a single output Q, static D-type flip-flop.

Logic Symbol



Functions table

INPUT		OUTPUT
D	CK	Q
0	R	0
1	R	1
x	x	IQ

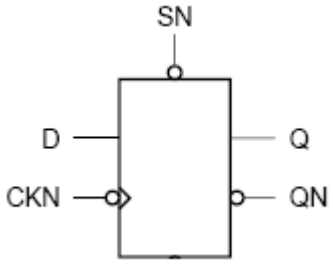
dfnrqN datasheet details refer to doc/DATASHEET/html/

DFPFB

Cell Description

The DFPFB cell is a negative-edge triggered, asynchronous active-low set (SN), static D-type flip-flop.

Logic Symbol



Functions table

INPUT			OUTPUT	
D	SN	CKN	Q	QN
0	1	F	0	1
1	1	F	1	0
x	0	x	1	0
x	1	x	IQ	IQN

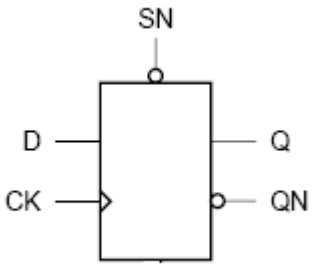
dfpfbN datasheet details refer to doc/DATASHEET/html/

DFPRB

Cell Description

The DFPRB cell is a positive-edge triggered, asynchronous active-low set (SN) static D-type flip-flop.

Logic Symbol



Functions table

INPUT			OUTPUT	
D	SN	CK	Q	QN
0	1	R	0	1
1	1	R	1	0
x	0	x	1	0
x	1	x	IQ	IQN

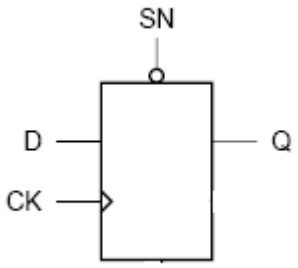
dfprbN datasheet details refer to doc/DATASHEET/html/

DFPRQ

Cell Description

The DFPRQ cell is a positive-edge triggered, asynchronous active-low set (SN) with a single output Q, static D-type flip-flop.

Logic Symbol



Functions table

INPUT			OUTPUT
D	SN	CK	Q
0	1	R	0
1	1	R	1
x	0	x	1
x	1	x	IQ

dfprqN datasheet details refer to doc/DATASHEET/html/

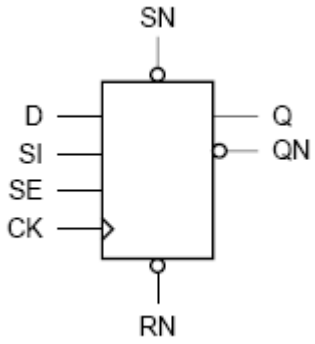
SCAN FLIP - FLOPS

SDBRB

Cell Description

The SDBRB cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN). Set (SN) dominates reset (RN).

Logic Symbol



Functions table

INPUT						OUTPUT	
D	SE	SI	RN	SN	CK	Q	QN
0	0	x	1	1	R	0	1
x	1	0	1	1	R	0	1
x	1	1	1	1	R	1	0
1	0	x	1	1	R	1	0
x	x	x	x	0	x	1	0
x	x	x	0	1	x	0	1
x	x	x	1	1	x	IQ	IQN

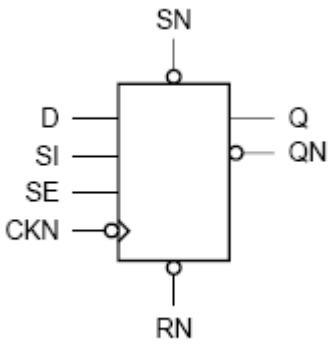
sdbrbN datasheet details refer to doc/DATASHEET/html/

SDBFB

Cell Description

The SDBFB cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN). Set (SN) dominates reset (RN).

Logic Symbol



Functions table

INPUT						OUTPUT	
D	SE	SI	RN	SN	CKN	Q	QN
0	0	x	1	1	F	0	1
x	1	0	1	1	F	0	1
x	1	1	1	1	F	1	0
1	0	x	1	1	F	1	0
x	x	x	x	0	x	1	0
x	x	x	0	1	x	0	1
x	x	x	1	1	x	IQ	IQN

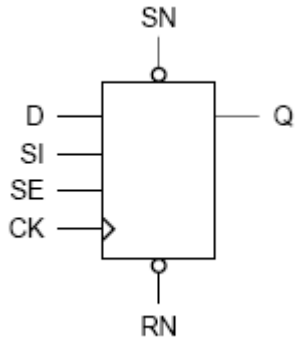
sdbfbN datasheet details refer to doc/DATASHEET/html/

SDBRQ

Cell Description

The SDBRQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) and set (SN), and set dominating reset. The cell has a single output (Q)

Logic Symbol



Functions table

INPUT						OUTPUT
D	SE	SI	RN	SN	CK	Q
0	0	x	1	1	R	0
x	1	0	1	1	R	0
x	1	1	1	1	R	1
1	0	x	1	1	R	1
x	x	x	x	0	x	1
x	x	x	0	1	x	0
x	x	x	1	1	x	IQ

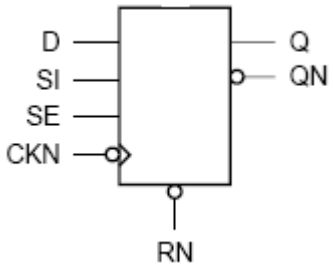
sdbrqN datasheet details refer to doc/DATASHEET/html/

SDCFB

Cell Description

The SDCFB cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN)

Logic Symbol



Functions table

INPUT					OUTPUT	
D	SE	SI	RN	CKN	Q	QN
0	0	x	1	F	0	1
x	1	0	1	F	0	1
x	1	1	1	F	1	0
1	0	x	1	F	1	0
x	x	x	0	x	0	1
x	x	x	1	x	IQ	IQN

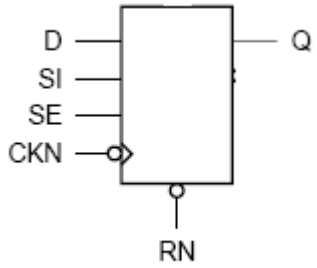
sdcfbN datasheet details refer to doc/DATASHEET/html/

SDCFQ

Cell Description

The SDCFQ cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) a single output (Q)

Logic Symbol



Functions table

INPUT					OUTPUT
D	SE	SI	RN	CKN	Q
0	0	x	1	F	0
x	1	0	1	F	0
x	1	1	1	F	1
1	0	x	1	F	1
x	x	x	0	x	0
x	x	x	1	x	IQ

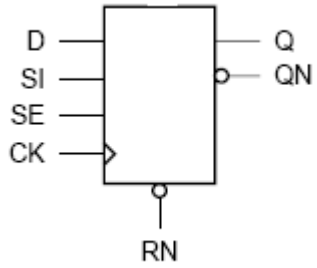
sdcfqN datasheet details refer to doc/DATASHEET/html/

SDCRB

Cell Description

The SDCRB cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN)

Logic Symbol



Functions table

INPUT					OUTPUT	
D	SE	SI	RN	CK	Q	QN
0	0	x	1	R	0	1
x	1	0	1	R	0	1
x	1	1	1	R	1	0
1	0	x	1	R	1	0
x	x	x	0	x	0	1
x	x	x	1	x	IQ	IQN

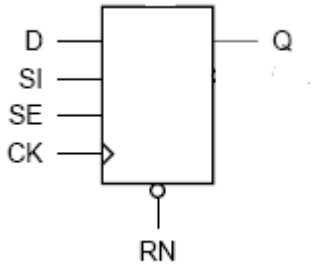
sdcrbN datasheet details refer to doc/DATASHEET/html/

SDCRQ

Cell Description

The SDCRQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) a single output (Q)

Logic Symbol



Functions table

INPUT					OUTPUT
D	SE	SI	RN	CK	Q
0	0	x	1	R	0
x	1	0	1	R	0
x	1	1	1	R	1
1	0	x	1	R	1
x	x	x	0	x	0
x	x	x	1	x	IQ

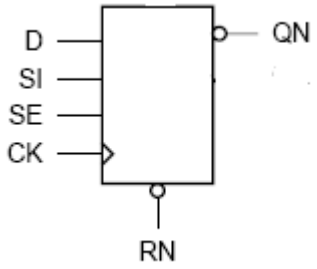
sdcrqN datasheet details refer to doc/DATASHEET/html/

SDCRN

Cell Description

The SDCRN cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low reset (RN) a single output (QN)

Logic Symbol



Functions table

INPUT					OUTPUT
D	SE	SI	RN	CK	QN
0	0	x	1	R	1
x	1	0	1	R	1
x	1	1	1	R	0
1	0	x	1	R	0
x	x	x	0	x	1
x	x	x	1	x	IQN

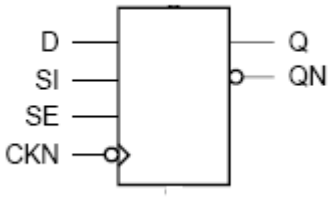
sdcrnN datasheet details refer to doc/DATASHEET/html/

SDNFB

Cell Description

The SDNFB cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE)

Logic Symbol



Functions table

INPUT				OUTPUT	
D	SE	SI	CKN	Q	QN
0	0	x	F	0	1
x	1	0	F	0	1
x	1	1	F	1	0
1	0	x	F	1	0
x	x	x	x	IQ	IQN

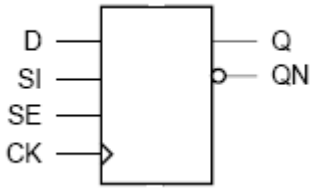
sdnfbN datasheet details refer to doc/DATASHEET/html/

SDNRB

Cell Description

The SDNRB cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE),

Logic Symbol



Functions table

INPUT				OUTPUT	
D	SE	SI	CK	Q	QN
0	0	x	R	0	1
x	1	0	R	0	1
x	1	1	R	1	0
1	0	x	R	1	0
x	x	x	x	IQ	IQN

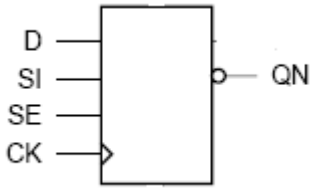
sdnrbN datasheet details refer to doc/DATASHEET/html/

SDNRN

Cell Description

The SDNRN cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), a single output (QN)

Logic Symbol



Functions table

INPUT				OUTPUT
D	SE	SI	CK	QN
0	0	x	R	1
x	1	0	R	1
x	1	1	R	0
1	0	x	R	0
x	x	x	x	IQN

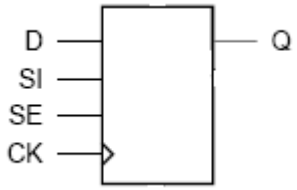
sdnrnN datasheet details refer to doc/DATASHEET/html/

SDNRQ

Cell Description

The SDNRQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), a single output (Q)

Logic Symbol



Functions table

INPUT				OUTPUT
D	SE	SI	CK	Q
0	0	x	R	0
x	1	0	R	0
x	1	1	R	1
1	0	x	R	1
x	x	x	x	IQ

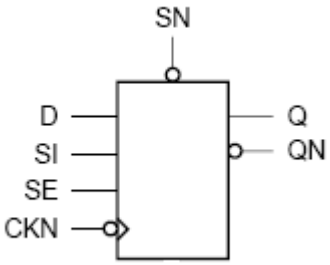
sdnrqN datasheet details refer to doc/DATASHEET/html/

SDPFB

Cell Description

The SDPFB cell is a negative-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN)

Logic Symbol



Functions table

INPUT					OUTPUT	
D	SE	SI	SN	CKN	Q	QN
0	0	x	1	F	0	1
x	1	0	1	F	0	1
x	1	1	1	F	1	0
1	0	x	1	F	1	0
x	x	x	0	x	1	0
x	x	x	1	x	IQ	IQN

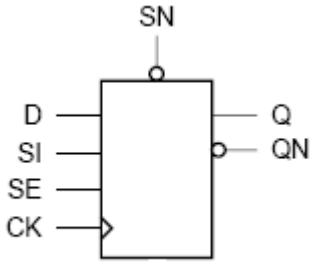
sdpfbN datasheet details refer to doc/DATASHEET/html/

SDPRB

Cell Description

The SDPRB cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN)

Logic Symbol



Functions table

INPUT					OUTPUT	
D	SE	SI	SN	CK	Q	QN
0	0	x	1	R	0	1
x	1	0	1	R	0	1
x	1	1	1	R	1	0
1	0	x	1	R	1	0
x	x	x	0	x	1	0
x	x	x	1	x	IQ	IQN

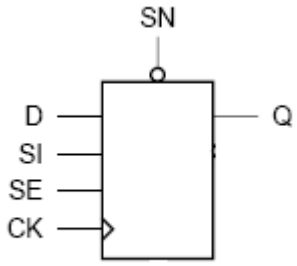
sdprbN datasheet details refer to doc/DATASHEET/html/

SDPRQ

Cell Description

The SDPRQ cell is a positive-edge triggered, static D-type flip-flop with scan input (SI), active-high scan enable (SE), and asynchronous active-low set (SN) a single output (Q)

Logic Symbol



Functions table

INPUT					OUTPUT
D	SE	SI	SN	CK	Q
0	0	x	1	R	0
x	1	0	1	R	0
x	1	1	1	R	1
1	0	x	1	R	1
x	x	x	0	x	1
x	x	x	1	x	IQ

sdprqN datasheet details refer to doc/DATASHEET/html/

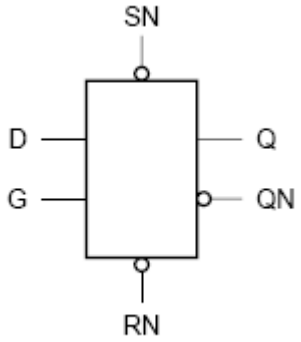
LATCHES

LABHB

Cell Description

The LABHB cell is an active-high D-type transparent latch with asynchronous active-low set (SN)and reset (RN),and set dominating reset.When the enable (G) is high, data is transferred to the outputs (Q, QN).

Logic Symbol



Functions table

INPUT				OUTPUT	
D	RN	SN	G	Q	QN
x	x	0	x	1	0
x	0	1	x	0	1
x	1	1	0	IQ	IQN
0	1	1	1	0	1
1	1	1	1	1	0

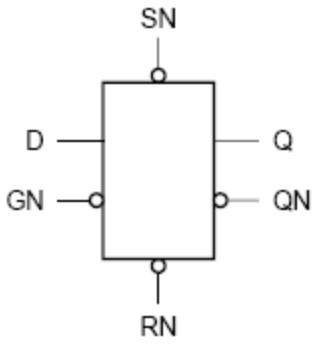
labhbN datasheet details refer to doc/DATASHEET/html/

LABLB

Cell Description

The LABLB cell is an active-low D-type transparent latch with asynchronous active-low set (SN)and reset (RN),and set dominating reset.When the enable (GN) is low, data is transferred to the outputs (Q, QN).

Logic Symbol



Functions table

INPUT				OUTPUT	
D	RN	SN	GN	Q	QN
x	x	0	x	1	0
x	0	1	x	0	1
0	1	1	0	0	1
x	1	1	1	IQ	IQN
1	1	1	0	1	0

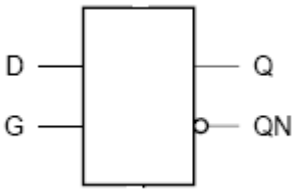
lablbN datasheet details refer to doc/DATASHEET/html/

LANHB

Cell Description

The LANHB cell is an active-high D-type transparent latch When the enable (G) is high, data is transferred to the outputs (Q, QN).

Logic Symbol



Functions table

INPUT		OUTPUT	
D	G	Q	QN
x	0	IQ	IQN
0	1	0	1
1	1	1	0

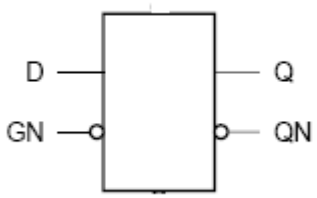
lanhbN datasheet details refer to doc/DATASHEET/html/

LANLB

Cell Description

The LANLB cell is an active-low D-type transparent latch , When the enable (GN) is low, data is transferred to the outputs (Q, QN)

Logic Symbol



Functions table

INPUT		OUTPUT	
D	GN	Q	QN
0	0	0	1
x	1	IQ	IQN
1	0	1	0

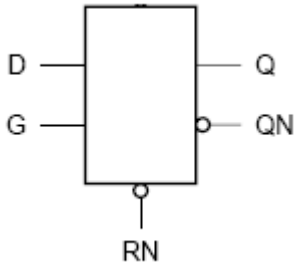
lanlbN datasheet details refer to doc/DATASHEET/html/

LACHB

Cell Description

The LACHB cell is an active-high D-type transparent latch with asynchronous active-low reset (RN) and When the enable (G) is high, data is transferred to the outputs (Q, QN)

Logic Symbol



Functions table

INPUT			OUTPUT	
D	RN	G	Q	QN
x	0	x	0	1
x	1	0	IQ	IQN
0	1	1	0	1
1	1	1	1	0

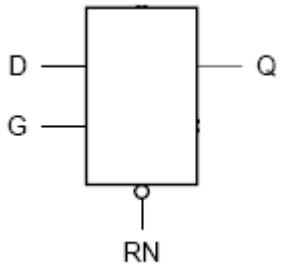
lachbN datasheet details refer to doc/DATASHEET/html/

LACHQ

Cell Description

The LACHQ cell is an active-high D-type transparent latch with asynchronous active-low reset (RN) and When the enable (G) is high, data is transferred to the output (Q)

Logic Symbol



Functions table

INPUT			OUTPUT
D	RN	G	Q
x	0	x	0
x	1	0	IQ
0	1	1	0
1	1	1	1

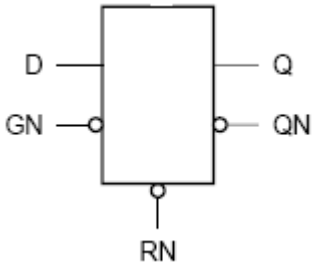
lachqN datasheet details refer to doc/DATASHEET/html/

LACLB

Cell Description

The LACLB cell is an active-low D-type transparent latch with asynchronous active-low reset (RN) and When the enable (GN) is low, data is transferred to the outputs (Q, QN)

Logic Symbol



Functions table

INPUT			OUTPUT	
D	RN	GN	Q	QN
x	0	x	0	1
0	1	0	0	1
x	1	1	IQ	IQN
1	1	0	1	0

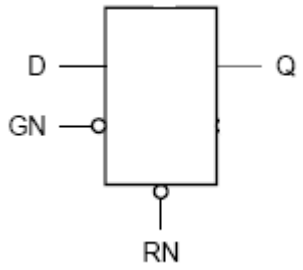
laclbN datasheet details refer to doc/DATASHEET/html/

LACLQ

Cell Description

The LACLQ cell is an active-low D-type transparent latch with asynchronous active-low reset (RN) and When the enable (GN) is low, data is transferred to the output (Q)

Logic Symbol



Functions table

INPUT			OUTPUT
D	RN	GN	Q
x	0	x	0
0	1	0	0
x	1	1	IQ
1	1	0	1

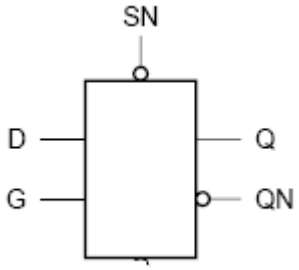
laclqN datasheet details refer to doc/DATASHEET/html/

LAPHB

Cell Description

The LAPHB cell is an active-high D-type transparent latch with asynchronous active-low set (SN) and When the enable (G) is high, data is transferred to the outputs (Q, QN)

Logic Symbol



Functions table

INPUT			OUTPUT	
D	SN	G	Q	QN
x	0	x	1	0
x	1	0	IQ	IQN
0	1	1	0	1
1	1	1	1	0

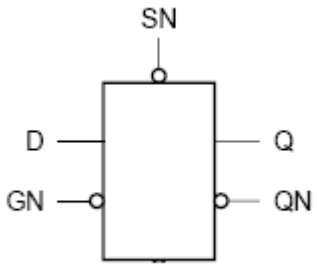
laphbN datasheet details refer to doc/DATASHEET/html/

LAPLB

Cell Description

The LAPLB cell is an active-low D-type transparent latch with asynchronous active-low set (SN) and When the enable (GN) is low, data is transferred to the outputs (Q, QN)

Logic Symbol



Functions table

INPUT			OUTPUT	
D	SN	GN	Q	QN
x	0	x	1	0
0	1	0	0	1
x	1	1	IQ	IQN
1	1	0	1	0

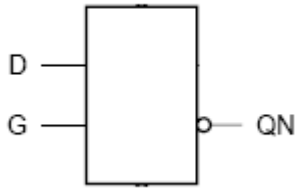
laplbN datasheet details refer to doc/DATASHEET/html/

LANHN

Cell Description

The LANHN cell is an active-high D-type transparent latch When the enable (G) is high, data is transferred to the output (QN)

Logic Symbol



Functions table

INPUT		OUTPUT
D	G	QN
x	0	IQN
0	1	1
1	1	0

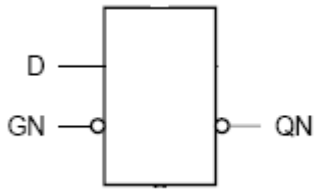
lanhnN datasheet details refer to doc/DATASHEET/html/

LANLN

Cell Description

The LANLN cell is an active-low D-type transparent latch When the enable (GN) is low, data is transferred to the output (QN)

Logic Symbol



Functions table

INPUT		OUTPUT
D	GN	QN
0	0	1
x	1	IQN
1	0	0

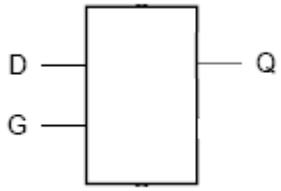
lanlnN datasheet details refer to doc/DATASHEET/html/

LANHQ

Cell Description

The LANHQ cell is an active-high D-type transparent latch When the enable (G) is high, data is transferred to the output (Q)

Logic Symbol



Functions table

INPUT		OUTPUT
D	G	Q
x	0	IQ
0	1	0
1	1	1

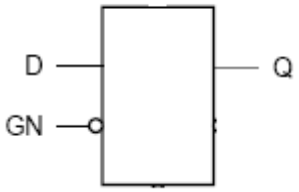
lanhqN datasheet details refer to doc/DATASHEET/html/

LANLQ

Cell Description

The LANLQ cell is an active-low D-type transparent latch When the enable (GN) is low, data is transferred to the output (Q)

Logic Symbol



Functions table

INPUT		OUTPUT
D	GN	Q
0	0	0
x	1	IQ
1	0	1

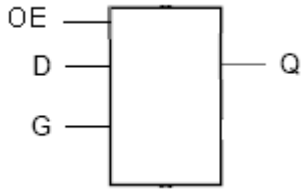
lanlqN datasheet details refer to doc/DATASHEET/html/

LANHT

Cell Description

The LANHT cell is an active-high D-type transparent latch When the enable (G) is high, data is transferred to the output (QN) by the enable pin (OE)

Logic Symbol



Functions table

INPUT			OUTPUT
D	OE	G	Q
x	0	x	HiZ
x	1	0	IQ
0	1	1	0
1	1	1	1

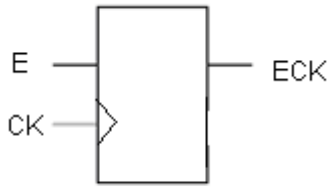
lanhtN datasheet details refer to doc/DATASHEET/html/

TLATNCAD

Cell Description

The TLATNCAD cell is clock gating cells with enable pin (E) .

Logic Symbol



Functions table

INPUT		Internal Pin	OUTPUT
E	CK	QN(n+1)	ECK
0	0	0	0
1	0	1	0
x	1	QN(n)	QN(n)

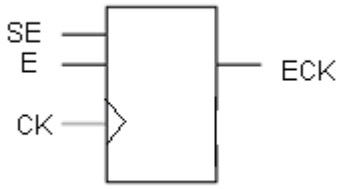
tlatncadN datasheet details refer to doc/DATASHEET/html/

TLATNTSCAD

Cell Description

The TLATNTSCAD cell is clock gating cells with enable pin (E) and test enable pin (SE)

Logic Symbol



Functions table

INPUT			Internal Pin	OUTPUT
E	SE	CK	QN(n+1)	ECK
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	1	0
x	x	1	QN(n)	QN(n)

tlatntscadN datasheet details refer to doc/DATASHEET/html/

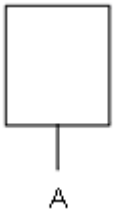
MISCELLANEOUS FUNCTIONS

ANTENNA

Cell Description

The library contains an antenna-fix cell which must be inserted manually. However, most place and route tools will indicate which nets require the antenna cell. The CSMC antenna effect prevention guideline, "*CSMC 0.153µm CMOS EN 1P6M process,*" specifies a maximum wire length. During place and route, the router may connect wires to the input gates of cells that are longer than the maximum length allowable by the guideline. The antenna cell can be used in this case to add an optional diode on the net close to the input gates which do not meet the guideline. Pin A on the antenna cell connects to a diode, reverse biased to ground.

Logic Symbol



antenna datasheet details refer to doc/DATASHEET/html/

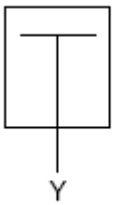
TIEHI

Cell Description

The TIEHI cell drives the output (Y) to a logic high. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:

$$Y = 1$$

Logic Symbol



tiehi datasheet details refer to doc/DATASHEET/html/

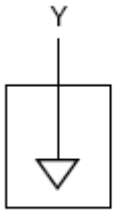
TIELO

Cell Description

The TIELO cell drives the output (Y) to a logic low. The output is driven through diffusion and not tied directly to the power rail to provide some ESD protection. The output (Y) is represented by the logic equation:

$$Y = 0$$

Logic Symbol



tielo datasheet details refer to doc/DATASHEET/html/

FILLER

Cell Description

The library contains several FILLER cells: FILLER1, FILLER2, FILLER4, FILLER8, FILLER16, FILLER32. The number appended to "FILLER" in the cell name denotes the width of the cell in tracks.

During place and route, the FILLER cells are used to connect power and ground rails across an area containing no cells. The FILLER cells are also used to ensure gaps do not occur between well or implant layers which could cause design rule violations. Using wider cells where appropriate reduces the size of the layout database.

FILLERCAP

Cell Description

The library contains several FILLER cells: FILLERCAP4, FILLERCAP8, FILLERCAP16, FILLERCAP32, FILLERCAP64. The number appended to "FILLERCAP" in the cell name denotes the width of the cell in tracks.