Data Sheet Summary

5V High Density Standard Cell Library for CSMC 0.153um
CMOS EN 5V Process

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DESCRIPTION

As technologies advance into deep sub-micron, a “System-On-Chip (SOC)” design posts great challenge to designers that need high quality standard cell libraries to achieve their design goals.
CSMC’s 0.153um cell library provides its customers with a cost effective SOC solutions to penetrate computer graphics, telecommunication, and consumer electronic markets. With the library development methodology, each core cell, input/output buffer, or memory macro is constructed from the most up-to-data design rules and electrical parameters.
CSMC offers almost all kinds of packages, including DIP, QFP, LQFP, TQFP, SOJ, SOP, SSOP and so on which can substantially reduce cost and turn-around time.
CSMC’s customers also receive DFT(Design-For-Test) service to ensure a high-quality library during mass production.

FEATURES

- CSMC 0.153um CMOS EN 5V Process
- 371 standard core cell
- Cell high :3.332um
- Interval cells optimized for synthesis.
- Accurate timing characterization
- Support most of the EDA tools
- Optimized for Cadence and Synopsys place&route tools.
- High density
- Routable for 3,4,5 or 6 metal

EDA TOOLS SUPPORT

- Verilog models
- VHDL models
- Synopsys synthesis models
- Composer schematic
- Synopsys test compiler models
- Cadence place & route tools
- Synopsys place & route
- GDSⅡ
- LVS spice netlist

Library Cell List

The csmc0153 CMOS EN internal library supports a rich set of variable functions. It includes the following types of function cells:

ad …….. Full Adder GATES
ah …….. Half Adder GATES
aoi …….. AND-NOR GATES
aor…….. AND-OR GATES
an……AND GATES
buff……Buffer GATES
buft……..TRI-STATE BUFFER
df…….D Flip-Flop
dl…….Delay GATES
filler ……. Filler CELL GATES
inv…….INVERTER GATES
la……..LATCH GATES
mi……Inverting MUX GATES
mx……MUX GATES
nd…….NAND GATES
nr……..NOR GATES
oai……OR-NAND GATES
or……OR GATES
sd……Scan D Flip-Flop
tla……Clock Gating
xn……...XNOR GATES
xr……XOR GATES

Cells listed below (368 cells in total)

Arithmetic Gates	
ad01dN	1-bit FULL ADDER (0,1,2)
ah01dN	1-bit Half Adder (0,1,2)

Buffers Gates

buffdN	Non Inverting(0,1,2,3,4,5,6,8,10)
buftdN	Non-inverting 3-state Buffer with active low enable (0,1,2)
buftldN	Non-inverting 3-state Buffer with active high enable (0,1,2,4,6,8)
inv0dN	Inverter (0,1,2,3,4,5,6,8,10)
invtdN	Inverter 3-state Buffer with active low enable (0,1,2)
invtldN	Inverter 3-state Buffer with active high enable (0,1,2)
dl01dN	Delay Gate(0,1,2)
dl02dN	Delay Gate(0,1,2)

COMPLEX Gates

aoi21dN	AND-NOR 2,1 (0,1,2)
aoi31dN	AND-NOR 3,1 (0,1,2)
aoi32dN	AND-NOR 3,2 (0,1,2)
aoi33dN	AND-NOR 3,3 (0,1,2)
aoi22dN	AND-NOR2,2 (0,1,2)
aoi211dN	AND-NOR 2,1,1 (0,1,2)
aoi221dN	AND-NOR 2,2,1 (0,1,2)
aoim21dN	AND-NOR2,1 2 invt (0,1,2)
aoim22dN	AND-NOR2,2 2 invt (0,1,2)
aoim31dN	AND-NOR3,3 1invt (0,1,2)
oai21dN	OR-NAND2,1 (0,1,2)
oai31dN	OR-NAND3,1 (0,1,2)
oai32dN	OR-NAND3,2 (0,1,2)
oai33dN	OR-NAND3,3 (0,1,2)
oai22dN	OR-NAND2,2 (0,1,2)
oai211dN	OR-NAND2,1,1 (0,1,2)
oai221dN	OR-NAND2,2,1 (0,1,2)
oai222dN	OR-NAND2,2,2 (0,1,2)
oai311dN	OR-NAND3,1,1 (0,1,2)
oai321dN	OR-NAND3,2,1 (0,1,2)
oai322dN	OR-NAND3,2,2 (0,1,2)
oaim21dN	OR-NAND2,1 2 invt (0,1,2)
oaim22dN	OR-NAND2,2 2 invt (0,1,2)
oaim211dN	OR-NAND2,1,1 2 invt (0,1,2)

oaim2m11dN	OR-NAND2,1 1 3 invt (0,1,2)
oaim31dN	OR-NAND3,1 3 invt (0,1,2)
aor21dN	AND-OR 2,1 (0,1,2)
aor22dN	AND-OR 2,2 (0,1,2)
aor211dN	AND-OR 2,1,1(0,1,2)
aor221dN	AND-OR 2,2,1 (0,1,2)
aor31dN	AND-OR 3,1 (0,1,2)
aor311dN	AND-OR 3,1,1 (0,1,2)
ora211dN	OR -AND 2,1,1 (0,1,2)
ora21dN	OR -AND 2,1 (0,1,2)
ora311dN	OR -AND 3,1,1 (1,2)
ora31dN	OR -AND 3,1 (0,1,2)

Gates

an02dN	AND 2 input (0,1,2)
an03dN	AND 3 input (0,1,2)
an04dN	AND 4 input (0,1,2)
an12dN	AND 2 input 1 invt (0,1,2)
an13dN	AND 3 input 1 invt (0,1,2)
an23dN	AND 3 input 2 invt (0,1,2)
nd02dN	NAND 2 input (0,1,2)
nd12dN	NAND 2 input 1 invt (0,1,2)
nd03dN	NAND 3 input (0,1,2)
nd13dN	NAND 3 input 1 invt (0,1,2)
nd04dN	NAND 4 input (0,1,2)
nd14dN	NAND 4 input 1 invt (0,1,2)
nd23dN	NAND 3 input 2 invt (0,1,2)
nd24dN	NAND 4 input 2 invt (0,1,2)
nr02dN	NOR 2 input (0,1,2)
nr12dN	NOR 2 input 1 inv (0,1,2)
nr03dN	NOR 3 input (0,1,2)
nr13dN	NOR 3 input 1 inv (0,1,2)
nr04dN	NOR 4 input (0,1,2)
nr14dN	NOR 4 input 1 inv (0,1,2)
nr23dN	NOR 3 input 2 inv (0,1,2)
nr24dN	NOR 4 input 2 inv (0,1,2)
or02dN	OR 2 input (0,1,2)
or03dN	OR 3 input (0,1,2)
or04dN	OR 4 input (0,1,2)
or12dN	OR 2 input 1 inv (0,1,2)
or13dN	OR 3 input 1 inv (0,1,2)
or23dN	OR 3 input 1 inv (0,1,2)

xn02dN	Excl-NOR 2 input (0,1,2)
xn03dN	Excl-NOR 3 input (0,1,2)
xr02dN	Excl-OR 2 input (0,1,2)
xr03dN	Excl-OR 3 input (0,1,2)

MULTIPLEXERS

mx02dN	Mux 2-to-1 (0,1,2)
mi02dN	Inverting Mux 2-to-1 (0,1,2)
mx04dN	Mux 4-to-1 (0,1,2)
mi04dN	Inverting Mux 4-to-1 (0,1,2)

FLIP FLOPS

dfbfbN	Neg. Edge DFF, preset & clear (1,2)
dfbrbN	Pos. Edge DFF, preset & clear (1,2)
dfbrqN	Pos. Edge DFF, preset & clear, Q only (1,2)
dfcfbN	Neg. Edge DFF, clear (1,2)
dfcfqN	Neg. Edge DFF, clear, Q only (1,2)
dfcrbN	Pos. Edge DFF, clear (1,2)
dfcrnN	Pos. Edge DFF, clear, QN only (1,2)
dfcrqN	Pos. Edge DFF, clear, Q only (1,2)
dfnfbN	Neg. Edge DFF (1,2)
dfnrbN	Pos. Edge DFF (1,2)
dfnrnN	Pos. Edge DFF, QN only (1,2)
dfnrqN	Pos. Edge DFF, Q only (1,2)
dfpfbN	Neg. Edge DFF, active-low preset (1,2)
dfprbN	Pos. Edge DFF, active-low preset (1,2)
dfprqN	Pos. Edge DFF, active-low preset,Q only(1,2)

LATCHES

labhbN	D latch, active-high enable, preset & clear (1,2)
lablbN	D latch, active-low enable, preset & clear (1,2)
lanhbN	D latch, active-high enable (1,2)
lanlbN	D latch, active-low enable (1,2)
lachbN	D latch, active-high enable, clear (1,2)
lachqN	D latch, active-high enable, clear , Q only (1,2)
laclbN	D latch, active-low enable, clear (1,2)
laclqN	D latch, active-low enable, clear , Q only (1,2)
laphbN	D latch, active-high enable, preset (1,2)
laplbN	D latch, active-low enable, preset (1,2)
lanhnN	D latch, active- high enable, QN only (1,2)
lanhqN	D latch, active- high enable, Q only (1,2)

lanlnN	D latch, active-low enable , QN only (1,2)
lanlqN	D latch, active-low enable , Q only (1,2)
lanhtN	D latch, active-high enable ,three tristate ,Q only (1,2)

SCAN FLIP FLOPS

sdbrbN	Pos.Edge Scan DFF, active-low set and clear (1,2)
sdbfbN	Neg.Edge Scan DFF, active-low set and clear (1,2)
sdbrqN	Pos.Edge Scan DFF, active-low set and clear, Q only (1,2)
sdcfbN	Neg.Edge Scan DFF, active-low clear (1,2)
sdcfqN	Neg.Edge Scan DFF, active-low clear, Q only (1,2)
sdcrbN	Pos.Edge Scan DFF, active-low clear (1,2)
sdcrqN	Pos.Edge Scan DFF, active-low clear, Q only (1,2)
sdcrnN	Pos.Edge Scan DFF, active-low clear, QN only (1,2)
sdnfbN	Neg.Edge Scan DFF (1,2)
sdnrbN	Pos.Edge Scan DFF (1,2)
sdnrnN	Pos.Edge Scan DFF, QN only (1,2)
sdnrqN	Pos.Edge Scan DFF, Q only (1,2)
sdpfbN	Neg.Edge Scan DFF, active-low preset (1,2)
sdprbN	Pos.Edge Scan DFF, active-low preset (1,2)
sdprqN	Pos.Edge Scan DFF, active-low preset ,Q only(1,2)

CLOCK GATE

tlatncadN	Clock gating(1,2,4)
tlatntscadN	Clock enable gating(1,2,4)

MISCELLANEOUS

antenna	Antenna Diode
fillercap	Filler cap cell(4,8,16,32,64)
filler	Filler cell(1,2,4,8,16,32)
fillersub	fillersub
tiehi	Logic High
tielo	Logic Low