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|  |  | **XXX 55nm** |  |  |
| No | **Rule name** | **Rules description** | **Value** | **Unit** |
| 1 | ACT\_W\_1 | ACT width | 0.08 | um |
| 2 | ACT\_W\_3a | Channel width for 0.9/1.2V NMOS/PMOS transistors | 0.12 | um |
| 3 | ACT\_S\_1 | Spacing between two ACTs | 0.11 | um |
| 4 |  |  |  | um |
| 5 | ACT\_EN\_2 | Enclosure P+ACT by NW1 | 0.15 | um |
| 6 | ACT\_S\_5 | Spacing between NW1 and N+ACT inside PW except NW1 resistor region | 0.15 | um |
| 7 | ACT\_S\_8 | Spacing between NW1 and P+ pickup ACT except LDMOS region | 0.15 | um |
| 8 | ACT\_A\_1 | ACT area | 0.038 | um² |
| 9 | PO\_W\_1/PO\_W\_3 | POLY width/Width of 45 degree PO | 0.06/0.18 | um |
| 11 | PO\_S\_3 | Space between two POs on ACT, DRC waive check the INDALL covered region. | 0.13 | um |
| 12 | PO\_EX\_1 | Extension of ACT outside of PO | 0.11 | um |
| 13 | PO-S.11 | Space between ACT and PO on STI. | 0.05 | um |
| 14 | PO\_Ex\_2 | Extension pf GATE poly outside of ACTs | 0.14 | um |
| 15 | NP\_W\_1 | NP width. Single-point-interaction is allowed | 0.18 | um |
| 16 | NP-S\_1 | Space between two NPs. | 0.18 | um |
| 17 | NP\_En\_1 /NP\_En\_2 | ACT exclosure by NP, except the SRAMALL region./N+AA enclosure by NP, except the SRAMALL region. | 0.02/0.12 | um |
| 18 | \ |  |  | um |
| 19 | \ |  |  | um |
| 20 | NP\_S\_2 | Space between NP and P+ACT inside NW | 0.12 | um |
| 21 | NP\_EX\_1\_EX\_1a | NP extension outside of NMOS GATE poly when NP edge is on ACT; | 0.3, | um |
|  | NP-En\_3 | NP extension outside of GATE/Minimum NP Enclosure PO | 0.16/0.15 | um |
| 22 | PP\_W\_1 | PP width. Single -point0-interaction is allowed | 0.18 | um |
| 23 | PP\_S\_1 | Spacing between two PPs. | 0.18 | um |
| 24 | PP\_EN\_1/PP\_EN\_2 | Enclosure of P+ ACT in PW, except the SRAMALL region./Enclosure of P+ ACT NW1， except the SRAMALL region | 0.02/0.12 | um |
|  |
| 25 | PP\_S\_3 | Space between PP and N+ ACT inside Nwell. | 0.02 | um |  |
|  |
| 26 | PP\_S\_2 | Space between PP and N+ ACT inside Nwell. | 0.12 | um |  |
| 27 | PP\_EX\_1\_EX\_1a/PP\_En\_3 | PP extension outside of PMIS GATE along source/drain direction; PP extension of PMOS gate when PP edge on ACTs./Minimum PP Eclosure of POLY | 0.16, 0.3/0.15 | um |  |
| 28 | CT-W.1 | Fixed CT width(square shape) exclude SRAMALL(177;4) FUSEALL, and GRID DRC waive rectangular CT in SRAM and EFUSRALL area, and waive protection ring purpose non-rectangulaer CT in GRID area | 0.09 | um |  |
| 29 | CT\_S\_1 | Space between two contacts | 0.11 | um |  |
| 30 | CT\_En\_2a/CT\_EN\_2b | CT enclosure by ACT for CT/CT enclosure by ACT for at least two opposite sides | 0.015/0.03 | um |  |
| 31 | CT\_S\_4 /CT-S.5 | Space between POLY and contact on ACT for 0.9V /1.2V /Space between POLY and contact on ACT for 1.8V /2.5V/3.3V | 0.055 /0.09 | um |  |
| 32 | CT\_EN\_3a\_3b\_3c | Min CT enclosure by poly is 0.01; Min CT enclosure by poly when one or both perpendicular directions < 0.04 | 0.01, 0.04 | um |  |
| 33 | CT\_S\_3 | Space between ACT and contact on POLY | 0.065 | um |  |
| 34 | MET1\_W\_1/MET1\_W\_2 | MET1 width /width of metal1 with 45 degree | 0.09/0.19 | um |  |
| 35 | MET1\_S\_1/MET1\_S\_2/MET1\_S\_3 | Space between two M1s, DRC don\BFt flag 89 to 90 degree space in the INDALL region/Min space between two M1is 0.15um when one or both M1 width >= 0.42um, and the parallel run length of two M1s >= 0.42um. /MinSpace between two M1 is 0.5um when one or both M1 width >=1.5um, and parallel run length of two M1s is >= 1.5um | 0.09/0.15/0.5 | um |  |
| 36 | CT\_EN\_4a\_4b\_4c/CT\_EN\_4b | Enclosure by M1; Enclosure by M1 at least two opposite sides< 0.04um; Enclosure by M1 for all sides./Minimum M1 enclosure of CT in line end region at least two opposite sides >=0.04 | 0;0.04;0.25/0.04 | um |  |
|  |
| 37 | MET1\_A\_1 | MET1 area | 0.042 | um² |  |
| 38 | Mn\_W\_1/Mn\_W\_2 | METn width /width of Mn with 45 degree | 0.1/0.19 | um |  |
| 39 | Mn\_S\_1 /Mn\_S\_2/Mn\_S\_3 | Space between two Mns/Space between two Mns when one or both Mn width >=0.42um, and the parallel run length of two Mns is >=0.42/Space between two Mns when one or both Mn width >1.5um, and the parallel run length of two Mns is >=1.5um | 0.1/0.15/0.5 | um |  |
| 40 | Vn-EN\_2a\_2b\_2c | Vn must fully enclosure by Mn; Min bottom metal enclosure of via\_layer dor two opposite sides; Vn must be fully enclosure by Mn.Mn=1 all sides | 0;0.04;0.03 | um |  |
| 41 | VIAn\_EN\_5a\_5b | Vn must be fully enclosure by Mn=1, Min up\_metal enclosure of via\_layer is 0.005; Min up\_metal enclosure of via\_layer is 0.02 when ip\_metal enclosure on one or both perpendicular directions | 0.005; 0.02 | um |  |
| 42 | V1\_W\_1 | Fixed Via 1 size (square shape) | 0.09 | um |  |
| 43 | V1\_S\_1 | Space between two Via 1s | 0.11 | um |  |