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Question: Cache block size (B) can affect both miss rate and miss late...

Cache block size (B) can affect both miss rate and miss latency. Assuming a machine with a base CPI of 1, and an average of 1.35 references (both instruction and data) per instruction, find the block size that minimizes the total miss latency given the following miss rates for various block sizes.

8: 4%	16: 3%	32: 2%	63: 1.5%	128: 1%
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- a.) What is the optimal block size for a miss latency of $20 \times B$ cycles?
 b.) What is the optimal block size for a miss latency of $24 + B$ cycles?
 c.) For constant miss latency, what is the optimal block size?

Expert Answer



Anonymous answered this
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a.) Average memory access time i.e (AMAT)

$$= (\text{Time for a hit}) + (\text{Miss rate}) \times (\text{latency})$$

but since CPI is given as "one", one cycle is time for a hit.

So

$$\begin{aligned} \text{AMAT} &= 1 + 4\% \times 160 = 7.4 \\ \text{AMAT} &= 1 + 3\% \times 320 = 10.6 \\ \text{AMAT} &= 1 + 2\% \times 640 = 13.8 \\ \text{AMAT} &= 1 + 1.5\% \times 1280 = 20.2 \\ \text{AMAT} &= 1 + 1\% \times 2560 = 26.6 \end{aligned}$$

Since from above,

Block size (B)	miss rate	latency	AMAT
8 bytes	4%	160 cycles	7.4
16 bytes	3%	320 cycles	10.6
32 bytes	2%	640	13.8
64 bytes	1.5%	1280	20.2
128 bytes	1%	2560	26.6

Hence the block size of 8 has the lowest AMAT i.e 7.4

b.) $\text{AMAT} = (\text{Time for a hit}) + (\text{Miss rate}) \times (\text{latency})$

$$\begin{aligned} \text{AMAT} &= 1 + 4\% \times 32 = 2.28 \\ &= 1 + 3\% \times 40 = 2.20 \\ &= 1 + 2\% \times 56 = 2.12 \\ &= 1 + 1.5\% \times 88 = 2.32 \\ &= 1 + 1\% \times 152 = 2.52 \end{aligned}$$

Block size	miss rate	latency	AMAT
8 bytes	4%	32 cycles	2.28
16	3%	40	2.20
32	2%	56	2.12
64	1.5%	88	2.32
128	1%	152	2.52

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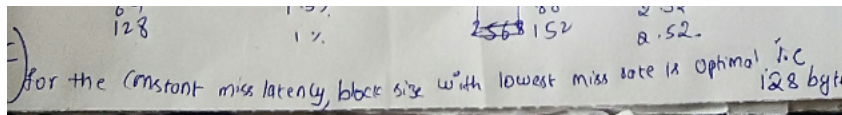
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M.Tech (CSE) from ...

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Q: 1. Consider one direct mapped cache with four sectors holding one block per sector and one 32-bit word per block. The machine is byte addressed on word boundaries and uses write allocation with write back. For each of the following cache accesses, is it a hit or miss? If it is a miss, identify the type of miss (compulsory, capacity, or conflict miss). Assume the cache starts out...

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