Question: Cache block size (B) can affect both miss rate and miss late...

Cache block size (B) can affect both miss rate and miss latency. Assuming a machine with a base CPI of 1, and an average of 1.35 references (both instruction and data) per instruction, find the block size that minimizes the total miss latency given the following miss rates for various block sizes.

8: 4%	16: 3%	32: 2%	63: 1.5%	128: 1%

a.) What is the optimal block size for a miss latency of 20 × B cycles?

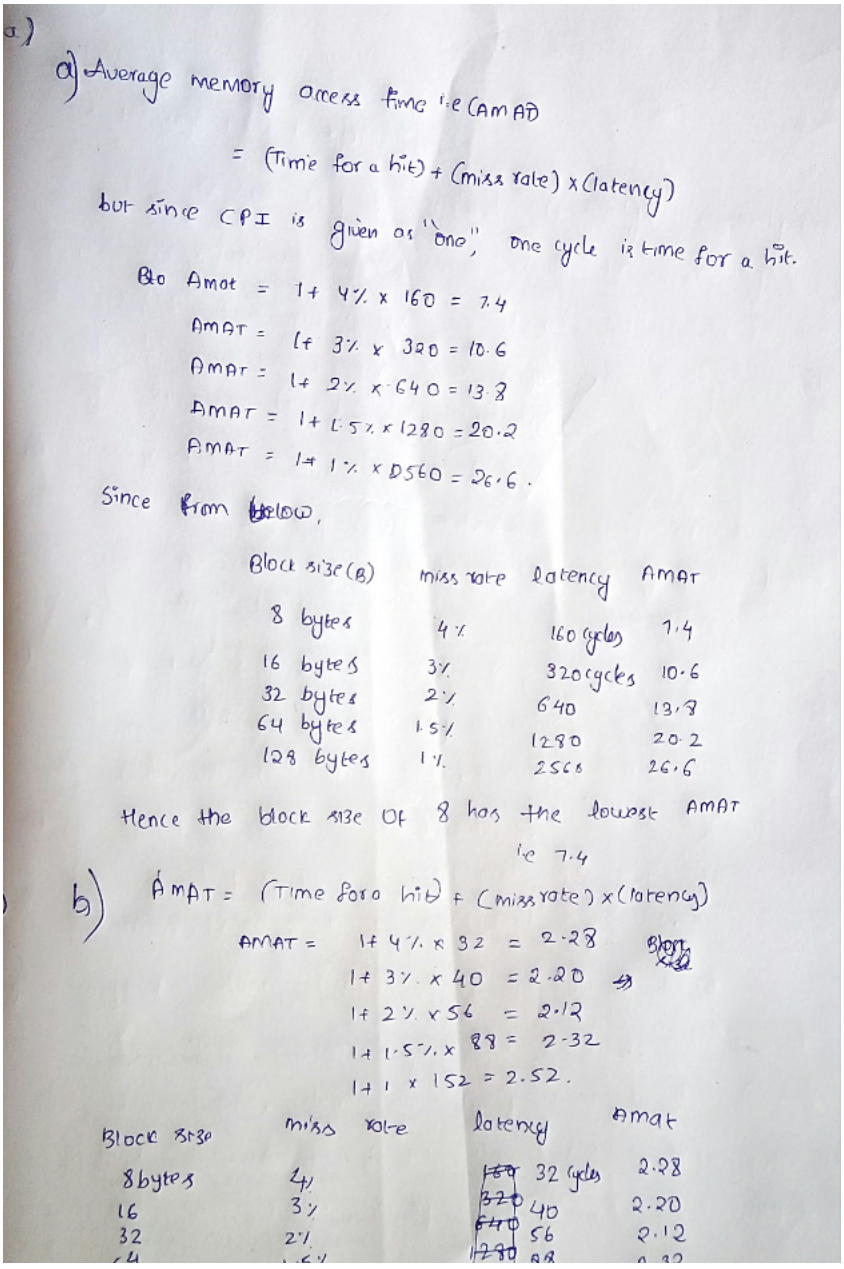
b.) What is the optimal block size for a miss latency of 24 + B cycles?

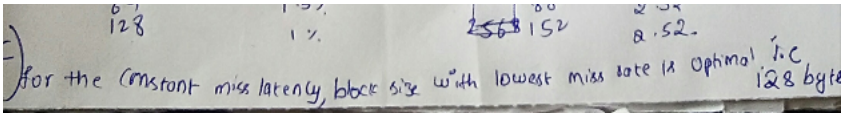
c.) For constant miss latency, what is the optimal block size?

Expert Answer

Anonymous answered this
239 answers

Was this answer helpful? 1 0





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Q: 1. Consider one direct mapped cache with four sectors holding one block per sector and one 32-bit word per block. The machine is byte addressed on word boundaries and uses write allocation with write back. For each of the following cache accesses, is it a hit or miss? If it is a miss, identify the type of miss (compulsory, capacity, or conflict miss). Assume the cache starts out...

A: See answer 100% (1 rating)

Q: help

A: See answer

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