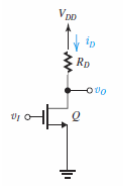
Module Quiz 6C (10 pts, close book & note)
Week 7 Thursday, Winter 2017

Design an invertor circuit to provide Voh = 1.2V, Vol = 50mV so that the current drawn from supply in the low output state is 30μA. Transistor Q has Vt = 0.4V, μnCox = 500μA/V2 and λ=0.



(a) Find Vdd, RD and (W/L)

(b) If RD is replaced by pMOS Qp to form a CMOS invertor and it is given that μp = μn/3, find Wp for Vm = Vdd/2 [Lp = Ln = 65nm, |Vtp| = 0.4V]. Comment on advantages and disadvantages of such a design.

(c) What is the output resistance of CMOS invertor designed in (b) when the output is high and low?