

EECS 112 & CSE 132, FALL 2017

Homework 1

Due date: October, 16, 2017

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256.

- 1) Represent the given numbers in the requested bases:

a) $(01101011001)_2 = (031121)_4 = (1531)_{16} = (359)_8$

b) $(7501)_8 = (F41)_{16}$
 $7 \cdot 8^3 + 5 \cdot 8^2 + 0 \cdot 8^1 + 1 \cdot 8^0 = 15 \cdot 16^2 + 4 \cdot 16^1 + 1 \cdot 16^0$
 $7 \cdot 512 + 5 \cdot 64 + 0 + 1 = 3584 + 320 + 1 = 3905$

c) $(11212)_3 = (203)_4$
 $1 \cdot 3^4 + 1 \cdot 3^3 + 2 \cdot 3^2 + 1 \cdot 3^1 + 2 \cdot 3^0 = 2 \cdot 4^3 + 3 \cdot 4^2$
 $81 + 27 + 18 + 3 + 2 = 131$

- 2) Find the binary representation of the following numbers in the correspondent system.

$n = 8 \text{ bits}$

$-37 \rightarrow 37 = (00100101)_2$

$-16 \rightarrow 16 = (00010000)_2$

Number	Sign Magnitude	1's Complement	2's Complement
-37	10100101	11011010	11011011
-16	10010000	11101111	11110000

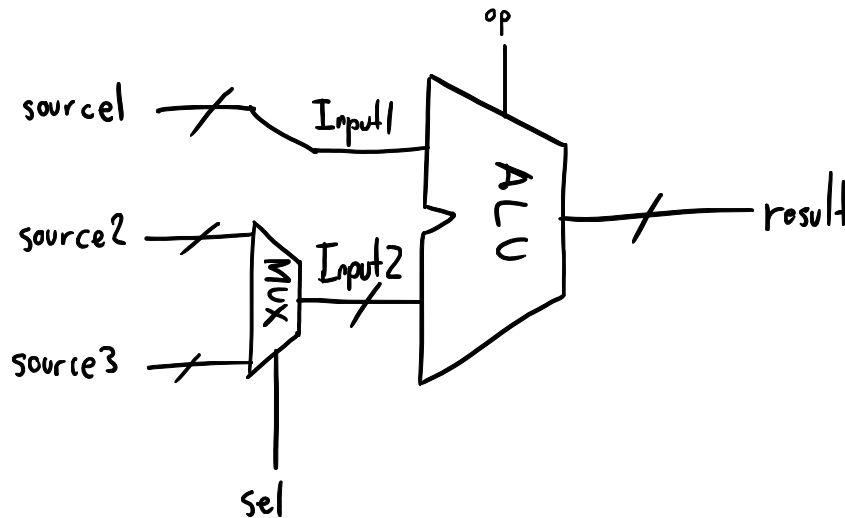
- 3) Find the correspondent decimal number of the following binary representations.

Binary representation (8 bit)	Sign Magnitude	1's Complement	2's Complement
$10011011 \rightarrow 27$ $16+8+2+1$	-27	-100	-101
$11010100 \rightarrow 54$ $64+16+4$	-84	-43	-44

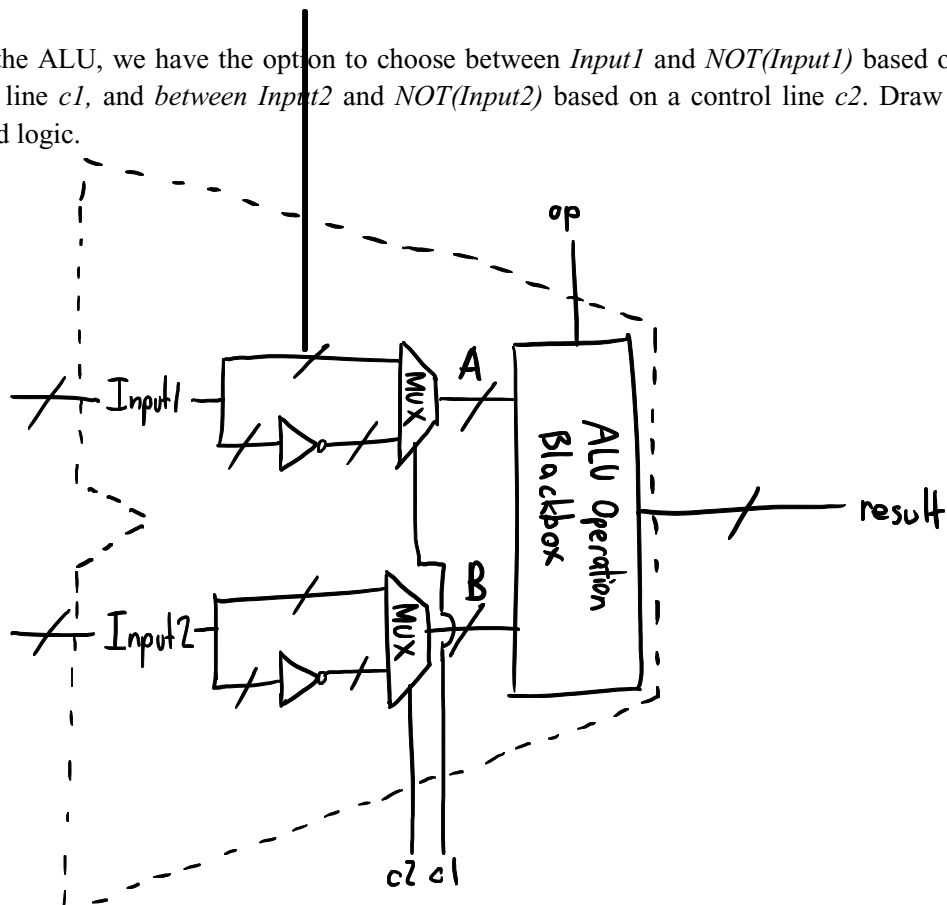
$1100100 \rightarrow 106$
 $64+32+4$
 $-128+27 = -101$
 $0101011 \rightarrow 43$
 $32+8+2+1$
 $-128+84 = -44$

- 4) Suppose we are implementing an ALU which always takes two inputs. The first input comes from *source1*, but the second input might come from either *source2* or *source3* based on some selection line *sel*.

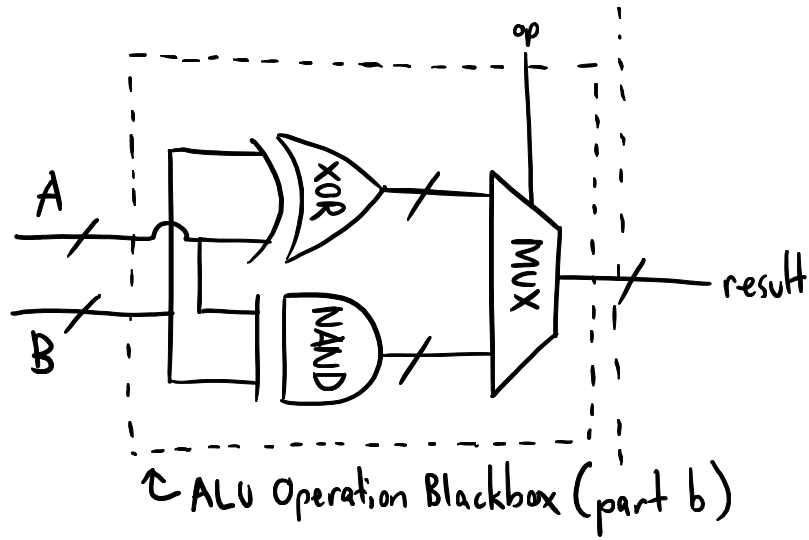
- a) Draw a black box for the ALU and add the required logic to support both *source2* and *source3* based on *sel*.



- b) Inside the ALU, we have the option to choose between *Input1* and $\text{NOT}(\text{Input1})$ based on a control line *c1*, and between *Input2* and $\text{NOT}(\text{Input2})$ based on a control line *c2*. Draw the required logic.

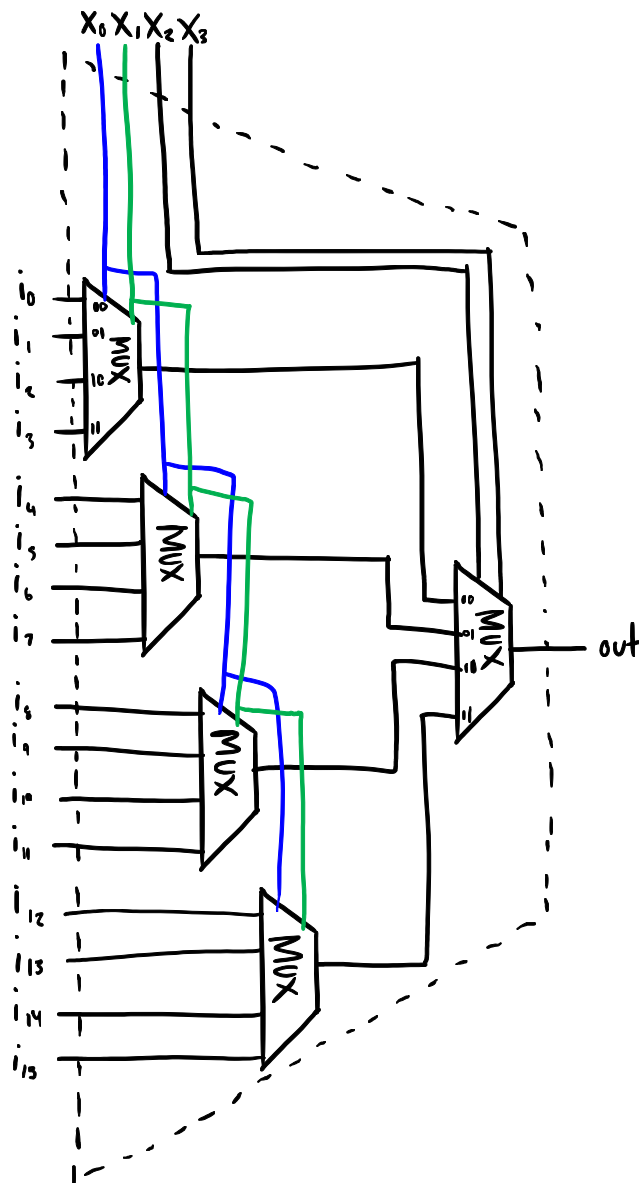


c) Finally, our ALU has two different instructions named XOR and NAND. Draw the required logic, assuming that the operation selection line is named *op*.



5) Design a 16-to-1 multiplexer using only 4-to-1 multiplexers.

Hint: A 16-to-1 multiplexer needs 4 select lines named $(X_3X_2X_1X_0)$. X_3 as the MSB and X_0 as the LSB.



Good Luck