Introduction to Digital Logic
EECS/CSE 31L

Final Project : Part 2

EECS Department
Henry Samueli School of Engineering
University of California, Irvine

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Demonstration during Wednesday (11/30/2016) and Thursday (12/01/2016) lab sessions.

1 Implementing the processor on BASYS 3 board.

The goal of this part of the project is to implement the processor on the FPGA board and prove that the processor design is working.

1.1 Assignment Description

Congratulations! Now that you have a correctly working processor, all you have to do is to configure your FPGA and connect the 7-segment display to the output of the processor. Figure 1 gives a basic idea.

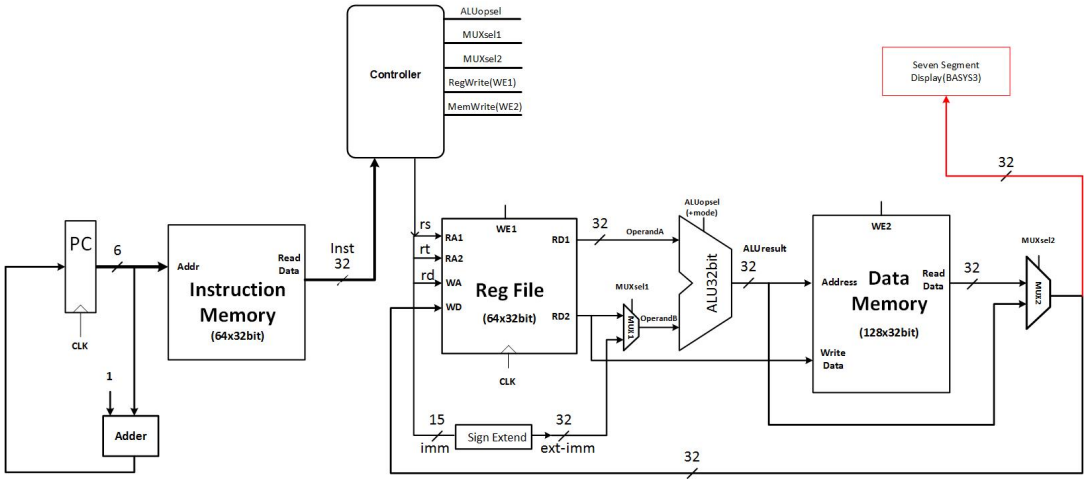

Figure 1: Processor

1.1.1 Processor module

Code 1: Port definition of processor in SystemVerilog

```
module processor(
    input logic clk,
    input logic rst,
    output logic [31:0]    reg_write_data
    );

endmodule
```

1.1.2 Instructions

To successfully implement your processor on the board you will need a Seven Segment display file and a Wrapper file. The seven segment display file will convert your processor output(Register write data) to seven segment output. The wrapper file will connect your processor to your seven segment display files.

Please make sure you processor module is same as above and add the wrapper and seven segment file to your design.

The next step is to assign the FPGA pin-outs. These pin assignments can be made using the constraint file. Download this file add as **constraints** to your project.

To test your design, you can hard code the instructions provided in the Instructions.txt to your Instruction memory.

1.2 Project Deliverables

A live demonstration of your processor will be required for all groups. You are encouraged to attend lab sessions either on Wednesday (11/23/2016) or Thursday (11/24/2016).

If you are unable to attend Wednesday and Thursday please email any of the TA's to setup another appointment for the demonstration.