Seek help early and not wait till the final 45 minutes of the lab class

The problems commonly encountered by students in lab 3, 4, 5 when using the Vivado software are documented here.

Students may use this as a "Self Help" guide to troubleshoot.

General problems in Lab 3, 4 and 5

	Wrong action	**Correct action**
1	Accidentally use earlier files created by other students	**Delete** any existing folder named Lab3, Lab4 or Lab5 from **Drive D**
2	Did not have all the required files for the project	Check that you have all the required • design files (*filename*.v) • simulation file (*filename*_tb.v) • and constraint file (*filename*.xdc) • in the **same** directory/folder (e.g. Lab3)
3	The required files are in different folders	• Create a directory (e.g. Lab3) in **Drive D** copy the required files to this new directory/folder (e.g. Lab3)
4	Unable to select the required FPGA part	Check that you are using the correct software **version**: Vivado 2022.2
5	Wrong FPGA part selected	• Go to Project Summary to select the correct **FPGA part**
6	The project is open in Drive C	• Create a directory (e.g. Lab3) in **Drive D** • copy the required files to this new directory/folder (e.g. Lab3) • Open the project and select **Drive D**
7	A module is missing	• Check that each module is contained within a single .v file • The module should have the same name as the filename Check that the .v file is added to the project as a **design** source
8	Wrong module is set as top module	• Right click on the correct module to set it as the **top module**
9	*filename*_tb.v file added as a design file or constraint file	• Right click to remove the file • add the file as a **simulation** source
10	*filename*.xdc file added as a design file or simulation file	• Right click to remove the file • add the file as a **constraint** source
11	*filename*.v file added as a constraint file or testbench file	• Right click to remove the file • add the file as a **design** source
12	*filename*.xdc file not added to project	• Constraint file is required for implementation • Add the file as a **constraint** source

13	More than one *filename*.xdc files are added to project	• A circuit only has **one** constraint file • Right click to remove the extra constraint file
14	Unable to program hardware	• Slide the FPGA board **power switch to ON**
15	Modify design file but no observable difference in simulation or implementation result	• Do not open more than one instance of Vivado • Keep only one instance – with the design file that you have modified – and close all the others

Common Problems in Lab 3

	Wrong action	**Correct action**
1	Syntax error: Did not enter semicolon after each assign statement	Make sure each assign statement ends with a semicolon (;)
2	Entered one or more incorrect Boolean expressions for segment c, d or f	• Look at the simulation result for seg_L[6:0] • Compare with the expected result of seg_L[6:0] given in the Vivado guide • Deduce the incorrect segment by looking at the bit position that has error • Seg_L[2] is segment c • Seg_L[3] is segment d • Seg_L[5] is segment f • Correct the segment expression

Common Problems in Lab 4

	Wrong action	**Correct action**
1	vaddflow only has inputs but no outputs declared	Make sure vaddflow has these outputs: • seg_L • oflow
2	[0:0] oflow declared	Do not declare size for a single-bit signal
3	[0:6] seg_L declared	should be [6:0] seg_L
4	Wrong size declared for inputs a and b of vaddflow	Inputs a, b are 4-bit signals
5	oflow not assigned a value	oflow is the carry output of (a+b)
6	Missing endcase	Make sure to end a case statement using the keyword **endcase**
7	seg_L wrongly declared as reg in module vaddflow	• seg_L is assigned a value by instantiating vsevenseg • seg_L should not be declared **reg**
8	seg_L is not declared as reg in module vsevenseg	• seg_L is assigned a value within an always block

		• seg_L should be declared **reg**
9	vsevenseg wrongly set as top module	right click to set vaddflow as top module

Common Problems in Lab 5

	Wrong action	**Correct action**
1	[0:0] clk, rst declared	Do not declare size for a single-bit signal
2	value not declared	• value is a multi-bit signal (aka vector or bus) • Its size must be correctly declared
3	Wrong clk used for scroll	Look carefully at Figure 1 of the lab manual to see the correct clock signal that scroll should use
4	Wrong inputs given to convert	Check that the correct inputs are given to each of the 4 instances of convert

Consider the following options when your circuit does not work correctly:

1. Look at the sources of other students whose circuits are working to compare and identify what your circuit design might have been done differently
2. Ask the lab supervisor or graduate student for assistance. Note that they may give you pointers but are not obliged to make your circuit work.
3. When nothing seems wrong with your sources (i.e. your circuit design) but there are still problems with Vivado, close it. Create a new folder with a different name (e.g. lab4a), copy all the essential source files into it. Start a new Vivado project pointing to this new folder, add all the needed sources correctly. Run implementation again. On many past occasions the problems got resolved by itself this way.
4. When all else have failed, you may repeat item (3) above on a different PC.