L1 practice questions

Logic gates & Boolean algebra

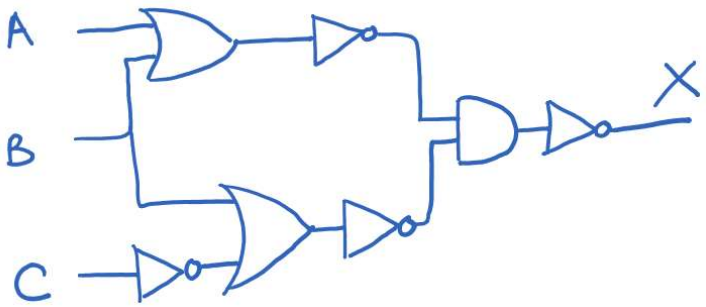
1. In each case below, draw a logic circuit diagram that implements the Boolean expression. Also construct the truth table for each circuit.

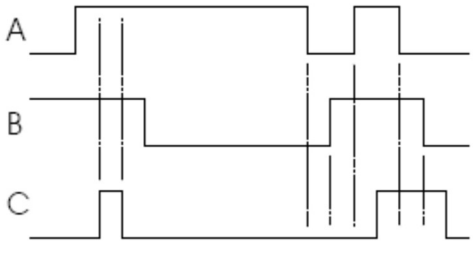
   (a) X = [(A+B)'(B'C)]'

   (b) X = [(ABC)'(A+D)]'

2. Suppose you have an unknown two-input gate that is either an OR gate or an AND gate. What combination of input levels should you apply to the gate's inputs to determine which type of gate it is? (Tocci et al. 10th ed Q3-9)

3. Write the expression for the output X of the circuit below and use it to determine the complete truth table. Then apply the waveforms that follow to the circuit inputs and draw the resulting output waveform. (Tocci et al. 10th ed Q3-19).





L2 practice problems

Algebraic simplification with Boolean theorems

1. Tocci et al 10th ed Q3-24(a)

Simplify the following expression using the theorems that follow.

$x = (M + N)(M' + P)(N' + P')$

Theorems :-

$x \cdot x = x$
$x \cdot x' = 0$
$(w + x)(y + z) = wy + xy + wz + xz$

2. Tocci et al 10th ed Q3-24(b)

Simplify the following expression using the theorems that follow.

$Z = A'BC' + ABC' + BC'D$

Theorems :-

$x(y + z) = xy + xz$
$x + x' = 1$
$x + 1 = 1$

3. Simplify each of the expressions using DeMorgan's theorem. (Tocci et al 10th ed Q3-26)

[a] (A'BC')'
[b] (A'+B'C)'
[c] (ABC'D)'
[d] (A+B')'
[e] (A'B')'
[f] (A'+C'+D')'
[g] (A(B+C')'D)'
[h] ((M+N')(M'+N))'
[i] (((AB)'C)'D)'

4. Draw the logic circuit diagram for each Boolean expression below using NAND and NOR symbols where suitable.

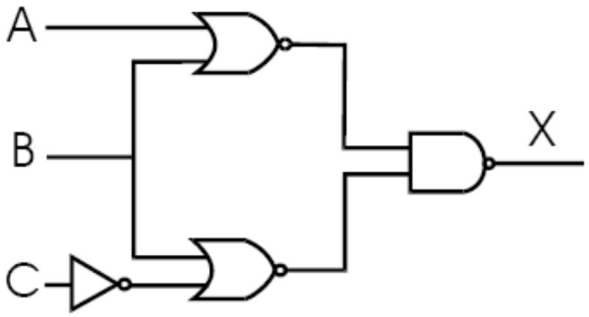
(a) X = [(A+B)'(B'C)]'

(b) X = [(ABC)'(A+D)]'

L3 practice problems

Alternate logic symbols

1. The following logic circuit diagram is taken from Question 3 in L1 Practice.



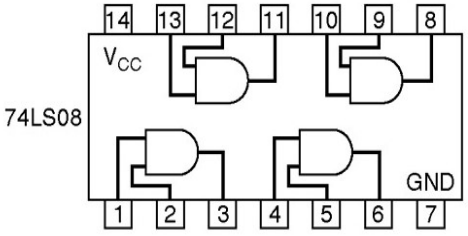
   a. Identify the connections that do not follow bubble-to-bubble matching.

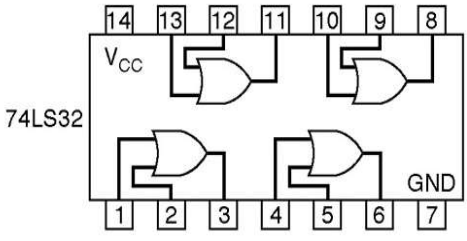
   b. Redraw the diagram using appropriate logic symbols such that it follows bubble-to-bubble matching. Your diagram should show clearly how logic 0 can be produced at output X.

   c. Redraw the diagram using appropriate logic symbols such that it follows bubble-to-bubble matching. Your diagram should show clearly how logic 1 can be produced at output X.

Circuit connection diagram

2. Given the following quad-AND and quad-OR ICs, draw the circuit connection diagram for the implementation of (A+B)(C+D). Include pin numbers and connections for Vcc and Gnd in your diagram.





L4 practice problems

4-bit additions

Complete the following pairs of 4-bit addition. Repeat using hexadecimal digits.

(a) 1010 + 0011

(b) 1000 + 1011

Signed number representations

Complete the following table for each signed decimal value given in the first column. Use only the necessary number of bits in each case.

	Signed decimal	Unsigned binary	**sign-magnitude** representation	**2's complement** representation
a	-127			
b	-112			
c	-60			
d	-30			
e	30			
f	60			
g	112			
h	127			

L5 practice problems

2's complement representation

1. The following are signed numbers in 8-bit 2's complement representation.

    a) 0010 0110
    b) 0111 1111
    c) 1000 0001
    d) 1111 1111

    (i) Rewrite the numbers in hexadecimal notation
    (ii) Determine their signed decimal values.

Arithmetic overflow

2. Determine whether arithmetic overflow occurs in each of the following 8-bit 2's complement arithmetic operations:

    a) 1110 0010 + 0100 0010
    b) 0101 1000 – 1000 0010
    c) 0111 1111 + 0000 0010
    d) 1110 0001 – 1111 1101

3. Repeat Q2 using hexadecimal digits.

L6 practice problems

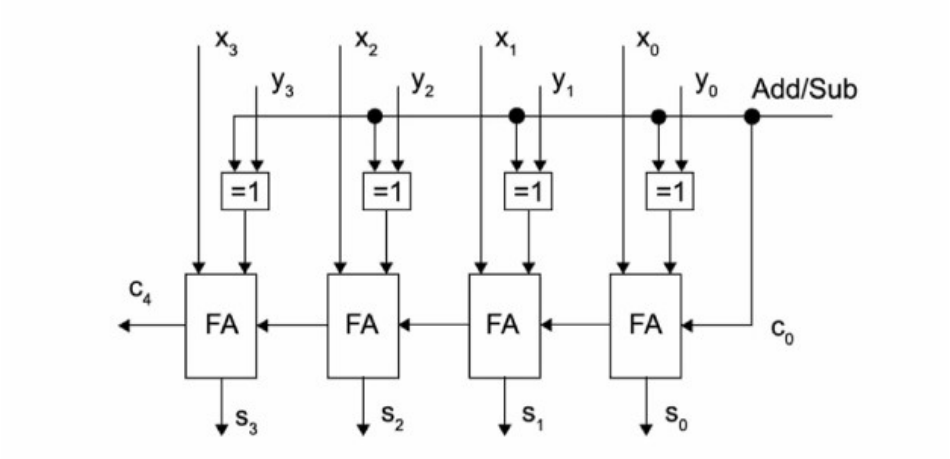
1. Perform the following unsigned addition operation. Each 8-bit unsigned input is represented in hexadecimal. Give the decimal equivalent of the input values and also of the result.

   9F + 4E

2. Perform the following signed 2's complement addition. Each 8-bit signed input is represented in hexadecimal. Give the decimal equivalent of the input values and also of the result.

   9F + 4E

3. Illustrate how the signed 2's complement subtraction of the decimal values (3 – 7) is carried out in the following circuit by indicating the logic level (i.e. 0 or 1) at every input and output (including carry signals) on the circuit.



4. Draw the diagram of a 6-bit wide 2's complement adder/subtractor circuit using six full adders.

L7 practice problems

1. Construct the truth table for the following logic functions.
   a. F(X,Y,Z) = X'Y + X'Y'Z
   b. F(A,B,C,D) = (((A+B')' + C)'+D)'

2. Write the canonical sum-of-minterm expression for output F in question 1(a).

3. Write the canonical product-of-maxterm expression for output F in question 1(b).

4. The following expressions are taken from lecture slides 5.23. Use algebraic manipulations to simplify each of them and obtain the minimum cost SOP (sum-of-product) expression.

   Students are required to know and apply Boolean theorems but are not required to cite the name of the theorems used

   a. Z = ABC + AB'(A'C')'

   b. X = (A' + B)(A + B + D)D'

L8 practice problems

1. Design a combinational logic circuit that converts a 4-bit Excess-3 code into a BCD code. Your design needs to accept only those inputs that produce valid BCD codes. Use K-map method for simplification and make use of any don't care conditions.

   Hint: this circuit has 4 inputs and 4 outputs. To fulfill the design, a Boolean expression must be obtained for each output.

   An excess-3 code is obtained by adding the decimal value 3 to a BCD code. For example, decimal 0 is 0000 in BCD, which is 0011 in excess-3. See partial truth table below.

   Partial truth table:

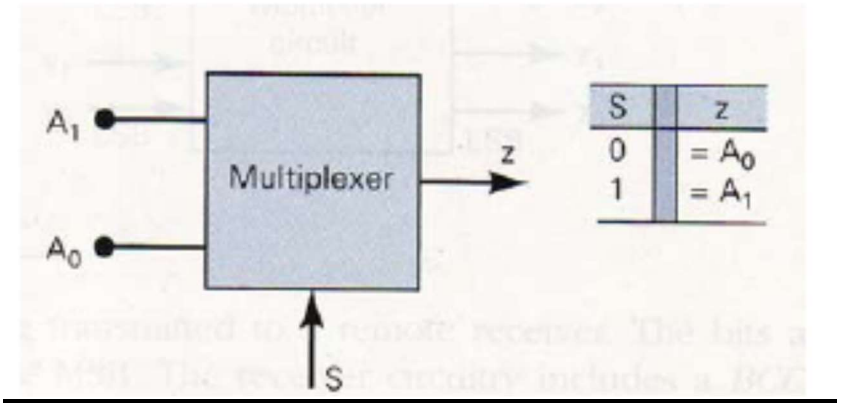
Input				Output			
Excess-3 code				BCD code			
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
1	1	0	0	1	0	0	1

2. Problem 4.7 from Tocci 9th Ed.
   A 4-bit binary number is represented as A3, A2, A1, A0 where A0 is the LSB. Design a logic circuit that will produce a High output whenever the binary number is greater than 0010 and less than 1000.

   Note: otherwise the circuit produces a LOW output.

   Design typically means a Boolean expression must be obtained for the circuit output. With the expression, a logic circuit diagram may be drawn if needed.

3. Problem 4-35 from Tocci 9th Ed.
Design a logic circuit that has two signal inputs A1 and A0 and a control input S so that it functions according to the requirements given in the figure below. This circuit is a multiplexer which will be covered in the MSI syllabus.



4. Modify the circuit obtained in Question 3 such that it now has an active-high enable input EN whose effect is shown in the new truth table:

Inputs		Output
EN	S	Z
0	X	0
1	0	A0
1	1	A1

X = “don’t care”, i.e. 0 or 1

You may describe the modification with words or sketch a diagram to illustrate

L9 practice problems

1. The following English expression describes the way a logic circuit needs to operate in order to drive a seatbelt warning indicator in a car.

   If the driver is present and the driver is not buckled up and the ignition switch is on, then turn on the warning light.

   Using active high inputs driver_present, buckled_up and ignition_on, design a circuit to produce the active high output warning_light.

   (a) Construct the truth table.

   (b) Write the Boolean expression for warning_light.

   (Question from Tocci, Widmer and Moss, 10th ed. Example 3-24)

2. Repeat Question 1. But this time with active low inputs driver_present*, buckled_up*, ignition_on* and active low output warning_light*.

   Note the meaning of active low. E.g. driver_present*=0 when the driver is present.

3. Repeat Question 1. But this time with active low inputs driver_present*, buckled_up*, active high input ignition_on and active high output warning_light.

4. A logic circuit has four inputs A, B, C*, D* and one output F.
   * denotes active low signals.
   The output F is only asserted when either A or C* is asserted (but not both), and either B or D* is negated (but not both).
   Construct the truth table for F and obtain its canonical sum-of-minterm expression.

L10 practice problems

CMOS Logic

Determine the truth tables for the following CMOS logic circuits.

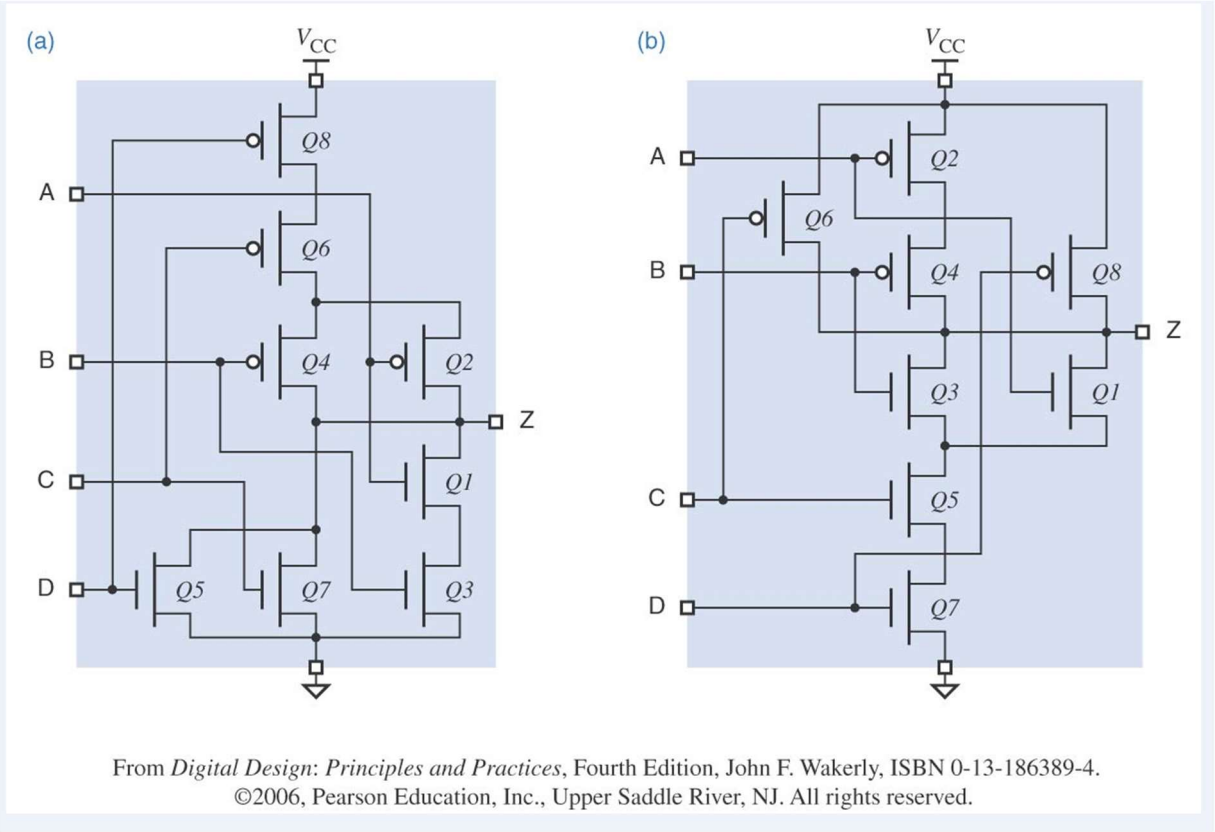


Fig. X3.11

Hint:
From the circuit diagram
Step 1: identify the inputs (e.g. A, B, C, D)
Step 2: identify the pair of transistors directly controlled by each input (e.g. input A controls Q1 and Q2)
Step 3: identify all the possible current paths (series as well as parallel) from Vcc to output so as to make output = 1.
For each possible path, identify the correct input values, and fill up the corresponding rows in the truth table with output=1
Step 4: identify all the possible current paths (series as well as parallel) from output to GND so as to make output = 0.
For each possible path, identify the correct input values, and fill up the corresponding rows in the truth table with output=0

L11 practice problems

1. Two different logic circuits have the characteristics shown below.

   (a) Which circuit has better DC noise margin?

   (b) Which circuit has better DC fan-out?

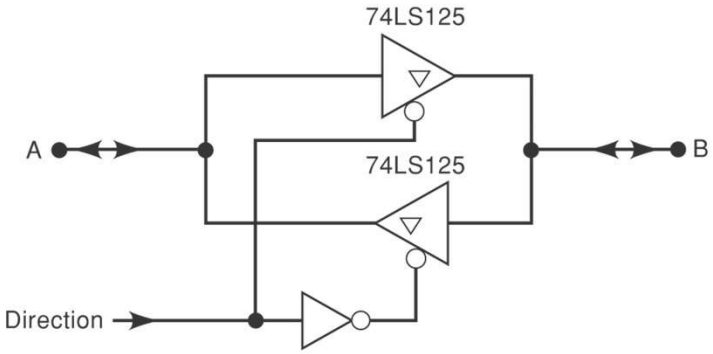
   (c) Which circuit can operate at a higher frequency?

   (d) Are the two circuits able to drive each other?

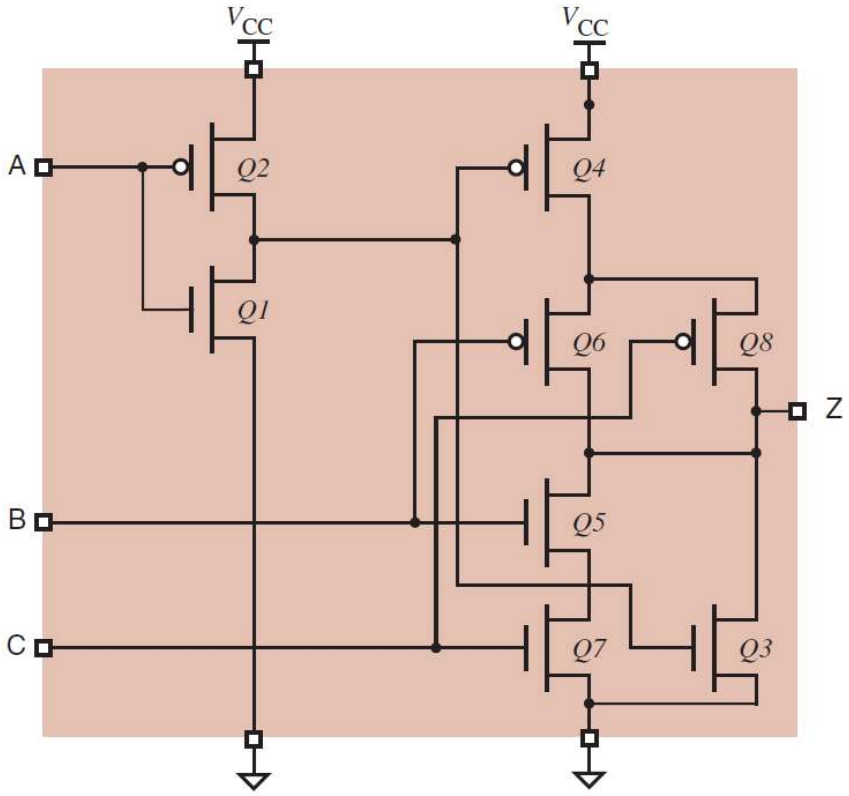
	Circuit A	Circuit B
Vcc (V)	5	5
VIH(min) (V)	1.6	1.8
VIL(max) (V)	0.9	0.7
VOH(min) (V)	2.2	2.5
VOL(max) (V)	0.4	0.3
IIH(max) (mA)	1.0	1.5
IIL(max) (mA)	1.0	1.5
IOH(max) (mA)	20	27
IOL(max) (mA)	25	30
tPLH (ns)	10	18
tPHL (ns)	8	14
PD (mW)	16	10

(Adapted from Tocci, Widmer and Moss, ed. 10)

2. The figure below shows how two tristate buffers can be used to construct a bidirectional transceiver that allows digital data to be transmitted from A to B, or from B to A. Describe the circuit operation.
   (Tocci, Widmer & Moss, ed. 10)



3. Describe the operation and hence obtain the Boolean expression for this CMOS circuit.
(Wakerly Ex. 3.59)

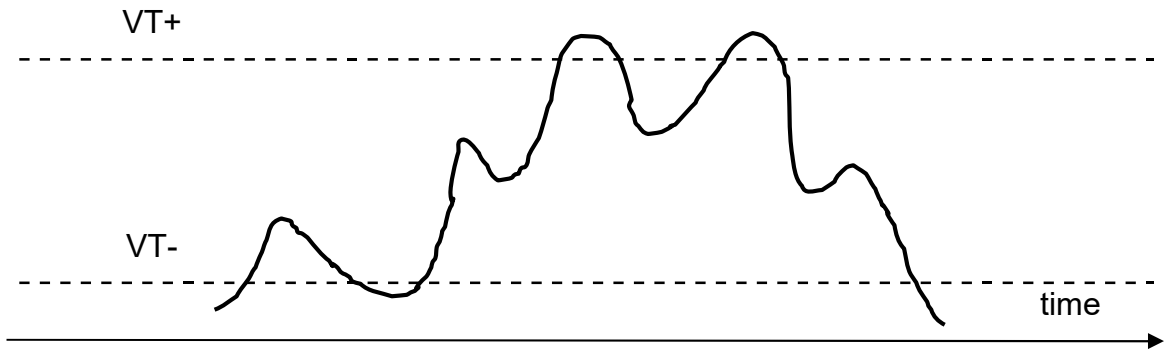


L12 practice problems

1. Given the following input waveform and threshold voltages VT+ and VT-, sketch the output waveforms for each Schmitt-Trigger device below:

   (a) buffer

   (b) inverter



2. Implement the given truth table using the following programmable logic device. Indicate the inputs, outputs and programmed connections clearly on the PLA diagram.

(Hint: use Karnaugh map to first obtain a minimum-cost SOP Boolean expression for x and for y)

Inputs				Outputs	
a	b	c	d	x	y
0	0	0	0	1	1
0	0	0	1	1	0
0	0	1	0	1	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	1	0	1
1	0	0	0	1	1
1	0	0	1	0	1
1	0	1	0	1	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	1	0

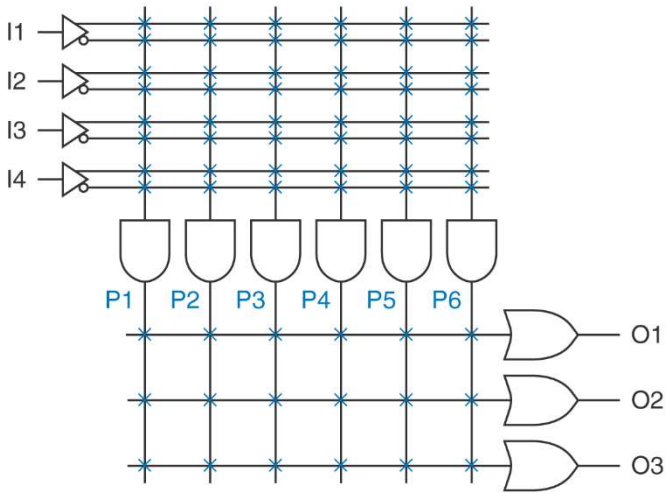


Figure 6-22

Compact representation of a 4 × 3 PLA with six product terms.

3. A digital system uses a 16-bit fixed point representation for unsigned numbers, with 8 bits allocated to the integer portion and 8 bits allocated to the fractional portion.
The 16-bit data format (in 4-bit groups for easy reading) is:
xxxx xxxx yyyy yyyy
where xxxx xxxx is the 8-bit integer portion, and yyyy yyyy is the 8-bit fractional portion.

(a) What is the smallest non-zero binary value that can be represented in this system? What is this value in decimal?

(b) What is the largest binary value that can be represented in this system? What is this value in decimal?

(c) What is the 16-bit representation of the decimal value 8.7? Is this an exact representation?