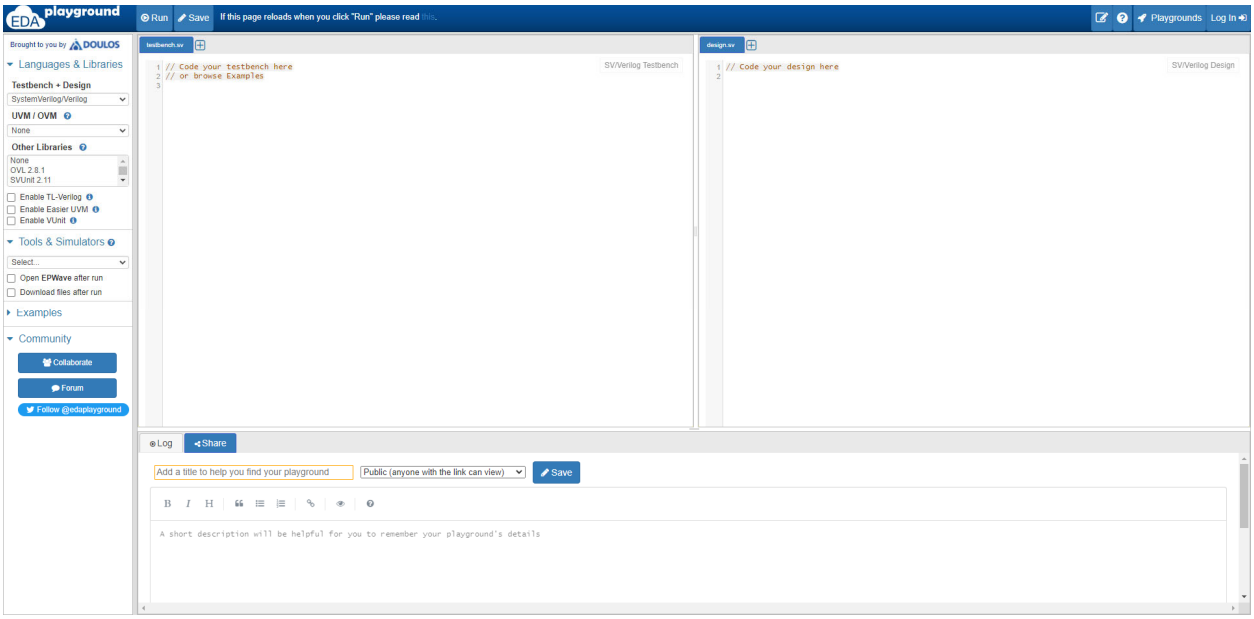
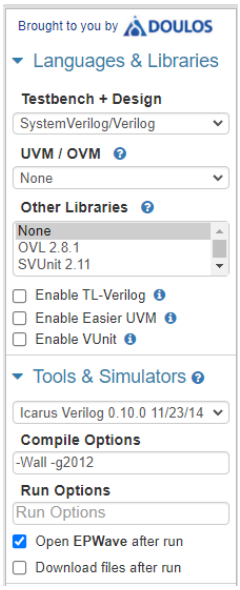
1. Access the URL https://www.edaplayground.com/ via your browser. You should see the following:



2. Register for an account if you have not done so by clicking 'Log in' at the upper right corner. Otherwise, login using your registered account.
3. In the left panel:
    - Select "System Verilog/Verilog" under **Testbench + Design**.
    - Select "None" under **UVM / OVM**.
    - Select "None" under **Other Libraries** and leave the subsequent options unchecked.
    - Select "Icarus Verilog 0.10.0" under **Tools & Simulators**. You can also explore the other free simulators available.
    - Tick the box "Open EPWave after run".



4. Type in your Verilog design in the **SV/Verilog Design** panel (right panel). I have used the example of a half adder.

design.sv

SV/Verilog Design

```
module half_adder (
    input wire a, b,
    output wire sum, carry
);

    assign sum = a ^ b;
    assign carry = a & b;

endmodule
```

5. Type in your Verilog tesbench in the **SV/Verilog Testbench** panel (left panel).
   Add a second initial block to your testbench file with the following system calls:

```
initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
end
```

   This will allow you to generate the waveform files in EPWave.

testbench.sv

SV/Verilog Testbench

```
// half_adder_tb.v

`timescale 1 ns/10 ps  // time-unit = 1 ns, precision = 10 ps

module half_adder_tb;

    reg a, b;
    wire sum, carry;

    // duration for each bit = 20 * timescale = 20 * 1 ns  = 20ns
    localparam period = 20;

    half_adder UUT (.a(a), .b(b), .sum(sum), .carry(carry));

    initial // initial block executes only once
        begin
            // values for a and b
            a = 0;
            b = 0;
            #period; // wait for period

            a = 0;
            b = 1;
            #period;

            a = 1;
            b = 0;
            #period;

            a = 1;
            b = 1;
            #period;
        end

  initial
        begin
            $dumpfile("dump.vcd");
            $dumpvars(1);
        end

endmodule
```

6. Click the **Run** button at the top of the window.
   You should see the following waveform.