Lab 1 Report

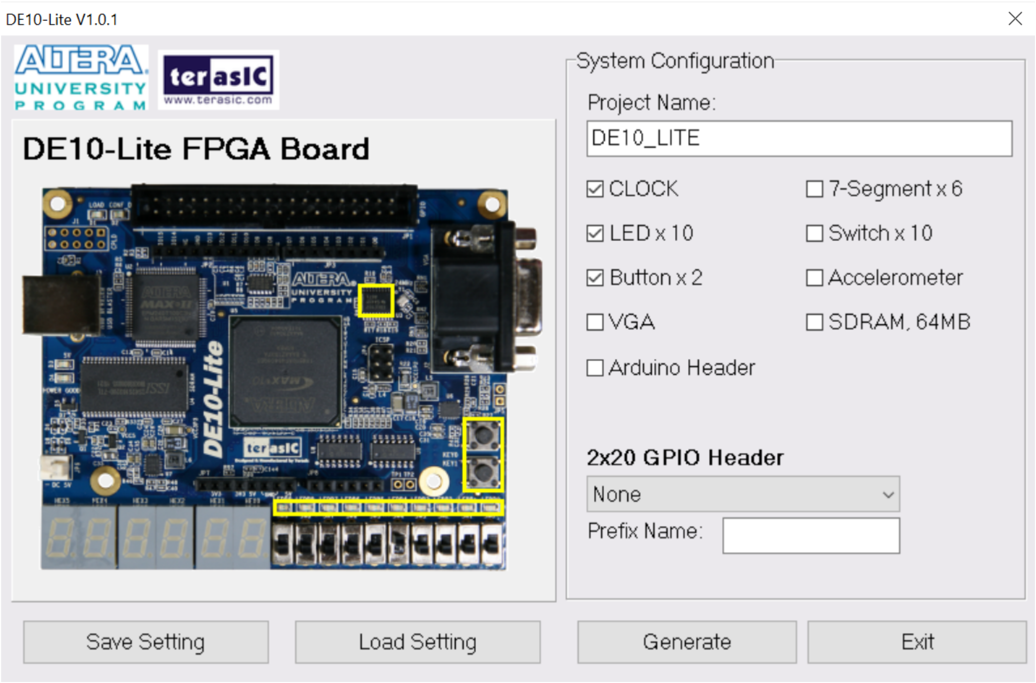
Matthew Crump A01841001
Nicholas Williams A02057223

Objectives

Implement a 10-bit counter on the DE-10 Lite development board. The timer should tick at a 1 Hz rate, have a reset button to set the counter back to zero, and be written in VHDL. Become familiar with Quartus Prime and simulate designs with ModelSim.

Procedure

We started out by reading the lab-1 requirements for the 10-bit counter. We then used the System Builder tool to initialize the Quartus Prime project for us (see Figure 1). We determined which I/O would be needed to implement the lab, those being: a 50 MHz clock, 10 LEDs, and a button for resetting the counter. As this was our first time writing a project in VHDL, we spent some time reviewing lecture slides covering VHDL syntax and conventions.



System Configuration

Project Name: DE10_LITE

☑ CLOCK
☑ LED x 10
☑ Button x 2
☐ VGA
☐ Arduino Header
☐ 7-Segment x 6
☐ Switch x 10
☐ Accelerometer
☐ SDRAM, 64MB

2x20 GPIO Header: None

Prefix Name:

Figure 1. System Builder tool

Our Project contains one entity and one architecture. In the entity we created a generic to make the 10-bit counter more configurable. The generic was set to the frequency of the clock, allowing the testbench to override this to a much smaller value for simulation. The entity also defined our device's clocks, keys (push buttons), and LEDs as ports for our model. The architecture contained two processes.

The architecture's first process is sensitive to the 50 MHz clock. The clock is used to increment a counter that then produces a 1 Hz tick. The 1 Hz tick is then used to increment the 10-bit counter. This was done because creating a clock divider with logic elements is not a good design practice (i.e. using a toggling register as a clock in a sensitivity list for a process). The generic that we defined in our entity is used to produce the 1 Hz tick, but for convenience that generic can be reduced for simulation purposes.

The architecture's second process is also sensitive to the 50 MHz clock. On the rising edge of the clock the process checks whether the reset button was pressed or whether the 1 Hz tick equals one. The reset button is considered a synchronous process since its functionality is reliant on the rising edge of the clock. When the reset button is pushed, the 10-bit counter is set to all zeros. When the 1 Hz tick equals one the 10-bit counter increments by one.

Results

Simulating the design showed that the VHDL for the board was functioning correctly. The clock counter would count up to 5 and produce a one clock tick pulse that would then cause the 10-bit counter to increment. After a few iterations, the reset signal would be applied and the counter would return to zero. To test the 10-bit counter rollover, we forced the registers to be 3 away from the max value and observed that the counter started counting over again after overflowing.

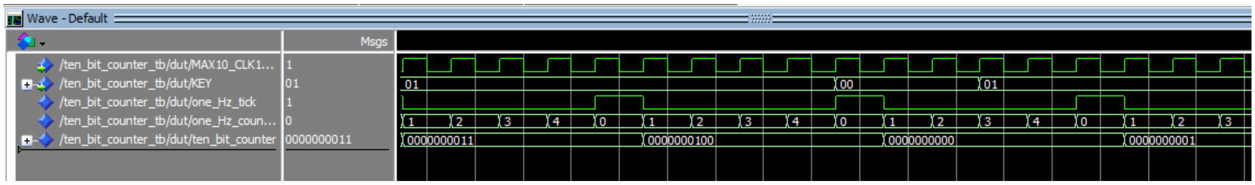
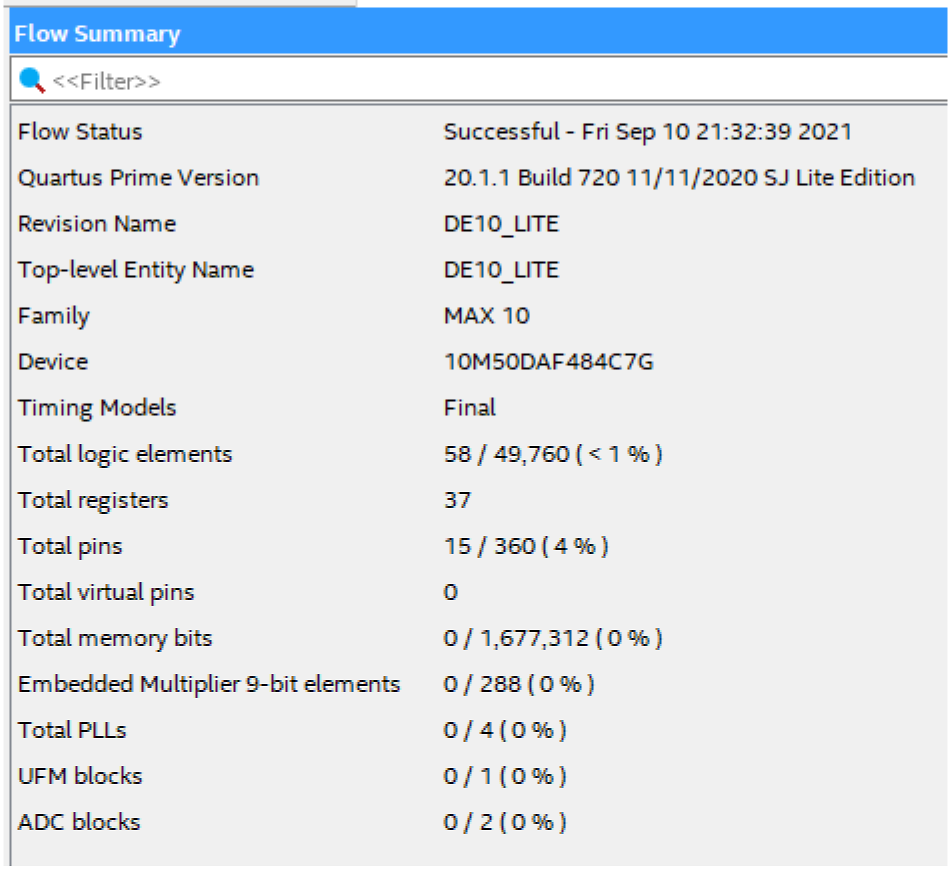

Wave - Default
Msgs
/ten_bit_counter_tb/dut/MAX10_CLK1... 1
/ten_bit_counter_tb/dut/KEY 01
/ten_bit_counter_tb/dut/one_Hz_tick 1
/ten_bit_counter_tb/dut/one_Hz_coun... 0
/ten_bit_counter_tb/dut/ten_bit_counter 0000000011
01
00
01
1 2 3 4 0 1 2 3 4 0 1 2 3 4 0 1 2 3
0000000011
0000000100
0000000000
0000000001

Figure 2. Simulation Waveform

As expected the design used 37 registers: 10 for the counter, 26 for the clock counter (as 26 bits are needed to represent 50 million), and 1 register for the 1 HZ tick signal. Just as the simulation had shown, the design worked as expected on the actual board.

We even waited 17 minutes to ensure the counter would rollover correctly (did other homework while waiting).



Flow Summary

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Flow Status	Successful - Fri Sep 10 21:32:39 2021
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	DE10_LITE
Top-level Entity Name	DE10_LITE
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	58 / 49,760 (< 1 %)
Total registers	37
Total pins	15 / 360 (4 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

Figure 3. Flow Summary

There was only one problem that we encountered while working on this lab. Since we are new to VHDL, certain errors were unclear how to fix them. One of those errors was not having a definition on how to add a bit to a register. This was caused by not using the correct ieee library for unsigned numbers. After adding that, the design finally compiled for simulation and implementation onto the board. One minor hiccup was we assumed the buttons were active high (like the Basys 3 board) but turned out they were active low. This caused the counter to be stuck in reset the first time we uploaded the design to the board.

Conclusion

We gained a better understanding of VDHL, with its odd syntax and data types . More importantly we learned how to use ModelSim to simulate the design and debug any issues if necessary. We have become more familiar with the DE10-Lite board and the system building to get a basic project started. We also learned the importance of matching data types as there is no type conversion.