A 96-nA Quiescent Current LDO With Embedded BGR Using Adaptive Pole Tracking and Adaptive Transconductance Technique

B.Mythri Reddy
23ECB1A10
bm23ecb1a10@student.nitw.ac.in

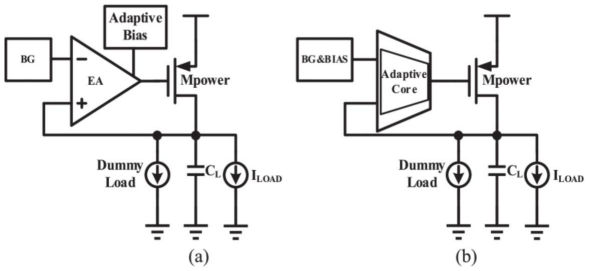
P.Satya Sree
23ECB1A11
ps23ecb1a11@student.nitw.ac.in

K.Lekhana
23ECB1A12
kl23ecb1a12@student.nitw.ac.in

***Abstract*—In this project, we design an ultra-low-power LDO (Low Dropout) voltage regulator optimized for efficient power management in modern integrated circuits. To balance performance and power consumption, the LDO smartly adapts to different load conditions. When the load current is low, only a folded cascode amplifier is used, ensuring precise output voltage while consuming minimal power. For higher load currents, an additional transconductance amplifier kicks in to handle rapid changes more effectively. The design also includes an adaptive pole tracking method, which keeps the system stable regardless of varying loads. A compact and low-power bandgap reference is built into the circuit to reduce the need for external components. The LDO was fabricated using a 0.18 µm BCD process and demonstrates excellent performance with just 12mV voltage variation during transients and a remarkably low quiescent current of 96nA, making it ideal for low-power and battery-operated systems.**

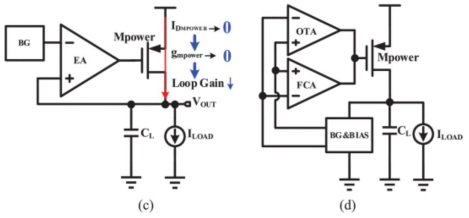
I. Introduction

There is a great demand for high-efficiency and ultra-low power management IC. Low dropout (LDO) regulators provide excellent transient response and consistent output voltage. The use of LDO in the low-power industry has promising potential.



In Fig. 1(a), adaptive biasing current technique (ABCT) reduces power consumption at light loads to achieve low quiescent current. But a trade-off between power consumption and loop stability in ABCT is challenging.

In Fig. 1(b), some circuits are turned off during light load in adaptive core technique to reduce power consumption however the adaptive core shutdown in light load leads to a decrease in loop gain, reducing the accuracy of the output voltage. Unity-gain feedback is commonly applied in most low-power LDO technologies, but there is a potential risk of breakdown during extremely light loads or no load.

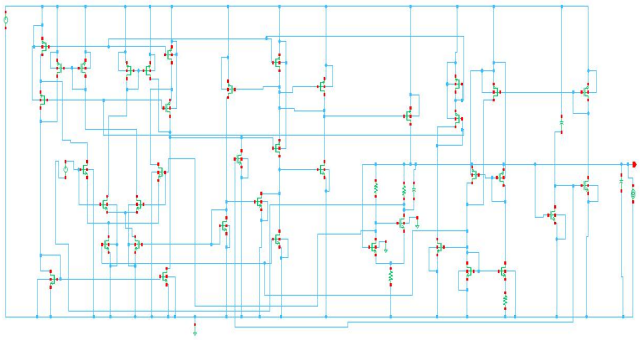


As is shown in Fig. 1(c), under extremely light load conditions, due to the absence of load current, loop gain of LDO drops sharply, leading to the failure of the LDO feedback loop. To maintain the LDO operational under light loads, a dummy load (Fig. 1(a), (b)) is added to the circuit, reducing efficiency. In reality, the leakage current of load also can alleviate this phenomenon.

To address the limitations of previous research, the adaptive transconductance technique (AGT) (Fig. 1(d)) is equipped in the proposed ultra-low-power LDO. In light current load, only the folded cascode amplifier (FCA) works to ensure high precision of output voltage. In heavy current load, the operational transconductance amplifier (OTA) and FCA work together to expand bandwidth and reduce the settling time, but the folded cascode amplifier can be ignored due to its smaller transconductance. A pole-tracking technique also be applied in AGT, which keeps the stability of the proposed LDO. To eliminate the requirement for an extra bandgap reference and dummy load in traditional low-power LDOs, a low-power bandgap reference is equipped in the proposed LDO.

II. Design of the Proposed LDO

The proposed ultra-low-power LDO is shown in Fig, which consists of error amplifier with AGT, buffer stage, power MOS, bandgap reference, and start-up circuit.

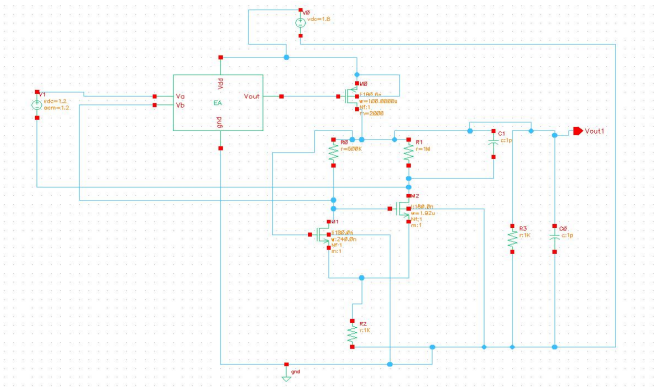


Circuit of the proposed ultra-low-power LDO.(implemented circuit)

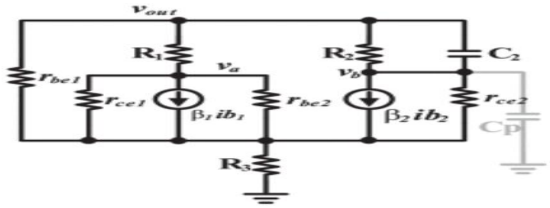
A. Low-Power Bandgap Reference Core

As is shown in Fig. 2, a low-power bandgap reference is equipped in the proposed LDO, which also acts as a dummy load to maintain the proposed LDO operational during light current load. In Fig. 3(a), the output voltage can be expressed as

$$V_{OUT} = V_{BE1} + \left(\frac{V_{BE1} - V_{BE2}}{R_1} + \frac{V_{BE1} - V_{BE2} - V_{ERR}}{R_2}\right) \cdot R_3 \qquad (1)$$



The proposed low-power bandgap reference(implemented)



(b)

Small-signal equivalent circuit with parasitic capacitance CP .

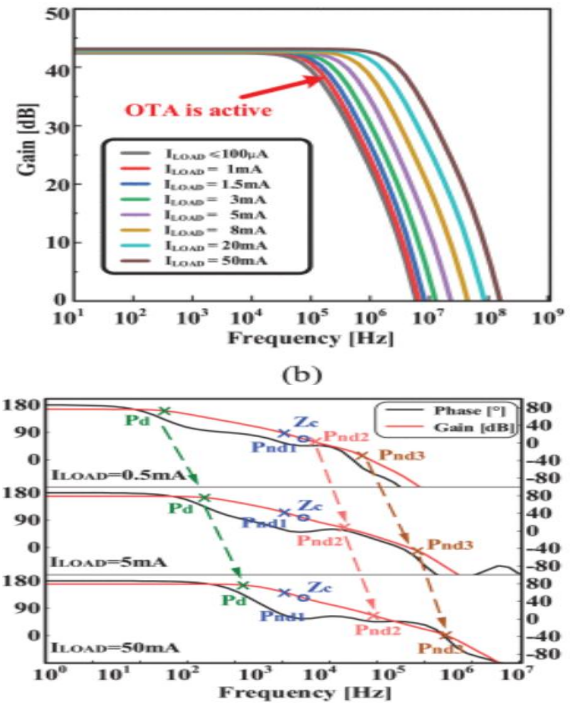
VBE1 has a negative temperature coefficient, whereas VBE1 -VBE2 has a positive temperature coefficient. By setting the ratios of resistors R1, R2, and R3, it is possible to achieve a VOUT that is independent of temperature variations. VERR is the gain error caused by the variation in loop gain of the LDO. In light load, VERR is small because of high loop gain. But with the increase of I_{LOAD}, VERR will increase which is caused by the decreasing gain of M_{POWER}. It can be concluded that

$$\Delta V_{OUT} \propto \frac{R_1}{R_2} \cdot V_{ERR}$$

As the ratio of R2/R1 increases, the impact of VERR is gradually suppressed.

The transfer function can be expressed

$$\begin{cases} T_{(s)}\left|_{\frac{V_A}{V_{OUT}}}\right. < 1 \\ T_{(s)}\left|_{\frac{V_B}{V_{OUT}}}\right. \approx \frac{1}{1+sC_P(R_2//r_{ce2})} \end{cases}$$



(b)

Expected Graphs For Gain and Phase with varying ILoad

Observably, a low-frequency pole is generated from R2 //rce2 and CP , which will destroy the stability of the proposed LDO. When the capacitor C2 is applied in the proposed bandgap reference, the new transfer function of the proposed bandgap reference is expressed as follows

$$\begin{cases} T_{(s)}\left|_{\frac{V_A}{V_{OUT}}}\right. < 1 \\ T_{(s)}\left|_{\frac{V_B}{V_{OUT}}}\right. \approx \frac{1+sC_2(R_2//r_{ce2})}{1+s(C_P+C_2)(R_2//r_{ce2})} \end{cases}$$

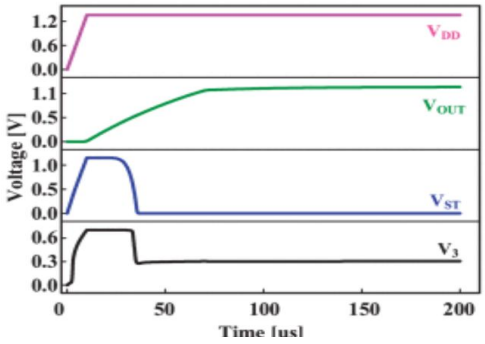
The capacitor C2 brings a zero and the location of the pole is changed. Therefore, the negative effects of the pole are canceled out by zero. C2 is typically in the pF, because large C2 will impede the response speed of node VB .

B. Error Amplifier With AGT and Adaptive Pole Tracking

In the proposed ultra-low-power LDO, an error amplifier (EA) with adaptive transconductance (AGT) and adaptive pole tracking is implemented to maintain both low power consumption and stability across varying load conditions.

During light load situations, the main power transistor (MPOWER) is nearly turned off, which disables M21 and places the AGT system in low-power mode. Only the folded cascode amplifier remains active to ensure precise output voltage regulation. All MOSFETs operate in the weak inversion region during this state, significantly reducing power usage. The EA's input stage consists of M1 and M2, while M10 acts as the load. M9 and M10 are deliberately sized with low W/L ratios to enhance the gain of the amplifier, given the low equivalent transconductance in this mode. As the load current increases, M21 turns on and provides additional adaptive bias current to the EA.

This activates the OTA amplifier (M3 and M4), which operate in weak inversion to ensure a linear increase in gain-bandwidth product (GBW) with the load current, while M9 and M10 remain in saturation to support stable gain. The EA's output parasitic capacitance (CEA) is made proportional to the load current, ensuring that the non-dominant pole at the EA output (Pnd2) shifts linearly with current. The overall transfer function of the LDO includes a dominant pole at the output (Pd), two other non-dominant poles (Pnd2 and Pnd3), and a zero (ZC) introduced to cancel the effects of Pnd1 from the reference circuit. To ensure stability, the sizing ratio K (between MPOWER, M19, and M21) is set to 10,000. This avoids issues like Pnd2 and Pd getting too close (which would reduce phase margin), or Pnd2 and Pnd3 becoming conjugate poles due to high buffer transconductance. This adaptive mechanism ensures that the loop remains stable, with a phase margin above 45°, even under different load conditions and process variations.



C. Start-Up Circuit

To ensure proper functioning of the LDO during power-up, a dedicated start-up circuit (comprising transistors M26 to M35) is included. When the power supply (VDD) is first applied, the output voltage (VOUT) of the LDO is initially zero. At this point, M34 is closed (conducting), and as VDD starts to rise, the voltage at node VST also increases. This turns on transistors M32 to M35, gradually increasing the voltage at node V3. As a result, M35 turns on the main power transistor (MPOWER), which allows the output voltage VOUT to begin rising. At the same time, a proportional-to-absolute-temperature (PTAT) current source made of M26 to M29 is activated, helping initiate the correct bias conditions. Once VOUT reaches a certain threshold, M31 turns on and disables the start-up circuit, ensuring it no longer consumes any additional current. This mechanism ensures smooth start-up and helps maintain ultra-low quiescent current in normal operation.

III. EXPERIMENTAL RESULTS

Fig8a shows the measured load response performance of the proposed LDO at VDD=1.8 V for a load current varying from 1 µ A to 50 mA and settling time is 30 µ s. This is because the adaptive pole-tracking technique contribute to extending the GBW and increase the current in the buffer stage, thereby improving the performance of load response.

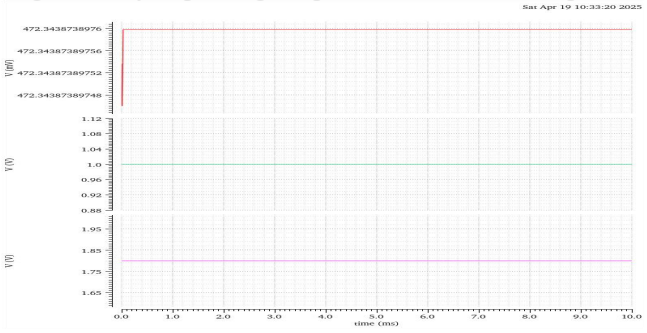


Fig8a - critical circuit startup timing diagram

the load response is measured at VDD=1 V, overshoot and undershoot voltage is approximately 20 mV. The load regulation degraded lightly because the MPOWER entered the linear region under low-dropout conditions

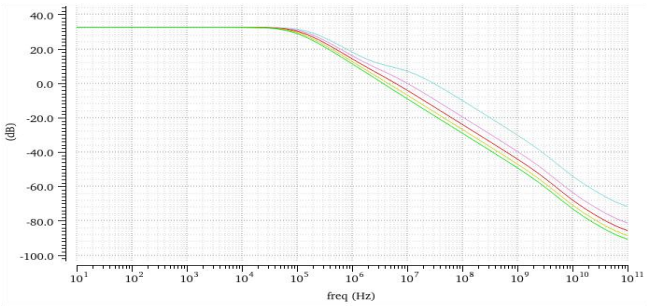


Fig.8b - Gain with varying ILoad from 1m A to 50m A

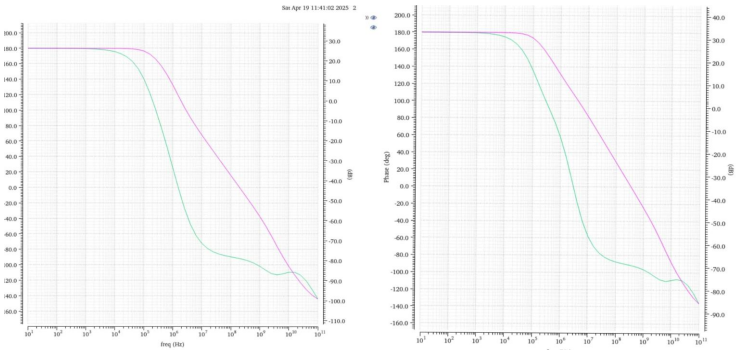


Fig.8c – phase with varying Iload for 10m A and 50m A

Fig.8d shows the measured line regulation of the proposed LDO, which is 15 mV/V at a load current of 50 mA and 2.5 mV/V at a null load current.

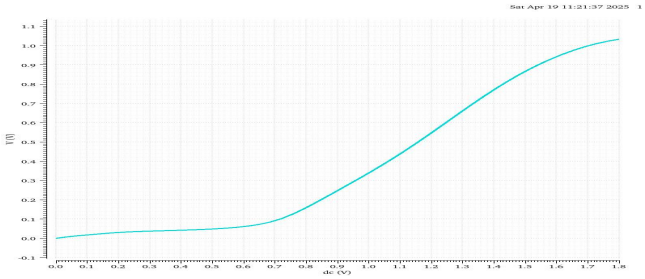


Fig8d - line regulation

IV. CONCLUSION

In this project, an ultra-low-power LDO regulator was designed using adaptive transconductance and adaptive pole-tracking techniques. The adaptive transconductance helps to significantly reduce quiescent current during light load conditions, while the adaptive pole-tracking extends the gain-bandwidth product (GBW), improving load response and stability. The proposed LDO achieves a high current efficiency of up to 99.94% across the entire load range. It operates with an ultra-low quiescent current of just 96 nA and maintains a very low overshoot voltage of 12 mV. Additionally, an integrated ultra-low-power bandgap reference is used, simplifying the external circuit requirements and making the design more practical for real-world applications.

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REFERENCES

1) *https://ieeexplore.ieee.org/document/10716787*