VSDBabySoC Project Summary

Introduction

The VSDBabySoC project focuses on building a compact, open-source System on Chip (SoC) based on the RVMYTH RISC-V core. It integrates a Phase-Locked Loop (PLL) for stable clock generation and a 10-bit Digital-to-Analog Converter (DAC) for interfacing with analog devices. This SoC, developed using Sky130 technology, provides an educational platform for learning digital-analog integration and real-world applications such as audio and video output.

What is a System on Chip (SoC)?

A System on Chip (SoC) is essentially a computer on a single chip, combining CPU, memory, I/O ports, GPU, DSP, and power management. SoCs are space-saving, energy-efficient, reliable, and cost-effective. They are widely used in smartphones, tablets, wearables, IoT devices, cars, and TVs.

Types of SoCs

- Microcontroller-based SoC: Simple, low-power, used in appliances and IoT devices. - Microprocessor-based SoC: More powerful, supports multitasking and operating systems, used in smartphones and tablets. - Application-specific SoC: Custom-designed for specialized tasks like graphics, AI, and high-performance computing.

VSDBabySoC Architecture

The VSDBabySoC integrates three main components:

1. RVMYTH CPU: A RISC-V-based open-source processor handling instruction execution and data processing.

2. Phase-Locked Loop (PLL): Generates a synchronized and stable clock signal for system coordination.

3. 3. Digital-to-Analog Converter (DAC): Converts digital values into analog signals for interfacing with external devices.

Component Details

- RVMYTH CPU: Handles processing using register r17 for sequential data updates. - PLL: Ensures timing synchronization, reduces jitter, and maintains clock accuracy despite external variations. - DAC: A 10-bit DAC converts digital data to analog signals, enabling

outputs like audio and video.

PLL Insights

A Phase-Locked Loop (PLL) consists of a Phase Detector, Loop Filter, and Voltage-Controlled Oscillator (VCO). It synchronizes the output signal with the input reference. On-chip PLLs overcome limitations of off-chip clocks, such as jitter, distribution delays, and frequency instability.

The Role of Functional Modelling Before RTL and Physical Design

Functional modelling captures system behavior without hardware details, ensuring interactions (CPU, PLL, DAC) work correctly before RTL or physical design. It helps validate specifications early, avoid costly errors, and provides a clear reference for RTL implementation. BabySoC demonstrates this by verifying its processor, clock, and DAC at a high level before moving to Verilog and Sky130 design.

Why BabySoC is a Simplified Model for Learning SoC Concepts

BabySoC uses only three key blocks: **RVMYTH (RISC-V CPU), PLL, and 10-bit DAC**. By avoiding the complexity of full-scale SoCs, it highlights core concepts: CPU instruction execution, clock synchronization, and digital-to-analog interfacing. Its open-source and well-documented nature makes it an ideal educational platform.

Conclusion

VSDBabySoC demonstrates the integration of digital (CPU) and analog (DAC) systems within a single SoC. It is an educational, open-source platform enabling learners to explore RISC-V architecture, clock synchronization using PLL, and digital-to-analog conversion. This compact design provides a practical foundation for understanding modern embedded systems.