Ignoring empty loop time

CPU Core Frequency (assume boost)	Cortex A72 1.80 GHz			Neoverse N1 3.00 GHz			Neoverse V1 2.60 GHz		Neoverse V2 3.45 GHz			Apple M1 3.20 GHz		
Mean instruction time	ns	inst/cycle	ref V1	ns	inst/cycle	ref V1	ns	inst/cycle	ns	inst/cycle	ref V1	ns	inst/cycle	ref V1
NOP	0.560	0.992	+977%	0.092	3.623	+195%	0.036	10.684	0.029	10.004	+7%	0.045	6.944	+54%
ADD	0.297	1.871	+108%	0.115	2.899	+34%	0.099	3.885	0.080	3.626	+7%	0.070	4.464	-13%
ADC	0.297	1.871	+108%	0.115	2.899	+34%	0.099	3.885	0.083	3.495	+11%	0.108	2.894	+34%
ADDS	0.315	1.764	+66%	0.120	2.778	+6%	0.131	2.936	0.124	2.340	+25%	0.107	2.921	+1%
ADCS	0.559	0.994	-0%	0.334	0.998	-1%	0.388	0.991	0.309	0.939	+6%	0.313	0.998	-1%
MUL	1.677	0.331	+502%	1.002	0.333	+499%	0.193	1.993	0.152	1.909	+4%	0.156	2.003	-1%
UMULH	2.236	0.248	+702%	1.336	0.250	+699%	0.193	1.993	0.152	1.909	+4%	0.156	2.003	-1%
DIV	3.353	0.166	+0%	2.005	0.166	+0%	2.311	0.166	1.824	0.159	+5%	0.625	0.500	-67%
MUL UMULH	1.957	0.284	+602%	1.169	0.285	+599%	0.193	1.993	0.152	1.909	+4%	0.156	2.003	-1%
MUL ADCS UMULH ADCS	0.978	0.568	+130%	0.584	0.571	+129%	0.294	1.308	0.238	1.219	+7%	0.157	1.990	-34%
MUL ADD	0.839	0.662	+453%	0.501	0.665	+451%	0.105	3.663	0.095	3.054	+20%	0.104	3.005	+22%
MUL ADC	0.838	0.663	+453%	0.501	0.665	+451%	0.105	3.663	0.102	2.844	+29%	0.105	2.976	+23%
MUL ADDS	0.838	0.663	+463%	0.501	0.665	+461%	0.103	3.734	0.099	2.930	+27%	0.104	3.005	+24%
MUL ADCS	0.839	0.662	+196%	0.501	0.665	+195%	0.196	1.962	0.188	1.543	+27%	0.156	2.003	-2%
MUL ADCS (alt)	0.838	0.663	+198%	0.501	0.665	+196%	0.195	1.972	0.156	1.860	+6%	0.156	2.003	-2%
UMULH ADD	1.118	0.497	+491%	0.668	0.499	+488%	0.131	2.936	0.106	2.737	+7%	0.105	2.976	-1%
UMULH ADC	1.118	0.497	+491%	0.668	0.499	+488%	0.131	2.936	0.113	2.567	+14%	0.105	2.976	-1%
UMULH ADDS	1.118	0.497	+430%	0.668	0.499	+428%	0.146	2.634	0.119	2.438	+8%	0.104	3.005	-12%
UMULH ADCS	1.118	0.497	+128%	0.668	0.499	+127%	0.340	1.131	0.270	1.074	+5%	0.156	2.003	-44%
UMULH ADCS (alt)	1.119	0.496	+129%	0.668	0.499	+127%	0.339	1.135	0.268	1.082	+5%	0.156	2.003	-43%
UMULH NOP ADCS	0.746	0.745	+131%	0.445	0.749	+129%	0.224	1.717	0.179	1.621	+6%	0.105	2.976	-42%
UMULH ADD ADCS	0.745	0.746	+146%	0.445	0.749	+145%	0.210	1.832	0.179	1.621	+13%	0.105	2.976	-38%
UMULH ADDS ADCS	0.745	0.746	+258%	0.445	0.749	+257%	0.144	2.671	0.129	2.249	+19%	0.117	2.671	+0%
UMULH ADCS ADCS	0.745	0.746	+43%	0.445	0.749	+42%	0.361	1.065	0.289	1.004	+6%	0.210	1.488	-28%
UMULH ADC ADDS	0.745	0.746	+356%	0.445	0.749	+354%	0.113	3.404	0.101	2.872	+18%	0.098	3.189	+7%
UMULH ADC ADDS (dep. regs)	0.745	0.746	+53%	0.445	0.749	+52%	0.337	1.141	0.256	1.133	+1%	0.210	1.488	-23%
MUL ADD UMULH ADD	0.978	0.568	+450%	0.584	0.571	+448%	0.123	3.127	0.106	2.737	+14%	0.104	3.005	+4%
PACIA							0.385	0.999				0.313	0.998	+0%
AUTIA							0.385	0.999				0.313	0.998	+0%
PACIA AUTIA							0.385	0.999				0.313	0.998	+0%
PACIA … AUTIA …							0.385	0.999				0.314	0.995	+0%

	Cortex A72	Neoverse N1	Neoverse V1	Neoverse V2	Apple M1
UMULH vs. MUL	+33.3%	+33.3%	+0.0%	+0.0%	+0.0%
UMULH ADCS vs. MUL ADCS	+33.3%	+33.3%	+73.5%	+43.6%	+0.0%

ref V1 = comparison of execution time with Neoverse V1, frequency ratio included