Digital System Design using VHDL

Final Exam-Group 3

Computer Engineering department, Iran University of Science and Technology

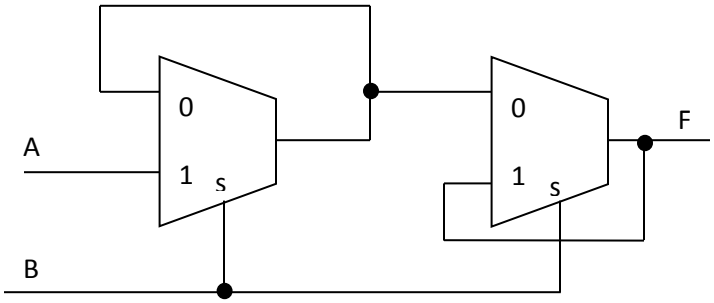
Time: 100 Minutes, Winter 2022

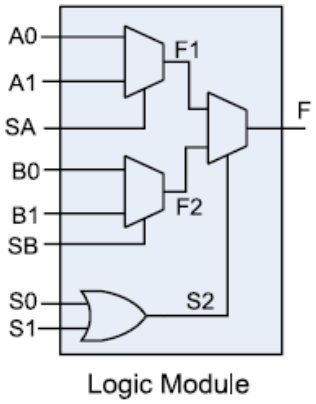
Q1. Using VHDL design a FSM that receives an n bit sequence serially and determine whether the sequence is symmetric or not. A symmetric sequence is a sequence that has the same from either is read from LSB to MSB or from MSB to LSB

11100111 is a symmetric sequence

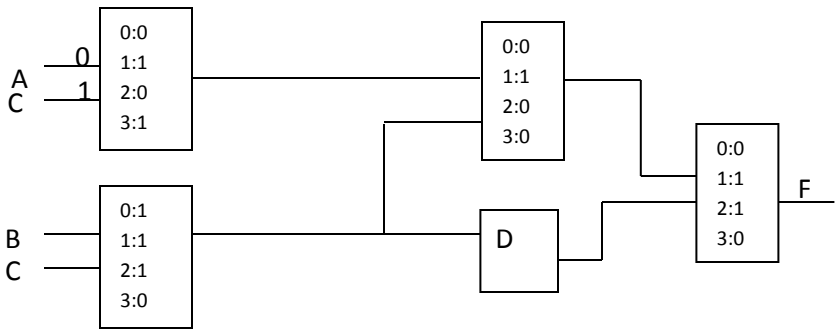
10100111 is not symmetric

Q2. Actel FPGAs are based on MUX-based units such as ACT1 module. Implement the following circuit with minimum number of Act1 module. What does the circuit do?



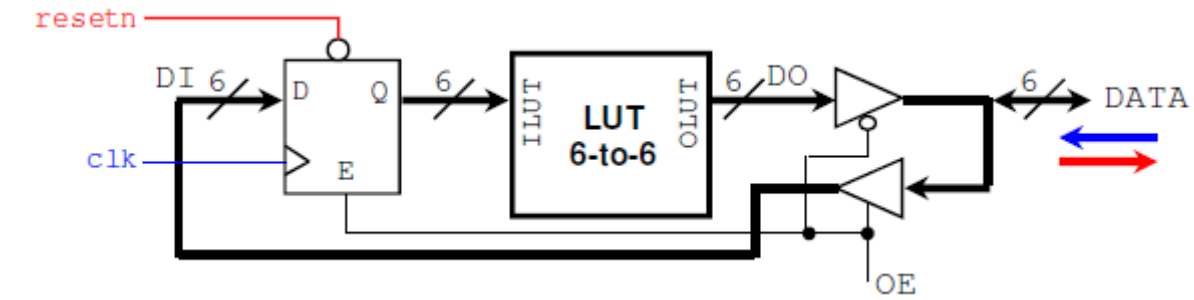


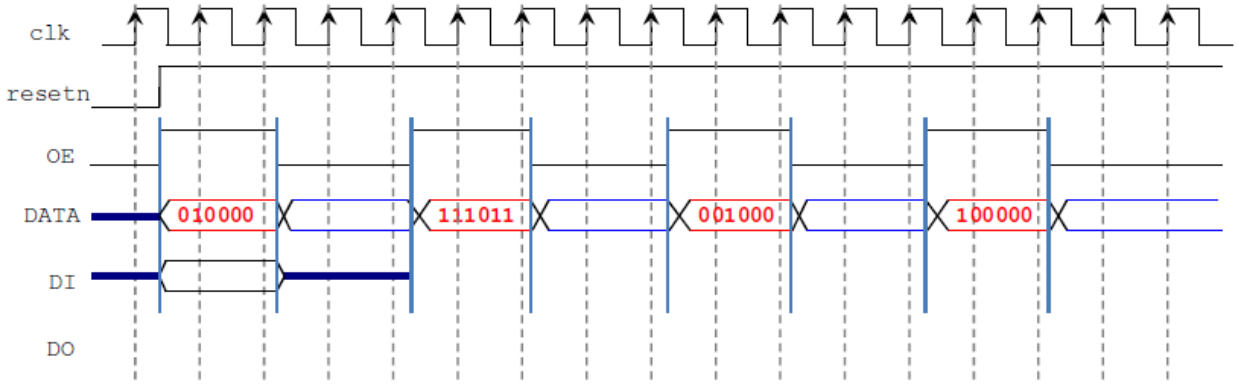
Q3. Implement the following circuit with minimum number of LUT-3s



Q4. Given the following system, The LUT-6 implements the following function: OLUT = ⌈sqrt(ILUT)⌉

A) complete the Timing Diagram.





B) Re-implement the circuit using LUT-3s