Digital System Design using VHDL

Final Exam-Group 2

Computer Engineering department, Iran University of Science and Technology

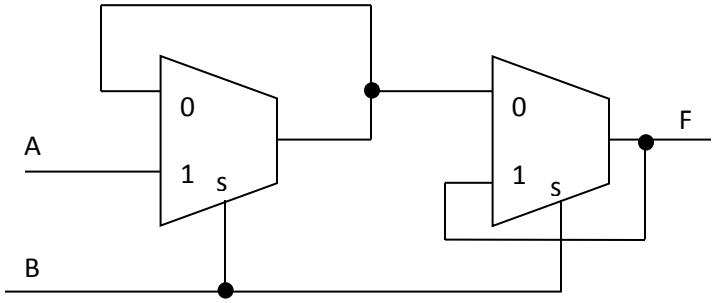
Time: 100 Minutes, Winter 2022

Q1. Using VHDL design a FSM that receives a 64 bits data and returns the maximum distance between two internal ones. See the example

10011101**1000001**10011101111001

You should return 5 because 5 zeros is the longest distance between two internal ones. Only FSM is accepted.

Q2. Implement the following circuit with minimum number of OLMC macrocell module. What does the circuit do?



Q3. Design the following circuits

A) Using minimum number of LUT-6s and three MUX2-1 implement an LUT-8 (No other hardware modules are allowed)
B) Implement a function with 5 variables using minimum number of LUT-3s (no other hardware modules are allowed).

Q4. Implement the following circuit

A) suppose you have LUT-3s

B) Suppose you have LUT-2s

C) suppose you have LUT-4s