Digital System Design using VHDL

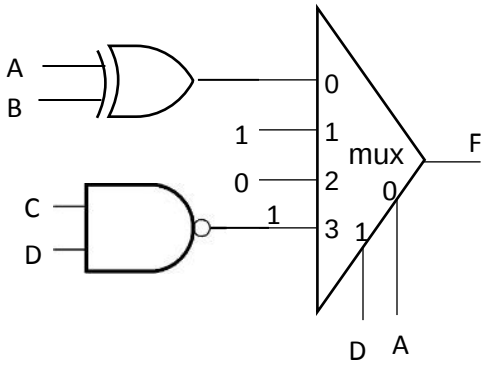
Final Exam-Group 4

Computer Engineering department, Iran University of Science and Technology

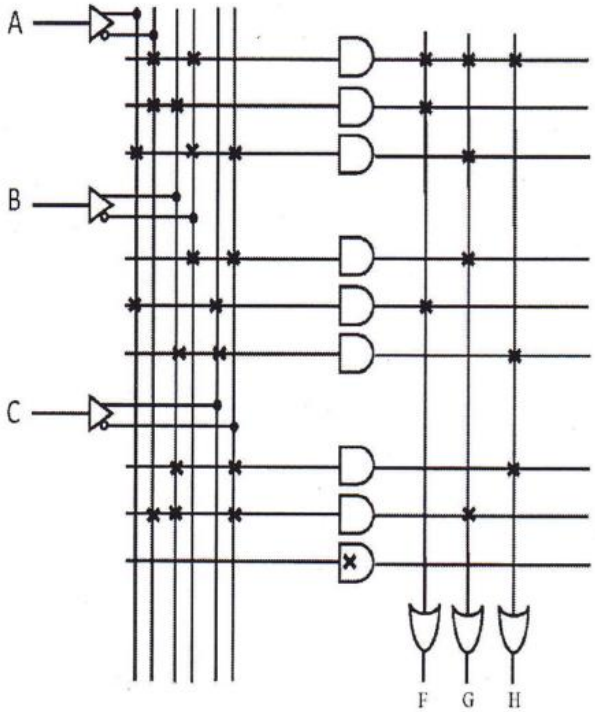
Time: 100 Minutes, Winter 2022

Q1. Using VHDL design a FSM that receive two separate sequence of bits (A and B) serially. The FSM machine each clock cycle randomly read from one of the sequences (perhaps two times read from sequence A). The output Z becomes one when you detect 01 in sequence A and then 10 in sequence B.

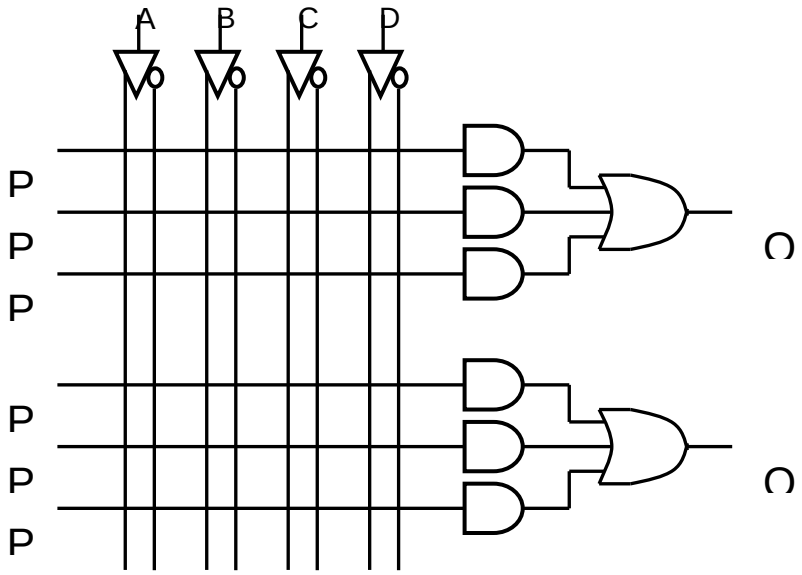
Q2. Implement the following circuit using LUT-3s.



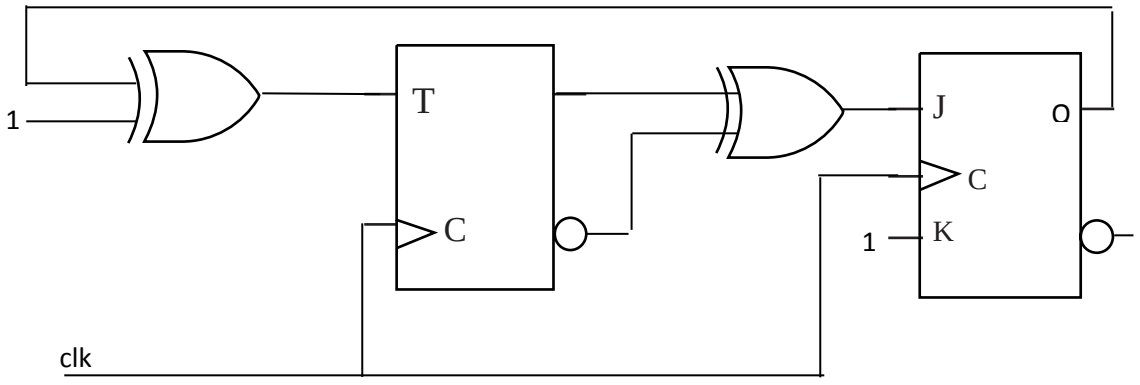
Q3. Consider the function of following PLA

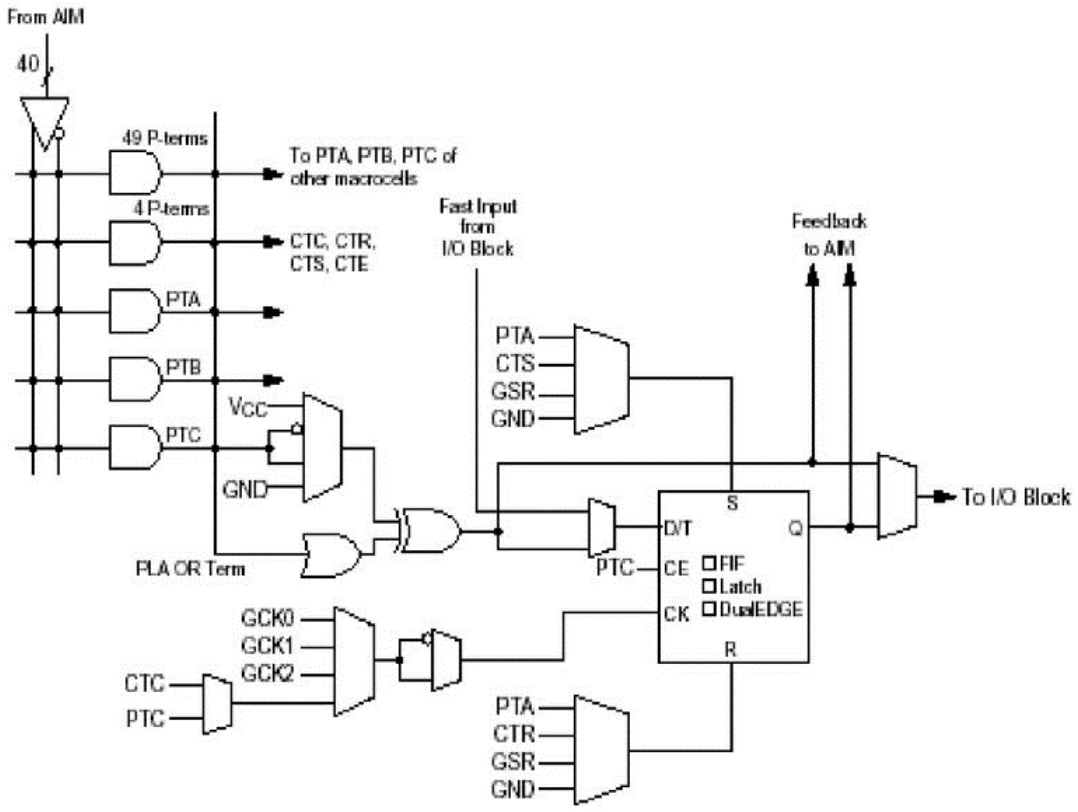


Convert it to the following PAL device. You can add another output to the following PAL device



Q4. Implement the following circuit using minimum number of Cool-Runner II macrocell.




From AIM
40
49 P-terms
To PTA, PTB, PTC of other macrocells
4 P-terms
CTC, CTR, CTS, CTE
PTA
PTB
PTC
Vcc
GND
PLA OR Term
Fast Input from I/O Block
PTA
CTS
GSR
GND
Feedback to AIM
To I/O Block
S
D/T
Q
CE
FF
Latch
DualEDGE
CK
R
PTC
GCK0
GCK1
GCK2
CTC
PTC
PTA
CTR
GSR
GND