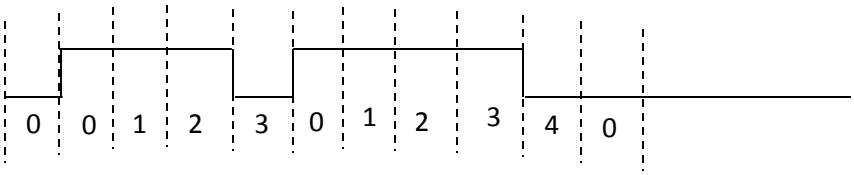
Digital System Design using VHDL

Final Exam-Group 1

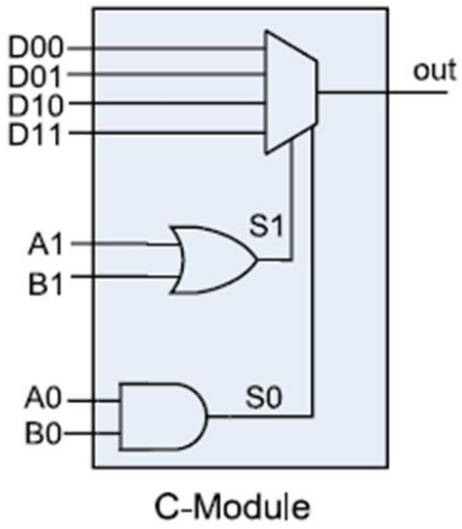
Computer Engineering department, Iran University of Science and Technology

Time: 100 Minutes, Winter 2022

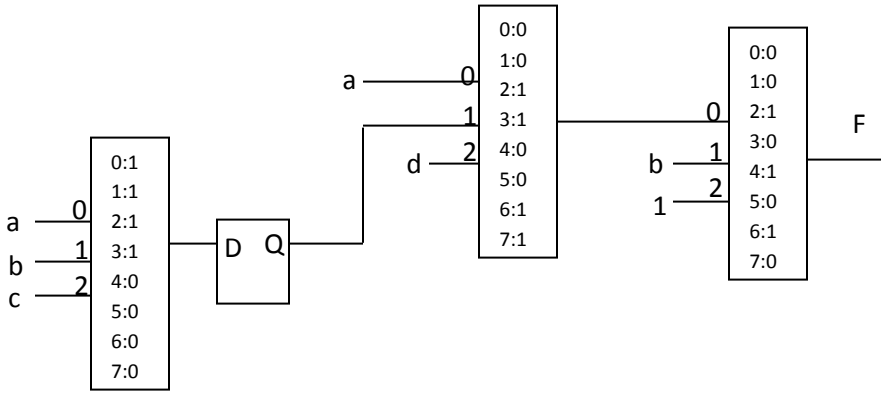
Q1. Using VHDL design a FSM that receives one bit input at each clock cycle. It should generates an output that shows number of subsequent ones in the input. The output should be behind the input for exactly one clock cycle. one sample of the circuit is shown below.

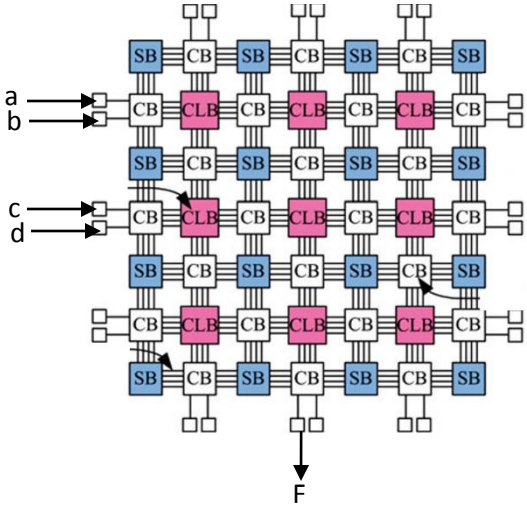


Q2. Actel FPGAs are based on mux-based modules such as C-module as shown below. Implement a T flip-flop with minimum number of C-modules



Q3. Implement the following circuit with 2-LUTs. The architecture of the FPGA is shown below.





Q4. Implement the following circuit using minimum number of LUT-4s. suppose a,b,c are **2 bits**.

```
[1] process (clk, a, b, c) begin
[2] x <= a + b;
[3] if rising_edge(clk) then
[4] if a = c then
[5] y <= b + c; z <= c;
[6] elsif b > c then
[7] y <= a - x;
[8] end if; end if; end process;
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