دانشکده کامپیوتر

آزمایشگاه معماری کامپیوتر
آزمایش دوم

دکتر محبتی

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اسفند ۱۴۰۰

هدف آزمایش:

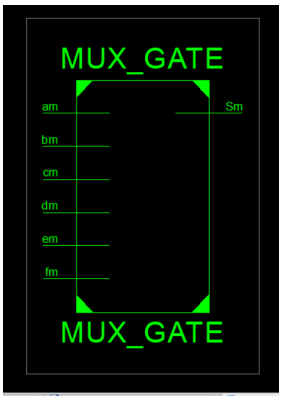
در این آزمایش با مدارهای دیکودر، انکودر، مالتی پلکسر و سون سگمنت آشنا می‌شویم و به طراحی آن‌ها با زبان vhdl در نرم افزار ISE می‌پردازیم. کاربرد سون سگمنت در مدارهای جمع کننده، تفریق کننده و ... برای نمایش خروجی می‌باشد.

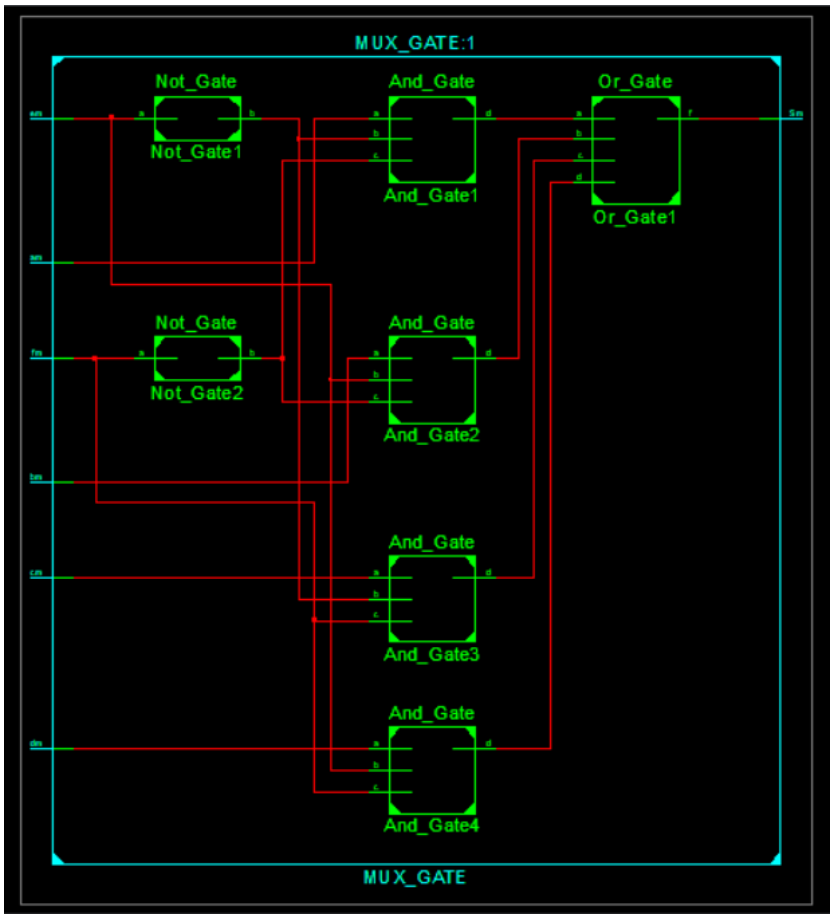
در آزمایش دوم ابتدا گیت MUX۲TO۱ را پیاده سازی کردیم. سپس با استفاده از آن گیت MUX۴TO۱ را ساختیم که کد آن به شکل زیر می باشد.

```
32  entity MUX_GATE is
33      Port ( am : in  STD_LOGIC;
34             bm : in  STD_LOGIC;
35             cm : in  STD_LOGIC;
36             dm : in  STD_LOGIC;
37             em : in  STD_LOGIC;
38             fm : in  STD_LOGIC;
39             Sm : out  STD_LOGIC);
40  end MUX_GATE;
41
42  architecture Behavioral of MUX_GATE is
43
44  Component And_Gate is
45      Port ( a : in  STD_LOGIC;
46             b : in  STD_LOGIC;
47             c : in  STD_LOGIC;
48             d : out  STD_LOGIC);
49  End Component And_Gate;
50
51  Component Or_Gate is
52      Port ( a : in  STD_LOGIC;
53             b : in  STD_LOGIC;
54             c : in  STD_LOGIC;
55             d : in  STD_LOGIC;
56             f : out  STD_LOGIC);
57  End Component Or_Gate;
58
59  Component Not_Gate is
60      Port ( a : in  STD_LOGIC;
61             b : out  STD_LOGIC);
62  End Component Not_Gate;
63  Signal X, Y, Z1, Z2, Z3, Z4 : STD_LOGIC;
64  begin
```

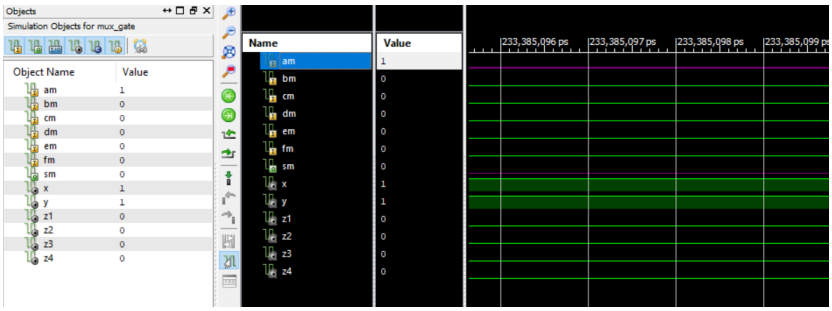
```
64  begin
65
66  Not_Gate1 : Not_Gate port map(a => em, b => X);
67  Not_Gate2 : Not_Gate port map(a => fm, b => Y);
68  And_Gate1 : And_Gate port map(a => am, b => X, c => Y, d => Z1);
69  And_Gate2 : And_Gate port map(a => bm, b => em, c => Y, d => Z2);
70  And_Gate3 : And_Gate port map(a => cm, b => X, c => fm, d => Z3);
71  And_Gate4 : And_Gate port map(a => dm, b => em, c => fm, d => Z4);
72  Or_Gate1 : Or_Gate port map (a => Z1, b => Z2, c => Z3, d => Z4, f=> Sm);
73  end Behavioral;
74
```

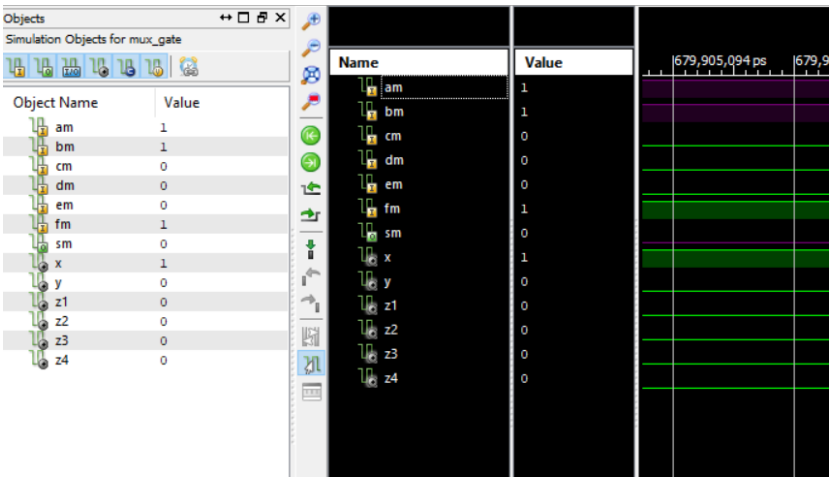
نمای داخلی گیت MUX۴TO۱ :

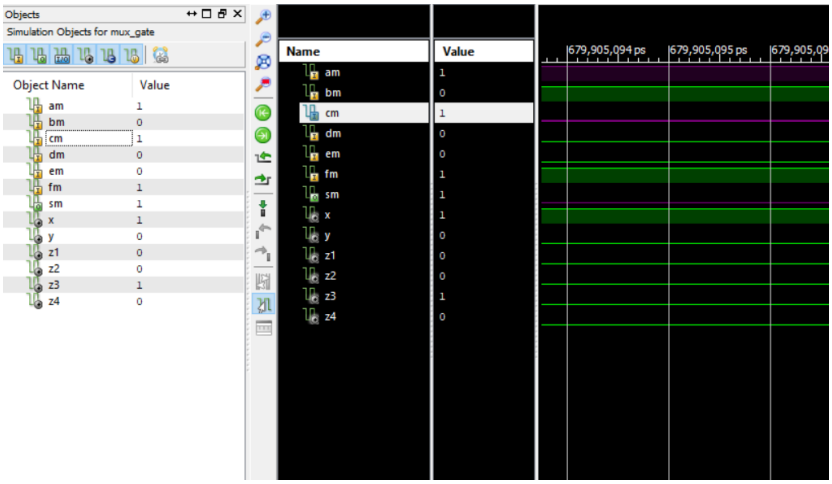




تست‌ها:


Objects
Simulation Objects for mux_gate
Object Name
Value
Name
Value
233,385,096 ps
233,385,097 ps
233,385,098 ps
233,385,099 ps
am 1
bm 0
cm 0
dm 0
em 0
fm 0
sm 0
x 1
y 1
z1 0
z2 0
z3 0
z4 0

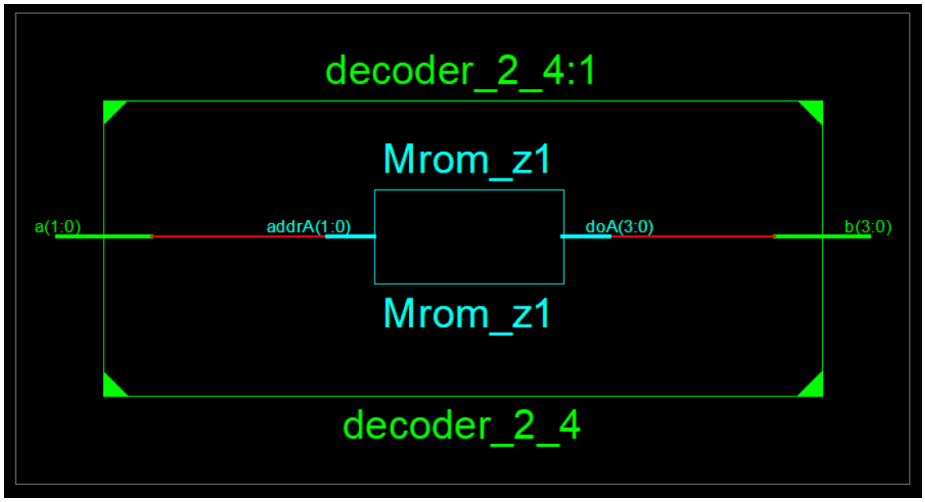

Objects
Simulation Objects for mux_gate
Object Name
Value
Name
Value
679,905,094 ps
am 1
bm 1
cm 0
dm 0
em 0
fm 1
sm 0
x 1
y 0
z1 0
z2 0
z3 0
z4 0


Objects
Simulation Objects for mux_gate
Object Name
Value
Name
Value
679,905,094 ps
679,905,095 ps
am 1
bm 0
cm 1
dm 0
em 0
fm 1
sm 1
x 1
y 0
z1 0
z2 0
z3 1
z4 0

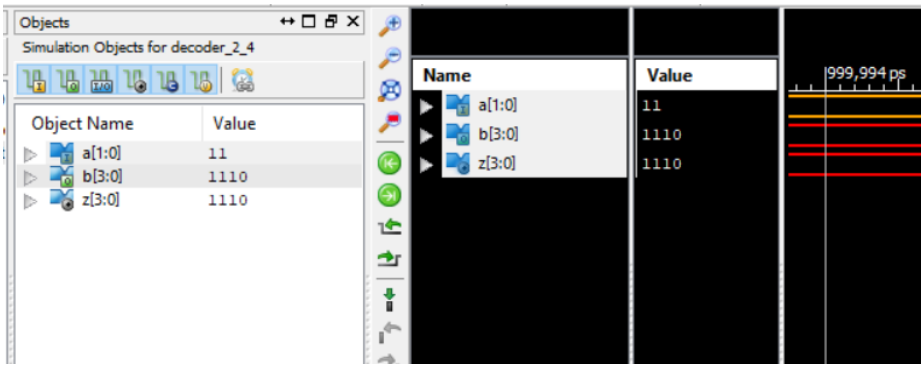
در این قسمت DECODER۲TO۴ پیاده سازی شده است که کدهای آن به شرح زیر می‌باشد.

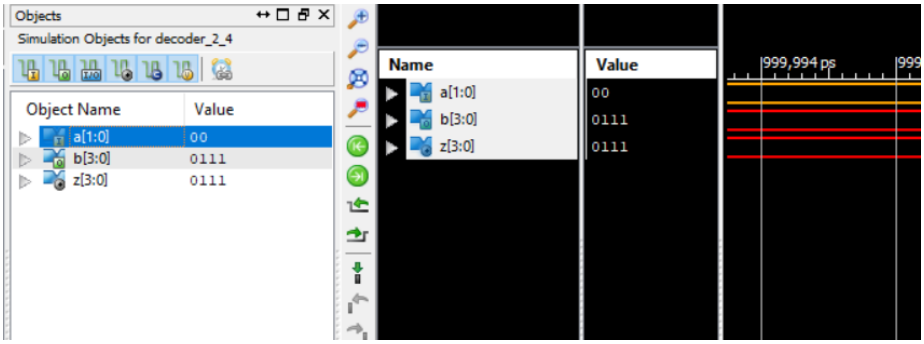
```
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22
23  -- Uncomment the following library declaration if using
24  -- arithmetic functions with Signed or Unsigned values
25  --use IEEE.NUMERIC_STD.ALL;
26
27  -- Uncomment the following library declaration if instantiating
28  -- any Xilinx primitives in this code.
29  --library UNISIM;
30  --use UNISIM.VComponents.all;
31
32  entity decoder_2_4 is
33      Port ( a : in  STD_LOGIC_VECTOR(1 downto 0);
34             b : out  STD_LOGIC_VECTOR(3 downto 0));
35  end decoder_2_4;
36
37  architecture Behavioral of decoder_2_4 is
38  signal z : STD_LOGIC_VECTOR(3 downto 0);
39  begin
40
41  z <= "0111" when a="00" else
42       "1011" when a="01" else
43       "1101" when a="10" else
44       "1110" when a="11" else
45       "XXXX";
46
47  b<=z;
48
49  end Behavioral;
50
```

نمای داخلی گیت :DECODER۲TO۴



تست‌ها:

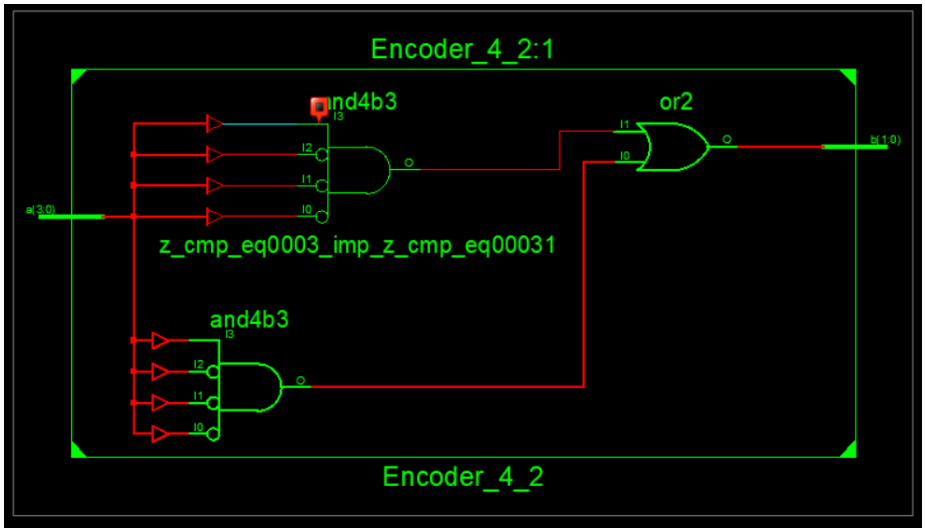

Objects
Simulation Objects for decoder_2_4
Object Name
Value
a[1:0]
11
b[3:0]
1110
z[3:0]
1110
Name
Value
a[1:0]
11
b[3:0]
1110
z[3:0]
1110
999,994 ps


Objects
Simulation Objects for decoder_2_4
Object Name
Value
a[1:0]
00
b[3:0]
0111
z[3:0]
0111
Name
Value
a[1:0]
00
b[3:0]
0111
z[3:0]
0111
999,994 ps

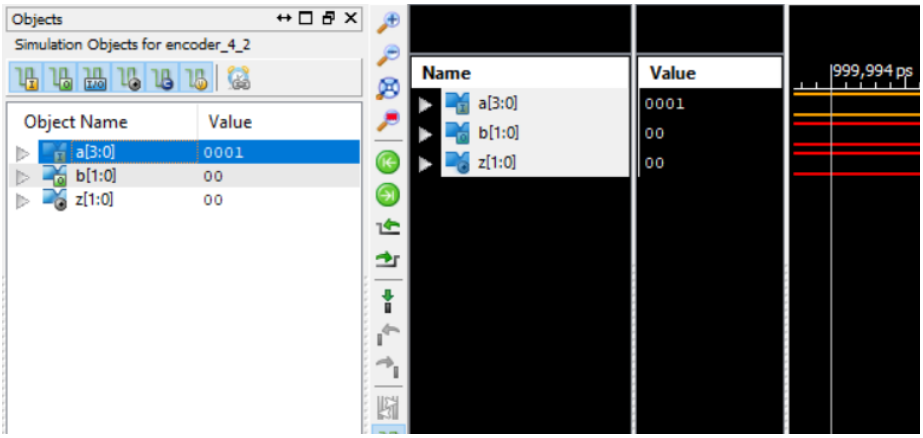
در این قسمت ENCODER۴TO۲ پیاده سازی شده است که کدهای آن به شرح زیر می‌باشد.

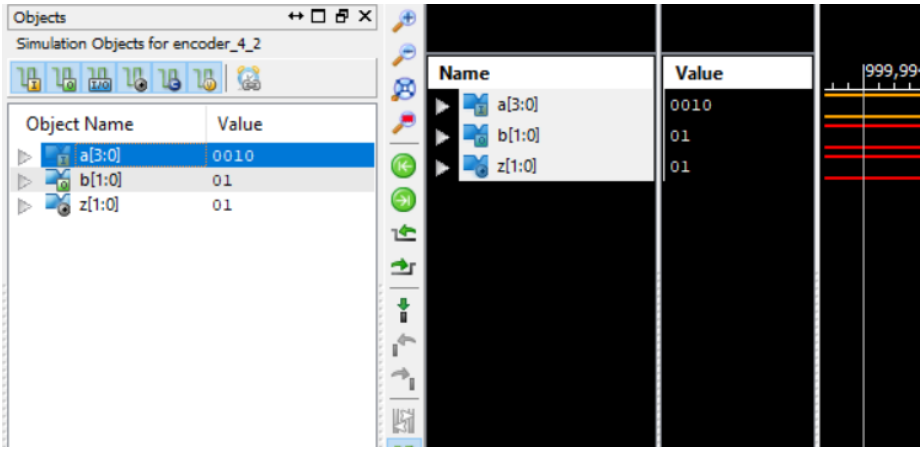
```
----------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Encoder_4_2 is
    Port ( a : in  STD_LOGIC_VECTOR(3 downto 0);
           b : out  STD_LOGIC_VECTOR(1 downto 0));
end Encoder_4_2;

architecture Behavioral of Encoder_4_2 is
signal z : STD_LOGIC_VECTOR(1 downto 0);
begin
        with a select
        z <= "00" when "0001" ,
             "01" when "0010" ,
             "10" when "0100" ,
             "11" when "1000" ,
             "XX" when others;
   b <= z;

end Behavioral;

```

نمای داخلی گیت :ENCODER۴TO۲



تست‌ها:

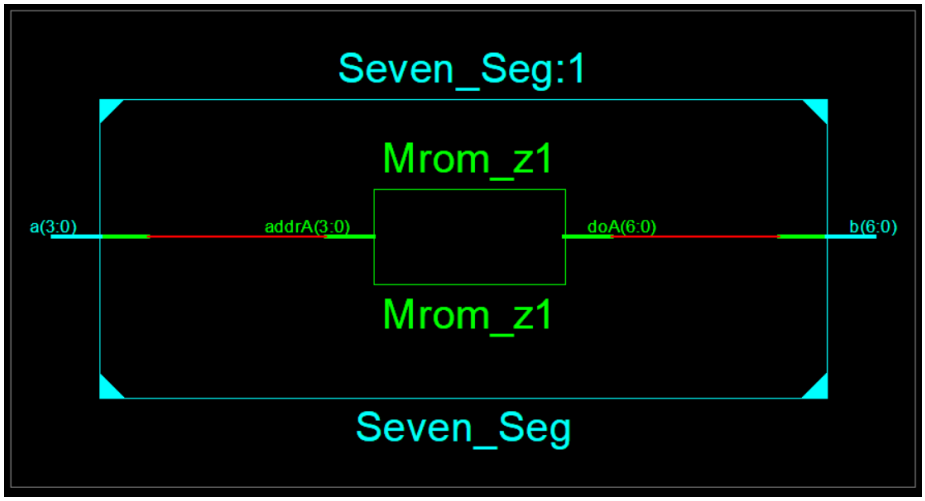

Objects
Simulation Objects for encoder_4_2
Object Name
Value
a[3:0]
0001
b[1:0]
00
z[1:0]
00
Name
Value
a[3:0]
0001
b[1:0]
00
z[1:0]
00
999,994 ps


Objects
Simulation Objects for encoder_4_2
Object Name
Value
a[3:0]
0010
b[1:0]
01
z[1:0]
01
Name
Value
a[3:0]
0010
b[1:0]
01
z[1:0]
01

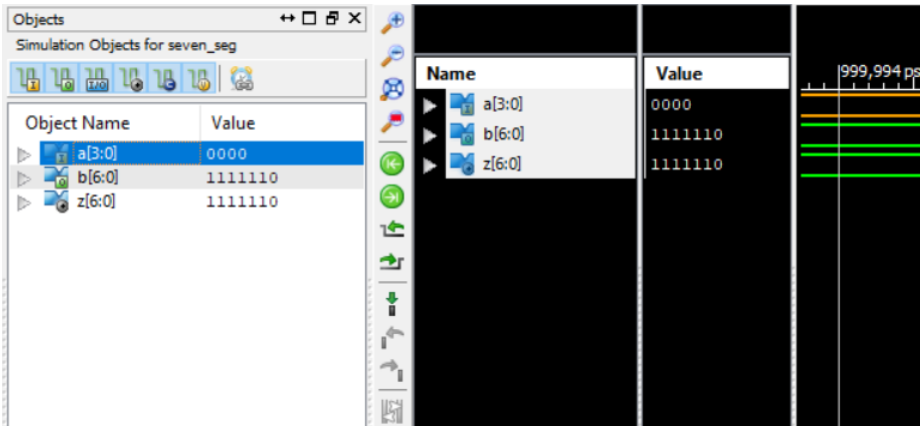
در این قسمت ۷SEGMENT پیاده سازی شده است که کدهای آن به شرح زیر می‌باشد.

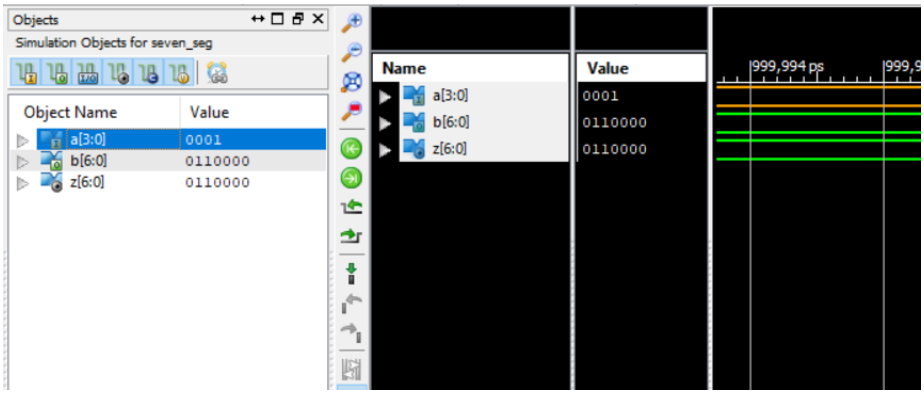
```
19  ----------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22
23  -- Uncomment the following library declaration if using
24  -- arithmetic functions with Signed or Unsigned values
25  --use IEEE.NUMERIC_STD.ALL;
26
27  -- Uncomment the following library declaration if instantiating
28  -- any Xilinx primitives in this code.
29  --library UNISIM;
30  --use UNISIM.VComponents.all;
31
32  entity Seven_Seg is
33      Port ( a : in  STD_LOGIC_VECTOR(3 downto 0);
34             b : out  STD_LOGIC_VECTOR(6 downto 0));
35  end Seven_Seg;
36
37  architecture Behavioral of Seven_Seg is
38  signal z : STD_LOGIC_VECTOR(6 downto 0);
39  begin
40     with a select
41          z <= "0110000" when "0001" ,
42               "1101101" when "0010" ,
43               "1111001" when "0011" ,
44               "0110011" when "0100" ,
45               "1011011" when "0101" ,
46               "0011111" when "0110" ,
47               "1110000" when "0111" ,
48               "1111110" when "0000" ,
49               "1111011" when "1001" ,
50               "1111111" when "1000" ,
51               "0000000" when others;
52
53  b <= z;
54
55  end Behavioral;
56
```

نمای داخلی گیت :7SEGMENT



تست‌ها:


Objects
Simulation Objects for seven_seg
Object Name
Value
a[3:0]
0000
b[6:0]
1111110
z[6:0]
1111110
Name
Value
999,994 ps


Objects
Simulation Objects for seven_seg
Object Name
Value
a[3:0]
0001
b[6:0]
0110000
z[6:0]
0110000
Name
Value
999,994 ps