HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY

LOGIC DESIGN LAB

MINI PROJECT

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Chapter 1: Introduction

I. Introduction to the topic:

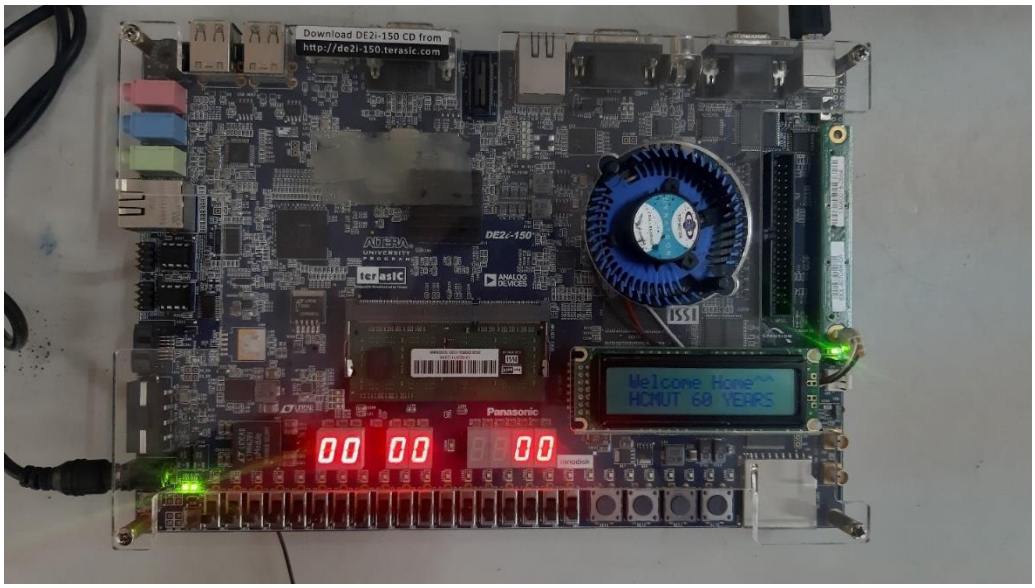
The clock is one of the most important devices in civilization. Everything we know is dependent on time, whether it be your everyday routine, TV programming or travel.

For this project our team choose to simulate a clock on the DE2i-150 board. Our goal is to get to know the function of the working digital clock, how to utilize the DE2i-150 board in order to make this project. Moreover, we get to practice our Verilog coding skill using the Quartus program.

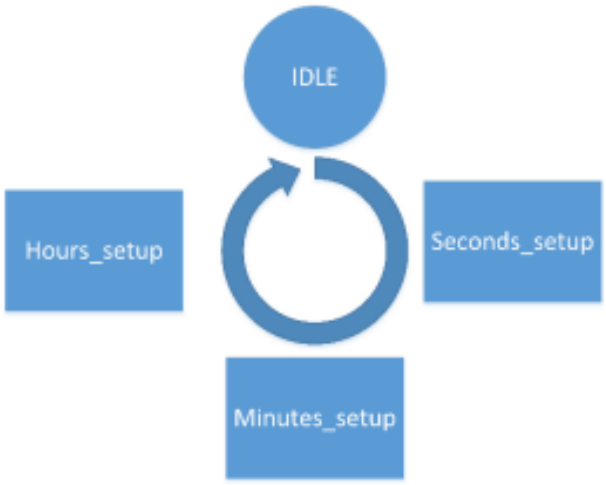
On the board there are 7 LEDs that show you the time. The HEX0 led shows the mode which show you the mode that you can change the index of time. In mode 0, it runs the time normally. In mode 1, you can change the second, in next 2 modes it will change minute and hour respectively. HEX2 and HEX3 show the second index. HEX4 and HEX5 show the minute index. HEX6 and HEX7 show the hour index. We use 3 another KEYs. The first KEY0 to change the mode that we showed. 2 others keys use to increase and decrease the index of 3 units of times. Second, minute and hour. When in mode 1 you can only change the second 2 others can not be changed.

II. Specification:

We use the DE2i-150 board for this project.



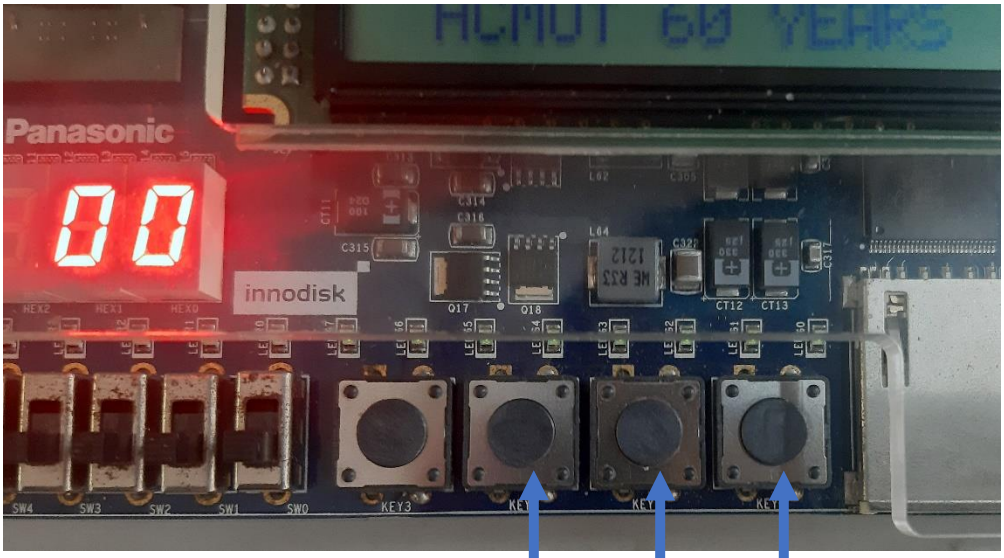
The clock has 4 states: Idle, Second setup, Minute setup, Hour setup.



Our clock will start at the Idle state which count up from 00:00:00. In order to switch between 4 states, we use the key as an input from the user to setup the value of our clock. 3 setup states contain the same feature which is increase or decrease the value of the corresponding mode.

a. Input Device:

For this project, we use the key integrated on the DE2i-150 board as the clock input for setting up the second, minute and hour value.



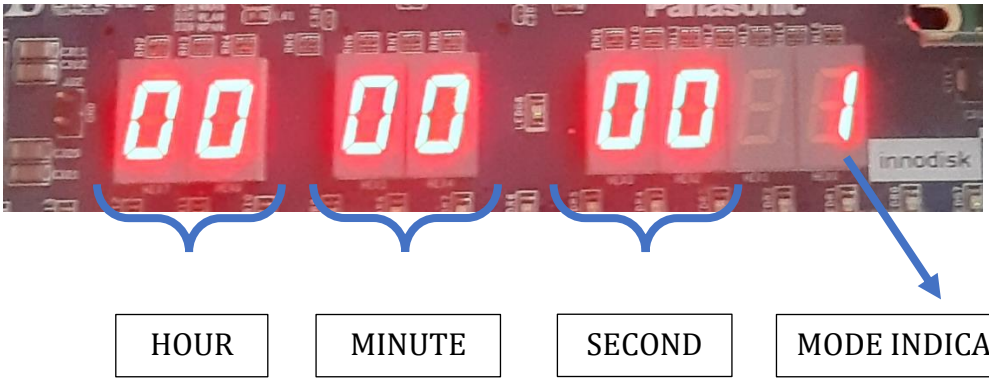
Function of the keys:

- KEY0: For switching among 4 states. Every time the key is pressed, the clock switches to the next state. When reaches the last state, it reset to the Idle state. The current state will be display on the 7 segments LED.
- KEY1: For increasing the value of the corresponding mode. Each time the key is pressed, the value is increased by 1 unit. When it reaches the maximum value (59 for second and minute, 23 for hour), it will reset back to 0.
- KEY2: For decreasing the value of the corresponding mode. Each time the key is pressed, the value is decreased by 1 unit. When it reaches 0, it will reset back to the maximum value.

b. Output device:

To display the value of the digital clock, we use seven 7 segments LED.

The function of each LED is shown in the image below.

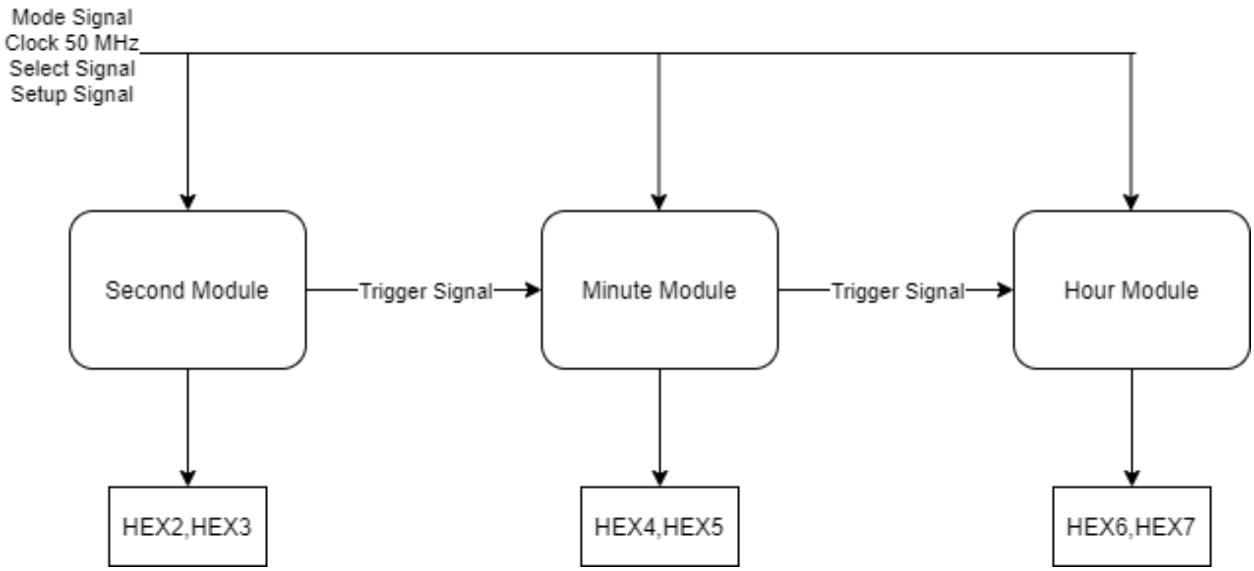


In order to use this 7 segments LED, we have to make a decoder to decode our counter value into a 7 bits signal so that it could be display on the LED. The content of the decoder will be explained later in the report.

Chapter 2: Design and Implement

I. Design Outline:

This digital clock project revolves using many modules, each has their own function, connect together. In this part, we going to explain how we designed the digital clock in the Quartus Prime software and implemented it on the DE2i-150 board.

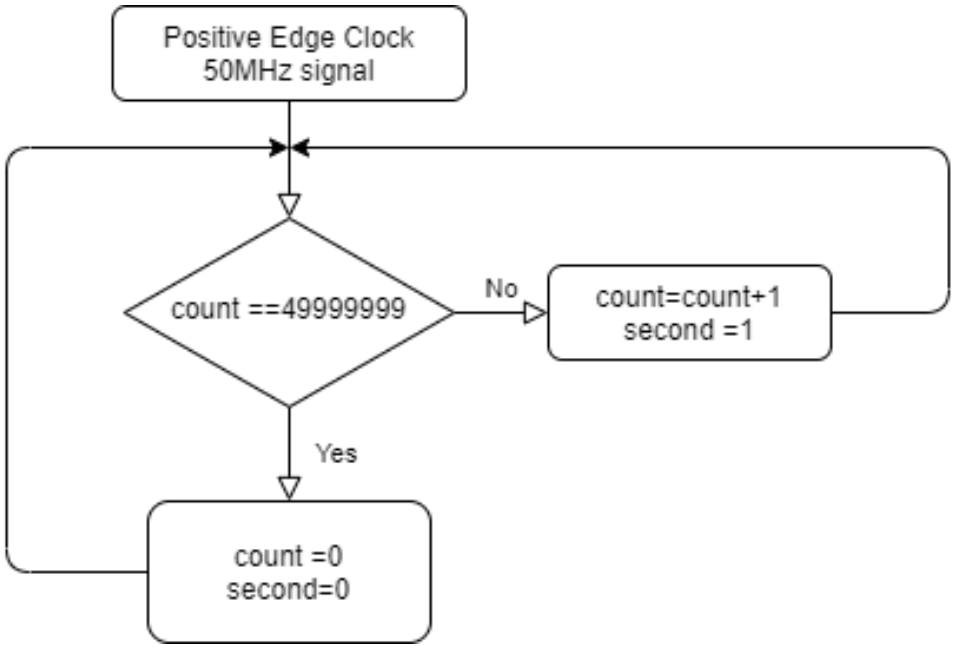


The above diagram illustrates the basic information of how our module connect together. There are 3 main modules which are the Second Module. Minute Module and Hour Module. Though each correspond to different value, but they have the same principle.

a. Second Module:

In order to make the digital clock on the DE2i-150 board, we use the clock signal 50MHz available on the board. But this signal is way too fast for us to see. To overcome this issue, we make a counter that count from 0 to 49 999 999. This value increase on the positive edge of the clock 50MHz signal. Every time the count variable reaches 49 999 999, 1 second had passed. By using this idea, we had developed a module to count the second.

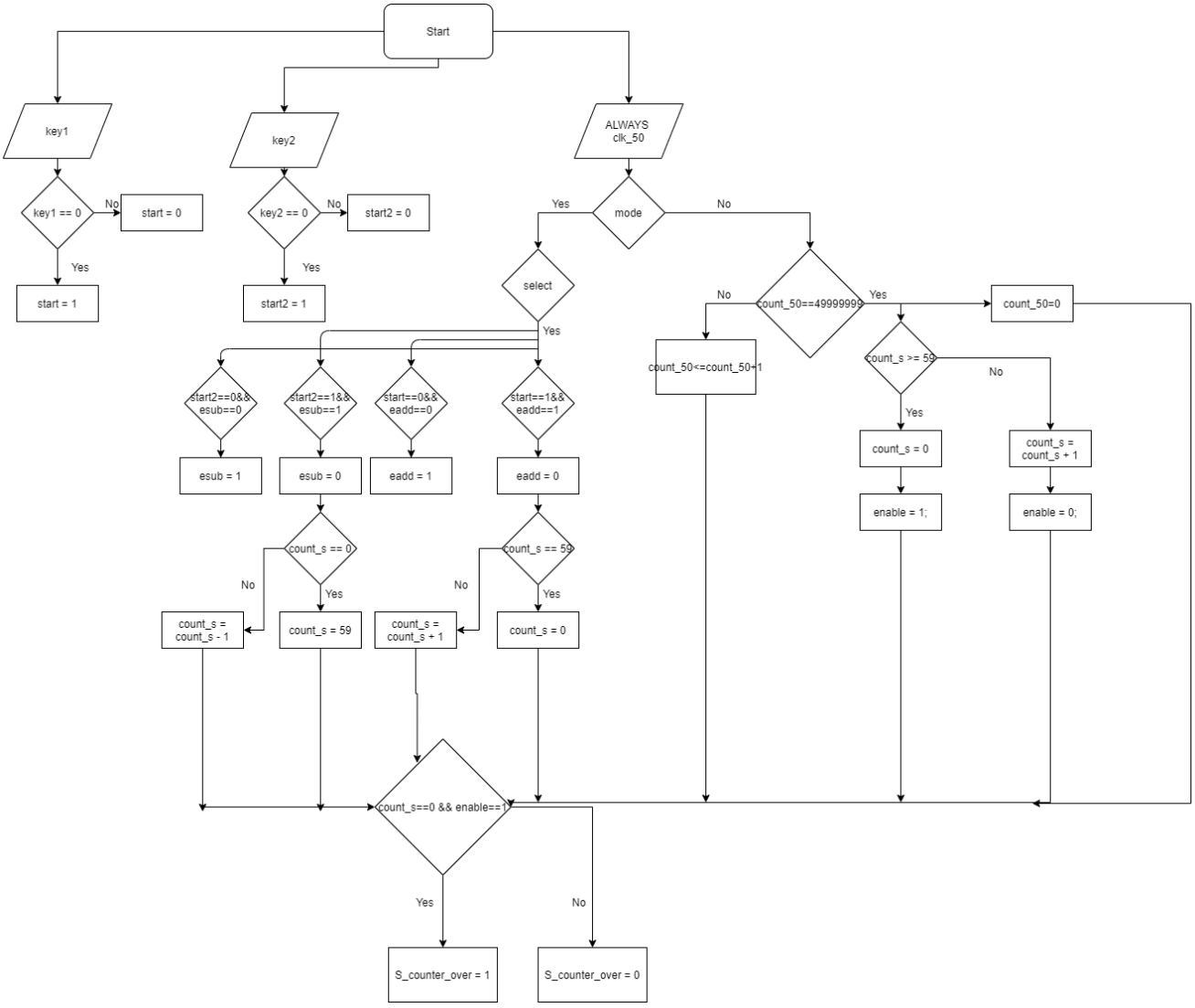
Flowchart example of this idea:



The second signal is use to trigger another counter which is use to count the value of second from 0 to 59. When this counter reaches 59, it will reset back to 0 and trigger a signal (in this case is the “second” in the flowchart above) to increase the minute value.

Integrating with this module is the second setup. This allows our clock to be adjustable. While making this clock, we encounter some problem with asynchronous signal from the key, so we choose to make these setup signal to be synchronous to the 50MHz signal. This signal changes so fast that our eyes can not even notice. Two keys are responsible for the increasing and decreasing of the second counter value. The key which is for mode picking is in the other module so we will discuss about it later.

Detailed flowchart of our Second Module:



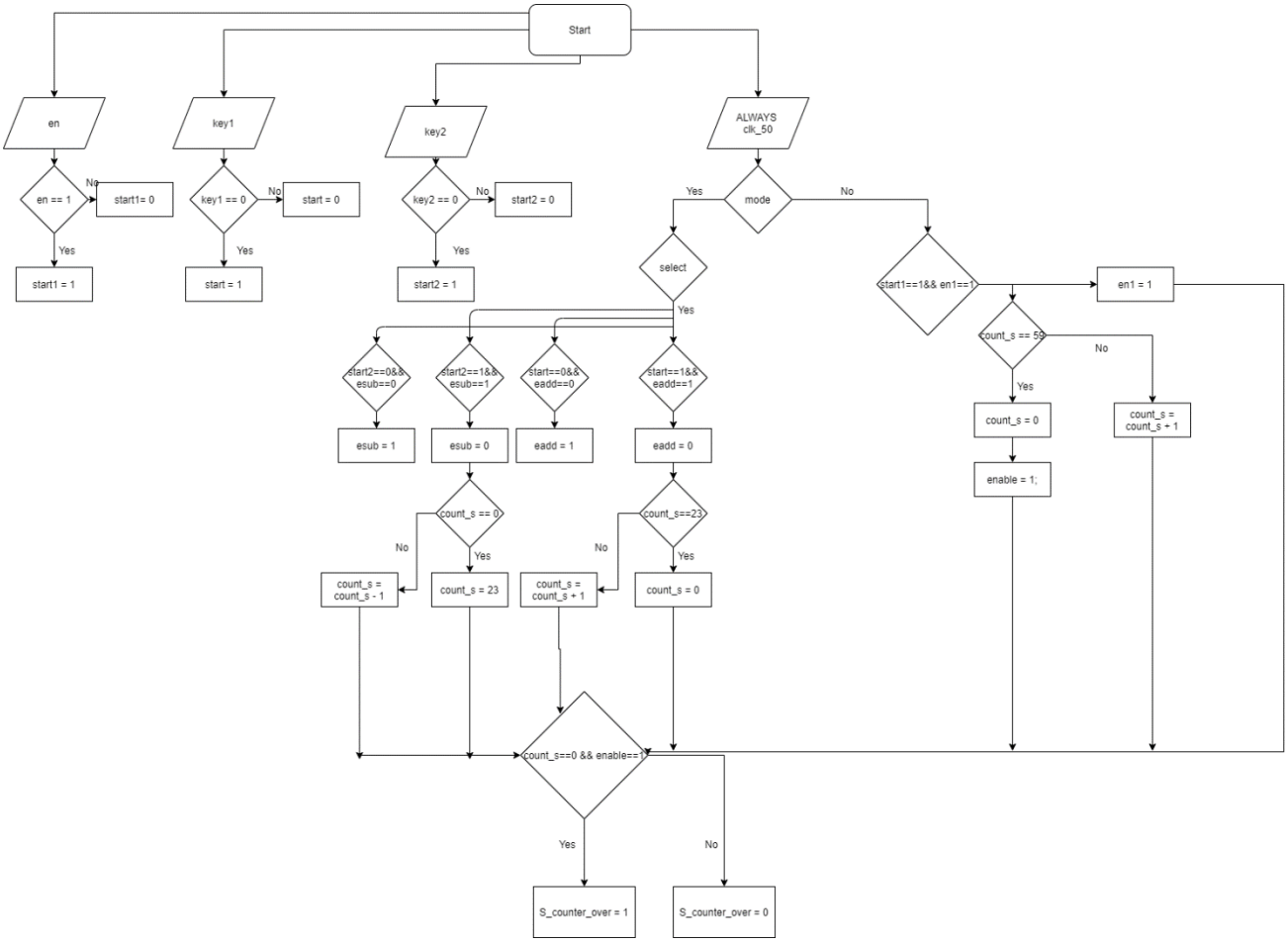
The output of this module is the S_counter_over signal. This signal later will be connected to the Minute Module as a enable signal, triggering the addition of the counter in the Minute Module. Moreover, the count variable in this module will to transfer to a decoder which will translate this signal into two 7 bits signal. These two 7 bits signal will be connected to the 7 segments LED on the DE2i-150 to display the second value to the user.

b. Minute Module:

The principle of this module is quite similar to the Second Module. But there are some differences. This module is synchronous to the 50MHz signal. Only

when received the enable signal from the previous module, it would increase the counter value.

Detail flowchart of the Minute Module:

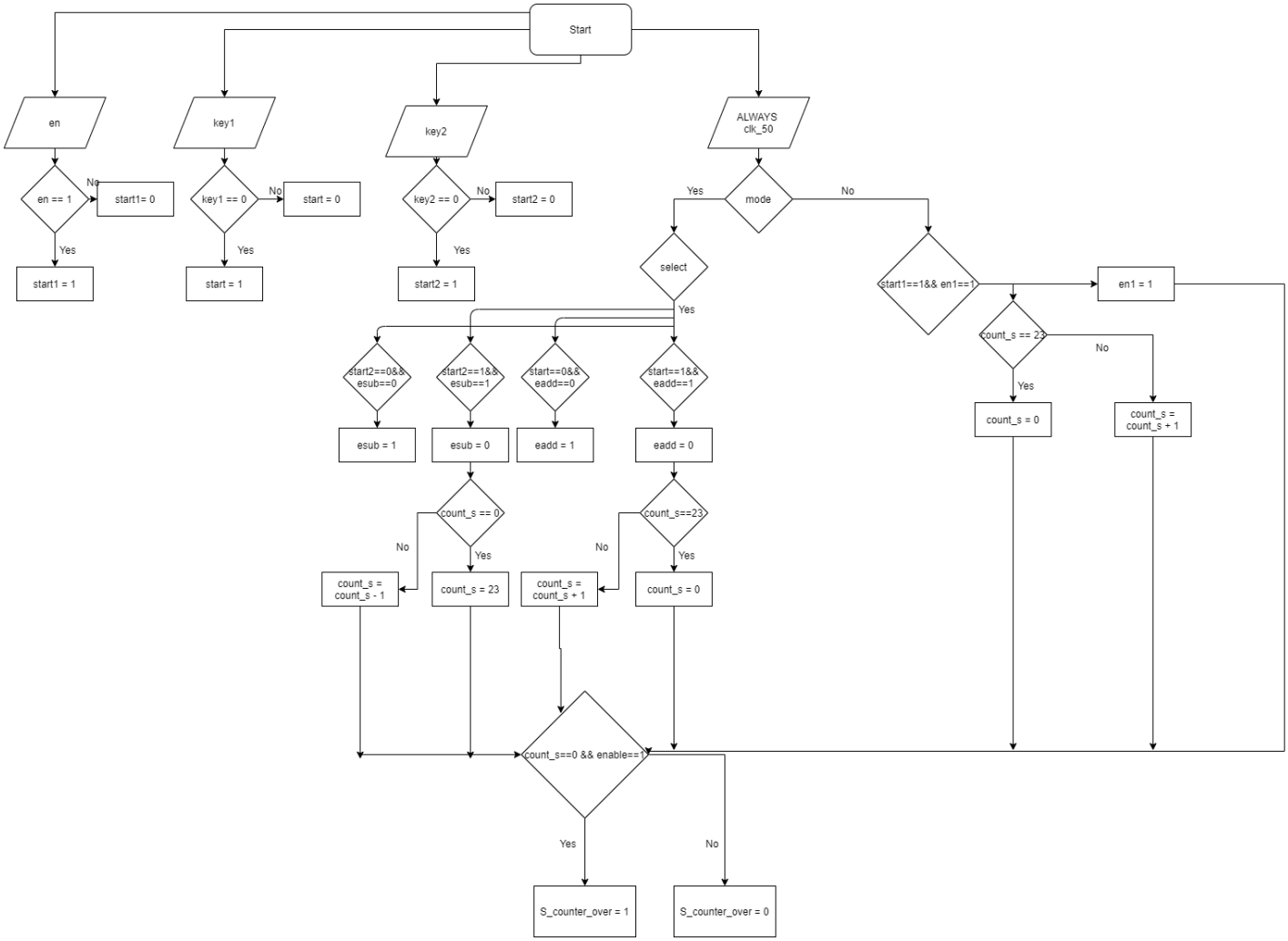


Same as the Second Module, the Minute Module also have a setup state which receive the signal from the Key to increase or decrease its counter value correspondingly.

c. Hour Module:

The Hour Module is totally alike the Minute Module with some little tweak. The maximum of the counter now is 23 (not 59 anymore). And the Hour Module does not output a trigger signal like two of its previous modules.

Detailed Flowchart of the Hour Module:



d. Control Module:

This module is used to control the mode of clock. It will pass the control signal to the 3 main module. This control module also has a counter that counts from 0 to 3 (4 states of the clock). When the counter is 0, the clock is at Idle state. When the counter is 1, the clock is at Second Set up state. When the counter is 2, the clock is at Minute Set up state. When the counter is 3, the clock is at Hour Set up state. When the counter reach over value 3, it will reset back to 0.

e. 7 segments LED decoder:

This module is used to translate all of the count signal in to 7 bits signal. With this, we can display our result to the 7 segments LED on the DE2i-150 board.

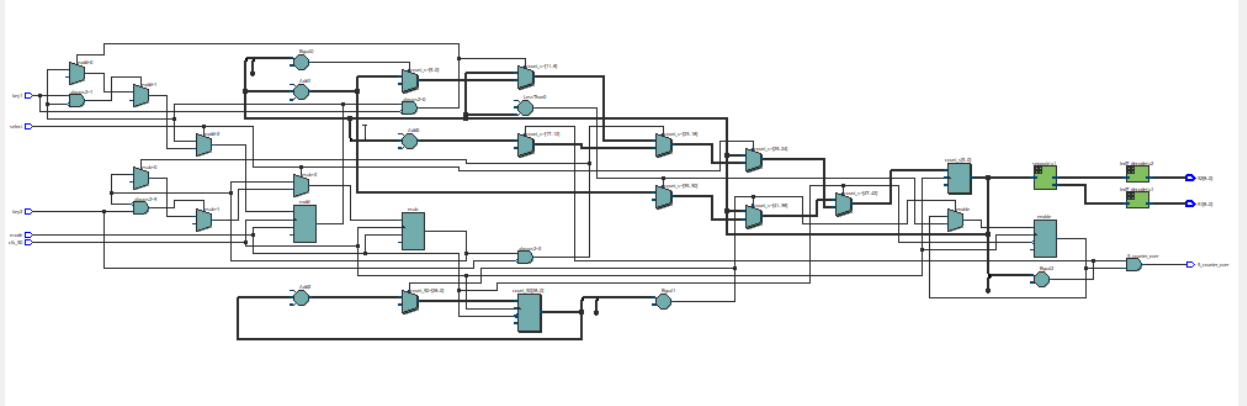
II. Implementation:

Base on our design idea, we implement it onto the Quartus Prime Software.

a. Second Counter:

The source code is attached in .zip file.

RTL viewer:

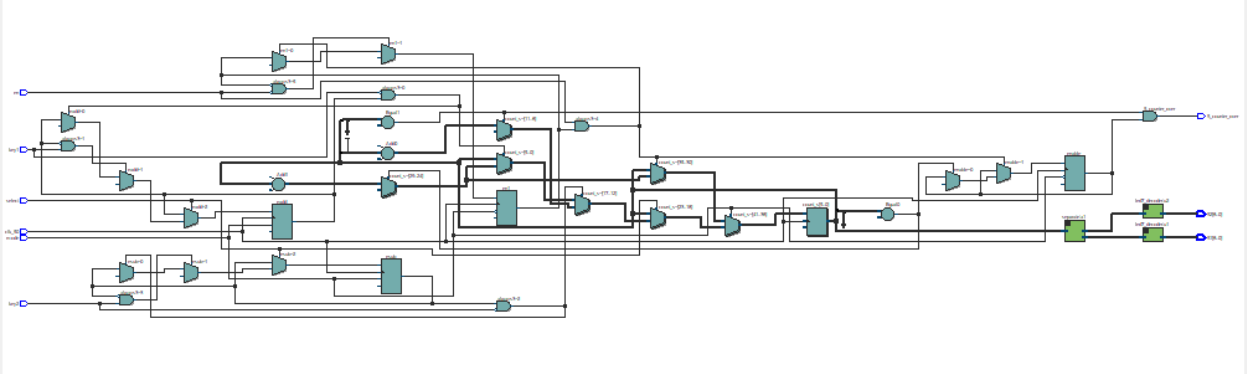


We also attached a separate .pdf file of the RTL viewer in .zip file.

Source code file name: second_counter.v

b. Minute Counter:

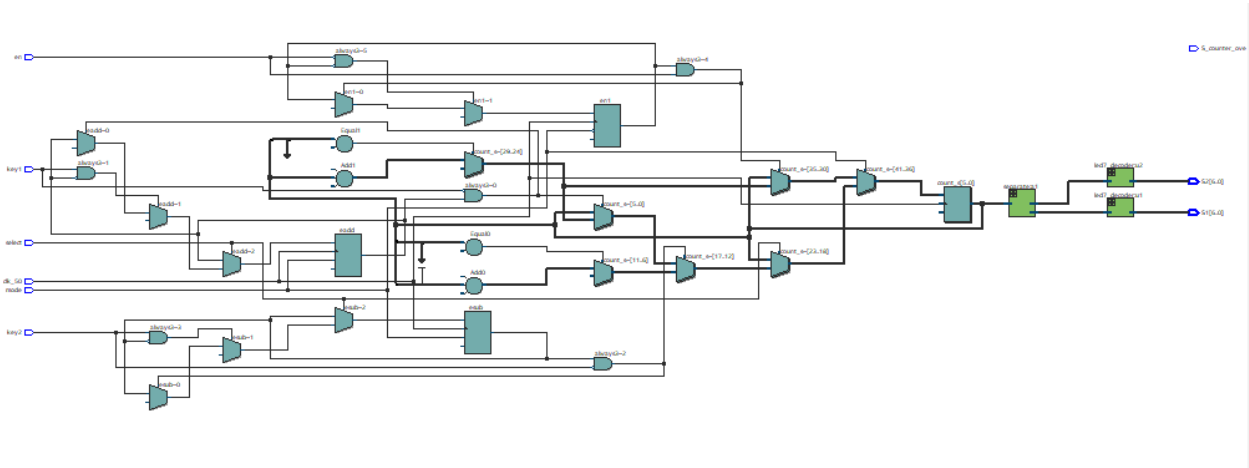
RTL viewer:



Source code file name: minute_counter.v

c. Hour Counter:

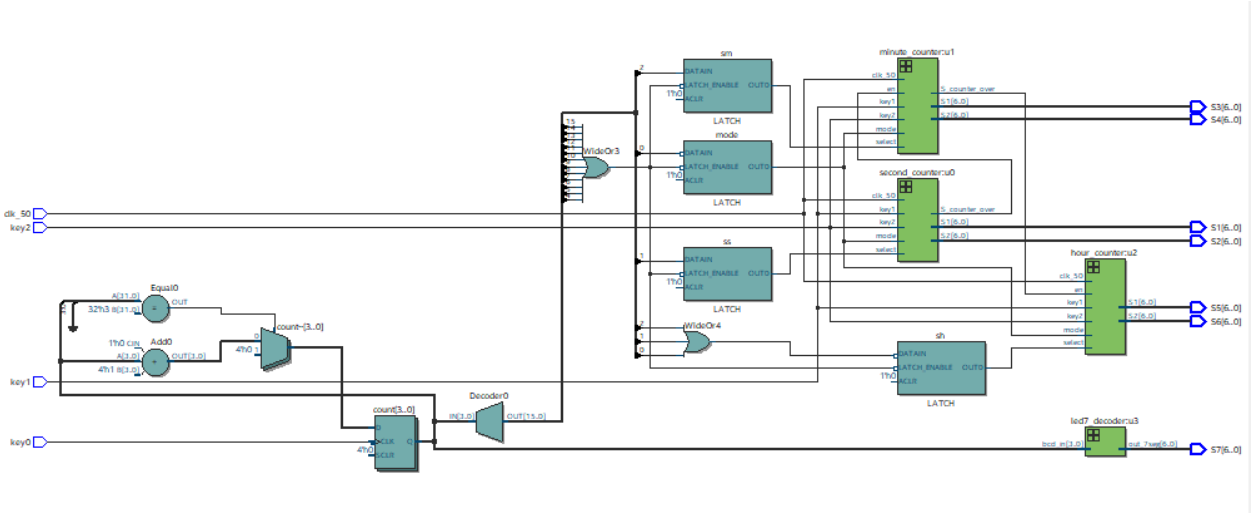
RTL viewer:



Source code file name: hour_counter.v

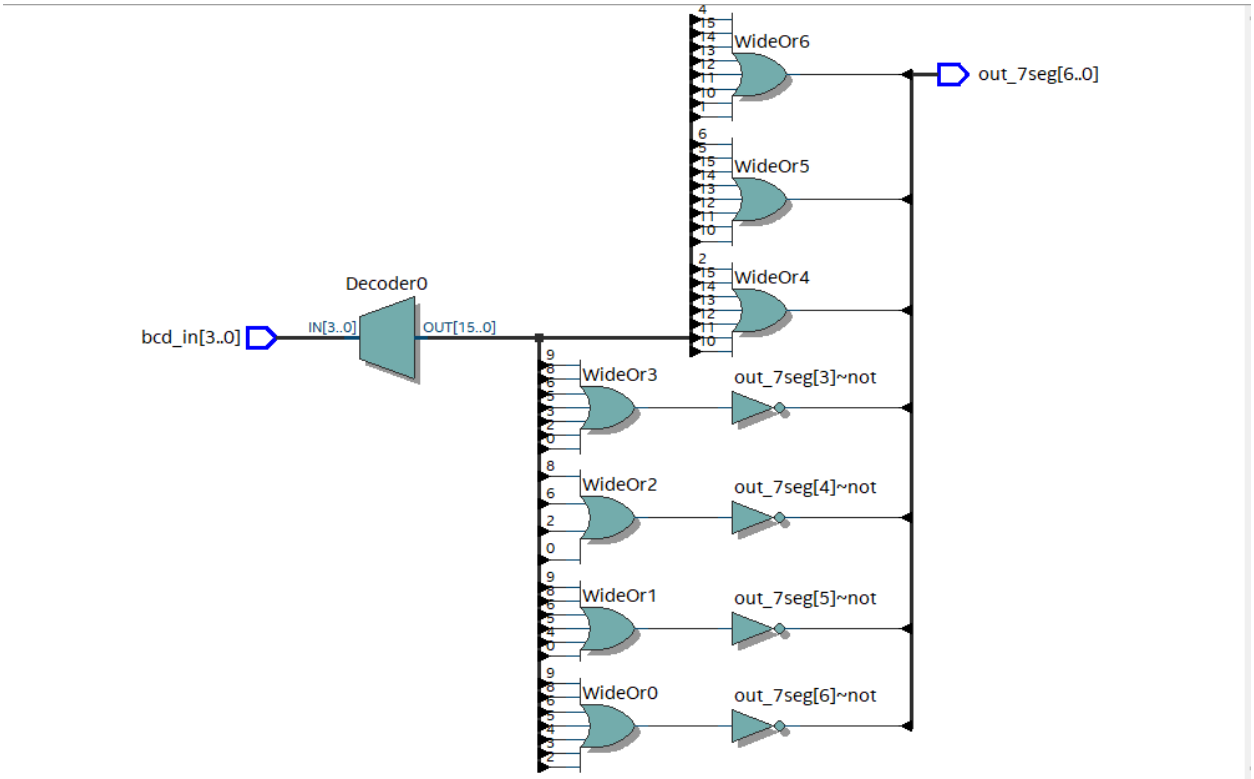
d. Control Module

RTL viewer:



Source code file name: clock_counter.v

e. 7 segments LED decoder:



Soure code file name: led7_decoder.v

Chapter 3: Experiments

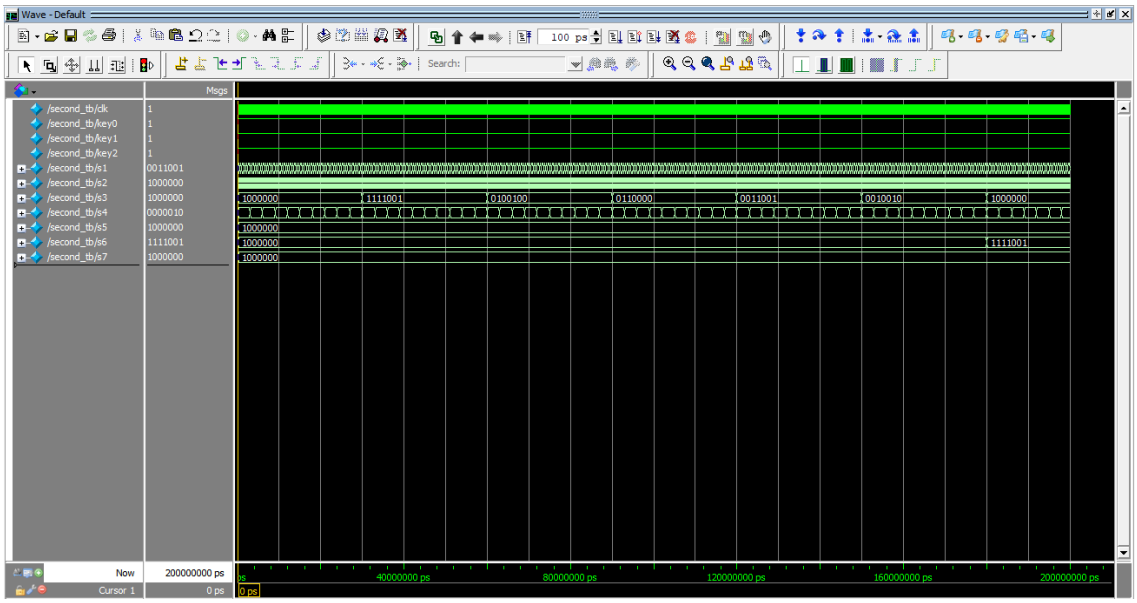
For the testbench, we modify the second module a little bit for easier simulation. In the second module, the counter which based on the 50MHz will count from 0 to 4.

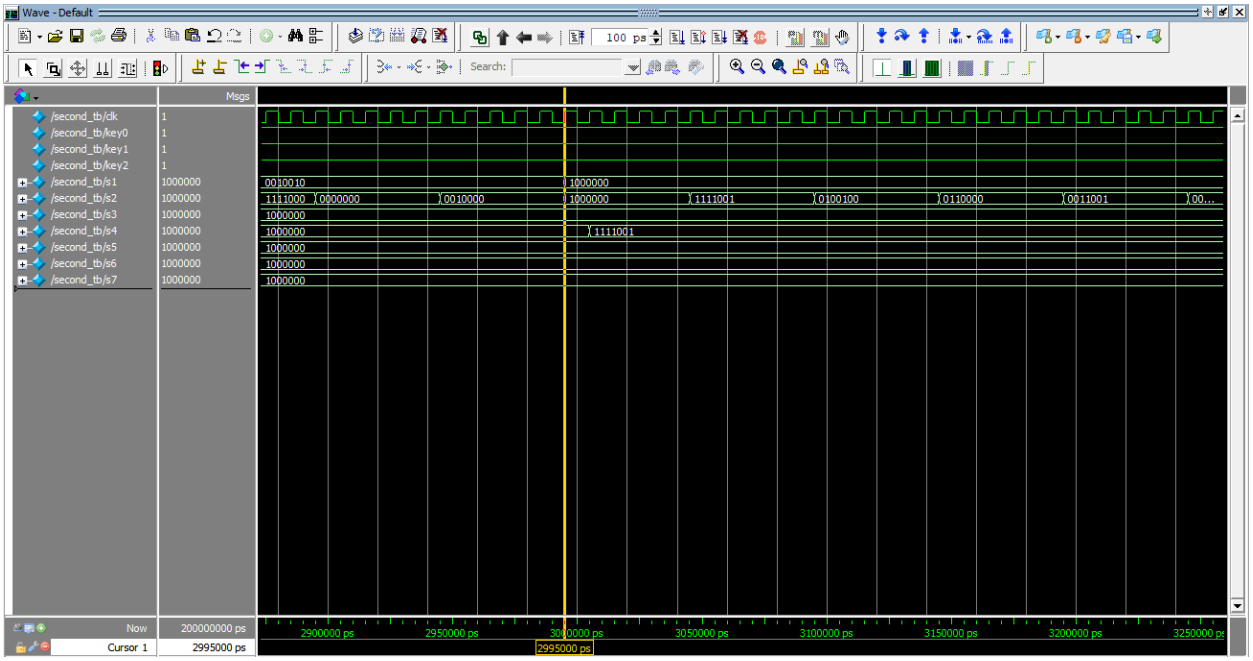
a. Normal clock simulation (mode 0):

Testbench code:

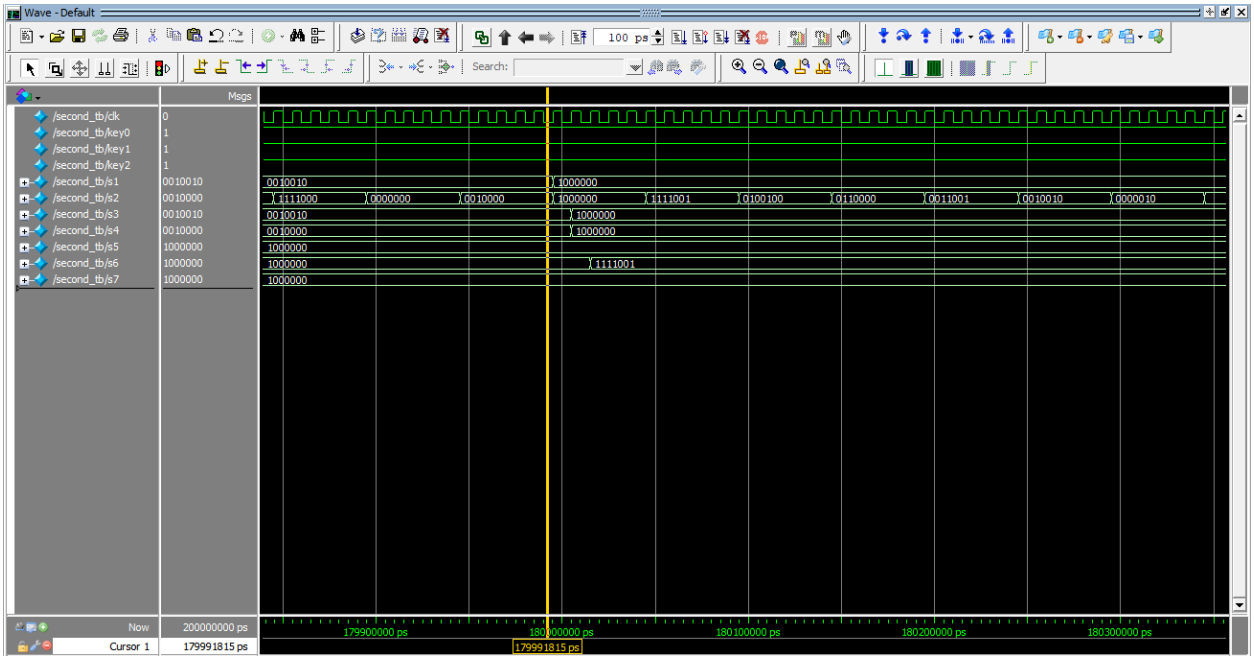
```
1   `timescale 1ns/1ps
2   module second_tb();
3      reg clk,key0,key1,key2;
4      wire [6:0]s1, s2,s3,s4,s5,s6,s7;
5      clock_counter uut(clk,key0,key1,key2,s1,s2,s3,s4,s5,s6,s7);
6
7      always begin
8
9      clk=~clk;
10     #5;
11     end
12     initial begin
13        clk=0;
14        key0=1;
15        key1=1;
16        key2=1;
17        #200000;
18        $stop;
19     end
20  endmodule
```

Waveform:





Zoom in of the wave at the position where the Second Module trigger the Minute Module. At this moment the board will display 00:01:00 corresponding to the 7 bits signal.



Zoom in of the wave at the position where the Second Module trigger the Minute Module. At this moment the board will display 01:00:00.

b. Second, Minute, Hour Setup Testbench:

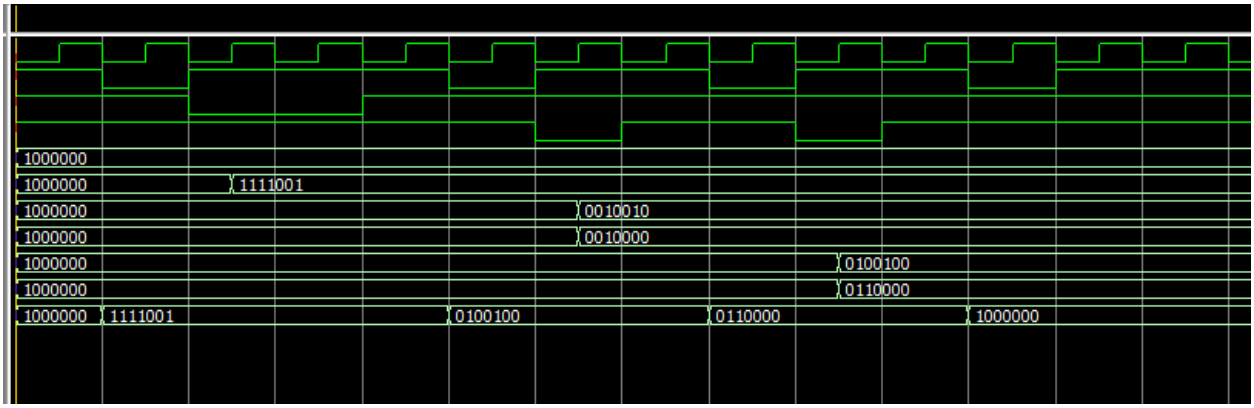
Testbench code:

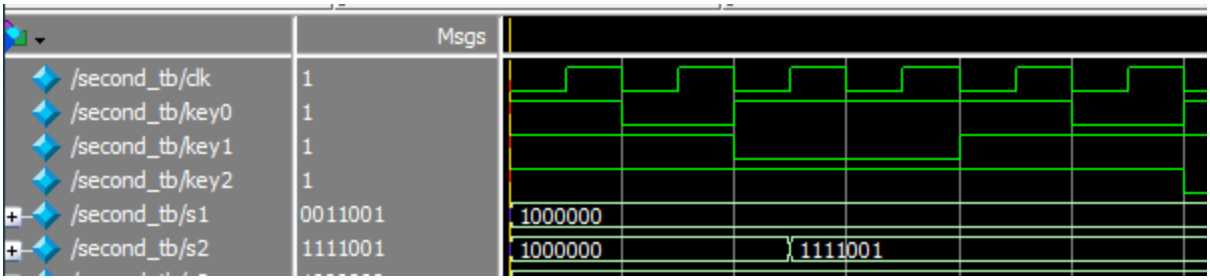
```
1   `timescale 1ns/1ps
2   module second_tb();
3      reg clk,key0,key1,key2;
4      wire [6:0]s1, s2,s3,s4,s5,s6,s7;
5      clock_counter uut(clk,key0,key1,key2,s1,s2,s3,s4,s5,s6,s7);
6
7      always begin
8
9      clk=~clk;
10     #5;
11     end
12     initial begin
13        clk=0;
14        key0=1;
15        key1=1;
16        key2=1;
17        #10;key0=0; #10 key0=1;
18        key1=0; #10 key1=1;
19        #10;key0=0; #10 key0=1;
20        key2=0; #10 key2=1;
21        #10;key0=0; #10 key0=1;
22        key2=0; #10 key2=1;
23        #10;key0=0; #10 key0=1;
24        #200000;
25        $stop;
26     end
27  endmodule
```

Explain code:

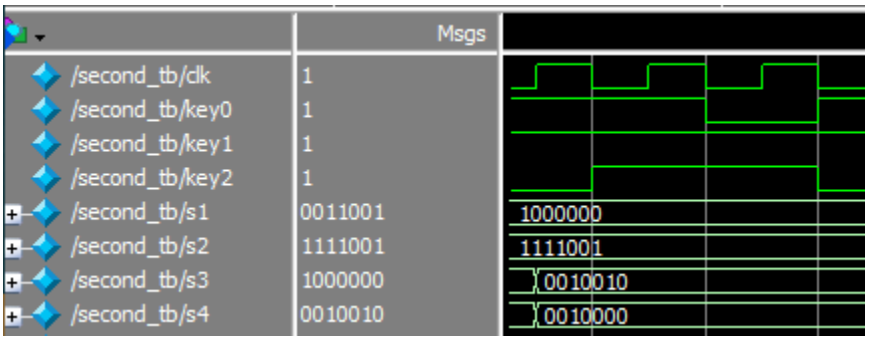
In this testbench we going to run through 4 mode of the clock, making adjustment to the second, minute and hour value of the clock. So key0 is the trigger the state change. Because the key on the DE2i-150 board produce a active low signal when it is pressed so we design all of our module to be negative edge trigger. In line 17, we simulate that key0 is pressed. This trigger the clock to change its mode from 0 to 1. Key1 in line 18 act as trigger for increasing the value of second by 1. So after line 18 the second signal is increased by 1. Next line 19, we change to mode 2. Line 20, we use key2 to decrease the value of minute value. Line 21, change to mode 3. Line 22, decrease hour value by 1. Line 23, trigger the clock back to the Idle state.

Waveform:

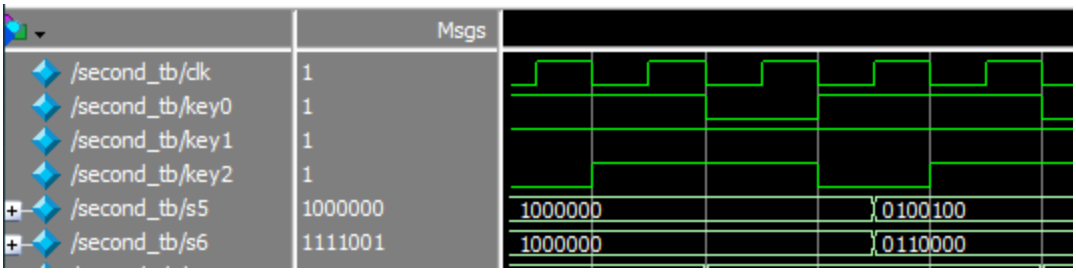




Increase in second value (from 00 to 01)



Decrease in minute value (from 00 to 59)



Decrease in hour value (from 00 to 23)

Chapter 4: Conclusion and future works

In conclusion, we had gained a lot of experience after working on this project. For this digital clock there are more to be improve. What we've worked is just 3 basics function. In the future we hope that we get more function into in clock such as alarm, stopwatch, ….

Major strength of our clock: It's won't get glitches as all of our module is synchronous on the 50MHz signal.

Weakness: The 50MHz signal is the major drawback of this design. Because of our lack of experience in using the asynchronous signal so we choose to stay with the 50MHz signal.

Table of duty roaster

Name	ID	Duty
Lê Nguyễn Tân Lộc	1952088	Minute Module, Second Module
Trần Cảnh Triệu	1952139	Hour Module, Control Module
Trần Ngọc Minh Yến	1952540	LED decoder, Report writing