XL710
REFERENCE SCHEMATICS

REV 1.3

NETWORK DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE: XL710 REFERENCE SCHEMATICS	SIZE: B	CODE	DOCUMENT NUMBER	REV: 1.3	DATE: 07/26/2018	SHEET: 1

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REVISION HISTORY

0.1 -- INITIAL DRAFT

0.5 -- RELEASE VERSION

0.75 -- UPDATED SERIES RESISTORS FOR SMBUS, SERIES RESISTORS TO NC-SI RX
ADDED JTAG HEADER, AND VOLTAGE LEVEL LABELS.
REMOVED BACKUPT MARGINING CONNECTION.

1.0 -- ADDED JUMPER TO ENABLE DEBUG MODE
ADDED LED SETTING DESCRIPTIONS
REMOVED REFERENCE TO CFGID THAT ARE NOT SUPPORTED

1.1 -- UPDATED NOTES ON PG 15 AND 16

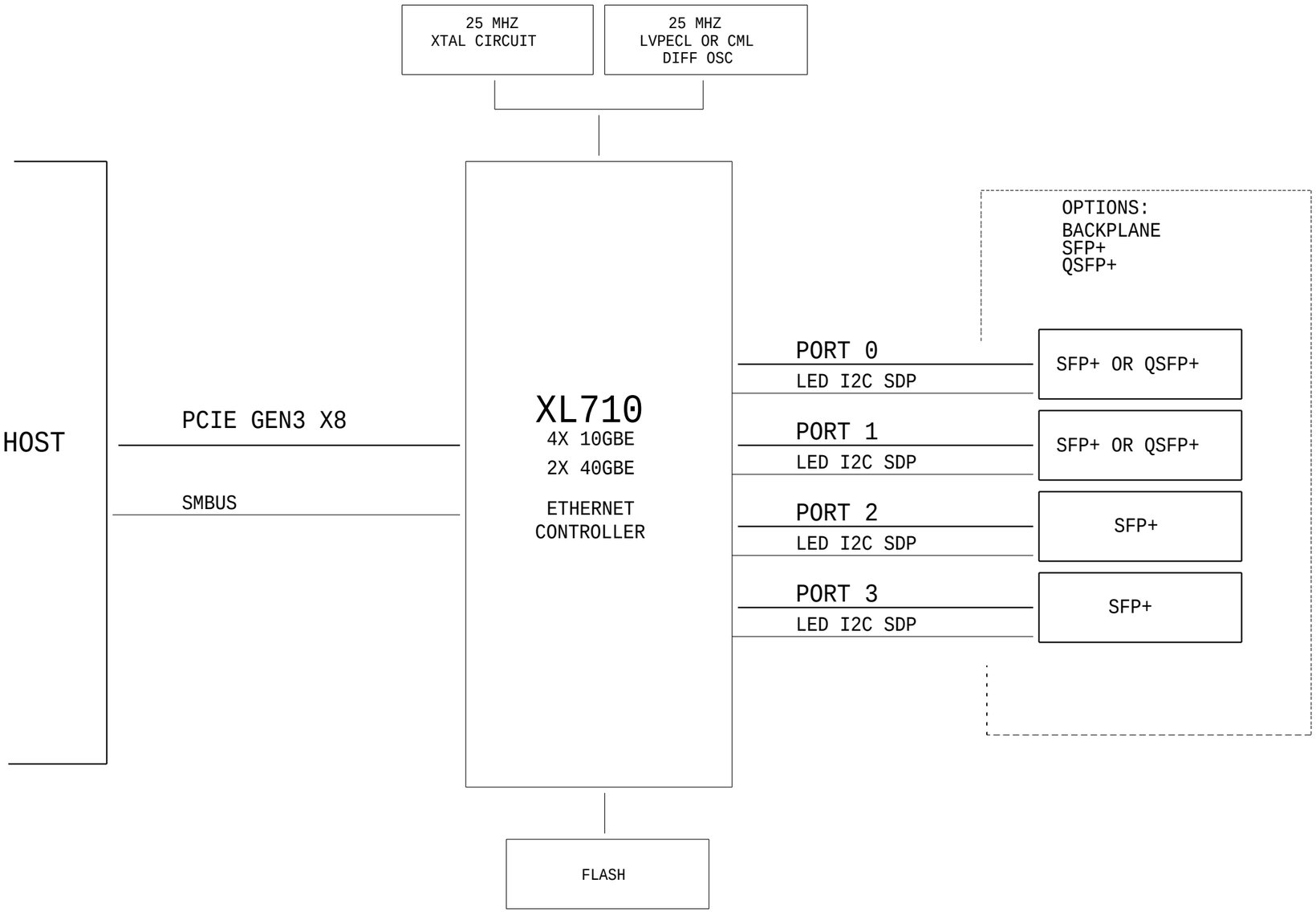
1.2 -- CHANGED NCSI_ARB_IN PULL DOWN FROM 100K TO 10K

1.3 -- UPDATED NC-SI OUTPUT LINES WITH 30 OHM SERIES RESISTORS AS PER
INTEL® ETHERNET CONTROLLER X710/XXV710/XL710 SPECIFICATION UPDATE REV 3.3
ON NCSI_CRS_DV, NCSI_RXD[1:0],AND NCSI_ARB_OUT

-- REMOVED CONNECTIONS TO VCCD EXT_SVR_SENSE_P/N. CHANGED VCCD TO FIXED VOLTAGE OPERATION.
ALL COMPONENTS USED IN EXT_SVR_SENSE_P/N CIRCUIT ARE NOW LABELED "VCCD LEGACY"

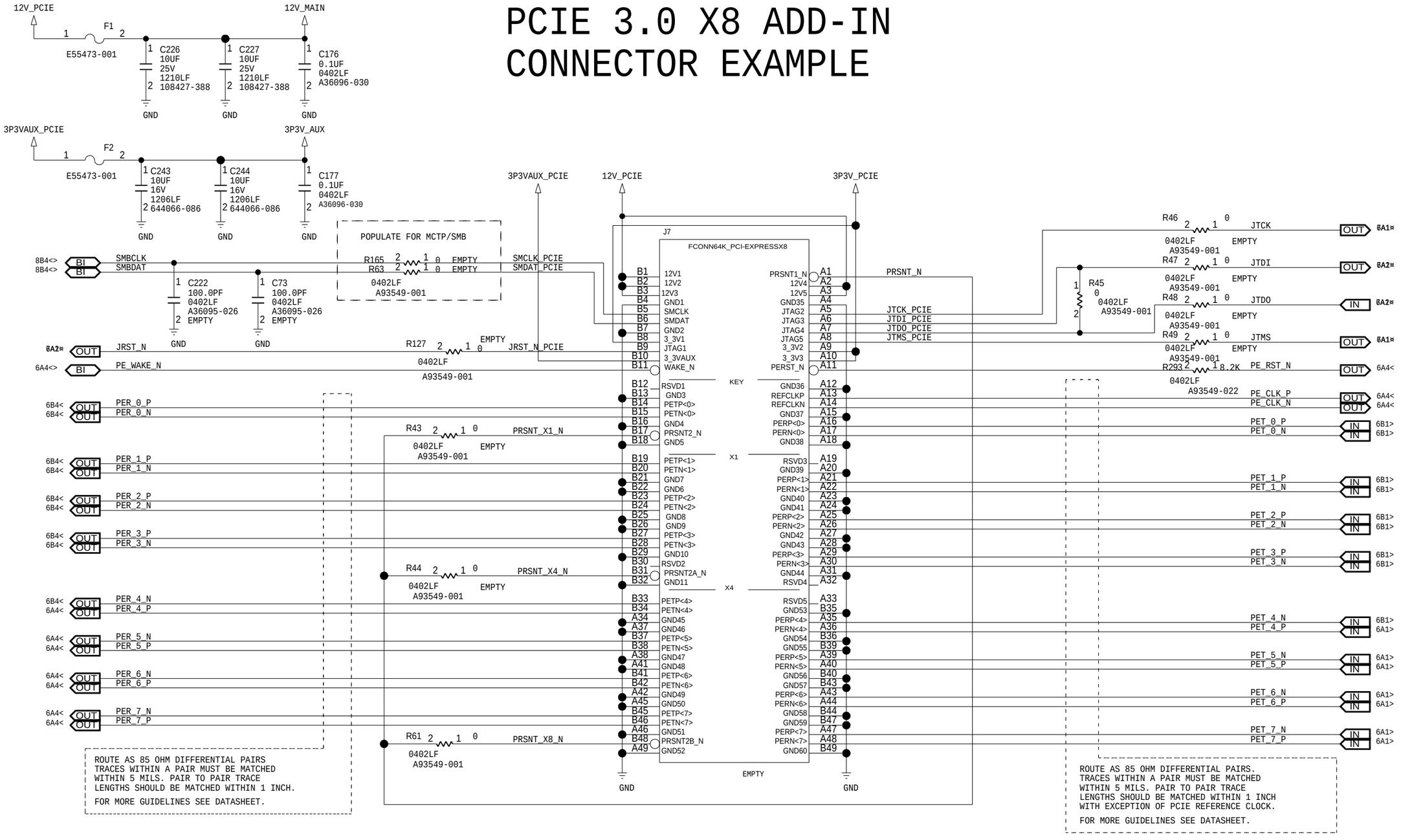
-- REMOVED RIPPLE INJECTION CIRCUIT FROM FEEDBACK PATH ON TPS53353

FUNCTIONAL BLOCK DIAGRAM



NETWORK DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE XL710 REFERENCE SCHEMATICS	SIZE B	CODE	DOCUMENT NUMBER	REV 1.3	DATE 07/26/2018	SHEET 4

PCIE 3.0 X8 ADD-IN CONNECTOR EXAMPLE



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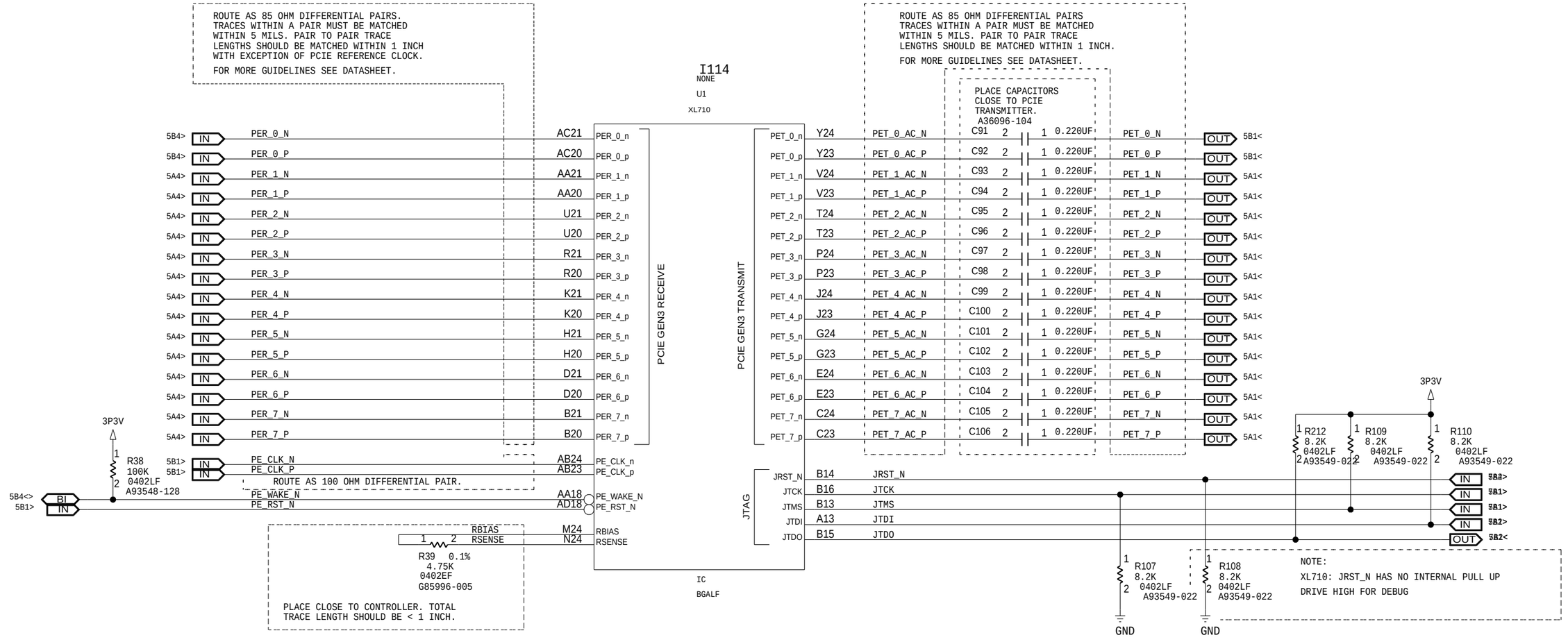

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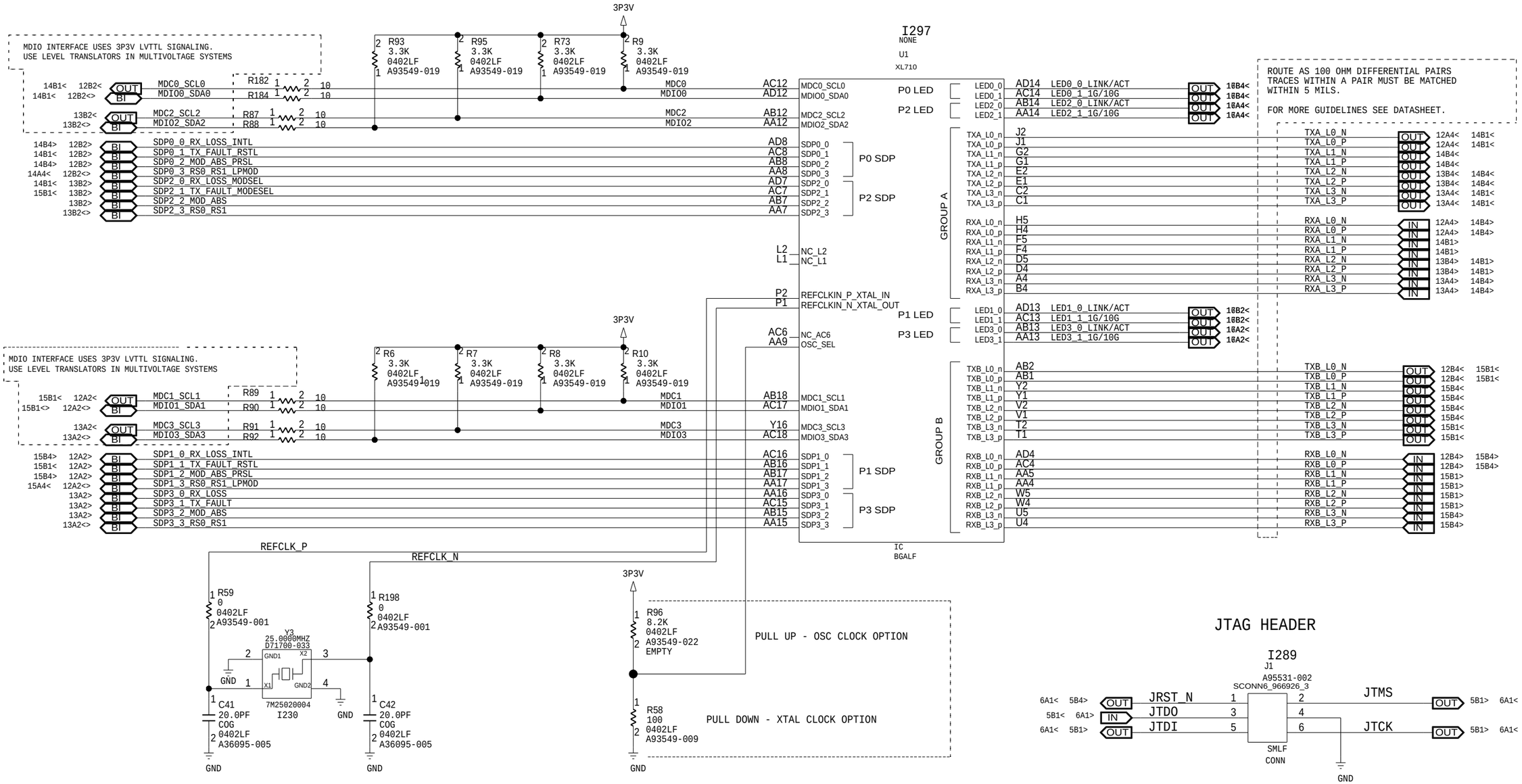

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IF NCSI NOT USED THEN PULL NCSI_RXD_X AND NCSI_TXD_X HIGH
AND PULL NCSI_CLK_IN, AND NCSI_TX_EN LOW

3P3V

R122 100K 0402LF A93548-128
R125 100K 0402LF A93548-128
R147 100K 0402LF A93548-128
R150 100K 0402LF A93548-128
R450 100K 0402LF A93548-128 EMPTY

IN NCSI_ARB_IN
OUT NCSI_ARB_OUT
IN NCSI_CLK_IN
OUT NCSI_CRS_DV
IN NCSI_TX_EN
IN NCSI_TXD_0
IN NCSI_TXD_1
OUT NCSI_RXD_0
OUT NCSI_RXD_1

R41 30 A36093-073
R40 30
R3 30
R4 30 A36093-073

R124 100K 0402LF A93548-128
R146 100K 0402LF A93548-128
R149 100K 0402LF A93548-128
R272 10.0K 0402LF A93548-034

GND GND GND GND

3P3V

R97 8.2K 0402LF A93549-022
R99 8.2K 0402LF A93549-022
R100 8.2K 0402LF A93549-022

5B4<> OUT SMBALRT_N
5B4<> BI SMBCLK
BI SMBDAT

R284 22
R285 22
R286 22 0402 A36093-003

IF SM_BUS IS NOT USED PULL SMBCLK AND SMBDAT UP

3P3V

R406 8.2K 0402LF A93549-022
R102 8.2K 0402LF A93549-022
R103 8.2K 0402LF A93549-022 D3-COLD SUPPORTED
R126 8.2K 0402LF A93549-022 EMPTY
R98 8.2K 0402LF A93549-022
R101 8.2K 0402LF A93549-022

15A4< 14A4<
IN MAIN_PWR_OK
IN VAUX_DIS_N
R343 1 2 0 0402LF A93549-001
IN LAN_PWR_GOOD

R123 100 0402LF A93549-009 EMPTY
R128 100 0402LF A93549-009 ENABLE INTERNAL POR
R148 5% 100 EMPTY 0402LF
R151 100 5% EMPTY 0402LF

GND GND

IN DEV_DIS_N
IN PCI_DIS_N

DEPENDING ON THE NVM SETTINGS PCI_DIS_N CAN
BE USED TO DISABLE CERTAIN PCI FUNCTIONS WHILE
DEV_DIS_N CAN BE USED TO DISABLE THE WHOLE DEVICE
OR SPECIFIC LAN PORTS SELECTED IN THE NVM

AUX_PWR: INDICATES TO THE DEVICE THAS AUXILIARY POWER IS AVAILABLE
THIS SIGNAL SHOULD BE CONNECTED TO AUX POWER OR MAIN/AUX POWER MONITOR CIRCUIT.
THIS PIN IS LATCHED AT THE RISING EDGE OF LAN_PWR_GOOD

MAIN_PWR_OK :INDICATES TO THE DEVICE MAIN POWER IS UP.
THIS SIGNAL SHOULD BE CONNECTED TO MAIN POWER OR MAIN/AUX POWER MONITOR CIRCUIT
THAT MAKES SURE SIGNAL IS DEASSERTED WHEN VAUX IS USED LIKE IN WOL CASE

I274
NONE
U1
XL710

Y8	NCSI_ARB_IN	NCSI	
Y10	NCSI_ARB_OUT		
AC11	NCSI_CLK_IN		
AB11	NCSI_CRS_DV		
AB10	NCSI_TX_EN		
AA10	NCSI_TXD_0		
AD11	NCSI_TXD_1		
AA11	NCSI_RXD_0		
AC10	NCSI_RXD_1		
R_SMBALRT_N	E14	SMBALRT_N	SMB
R_SMBCLK	E8	SMBCLK	
R_SMBDAT	E10	SMBD	
LAN0/DEV_DIS_N	AD21	DEV_DIS_N	
LAN1/PCI_DIS_N	AD20	PCI_DIS_N	
	AC9	MAIN_PWR_OK	
	AB9	AUX_PWR	
POR_BYPASS	D19	POR_BYPASS	
	A14	LAN_PWR_GOOD	

IC
BGALF

GPIO0 E18 GPIO0_R
GPIO1 E16 GPIO1_R
GOPI2 B18 GPIO2_R
GPIO3 A18 GPIO3_R
GPIO5 Y14
GPIO4 Y12

TX DISBLE FOR SFP+
WILL BE IMPLEMENTED
THREOUGH I2C ACCESS

R344 2 1 0 EMPTY TX_DIS0 BI 12B2<
R345 2 1 0 EMPTY TX_DIS1 BI 12A2<
R346 2 1 0 EMPTY TX_DIS2 BI 13B2<
R347 2 1 0 EMPTY TX_DIS3 BI 13A2<
0402LF A93549-001

FLSH_CE_N	B7	FLSH_CE_N	FLASH
FLSH_SCK	A8	FLSH_SCK	
FLSH_SI	B6	FLSH_SI	
FLSH_SO	A7	FLSH_SO	

R33 2 1 22 FLSH_SCK_R
0402LF A93549-003

SERIAL FLASH

3P3V

R153 10.0K 0402LF A93548-034
R156 8.2K 0402LF A93549-022
FLSH_WP_N

U2
IC
AT25DF321A

CS_N VCC
WP_N SO
SI GND
SCK HOLD_N

G86187-001

R154 8.2K 0402LF A93549-022

GND GND

3P3V

R35 8.2K 0402LF A93549-022
C69 0.1UF 0402 A36096-035
FLSH_HOLD_N IN

GND GND

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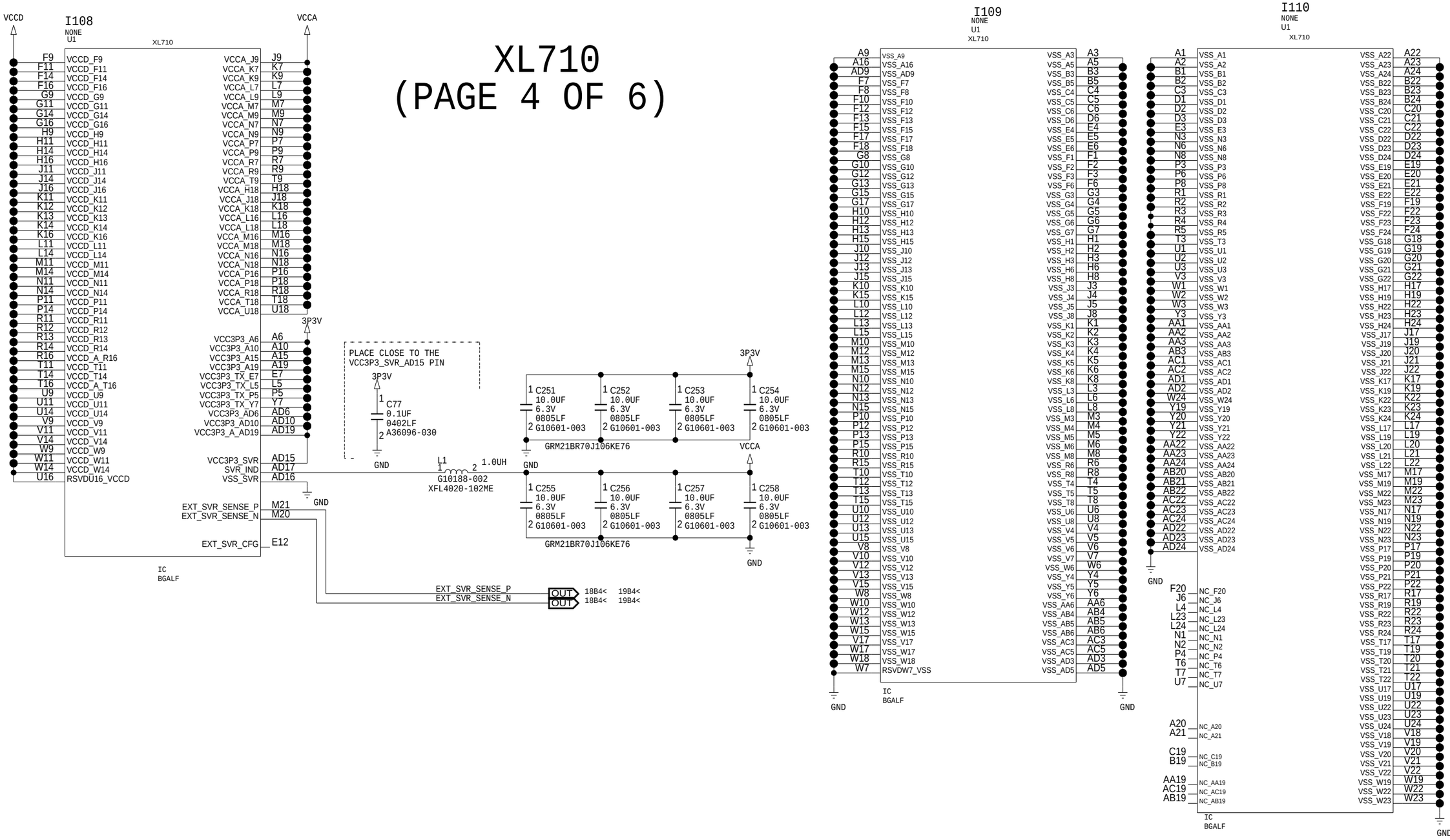

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UNKNOWN

NETWORK DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE: XL710 REFERENCE SCHEMATICS	SIZE: B	CODE	DOCUMENT NUMBER: G9986101	REV: 1.3	DATE: 07/26/2018	SHEET: 9

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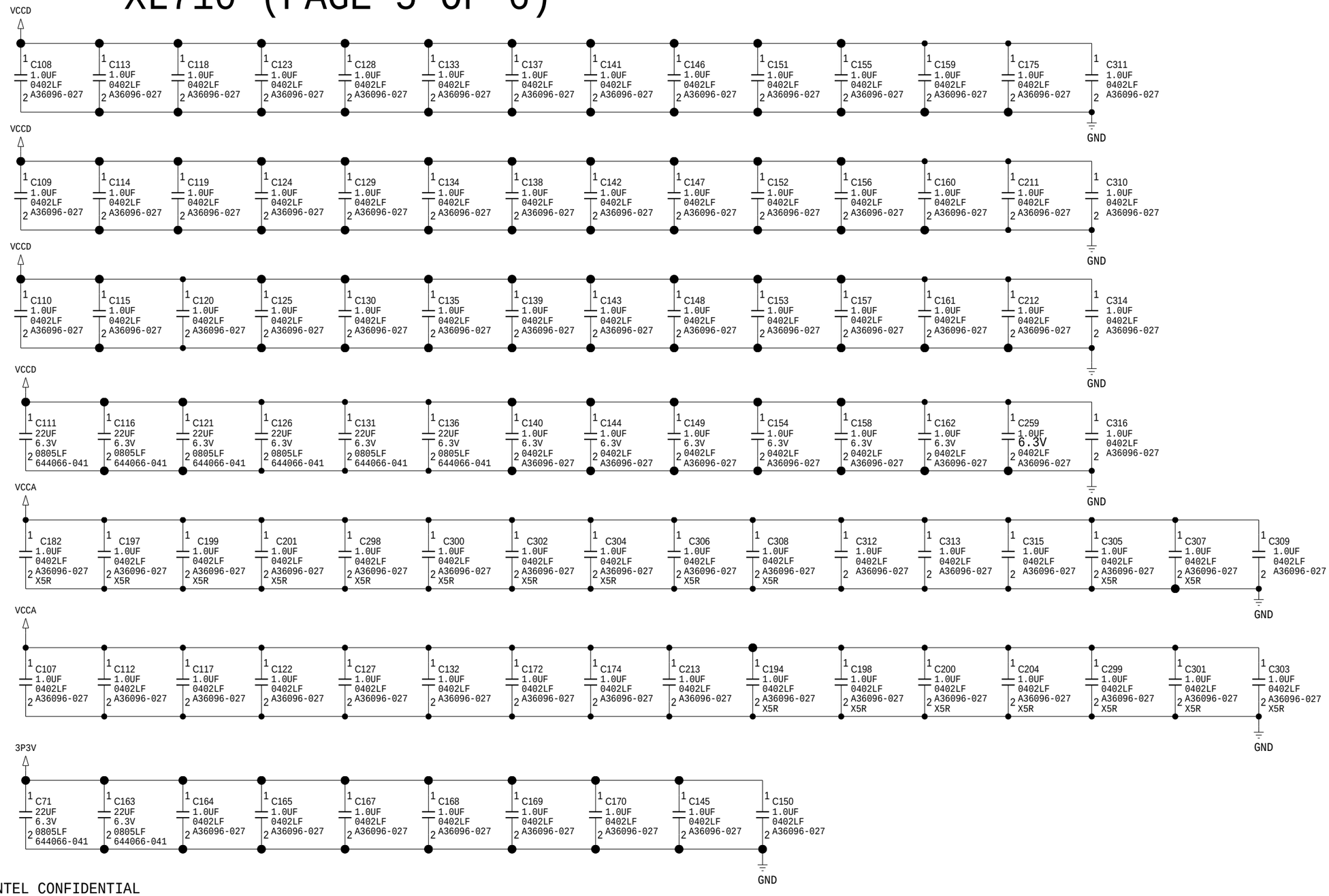

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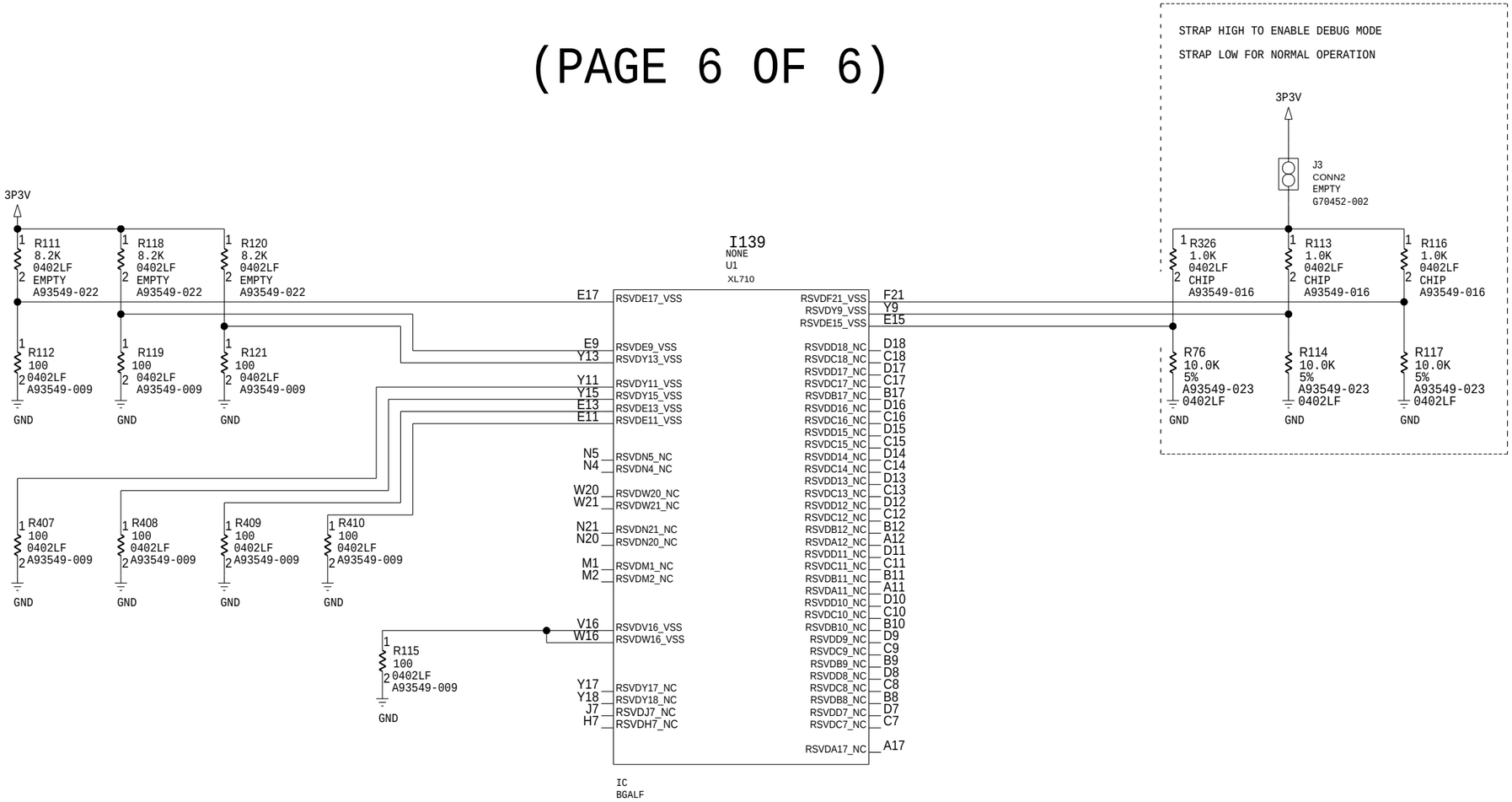

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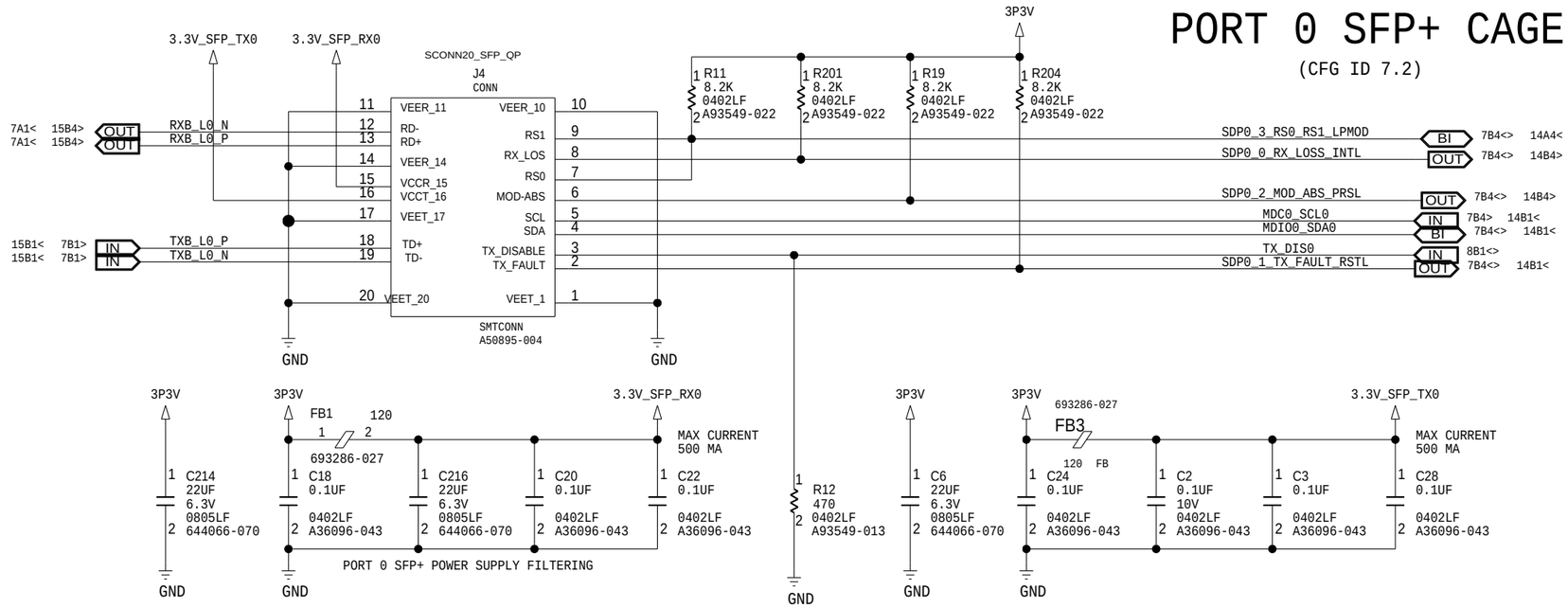
PORT 0 SFP+ CAGE

(CFG ID 7.2)

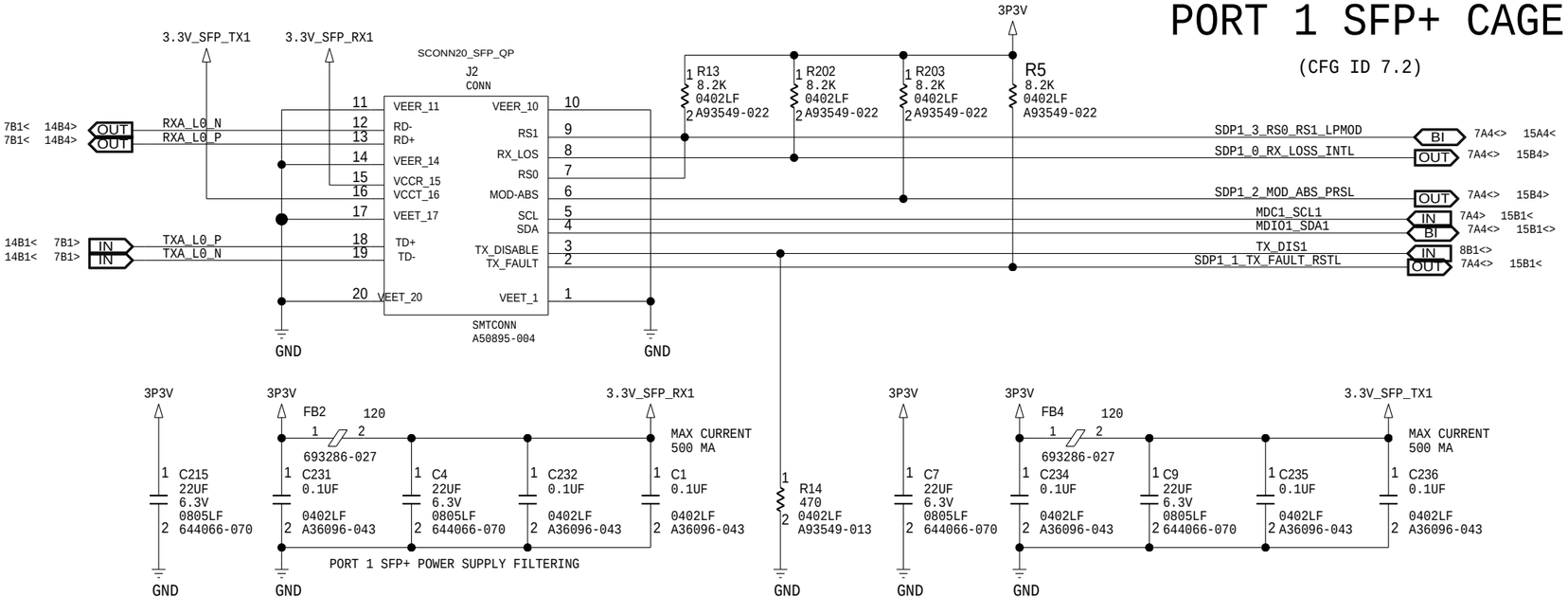


SFP+ OPTION

(1 OF 2)

PORT 1 SFP+ CAGE

(CFG ID 7.2)



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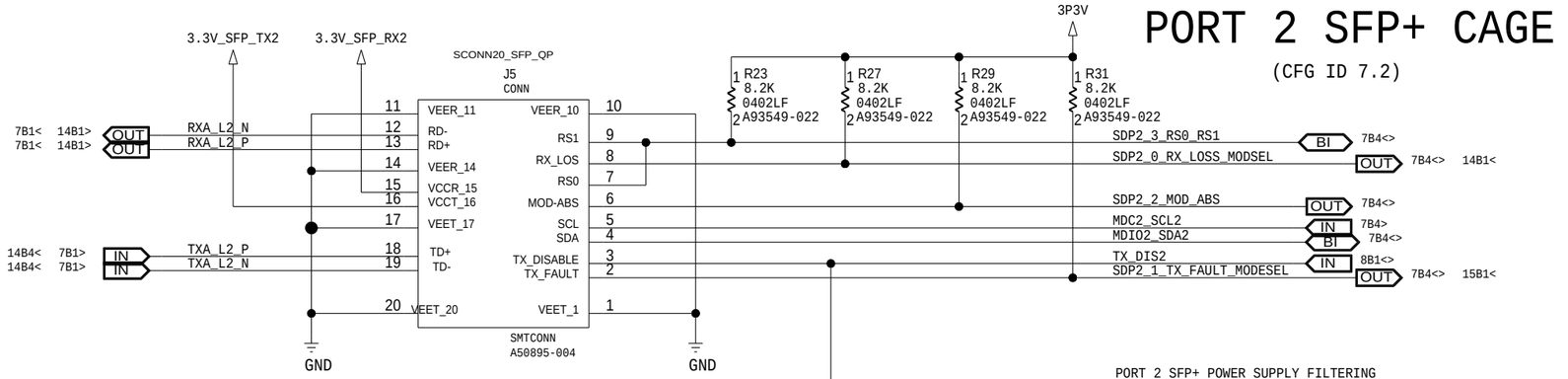
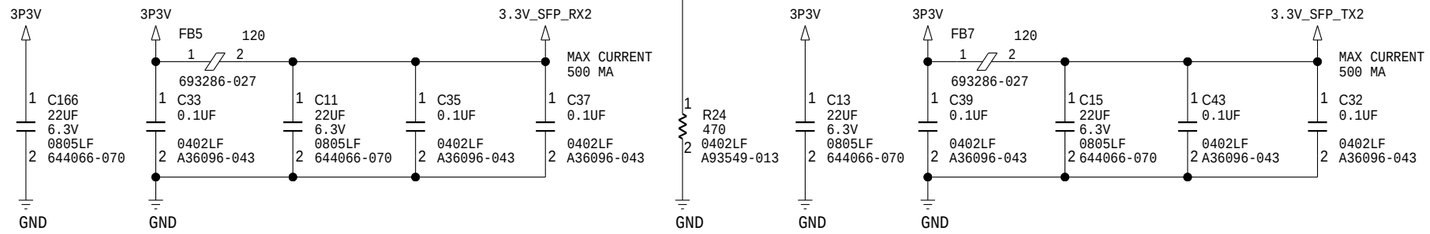
PORT 2 SFP+ CAGE

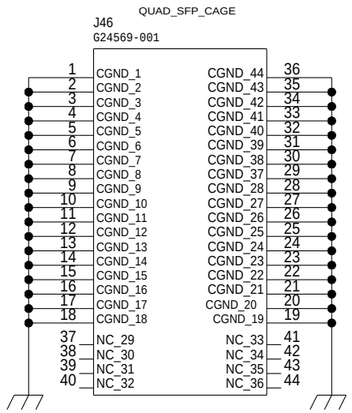
(CFG ID 7.2)

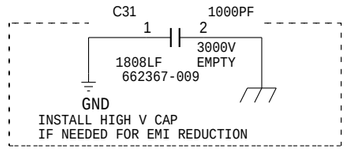


PORT 2 SFP+ POWER SUPPLY FILTERING



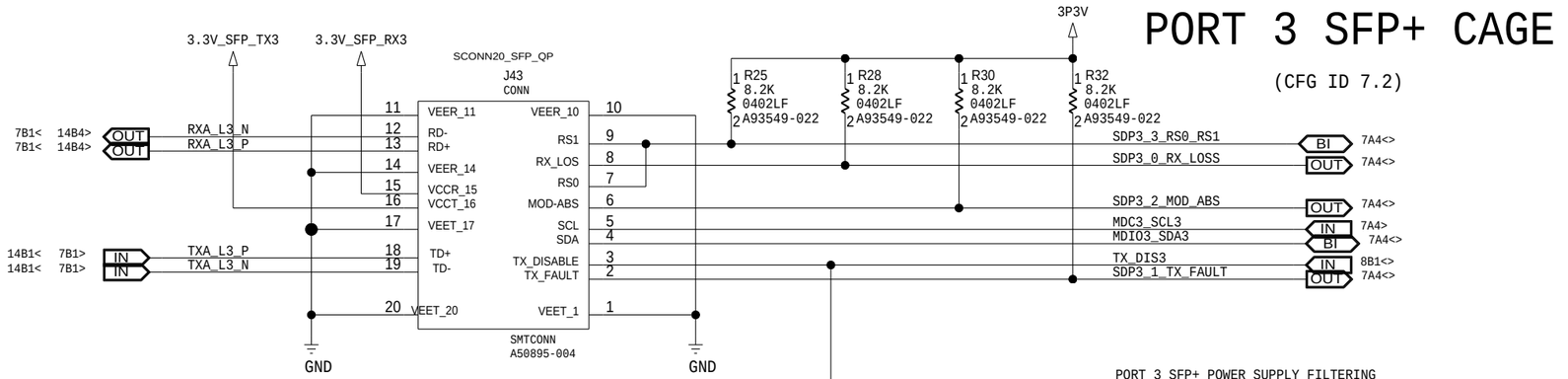
4 PORT GANGED CAGE



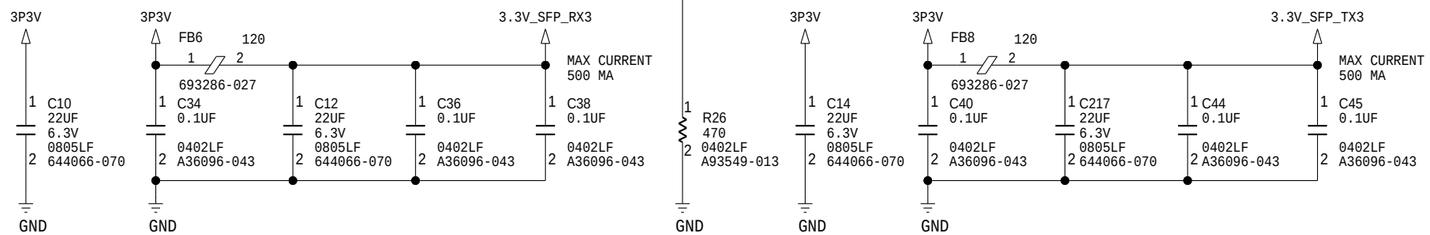


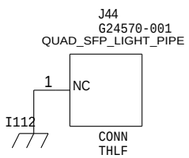
PORT 3 SFP+ CAGE

(CFG ID 7.2)



PORT 3 SFP+ POWER SUPPLY FILTERING





SFP+ OPTION

(2 OF 2)

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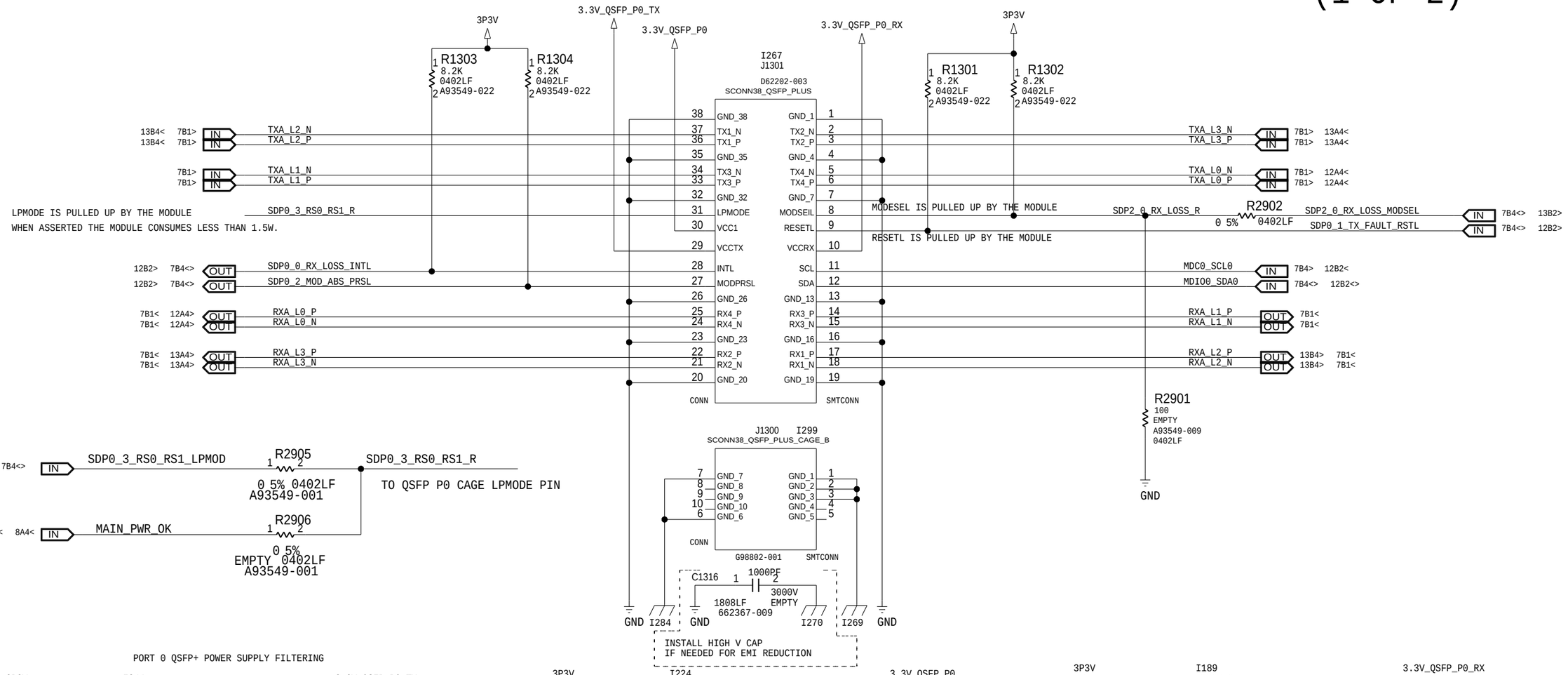
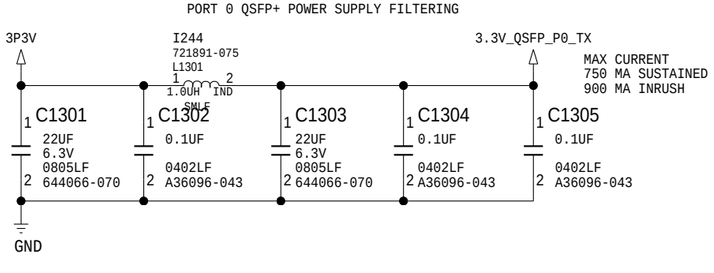
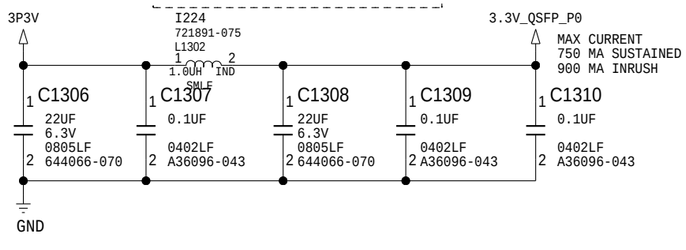
PORT 0 QSFP+ CAGE

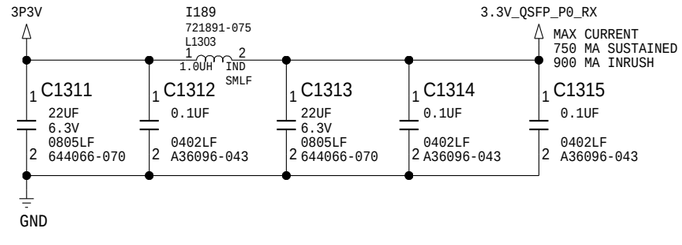
QSFP+ OPTION
(1 OF 2)

(CFG ID 4.0 FOR SINGLE PORT CASE)
(CFG ID 4.5 FOR DUAL PORT CASE)









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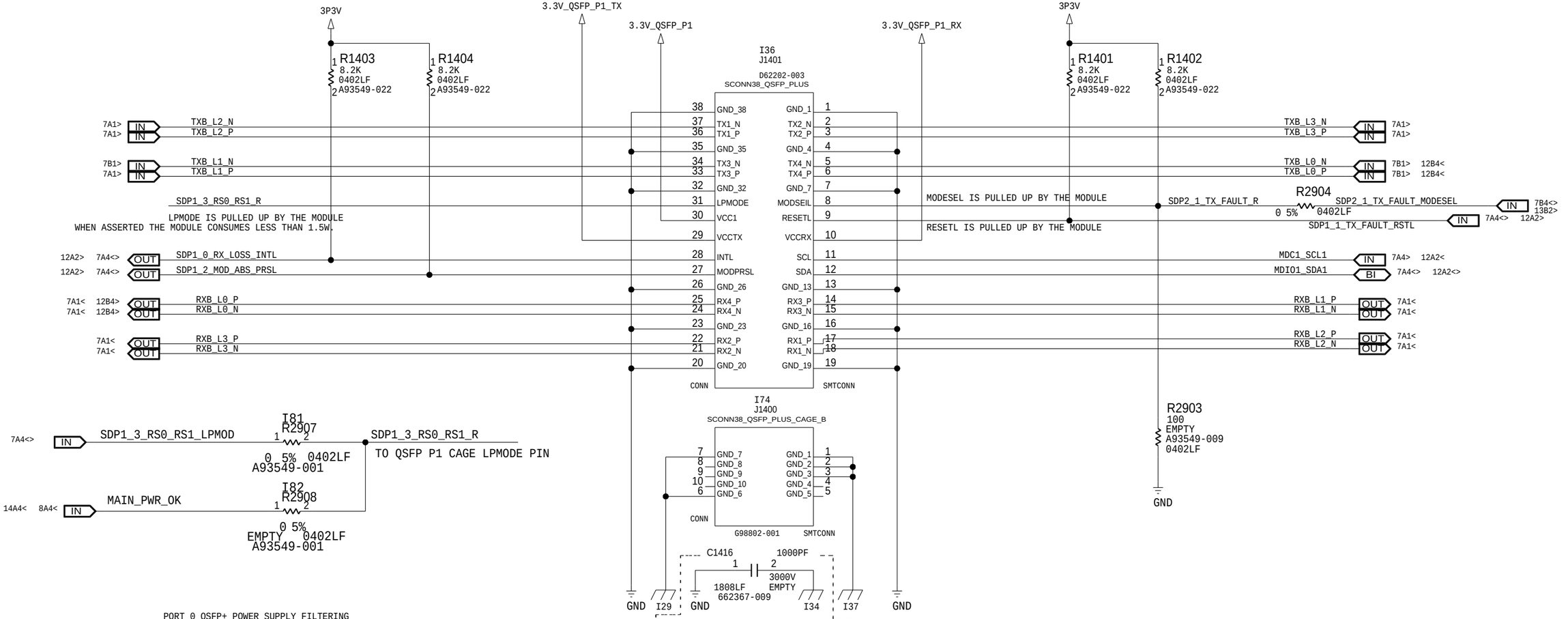
QSFP+ OPTION
(2 OF 2)

PORT 1 QSFP+ CAGE

(CFG ID 4.5 FOR DUAL PORT CASE)



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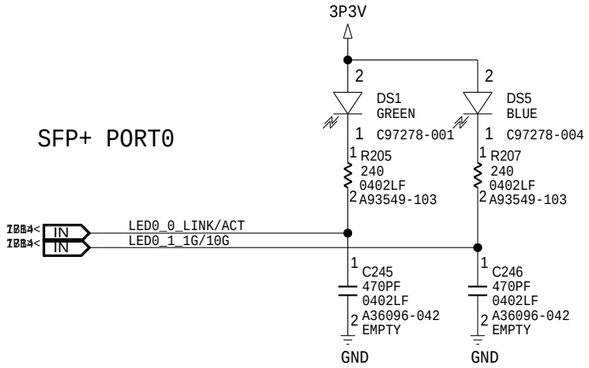
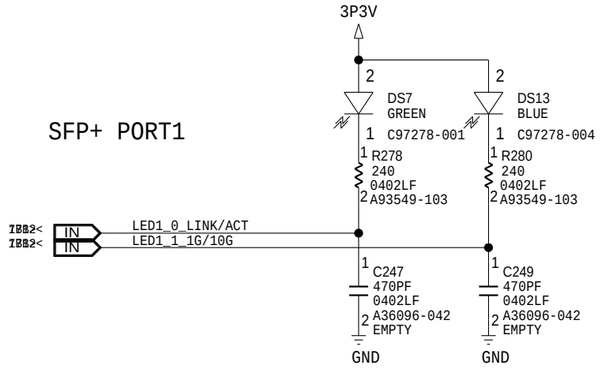
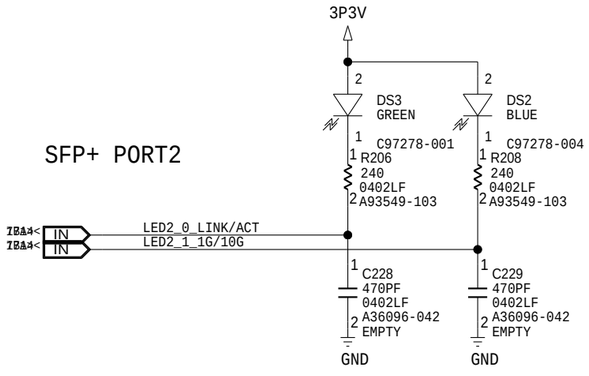
LEDS

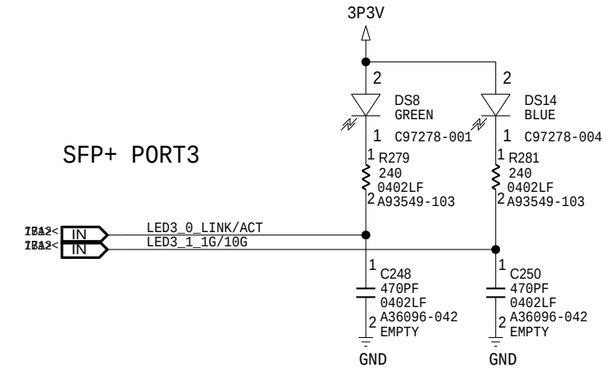
4X10GBE

CFGID 7.2









LED SETTING	DESCRIPTION
1X40	SP 40G
2X40	DP 40G
4X10	4X10 OR 2X2X10 BREAKOUT
2X2X10	4X10 OR 2X2X10 BREAKOUT

BALL#	PIN	GPIO	PORT	LED_MODE (10G)
AD14	LED0_0	22	1	LINK_ACT(0XC)
AC14	LED0_1	23	1	LINK_10G(0X3)
AD13	LED1_0	24	0	LINK_ACT(0XC)
AC13	LED1_1	25	0	LINK_10G(0X3)
AB14	LED2_0	26	2	LINK_ACT(0XC)
AA14	LED2_1	27	2	LINK_10G(0X3)
AB13	LED3_0	28	3	LINK_ACT(0XC)
AA13	LED3_1	29	3	LINK_10G(0X3)

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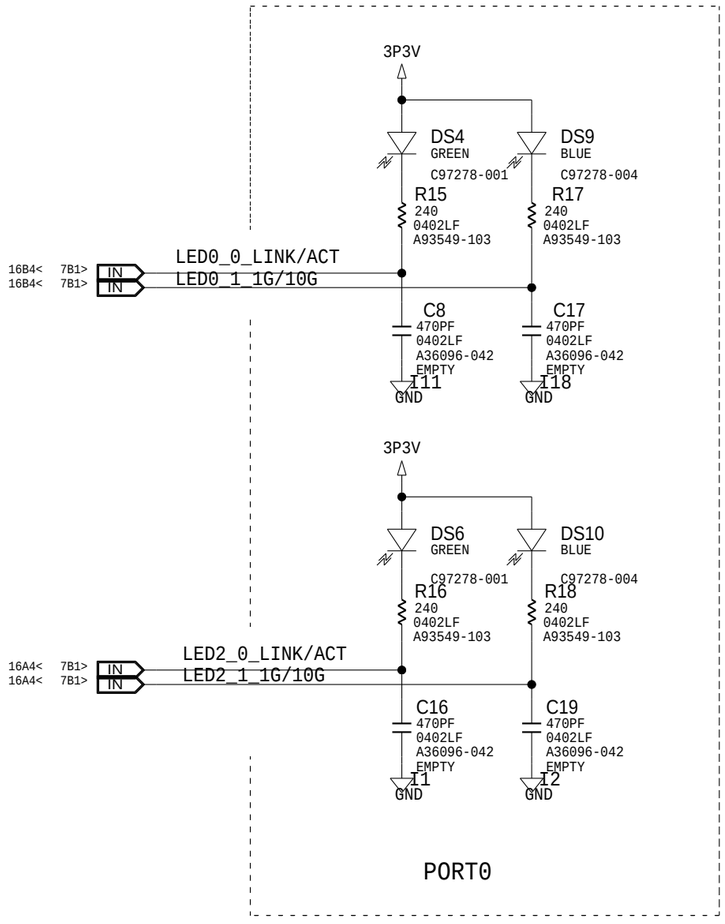
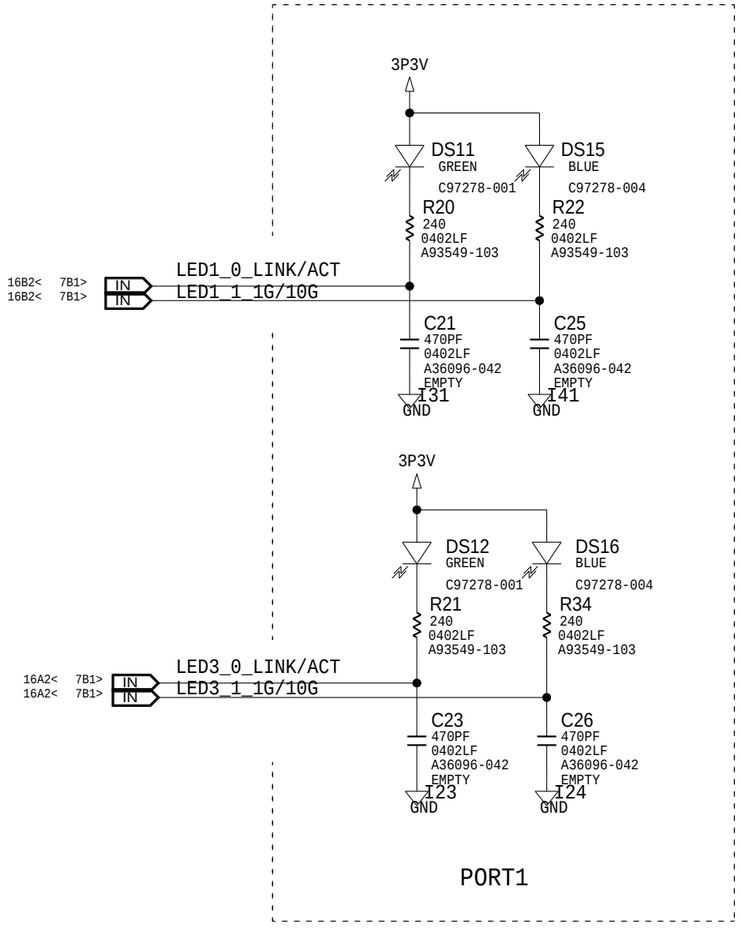
LEDS

2X40GBE

CFGID 4.5





LED SETTING	DESCRIPTION
1X40	SP 40G
2X40	DP 40G
4X10	4X10 OR 2X2X10 BREAKOUT
2X2X10	4X10 OR 2X2X10 BREAKOUT

BALL#	PIN	GPIO	LED MODE (40G + KX4)
AD14	LED0_0	22	LINK_ACT(0XC)
AC14	LED0_1	23	LINK_40G(0X2)
AD13	LED1_0	24	LINK_ACT(0XC)
AC13	LED1_1	25	LINK_40G(0X2)
AB14	LED2_0	26	LINK_10G(0X3)
AA14	LED2_1	27	LINK_1G(0X4)
AB13	LED3_0	28	LINK_10G(0X3)
AA13	LED3_1	29	LINK_1G(0X4)

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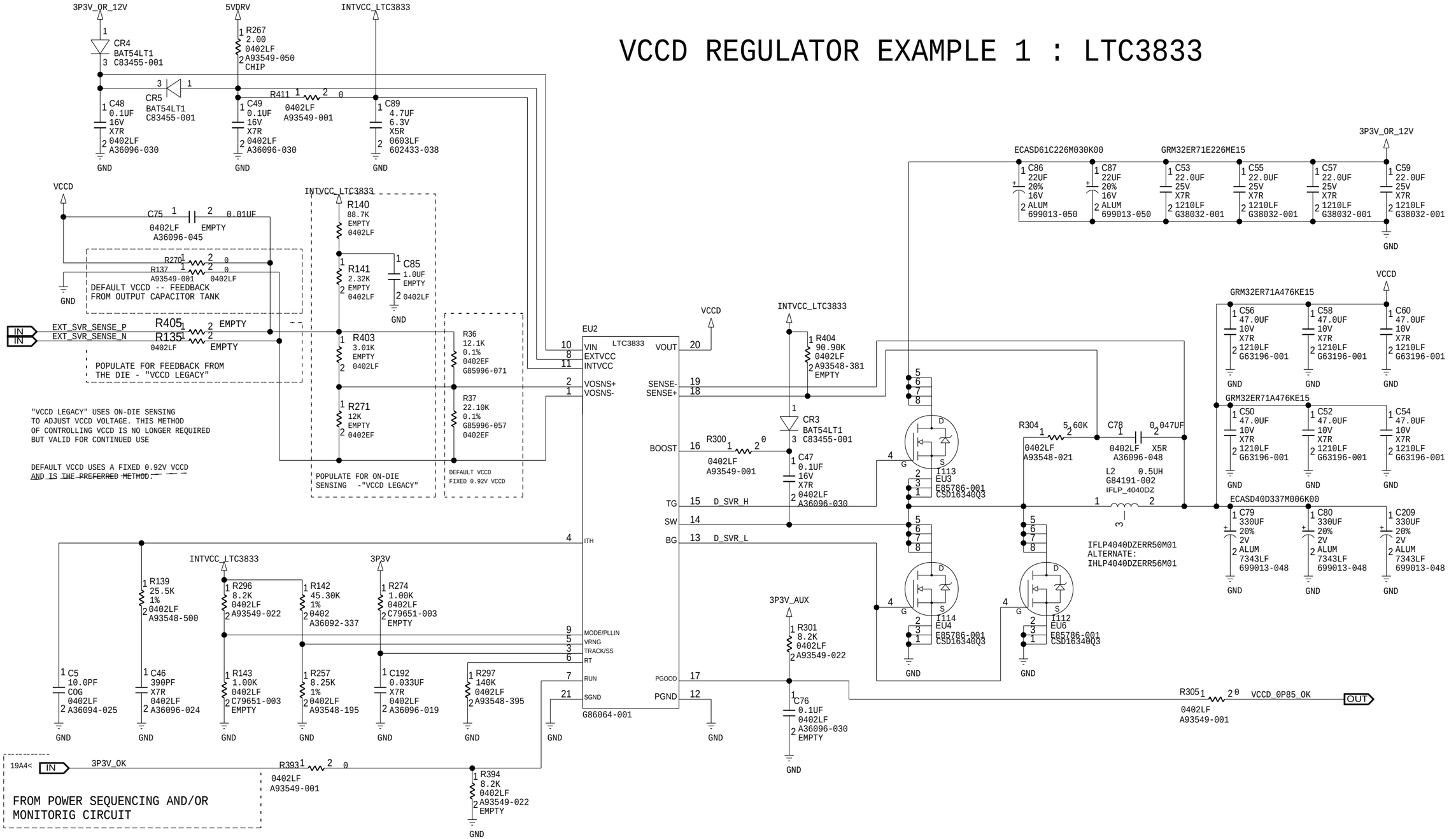
VCCD REGULATOR EXAMPLE 1 : LTC3833



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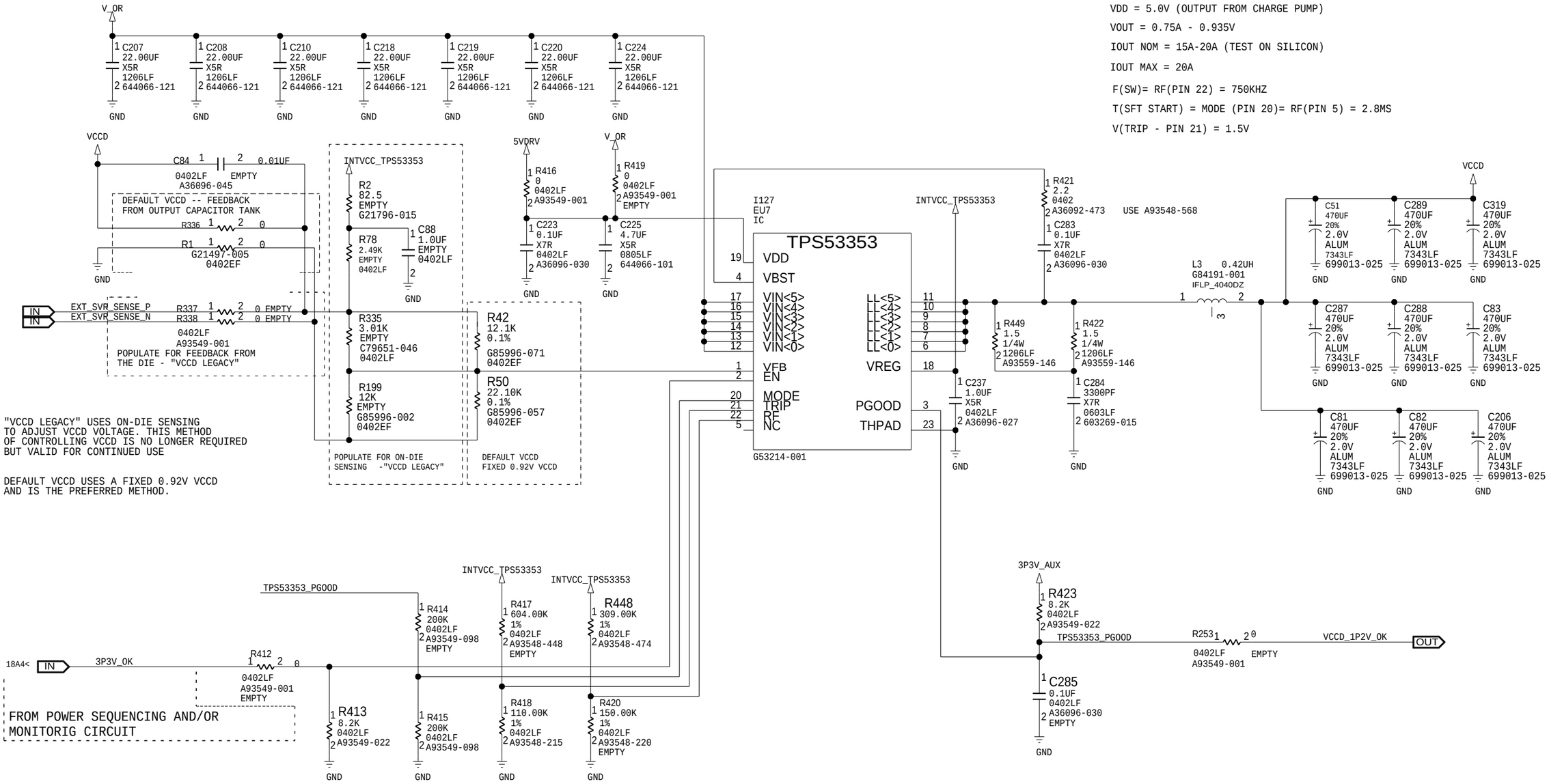
VCCD REGULATOR EXAMPLE 2 : TPS53353

VIN = 4.5V - 13.2V
VDD = 5.0V (OUTPUT FROM CHARGE PUMP)
VOUT = 0.75A - 0.935V
IOUT NOM = 15A-20A (TEST ON SILICON)
IOUT MAX = 20A
F(SW)= RF(PIN 22) = 750KHZ
T(SFT START) = MODE (PIN 20)= RF(PIN 5) = 2.8MS
V(TRIP - PIN 21) = 1.5V



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NETWORK DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE: XL710 REFERENCE SCHEMATICS	SIZE: B	CODE	DOCUMENT NUMBER	REV: 1.3	DATE: 07/26/2018	SHEET: 19