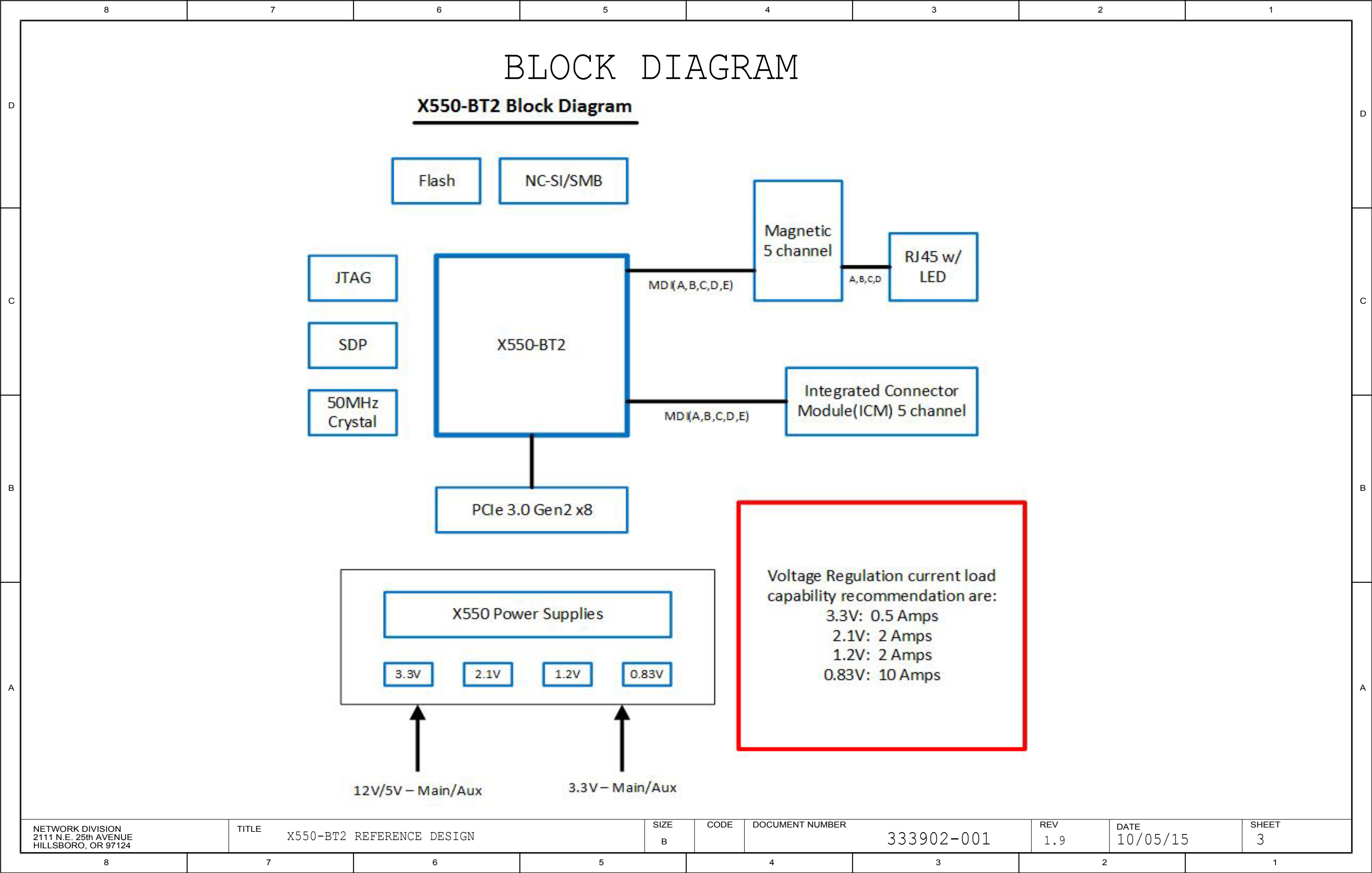


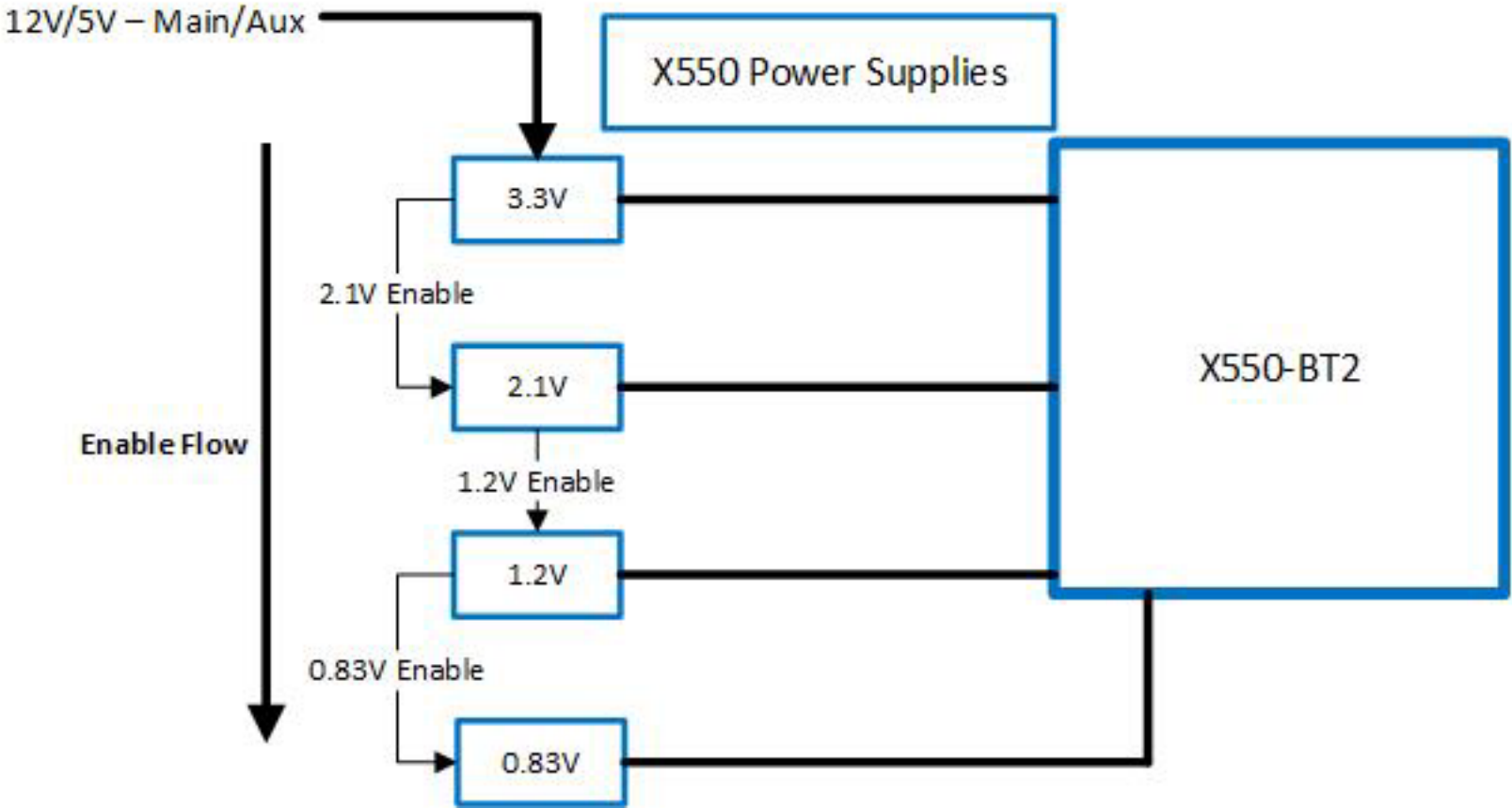
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|  | TABLE OF CONTENTS                               |                                 |   |   |   |           |      |                            |   |   |   |            |               |   |         |  |
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| C  | TITLE PAGE.....1                                |                                 |   |   |   |           |      |                            |   |   |   |            |               |   |         |  |
|  | TABLE OF CONTENTS.....2                         |                                 |   |   |   |           |      |                            |   |   |   |            |               |   |         |  |
|  | BLOCK DIAGRAM.....3                             |                                 |   |   |   |           |      |                            |   |   |   |            |               |   |         |  |
|  | POWER SUPPLY BLOCK DIAGRAM.....4                |                                 |   |   |   |           |      |                            |   |   |   |            |               |   |         |  |
|  | HOST & NETWORK INTERFACES (PCIE & BASE-T).....5 |                                 |   |   |   |           |      |                            |   |   |   |            |               |   |         |  |
|  | AUXILIARY CIRCUITRY & INTERFACES (1 OF 2).....6 |                                 |   |   |   |           |      |                            |   |   |   |            |               |   |         |  |
|  | AUXILIARY CIRCUITRY & INTERFACES (2 OF 2).....7 |                                 |   |   |   |           |      |                            |   |   |   |            |               |   |         |  |
|  | MDI INTERFACE.....8                             |                                 |   |   |   |           |      |                            |   |   |   |            |               |   |         |  |
|  | POWER SUPPLIES.....9                            |                                 |   |   |   |           |      |                            |   |   |   |            |               |   |         |  |
|  | VSS & CAPACITOR BANKS.....10                    |                                 |   |   |   |           |      |                            |   |   |   |            |               |   |         |  |
| EXAMPLE 2.1V POWER SUPPLY.....11                                 |   |                                 |   |   |   |           |      |                            |   |   |   |            |               |   |         |  |
| REVISION HISTORY.....12  |   |                                 |   |   |   |           |      |                            |   |   |   |            |               |   |         |  |
| B  |   |                                 |   |   |   |           |      |                            |   |   |   |            |               |   |         |  |
|  |   |                                 |   |   |   |           |      |                            |   |   |   |            |               |   |         |  |
| A  |   |                                 |   |   |   |           |      |                            |   |   |   |            |               |   |         |  |
|  |   |                                 |   |   |   |           |      |                            |   |   |   |            |               |   |         |  |
| NETWORK DIVISION<br>2111 N.E. 25th AVENUE<br>HILLSBORO, OR 97124 |   | TITLE X550-BT2 REFERENCE DESIGN |   |   |   | SIZE<br>B | CODE | DOCUMENT NUMBER 333902-001 |   |   |   | REV<br>1.9 | DATE 10/05/15 |   | SHEET 2 |  |
| 8  |   | 7                               |   | 6 |   | 5         |      | 4                          |   | 3 |   | 2          |               | 1 |         |  |

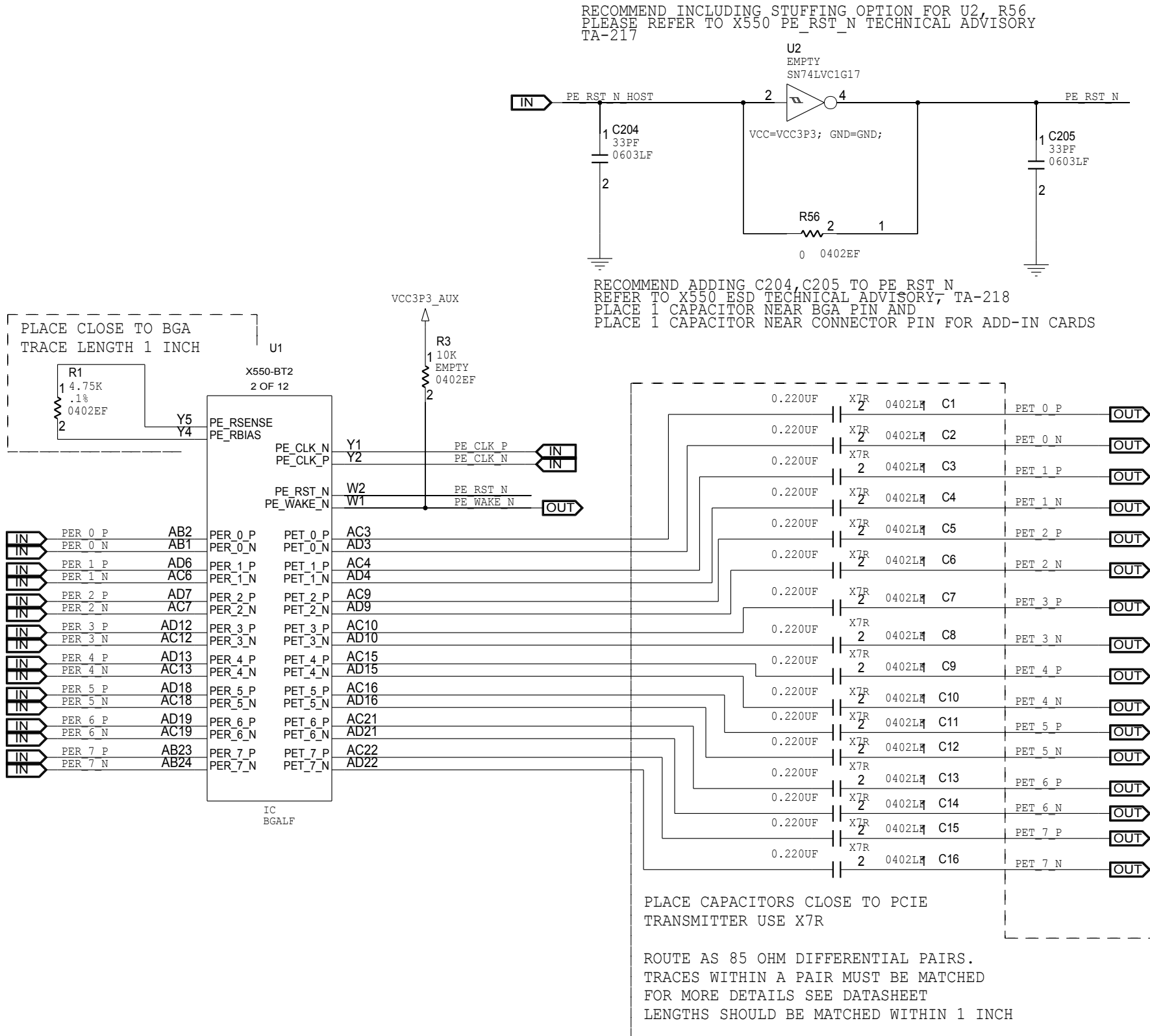
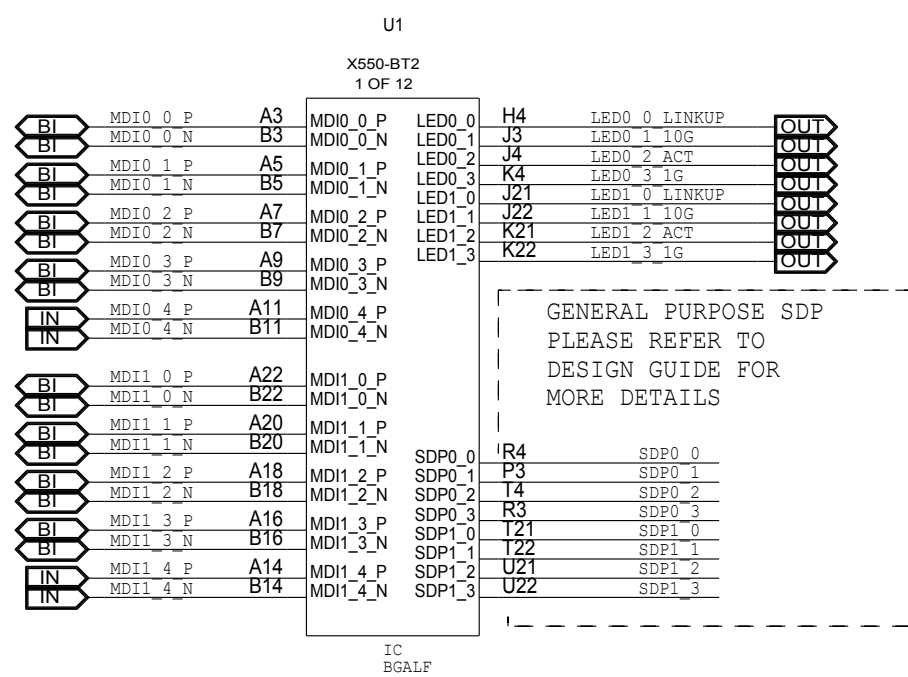


# POWER SUPPLY BLOCK DIAGRAM

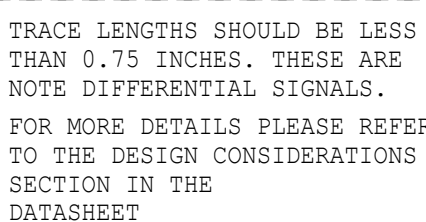
## X550-BT2 Supply Diagram

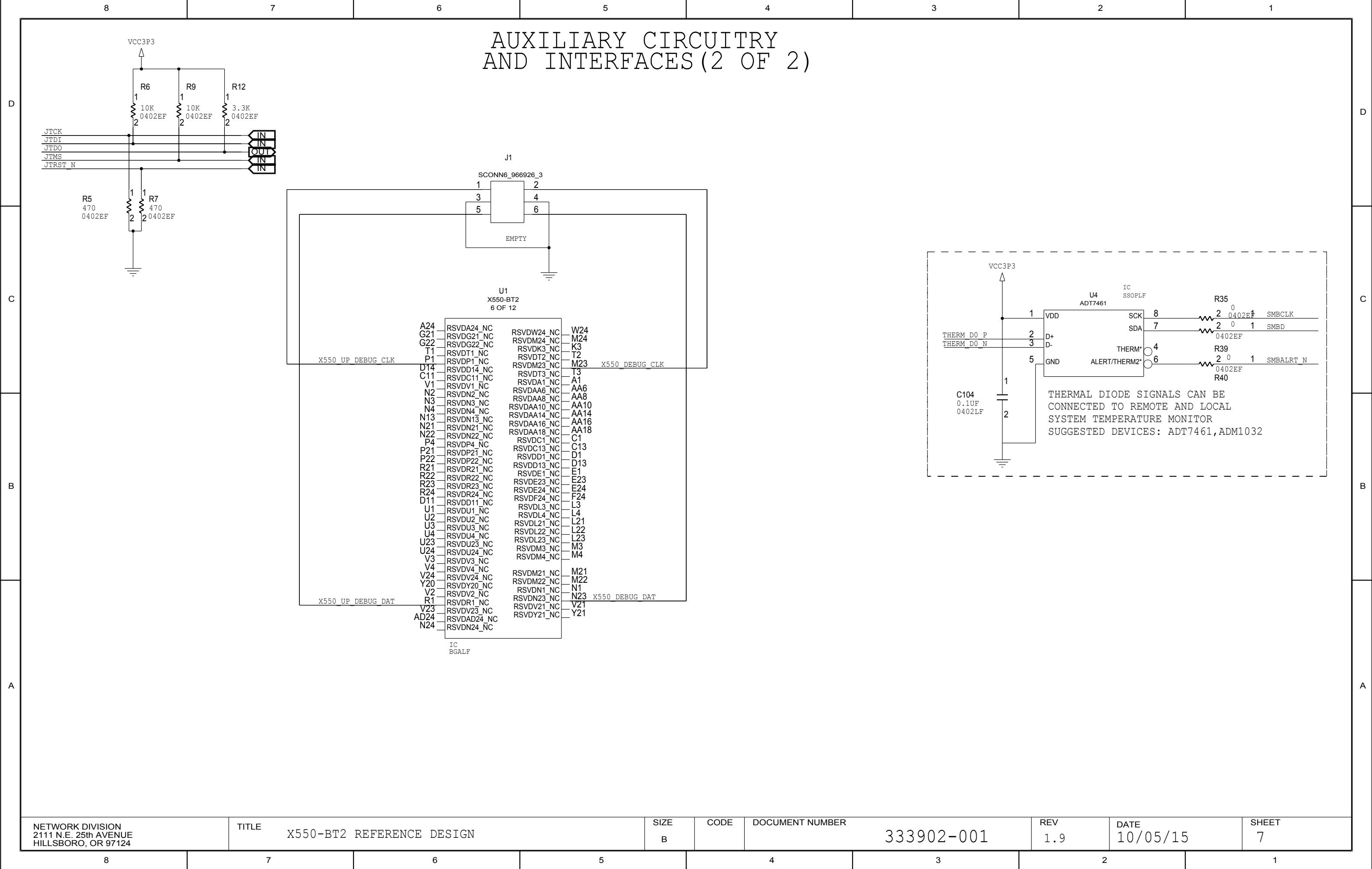


# HOST AND NETWORK INTERFACE

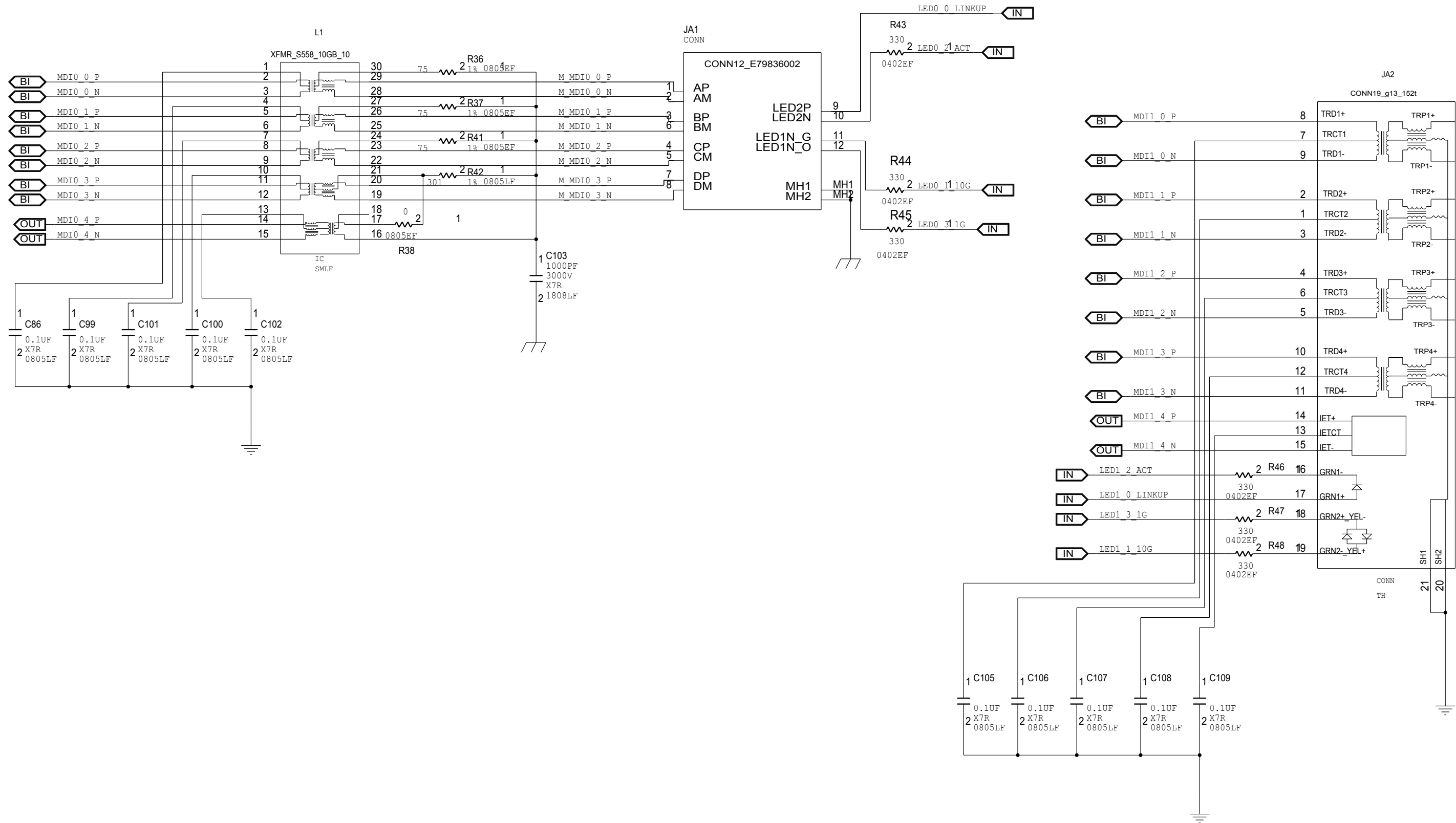


MAIN PWR OK:  
INDICATES PLATFORM POWER IS UP  
MUST BE CONNECTED EXTERNALLY



[illegible]

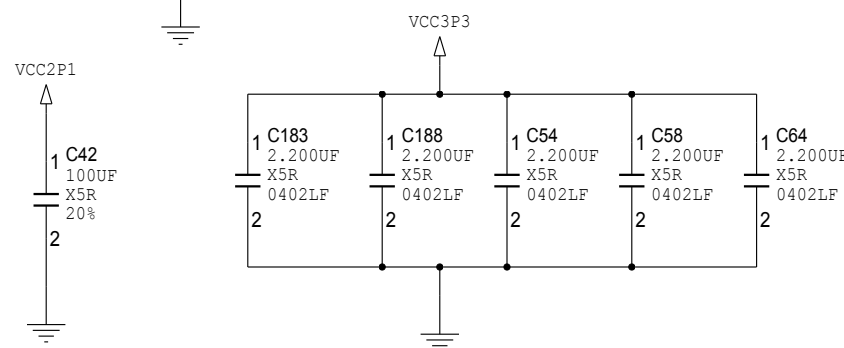
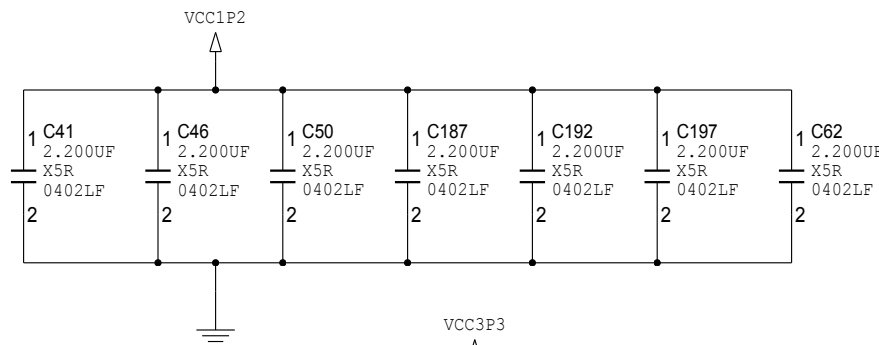
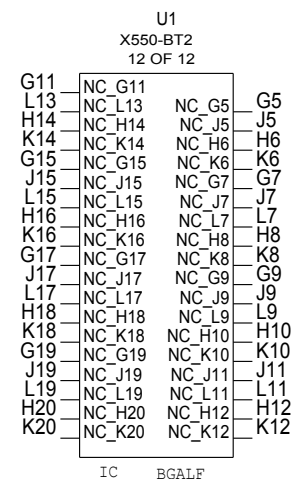
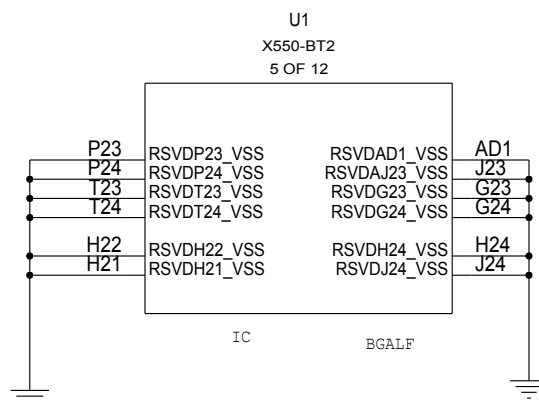
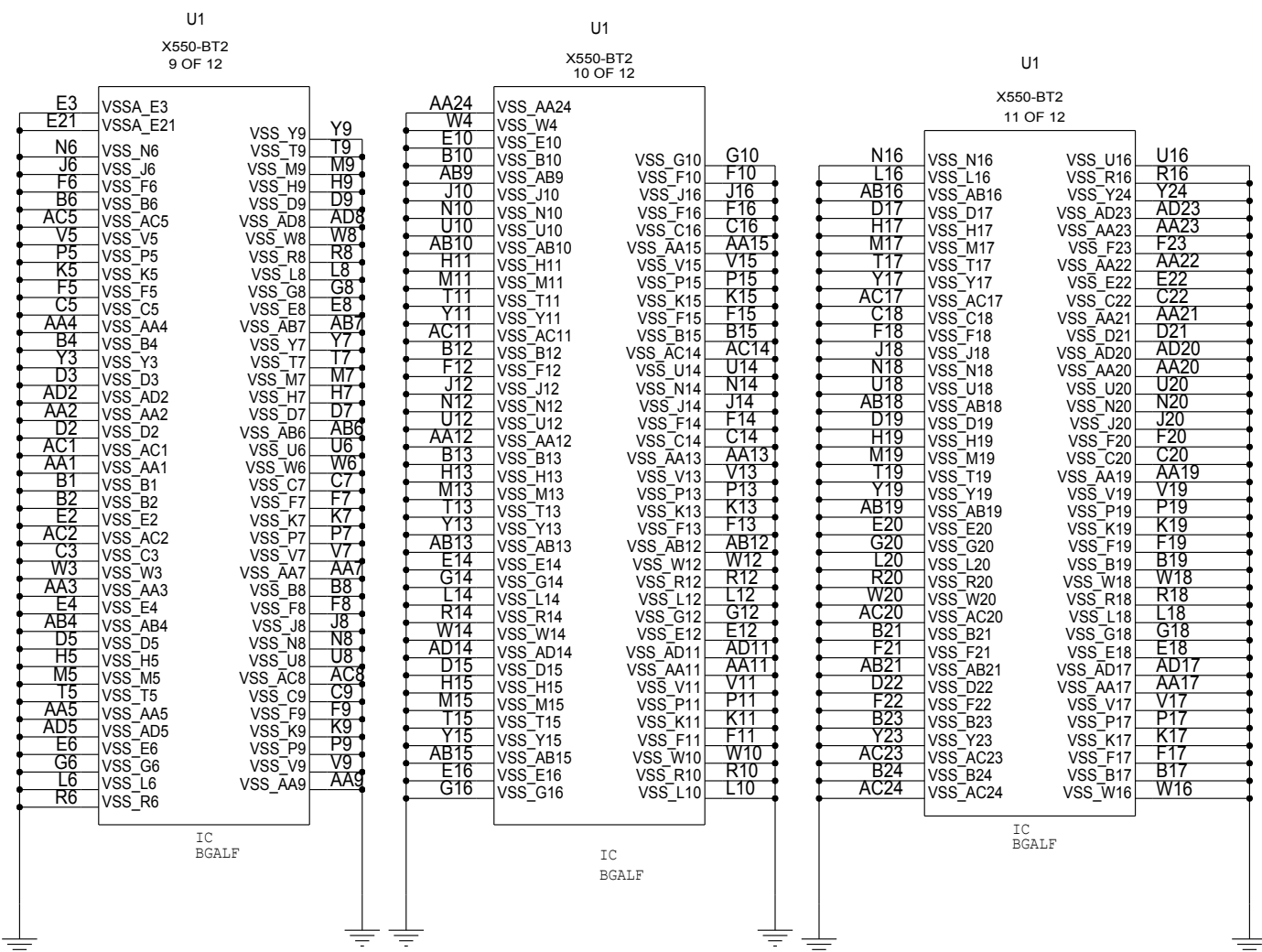
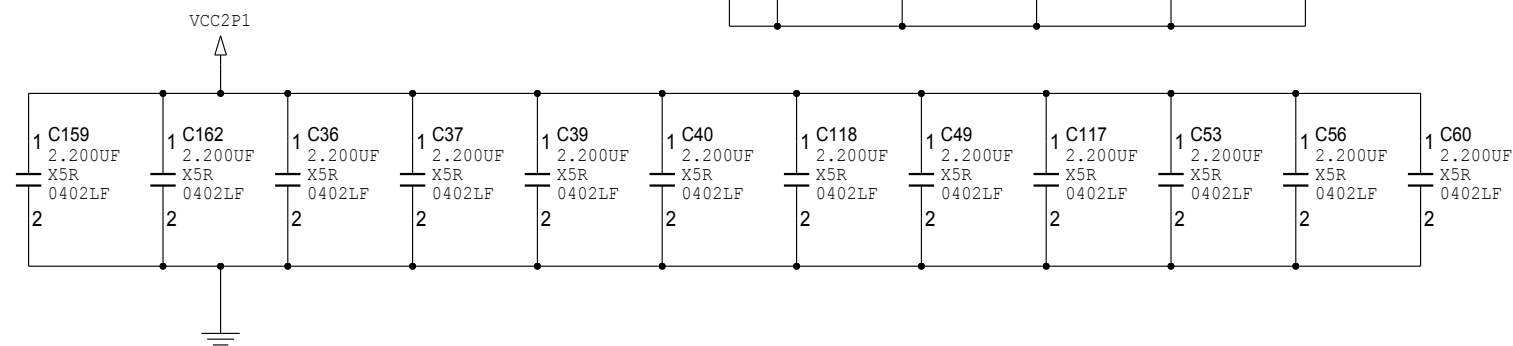
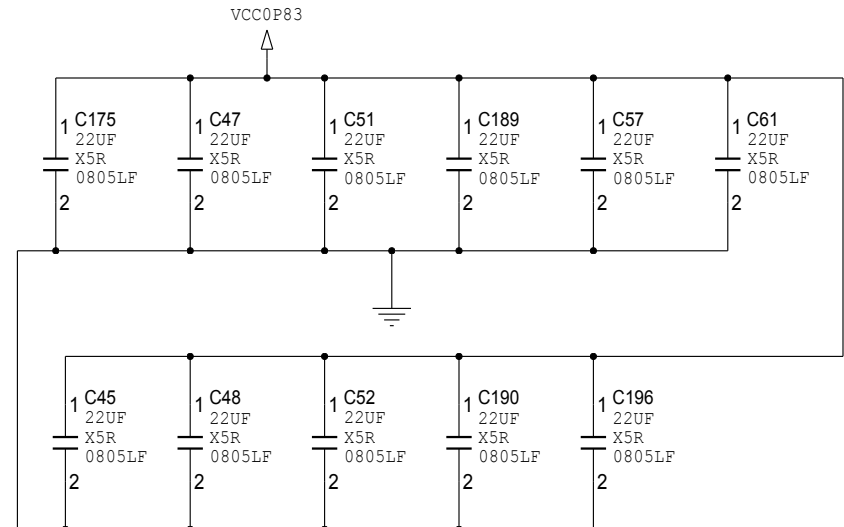
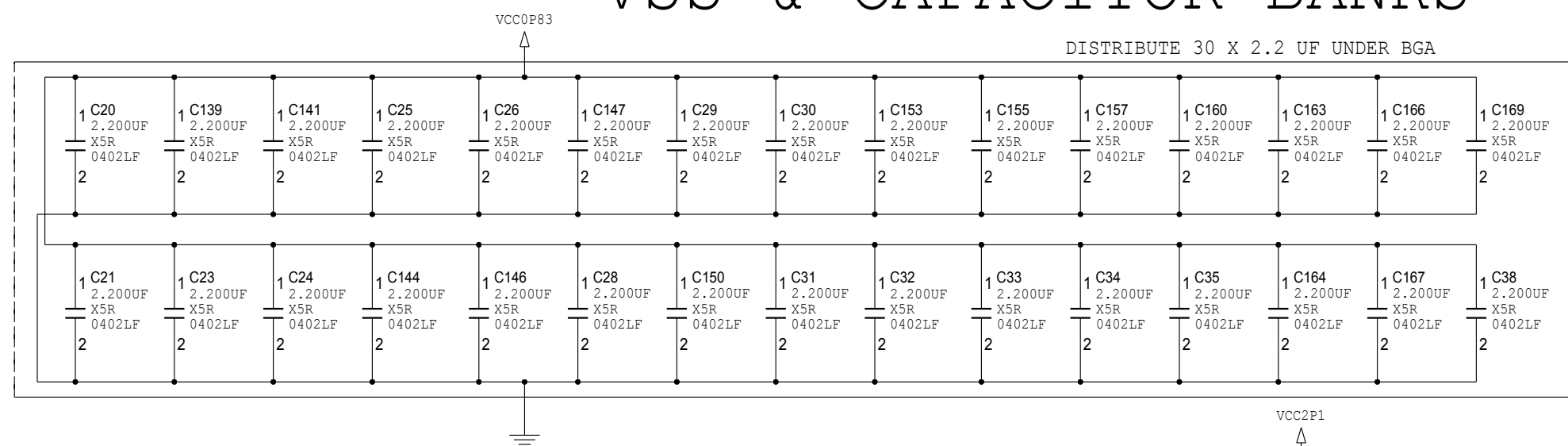
MDI INTERFACE





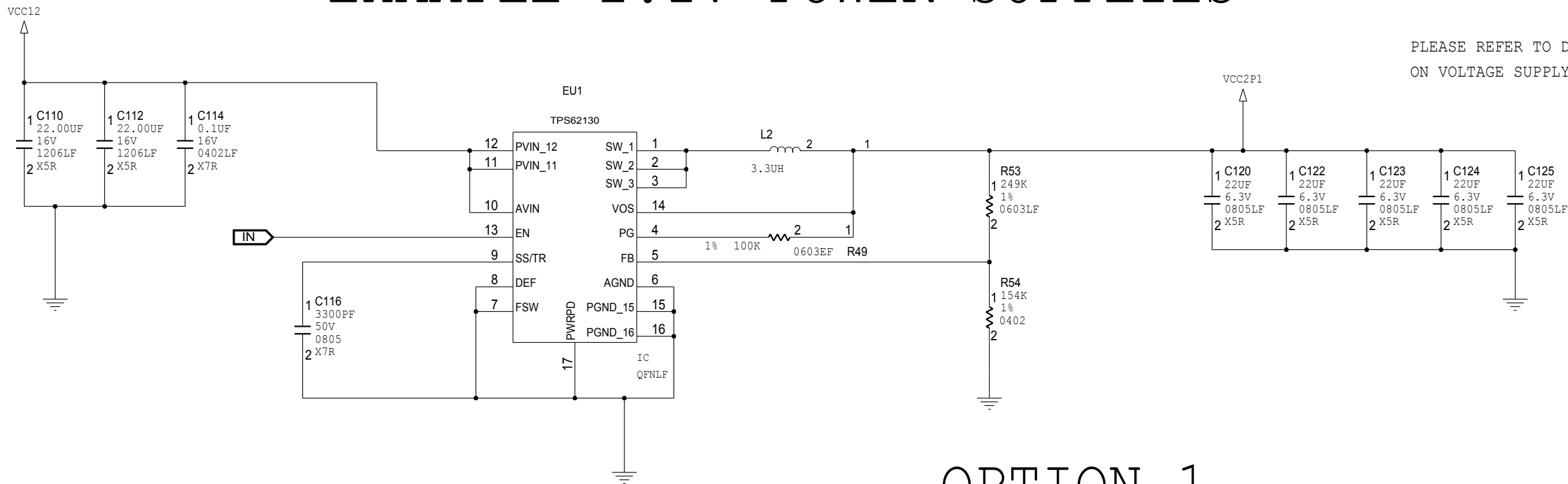


## VSS & CAPACITOR BANKS



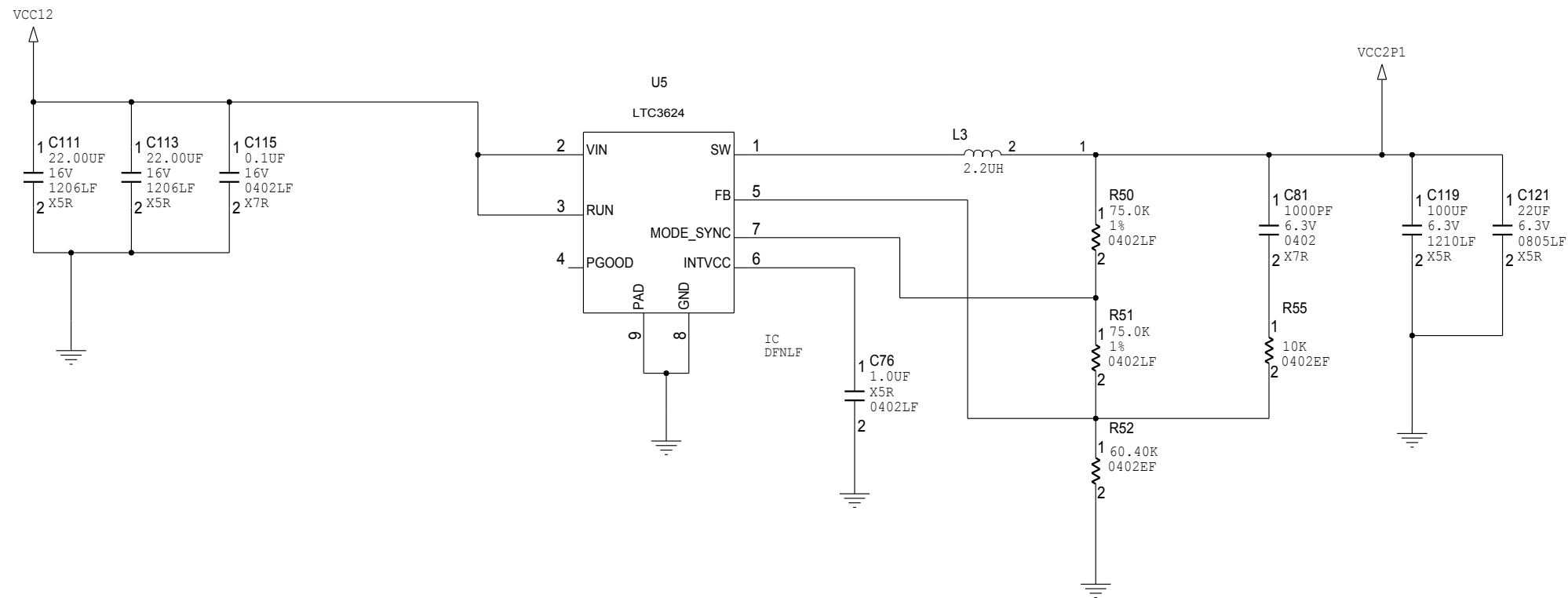
EXAMPLE 2.1V POWER SUPPLIES

PLEASE REFER TO DATASHEET FOR DETAILS  
ON VOLTAGE SUPPLY SPECIFICATIONS



OPTION 1

PLEASE REFER TO DATASHEET FOR DETAILS  
ON VOLTAGE SUPPLY SPECIFICATIONS



OPTION 2

|  |  |                                 |  |   |  |           |      |                            |  |   |            |               |  |          |  |
|--|--|---------------------------------|--|---|--|-----------|------|----------------------------|--|---|------------|---------------|--|----------|--|
| 8  |  | 7                               |  | 6 |  | 5         |      | 4                          |  | 3 |            | 2             |  | 1        |  |
| REVISION HISTORY   |  |                                 |  |   |  |           |      |                            |  |   |            |               |  |          |  |
| 0.5.....INITIAL RELEASE  |  |                                 |  |   |  |           |      |                            |  |   |            |               |  |          |  |
| 0.51.....CORRECTED FLASH VCC, UPDATED RSVDXXX_VSS PINS   |  |                                 |  |   |  |           |      |                            |  |   |            |               |  |          |  |
| 0.52.....ADDED BYPASS CAPACITORS   |  |                                 |  |   |  |           |      |                            |  |   |            |               |  |          |  |
| 0.55.....REMOVED A0 PE_WAKE_N CIRCUITRY, REFER TO TECHNICAL ADVISORY, ADDED 100 UF BYPASS TO VCC0P83         |  |                                 |  |   |  |           |      |                            |  |   |            |               |  |          |  |
| CHANGED VCC0P85 TO VCC0P83, CHANGED PIN M1 FROM SEC_EN TO ENCRYPTION_EN, CORRECTED NCSI STUFFING OPTIONS     |  |                                 |  |   |  |           |      |                            |  |   |            |               |  |          |  |
| 1.9.....CORRECTED VCC0P85 NET TO VCC0P83. ADDED DEBUG HEADER, ADDED DEBUG MODE STUFFING OPTION, ADJUSTED THE |  |                                 |  |   |  |           |      |                            |  |   |            |               |  |          |  |
| LAN_DIS_N PULL UP VALUES, ADDED PE_RST_N SCHMITT TRIGGER OPTION, ADDED PE_RST_N ESD SHUNT CAPACITIVE FILTER  |  |                                 |  |   |  |           |      |                            |  |   |            |               |  |          |  |
| NETWORK DIVISION<br>2111 N.E. 25th AVENUE<br>HILLSBORO, OR 97124   |  | TITLE X550-BT2 REFERENCE DESIGN |  |   |  | SIZE<br>B | CODE | DOCUMENT NUMBER 333902-001 |  |   | REV<br>1.9 | DATE 10/05/15 |  | SHEET 12 |  |
| 8  |  | 7                               |  | 6 |  | 5         |      | 4                          |  | 3 |            | 2             |  | 1        |  |