Intel® 82579 Gigabit Ethernet Controller Checklists v2.0

LAN Access Division (LAD)

Project Name	
Fab Revision	
Date	
Schematic Designer	
Layout Designer	
Intel Contact(s)	
Reviewer(s)	

Revision	Date	Changes
1.1	January-10	Replaced 10 µF capacitor with 0 W resistor.
1.2	January-10	Reworded majority of layout guidance for clarity Relaxed restrictions on crystal layout placement guidance Clarified which PCIe pins have to be connected. Updated JTAG guidance. Reworded different sections of the schematic guidance for clarity. Better explained the two 1.05V power delivery options.
1.3	May-10	Updated 1.05 Vdc decoupling requirement to 20 uF min & 3.3 Vdc decoupling requirement to 22 uF min. Updated the oscillator connection requirements. (6.8 pF series cap) Updated iSVR inductor selection requirements
2.0	May-11	Removed pull-up resistor for LAN-DISABLE signal. Converted to PDF Form for public distribution.

Rev 2.0; 325261-002EN

NOTE: Adobe* Reader* version 8 or above must be used in order to save your input to this form electronically.
To update, the latest Reader application is available for free download at http://get.adobe.com/reader/.

82579 Schematic Checklist v2.0

SECTION	CHECK ITEMS	REMARKS	DONE (check)	NOTES
General	Obtain the most recent documentation and specification updates.	Documents can be subject to frequent changes made without notice.		
	This checklist is intended to be used in conjunction with the Customer Reference Board (CRB) reference schematics.			
	The instructions for special pins needing pull-up or pull-down resistors should be followed carefully to ensure proper operation.			
	For further LAN/platform information, refer to the appropriate Platform Design Guides. For integrated GbE LAN (MAC) detail, refer to the PCH EDS, and Specification Updates.			
Support Pins	Connect TEST_EN (pin 30) through a 1 kΩ pull-down resistor.			
	Connect LAN_DISABLE_N (pin 3) to a 10 kΩ no-stuff pull-up resistor to 3.3 Vdc and a 10 kΩ no-stuff pull-down resistor to ground and then connect to PCH pin LAN_PHY_PWR_CTRL through a 0 Ω resistor. Make sure to connect to PCH pin LAN_PHY_PWR_CTRL through a 0 Ω resistor.	This is mandatory for all 82579 designs.		
	Connect RBIAS (pin 12) to a 3.01 kΩ 1% pull-down resistor.			
	Connect RSVD_VCC3P3 (pin 1) and RSVD_VCC3P3 (pin 2) to a 4.7 kΩ 5% pull-up resistor to 3.3 Vdc.	A range of 3 kΩ to 10 kΩ can also be used.		
	Connect the VSS_Epad (pin 49) to ground plane.	Refer to the platform design guides (PDG) for more information.		
PCIe Interface	Connect PETn (pin 39) and PETp (pin 38) to PERn6 and PERp6 respectively.	The PCIe interface pins can be connected to any available PCH PCIe port. This checklist only refers to port 6 as the default connection.		
	Connect PERn (pin 42) and PERp (pin 41) to PETn6 and PETp6 respectively.			
	Place AC coupling capacitors (0.1 µF) near the PCIe transmitter.	Size 0402, X7R is recommended.		
	Connect PE_CLKn (pin 45) and PE_CLKp (pin 44) to CLKOUT_PCIE5N and CLKOUT_PCIE5P, respectively.	The PCIe* clock buffer can be connected to any clock port. It does not have to match the same port used for the PCIe lanes.		

82579 Schematic Checklist v2.0

SECTION	CHECK ITEMS	REMARKS	DONE (check)	NOTES
PCIe Interface *(cont.)*	**Mobile platforms only** Connect CLK_REQ_N (pin 48) through a 10 kΩ pull-up resistor to 3.3 Vdc and then through a series 0 Ω resistor to PCH pin PCIECLKRQ5#. **All non-mobile Platforms** Connect CLK_REQ_N (pin 48) through a 10 kΩ pull-up resistor to 3.3 Vdc and then add an empty series 0 Ω resistor to PCH pin PCIECLKRQ5#.	CLK_REQ_N can be connected to one of the eight PCH inputs (PCIECLKRQ[7:0]#). If connecting this PHY output to the PCIECLKRQ1# or PCIECLKRQ2# pins (powered by the core well), the pull-up resistor needs to be connected to the +V3.3S rail. If connecting to any of the other PCIECLKRQ# pins (powered by Sus well), the pull-up resistor needs to be connected to the +V3.3A rail. The CLK_REQ_N port number can be mapped to any PCIe clock out port using the ME configuration tab in the FITC tool.		
	Connect PE_RST_N (pin 36) through a series 0 Ω resistor to PCH PLTRST#.			
SMBus	Connect 2.2 kΩ 5% pull-up resistors (3.3Vdc) to SMB_CLK (pin 28) and SMB_DATA (pin 31).	Ensure pull-ups are connected to the power rail that is present while in Sx states and while transitioning from G3 to S5. Note that the PHY SMBus address is 0xC8 and default MAC SMBus address is 0xE0.		
	Connect SMB_CLK (pin 28) and SMB_DATA (pin 31) to PCH SML0CLK and SML0DATA, respectively.	The PCH has a dedicated SMBus for the PHY (SMBus channel 0). No other device (such as an external BMC) can be connected to SML0CLK or SML0DATA.		
Clock Source (Crystal Option)	Use a 25 MHz 30 ppm accuracy @ 25 °C crystal. Avoid components that introduce jitter.	Parallel resonant crystals are required. The calibration load should be 18 pF. Specify Equivalent Series Resistance (ESR) to be 50 Ω or less. Avoid PLL clock buffers. Refer to 82579 datasheet for Crystal Specifications. Please provide a crystal datasheet to Intel representative for review.		
	Connect two load capacitors to the crystal; one on XTAL_OUT (pin 9) and one on XTAL_IN (pin 10). Use 33 pF capacitors as a starting point, but be prepared to change the value based on testing.	Capacitance affects accuracy of the frequency and must be matched to crystal specifications, including estimated trace capacitance in calculation. Use capacitors with low ESR (types C0G or NPO, for example). Refer to the Datasheet and the Intel Ethernet Controllers Timing Device Selection Guide for more information.		
	Connect a series 0 Ω resistor to the XTAL_OUT (pin 9).			

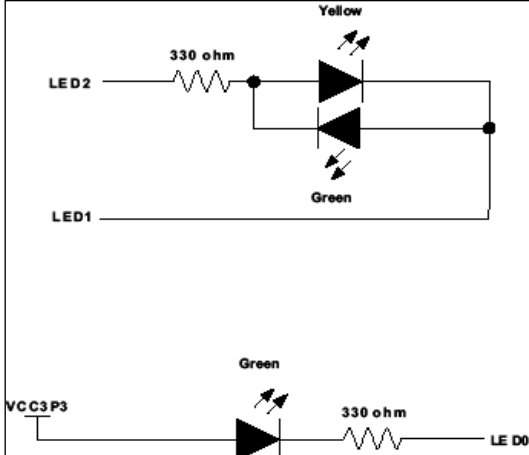| 82579 Schematic Checklist v2.0				
SECTION	CHECK ITEMS	REMARKS	DONE (check)	NOTES
Clock Source (Crystal Option) *(cont.)*	Connect XTAL_IN (pin 10) and XTAL_OUT (pin 9) to the appropriate crystal pins.			
Clock Source (Oscillator Option)	Connect the output of the clock oscillator to pin XTAL_IN (pin 10) through a 6.8 pF coupling capacitor (capacitance-coupled voltage divider). Do not connect XTAL_OUT (pin 9). Place the 6.8pF capacitor near the XTAL_IN of the PHY (less than 325 mils).	Use a 25 MHz 50 ppm oscillator. The oscillator needs to maintain 50 ppm under all applicable temperature and voltage conditions. Avoid PLL clock buffers. Refer to the 82579 datasheet for oscillator specifications. Refer to the Platform Design Guide for details about the signal conditioning circuit.		
	Use a local decoupling capacitor on the oscillator power supply. Include a bulk 1 µf capacitor as well as a high frequency 0.1 µf decoupling capacitor.	If isolated with a ferrite bead, include a bulk decoupling capacitor next to the oscillator. Refer to the PDG for more details.		
	The signal from the oscillator must be AC coupled into the 82579.	The input common mode voltage is set internally by the 82579.		
	If the oscillator driver is more than two inches away, add a 33 Ω series resistor directly at the output.			
3.3V Rail	Provide a 3.3 Vdc supply. Use the power rail that is present while in Sx states and while transitioning from G3 to S5.	This is necessary to support wake up from power down states.		
	Place a 22 uF cap and a 0.1 uF cap on the 3.3 V LAN rail near the PHY.	The previous guidance was to place two 10 uF caps with one being unstuffed, along with the 0.1 uF cap. After completing validation it was determined that a 22 uF cap and a 0.1 uF cap are needed.		
	Place a 1 uF cap to ground near the 3.3 V output (pin 4) of the PHY and connect the 3.3V output (pin 4) with the three inputs together. (VDD3P3_15, VDD3P3_19, VDD3P3_29)			

82579 Schematic Checklist v2.0

SECTION	CHECK ITEMS	REMARKS	DONE (check)	NOTES
1.05V Rail	Option#1: Using internal SVR from 82579 Connect a 4.7 uH inductor to the CTRL_1P0 output pin of the PHY and connect the other side of the inductor to the 1.05 V input to the PHY (Pin 8, 11, 16, 22, 37, 40, 43, 46, 47)	Using the integrated SVR of the PHY is the simplest design. The 4.7 uH inductor must be a power type inductor. At the maximum current load (~320 mA) the inductance must not drop below 3.9 uH. DCR of inductor should be less or equal to 100 mΩ. Most 20% inductors should be ok but make sure to verify against the datasheet. Inductor Testing Frequency should be near to 82579's iSVR operating frequency (~1.5MHz). For more details on how to select the 4.7 uH inductor, please refer to IBL ref # 448737 -Intel(R) 82579LM Gigabit Ethernet PHY Inductor Selection Guide - Application Note - Rev 1.0.		
	Option#2: Using output of the PCH 1.05V SVR as power input to the PHY. This power rail should be controlled by SLP_LAN#. Connect VDD1P0 (Pin 8, 11, 16, 22, 37, 40, 43, 46, 47) to the PCH 1.05 Vcc Switching Voltage Regulator (SVR). CTRL_1P0 should be left as no connect. NOTE: If sharing the PCH 1.05 Vdc as the input to the PHY then make sure that SLP_LAN# controls both the 3.3 V and 1.05 V input to the PHY. Also, make sure layout requirements are met for trace length calculation.	If SLP_LAN# is not used to control both power inputs then there will be unexpected behavior. For implementing both 1.05V power delivery options for validation refer to the latest reference schematic.		
	Place a 22 uF capacitor or two 10 uF and a 0.1 uF capacitors near the 1.05 V input to the PHY (VDD1P0). This is the same for both power delivery options.	Please note that the 20 uF is the <u>minimum</u> recommended decoupling value to use. Since a 20 uF cap value may not be available, either a single 22 uF or two 10 uF capacitors can be used.		
Magnetics	Qualify magnetic modules carefully for return loss, insertion loss, open circuit inductance, common mode rejection, and crosstalk isolation.	Magnetics module is critical to passing IEEE PHY conformance tests and EMI test. Refer to the 82579 Datasheet for magnetics requirements. Please provide a magnetics datasheet to your Intel® representative.		

82579 Schematic Checklist v2.0

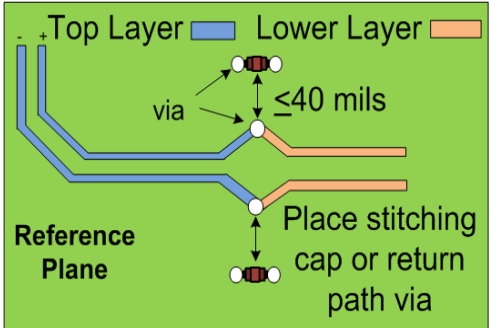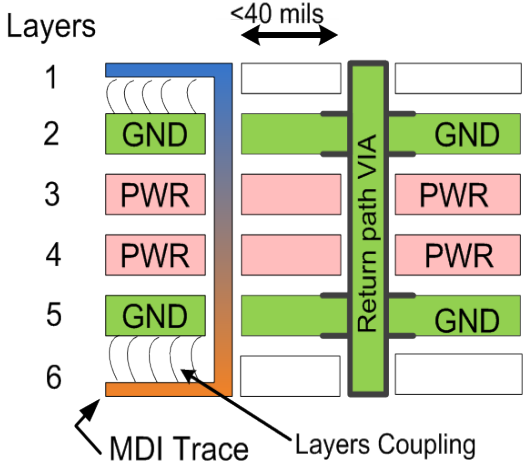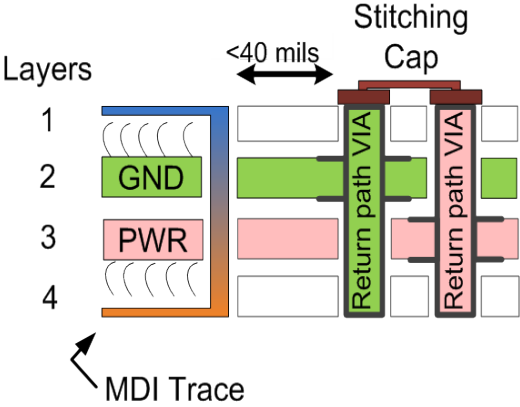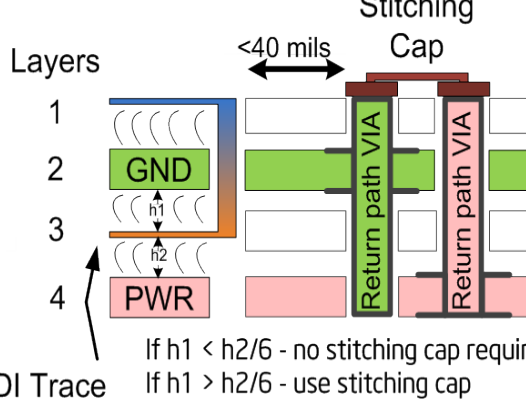| SECTION	CHECK ITEMS	REMARKS	DONE (check)	NOTES
Magnetics (cont.)	On the magnetics center tap, use 0.1 µF bypass capacitors. Connect to ground through a 1 µF bulk decoupling capacitor placed near the magnetics center tap input to the transformer. Mobile only - If a docking station is used make sure the docking station magnetics center tap also use 0.1 µF bypass capacitors and connects to ground through a 1 µF bulk decoupling capacitor. The 1 µF capacitor should be placed near the docking station magnetics center tap input to the transformer.	Ceramic capacitors with low ESR should be used. **Note:** Some integrated magnetics assemblies have local decoupling (0.1 µF) integrated into the part.		
	Bob Smith termination: If the RJ-45 connector does not have integrated Bob Smith termination, use 4 x 75 Ω resistors for cable-side center taps and unused pins. Use a high-voltage isolation capacitor attached to the termination plane. A suggested value is 1500 pF/3 KV.	Terminate pair-to-pair common mode impedance of the CAT5 cable. If the discrete magnetics already has Bob Smith termination, then there is no need to add. **Note:** Some integrated magnetics assemblies have Bob Smith termination integrated into the part. Name the net of the common connection between the 75 Ω resistors and high-voltage isolation capacitor so it can be used as a reference plane.		
MDI Termination	The 82579 has internal termination for the MDI. No external termination is required.	If leveraging an existing 82578 design make sure to remove the MDI termination before using the 82579.		
Chassis Ground (10/100/1000Base-T interface)	If possible, provide a separate chassis ground to connect the shroud of the RJ-45 connector and to terminate the line side of the magnetic module.	This design improves EMI behavior. Also, if using integrated magnetics with USB, do not isolate ground for RJ45.		
	Place pads for approximately 4-6 "stitching" capacitors to bridge the gap from chassis ground to signal ground.	Typical values range from 0.1µF to 4.7 µF. The correct value should be determined experimentally.		

82579 Schematic Checklist v2.0

SECTION	CHECK ITEMS	REMARKS	DONE (check)	NOTES
LED Circuits	Basic recommendation is a single green LED for Activity and a dual (bi-color) LED for Speed. Many other configurations are possible. LEDs are configurable through the NVM.	Two LED configuration is compatible with integrated magnetic modules. • For Link/Activity (green) LED, connect the cathode to the LED0 pin and the anode to VCC. • For the link-speed (bi-color; green and yellow) LED, one end is driven by the LED2 signal and the other end is driven by the LED1 signal. When LED2 is low, the 100 Mb/s (green) LED is lit. When LED1 is low the 1000 Mb/s (yellow) LED is lit.		
	Connect LEDs to 3.3 Vdc as indicated in reference schematics.	Use the power rail for designs supporting wake-up (present in Sx states and G3 to S5 transition). Consider adding one or two filtering capacitors per LED for extremely noisy situations. Suggested starting value is 470 pF.		
	Add current limiting resistors to LED paths.	Typical current limiting resistors are 250 Ω to 330 Ω when using a 3.3 Vdc supply. Current limiting resistors are typically included with integrated magnetic modules.		
Miscellaneous	PCH output pin SLP_LAN#, can be used to gate power rails that do not need to be on when host WoL and manageability hardware are disabled.	Specific configurations that leave power on/off depending on WoL and manageability hardware settings are design dependent. Refer to the *Intel® PCH Family External Design Specification* (PCH EDS) for more details.		
	PCH pin LAN_RST#, MEPWROK, and SYSPWROK timing requirement needs to be met.	Refer to the PCH EDS for more details on LAN_RST#, MEPWROK, and SYSPWROK timing requirements.		
	Mobile platforms only. For designs that support docking stations, use a LAN switch to reduce stub length on the MDI interface between the local RJ-45 and the docking station and verify the MDI connections are correct.	Stubs on the MDI interface in systems with a local RJ-45 and a docking connector causes IEEE conformance test failures. The LAN switch disconnects the unused interface, which improves IEEE performance.		
	Leave an empty site for a TVS device between the RJ-45 and the magnetics assembly.	TVS diodes can be added to the MDI for additional ESD protection.		

82579 Schematic Checklist v2.0

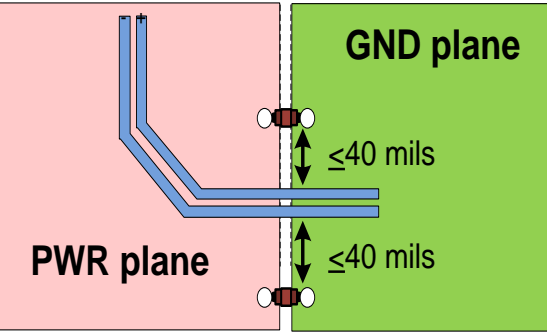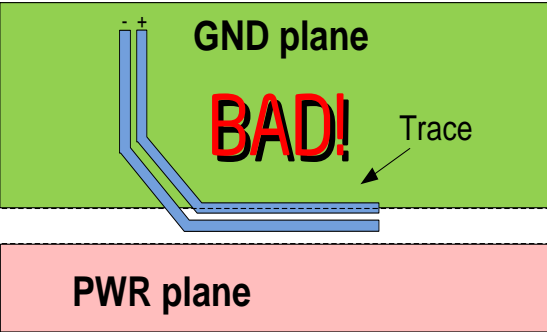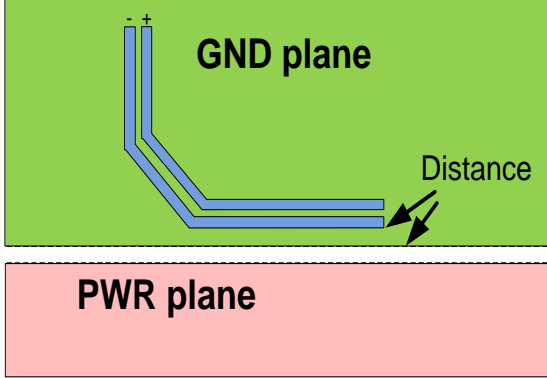| SECTION	CHECK ITEMS	REMARKS	DONE (check)	NOTES
Miscellaneous (cont.)	Pin 6 is reserved, keep it no connect.			
Mfg Test	The 82579 allows a JTAG Test Access Port.	Because of pin sharing, the 82579 cannot be used in a JTAG chain. The JTAG pins must be individually driven and sampled.		
	JTAG_TMS and JTAG_TCK should be pulled up to 3.3V with a 10 kΩ that is unstuffed. Route JTAG_TDI and JTAG_TDO to test points.	The 10 kΩ pull up resistors may have to be added when using a Test Access Port (TAP) controller.		

82579 Layout Checklist v2.0

SECTION	CHECK ITEMS	REMARKS	Done (check)	NOTES
General	Obtain the most recent documentation and specification updates.	Documents are subject to frequent change.		
	Route the transmit and receive differential traces before routing the digital traces. Following the design guide, route the differential PCIe and MDI traces first relative to other traces on the board. Then route the clock traces.	Layout of differential traces is critical.		
	IMPORTANT: All impedance controlled signals should be routed in reference to a solid plane. If there are plane splits on a reference layer and the signal traces cross those splits then stitching caps should be used within 40 mils of where the crossing occurs.

If signals transition from one reference layer to another reference layer then stitching caps or connecting vias should be used based on the following.

If the transition is from power referenced layer to ground referenced layer or from one voltage power referenced layer to a different voltage power referenced layer then stitching caps should be used within 40 mils of the transition.

If the transition is from one ground referenced layer to another ground referenced layer or is from a power referenced layer to the same net power referenced layer then connecting vias should be used within 40 mils of the transition. | These are especially important on single ended signaling such as the crystal/oscillator clocking. It is also very important for the MDI differential signaling.

If stitching caps or connecting vias are not used then it will increase the probability of having EMI issues, ESD immunity, and may have some IEEE test conformance issues.

If this is not followed for single ended signaling (such as the crystal/oscillator trace) then the 25Mhz crystal may broadcast as EMI as well as pick up noise potentially causing jitter and BER issues with longer Ethernet cables.

If the bus has several signals or differential pairs it may not be possible to place a single stitching cap or connecting via within 40 mils of all of the signals. In this case multiple stitching caps or connecting vias should be used. | | |

82579 Layout Checklist v2.0

SECTION	CHECK ITEMS	REMARKS	Done (check)	NOTES
General *(cont.)*	**Transitioning Reference Layers** Top Layer / Lower Layer via / ≤40 mils Reference Plane / Place stitching cap or return path via **Return path via's with stitching cap connecting two planes on different nets** Layers / <40 mils / Stitching Cap 1 / 2 GND / 3 PWR / 4 Return path VIA / Return path VIA MDI Trace Layers / <40 mils / Stitching Cap 1 / 2 GND / 3 / 4 PWR Return path VIA / Return path VIA MDI Trace h1 / h2 If h1 < h2/6 - no stitching cap required If h1 > h2/6 - use stitching cap	**Return path via connecting two planes on the same net** Layers / <40 mils 1 2 GND / GND 3 PWR / PWR 4 PWR / PWR 5 GND / GND 6 Return path VIA MDI Trace / Layers Coupling		

82579 Layout Checklist v2.0

SECTION	CHECK ITEMS	REMARKS	Done (check)	NOTES
General (cont.)	**Crossing Plane Splits Use Stitching Caps** GND plane ≤40 mils PWR plane ≤40 mils **Do NOT split diff pair along plane edge** GND plane BAD! Trace PWR plane **Keep enough distance from trace edge to plane edge on adjacent layer** - + GND plane Distance PWR plane For MDI – Use 6x dielectric height for stripline Use 7x dielectric height for microstrip For PCIe - Use 3x dielectric height for stripline (Rev1) Use 4x dielectric height for microstrip			
	Obtain the most recent stack-up information including the dielectric constant (dk) within the 1 to 100Mhz range and the dk at 1Ghz or higher from your Printed Circuit Board (PCB) vendor.	This is needed to calculate the transmission line impedance. See below.		
	Refer to the Platform Design Guide (PDG) for detailed routing requirements.			
Placement	The Lan Device must be placed greater than 1" away from any hole to the outside of the chassis bigger than 0.125 inches (125 mils)	The larger the hole the higher the probability the EMI and ESD immunity will be negatively affected.		
	The Lan Device should be placed greater than 250mils from the board edge.	Make sure that the Lan Device is at least 1" from any chassis openings.		
	If the connector or integrated magnetics module is not shielded, the Lan Device should be placed at least one inch from the magnetics (if a LAN switch is not used).	Placing the Lan Device closer than one inch to unshielded magnetics or connectors will increase probability of failed EMI and common mode noise.		
	If there is a LAN switch, the LAN device should be placed within 2 inches	If the LAN switch is too far away it will negatively affect IEEE return loss performance.		

82579 Layout Checklist v2.0

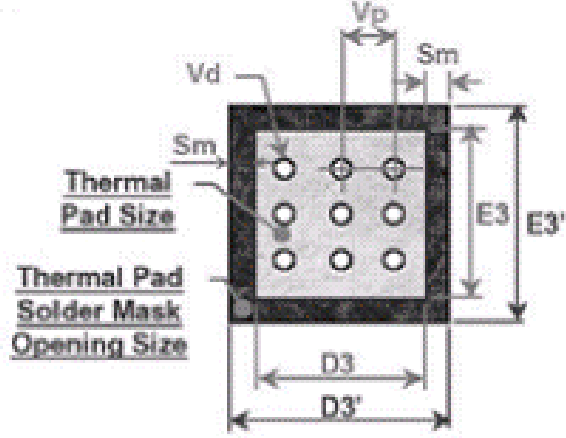| SECTION	CHECK ITEMS	REMARKS	Done (check)	NOTES
Placement *(cont.)*	• For Stripline traces, trace separation "TS" should be six times the dielectric height (thickness) of thinnest adjacent layer • For Microstrip traces, trace separation "TS" should be seven times the dielectric height (thickness) of thinnest adjacent layer Non-Docking: $R_{D1}+R_{D2}+R_{D3}<10$ Ohms total trace resistance, including LAN switch Docking: $R_{D1}+R_{D4}+R_{D5}+R_{D6}<10$ Ohms total trace resistance, including LAN switch			
	The RBIAS trace length should be less than 0.5"	The RBIAS is used to set internal current sources. It is more sensitive to noise that can come from the board which could lead to issues with BER, common mode noise, etc..		
Clock Source (Crystal Option)	The crystal trace lengths should be less than 1 inch.	This reduces EMI. This can also affect the IEEE BER, Jitter, and crystal PPM.		
	The crystal load caps should be placed less than 1" from the crystal.			
	The clock lines must be at least 5 times the height of the thinnest adjacent dielectric layer away from other from other digital traces (especially reset signals), I/O ports, board edge, transformers and differential pairs.	This helps reduce EMI. Do not route the crystal traces as differential pairs.		
	The clock lines must not cross any plane cuts on adjacent power or ground reference layers unless there are decoupling caps or connecting vias near the transition.	It is best that the clock signals reference a ground plane. If they reference a power plane it is possible they might pick up noise from power sources. Refer to the guidance on impedance controlled signals in the "general" section above on when and where stitching caps or ground vias are needed when crossing plane splits or transitioning between layers.		
	The clock lines should not cross or run in parallel (within 3x the dielectric thickness of the closest dielectric layer) with any trace (100Mhz signal or higher) on an adjacent layer.			

82579 Layout Checklist v2.0

SECTION	CHECK ITEMS	REMARKS	Done (check)	NOTES
Clock Source (Oscillator Option)	The oscillator clock trace should be less than 2 inches from the LAN device.	If it is greater than 2 inches then verify the signal quality, jitter, and clock frequency measurements at the LAN Device. The clock lines should also target 50 Ω +/- 15% and should have 33 Ω series back termination placed close to the series oscillator. See the platform design guide.		
	The clock lines must be at least 5 times the height of the thinnest adjacent dielectric layer away from other from other digital traces (especially reset signals), I/O ports, board edge, transformers and differential pairs.	This helps reduce EMI. Do not route the crystal traces as differential pairs		
	The clock lines must not cross any plane cuts on adjacent power or ground reference layers unless there are decoupling caps or connecting vias near the transition.	It is best that the clock signals reference a ground plane. If they reference a power plane it is possible they might pick up noise from power sources. Refer to the guidance on impedance controlled signals in the "general" section above on when and where stitching caps or ground vias are needed when crossing plane splits or transitioning between layers.		
	The clock lines should not cross or run in parallel with any trace (100Mhz signal or higher) on an adjacent layer.			
	The oscillator must have it's own decoupling caps and they must be placed within 0.25 inches.	If a power trace is used (not power plane) the trace from the cap to the oscillator must not exceed 0.25 inches in length. The decoupling caps help to improve the oscillator stability.		
	There should be a ferrite bead within 250 mils of the oscillator power pin	The ferrite bead filters noise off the power supply which translates to less jitter on the transmit and receiver. If the ferrite bead is placed too far away then it becomes ineffective.		
	If there is a ferrite bead on the power trace for the oscillator (see above rule), there must be a 1uF or greater capacitor within 250 mils of the oscillator and connected to the power trace between the oscillator input and ferrite bead.	The bulk decoupling cap reduces the power supply ripple.		
	If there is a ferrite bead on the power trace for the oscillator there should be a power pour (or fat trace) to supply power to the oscillator.	This will provide a lower series impedance path to the bulk decoupling and power input to the inductor which avoids voltage drops that would cause ringing and jitter.		

82579 Layout Checklist v2.0

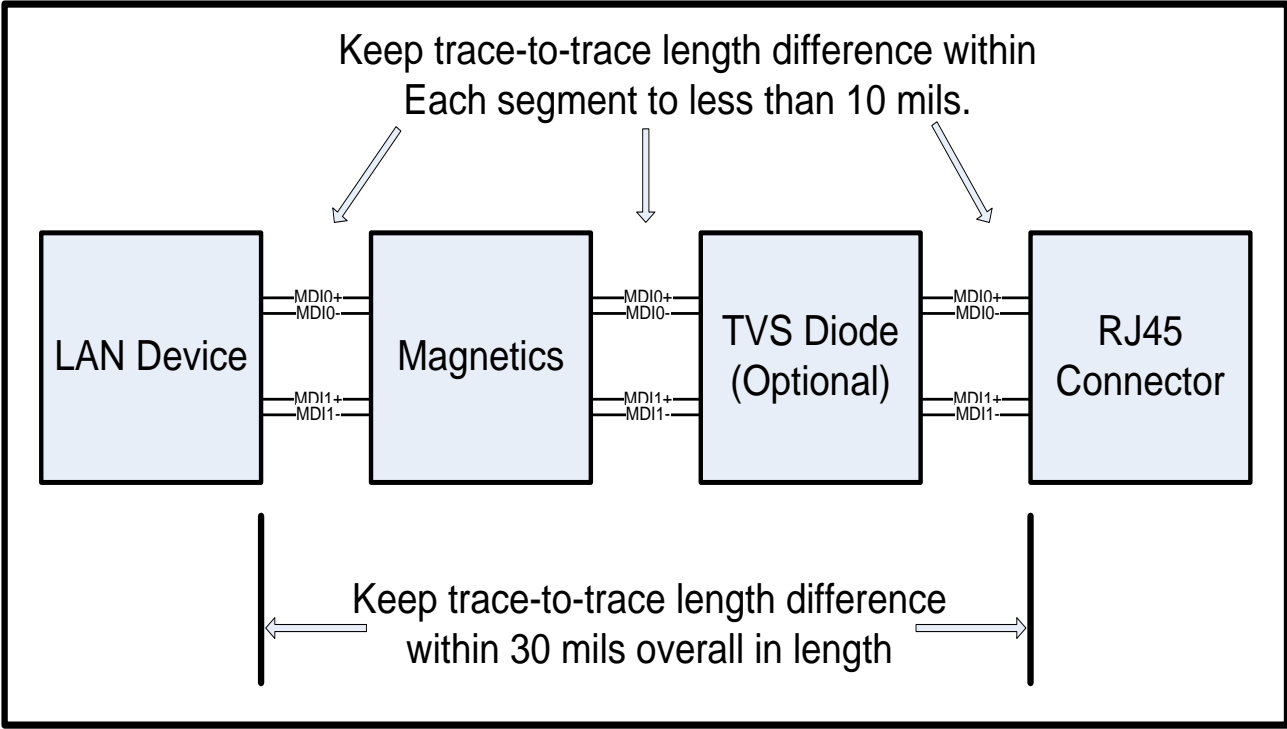| SECTION	CHECK ITEMS	REMARKS	Done (check)	NOTES
General Power Supply Guidance	The user should use planes to deliver power for all DC power rails	Not using planes can cause resistive voltage drop, inductive voltage drop (due to transient or static currents). Some of the symptoms of these voltage drops can include higher EMI, radiated immunity, radiated emissions, IEEE conformance issues, and register corruption. Use the copper loss calculator as an aid to determine the power loss due to trace width.		
	The decoupling capacitors (0.1uF and smaller) should be placed within 250 mils of the LAN silicon			
	The decoupling capacitors (0.1uF and smaller) should be distributed around the Lan Device and some should be in close proximity to the power pins.			
	The bulk capacitors (1uF or greater) should be placed within 1 inch if using a trace (50 mils wide or wider) and within 1.5 inches if using a plane.	The trace does not have to be the full width within the first 50 mils of the C6 pins due to the pin placement.		
1.0 V Rail	If using the internal SVR to generate the 1.05V power, the trace should be less than 0.5" and should be at least 20 mils wide.	For other lengths and widths, use the copper loss calculator on the 1.05V tab to determine whether the routing meets the recommendation. The trace does not have to be the full width within the first 50 mils of the Lan Device pins due to the pin placement.		

Epad	The ground vias of the Lan Device should be connected as shown below.	Refer to the design guide for additional details.
		
		Note that the Epad connection is the only source for ground and is used for both electrical and thermal.
		
		Thermal pad size = D3 * E3 = D2 * E2.
		Solder mask opening size = D3' * E3'
		= (D3+2*Sm)*(E3+2*Sm)
		=(D2+0.1)*E2+0.1)
		  where Sm = 0.05 mm (machine capability)
		    D2.E2 are exposed die attach pad size
		
		Thermal via diameter Vd (circled hole)
		  Vd = 0.3~0.33 mm (general drilling
		      machine capability)
		where thermal via is a Plated Through Hole (PTH) and plugged in solder mask from top-side of PCB.
		
		The thermal via pitch Vp
		  Vp = 1.0~1.25 mm		

82579 Layout Checklist v2.0

SECTION	CHECK ITEMS	REMARKS	Done (check)	NOTES
Epad *(cont.)*				
PCIe-based Interface	All impedance controlled signals should be routed in reference to a solid plane.	Refer to the guidance on impedance controlled signals in the "general" section above on when and where stitching caps or ground vias are needed when crossing plane splits or transitioning between layers. for the PCIe-based interface, the stitching caps and return vias need to be within 100 mils.		
	The AC coupling capacitors should be placed within 1" of the transmit or receiver side.	Size 0402, X7R is recommended. The AC coupling capacitors should be placed reasonably close to the transmitter for the PCIe interface for test purposes. This rule is based on the PCIe spec but it typically does not matter where the capacitors are placed. Placing them near the transmitter gives a convenient point to measure the transmitter output.		
	The nominal target differential trace impedance for the PCIe-based interface data pairs (transmit/receive) should be 85 Ω with ±15% manufacturing tolerance.	Simulation shows 85 Ω differential trace impedances meets Intel's PCIe-based minimum receive eye requirements when using the Customer Reference Board (CRB) design stack up. When using the CRB design stack up, Intel recommends that board designers use a 85 Ω differential trace impedance for PCIe-based I/O with the expectation that the center of the impedance is always targeted at 85 Ω. The ±15% tolerance is provided to allow for board manufacturing process variations and not lower target impedances.		

82579 Layout Checklist v2.0				
SECTION	CHECK ITEMS	REMARKS	Done (check)	NOTES
PCIe-based Interface *(cont.)*	The nominal target differential trace impedance for the PCIe interface clock pair should be within the range 90 Ω to 100 Ω with ±15% manufacturing tolerance.	When using the CRB design stack up, Intel recommends that board designers use a 90 Ω to 100 Ω differential trace impedance for PCIe clock with the expectation that the center of the impedance is always targeted at somewhere between 90 and 100 Ω. The ±15% tolerance is provided to allow for board manufacturing process variations and not lower target impedances.		
	The in-pair trace length matching on the PCIe differential pairs should be within 5 mils on a segment by segment basis.	A PCIe segment is defined as any trace within the same layer. For example, transitioning from one layer to another through a via is considered as two separate PCIe segments. The differential pairs within each segment needs to be matched to 5 mils. The PCIe clock runs at a lower frequency and is more tolerant to in-pair length skew mismatch. We recommend less than 20 mils of in-pair skew mismatch on each segment for the clock pair. However, if the clock is within 4x the thinnest adjacent dielectric height of a high speed parallel signal trace then keep the in-pair mismatch within 5 mils.		
	The end to end trace lengths within each PCIe differential pair should match within 5 mils.	The end to end trace length is defined as the total PCIe length from one component to another regardless of layer transitions. For the PCIe clock we recommend less than 20 mils of in-pair end to end length mismatch. However, if the clock is within 4x the thinnest adjacent dielectric height of a high speed parallel signal trace then keep the in-pair mismatch within 5 mils.		
	Whenever the accumulated in-pair skew on the PCIe data pairs exceeds 25 mils then it should be corrected within 600 mils.	The running in-pair skew is the mismatch of each trace within a differential pair on a segment. This mismatch is often caused by bends or staggered pins. The general guidelines is that two bends in the same direction are roughly equivalent to 25mils of skew. The skew can be corrected by adding serpentine routes on the shorter trace to increase its length to match it to its pair. It is acceptable to do this for PCIe. If adding the serpentine route this is a good opportunity to correct the segment by segment in-pair matching to within 5 mils (see rule above).		

82579 Layout Checklist v2.0

SECTION	CHECK ITEMS	REMARKS	Done (check)	NOTES
PCIe-based Interface (cont.)	The PCIe spacing between differential pairs (transmit/receive and PCIe clock) should be at least 3x the thinnest adjacent dielectric thickness for stripline and at least 4x for microstrip.	This is to reduce the amount of crosstalk between adjacent pairs. Some platforms might use 5x or greater the distance between pairs if they are using Gen 2 or higher PCIe. Example for 3 mil thick dielectric: For stripline Use a minimum of 9 mil pair-to-pair spacing. For microstrip a minimum of 12 mil pair-to-pair spacing would need to be used. This minimizes crosstalk and noise injection. Tighter spacing is allowed within 200 mils of the components pins.		
	The distance from the edge of any PCIe trace to the edge of any adjacent reference plane should be at least 3x the thinnest adjacent dielectric thickness for stripline and at least 4x for microstrip.	This is to prevent causing an impedance imbalance within a differential pair. This could lead to EMI and reflections.		
	The separation from the outside edge of any SERDES trace to any other signal trace on the same layer and any adjacent signal layer (including other SERDES trace pairs) should be at least 6x the thinnest adjacent dielectric thickness for stripline and at least 7x for microstrip. This rule does not apply to the separation within a differential pair.	This is to reduce the amount of crosstalk between adjacent pairs. Example for 3 mil thick dielectric: For stripline Use a minimum of 18 mil pair-to-pair spacing. For microstrip a minimum of 21 mil pair-to-pair spacing would need to be used. This minimizes crosstalk and noise injection. Tighter spacing is allowed within 200 mils of the components pins.		
	The distance from the edge of any SERDES trace to the edge of any adjacent reference plane should be at least 6x the thinnest adjacent dielectric thickness for stripline and at least 7x for microstrip.	This is to prevent causing an impedance imbalance within a differential pair. This could lead to EMI and reflections.		
SMBus	**System LOM:** The traces should be less than 70 inches for stripline and less than 100 inches for microstrip.	These numbers depend on the stackup, dielectric layer thickness, and trace width. The total capacitance on the trace and input buffers should be under 400pF.		
MDI Interface	All impedance controlled signals should be routed in reference to a solid plane.	Refer to the guidance on impedance controlled signals in the "general" section above on when and where stitching caps or ground vias are needed when crossing plane splits or transitioning between layers.		
	The MDI traces must not have 90° bends.	Bevel corners with turns based on 45° angles or use rounded trace corners.		

82579 Layout Checklist v2.0

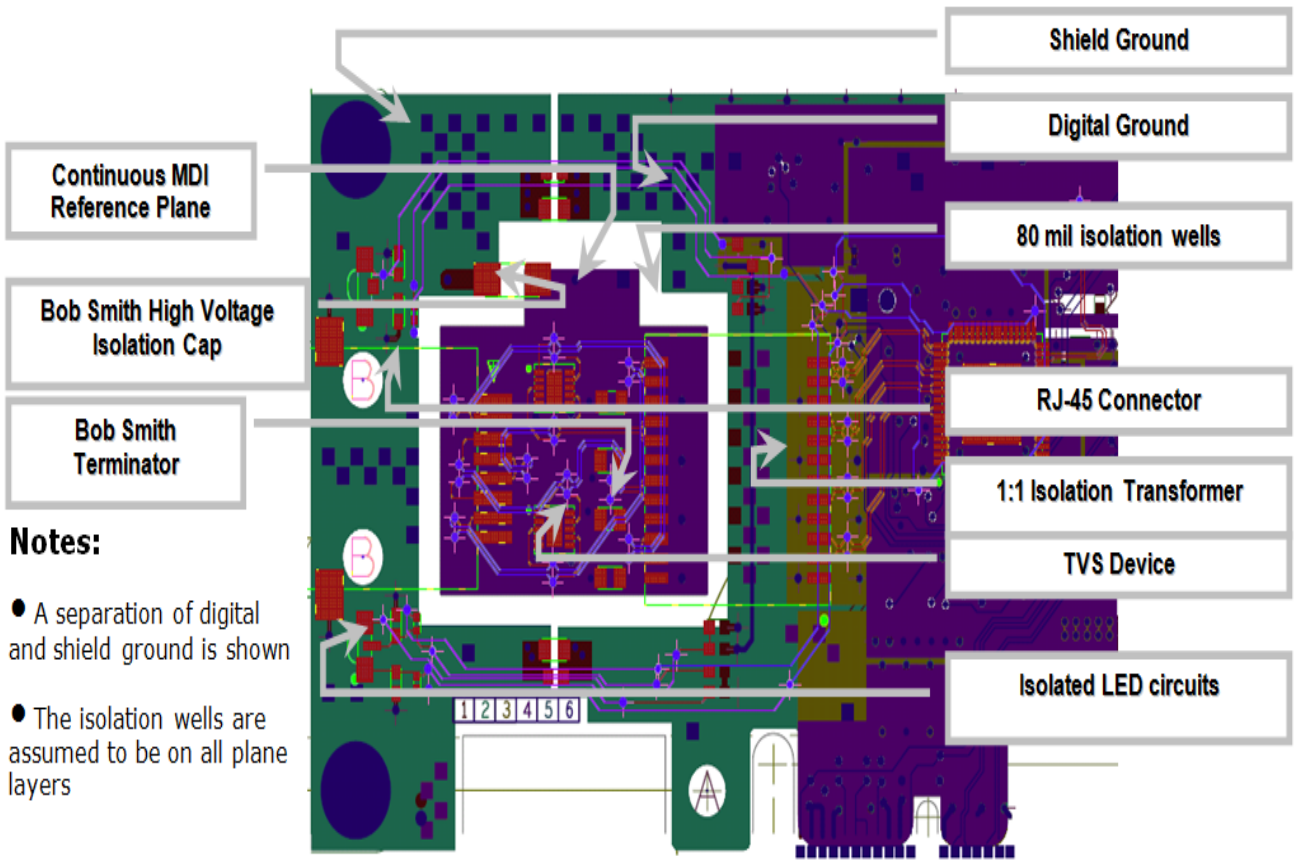| SECTION	CHECK ITEMS	REMARKS	Done (check)	NOTES
MDI Interface *(cont.)*	The in-pair trace length matching for each differential pair must be within 10 mils on a segment by segment basis.	An MDI segment is defined as any trace within the same layer. For example, transitioning from one layer to another through a via is considered as two separate MDI segments. The differential pairs within each segment needs to be matched to 5 mils. Do not use serpentine routing (zig zag of shorter trace) to match the trace lengths. Serpentine routing to the RJ-45 connector which connects to long out-of-system unshielded cables can contribute to radiated EMI and can decrease immunity to ESD.		
			☐	
	The end to end trace lengths within each differential pair must match within 30 mils. Make sure to include each segment before and after the AC decoupling caps.	The end to end trace length is defined as the total MDI length from one component to another regardless of layer transitions. The pair to pair length matching is not as critical as the in-pair length matching but it should be within 2 inches. Do not use serpentine routing (zig zag of shorter trace) to match the trace lengths. Serpentine routing to the RJ-45 connector which connects to long out-of-system unshielded cables can contribute to radiated EMI and can decrease immunity to ESD. ☐		

82579 Layout Checklist v2.0

SECTION	CHECK ITEMS	REMARKS	Done (check)	NOTES
MDI Interface (cont.)	Aside from vias and their stubs covered in prior rules, there should not be more than two stubs longer than 300 mils per MDI trace.	Stubs cause discontinuities. Stubs could come from vias, MDI termination, TVS stuffing, and test points.		
	The nominal target differential impedance for the MDI traces should be 100 Ω with ±15% manufacturing tolerance. For MDI traces longer than 3.5" refer to the platform design guide table "design guide for the maximum trace lengths based on trace geometry and board stack-up" to determine maximum recommended traces.	This is a primary requirement for 10/100/1000 Mb/s Ethernet. Paired 50 Ω traces do not make 100 Ω differential. An impedance calculator can be used to verify this. Use a good differential impedance calculator and make sure to work with the fab vendor. If a trusted commercial differential impedance calculator is not available then use the Intel MDI trace calculator. When using impedance calculators and when working with the fab vendor for microstrip traces make sure that the post plating thickness is taken into account. The post plated thickness is typically 1.9 to 2.0 mils. Optimal Trace width and separation of the MDI pairs is influenced by the board stack up in order to achieve the correct impedance. For applications that require a longer MDI trace lengths, Intel recommends that thicker dielectric or lower Er materials be used. This permits higher differential trace impedance and wider, lower loss traces. Target differential impedance is 100 Ω +/- 15% or 95 Ω +/- 10% to stay within the IEEE spec tolerances. Violating these tolerances can lead to issues with return loss, common mode noise, and Bit Error Rate. Complying with this rule is important for longer traces. It is possible to achieve longer trace lengths with IEEE and BER conformance but the MDI path may require		
	There should be no more than 2 vias per segment (Lan Device to magnetics or magnetics to RJ45) and there should not be more than 4 vias total.	Every via adds lumped capacitance to the traces at the point it is located. Each reference plane layer that a via passes through typically adds ~0.2pF to the via capacitance. For example, a 6 layer board with 2 reference layers where a via goes from the top layer to the bottom would be ~0.4pF of lump capacitance at that via. This lump capacitance causes a discontinuity in the MDI transmission lines. It is preferable that the vias be located closest to the pins and pads of devices on the MDI path (ex: magnetics, Lan Device, RJ45). Placing the vias farther than an inch from the end points may have a greater adverse impact on return loss and rise/fall times.		

82579 Layout Checklist v2.0

SECTION	CHECK ITEMS	REMARKS	Done (check)	NOTES
MDI Interface (cont.)	The separation from the outside edge of any MDI trace to any other signal trace on the same layer and any adjacent signal layer (including other MDI trace pairs) should be at least 6x the thinnest adjacent dielectric thickness for stripline and at least 7x for microstrip. This rule does not apply to the other trace within the same differential pair.	This is to reduce the amount of crosstalk between adjacent pairs. Example for 3 mil thick dielectric: For stripline Use a minimum of 18 mil pair-to-pair spacing. For microstrip a minimum of 21 mil pair-to-pair spacing would need to be used. This minimizes crosstalk and noise injection. Tighter spacing is allowed within 200 mils of the components' MDI pins.		
	The distance from the edge of any MDI trace to the edge of any adjacent reference plane should be at least 7x the adjacent dielectric.	It keeps the differential signals impedance balanced which enables IEEE conformance and reduces EMI caused by differential to common mode conversion. The 7x distance from the edge of an adjacent reference plane is not the same as 7x from the edge of a board. If the trace is routed near any holes or connectors in the chassis then this rule must be followed.		
	If using an integrated magnetics module without USB, provide a separate chassis ground "island" to ground around the RJ-45 connector. The split in the ground plane should be at least 20 mils wide. If using an integrated magnetics module with USB, do not use a separate chassis ground.	This split is mainly intended for EMI tuning so it does not have to be 80 mils as required for high voltage isolation. It is expected that the high voltage isolation requirements are already built into the integrated+C85 magnetics. The split may not be necessary but can limit EMI performance by 1 to 2 dB. Because integrated magnetics with USB have (Digital) DC power and DC ground there is no way to isolate the chassis ground from the digital ground which limits the ability to tune for potentially 1 to 2 dB better EMI. If the split is used, there should be stuffing options for AC coupling caps across the split on both sides of the magnetic modules. The values of the caps and whether to stuff the caps is determined during EMI testing. A good starting value is 0.1uF.		
	DISCRETE MAGNETICS: In order to meet IEEE high voltage isolation requirements the MDI traces and Bob Smith termination on the RJ45 side (between discrete magnetics and RJ45) must be at least 80 mils from all other traces and plane fills including adjacent layers.	This is to reduce the risk of shock hazard to the end user. Refer to the PDG for routing and placement guidelines. It can also be helpful for ESD and EFT immunity. Solder mask is not sufficient to ensure high voltage isolation. Air bubbles can cause pin holes and therefore it can not be relied upon. Internally routed traces also need to follow this rule because they could potentially arc through air filled pinholes in the glass epoxy dielectric to planes/traces above/below.		

82579 Layout Checklist v2.0

SECTION	CHECK ITEMS	REMARKS	Done (check)	NOTES
MDI Interface (cont.)			☐	
	DISCRETE MAGNETICS: In order to meet IEEE high voltage isolation requirements there must be a separate chassis ground for the LAN connector.	If using a discrete magnetics module, provide a separate chassis ground "island" to ground the shroud of the RJ-45 connector and to terminate the line side of the magnetics module.

The physical separation between the ground planes (Chassis and digital) and the reference plane (aka termplane) should be at least 80 mils wide. This separation should run under the center of magnetics module. Differential pairs must never cross the split. Refer to the PDG for more details. | | |
| | **USING LAN SWITCH:** The total resistance from the LAN device to the LAN magnetics center tap (including LAN switch resistance) must not exceed 10 Ω.

NO LAN SWICH: The total MDI path resistance from | The trace resistance includes the series resistance of any components that might be present such as LAN switches, inductors, or resistors. Desktop designs and some mobile designs do not use a LAN switch. Some embedded designs and many mobile designs use a | | |
| **Magnetics Module** | **ALL MAGNETICS**: 1uF caps should be connected within 1" of each magnetics center-tap pin. | This decoupling cap helps improve BER. It filters out some of the power supply noise and other noise on the platforms. It can also help reduce conductive EMI. | | |

82579 Layout Checklist v2.0

SECTION	CHECK ITEMS	REMARKS	Done (check)	NOTES
Magnetics Module *(cont.)*	**DISCRETE MAGNETICS**: 0.1uf caps should be connected within 100 mils of each magnetics center-tap pin.	This can decrease radiated emissions and can improve BER. NOTE: Some integrated magnetics do not include this cap internally and need the 0.1uF caps placed. Please check the datasheet to confirm this.		
	DISCRETE MAGNETICS: The discrete magnetics MDI traces should be less than 2" length from the RJ-45 connector.	Keep as short as possible.		
	DISCRETE MAGNETICS: If the connector is not shielded, the discrete magnetics should be placed at least one inch from the RJ-45 connector.	Placing the discrete magnetics closer than one inch to an unshielded connector will increase probability of failed EMI and common mode noise.		
LED Circuits	Decoupling capacitors should be placed within 250 mils of the LED pins to mitigate potential EMI and ESD issues. If decoupling capacitors are not used then there should be empty pads for placing caps to prevent a potential board redesign.	If the decoupling capacitors are used in conjunction with LED current limiting resistors then a filter could be implemented that will separate the digital ground noise from the chassis noise creating a more robust EMI solution. The preferred package size for the caps are 0402.		
	LAN LED traces should be placed at least 6x (side by side separation) the dielectric height from sources of noise (ex: signaling traces) and susceptible signal traces (ex: reset signals) on the same layer. LAN LED traces should be placed at least 7x (broadside coupling) the dielectric height from sources of noise (ex: signaling traces) and susceptible signal traces (ex: reset signals) on adjacent layers.	LED traces can carry noise into integrated magnetics modules, RJ-45 connectors, or out to the edge of the board, increasing EMI. LED traces can also carry outside ESD/EMP onto adjacent internal signals which can cause issues to other signals. For example: an ESD event can be coupled onto a device reset trace and cause the device or system to reset.		