# Zhihao **Zhou**

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Purgwal 21, 2611 GE, Delft, the Netherlands

i Born on Mar. 10, 1992 in Shandong, China

### **Education**

Nov. 2017 | M.Sc. in Electrical Engineering

Delft University of Technology, Delft, the Netherlands

Major in Microelectronics, graduate with honor (Cum Laude)

Jun. 2014 | B.Eng. in Electronic Science and Engineering

Southeast University, Nanjing, China

GPA: 88/100





unec

### Internship

### Sept. 2017

#### Master Thesis Intern, imec, Eindhoven, the Netherlands

Aug. 2016

> Title: a digital-intensive wakeup timer based on an RC frequency-locked loop for Internet of Things (IoT) applications

> Proposed a novel ultra-low-power oscillator architecture to fully exploit the small area and low supply voltage advantages in advanced CMOS processes

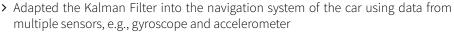
- > System-level modeling with MATLAB to estimate stabilities of the oscillator w.r.t. temperature, supply and noise
- > Transistor-level implementation in Cadence and tape-out in TSMC 40-nm CMOS
- > Measurements show the oscillator has the lowest supply voltage, the highest energy efficiency, and comparable stabilities w.r.t. the state-of-the-art

Analog/Mixed-Signal Ultra-Low Power Oscillator MATLAB Low Noise Cadence Layout Measurement Git

Aug. 2015 June 2015

### Intern, Changzhou Research Institute of Zhejiang University, Jiangsu, China

> Explored control algorithms in smart car systems



> Collaborated with other colleagues in the PCB design of the hardware

Control System | Embedded System | MATLAB | PCB | Team Collaboration



## </> Project Experience

### June 2016

### All Digital Phase-Locked Loop (ADPLL)

May. 2016

- > Course project of Digital RF
- > Learned knowledge about digital RF and frequency synthesis
- > Built a time-domain model of the ADPLL based on its phase operation
- > System-level design with the model for behavior-level noise simulation in using MATLAB

Digital RF | ADPLL | Frequency Synthesis | Modeling | MATLAB

### May. 2016

#### Transistor Fabrication

Apr. 2016

- > Course project of IC-technology lab.
- > Learned basic CMOS fabrication steps and their physical mechanisms with a 1-μm Bi-CMOS process in Else Kooi Lab at Delft University of Technology
- > Simulation and hands-on operation of the fabrication of MOS transistors in a clean room
- > Lab measurement of the fabricated transistors using a microscope and a probe station

CMOS process | Simulation | Fabrication | Clean Room | Measurement

#### Mar. 2016

#### Audio Amplifier Design

Feb. 2016

- > Course project of Analog CMOS Design
- > Designed a class-AB amplifier architecture to handle a low-ohmic load with a rail-to-rail swing
- > Implemented the amplifier using LTspice in 0.18-μm CMOS, and it achieved a high SNR, a high SFDR, and a low IM3
- > Optimized the gain and phase margins of the amplifier to achieve a stable operation within the given bandwidth

Analog Design | Amplifier Design | Low Noise | Stability Margins | LTspice

#### Jan. 2016

#### Time-to-Digital Converter (TDC)

Dec. 2015

- > Course Project of Digital IC Design
- > Designed a 10-bit TDC with a 4-bit delay line and a counter to save area and power
- > Implemented the TDC using Cadence in UMC 90-nm CMOS, and it achieved a worst-case 27-ps resolution with both DNL and INL smaller than 1 at every process corner
- > Optimized the area of the TDC in the layout

Mixed-Signal Design | TDC | Corner Simulation | Layout | Cadence

### Dec. 2015

#### Low-Noise Amplifier (LNA)

Nov. 2015

- > Course project of Microwave Circuit Design
- > Learned impedance matching, stability, and noise figure in microwave/RF designs
- > Designed a CMOS LNA with an inductive degeneration for simultaneous input noise and impedance matching using ADS
- > Designed the corresponding output matching network of the LNA to achieve stability

Microwave/RF Design LNA Matching Network Stability ADS

#### May. 2014 Mar. 2013

#### Micro-Electro-Mechanical System (MEMS) Magnetic Sensor

- > Student research project at Ministry of Education Key Lab. of MEMS, funded by National Science Foundation of China (No. 61201032)
- > Designed a two-dimensional MEMS magnetic sensor in collaboration with other students using ANSYS
- > Simulation and optimization of the sensor under various electrical and magnetic (EM) conditions and at process corners
- > Resulted in two patent applications

MEMS | Sensor | Team Collaboration | Modeling | Simulation | ANSYS |

### **Extracurricular Activity**

#### Aug. 2013 July 2013

### Trainee, Xilinx Summer School, Nanjing, China



- > Innovation training program organized by Xilinx in Southeast University
- > Learned industrial project development and management skills
- > Conducted a smart car project using a FPGA/ARM platform in collaboration with other trainees

Project Development | Project Management | Team Building | Verilog-HDL | C | FPGA | ARM

June 2012 June 2011

### Member, Red Cross Society of Southeast University, Nanjing, China

- > Responsible for advertising organization events by making posters, flyers, etc.
- > Planned and organized volunteer activities, and received a considerable amount of positive feedback

| Volunteer Work | Time Management | Communication Skills | Coordination Capabilities |



### Professional Skills

**Development Tools:** Cadence, LTspice, ADS, Vivado, Quartus II, Altium Designer, ANSYS, Git

**Programming Languages:** Verilog-HDL, VHDL, C/C++, MATLAB, Python

**Operating Systems:** Windows, Linux, macOS

Miscellaneous: Team Collaboration, ETFX, Microsoft Office, Computer Maintenance

### ZA

### Language



### Awards

2013	Scholarship of Suzhou Industrial Park	2%
2013	2 <sup>nd</sup> Prize in 12 <sup>th</sup> Structure Innovation Competition	5%
2013	Meritorious Winner in 7 <sup>th</sup> Freescale Smart Car Competition	10%
2012	Outstanding Student of Southeast University	1%