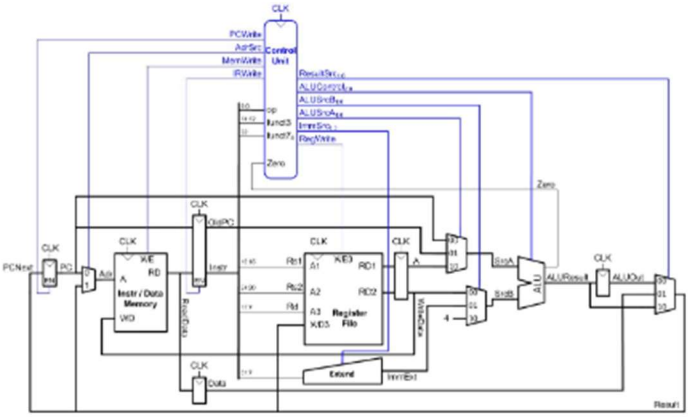
❖ Problem Set 10:

Problem Set due Jul 31, 2023 20:06 PDT Completed

Consider implementing the lui instruction on the multicycle processor.



lui

1/1 point (graded)

What are necessary elements of the simplest (and lowest-cost) implementation of lui? Check all that apply.

- [x] Modify the sign extender to support a fifth mode in which the 20-bit immediate is placed in the upper 20 bits and zeros are placed in the bottom 12 bits.
- [x] Add a third bit to the ImmSrc signal to support the sign extender mode.
- [ ] Add a shifter to the ALU
- [ ] Add a constant 12 as a fourth input to the ALUSrcB multiplexer to shift the immediate left by 12
- [x] Add ImmExt as a fourth input to the Result multiplexer.
- [ ] Add a multiplier to multiply the 20-bit immediate by 2^12 to put it in the upper 20 bits.
- [ ] Add a second port to the data memory to read the immediate.
- [ ] You must cut down the mightiest tree in the forest with ... a herring.

✔

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Main FSM

1/1 point (graded)

Suppose you implement lui using the method from the previous part (click Show Answer if necessary). How many additional states must you add to the main FSM?

1 ✔

1

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Control Signals

1/1 point (graded)

Which of the following signals {RegWrite, MemWrite, IRWrite} should be asserted in the first new state added in the main FSM for lui?

- ○ {0, 0, 0}
- ○ {0, 0, 1}
- ○ {0, 1, 0}
- ○ {0, 1, 1}
- ◉ {1, 0, 0}
- ○ {1, 0, 1}
- ○ {1, 1, 0}
- ○ {1, 1, 1}

✔

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Golliath Corporation claims to have a patent on a three-ported register file. Rather than fighting Goliath in court, you propose to design a new register file with only two ports. Port 1 can be read or written, and port 2 is read-only. Redesign the multicycle data path and controller to use your new register file.

Register File Signals

1/1 point (graded)

Which signals are part of the new 2-ported register file? Check all that apply.
The numbers on each signal indicate the port with which they are associated.

- [x] A1
- [x] A2
- [ ] A3
- [x] RD1
- [x] RD2
- [x] WD1
- [ ] WD3
- [x] WE1
- [ ] WE3
- [x] clk

✔

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Datapath Change

1/1 point (graded)

What other modifications are necessary to integrate the new register file into the datapath? Check all that apply.

- [x] add a multiplexer to choose A1 from either the Rs1 or Rd field of the instruction.
- [ ] add a multiplexer to choose A1 from either the Rs1 or Rs2 field of the instruction
- [ ] add a multiplexer to choose A2 from either the Rs1 or Rs2 field of the instruction
- [ ] add a second port to the memory to make up for the missing register file port
- [ ] add a multiplexer to choose WD1 from either Result during writes or 0 during reads.

✔

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Mux Control

1/1 point (graded)

What is the simplest way to control the address multiplexer that was added to the datapath in the question above?

- (●) Use the existing RegWrite signal to choose the address from Rs1 when RegWrite = 0 or Rd when RegWrite = 1
- ( ) Use the existing RegWrite signal to choose the address from Rs1 when RegWrite = 0 or Rs2 when RegWrite = 1
- ( ) Add a new RegAdrSrc control signal to the Main FSM that is 1 in the ALUWB state and 0 in all other states.
- ( ) Add a new HCF control signal to Halt and Catch Fire if the register file is attempting to read and write on port 1 in the same cycle.

✔

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Performance

1/1 point (graded)

Suppose the dual-ported register file has 30% lower delay and setup time because it has fewer ports. How long will your improved multicycle processor take to execute the 100-billion instruction program from Example 7.8 (and the lecture slides)? Express your answer in seconds.

155 ✔

155

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The pipelined RISC-V processor (including hazard unit) is running the following code snippet.

```
addi s1, zero, 42
addi s0, s1, -5
lw   s3, 7(s0)
sw   s4, 66(s1)
or   s2, s0, s3
```

Sketch a cartoon like the one from the textbook and lecture slides showing which is happening in the pipeline on each cycle, and where forwarding and stalls take place.

Pipeline Stalls

1/1 point (graded)

Does the processor have any stalls while executing this code?

- (•) no
- ( ) yes

✔

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Forwarding

1/1 point (graded)

What forwarding occurs while the pipelined processor runs this code? Check all that apply.

- [ ] s1 is forwarded from the first addi to the second addi in cycle 3
- [x] s1 is forwarded from the first addi to the second addi in cycle 4
- [x] s0 is forwarded from the second addi to lw
- [ ] s1 is forwarded from the first addi to sw
- [x] s3 is forwarded from lw to or

✔

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The pipelined RISC-V processor (including hazard unit) is running the following code snippet.

```
add s0, s4, s5
sub s0, s0, s2
lw  s1, 60(s0)
and s2, s1, s0
```

Sketch a cartoon like the one from the textbook and lecture slides showing which is happening in the pipeline on each cycle, and where forwarding and stalls take place.

Execution Cycles

1/1 point (graded)

If the add instruction is fetched on cycle 1, in which cycle is s2 written?

9 ✔

9

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