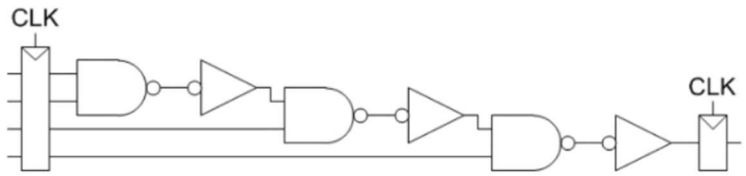
❖ Problem Set 4: Timing, SystemVerilog

Problem Set due May 6, 2023 10:37 PDT Completed

Consider the following component delays

Cell	Propagation Delay (ps)	Contamination Delay (ps)	Setup Time (ps)	Hold Time (ps)
NOT	6	4		
NAND (2-input)	8	6		
NOR (2-input)	10	8		
NAND (3-input)	10	8		
NOR (3-input)	12	10		
Flop	20	15	10	5

and the circuit below, in which registers are added to the circuit you analyzed in Problem Set 3.



Cycle Time

1/1 point (graded)

What is the minimum clock cycle time of this circuit, in the absence of clock skew? Express your answer in picoseconds.

72 ✔

72

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Clock Frequency

1/1 point (graded)

What is the maximum clock frequency? Express your answer in GHz.

13.89 ✔

13.89

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Hold Time

1/1 point (graded)

How much clock skew could this circuit endure before possibly violating the hold time? Express your answer in picoseconds.

20 ✔

20

Problem Set due May 6, 2023 10:37 PDT Completed

Synchronizers

1/1 point (graded)

A synchronizer is built from a pair of flip-flops. The flip-flops have a setup time of 50 ps, T0 of 20 ps, and tau of 30 ps. The synchronizer samples an asynchronous input that changes 100 million times per second. What is the minimum clock period of the synchronizer to achieve a mean time betwen failures (MTBF) of 100 years? Express your answer in ns.

1.14 ✔

1.14

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Consider the following possible SystemVerilog descriptions of a 2:4 Decoder.

```
module dec2to4a(input  logic [1:0] a,
                output logic [3:0] y);
  assign y[3] =  a[1] &  a[0];
  assign y[2] =  a[1] & ~a[0];
  assign y[1] = ~a[1] &  a[0];
  assign y[0] = ~a[1] & ~a[0];
endmodule
module dec2to4b(input  logic [1:0] a,
                output logic [3:0] y);
   logic [1:0] ab;

  not gn1(ab[1], a[1]);
  not gn0(ab[0], a[0]);
  and ga3(y[3], a[1], a[0]);
  and ga2(y[2], a[1], ab[0]);
  and ga1(y[1], ab[1], a[0]);
  and ga0(y[0], ab[1], ab[0]);
endmodule
module dec2to4c(input  logic [1:0] a,
                output logic [3:0] y);
  always_comb
    case(a)
      2'b00: y = 4'b0001;
      2'b01: y = 4'b0010;
      2'b10: y = 4'b0100;
      2'b11: y = 4'b1000;
    endcase
endmodule
module dec2to4d(input  logic [1:0] a,
                output logic [3:0] y);
  always_comb
    begin
       y = 4'b0;
       y[a] = 1;
    end
endmodule
module dec2to4e(input  logic [1:0] a,
                output logic [3:0] y);
  always_comb
    if      (a == 2'b00) y = 4'b0001;
    else if (a == 2'b01) y = 4'b0010;
    else if (a == 2'b10) y = 4'b0100;
    else                 y = 4'b1000;
endmodule
```

Correctness

1/1 point (graded)

Which of these descriptions are logically correct? Check all that apply.

- [x] dec2to4a
- [x] dec2to4b
- [x] dec2to4c
- [x] dec2to4d
- [x] dec2to4e

✔

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Style

1/1 point (graded)

Which of the descriptions above would be the best idiom for a 2:4 decoder?

- ( ) (a) because it is easiest to understand the function of a block from its Boolean equations
- ( ) (b) because structural Verilog is more readable than behavioral Verilog
- (•) (c) or (d) because it is easiest to understand the function of a block from its truth table in (c), while (d) is concise and scales well to larger decoders
- ( ) (e) because expressing a truth table with if statements is clearer and more concise than using case statements

✔

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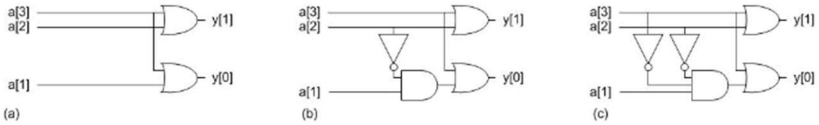
Consider the following SystemVerilog module and possible implementations.

```
module exercise(input  logic [3:1] a,
                output logic [1:0] y);
  always_comb
    if      (a[3]) y = 2'b11;
    else if (a[2]) y = 2'b10;
    else if (a[1]) y = 2'b01;
    else           y = 2'b00;
endmodule
```



HDL Synthesis

1/1 point (graded)

Which hardware schematic is implied by the code above? Simplify as much as possible.

- ( ) (a)
- (•) (b)
- ( ) (c)
- ( ) none of the above

✔

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HDL Idioms

1/1 point (graded)

Which is the name of the building block implied by the "exercise" module above?

- ( ) Decoder
- ( ) Multiplexer
- (•) Priority Encoder
- ( ) Gray Code Counter
- ( ) Level to Pulse Converter
- ( ) Finite State Machine

✔

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