❖ Lab 10:


SystemVerilog Deisgn
1/1 point (graded)
Did you describe your datapath structurally?
No
Yes
I don't know
Submit
You have used 1 of 1 attempt
Show answer

Predicting Behavior 1

1/1 point (graded)

Referring to the table above and defining Cycle 4 as the cycle in which Instr becomes 00500113 (addi x2, x2 5), in which cycle does Instr become 00C00193 (addi x3, x0, 12)?

8 ✔

8

Submit You have used 1 of 2 attempts Save | Show answer

Predicting Behavior 2

1/1 point (graded)

What is the value of PC on cycle 11?

8 ✔

8

Submit You have used 1 of 2 attempts Save | Show answer

Predicting Behavior 3

1/1 point (graded)

What is the value on the Result bus on cycle 14?

3 ✔

3

Submit You have used 1 of 2 attempts Save | Show answer

Predicting Behavior 4

1/1 point (graded)

Which state is the controller in on cycle 17?

- ○ Fetch
- ○ Decode
- ◉ ExecuteR
- ○ ExecuteI
- ○ ALUWB

✔

Submit You have used 1 of 2 attempts Save | Show answer

Hash

4.0/4.0 points (graded)

What hash is produced by your multicycle processor? Express your answer as an 8-digit hexadecimal number with no leading 0x (e.g. FF718393).

Note that if your simulation succeeds but you get a hash of 8759E4E8, you forgot to provide reset to your instruction register. Please add reset so your system behaves the same as the solution.

ffe0b9e2 ✔

Submit You have used 1 of 3 attempts

Save | Show answer