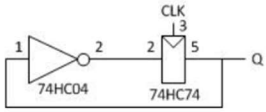
Midterm Exam due May 27, 2023 10:37 PDT Completed

Consider the following clock divider built from a 74HC74 D flip-flop and a 74HC04 inverter (data sheets linked here). The divider receives a clock on the CLK terminal and produces an output on the Q terminal. The pin numbers are annotated on the schematic.

Suppose that the system operates under typical conditions (TYP column of the datasheet) at room temperature (25 C) with VCC = 4.5 V.



Propagation Delay

1/1 point (graded)

What is the propagation delay of the NOT gate (in ns)?

9 ✔

9

Submit You have used 1 of 2 attempts Save Show answer

Setup Time

1/1 point (graded)

What is the setup time of the flip-flop with respect to the input (in ns)?

20 ✔

20

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Clock-to-Q Delay

1/1 point (graded)

What is the clock-to-Q delay of the flip-flop (in ns)?

20 ✔

20

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Clock Period

1/1 point (graded)

What is the minimum clock period for which the system will operate properly, assuming no clock skew (in ns)?

49 ✔

49

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Output Behavior

1/1 point (graded)

Suppose CLK switches at 10 MHz. What frequency would Q switch at? Express your answer in MHz.

5 ✔

5

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Dynamic Power

2.0/2.0 points (graded)

The Cpd entry on the data sheet represents the effective capacitance of the component for the purpose of dynamic power consumption calculations. Disregard input capacitance (Ci) for power calculations. The effective frequency of the flip-flop is the clock frequency (10 MHz), and the effective frequency of the inverter is the switching frequency of its input. Suppose that the system is on a breadboard that has an additional 10 pF of capacitance switching at the same frequency as Q. Use VCC = 5 V. Compute the dynamic power consumption. Express your answer in µW.

12500 ✔

12500

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Static Power

1/1 point (graded)

Compute the static power drawn by the power supply pins. Ignore input leakage. Use VCC = 5 V. The supply current is only specified at a higher VCC, so conservatively use that figure. Express your answer in units of µW.

30 ✔

30

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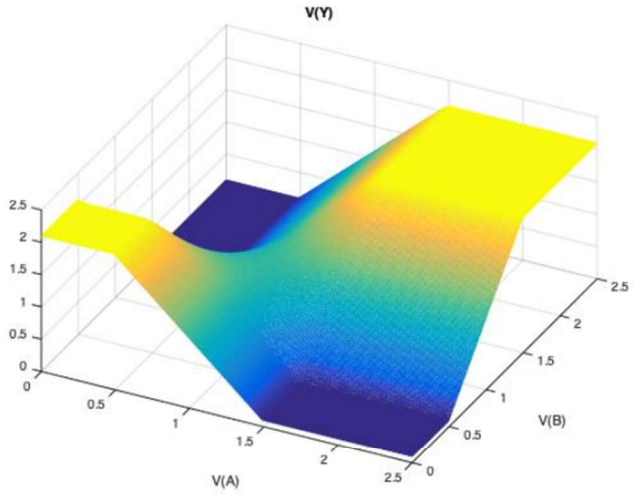
Consider the following two-dimensional plot of voltage-transfer characteristics. The yellow area are square, and the blue areas are symmetric. It's impossible to read this plot with complete precision, so the question will accept a reasonable range of answers.



Logic Function

2.0/2.0 points (graded)

What is the logic function performed by this system?

- ○ NOT
- ○ AND
- ○ OR
- ○ NAND
- ○ NOR
- ○ XOR
- ◉ XNOR

✔

Submit You have used 1 of 2 attempts

Save | Show answer

VIL

1/1 point (graded)

What is V_{IL}?

0.5

0.5

Submit You have used 1 of 2 attempts Save Show answer

VIH

1/1 point (graded)

What is V_{IH}?

1.5

1.5

Submit You have used 1 of 2 attempts Save Show answer

VOL

1/1 point (graded)

What is V_{OL}?

0.1

0.1

Submit You have used 2 of 2 attempts Show answer

VOH

1/1 point (graded)

What is V_{OH}?

2.1 ✔

2.1

Submit You have used 1 of 2 attempts Save | Show answer

Noise Margin

1/1 point (graded)

What is the smaller of the two noise margins?

0.6 ✔

0.6

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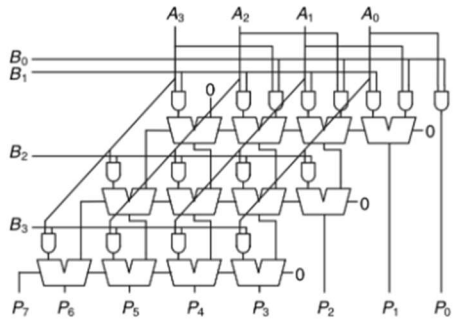
Figure 5.20 from the textbook, repeated below, is a 4×4 unsigned multiplier that takes in two 4-bit inputs A[3:0] and B[3:0] and produces an 8-bit product P[7:0].



The multiplier contains 12 full adder cells. Suppose the cells are implemented as shown below.

```
module fulladder(input  logic a, b, cin,
                 output logic s, cout);
  logic n1, n2, n3, x1;
  // sum
  xor gx1(x1, a, b);
  xor gx2(s, x1, cin);
  // carry
  and ga1(n1, a, b);
  and ga2(n2, a, cin);
  and ga3(n3, b, cin);
  or  go1(cout, n1, n2, n3);
endmodule
```

Suppose the cells have properties given in the following table

Cell	t_{pd} (ps)	t_{cd} (ps)	Relative Size
NOT	6	4	2
AND2	14	10	5
AND3	18	14	6
OR2	16	12	5
OR3	20	16	6
XOR2	24	18	9
NAND2	8	6	3
NAND3	12	10	4
NOR2	10	8	3
NOR3	14	12	4

Multiplication

1/1 point (graded)

Suppose A[3:0] = 1010 and B[3:0] = 1110. Express P[7:0] in hexadecimal.

8c ✔

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Circuit Cost

1/1 point (graded)

Determine the cost of the circuit, measured in the same units as the relative sizes.

548 ✔

548

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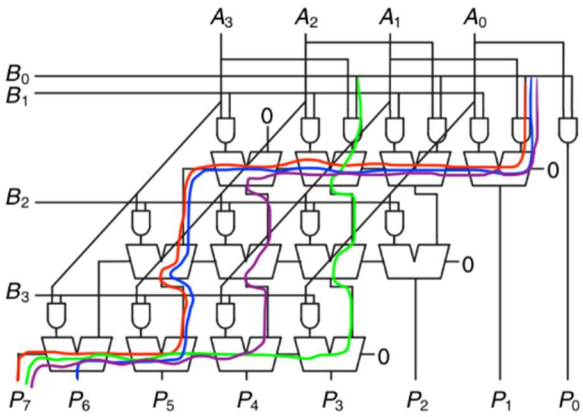
Consider the following possible critical paths annotated on the multiplier:



Critical Path

2.0/2.0 points (graded)

What is the longest path through the multiplier? (Descriptions are added in case you have trouble seeing color.)

- ○ red (from the first column to P7)
- ○ blue (from the first column to P6)
- ◉ purple (from the first column down the P4 column to P7)
- ○ green (down the P3 column to P7)

✔

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Save | Show answer

Critical Path Cells

1/1 point (graded)

What are the elements on the critical path?

- ○ 5AND2 + 4OR3 + 4XOR
- ○ 6AND2 + 5OR3 + 3XOR
- ○ 7AND2 + 6OR3 + 2XOR
- ◉ 7AND2 + 6OR3 + 3XOR ✔

Submit You have used 1 of 2 attempts Save | Show answer

Propagation Delay

1/1 point (graded)

What is the propagation delay of the multiplier? Express your answer in ps.

290 ✔

290

Submit You have used 1 of 2 attempts Save | Show answer

Contamination Delay

1/1 point (graded)

What is the contamination delay of the multiplier? Express your answer in ps.

10 ✔

10

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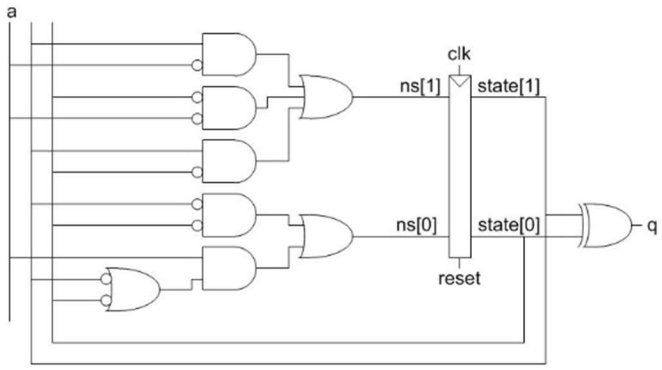
Consider the following circuit:



Download a SystemVerilog template and test vectors for this circuit.

fsm.sv

fsm.tv

The expected test vector outputs are given as x. You may change them for testing purposes, but may not change the inputs because that would mess up your hash.

Modify fsm.sv to describe the circuit with behavioral (not structural) SystemVerilog. Simulate and debug, and report the hash you obtained.

This MOOC cannot give partial credit, so the stakes for getting it right are high. Use the verification techniques you have learned in this class to confirm that your design is right.

Behavioral FSM

1/1 point (graded)

Check all the boxes below that apply to your behavioral FSM description:

- [x] fsm has an always_ff block describing the state register
- [ ] fsm instantiates two flopr modules describing the state register
- [x] the state register has a reset input
- [ ] the state register doesn't need reset because its state naturally starts at 0 when first turned on.
- [ ] fsm instantiates AND, OR, and NOT gates to structurally describe the circuit
- [ ] fsm uses assign statements with Boolean equations to describe the next state logic
- [x] fsm uses a case statement to describe the next state logic

✔

Submit You have used 1 of 2 attempts Save | Show answer

Hash

4.0/4.0 points (graded)

What hash did your testbench produce? Enter the hash as a 2-digit hexadecimal number with lowercase letters where applicable.

30 ✔

Submit You have used 1 of 2 attempts Save | Show answer