❖ Chapter 7: Microarchitecture / Introduction

Practice due May 11, 2023 21:19 PDT Completed

Architectural State

1/1 point (graded)

The architectural state of a RISC-V processor includes (check all that apply):

- [x] The register file
- [x] The program counter
- [x] The memory
- [ ] Pipeline registers used to increase the processor performance
- [ ] An instruction register used to hold the instruction after it is loaded from architectural state.
- [ ] A state register used to sequence a multicycle controller through various steps.

✔

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Processor Operation

1/1 point (graded)

Consider a single-cycle processor executing lw x3, 4(s0). The instruction is stored at address 0×000020AC. Suppose s0 contained 0×12345678. What value is on the ALUResult bus by the end of the cycle? Express your answer in hexadecimal with no leading 0x.

1234567C ✔

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Processor Operation 2

1/1 point (graded)

In the example above, what value is on the PCNext bus? Express your answer in hexadecimal with no leading 0x.

20B0 ✔

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Control Signals

1/1 point (graded)

Why is the ResultSrc control signal needed?

- ○ To determine whether Result is selected from SrcA or SrcB.
- ◉ To determine whether Result is selected from ALUResult for beq or R-type instructions, or from ReadData for lw.
- ○ To determine wehther Result is 0 or 1
- ○ What is the airspeed velocity of an unladen swallow?

✔

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ImmExt

1/1 point (graded)

When executing addi s0, s0, -1, what is ImmExt? Express your result as a 32-bit hexadecimal number with no leading 0x.

FFFFFFFF ✔

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Control Signals

1/1 point (graded)

Which of the following instructions assert RegWrite? Check all that apply.
Try to answer the question from first principles about what the instructions do and what RegWrite does, before optionally checking your work against the truth table in the lecture.

- [x] lw
- [ ] sw
- [x] R-type instructions
- [ ] beq

✔

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ALUOp

1/1 point (graded)

When ALUOp = 01, what does the ALU do?

- ○ add
- ◉ subtract
- ○ and
- ○ or
- ○ not enough information to answer this question

✔

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ALU Decoder Design

1/1 point (graded)

The ALU Decoder computes a combinational function of 7 inputs and 3 outputs. What is the most practical way to design the hardware to implement this function?

- ○ Karnaugh maps
- ○ inspection
- ○ sum of products and Boolean algebra
- ◉ Describe the truth table in HDL and allow a logic synthesizer to optmize
- ○ finite state machines
- ○ Petri networks

✔

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xor instruction

1/1 point (graded)

Consider modifying the single-cycle processor to support the xor instruction, which is an R-type instruction. What changes would be necessary? Check all that apply.

- [x] Extend the ALU with 32 XOR gates, selected by a new value of the ALUControl signal (e.g. 101).
- [x] Add a line to the ALU Decoder truth table to produce the new value of ALUControl when the instruction is xor
- [ ] Add a line to the Main Decoder truth table to produce appropriate control signals for the xor instruction
- [ ] Place 32 XOR gates between the register file RD2 port and the SrcB multiplexer.
- [ ] None of the above.

✔

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Performance Analysis

1/1 point (graded)

Suppose you design a better ALU that is 10 ps faster, and reduce the clock cycle time accordingly. What would be the execution time for the program described in this section? Express your answer in seconds.

74 ✔

74

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Refer to the riscvtest.asm code below:

```
# Test the RISCV processor.
#  add, sub, and, or, slt, addi, lw, sw, beq, jal
# If successful, it should write the value 71 to address 84
#       Assembly                Description           Address
main:   addi x2, x0, 5          # initialize x2 = 5     0
 addi x3, x0, 12 # initialize x3 = 12 4
 addi x7, x3, -9 # initialize x7 = 3 8
 or   x4, x7, x2 # x4 = (3 OR 5) = 7 C
 and  x5, x3, x4 # x5 = (12 AND 7) = 4 10
 add  x5, x5, x4 # x5 = 4 + 7 = 11 14
 beq  x5, x7, end # shouldn't be taken 18
 slt  x4, x3, x4 # x4 = (12 < 7) = 0 1C
 beq  x4, x0, around # should be taken 20
 addi x5, x0, 0 # shouldn't happen 24
around: slt  x4, x7, x2         # x4 = (3 < 5) = 1 28
 add  x7, x4, x5 # x7 = 1 + 11 = 12 2C
 sub  x7, x7, x2 # x7 = 12 - 5 = 7 30
 sw   x7, 68(x3) # [80] = 7 34
 lw   x2, 80(x0) # x2 = [80] = 7 38
 jal  x3, end # save 64 in x3 3C
 addi x2, x0, 1 # shouldn't happen 40
end: add  x2, x2, x3 # x2 = 7 + 64 = 71 44
 sw   x2, 84(x0) # write mem[84] = 71 48
```

Implementation Error

1/1 point (graded)

Suppose there were a bug in the processor design that caused the processor to write PC rather than PC+4 as the return address of JAL. What value would be written to address 84 at the end of the program?

67 ✔

67

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Refer to the aludecoder Verilog module below:

```
module aludec(input  logic       opb5,
              input  logic [2:0] funct3,
              input  logic       funct7b5,
              input  logic [1:0] ALUOp,
              output logic [2:0] ALUControl);

  logic  RtypeSub;
  assign RtypeSub = funct7b5 & opb5;  // TRUE for R-type subtract

  always_comb
    case(ALUOp)
      2'b00:                ALUControl = 3'b010; // addition
      2'b01:                ALUControl = 3'b110; // subtraction
      default: case(funct3) // R-type or I-type ALU
                 3'b000:  if (RtypeSub)
                            ALUControl = 3'b110; // sub
                          else
                            ALUControl = 3'b010; // add, addi
                 3'b010:    ALUControl = 3'b111; // slt, slti
                 3'b110:    ALUControl = 3'b001; // or, ori
                 3'b111:    ALUControl = 3'b000; // and, andi
                 default:   ALUControl = 3'bxxx; // unknown
               endcase
    endcase
endmodule
```

xor

1/1 point (graded)

xor is an R-type instruction with funct3=100. Suppose you've already modified the ALU to perform xor when ALUControl=101. What would you need to change in the aludecoder to finish supporting xor?

- (●) 3'b100: ALUControl = 3'b101;
- ( ) 3'b101: ALUControl = 3'b100;
- ( ) 2'b11: ALUControl = 3'b100;
- ( ) if (funct3 == 3'b100) ALUControl = 3'b101;

✔

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Consider the multicycle datapath executing

lw s0, 8(s1)

Suppose the instruction is at address 2000. s0 contains 40 and s1 contains 5000.

ALU Step 3

1/1 point (graded)

During step 3, what is the value of ALUResult?

5008 ✔

5008

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ALU Step 6

1/1 point (graded)

During step 6, what is the value of ALUResult?

2004 ✔

2004

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Architectural State

1/1 point (graded)

The multicycle datapath has registers Instr, Data, OldPC, A, B, and ALUOut that are not in the single-cycle datapath. Are these registers part of the architectural state of the multicycle processor?

- ○ Yes, because you can't build a multicycle processor without them.
- ○ Yes, because they contain bits of state, even though you could conceivably design a different multiyclce processor with different registers.
- ◉ No, because architectural state only encompasses the state elements visible to the programmer.
- ○ No, because some of them have enable signals.

✔

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Single/Multicycle Comparison

1/1 point (graded)

As compared to the single-cycle processor, the multicycle processor has (check all that apply)

- ☑ a unified instruction and data memory rather than two separate memories
- ☑ fewer adders
- ☐ fewer multiplexers
- ☑ more and bigger multiplexers
- ☑ nonarchitectural state registers

✔

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Instruction Decoder

1/1 point (graded)

The instruction decoder is a combinational function of A bits of input and B bits of output. What is A?

7 ✔

7

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Fetch State Activity

1/1 point (graded)

During the fetch state, what activity occurs in the multicycle datapath?

- [x] A multiplexer chooses the address to the memory from the PC
- [x] The memory reads the current instruction
- [ ] The register file reads the source registers for the instruction
- [ ] The ALU performs the instruction if it is R-type
- [x] The ALU adds 4 to the program counter
- [x] A multiplexer chooses Result from the ALU
- [ ] A multiplexer chooses Result from the Data register
- [x] The Instr register is written at the end of the cycle
- [x] The PC is written at the end of the cycle
- [ ] The register file is written at the end of the cycle

✔

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Multiplexer Control Signals

1/1 point (graded)

When a multiplexer control signal such as ALUSrcA is not specified in the FSM diagram, that means:

- ○ It must be 0.
- ○ It must be 1.
- ◉ It is a don't care.
- ○ There is a bug in the FSM.

✔

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Write Enable Signals

1/1 point (graded)

When a write enable signal such as IRWrite is not specified in the FSM diagram, that means:

- ◉ It must be 0.
- ○ It must be 1.
- ○ It is a don't care.
- ○ There is a bug in the FSM.

✔

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Multicycle FSM

1/1 point (graded)

When a sw instruction is being executed, what sequence of states does the FSM follow?

- ○ S0 Fetch, S1 Decode, S2 MemAdr, S3 MemRead, S4 MemWB
- ◉ S0 Fetch, S1 Decode, S2 MemAdr, S5 MemWrite
- ○ S0 Fetch, S1 Decode, S6 ExecuteR, S7 ALUWB
- ○ S0 Fetch, S1 Decode, S2 MemAdr, S3 MemRead, S4 MemWB, S5 MemWrite, S6 ExecuteR, S7 ALUWB, S10 BEQ
- ○ It depends on the contents of the register file

✔

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Decode State

1/1 point (graded)

Why are ALUSrcA, ALUSrcB, and ALUOp used in S1?

- ○ To execute R-type instructions.
- ○ To compute the base address + offset for lw and sw.
- ◉ To compute the branch target address for branches, while the ALU otherwise would be idle.
- ○ To compute the branch target address, which is needed in subsequent steps for all instructions.

✔

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CPI

1/1 point (graded)

Suppose you were running a program with a different mix of instructions than SPECInt. Suppose the relative frequencies were 20% loads, 20% branches, 5% stores, and 55% R-type. What would the average CPI be?

4 ✔

4

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Design Methodology

1/1 point (graded)

Our pipelined processor is designed by:

- (●) partitioning the single-cycle processor into multiple stages
- ( ) partitioning the multicycle processor into multiple stages
- ( ) starting from first principles and connecting architectural state as necessary for each instruction

✔

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Pipeline Operation

1/1 point (graded)

Referring to the Pipelined Processor Abstraction slide, which registers are being read from the register file on cycle 4? Check all that apply.

- [ ] s0
- [ ] s2
- [ ] s5
- [x] s8
- [ ] s11
- [ ] t0
- [x] t1
- [ ] t5
- [ ] t4

✔

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More Pipeline Operation

1/1 point (graded)

Referring again to the Pipelined Processor Abstraction diagram, on which cycles are the data memory being used?

- [ ] 1
- [ ] 2
- [ ] 3
- [x] 4
- [ ] 5
- [ ] 6
- [ ] 7
- [x] 8
- [ ] 9
- [ ] 10

✔

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Consider the following program running on our pipelined processor. Suppose s0 initially had the value 42.

```
addi s0, zero, 10

add  s1, s0, s0
```

Program Operation

1/1 point (graded)

If the processor handles hazards correctly, what value should be in s1 when the program completes?

20 ✔

20

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Hazards

1/1 point (graded)

Suppose the pipelined processor was missing the hazard unit. What value would be in s1 when the program completes?

84 ✔

84

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Branch Misprediction Penalty

1/1 point (graded)

What is the branch misprediction penalty for our pipelined processor? Express your answer in cycles or instructions.

2 ✔

2

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Pipelined CPI

1/1 point (graded)

Suppose the pipelined processor ran a program with 100 billion instructions, of which 20% are loads, 12% are stores, 15% are branches, and the remainder are R-type. Suppose that 25% of the loads are used by the next instruction and that 1/3 of the branches are mispredicted. What is the average CPI?

1.15 ✔

1.15

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Deep Pipelines

1/1 point (graded)

A deeper pipeline may improve performance by:

- (•) Reducing the cycle time
- ( ) Reducing the CPI
- ( ) Reducing the number of instructions to execute

✔

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Branch Predictors

1/1 point (graded)

A branch predictor may improve performance by:

- ( ) Reducing the cycle time
- (•) Reducing the CPI
- ( ) Reducing the number of instructions to execute

✔

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Register Renaming

1/1 point (graded)

Benefits of register renaming are (select all that apply):

- [x] Eliminating WAR and WAW hazards by introducing more registers to prevent these hazards that occur when a finite number of registers need to be recycled for different purposes.
- [ ] Eliminating RAW hazards by reordering a program.
- [ ] Reducing the cycle time by using a smaller register file.
- [ ] Increasing the IPC by providing more execution units.

✔

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Processes and Threads

1/1 point (graded)

Which statement correctly describes the relationship of processes and threads?

- ○ Each process has exactly one thread.
- ◉ A process may have more than one thread.
- ○ A thread may have more than one process.

✔

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Multithreaded Processors

1/1 point (graded)

Multithreading can improve the performance of a computer by:

- ◉ Reducing the time to switch between threads
- ○ Running several threads concurrently on mulitple cores
- ○ Reducing the cycle time
- ○ Executing instructions out of order

✔

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Multiprocessors

1/1 point (graded)

Multiprocessing can improve the performance of a computer by:

- ○ Reducing the time to switch between threads
- ◉ Running several threads concurrently on mulitple cores
- ○ Reducing the cycle time
- ○ Executing instructions out of order

✔

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