❖ Chapter 3: Sequential Logic / Introduction

Lecture Practice due Apr 15, 2023 10:37 PDT Completed

Bits of State

1/1 point (graded)

A system could be in one of 11 states. How many bits are required to represent the state?

4 ✔

4

Submit Try again (1 attempt remaining) Show answer

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Bistable Limitation

1/1 point (graded)

What is the main limitation of a bistable circuit constructed from cross-coupled inverters?

- ○ There is no way to observe the state of the circuit.
- ◉ There is no way to change the state of the circuit.
- ○ If one node starts at a voltage in the forbidden zone, the circuit will heat up and eventually catch on fire.
- ○ If you give them more positive feedback, they might not feel so cross.

✔

Submit Try again (1 attempt remaining) Show answer

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Consider the following waveforms:

SR Latch Final Value

1/1 point (graded)

If wave A is applied to the S terminal of an SR latch and wave B is applied to the R terminal, what is the final value of Q

0 ✔

0

Submit Try again (1 attempt remaining) Show answer

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Consider the following waveforms:

D Latch Final Value

1/1 point (graded)

If wave A is applied to the CLK terminal of an D latch and wave B is applied to the D terminal, what is the final value of Q

1 ✔

1

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Consider the following waveforms:

D Flip-Flop Final Value

1/1 point (graded)

If wave A is applied to the CLK terminal of an D flip-flop and wave B is applied to the D terminal, what is the final value of Q

0 ✔

0

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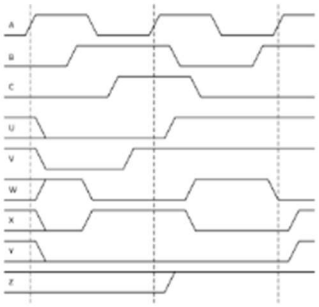
Consider the following input and output waveforms.

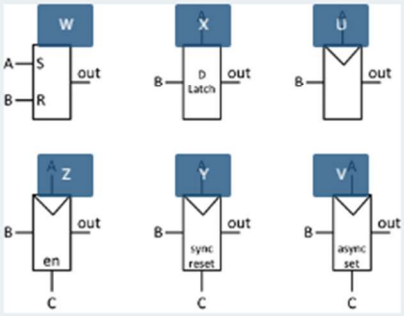


Sequential Element Waveforms

1/1 point (graded)

Keyboard Help

Consider the sequential elements below with inputs A, B, and C shown above. Drag the appropriate letter to the element to indicate its output response.



Reset

FEEDBACK

Good work! You have shown the relationship between input and output for each sequential element.

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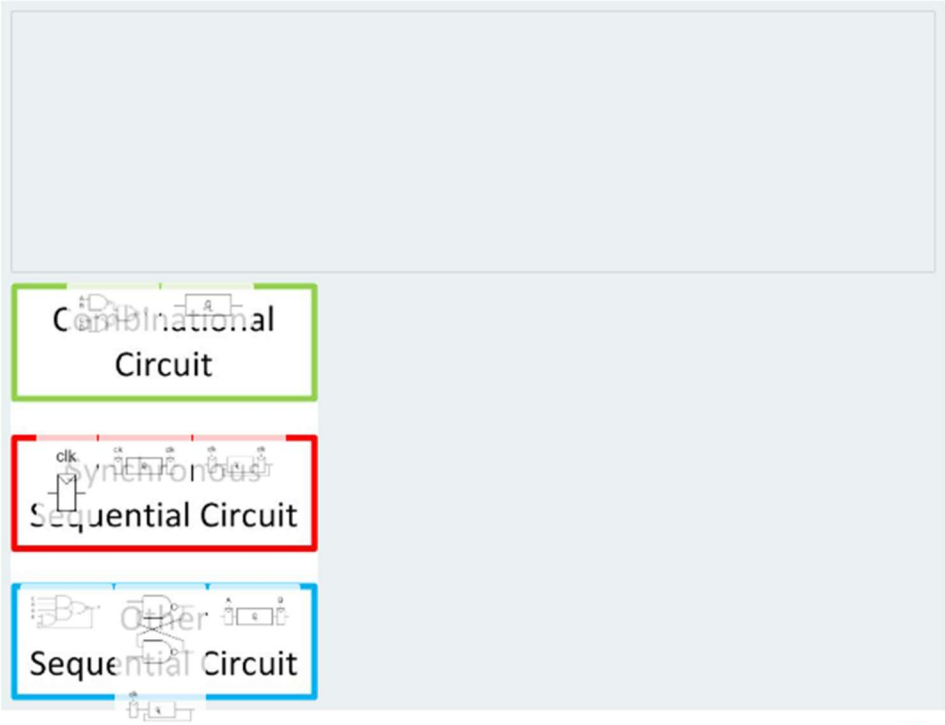
Circuit Types

1/1 point (graded)

Keyboard Help

Drag each circuit to the corresponding box to classify it.



Reset

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FSM Types

1/1 point (graded)

In a Moore FSM, the output is a function of only the current state.

- ○ FALSE
- ◉ TRUE

✔

Submit Try again (1 attempt remaining) Show answer

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Bits of State

1/1 point (graded)

What is the minimum number of bits of state to build a FSM with 5 states?

3 ✔

3

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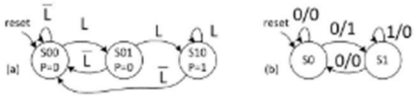
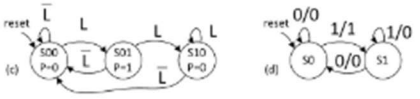
A level-to-pulse converter is a synchronous system with an input L and an output P. When L rises from 0 to 1, P will pulse high for one clock cycle after L rose. The figure below shows waveforms for the circuit:

Consider the following state transition diagrams and next state logic:





State	L	Next State
00	0	00
00	1	01
01	0	00
01	1	10
10	0	00
10	1	01

(a)

State	L	Next State
00	0	00
00	1	01
01	0	00
01	1	10
10	0	00
10	1	10

(b)

State	L	Next State	P
0	0	0	0
0	1	1	1
1	0	0	0
1	1	0	0

(c)

State Transition Diagram

1/1 point (graded)

Which state transition diagram correctly generates the waveforms shown above?

- a
- b
- **c**
- d
- c and d

✔

Submit Try again (1 attempt remaining) Show answer

State Transition Table

1/1 point (graded)

Which state transition table corresponds to the correct state transition diagram?

- a
- **b**
- c
- none of the above

✔

Submit Try again (1 attempt remaining) Show answer

State Transition Logic

1/1 point (graded)

Which equations describe the next state logic?

- (●) S'[1] = (S[1] + S[0])L; S'[0] = (~S[1])(~S[0])L
- ( ) S' = (~S)L; P = S'
- ( ) S'[1] = (~S[0])(~S[1])L; S'[0] = S[1]S[0]L

✔

Submit | Try again (1 attempt remaining) | Show answer

Output Logic

1/1 point (graded)

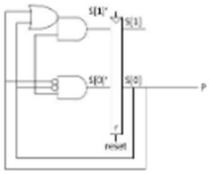
Which equation describes the output logic as simply as possible?

- (●) P = S[0]
- ( ) P = S[1]
- ( ) P = (~S[1])S[0]
- ( ) P = S

✔

Submit | Try again (1 attempt remaining) | Show answer

Consider the schematic below purporting to implement the FSM.



Schematic

1/1 point (graded)

What errors exist in the circuit schematic for the level-to-pulse converter? Check all that apply.

- [ ] The reset terminal of the register should be a set terminal instead.
- [ ] P should come from S[1], not S[0].
- [x] One of the state feedback lines should come from S[1] rather than both from S[0].

✔

Submit | Try again (1 attempt remaining) | Show answer

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Mealy FSM

1/1 point (graded)

A Mealy FSM (check all that applies)

- [x] lists output values on arcs
- [ ] lists output values on nodes
- [x] may have fewer states than a Moore machine doing the same function
- [x] may be more difficult to visualize than a Moore machine because the output depends on inputs as well as the current state

✔

Submit Try again (1 attempt remaining) Show answer

Consider building a serial 2's complementer FSM with an input A and output N. This FSM takes a binary number starting with the least significant bit on A and produces its 2's complement (the negative of the number) starting with the least significant bit on N.

To do this, remember that taking the two's complement involves inverting the bits and adding 1. When adding, we need to keep track of the carry from the previous column. We can treat the adding 1 as a carry in at the very start. Hence, we need a 2-state FSM with states C0 and C1 indicating the current carry in. The FSM starts in a C1 state indicating the carry in is 1. The output depends on the input, so let's build a Mealy FSM.

When in the C1 state, if the input A is 0, we invert it to 1, then add the carry to get N = 0 and a carry out, so we remain in the C1 state. If the input A is 1, we invert it to get 0, then add the carry to get N = 1, but no carry out, so we transition to the C0 state.

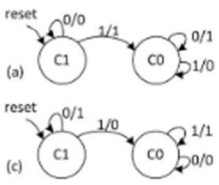
When in the C0 state, there is no carry to add. If A is 0, we invert it to get N = 1. If A is 1, we invert it to get N = 0. In either case, we remain in the C0 state because there is no carry out.

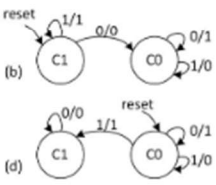
For example, consider taking the two's complement of 1010 (-6 in decimal). The following table shows the state, input, and output, starting with the least significant bit over four cycles of operation:

Cycle	state A	nextstate N
0	1	0 / 1	0
1	1	1 / 0	1
2	0	0 / 0	1
3	0	1 / 0	0

Thus the output is 0110, or +6.

Consider the following possible state transition diagrams and tables.





State	A	Next State	N
0	0	0	1
0	1	0	0
1	0	0	0
1	1	1	1

(a)

State	A	Next State	N
0	0	0	1
0	1	0	0
1	0	1	0
1	1	0	1

(b)

State	A	Next State	N
0	0	0	0
0	1	0	1
1	0	1	1
1	1	0	0

(c)

Mealy State Transition Diagram

1/1 point (graded)

Which state transition diagram above describes the 2's complementer?

- (●) a
- ( ) b
- ( ) c
- ( ) d

✔

Submit | Try again (1 attempt remaining) | Show answer

Mealy State Transition Table

1/1 point (graded)

Which state transition tables above describes the 2's complementer?

- ( ) a
- (●) b
- ( ) c

✔

Submit | Try again (1 attempt remaining) | Show answer

Next State Equation

1/1 point (graded)

Give a Boolean equation for the next state S' in terms of current state S and input A.

- ( ) S = S'(~A)
- ( ) S' = (~S)A
- ( ) S' = SA
- (●) S' = S(~A)

✔

Submit | Try again (1 attempt remaining) | Show answer

Output Equation

1/1 point (graded)

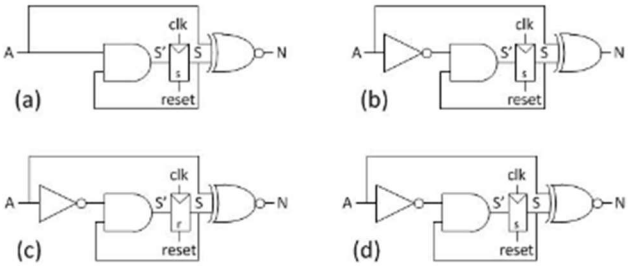
Give a Boolean equation for the output N in terms of current state S and input A.

- ( ) N = S XOR A
- (●) N = S XNOR A
- ( ) N = S(~A)
- ( ) N = SA

✔

Submit | Try again (1 attempt remaining) | Show answer

Consider the following FSM circuits.



Mealy FSM Circuit

1/1 point (graded)

Which circuit above correctly implements the FSM? Note that the small s or r in the flip-flop corresponds to a set or reset input.

- a
- b
- c
- d ✔

Submit | Try again (1 attempt remaining) | Show answer

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Multiple Choice

1/1 point (graded)

A motivation for factoring a FSM is:

- ○ to see if it is not prime
- ◉ to reduce a complex FSM into two simpler interacting FSMs
- ○ to make digital design students suffer

✔

Submit Try again (1 attempt remaining) Show answer

Multiple Choice

1/1 point (graded)

Consider a factored FSM built from an 8-state FSM and a 3-state FSM that interact. If you were to build the entire thing as a single unfactored FSM, it might need as many as ___ states.

- ○ 8
- ○ 11
- ◉ 24
- ○ 512

✔

Submit Try again (1 attempt remaining) Show answer

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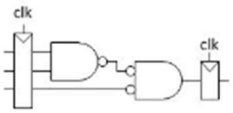
Consider the component delays in the table below

Cell	Propagation Delay (ps)	Contamination Delay (ps)	Setup Time (ps)	Hold Time (ps)
NOT	6	4		
NAND (2-input)	8	6		
NOR (2-input)	10	8		
NAND (3-input)	10	8		
NOR (3-input)	12	10		
Flop	20	15	10	5

and the following circuit. Remember that, per DeMorgan's Law, the second gate in this circuit is an alternate symbol for a NOR gate.



Cycle Time

1/1 point (graded)

What is the minimum clock period T_c for which the circuit is guaranteed to operate correctly? (Express your answer in ps). Disregard inputs and outputs, and assume clock skew is 0.

48 ✔

48

Submit Try again (1 attempt remaining) Show answer

Multiple Choice

1/1 point (graded)

What is the maximum clock frequency for which the system will work?

- (●) $1/T_c$
- ( ) $2\pi/T_c$
- ( ) T_c

✔

Submit Try again (1 attempt remaining) Show answer

Hold Time

1/1 point (graded)

Why is violating a hold time so insidious?

- ( ) The system will not work reliably at low frequency.
- (●) The system will not work reliably at any frequency.
- ( ) The system will not operate as fast as desired, and you may have to sell it for less money.

✔

Submit Try again (1 attempt remaining) Show answer

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Consider the component delays in the table below

Cell	Propagation Delay (ps)	Contamination Delay (ps)	Setup Time (ps)	Hold Time (ps)
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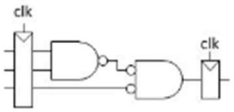
NOR (2-input)	10	8		
NAND (3-input)	10	8		
NOR (3-input)	12	10		
Flop	20	15	10	5

and the following circuit:



Remember that, according to DeMorgan's Law, an AND with bubbles on the input is a NOR.

Cycle Time Without Skew

1/1 point (graded)

If there is no clock skew, what is the minimum cycle time for which the system will operate reliably? (Express your answer in ps).

48 ✔

48

Submit Try again (1 attempt remaining) Show answer

Cycle Time

1/1 point (graded)

If the clock skew is 5 ps, what is the minimum cycle time for which the system will operate reliably? (Express your answer in ps).

53 ✔

53

Submit Try again (1 attempt remaining) Show answer

Hold Time

1/1 point (graded)

Suppose the clock period is long enough that the setup time is not a concern. What is the maximum clock skew for which this system is guaranteed to work correctly without violating the hold time at the second flip-flop? (Express your answer in ps).

18 ✔

18

Submit Try again (1 attempt remaining) Show answer

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Consequences of Violating Setup or Hold

1/1 point (graded)

If an asynchronous input is changing while a flip-flop samples the input: (check all that apply)

- [x] The output of the flip-flop could be metastable and take on a logic level in the forbidden zone.
- [ ] If the flip-flop output is in the forbidden zone, it will cause contention in the next logic gate that is likely to cause physical damage to the system.
- [x] If the metastable output of the flip-flop feeds more than one circuit, one circuit may perceive the metastable output as low and another may percieve it as high, leading to logically inconsistent results that should never occur if the flip-flop output were at a valid logic level.
- [x] The output of the flip-flop will eventually settle to a good zero or one if you wait long enough.
- [x] Because the output of the flip-flop will eventually settle, the system may rarely or never manifest a problem.
- [ ] Because metastability is rare and usually resolves, it is really a theoretical problem that practicing digital designers don't need to seriously consider.
- [x] If the system does manifest a problem, it may be difficult to reproduce and troubleshoot.

✔

Submit You have used 2 of 2 attempts Show answer

An Ounce of Prevention

1/1 point (graded)

The best way to prevent problems from asynchronous inputs is to:

- ○ Exercise the synchronous discipline and forbid any inputs from the real world outside your synchronous system.
- ○ Use flip-flops with a short tau so it is unlikely that metastability persists long enough to impact your system.
- ◉ Put synchronizers on every asynchronous input and wait long enough for the synchronizer to resolve with acceptably high probability.

✔

Submit Try again (1 attempt remaining) Show answer

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Latency

1/1 point (graded)

Ben Bitdiddle is the manager of the lacrosse team and is responsible for cleaning the team uniforms. A load of laundry takes 1 hour in the washer, 1 hour in the dryer, 0.75 hours to fold, and 0.5 hours to put away. What is the latency from when Ben recieves a load of laundry until it is put away. Express your answer in hours.

3.25 ✔

3.25

Submit Try again (1 attempt remaining) Show answer

Throughput

1/1 point (graded)

Ben's team is hosting the regional championship and Ben has a lot of laundry to do. What is his throughput?

- (●) 1 load / 3.25 hours
- ( ) 2 loads / 3.25 hours
- ( ) 1 load / hour
- ( ) 2 loads / hour

✔

Submit Try again (1 attempt remaining) Show answer

Increasing Throughput

1/1 point (graded)

Ben proposes to speed up the job by buying a second washer, a second dryer, and a second folding table. He asks his friend Alyssa to work alongside him so they can each process their own load of laundry. This is an example of:

- (●) Spatial parallelism
- ( ) Temporal parallelism (pipelining)
- ( ) None of the above

✔

Submit Try again (1 attempt remaining) Show answer

Throughput II

1/1 point (graded)

Under Ben's proposal, what is the throughput?

- ( ) 1 load / 3.25 hours
- (●) 2 loads / 3.25 hours
- ( ) 1 load / hour
- ( ) 2 loads / hour

✔

Submit Try again (1 attempt remaining) Show answer

Increasing Throughput

1/1 point (graded)

Alyssa says she has a better idea that is faster and will cost less. She proposes overalapping stages so that one load can be in the washer while a second load in the dryer. Meanwhile, she could fold a third load, and Ben could put a fourth load away. Each hour, they would finish one load and put a new one into the system. This is known as

- ○ Spatial parallelism
- ◉ Temporal parallelism (pipelining)
- ○ None of the above

✔

Submit | Try again (1 attempt remaining) | Show answer

Throughput III

1/1 point (graded)

Under Alyssa's proposal, what is the throughput?

- ○ 1 load / 3.25 hours
- ○ 2 loads / 3.25 hours
- ◉ 1 load / hour
- ○ 2 loads / hour

✔

Submit | Try again (1 attempt remaining) | Show answer