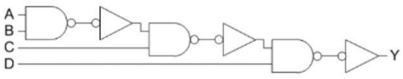
❖ Problem Set 3: Timing, Sequential Logic

Problem Set due May 6, 2023 10:37 PDT Completed

Consider the following component delays

Cell	Propagation Delay (ps)	Contamination Delay (ps)
NOT	6	4
NAND2	8	6
NOR2	10	8
NAND3	10	8
NOR3	12	10

and the circuit below.



Propagation Delay

1/1 point (graded)

What is the propagation delay of the circuit? Express your answer in picoseconds.

42 ✔

42

Submit Try again (1 attempt remaining) Show answer

Contamination Delay

1/1 point (graded)

What is the contamination delay of the circuit? Express your answer in picoseconds.

10 ✔

10

Submit Try again (1 attempt remaining) Show answer

Delay Optimization

1/1 point (graded)

Redesign the circuit to minimize the propagation delay, using only the cell types from the table above. What is your improved propagation delay?

18 ✔

18

Submit Try again (1 attempt remaining) Show answer

Late Input

1/1 point (graded)

Suppose input D arrived much later than the others. Your goal is to compute output Y as soon as possible. Which design produces Y faster?

- (•) The original design
- ( ) Your optimized design that minimizes propagation delay
- ( ) Not enough information to say

✔

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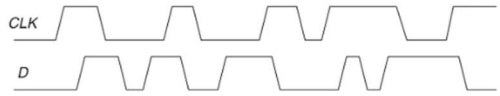
Consider the following waveforms.



D Latch Response

1/1 point (graded)

Suppose the waveforms above are applied to a D latch. The output Q is initially 0. Sketch the response Q. How many times does Q rise from 0 to 1?

4 ✔

4

Submit Try again (1 attempt remaining) Show answer

D Flip-Flop Response

1/1 point (graded)

Suppose the waveforms above are applied to a D flip-flop. The output Q is initially 0. Sketch the response Q. How many times does Q rise from 0 to 1?

2 ✔

2

Submit Try again (1 attempt remaining) Show answer

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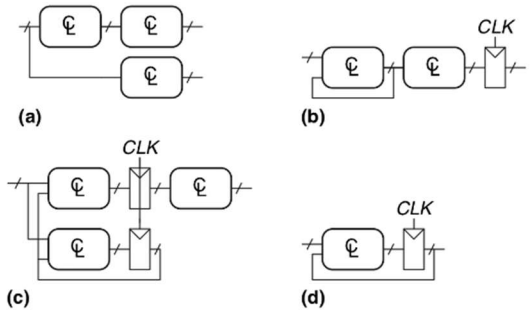
Consider the following circuits (Exercise 3.18):



Synchronous Logic

1/1 point (graded)

Select which of the circuits above are synchronous sequential logic. Remember that the CL blocks are combinational.

- [ ] (a)
- [ ] (b)
- [x] (c)
- [x] (d)

Submit Try again (1 attempt remaining) Show answer

Bits of State

1/1 point (graded)

A digital system receives an input A every clock cycle. It produces an output E that is TRUE if A has been 1 an even number of times since the system was first turned on. What is the minimum number of bits of state necessary to build this system?

1 ✔

1

Submit Try again (1 attempt remaining) Show answer

Bits of State II

1/1 point (graded)

A digital system receives an input A every clock cycle. It produces an output E that is TRUE if A has been 1 an even number of times in the past 20 clock cycles. What is the minimum number of bits of state necessary to build this system?

20 ✔

20

Submit Try again (1 attempt remaining) Show answer

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Soda Machine Dispenser

1/1 point (graded)

You have been enlisted to design a soda machine dispenser for your department lounge. Sodas are partially subsidized by the student chapter of the IEEE, so they cost only 25 cents. The machine accepts nickels, dimes, and quarters. When enough coins have been inserted, it dispenses the soda and returns any necessary change. Design a Moore FSM controller for the soda machine with the minimum number of states necessary. The FSM inputs are Nickel, Dime, and Quarter, indicating which coin was inserted. Assume that exactly one coin is inserted on each cycle. The outputs are Dispense, ReturnNickel, ReturnDime, and ReturnTwoDimes. When the FSM reaches 25 or more cents, it asserts Dispense and the necessary Return outputs required to deliver the appropriate change. Then it should be ready to immediately start accepting coins for another soda. What is the minimum number of bits of state required to build your FSM?

4 ✔

4

Submit Try again (1 attempt remaining) Show answer

Soda Machine Dispenser Output

1/1 point (graded)

In how many of the states is the Dispense output asserted?

5 ✔

5

Submit | Try again (1 attempt remaining) | Show answer

Soda Machine Dispenser Output II

1/1 point (graded)

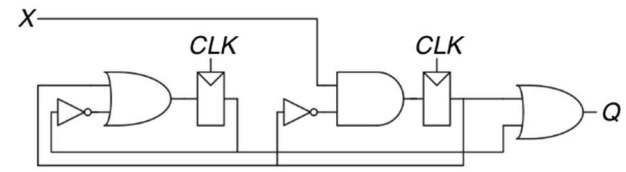
In how many of the states is the ReturnNickel output asserted?

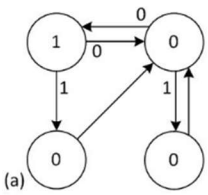
2 ✔

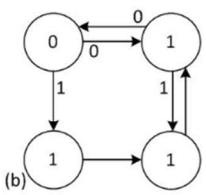
2

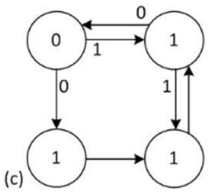
Submit | Try again (1 attempt remaining) | Show answer

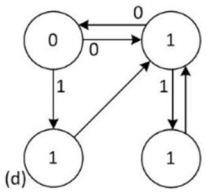
Consider the following schematic and possible associated state transition diagrams:











Reverse Engineering FSM

1/1 point (graded)

Which state transition diagram above has the same behavior as the schematic?

- (a)
- (b)
- (c)
- (d)

Submit | Try again (1 attempt remaining) | Show answer