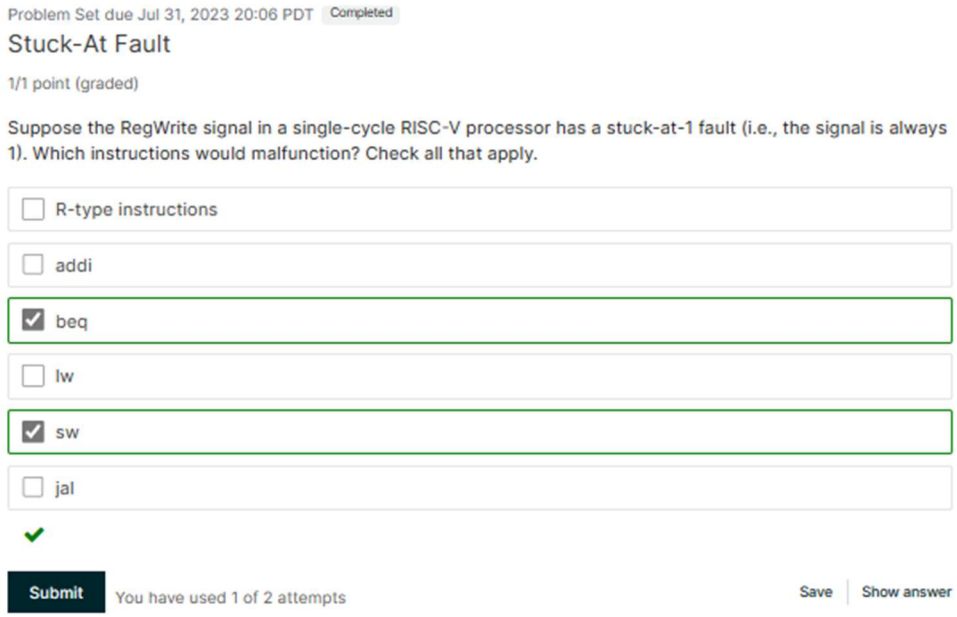
❖ Problem Set 9:



Problem Set due Jul 31, 2023 20:06 PDT Completed

Table 7.7 Delay of circuit elements

Element	Parameter	Delay [ps]
Register clk-to-Q	t_{pcq}	40
Register setup	t_{setup}	50
Multiplexer	t_{mux}	30
AND-OR gate	t_{AND-OR}	20
ALU	t_{ALU}	120
Decoder (control unit)	t_{dec}	25
Extend unit	t_{ext}	35
Memory read	t_{mem}	200
Register file read	t_{RFread}	100
Register file setup	$t_{RFsetup}$	60

Component Optimization

1/1 point (graded)

Alyssa P. Hacker is a crack circuit designer. She offers to speed up one of the functional units in Table 7.7 by 50% (i.e., cut the delay in half) to improve the overall performance of the single-cycle processor. Which unit should she optimize to get the greatest performance benefit?

- ○ Flip-flop
- ○ Multiplexer
- ○ ALU
- ◉ Memory
- ○ Register File

✔

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Performance

1/1 point (graded)

By what percentage will the execution time decrease? Express your answer as an integer without the percent sign (e.g. write 14% as 14).

27 ✔

27

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Modify the single-cycle RSIC-V processor to add support for the **sll** instruction. Keep your changes as simple as possible.

Use these hyperlinks to download the single-cycle processor Verilog from the textbook (riscvsingle.sv), the assembly language test program (riscvtest.s) and the machine language test program (riscvtest.txt).

Also download a modified test program (riscvtest_sll.s) that add a test of the sll instruction.

Changed Modules

1/1 point (graded)

Which modules require substantive changes (not just signals passing through)?

- [ ] adder
- [x] alu
- [x] aludec
- [ ] dmem
- [ ] immext
- [ ] regfile

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Machine Language

1.0/1.0 point (graded)

Create a riscvtest_sll.txt machine language program for your testbench. It should be identical to the riscvtest.txt program except it adds the sll instruction. Refer to the riscvtest_sll.s assembly language program to see the new instruction (sll x2, x2, x4). Translate this instruction into machine language and add it to the appropriate location in the riscvtest_sll.txt file. What is the machine language instruction? Express your answer as an 8-digit hexadecimal number with no leading 0x (e.g. FF718393).

00411133

00411133

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Hash

3.0/3.0 points (graded)

Edit the riscvsingle.sv file below to make your changes. When you run it on riscvtest.txt, you should get a hash of AB63135B if you haven't broken anything. Edit the imem module to $readmemh the riscvtest_sll.txt test code that adds tests for this instruction. Edit the testbench to check for the new expected answer (instead of 25). Run the testbench and debug your design. Report the hash below, as an 8-digit hexadecimal number with no leading 0x (e.g. AB63135B).

5B07A210

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