❖ Chapter 5: Building Blocks / Introduction

Lecture Practice due Apr 29, 2023 10:37 PDT Completed

Structural and Behavioral Verilog

1/1 point (graded)

Describing a circuit in SystemVerilog by instantiating submodules is an example of

- (●) Structural modeling
- ( ) Behavioral modeling
- ( ) Isomorphic modeling
- ( ) Dialectic modeling
- ( ) Fashion modeling

✔

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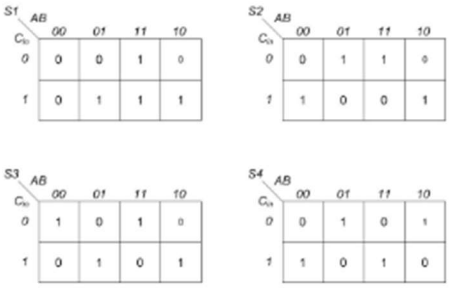
Consider the following K-maps.



Full Adder Sum Logic

1/1 point (graded)

Which K-map describes the S output of a full adder?

- ( ) S1
- ( ) S2
- ( ) S3
- (●) S4
- ( ) none of the above

✔

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Ripple Carry Adder Delay

1/1 point (graded)

Consider the propagation delay of an N-bit ripple carry adder computing Y = A + B. The ripple carry adder has no carry in or carry out terminals (although there are internal carries, of course). Instead of using the worst case delay of each full adder, let us consider the delays from particular inputs to particular outputs. Let each full adder have the following delays:

ABC_C: Delay from any input (A, B, or Cin) to Cout;
AB_S: Delay from A or B input to S;
C_S: Delay from Cin input to S.

(As should be intuitive, assume that each of these delays is roughly the same length; no one is many times larger than another)
Choose the proper expression for the propagation delay of the ripple carry adder.

- ○ N*max(ABC_C, AB_S, C_S)
- ◉ (N-1)ABC_C+C_S
- ○ (N-1)ABC_C+AB_S
- ○ N*ABC_C
- ○ N*AB_S
- ○ N(AB_S+ABC_C)

✔

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Lecture Practice due Jul 8, 2023 11:05 PDT

Propagate

1/1 point (graded)

A column in an adder propagates a carry if

- (●) either input is true
- ( ) both inputs are true
- ( ) neither input is true
- ( ) none of the above

✔

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Generate

1/1 point (graded)

A column in an adder generates a carry if

- ( ) either input is true
- (●) both inputs are true
- ( ) neither input is true
- ( ) none of the above

✔

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Propagate and Generate

1/1 point (graded)

The main reason carry-lookahead adders compute block propagate and generate signals is:

- ( ) to reduce power consumption by only having a fraction as many cells
- (●) to speed up the adder by quickly computing the carry out of a block as soon as the carry in becomes available, without waiting for the carry to ripple through every full adder in the block
- ( ) to confuse innocent students in digital design courses

✔

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Block Propagate

1/1 point (graded)

A block propagates a carry if

- ( ) at least one bit in the block propagates
- (●) every bit in the block propagates
- ( ) the most significant bit propagates, or the most signifciant bit generates and the next most significant bit propagates, and so forth.

✔

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Block Generate

1/1 point (graded)

A block generates a carry if

- ○ at least one bit in the block generates
- ○ every bit in the block generates
- ◉ the most significant bit generates, or the most significant bit propagates and the next most significant bit generates, and so forth.

✔

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Prefix Adders

1/1 point (graded)

Prefix adders:

- [x] can add numbers in time that scales with the logarithm of the number of bits
- [x] are best suited to adding relatively large numbers
- [ ] use fewer gates than any other kind of adder
- [ ] use less power than ripple carry adders
- [x] illustrate a technique that can apply to accelerating any other problem in which each output depends on all of the previous inputs

✔

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Prefix Adder Structure

1/1 point (graded)

An N-bit prefix adder is composed of

- ( ) N full adders cascaded such that the carry out of each column is the carry into the next column
- ( ) one level of gates to compute generate and propagate for each column, then a larger cell to compute the generate and propagate for each block, then AND/OR gates to ripple the carry across blocks, then one level of full adders to compute the sums for a block based on the carry into each block
- (•) one level of gates to compute generate and propagate for each column, then log_2 N levels of gates to combine the generates and propagates to compute the carry out of each column, then one level of XOR gates to compute the sum given the carry in.
- ( ) one level of gates to compute propagate for each column based on the generate signal, then log_2 N levels to compute the group propagate signals for each prefix group, then one level of AND gates to compute the sum based on the group prefixes.

✔

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Subtraction

1/1 point (graded)

Check all true statements:

- [x] To compute A - B, generate B' = -B by inverting the bits of B and adding 1, then add A + B'
- [x] The 1 can be added using the Cin input of a carry propagate adder so only a single adder is required
- [x] Subtractor hardware is the same whether the inputs are unsigned or twos complement numbers
- [ ] Subtractor hardware is the same whether the inputs are two's complement or sign/magnitude numbers

✔

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Subtraction

1/1 point (graded)

Subtract the following 4-bit binary numbers: 0101 - 0011 using binary arithmetic instead of converting to decmial. Express your answer as a 4-bit binary number.

0010 ✔

0010

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ALU Operation

1/1 point (graded)

Suppose you present a 4-bit ALU with inputs A = 1100, B = 0101, and ALUControl = 11. What is the output Y, expressed as a 4-bit binary number?

1101 ✔

1101

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More ALU Operation

1/1 point (graded)

Suppose you present a 4-bit ALU with inputs A = 1100, B = 0101, and ALUControl = 01. What is the output Y, expressed as a 4-bit binary number?

0111 ✔

0111

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Z Flag

1/1 point (graded)

When is the ALU Z flag asserted?

- ○ When the most significant bit of the result is 1.
- ◉ When all the bits of the result are 0. ✔
- ○ When the operation is addtion, the two inputs have the same sign, and the ouput has the opposite sign OR when the operation is subtraction, the two inputs have opposite signs, and the ouput has the opposite sign of the first input.
- ○ When the operation is addition or subtraction and the carry out of the adder is 1

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C Flag

1/1 point (graded)

When is the ALU C flag asserted?

- ○ When the most significant bit of the result is 1.
- ○ When all the bits of the result are 0.
- ○ When the operation is addtion, the two inputs have the same sign, and the ouput has the opposite sign OR when the operation is subtraction, the two inputs have opposite signs, and the ouput has the opposite sign of the first input.
- ◉ When the operation is addition or subtraction and the carry out of the adder is 1 ✔

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V Flag

1/1 point (graded)

When is the ALU V flag asserted?

- ○ When the most significant bit of the result is 1.
- ○ When all the bits of the result are 0.
- ◉ When the operation is addition, the two inputs have the same sign, and the output has the opposite sign OR when the operation is subtraction, the two inputs have opposite signs, and the output has the opposite sign of the first input.
- ○ When the operation is addition or subtraction and the carry out of the adder is 1.

✔

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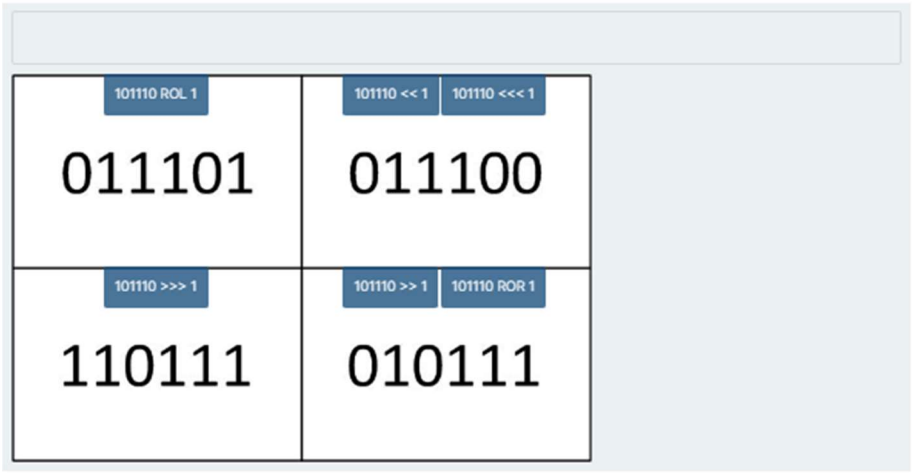
Shifters

1/1 point (graded)

Keyboard Help

PROBLEM

Drag each shift operation to its answer.



Reset

FEEDBACK

Good work! You can do binary shifts.

Multiplication and Division with Shifts

1/1 point (graded)

An arithmetic right shift by 3 is equivalent to

- multiplying a signed number by 3
- multiplying an unsigned number by 8
- dividing an unsigned number by 3
- dividing an unsigned number by 8
- dividing a signed number by 8 ✔

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Multiplication

1/1 point (graded)

Multiply the unsigned 4-bit binary numbers 0101 × 1001. Express your result as an 8-bit binary number.

00101101 ✔

00101101

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Fixed Point Numbers

1/1 point (graded)

Write -3.375 as a Q3.5 binary number.

10010100 ✔

10010100

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Decimal to Floating Point

1/1 point (graded)

Write -0.1875 as a single-precision floating point number. Express your answer with 8 lowercase hexadecimal digits.

be400000 ✔

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Floating Point Addition

1/1 point (graded)

By hand, add the following two single-precision floating point numbers, represented in hexadecimal: 40540000 + 40B80000. Express your result in hexadecimal, using lower-case letters where necessary.

41110000 ✔

Answer
Correct: Spiffy!

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Scan Chain

1/1 point (graded)

Suppose you have a system with thousands of flip-flops and lots of combinational logic. You'd like to be able to test the system by loading the flip-flops with desired bit patterns, running for a clock cycle, and reading out the contents of the flip-flops. However, you don't have thousands of pins available to directly observe and control each flip-flop. This is a good application for:

- ○ counters
- ◉ shift registers
- ○ ALUs
- ○ comparators
- ○ ROMs
- ○ dongles and widgets

✔

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Memory capacity

1/1 point (graded)

You need a memory that will hold 512 64-bit words. How many bits should the address input be?

9 ✔

9

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RAM

1/1 point (graded)

Check all that apply

- ☑ SRAM holds its value as long as power is applied, while DRAM periodically needs to be refreshed to avoid losing its contents
- ☐ SRAM will retain its value even after power is turned off
- ☑ DRAM is cheaper than SRAM because it only needs one transistor and one capacitor for each bit stored.
- ☑ Most memory in a computer or phone is DRAM because of cost

✔

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Logic with Lookup Tables

1/1 point (graded)

Consider a ROM implementing X = ABCD, Y = A+B+C+D (+ meaning OR), and Z = A ^ B. The ROM has:

- ○ 3 address inputs, 4 data outputs, and 32 bits of storage
- ○ 4 address inputs, 3 data outputs, and 36 bits of storage
- ◉ 4 address inputs, 3 data outputs, and 48 bits of storage
- ○ 16 address inputs, 3 data outputs, and 24 bits of storage

✔

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Logic with Lookup Tables: ROM Contents

1/1 point (graded)

In the question above, how many 1's are in the ROM?

24 ✔

24

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Register File Organization

1/1 point (graded)

A 3-ported register file (2 read ports and 1 write port) with 2^N entries x M bits has 3N address bits of address input, M bits of WriteData input, and 1 bit of WriteEnable input, for a total of 3N+M+1 bits of input. How many bits of input are required for a 5-ported register file (3 read and 2 write ports) with 32 entries of 64 bits each?

155 ✔

155

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Logic Elements: Combinational Logic

1/1 point (graded)

How many Cyclone IV LEs are required to compute X = ABCD and Y = ABCDEF?

2 ✔

2

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Hint | Save | Show answer

Logic Elements: Decoder

1/1 point (graded)

How many Cyclone IV LEs are required to build a 4:16 decoder

16 ✔

16

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Logic Elements: Shift Register

1/1 point (graded)

A 10-bit serial-to-parallel shift register takes a clock and a Sin serial input. It produces a 10-bit output Q. How many Cyclone IV LEs are needed?

10 ✔

10

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