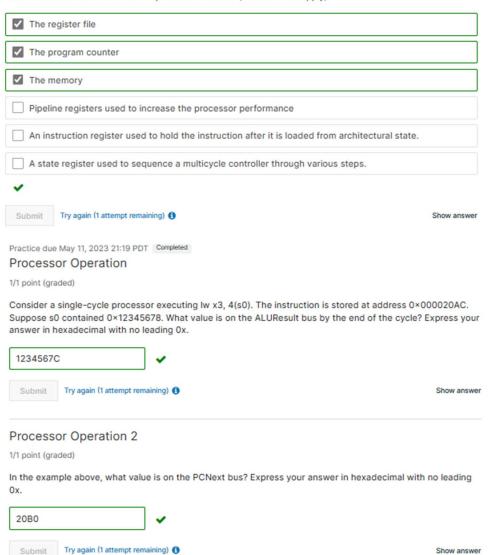
Chapter 7: Microarchitecture / Introduction

Practice due May 11, 2023 21:19 PDT Completed

Architectural State

1/1 point (graded)

The architectural state of a RISC-V processor includes (check all that apply):



Control Signals

1/1 point (graded)

Why is the ResultSrc control signal needed?

To determine whether Result is selected from ALUResult for beq or R-type i ReadData for lw.	nstructions, or from
O To determine wehther Result is 0 or 1	
What is the airspeed velocity of an unladen swallow?	
Submit Try again (1 attempt remaining) •	Show answe
mmExt	
/1 point (graded)	

When executing addi s0, s0, -1, what is ImmExt? Express your result as a 32-bit hexadecimal number with no leading 0x.



Control Signals

1/1 point (graded)

Which of the following instructions assert RegWrite? Check all that apply.

Try to answer the question from first principles about what the instructions do and what RegWrite does, before optionally checking your work against the truth table in the lecture.

✓ Iw
sw
R-type instructions
beq
✓
Submit Try again (1 attempt remaining) (1 Show answer
ALUOp
1/1 point (graded)
When ALUOp = 01, what does the ALU do?
O add
subtract
o and
O or
onot enough information to answer this question
✓
Submit Try again (1 attempt remaining) (1 Show answer
ALU Decoder Design
1/1 point (graded)
The ALU Decoder computes a combinational function of 7 inputs and 3 outputs. What is the most practical way to design the hardware to implement this function?
○ Karnaugh maps
inspection
sum of products and Boolean algebra
Describe the truth table in HDL and allow a logic synthesizer to optmize
○ finite state machines
O Petri networks
•
Submit Try again (1 attempt remaining) (3 Show answer

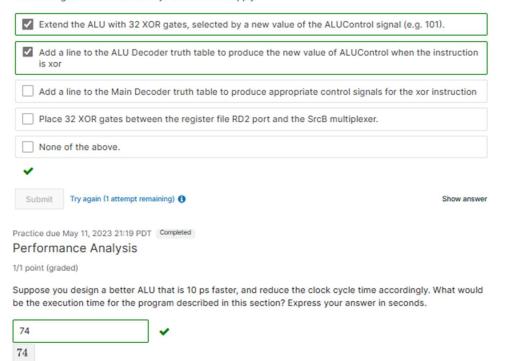
Try again (1 attempt remaining) (

Submit

xor instruction

1/1 point (graded)

Consider modifying the single-cycle processor to support the xor instruction, which is an R-type instruction. What changes would be necessary? Check all that apply.



Refer to the riscytest.asm code below:

```
# Test the RISCV processor.
# add, sub, and, or, slt, addi, lw, sw, beq, jal
# If successful, it should write the value 71 to address 84
                                                    Address
      Assembly
                               Description
main: addi x2, x0, 5
                              # initialize x2 = 5
                                                     0
addi x3, x0, 12 # initialize x3 = 12 4
 addi x7, x3, -9 # initialize x7 = 3 8
 or x4, x7, x2 # x4 = (3 OR 5) = 7 C
and x5, x3, x4 # x5 = (12 AND 7) = 4 10
 add x5, x5, x4 # x5 = 4 + 7 = 11 14
beq x5, x7, end # shouldn't be taken 18
 slt x4, x3, x4 # x4 = (12 < 7) = 0 1C
 beq x4, x0, around # should be taken 20
addi x5, x0, 0 # shouldn't happen 24
around: slt x4, x7, x2
                              \# x4 = (3 < 5) = 128
add x7, x4, x5 # x7 = 1 + 11 = 12 2C
 sub x7, x7, x2 # x7 = 12 - 5 = 7 30
 sw x7, 68(x3) # [80] = 7 34
 lw x2, 80(x0) # x2 = [80] = 7 38
 jal x3, end # save 64 in x3 3C
addi x2, x0, 1 # shouldn't happen 40
end: add x2, x2, x3 # x2 = 7 + 64 = 71 44
sw x2, 84(x0) # write mem[84] = 71 48
```

Implementation Error

1/1 point (graded)

Suppose there were a bug in the processor design that caused the processor to write PC rather than PC+4 as the return address of JAL. What value would be written to address 84 at the end of the program?



```
Practice due May 11, 2023 21:19 PDT Completed
```

Refer to the aludecoder Verilog module below:

```
module aludec(input logic
                                 opb5,
              input logic [2:0] funct3,
              input logic
                                 funct7b5,
              input logic [1:0] ALUOp,
              output logic [2:0] ALUControl);
  logic RtypeSub;
  assign RtypeSub = funct7b5 & opb5; // TRUE for R-type subtract
  always_comb
    case (ALUOp)
      2'600:
                            ALUControl = 3'b010; // addition
                            ALUControl = 3'b110; // subtraction
      2'b01:
      default: case(funct3) // R-type or I-type ALU
                 3'b000: if (RtypeSub)
                            ALUControl = 3'b110; // sub
                          else
                            ALUControl = 3'b010; // add, addi
                 3'b010:
                           ALUControl = 3'b111; // slt, slti
                 3'b110: ALUControl = 3'b001; // or, ori
                 3'b111: ALUControl = 3'b000; // and, andi
default: ALUControl = 3'bxxx; // unknown
               endcase
    endcase
endmodule
```

xor

1/1 point (graded)

xor is an R-type instruction with funct3=100. Suppose you've already modified the ALU to perform xor when ALUControl=101. What would you need to change in the aludecoder to finish supporting xor?





Submit Try again (1 attempt remaining) (3

Practice due May 11, 2023 21:19 PDT Completed Consider the multicycle datapath executing lw s0, 8(s1) Suppose the instruction is at address 2000. s0 contains 40 and s1 contains 5000. ALU Step 3 1/1 point (graded) During step 3, what is the value of ALUResult? 5008 5008 Try again (1 attempt remaining) 6 Submit Show answer ALU Step 6 1/1 point (graded) During step 6, what is the value of ALUResult? 2004 2004Try again (1 attempt remaining) 6 Submit Show answer

Submit Try again (1 attempt remaining) 1

Architectural State

1/1 point (graded)

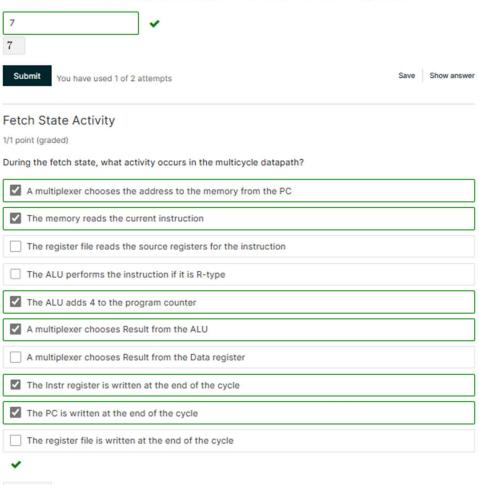
1/1 point (graded)
The multicycle datapath has registers Instr, Data, OldPC, A, B, and ALUOut that are not in the single-cycle datapath. Are these registers part of the architectural state of the multicycle processor?
Yes, because you can't build a multicycle processor without them.
Yes, because they contain bits of state, even though you could conceivably design a different multiyclce processor with different registers.
No, because architectural state only encompasses the state elements visible to the programmer.
No, because some of them have enable signals.
Submit Try again (1 attempt remaining) (3) Show answer
Single/Multicycle Comparison 1/1 point (graded)
As compared to the single-cycle processor, the multicycle processor has (check all that apply)
a unified instruction and data memory rather than two separate memories
✓ fewer adders
fewer multiplexers
more and bigger multiplexers
onnarchitectural state registers
•

Submit You have used 2 of 2 attempts

Instruction Decoder

1/1 point (graded)

The instruction decoder is a combinational function of A bits of input and B bits of output. What is A?



Multiplexer Control Signals

1/1 point (graded)

When a multiplexer control signal such as ALUSrcA is not specified in the FSM diagram, that means: It must be 0. It must be 1. It is a don't care. There is a bug in the FSM. Submit Save Show answer You have used 1 of 2 attempts Write Enable Signals 1/1 point (graded) When a write enable signal such as IRWrite is not specified in the FSM diagram, that means: It must be 0. It must be 1. It is a don't care. There is a bug in the FSM. Save Show answer Submit You have used 1 of 2 attempts Multicycle FSM 1/1 point (graded) When a sw instruction is being executed, what sequence of states does the FSM follow? O S0 Fetch, S1 Decode, S2 MemAdr, S3 MemRead, S4 MemWB S0 Fetch, S1 Decode, S2 MemAdr, S5 MemWrite S0 Fetch, S1 Decode, S6 ExecuteR, S7 ALUWB O S0 Fetch, S1 Decode, S2 MemAdr, S3 MemRead, S4 MemWB, S5 MemWrite, S6 ExecuteR, S7 ALUWB, S10 BEQ It depends on the contents of the register file Submit Save Show answer You have used 1 of 2 attempts

Decode State

1/1 point (graded)

Why are ALUSrcA, ALUSrcB, and ALUOp used in S1?

○ To execute R-type instructions.		
To compute the base address + offset for lw and sw.		
To compute the branch target address for branches, while the ALU otherwise would be	e idle.	
To compute the branch target address, which is needed in subsequent steps for all inst	truction	ns.
✓		
Submit You have used 1 of 2 attempts	Save	Show answer
Practice due Jul 20, 2023 22:46 PDT Completed		
1/1 point (graded)		
Suppose you were running a program with a different mix of instructions than SPECInt. Supp frequencies were 20% loads, 20% branches, 5% stores, and 55% R-type. What would the av		
4		
Submit You have used 1 of 2 attempts	Save	Show answer

Practice due Jul 20, 2023 22:46 PDT Completed

Design Methodology

1/1 point (graded)

Our	pipelined	processor	is designed by
-----	-----------	-----------	----------------

partitioning the single-cycle processor into multiple stages		
partitioning the multicycle processor into multiple stages		
starting from first principles and connecting architectural state as necessary for early starting from first principles and connecting architectural state as necessary for early starting from first principles and connecting architectural state as necessary for early starting from first principles and connecting architectural state as necessary for early starting from first principles and connecting architectural state as necessary for early starting from first principles and connecting architectural state as necessary for early starting from first principles and connecting architectural state as necessary for early starting from the first principles and connecting architectural state as necessary for early starting from the first principles and connecting architectural state as necessary for early starting from the first principles are starting from the first	ch instruc	tion
✓		
Submit You have used 1 of 2 attempts	Save	Show answe
Pipeline Operation		
/1 point (graded)		
Referring to the Pipelined Processor Abstraction slide, which registers are being read from cycle 4? Check all that apply.	m the regi	ster file on
_ s0		
s2		
s5		
✓ s8		
s11		
to		
▼ t1		
t5		
t4		
•		
Submit You have used 1 of 2 attempts	Save	Show answe

More Pipeline Operation	
1/1 point (graded)	
Referring again to the Pipelined Processor Abstraction diagram, on which cycles are the datused?	ta memory being
1	
_ 2	
3	
☑ 4	
5	
□ 6	
7	
▼ 8	
9	
□ 10	
~	
Submit You have used 1 of 2 attempts	Save Show answer

Practice due Jul 20, 2023 22:46 PDT Completed Consider the following program running on our pipelined processor. Suppose s0 initially had the value 42. addi s0, zero, 10 add s1, s0, s0 **Program Operation** 1/1 point (graded) If the processor handles hazards correctly, what value should be in s1 when the program completes? 20 20 Submit Save Show answer You have used 1 of 2 attempts Hazards 1/1 point (graded) Suppose the pipelined processor was missing the hazard unit. What value would be in s1 when the program completes? 84 84 Submit Save Show answer You have used 1 of 2 attempts Practice due Jul 20, 2023 22:46 PDT Completed **Branch Misprediction Penalty** 1/1 point (graded) What is the branch misprediction penalty for our pipelined processor? Express your answer in cycles or instructions. 2 2 Save Show answer Submit You have used 1 of 2 attempts Practice due Jul 20, 2023 22:46 PDT Completed Pipelined CPI 1/1 point (graded) Suppose the pipelined processor ran a program with 100 billion instructions, of which 20% are loads, 12% are stores, 15% are branches, and the remainder are R-type. Suppose that 25% of the loads are used by the next instruction and that 1/3 of the branches are mispredicted. What is the average CPI? 1.15 1.15

Save Show answer

Submit

You have used 1 of 2 attempts

Deep Pipelines

1/1 point (graded)

A deeper pipeline may improve performance by:

Reducing the cycle time		
Reducing the CPI		
Reducing the number of instructions to execute		
✓		
Submit You have used 1 of 2 attempts	Save	Show answer
Branch Predictors		
1/1 point (graded)		
A branch predictor may improve performance by:		
Reducing the cycle time		
Reducing the CPI		
Reducing the number of instructions to execute		
✓		
Submit You have used 1 of 2 attempts	Save	Show answer
Practice due Jul 20, 2023 22:46 PDT Completed		
Register Renaming		
1/1 point (graded)		
Benefits of register renaming are (select all that apply):		
Eliminating WAR and WAW hazards by introducing more registers to prevent these h when a finite number of registers need to be recycled for different purposes.	azards tl	hat occur
Eliminating RAW hazards by reordering a program.		
Reducing the cycle time by using a smaller register file.		
☐ Increasing the IPC by providing more execution units.		
~		
Submit You have used 1 of 2 attempts	Save	Show answer

Processes and Threads

1/1 point (graded)

Which statement correctly describes the relationship of processes and threads?		
Each process has exactly one thread.		
A process may have more than one thread.		
A thread may have more than one process.		
✓		
Submit You have used 1 of 2 attempts	Save	Show answer
Multithreaded Processors		
1/1 point (graded)		
Multithreading can improve the performance of a computer by:		
Reducing the time to switch between threads		
Running several threads concurrently on mulitple cores		
Reducing the cycle time		
Executing instructions out of order		
•		
Submit You have used 1 of 2 attempts	Save	Show answer
Multiprocessors		
1/1 point (graded)		
Multiprocessing can improve the performance of a computer by:		
Reducing the time to switch between threads		
Running several threads concurrently on mulitple cores		
Reducing the cycle time		
Executing instructions out of order		
✓		
Submit You have used 1 of 2 attempts	Save	Show answer