Lecture Notes in Computer Science 6760

Commenced Publication in 1973
Founding and Former Series Editors:
Gerhard Goos, Juris Hartmanis, and Jan van Leeuwen

Per Stenström (Ed.)

Transactions on High-Performance Embedded Architectures and Compilers IV

Springer

Volume Editor

Per Stenström
Chalmers University of Technology
Department of Computer Science and Engineering
412 96 Gothenburg, Sweden
E-mail: per.stenstrom@chalmers.se

ISSN 0302-9743 (LNCS)
ISSN 1864-306X (THIPEAC)
ISBN 978-3-642-24567-1
DOI 10.1007/978-3-642-24568-8
Springer Heidelberg Dordrecht London New York

e-ISSN 1611-3349 (LNCS)
e-ISSN 1864-3078 (THIPEAC)
e-ISBN 978-3-642-24568-8

Library of Congress Control Number: 2011940725

CR Subject Classification (1998): B.2, C.1, D.3.4, B.5, C.2, D.4

Typesetting: Camera-ready by author, data conversion by Scientific Publishing Services, Chennai, India

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

Editor-in-Chief's Message

It is my pleasure to introduce you to the fourth volume of *Transactions on High-Performance Embedded Architectures and Compilers*. This journal was created as an archive for scientific articles in the converging fields of high-performance and embedded computer architectures and compiler systems. Design considerations in both general-purpose and embedded systems are increasingly being based on similar scientific insights. For example, a state-of-the-art game console today consists of a powerful parallel computer whose building blocks are the same as those found in computational clusters for high-performance computing. Moreover, keeping power/energy consumption at a low level for high-performance general-purpose systems as well as in, for example, mobile embedded systems is equally important in order to either keep heat dissipation at a manageable level or to maintain a long operating time despite the limited battery capacity. It is clear that similar scientific issues have to be solved to build competitive systems in both segments. Additionally, for high-performance systems to be realized – be it embedded or general-purpose – a holistic design approach has to be taken by factoring in the impact of applications as well as the underlying technology when making design trade-offs. The main topics of this journal reflect this development and include (among others):

- Processor architecture, e.g., network and security architectures, application-specific processors and accelerators, and reconfigurable architectures
- Memory system design
- Power-, temperature-, performance-, and reliability-constrained designs
- Evaluation methodologies, program characterization, and analysis techniques
- Compiler techniques for embedded systems, e.g, feedback-directed optimization, dynamic compilation, adaptive execution, continuous profiling/ optimization, back-end code generation, and binary translation/optimization
- Code size/memory footprint optimizations

This volume contains 21 papers divided into four sections. The first section contains five regular papers. The second section is a special one containing the top four papers from the 4th International Conference on High-Performance and Embedded Architectures and Compilers - HiPEAC. I would like to thank Michael O'Boyle (University of Edinburgh) and Margaret Martonosi (Princeton University) for acting as guest editors of that section. The contributions in this section deal with issues related to exploiting parallelism and to reducing power consumption in emerging multicore architectures.

The third section contains a set of six papers providing a snap-shot from the Workshop on Software and Hardware Challenges of Many-Core Platforms (SHCMP 2008). I am indebted to Albert Cohen (INRIA), Xinmin Tian (Intel) and Wenguang Chen (Tsinghua University) for putting together this special section.

Finally, the fourth section provides a snap-shot of six papers from the 8th IEEE International Symposium on Systems, Architectures, Modeling and Simulation, 2008 (SAMOS VIII). I am very much indebted to Nikitas Dimopoulos (University of Victoria), Walid Najjar (UC Riverside), Mladen Berekovic (Technical University of Braunschweig), and Stephan Wong (Delft University of Technology) for their effort in putting together this special section.

In the third volume of *Transactions of HiPEAC*, one of the papers entitled "Software-Level Instruction-Cache Leakage Reduction Using Value-Dependence of SRAM Leakage in Nanometer Technologies" by Maziar Goudarzi et al. was incorrectly listed as belonging to the special issue on the MULTIPROG workshop. This paper was indeed a regular paper and should have been listed accordingly.

In closing, I would like to mention that the editorial board has worked diligently to handle the papers for the journal. I would like to thank all the contributing authors, editors, and reviewers for their excellent work.

Per Stenström, Chalmers University of Technology
Editor-in-Chief
Transactions on HiPEAC

4th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC)

Selected Papers

In January 2009 the 4th International Conference on High-Performance Embedded Architectures was held in the beautiful city of Paphos, Cyprus. We were fortunate to attract 97 submissions of which 27 were selected for presentation at the conference. After the conference and in consultation with the Program Committee, we selected four of the most highly-rated and best-received papers to be invited for inclusion in this volume. The authors have prepared extended versions, which are included here.

The first paper by Azevedo et al. addresses the problem of application scaling on multi-core systems. It develops a new algorithm to exploit inter-frame parallelism in the widely-used video decoder H.264. Combining this with existing intra-frame parallelism leads to a new technique that gives scalable performance on a greater number of processors than existing techniques.

In the second paper by Muralidhara and Kandemir, multi-core utilization is again the subject of study. This paper addresses the energy cost of within-chip communication. The authors develop a new Markov-based approach that predicts when links can be powered down. This accurate scheme is able to deliver significant power reduction without incurring excessive performance impact.

The third paper, by Vandeputte and Eeckhout, tackles the issue of workload selection for design and evaluation of computer systems. Using representative sampling, they propose a technique that can automatically select benchmarks that stretch a processor's capabilities. Using threshold clustering they can find stress patterns significantly faster than standard approaches.

Finally, the fourth paper combines the issues of application behavior and power reduction. Here, Henry and Nazhandali tackle the widely used FFT algorithm and investigate the use of partitioning a hardware implementation of the algorithm into two different circuit technologies. They show that the correct partition can deliver a large energy reduction, significantly increasing battery life.

Michael F.P. O'Boyle
Margaret Martonosi

Workshop on Software and Hardware Challenges of Many-Core Platforms (SHCMP)

Selected Papers

Processors built with two or more on-chip cores are already shipping in volume. Soon, most mainstream computers could be configured with many-core processors built with eight or more on-chip cores and possibly on-chip heterogeneous many-cores. This shift to an increasing number of cores places new burdens on mainstream software and will require new software tools for developing systems. Meanwhile, parallel programming and computing has come a long way boosting the performance for numerical scientific applications. However, today, mainstream application programmers are challenged by the daunting task of parallelizing general non-numerical applications and must have reasonable knowledge of architecture, compilers, threading libraries and multithreading. It is time to explore new technologies so that general programs can be multithreaded efficiently and effectively for many-core platforms.

In this context, a workshop on Software and Hardware Challenges of Many-Core Platforms (SHCMP 2008) was held together with the 35th International Symposium on Computer Architecture (ISCA 2008). It provided a forum for the presentation and discussion of research on all aspects of software and hardware for developing applications on many-core platforms.

We received 23 submissions in response to a call for papers, and each submission was evaluated by three reviewers. Based on feedback received, the Program Committee accepted 13 papers which were presented in the SHCMP 2008 workshop held on June 22, 2008. Of the 13 accepted papers, the 8 papers ranked at the top were selected by the SHCMP 2008 Program Committee. We invited the authors of these eight papers to submit a revised version to be considered for publication in this special issue. Authors of seven out of eight invited papers accepted the invitation and submitted their revised journal version. The revised papers were reviewed by the same reviewers again to ensure the authors addressed the issues raised in the first round of review. Finally, of the eight papers, six were accepted for inclusion in this Special Section.

We are deeply grateful to the Program Committee members. The Program Committee was working under a tight schedule. We wish to thank all Program Committee members for their assistance in organizing the SHCMP 2008 program and determining the paper selection guidelines. Without the solid work and dedication of these committee members, the success of the program and the workshop itself would not have been possible. We appreciate the contribution of Wenguang Chen's local team at Tsinghua University Beijing who organized and handled the workshop website for paper submission and review.

We would also like express our gratitude for the support and sponsorship we received from the Steering Committee and the 35th International Symposium on Computer Architecture (ISCA 2008) Organizing Committee for their support in this endeavor. Finally, we are grateful to the HiPEAC network, and Per Stenstrom in particular, for making this special issue possible.

Albert Cohen
Xinmin Tian
Wenguang Chen

8th IEEE International Symposium on Systems, Architectures, Modeling and Simulation (SAMOS VIII)

Selected Papers

It is our pleasure to introduce this special issue that includes selected papers from the International Symposium on Systems, Architectures, Modeling and Simulation 2008 (SAMOS VIII). The International Symposium on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS) is an annual gathering of highly qualified researchers from academia and industry, sharing a three-day lively discussion on the quiet and inspiring northern mountainside of the Mediterranean island of Samos. The symposium is unique in the sense that not only solved research problems are presented and discussed, but also (partly) unsolved problems and in-depth topical reviews can be unleashed in the scientific arena. It comprises two co-located events: The International SAMOS Conference and the SAMOS Workshop. In 2008, more than 200 papers were submitted for these two events. After a very competitive selection process only about 30% of these papers were selected for presentation. According to the symposium's ranked results and the results of a second stage review process of all presentations from the SAMOS workshop and conference, ten papers were invited to this special issue, out of which the following seven papers were selected for publication in this special issue. These works address a broad spectrum of issues in embedded systems architecture and design and range from design space exploration environments to networking.

The paper by Beiu et al. presents an interesting use of Rent's rule to compare the connectivity of a variety of networks. The authors further utilize Rent's rule to also compare the connectivity of the brain and show through their analysis that two-layer hierarchical networks mimic the brain's connectivity, and that particular combinations of parameters produce global networks with significantly reduced complexity.

The paper by Llorente et al. presents two novel packet segmentation algorithms targeting network processors. These algorithms aim to achieve increased system throughput by balancing the number of segments per packet to the memory efficiency.

The paper by Osborne et al. presents a method of developing energy-efficient run-time reconfigurable designs. The authors propose to deactivate part of the design by restricting the accuracy of the computations (i.e., optimizing the word length) and then select the most optimal reconfiguration strategy. The authors have developed a model through which they determine the conditions that establish when the bitstream reconfiguration method is more efficient than multiplexing. They have applied their approach to various case studies including ray tracing, vector multiplication B-Splines etc.

The paper by Rullman and Merker develops a cost model for reconfigurable architectures. Based on a general module transition model (MTM), the authors develop two metrics that estimate the reconfiguration time and reconfiguration size. These two quantities constitute the reconfiguration cost. The model is then applied to analyze costs at different levels of abstraction. Benchmark results show the efficacy of the method in lowering the reconfiguration costs.

The paper by Plishker et al. presents a new dataflow approach that enables the description of heterogeneous applications utilizing multiple forms of dataflow. Existing dataflow models are translated to the new dataflow formalism. A simulation environment allows designers to model and verify the designs. The paper provides a design example based on polynomial evaluation. A programmable polynomial evaluation accelerator (PEA) is presented, as well as a design employing two PEAs each targeting a different polynomial function (hence the heterogeneity).

The paper by Cope et al. presents a design exploration tool that is capable of exploring the customization options for a homogeneous multiprocessor (HoMP). The impact of architectural parameters on the performance of a variety of algorithms is explored and this is used to suggest post-fabrication optimizations where reconfigurable logic (RL) can be used to optimize the architecture as suggested during the exploration. The examples taken are from the domain of video processing utilizing graphics processing units; however, the tool is general enough to be applicable to a larger range of architectures.

The paper by Jaddoe et al. focuses on the problem of calibrating the analytical performance models used in system-level simulation environments. To accomplish this goal, the authors use the notion of separation of concerns (i.e., the decoupling of the computational requirements of an application from the capabilities of the architecture). The computational requirements of an application are described as signatures, i.e., vectors of instruction counts from an abstract instruction set (AIS) that expresses the application. The architectural capabilities are then expressed as the clock cycles required for an application (or operation) to run on a particular architecture. The signatures of several applications (operations) from a training set are then used to derive a best fit estimate of cycles per (AIS) instruction. These processor signatures can now be used to estimate the time (in terms of cycles) an application would require to run on a particular architecture. The paper presents experimental results of the application of the said approach in the mapping of a motion-JPEG encoder to an MP-Soc.

We would like to thank all the authors who submitted manuscripts for this special issue. Special thanks go to all the reviewers for their valuable comments, criticism, and suggestions. The investment of their time and insight is very much appreciated and helped to generate this selection of high-quality technical papers. We also appreciate the support from the editor-in-chief and publisher of the *Transactions on HiPEAC* for organizing this special issue.

Nikitas Dimopoulos
Walid Najjar
Mladen Berekovic
Stephan Wong

Editorial Board

Per Stenström is a professor of computer engineering at Chalmers University of Technology. His research interests are devoted to design principles for high-performance computer systems and he has made multiple contributions to high-performance memory systems in particular. He has authored or co-authored three textbooks and more than 100 publications in international journals and conferences. He regularly serves Program Committees of major conferences in the computer architecture field. He is also an associate editor of *IEEE Transactions on Parallel and Distributed Processing Systems*, a subject-area editor of the *Journal of Parallel and Distributed Computing*, an associate editor of the *IEEE TCCA Computer Architecture Letters*, and the founding Editor-in-Chief of *Transactions on High-Performance Embedded Architectures and Compilers*. He co-founded the HiPEAC Network of Excellence funded by the European Commission. He has acted as General and Program Chair for a large number of conferences including the ACM/IEEE International Symposium on Computer Architecture, the IEEE High-Performance Computer Architecture Symposium, and the IEEE International Parallel and Distributed Processing Symposium. He is a Fellow of the ACM and the IEEE and a member of Academia Europaea and the Royal Swedish Academy of Engineering Sciences.

Koen De Bosschere obtained his PhD from Ghent University in 1992. He is a professor in the ELIS Department at the Universiteit Gent where he teaches courses on computer architecture and operating systems. His current research interests include: computer architecture, system software, code optimization. He has co-authored 150 contributions in the domain of optimization, performance modeling, microarchitecture, and debugging. He is the coordinator of the ACACES research network and of the European HiPEAC2 network. Contact him at Koen.DeBosschere@elis.UGent.be.

Jose Duato is Professor in the Department of Computer Engineering (DISCA) at UPV, Spain. His research interests include interconnection networks and multiprocessor architectures. He has published over 340 papers. His research results have been used in the design of the Alpha 21364 microprocessor, and the Cray T3E, IBM BlueGene/L, and Cray Black Widow supercomputers. Dr. Duato is the first author of the book *Interconnection Networks: An Engineering Approach*. He served as associate editor of IEEE TPDS and IEEE TC. He was General Co-chair of ICPP 2001, Program Chair of HPCA-10, and Program Co-chair of ICPP 2005. Also, he served as Co-chair, Steering Committee member, Vice-Chair, or Program Committee member in more than 55 conferences, including HPCA, ISCA, IPPS/SPDP, IPDPS, ICPP, ICDCS, Europar, and HiPC.

Manolis Katevenis received the PhD degree from U.C. Berkeley in 1983 and the ACM Doctoral Dissertation Award in 1984 for his thesis on "Reduced Instruction Set Computer Architectures for VLSI." After a brief term on the faculty of Computer Science at Stanford University, he is now in Greece, and has been with the University of Crete and with FORTH since 1986. After RISC, his research has been on interconnection networks and interprocessor communication. In packet switch architectures, his contributions since 1987 have been mostly in per-flow queueing, credit-based flow control, congestion management, weighted round-robin scheduling, buffered crossbars, and non-blocking switching fabrics. In multiprocessing and clustering, his contributions since 1993 have been on remote-write-based, protected, user-level communication.

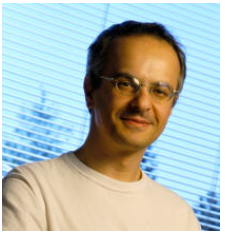
His home URL is http://archvlsi.ics.forth.gr/∼kateveni.

Michael O'Boyle is a professor in the School of Informatics at the University of Edinburgh and an EPSRC Advanced Research Fellow. He received his PhD in Computer Science from the University of Manchester in 1992. He was formerly an SERC Postdoctoral Research Fellow, a Visiting Research Scientist at IRISA/INRIA Rennes, a Visiting Research Fellow at the University of Vienna and a Visiting Scholar at Stanford University. More recently he was a Visiting Professor at UPC, Barcelona.

Dr. O'Boyle's main research interests are in adaptive compilation, formal program transformation representations, the compiler impact on embedded systems, compiler-directed low-power optimization and automatic compilation for parallel single-address space architectures. He has published over 50 papers in international journals and conferences in this area and manages the Compiler and Architecture Design group consisting of 18 members.

Cosimo Antonio Prete is full professor of Computer Systems at the University of Pisa, Italy, and faculty member of the PhD School in Computer Science and Engineering (IMT), Italy. He is coordinator of the graduate degree program in Computer Engineering and Rector's Adviser for Innovative Training Technologies at the University of Pisa. His research interests are focused on multiprocessor architectures, cache memory, performance evaluation and embedded systems. He is an author of more than 100 papers published in international journals and conference proceedings. He has been project manager for several research projects, including: the SPP project, OMI, Esprit IV; the CCO project, supported by VLSI Technology, Sophia Antipolis; the ChArm project, supported by VLSI Technology, San Jose, and the Esprit III Tracs project.

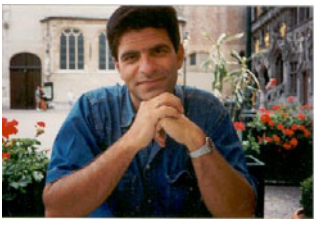
André Seznec is "directeur de recherches" at IRISA/INRIA. Since 1994, he has been the head of the CAPS (Compiler Architecture for Superscalar and Special-purpose Processors) research team. He has been conducting research on computer architecture for more than 20 years. His research topics have included memory hierarchy, pipeline organization, simultaneous multithreading and branch prediction. In 1999–2000, he spent a sabbatical with the Alpha Group at Compaq.



Olivier Temam obtained a PhD in computer science from the University of Rennes in 1993. He was assistant professor at University of Versailles from 1994 to 1999, and then professor at University of Paris Sud until 2004. Since then, he is a senior researcher at INRIA Futurs in Paris, where he heads the Alchemy group. His research interests include program optimization, processor architecture, and emerging technologies, with a general emphasis on long-term research.

Theo Ungerer is Chair of Systems and Networking at the University of Augsburg, Germany, and Scientific Director of the Computing Center of the University of Augsburg. He received a Diploma in Mathematics at the Technical University of Berlin in 1981, a Doctoral Degree at the University of Augsburg in 1986, and a second Doctoral Degree (Habilitation) at the University of Augsburg in 1992. Before his current position he was scientific assistant at the University of Augsburg (1982-89 and 1990-92), visiting assistant professor at the University of California, Irvine (1989-90), professor of computer architecture at the University of Jena (1992-1993) and the Technical University of Karlsruhe (1993-2001). He is Steering Committee member of HiPEAC and of the German Science Foundation's priority programme on "Organic Computing." His current research interests are in the areas of embedded processor architectures, embedded real-time systems, organic, bionic and ubiquitous systems.

Mateo Valero obtained his PhD at UPC in 1980. He is a professor in the Computer Architecture Department at UPC. His research interests focus on high-performance architectures. He has published approximately 400 papers on these topics. He is the director of the Barcelona Supercomputing Center, the National Center of Supercomputing in Spain. Dr. Valero has been honored with several awards, including the King Jaime I by the Generalitat Valenciana, and the Spanish national award "Julio Rey Pastor" for his research on IT technologies. In 2001, he was appointed Fellow of the IEEE, in 2002 Intel Distinguished Research Fellow and since 2003 he has been a Fellow of the ACM. Since 1994, he has been a foundational member of the Royal Spanish Academy of Engineering. In 2005 he was elected Correspondant Academic of the Spanish Royal Academy of Sciences, and his native town of Alfamén named their Public College after him.



Georgi Gaydadjiev is a professor in the computer engineering laboratory of the Technical University of Delft, The Netherlands. His research interests focus on many aspects of embedded systems design with an emphasis on reconfigurable computing. He has published about 50 papers on these topics in international refereed journals and conferences. He has acted as Program Committee member of many conferences and is subject area editor for the *Journal of Systems Architecture*.

Table of Contents

Regular Papers

4th International Conference on High-Performance and Embedded Architectures and Compilers – HiPEAC (Selected Papers)

Workshop on Software and Hardware Challenges of Many-core Platforms – SHCMP (Selected Papers)

8th IEEE International Symposium on Systems, Architectures, Modeling and Simulation – SAMOS VIII (Selected Papers)