

Global Feature Extractor (gFEX) Readout



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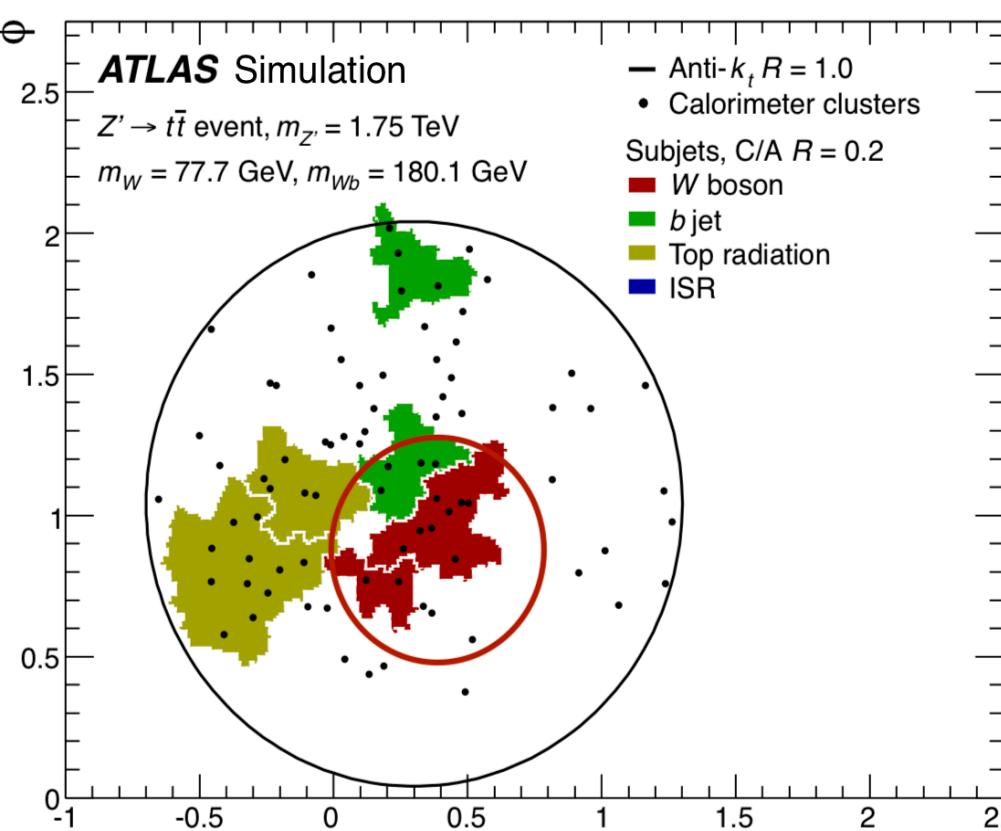
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Abstract

The Global Feature Extractor (gFEX) is a new part of the ATLAS level 1 calorimeter trigger subsystem that will be installed during the Phase-I upgrade. It is designed to maintain the level 1 trigger acceptance rate as the LHC luminosity increases and to increase sensitivity to interesting physics channels such as boosted topologies and events with large missing transverse energy. Testing and validating the firmware on the board is underway. And the process of integrating the board into the larger readout chain is beginning.

Motivation

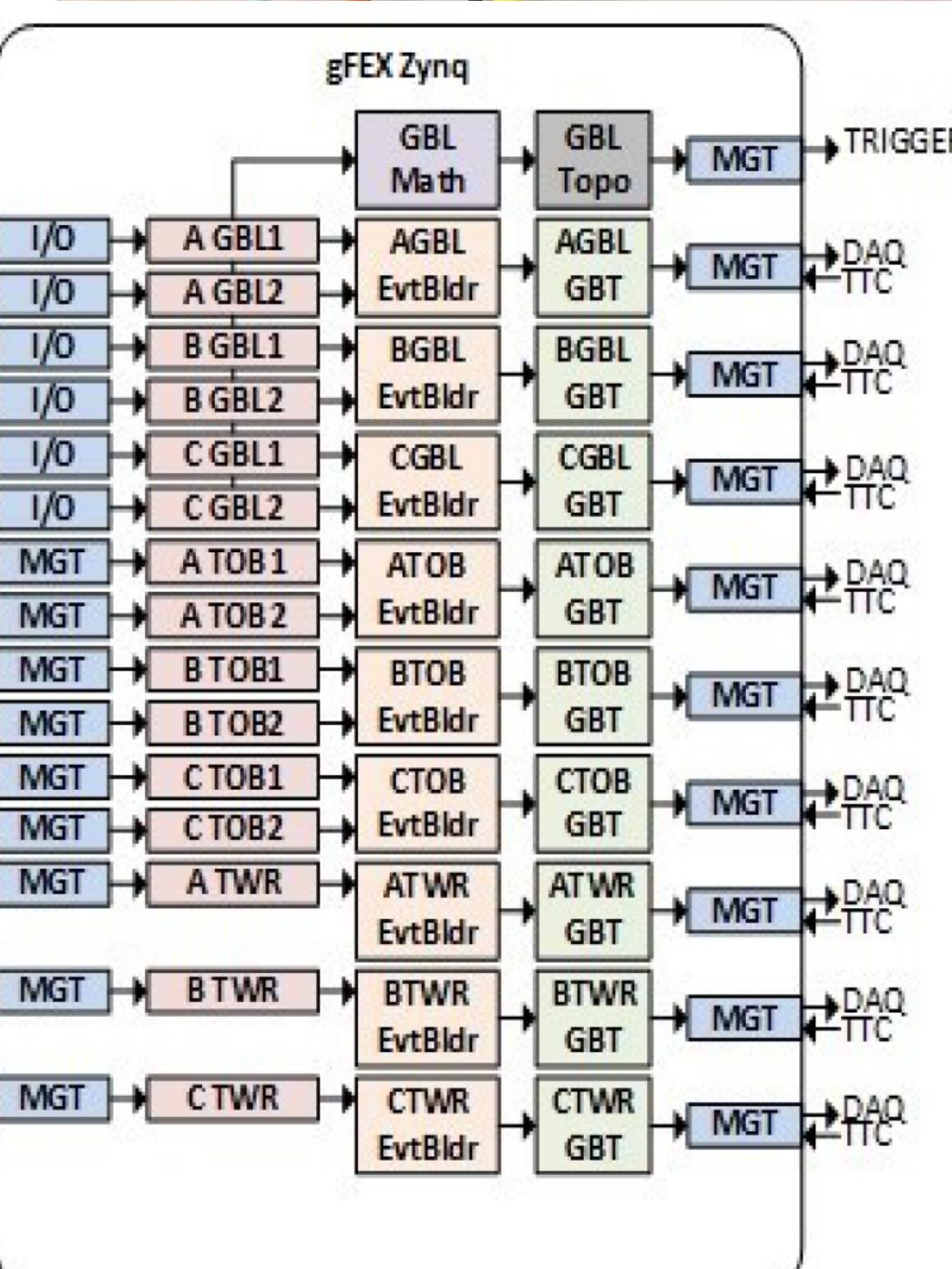
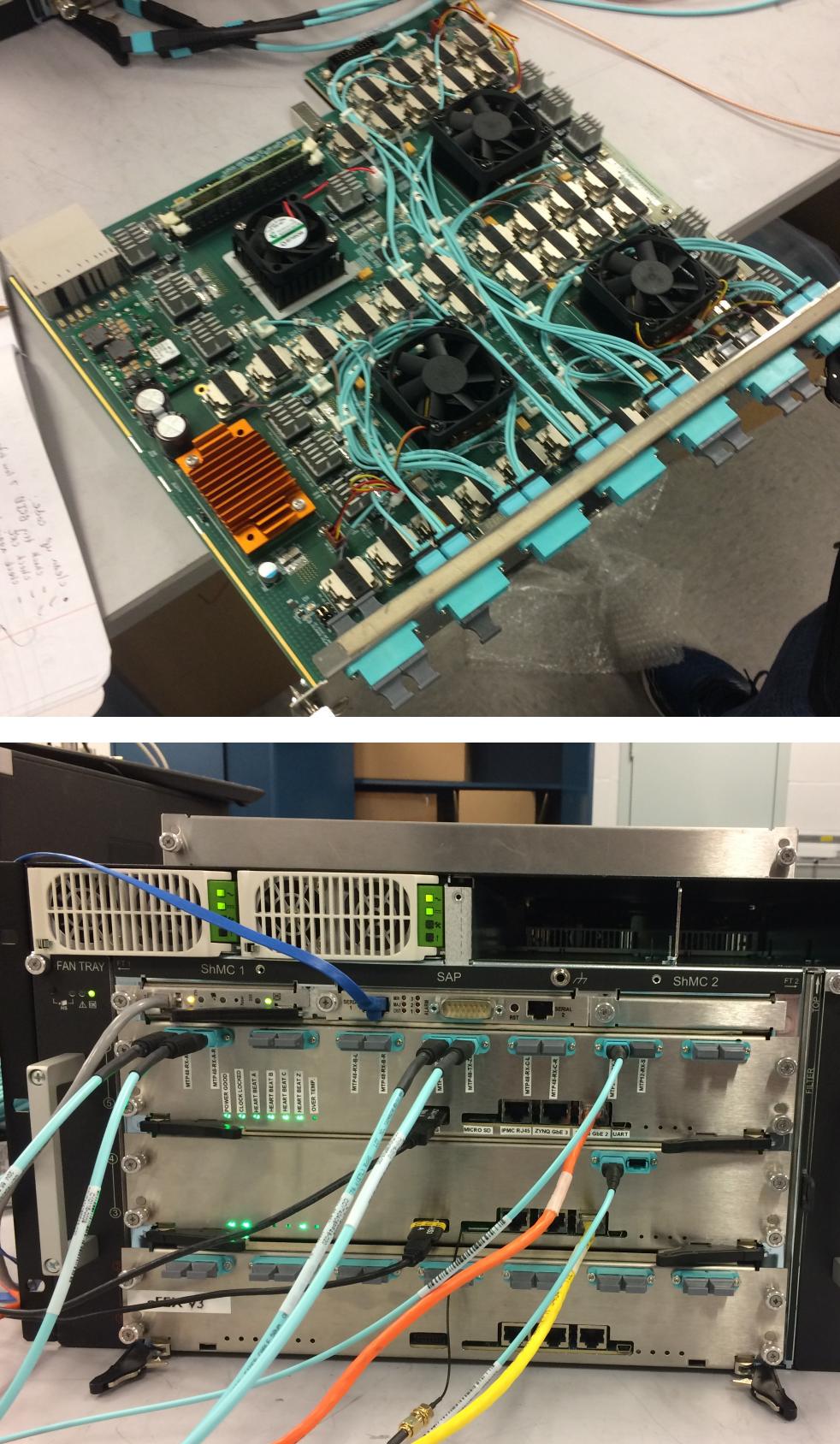
- Maintain manageable trigger acceptance rates in Run 3 and beyond
- Create more sensitive L1 boosted object triggers
- The gFEX supports several different methods for Missing E_T calculation which enables flexibility for algorithms at L1.
- Exploit the ability to scan the entire calorimeter at once to select interesting events
- Versatile enough to operate beyond Run 3 during the HL-HLC
- Event-by-event pileup subtraction capability



(Figure 24a from: ATLAS-TDR-029)

gFEX Board Overview

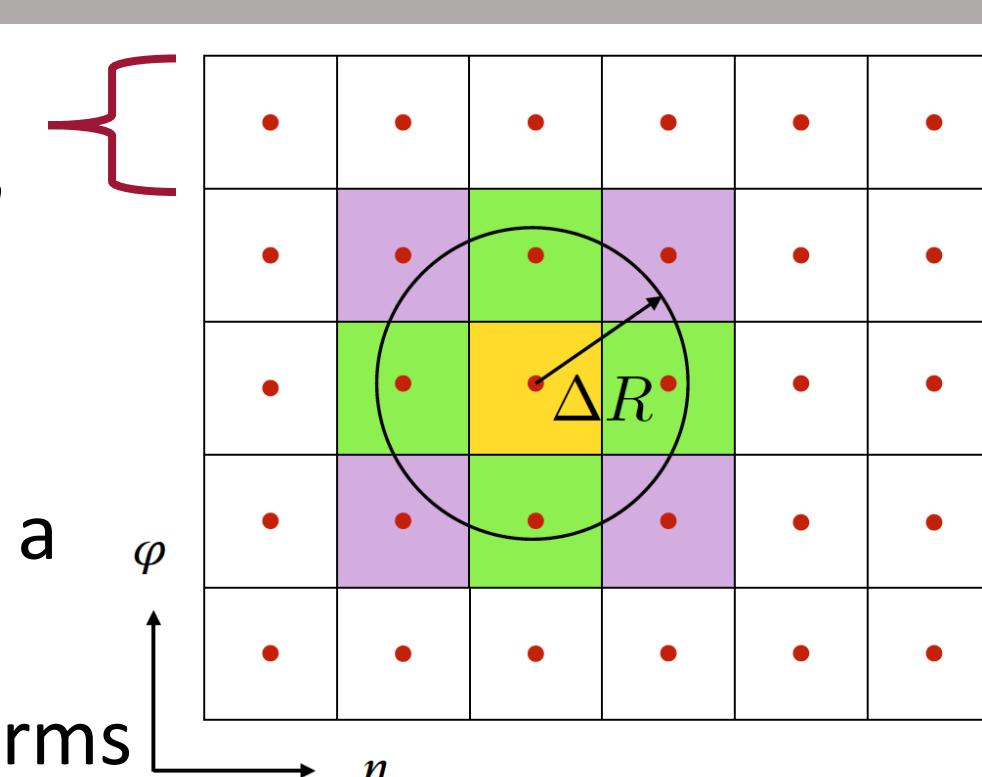
- 1 Zynq® Ultrascale+ MPSoC (PS and PL on the same chip)
- 3 Virtex Ultrascale+ processor FPGAs
- Outputs to FELIX-SWROD and L1Topo
- Trigger object output and full gTower readout on as-needed basis
- Modular readout design
- “Plug-and-play” trigger algorithms



“Jets Without Jets Algorithm”

Bertolini, Chan, and Thaler, *Jet Observables Without Jet Algorithms*. 2014
arXiv:1310.7584v2 [hep-ph]

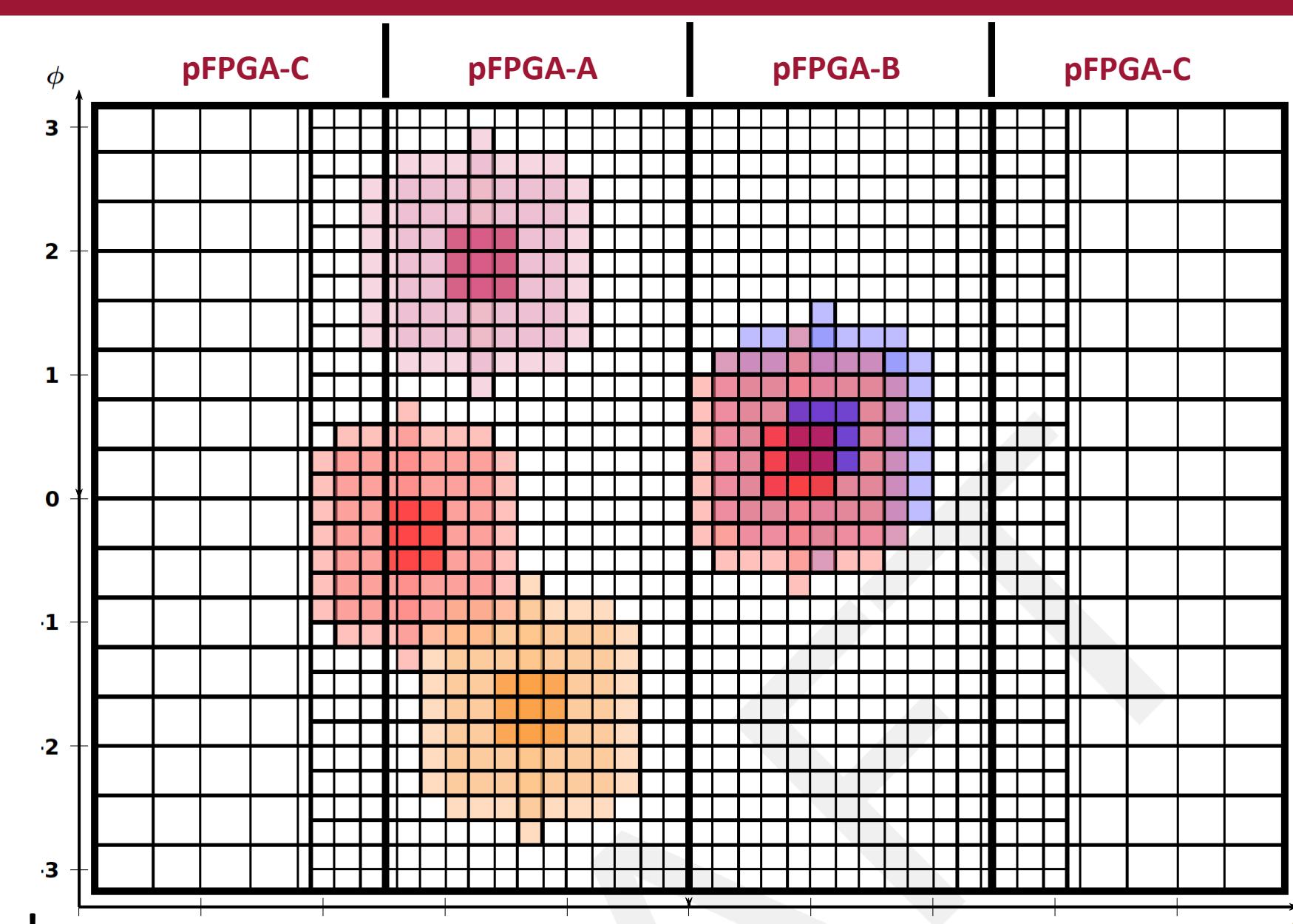
“gTower” := A sum of electromagnetic and hadronic calorimeter towers, most have a size of 0.2×0.2 in $\Delta\phi \times \Delta\eta$



Large-Area Jets Algorithm

Algorithm Outline:

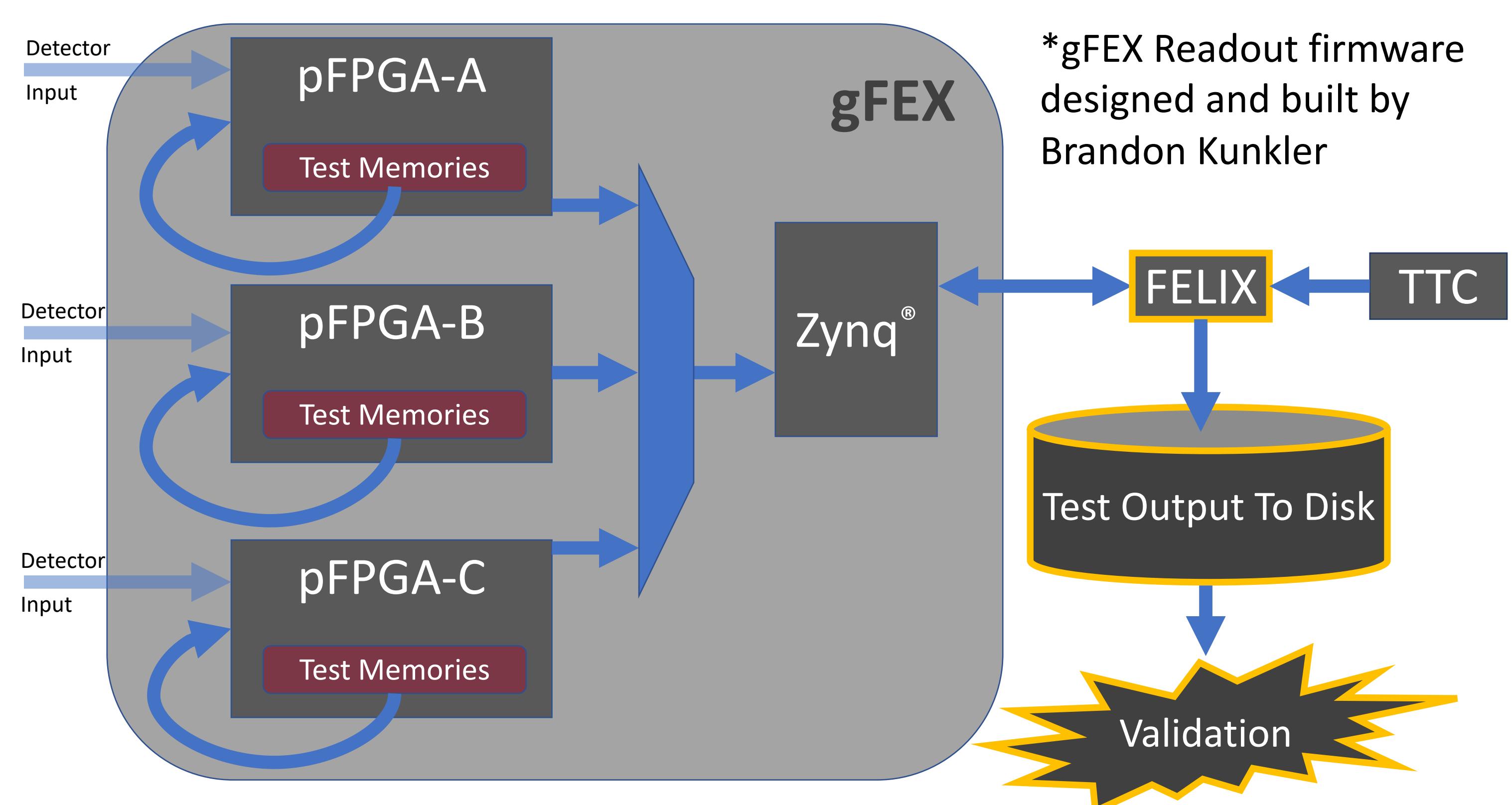
- Form gBlocks ($3 \times 3 E_T$ sums)
- Select gBlocks above a threshold
- Form jet by summing gTower E_T values in fixed radius around gBlock center
- Send out jet positions and E_T sums



A couple of things to note:

- Jets can overlap!
- Jets can cross pFPGA boundaries!

Readout Validation Flow



*gFEX Readout firmware designed and built by Brandon Kunkler

Data Structures

00	01	CD	AB	EE	34	12	EE	09	00	1A	6B	06	FF	FF	71	A5	5A	8E	8E	5A	
A5	71	F0	6A	AC	5D	31	01	00	00	58	55	55	85	A7	AA	AA	7A	06	99	ED	FE
0A	FC	75	09	E5	E5	E5	00	00	00	E6	E6	E6	E6	0A	FC	75	09	E7	E7		
E7	E7	00	00	00	00	02	00	00	D0	03	00	00	D0	03	00	00	00	07	00	00	
01	00	00	00	58	64	00	00	EE	34	12	EE	09	00	1A	6B	06	FF	FF	71	A5	

Binary data words, aligned on 32-bit boundaries:

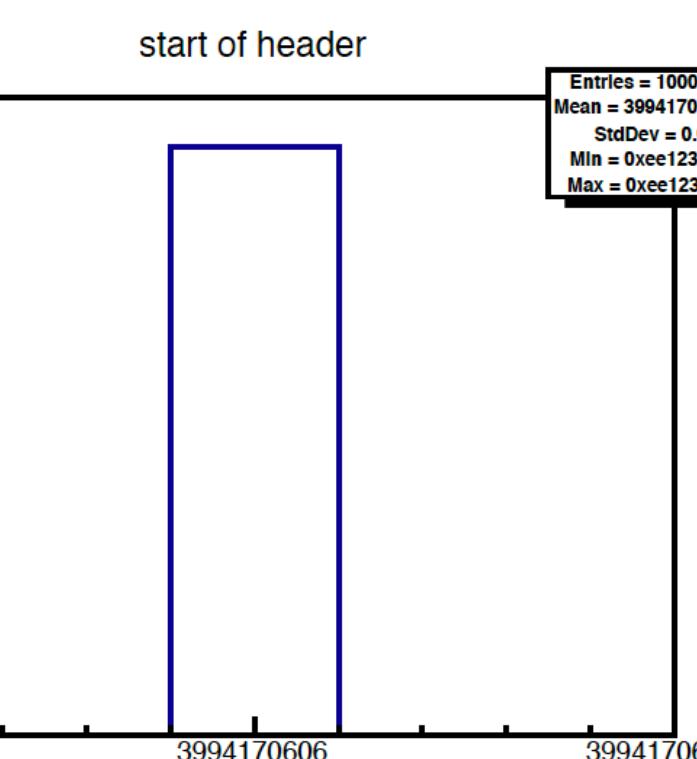
- Light Blue**: One gFEX event packet received by FELIX
 - 9 header words
 - 7 words in trigger object payload from pFPGA-A
 - 3 status words
 - 3 trailer words
- Green**: FELIX block header
- Red**: Start of ATLAS event header
- Orange**: Missing E_T x (high 16 bits) and y (low 16 bits) components
- Purple**: FELIX fragment trailer

Readout Validation

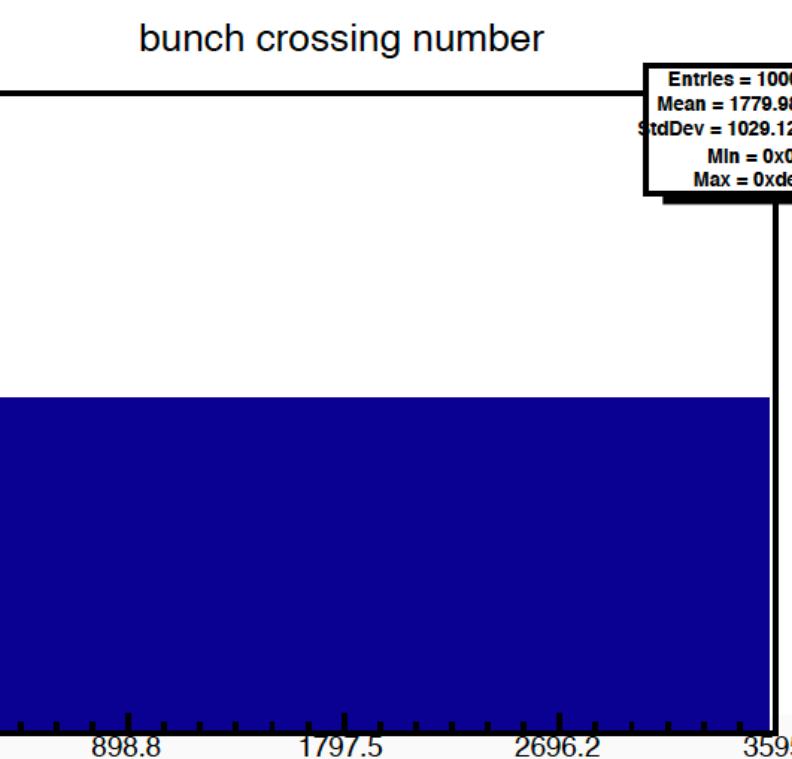
Verify Packet Contents:

- Check many packets ($\sim 10^7$)
- Do direct comparison on constant values
 - Header words
 - Bunch crossing ID
 - Packet size
 - And more!

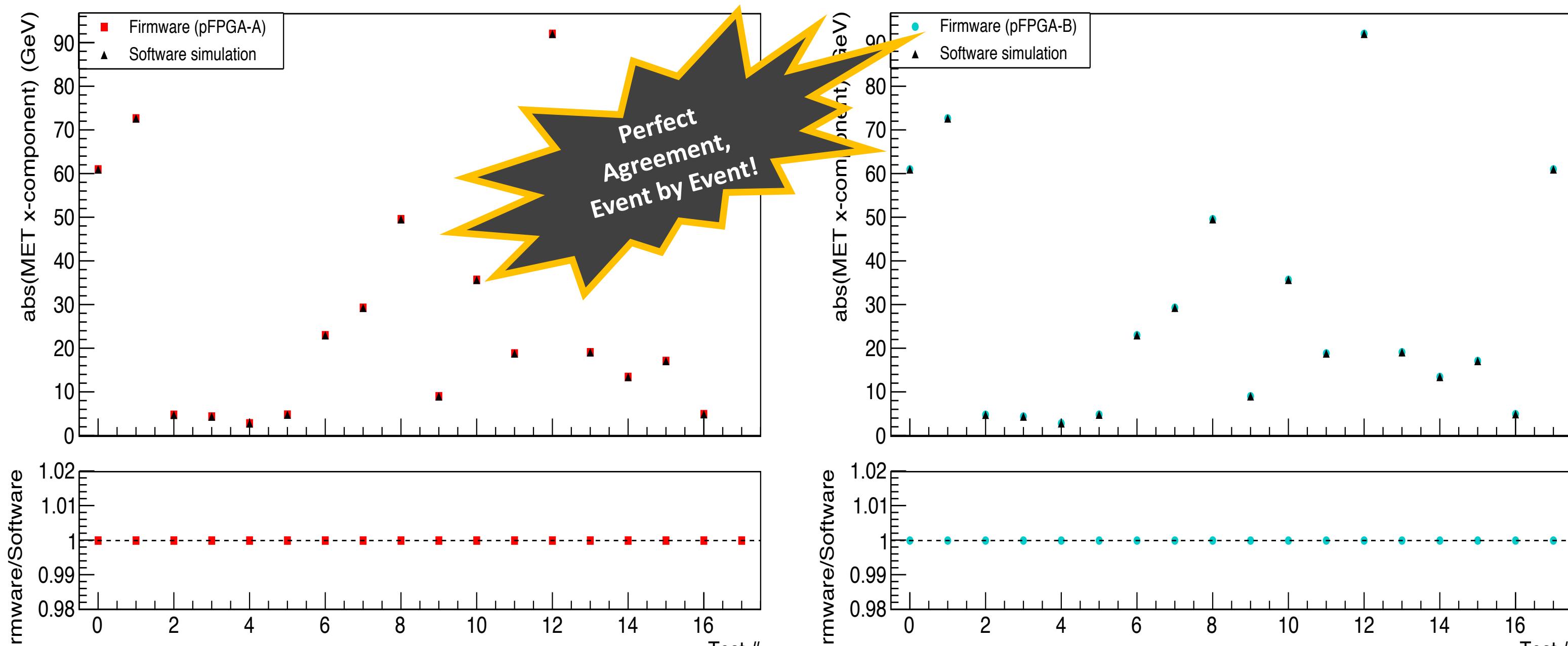
start of header



bunch crossing number



Verify Trigger Object Values in Data Payload:



Coming Milestones to Commissioning

- Test gFEX->FELIX->SWROD readout path
- Validate large-area jets algorithm
- Test data transfer with L1Topo
- Test data transfer with LATOME
- And much more!

Collaborating Institutes

- Indiana University
- Lund University
- University of Chicago
- Stockholm University
- University of Oregon
- University of Pittsburgh
- Brookhaven National Laboratory

For More Information on the gFEX!

gFEX Phase-I TDAQ Upgrade: Final Design Report (ATL-COM-DAQ-2016-184)