

		Instructions	
Instr. Kind	Instr. Name	Operators	Description
	add	Reg1, Reg2, Reg3	Reg1 := Reg2 + Reg3
	sub	Reg1, Reg2, Reg3	Reg1 := Reg2 - Reg3
ALU	sll	Reg1, Reg2, Reg3	Reg1 := Reg2 << Reg3
Instructions	srl	Reg1, Reg2, Reg3	Reg1 := Reg2 >> Reg3 logical
without			(fill space with 0)
Immediate	sra	Reg1, Reg2, Reg3	Reg1 := Reg2 >> Reg3 arith-
			metical (fill space with sign bit)
	xor	Reg1, Reg2, Reg3	Reg1 := Reg2 xor Reg3
	or	Reg1, Reg2, Reg3	Reg1 := Reg2 or Reg3
	and	Reg1, Reg2, Reg3	Reg1 := Reg2 and Reg3
	addi	Reg1, Reg2, Imm	Reg1 := Reg2 + Imm
	subi	Reg1, Reg2, Imm	Reg1 := Reg2 - Imm
ALU	slli	Reg1, Reg2, Imm	Reg1 := Reg2 << Imm
Instructions	srli	Reg1, Reg2, Imm	Reg1 := Reg2 >> Imm logical
with			(fill space with 0)
Immediate	srai	Reg1, Reg2, Imm	Reg1 := Reg2 >> Imm arith-
			metical (fill space with sign bit)
	xori	Reg1, Reg2, Imm	Reg1 := Reg2 xor Imm
	ori	Reg1, Reg2, Imm	Reg1 := Reg2 or Imm
	andi	Reg1, Reg2, Imm	Reg1 := Reg2 and Imm
	lw	Reg1, Reg2, Imm	addr:=Reg2(base)+Imm(offset),
Manaans			$Reg1:=(Mem_word[addr])$
Memory Instructions	ll lb	Reg1, Reg2, Imm	addr:=Reg2(base)+Imm(offset),
mstructions			$Reg1:=(Mem_byte[addr])$
	sw	Reg1, Reg2, Imm	addr:=Reg2(base)+Imm(offset),
			Mem_word[addr]:=Reg1
	sb	Reg1, Reg2, Imm	addr:=Reg2(base)+Imm(offset),
			Mem_byte[addr]:=Reg1
	flush	Reg, Imm	addr:=Reg(base)+Imm(offset),
			flush_cashline(adr)
	beq	Reg1, Reg2, Label	pc:=Label if Reg1==Reg2, else
			pc+=1
	bne	Reg1, Reg2, Label	pc:=Label if Reg1! =Reg2
Branch	bltu	Reg1, Reg2, Label	pc:=Label if u(Reg1) < u(Reg2)
Instructions	bleu	Reg1, Reg2, Label	pc:=Label if u(Reg1) <= u(Reg2)
	bgtu	Reg1, Reg2, Label	pc:=Label if u(Reg1)>u(Reg2)
	bgeu	Reg1, Reg2, Label	pc:=Label if u(Reg1)>=u(Reg2)
	blts	Reg1, Reg2, Label	pc:=Label if s(Reg1) < s(Reg2)
	bles	Reg1, Reg2, Label	pc:=Label if s(Reg1) <= s(Reg2)
	bgts	Reg1, Reg2, Label	pc:=Label if s(Reg1)>s(Reg2)
	bges	Reg1, Reg2, Label	pc:=Label if s(Reg1)>=s(Reg2)
Special	rdtsc	Reg	Reg:=cyclecount(number of exe-
Instructions			cuted execution unit ticks)
	fence	none	all instr in the EU unit at the
			point of issueing the fence are ex-
		2	ecuted before the fence ist exe-
			cuted; no new instructions are is-
			sued before the fence is executed