M200

Wearable Application Processor

Data Sheet

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Disclaimer

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1 Overview

M200 is a low power consumption, high performance and high integrated application processor, the application is focus on wearable devices, such as smart watch and smart glass. And it can match the requirements of many other embedded products.

1.1 Block Diagram

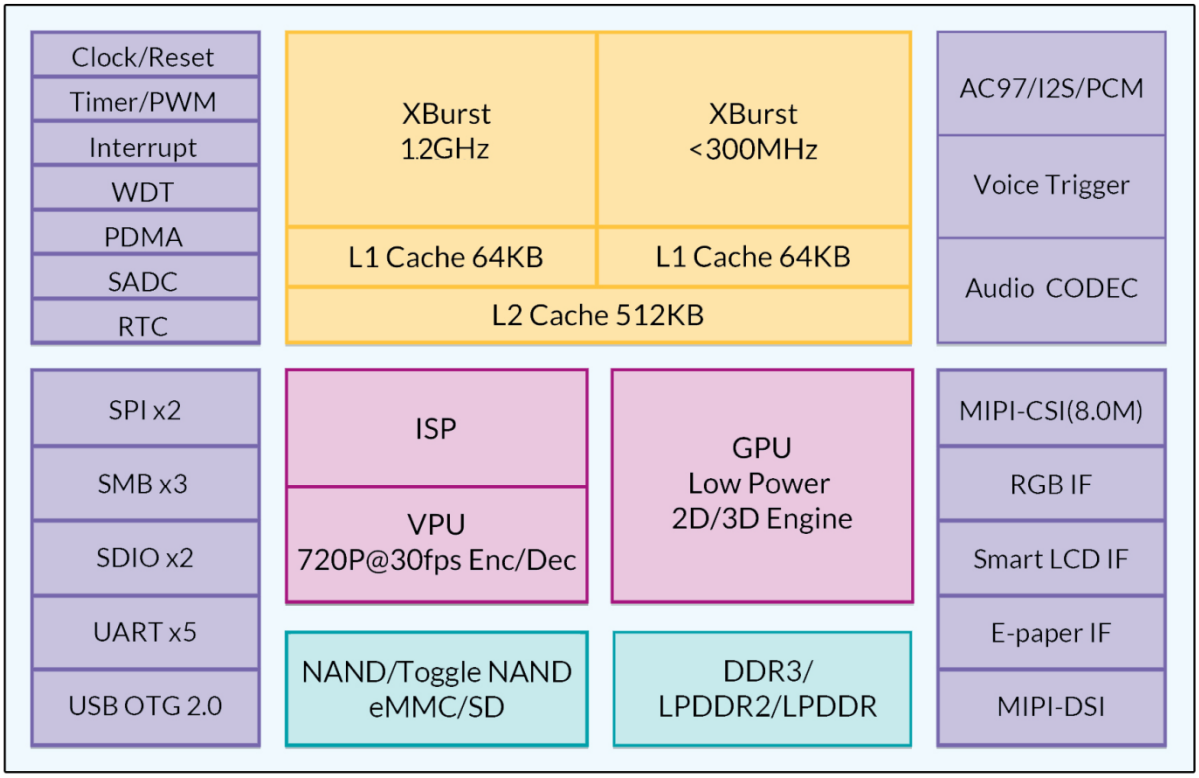


Figure 1-1 M200 Diagram

1.2 Features

1.2.1 CPU Core

- Two MIPS-Based XBurst® cores (One core up to 1.2GHz for high performance application, the other is 300MHz for low power application)
- MIPS-Based XBurst CPU
  - XBurst® RISC instruction set
  - XBurst® SIMD instruction set
  - XBurst® FPU instruction set supporting both single and double floating point format which are IEEE754 compatible
  - XBurst® 9-stage pipeline micro-architecture
- MMU

  - 32-entry joint-TLB
  - 4 entry Instruction TLB
  - 4 entry data TLB
- L1 Cache
  - 32KB instruction cache for each core
  - 32KB data cache for each core
- Hardware debug support
- 16KB tight coupled memory
- L2 Cache
  - 512KB unify cache

1.2.2 VPU Core

- Video encoder up to 720P@30fps
  —H.264, VP8
- Video decoder up to 720P@30fps
  —H.264, MPEG-4, MPEG-1/2, VC-1, RV9, VP8

1.2.3 GPU Core

- 3D Graphic
  - OpenGL ES 2.0 / 1.1 compliance, including extensions; OpenVG 1.1
  - Low CPU loading
  - Up to 12 programmable elements per vertex
  - Dependent texture operation with high-performance
  - Alpha blending
  - Depth and stencil compare
  - Support for 8 fragment shader simultaneous textures
  - Support for 4 vertex shader simultaneous textures
  - Point sampling, bi-linear sampling, tri-linear filtering, and cubic textures
  - Resolve and fast clear
  - 8k x 8k texture size and 8k x 8k rendering target
  - 4 Vertex DMA streams
  - Supports YUV formats in display output (YUY2 4:2:2)
  - MMU functionality supported
- 2D feature
  - Bit BLT and stretch BLT
  - Rectangle fill and clear
  - Line drawing
  - High-performance stretch and shrink
  - Monochrome expansion for text rendering
  - ROP2, ROP3, ROP4
  - Alpha blending including Java 2 Porter-Duff compositing blending rules
  - 32k x 32k coordinate system

- 90, 180, and 270 degrees rotation
- Transparency by monochrome mask, chroma key, or pattern mask
- Support 2x2 in 4x4 tile format
- A8/RG16 output with rotation in FilterBlit and BitBlit

- Multi Source Blending
  - Full support for Multi source blending with variable block size to improve BW and reduce SW overhead.
  - Up to 8 sources are supported.
  - Programmable block size guarantees cache efficiency so each source is read once and each destination is written once.
  - Supports 90, 180, 270 degree rotation with different block size for higher cache efficiency.
  - Supports independent source rotation with blending.

1.2.4 ISP Core

- ISP core for image pre-process.
  - Wide Dynamic Range Processing(EDR)
  - Dual-stream processing
  - Video and still image stabilization
  - Image cropping and rescaling
  - Auto exposure and gain control
  - Auto white balancing
  - Auto focus control
  - 50/60Hz flicker cancellation
  - Lens shading correction
  - Defect pixel correcting recorded and on the fly
  - Edge sharpening
  - Advanced noise reduction
  - Enhanced color interpolation(RGB Bayer demosaicing)
  - Color correction
  - Color management
  - Auto contrast enhancement
  - Gamma correction
  - Special digital effects
- Support MIPI-CSI2(v1.0) interface
  - 2-lanes
- Independent SMB interface(ISP_SDA, ISP_SCK)

1.2.5 Display/Camera/Audio

- LCD controller
  - Basic Features

        - Support panel(TFT, SLCD, MIPI-DSI)
        - Display size up to 800x480@60Hz(BPP24)
    - Colors Supports
        - Encoded pixel data of 16, 18 in TFT mode
        - Support up to 16,777,216 (16M) colors in TFT mode
    - Panel Supports
        - Support 16-bit parallel TFT panel
        - Support 18-bit parallel TFT panel
        - Support SLCD panel
    - OSD Supports
        - Supports one single color background
        - Supports two foregrounds, and every size can be set for each foreground
        - Supports one transparency for the whole graphic
        - Supports one transparency for each pixel in one graphic
        - Supports color key and mask color key
        - Supports porter-duff blending
    - MIPI-DSI(v1.1) Supports
        - 2-lanes
- EPD Controller
    - Supports multiple types of compatible EPD panels
    - Supports different size up to 480x480@60Hz
    - Supports 2/3/4 bits grayscale
    - Pixel base updating
    - Supports hand-writing mode
    - Supports SW LUT algorithm
    - Supports AUTO-DU, AUTO-GC4 mode
- Image post processor(IPU)
    - Input format
        - Separate frame: YUV /YCbCr (4:2:0, 4:2:2, 4:4:4, 4:1:1), RGB888
        - Packaged data: YUV422, RGB888, RGB565, RGB555, YUV444
        - Separate frame in block format: YUV/YCbCr 420
    - Output data format
        - RGB (565, 555, 888, AAA)
        - Packaged data YUV422
    - Color convention coefficient: configurable (CSC enable)
    - Minimum input image size (pixel): 4x4
    - Maximum input image size (pixel): 8096x8096
    - Maximum output image size (pixel)
        - Width: up to 4095 (without vertical resizing)
        - up to 1280 (with vertical resizing)
        - Height: up to 4095
    - Image resizing
        - Support bilinear

- Up scaling ratios up to 1:31 in fractional steps with 1/32 accuracy
- Down scaling ratios up to 31:1 in fractional steps with 1/32 accuracy

- Camera interface
  - MIPI-CSI2(v1.0) interface Supports (Depend on ISP feature)
    - 2-lanes
- AC97/I2S controller
  - AC-link (AC97) features
    - Up to 20 bit audio sample data sizes supported
    - DMA transfer mode supported
    - Stop serial clock supported
    - Programmable Interrupt function supported
    - Support mono PCM data to stereo PCM data expansion on audio play back
    - Support endian switch on 16-bits normal audio samples play back
    - Support variable sample rate in AC-link format
    - Multiple channel output and double rated supported for AC-link format
    - Power Down Mode and two Wake-Up modes Supported for AC-link format
  - I2S features
    - 8, 16, 18, 20 and 24 bit audio sample data sizes supported, 16 bits packed sample data is supported
    - Up to 8 channels sample data supported
    - DMA transfer mode supported
    - Stop serial clock supported
    - Programmable Interrupt function supported
    - Support share clock mode and split clock mode.
    - Support mono PCM data to stereo PCM data expansion on audio play back
    - Support endian switch on 16-bits normal audio samples play back
    - Internal programmable or external serial clock and optional system clock supported for I2S or MSB-Justified format
    - Internal I2S CODEC supported
    - Two FIFOs for transmit and receive respectively
- PCM interface
  - Support master mode and slave mode
  - Data starts with the frame PCMSYN or one PCMCLK later
  - Support three modes of operation for PCM
    - Short frame sync mode
    - Long frame sync mode
    - Multi-slot mode
  - Data is transferred and received with the MSB first
  - The PCM serial output data, PCMDOUT, is clocked out using the rising edge of the PCMSCLK
  - The PCM serial input data, PCMDIN, is clocked in on the falling edge of the PCMSCLK
  - 8/16 bit sample data sizes supported
  - DMA transfer mode supported

  - Two FIFOs for transmit and receive respectively with 16 samples capacity in every direction
- Internal CODEC
  - 24 bits ADC and DAC
  - Headphone load up to 16 Ohm
  - Sample frequency supported: 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k, and 96k
  - Stereo line input
  - DAC to HP path: Power consumption: 17.6mW, THD: -65dB @17.6mW /16Ohm
  - DAC to stereo line output path @10kOhm: SNR: 100dB A-Weighted, THD: -80dB @FS-1dB
  - Line input to ADC path: SNR: 90dB A-Weighted, THD: -80dB @FS-1dB
  - Separate power-down modes for ADC and DAC path with several shutdown modes
  - Reduction of audible glitches systems: Pop Reduction system, Soft Mute mode
  - Output short circuit protection
  - Embedded low noise Linear Regulator
  - 2 MIC in path or 2 line in path Maximum (Total 2 analog input)
  - Support Digital MIC
- Low power DMIC Controller
  - 16 bits data interface and 24bit precision internal controller.
  - SNR: 90dB, THD: -90dB @ FS -20dB
  - Linear high pass filter include. Attenuation: -2.9dB@100Hz, -22dB@27Hz. -36dB@10Hz
  - Low power voice trigger when waiting to start talking.
  - Mono and stereo digital MIC support.
  - Support voice data pre-fetch when trigger enable and the data interface disable, but do not increase the power dissipation.
  - Sample frequency supported: 8k, 16k.
  - Support low power mode, user for decrease DMIC sensor and DMIC Controller power dissipation.

1.2.6 Memory Interface

- DDR Controller
  - Support DDR2, DDR3, DDR3L, mobile DDR (LPDDR), LPDDR2, memory，up to 667Mbps
  - Support x16 and x32 external DDR bus width
  - Asynchornize to system bus and each port.
  - Support clock-stop mode
  - Support auto self-refresh mode
  - Support power-down mode and deep-power-down mode
  - Programmable DDR timing parameters
  - Programmable DDR row and column address width and order
- NAND flash interface

- Support on CS3~CS1#, sharing with static memory bank3~bank1
- Support both of conventional NAND flash memory and Toggle NAND flash memory
- Support most types of NAND flashes, 8/16-bit data access, 512B/2KB/4KB/8KB/16KB page size. For 512B page size, 3 and 4 address cycles are supported. For 2KB/4KB/8KB/16KB page size, 4 and 5 address cycles are supported
- Support read/erase/program NAND flash memory
- Support boot from NAND flash
- Support Toggle1.0/ONFI2.0 NAND

- BCH Controller
  - Support up to 64-bit ECC encoding and decoding for NAND
- The XBurst® processor system supports little endian only

1.2.7 System Functions

- Clock generation and power management
  - On-chip oscillator circuit
  - Two phase-locked loops (PLL) with programmable multiplier
  - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK, VPU_CLK frequency can be changed separately for software by setting registers
  - Functional-unit clock gating
  - Supply block power shut down
- Timer and counter unit with PWM output and/or input edge counter
  - Provide 4 channels, all can generate PWM, two of them have input signal transition edge counter
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- OS timer
  - One channel
  - 32-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Interrupt controller
  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled
  - Priority mechanism to indicate highest priority interrupt
  - All the registers are accessed by CPU and PDMA
  - Unmasked interrupts can wake up the chip in sleep mode
  - Another set of source, mask and pending registers to serve for PDMA
- Watchdog timer
  - Generates WDT reset

- A 16-bit Data register and a 16-bit counter
- Counter clock uses the input clock selected by software
  - PCLK, EXTAL and RTCCLK can be used as the clock for counter
  - The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software

- PDMA Controller
  - Support up to 32 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode
  - A simple Xburst®-1 CPU supports smart transfer mode controlled by programmable firmware
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit: 1 ~ 2^{24} - 1
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
  - A dedicated bus interface - BIF interconnects with on-chip BCH
  - A dedicated bus interface - NIF interconnects with on-chip NEMC or off-chip NEMC.
  - An extra INTC IRQ can be bound to one programmable DMA channel
- SAR A/D Controller
  - 3 Channels
  - Resolution: 12-bit
  - Integral nonlinearity: ±1 LSB
  - Differential nonlinearity: ±0.5 LSB
  - Resolution/speed: up to 2Msps
  - Max Frequency: 200k
  - Low power dissipation: 1.5mW(worst)
  - Support write control command by software
  - Support voltage measurement (Through pin VBAT)
  - Support two auxiliary input (Through pin AUX1, AUX2)
- RTC (Real Time Clock)
  - Need external 32768Hz oscillator for 32KHz clock generation.
  - RTCLK selectable from the oscillator or from the divided clock of EXCLK, so that 32k crystal can be absent if the hibernating mode is not needed
  - 32-bits second counter
  - Programmable and adjustable counter to generate accurate 1 Hz clock
  - Alarm interrupt, 1Hz interrupt
  - Stand alone power supply, work in hibernating mode
  - Power down controller
  - Alarm wakeup
  - External pin wakeup with up to 2s glitch filter

1.2.8 Peripherals

- General-Purpose I/O ports
  - Each port can be configured as an input, an output or an alternate function port

- Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering. Every interrupt source can be masked independently
- Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled
- GPIO output 7 interrupts, 1 for every group, to INTC

- Four SMB Controller (SMB0, SMB1, SMB2, SMB3)
  - Two-wire SMB serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
  - Two speeds
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
  - Device clock is identical with pclk
  - Programmable SCL generator
  - Master or slave SMB operation
  - 7-bit addressing/10-bit addressing
  - -level transmit and receive FIFOs
  - Interrupt operation
  - The number of devices that you can connect to the same SMB-bus is limited only by the maximum bus capacitance of 400pF
  - APB interface
- Two Synchronous serial interfaces (SSI0,SSI1)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - Support 1，2，4 bit data width
  - Full-duplex or transmit-only or receive-only operation
  - Programmable transfer order: MSB first or LSB first
  - 128 entries deep x 32 bits wide transmit and receive data FIFOs
  - Configurable normal transfer mode or Interval transfer mode
  - Programmable clock phase and polarity for Motorola's SSI format
  - Two slave select signal (SSI_CE0_ / SSI_CE1_) supporting up to 2 slave devices
  - Back-to-back character transmission/reception mode
  - Loop back mode for testing
- Five UARTs (UART0, UART1, UART2, UART3, UART4)
  - Full-duplex operation
  - 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
  - 64x8 bit transmit FIFO and 64x11bit receive FIFO
  - Independently controlled transmit, receive (data ready or timeout), line status interrupts
  - Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
  - Separate DMA requests for transmit and receive data services in FIFO mode
  - Supports modem flow control by software or hardware
  - Slow infrared asynchronous interface that conforms to IrDA specification
- Two MMC/SD/SDIO controllers (MSC0, MSC1)

- Fully compatible with the MMC System Specification version 4.2
- Support SD Specification 3.0
- Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
- Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
- Maximum data rate is 50MBps
- Support MMC data width 1bit ,4bit and 8bit
- Built-in programmable frequency divider for MMC/SD bus
- Built-in Special Descriptor DMA
- Mask-able hardware interrupt for SDIO interrupt, internal status and FIFO status
- 128 x 32 built-in data FIFO
- Multi-SD function support including multiple I/O and combined I/O and memory
- IRQ supported enable card to interrupt MMC/SD controller
- Single or multi block access to the card including erase operation
- Stream access to the MMC card
- Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
- Supports CE-ATA digital protocol commands
- Support Command Completion Signal and interrupt to CPU
- Command Completion Signal disable feature
- The maximum block length is 4096bytes

- USB 2.0 OTG interface
  - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
  - Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - UTMI+ Level 3 Transceiver Interface
  - Soft connect/disconnect
  - 8 endpoints in device mode, 16 channels for host mode.
  - Dedicate FIFO
  - Supports control, interrupt, ISO and bulk transfer

- OTP Slave Interface
  - Total 4KB.

1.2.9 Bootrom

32KB Boot ROM memory

2 Packaging and Pinout Information

2.1 Overview

M200 processor is offered in 270-pin BGA package, which is 7.7mm x 8.9mm x 0.76mm outline, 22 x 19 matrix ball grid array and 0.4mm ball pitch, show in Figure 2-1. The M200 pin to ball assignment is show in Figure 2-2.

The detailed pin description is listed in Table 2-1~Table 2-21.

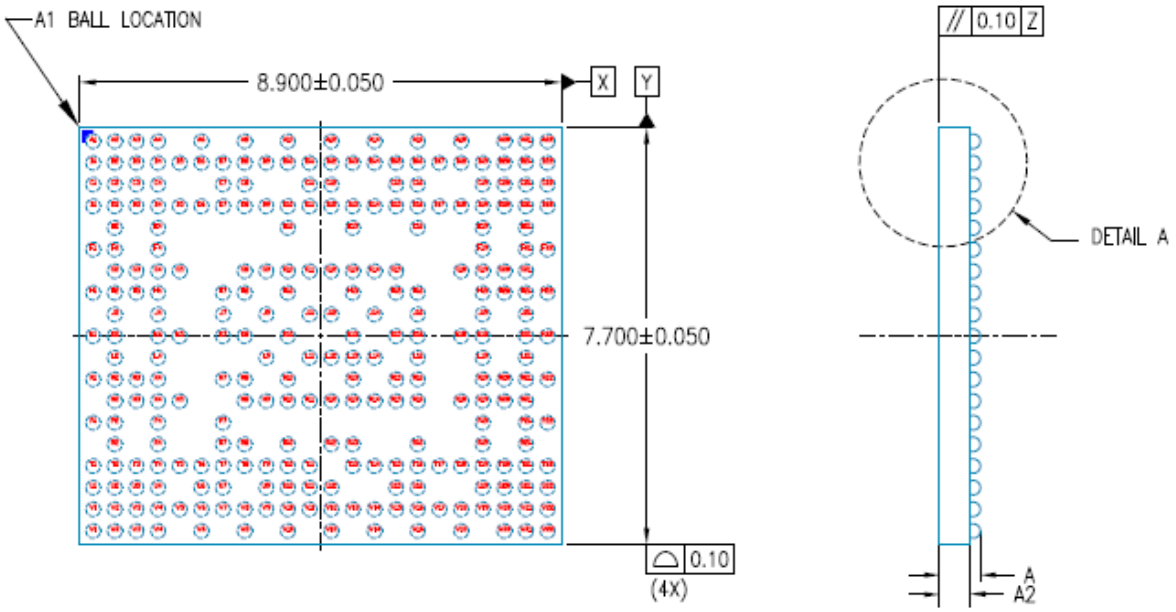
2.2 Solder Process

M200 package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.

2.3 Moisture Sensitivity Level

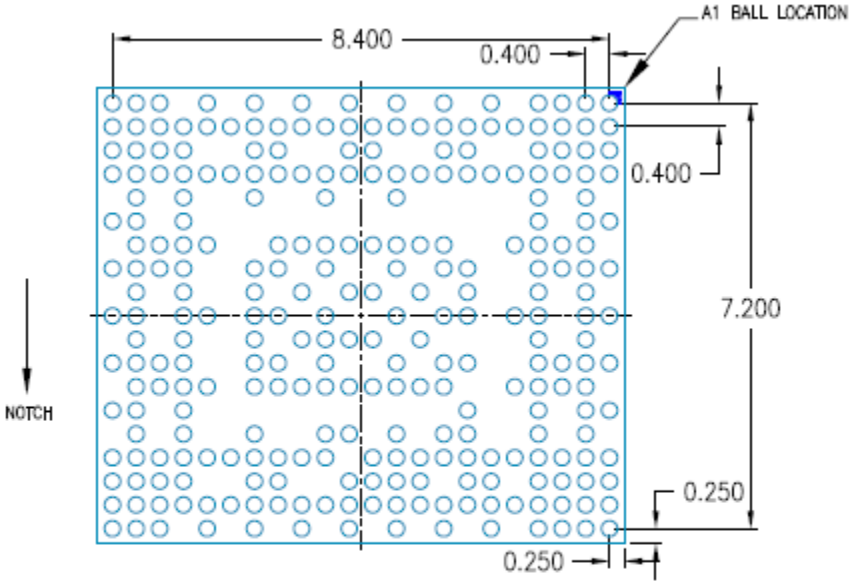
M200 package moisture sensitivity is level 3.

2.4 M200 Package

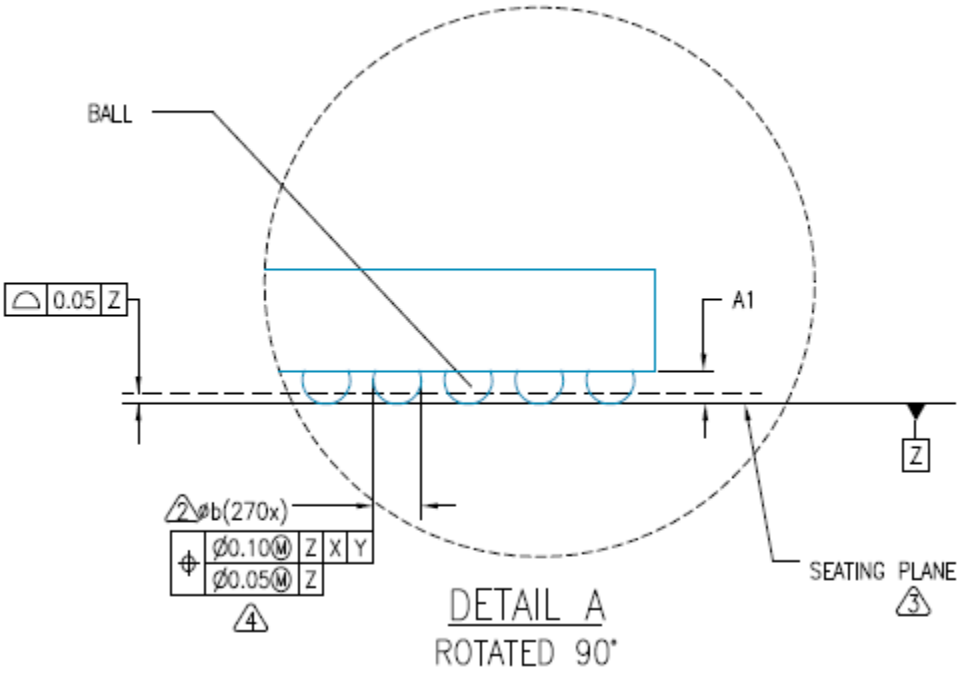


WAFER BACK SIDE

SIDE VIEW



BUMP SIDE



WITH BACK SIDE OVERMOLD			
DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	0.720	0.755	0.790
A1	0.175	0.190	0.205
A2	0.545	0.565	0.585
b	0.240	0.270	0.300
NUMBER OF BUMPS: 270			

Figure 2-1 M200 package outline drawing

Notes:

1. Dimensions and tolerance per asme Y 14.5M - 1994.

2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.

4. Bump position designation per JESD 95-1, SPP-010.

5. There shall be a minimum clearance of 0.10mm between the edge of the bump and the body edge.

Figure 2-2 M200 pin to ball assignment

2.5 Pin Descriptions

2.5.1 DRAM

Table 2-1 Port 0 DDR(mDDR, DDR2, DDR3) Pins (76)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DQ0_0	IO	D18	Bi-dir, Single-end	DQ0_0: DDR data bus bit 0	VDDQ
DQ0_1	IO	C19	Bi-dir, Single-end	DQ0_1: DDR data bus bit 1	VDDQ
DQ0_2	IO	C20	Bi-dir, Single-end	DQ0_2: DDR data bus bit 2	VDDQ
DQ0_3	IO	B20	Bi-dir, Single-end	DQ0_3: DDR data bus bit 3	VDDQ
DQ0_4	IO	A22	Bi-dir, Single-end	DQ0_4: DDR data bus bit 4	VDDQ
DQ0_5	IO	B19	Bi-dir, Single-end	DQ0_5: DDR data bus bit 5	VDDQ
DQ0_6	IO	A20	Bi-dir, Single-end	DQ0_6: DDR data bus bit 6	VDDQ
DQ0_7	IO	A21	Bi-dir, Single-end	DQ0_7: DDR data bus bit 7	VDDQ
DQ1_0	IO	B18	Bi-dir, Single-end	DQ1_0: DDR data bus bit 8	VDDQ
DQ1_1	IO	C16	Bi-dir, Single-end	DQ1_1: DDR data bus bit 9	VDDQ
DQ1_2	IO	C15	Bi-dir, Single-end	DQ1_2: DDR data bus bit 10	VDDQ
DQ1_3	IO	A18	Bi-dir, Single-end	DQ1_3: DDR data bus bit 11	VDDQ
DQ1_4	IO	D14	Bi-dir, Single-end	DQ1_4: DDR data bus bit 12	VDDQ
DQ1_5	IO	B16	Bi-dir, Single-end	DQ1_5: DDR data bus bit 13	VDDQ
DQ1_6	IO	B17	Bi-dir, Single-end	DQ1_6: DDR data bus bit 14	VDDQ
DQ1_7	IO	A16	Bi-dir, Single-end	DQ1_7: DDR data bus bit 15	VDDQ
DQ2_0	IO	A12	Bi-dir, Single-end	DQ2_0: DDR data bus bit 16	VDDQ
DQ2_1	IO	B13	Bi-dir, Single-end	DQ2_1: DDR data bus bit 17	VDDQ
DQ2_2	IO	B11	Bi-dir, Single-end	DQ2_2: DDR data bus bit 18	VDDQ
DQ2_3	IO	B12	Bi-dir, Single-end	DQ2_3: DDR data bus bit 19	VDDQ
DQ2_4	IO	C11	Bi-dir, Single-end	DQ2_4: DDR data bus bit 20	VDDQ
DQ2_5	IO	B10	Bi-dir, Single-end	DQ2_5: DDR data bus bit 21	VDDQ
DQ2_6	IO	A10	Bi-dir, Single-end	DQ2_6: DDR data bus bit 22	VDDQ
DQ2_7	IO	D11	Bi-dir, Single-end	DQ2_7: DDR data bus bit 23	VDDQ
DQ3_0	IO	A8	Bi-dir, Single-end	DQ3_0: DDR data bus bit 24	VDDQ
DQ3_1	IO	B7	Bi-dir, Single-end	DQ3_1: DDR data bus bit 25	VDDQ
DQ3_2	IO	B8	Bi-dir, Single-end	DQ3_2: DDR data bus bit 26	VDDQ
DQ3_3	IO	C8	Bi-dir, Single-end	DQ3_3: DDR data bus bit 27	VDDQ
DQ3_4	IO	A6	Bi-dir, Single-end	DQ3_4: DDR data bus bit 28	VDDQ
DQ3_5	IO	B6	Bi-dir, Single-end	DQ3_5: DDR data bus bit 29	VDDQ
DQ3_6	IO	B5	Bi-dir, Single-end	DQ3_6: DDR data bus bit 30	VDDQ
DQ3_7	IO	C7	Bi-dir, Single-end	DQ3_7: DDR data bus bit 31	VDDQ
A0	O	D6	Output, Single-end	A0: DDR address bus bit 0	VDDQ
A1	O	D1	Output, Single-end	A1: DDR address bus bit 1	VDDQ
A2	O	F2	Output, Single-end	A2: DDR address bus bit 2	VDDQ
A3	O	F4	Output, Single-end	A3: DDR address bus bit 3	VDDQ
A4	O	D5	Output, Single-end	A4: DDR address bus bit 4	VDDQ
A5	O	D3	Output, Single-end	A5: DDR address bus bit 5	VDDQ
A6	O	D4	Output, Single-end	A6: DDR address bus bit 6	VDDQ
A7	O	B2	Output, Single-end	A7: DDR address bus bit 7	VDDQ
A8	O	E4	Output, Single-end	A8: DDR address bus bit 8	VDDQ
A9	O	A2	Output, Single-end	A9: DDR address bus bit 9	VDDQ

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
A10	O	H1	Output, Single-end	A10: DDR address bus bit 10	VDDQ
A11	O	E2	Output, Single-end	A11: DDR address bus bit 11	VDDQ
A12	O	C1	Output, Single-end	A12: DDR address bus bit 12	VDDQ
A13	O	C2	Output, Single-end	A13: DDR address bus bit 13	VDDQ
A14	O	D2	Output, Single-end	A14: DDR address bus bit 14	VDDQ
CS0_N	O	B4	Output, Single-end	CS0_N: DDR chip select 0	VDDQ
CS1_N	O	B3	Output, Single-end	CS1_N: DDR chip select 1	VDDQ
RAS_N	O	G3	Output, Single-end	RAS_N: DDR row address strobe	VDDQ
CAS_N	O	A3	Output, Single-end	CAS_N: DDR column address strobe	VDDQ
WE_N	O	G2	Output, Single-end	WE_N: DDR write enable	VDDQ
DQS0	IO	D17	Bi-dir, Differential	DQS0: DDR data byte 0 strobe positive	VDDQ
DQS0_N	IO	D16	Bi-dir, Differential	DQS0_N: DDR data byte 0 strobe negative for differential. Use this pin for differential DQS signal.	VDDQ
DQS1	IO	B14	Bi-dir, Differential	DQS1: DDR data byte 1 strobe positive	VDDQ
DQS1_N	IO	B15	Bi-dir, Differential	DQS1_N: DDR data byte 1 strobe negative for differential.	VDDQ
DQS2	IO	C12	Bi-dir, Differential	DQS2: DDR data byte 2 strobe positive	VDDQ
DQS2_N	IO	D12	Bi-dir, Differential	DQS2_N: DDR data byte 2 strobe negative for differential.	VDDQ
DQS3	IO	D9	Bi-dir, Differential	DQS3: DDR data byte 3 strobe positive	VDDQ
DQS3_N	IO	D10	Bi-dir, Differential	DQS3_N: DDR data byte 3 strobe negative for differential.	VDDQ
DM0	O	E16	Output, Single-end	DM0: DDR data byte 0 mask	VDDQ
DM1	O	D15	Output, Single-end	DM1: DDR data byte 1 mask	VDDQ
DM2	O	A14	Output, Single-end	DM2: DDR data byte 2 mask	VDDQ
DM3	O	B9	Output, Single-end	DM3: DDR data byte 3 mask	VDDQ
BA0	O	D7	Output, Single-end	BA0: DDR address bus bank 0	VDDQ
BA1	O	C3	Output, Single-end	BA1: DDR address bus bank 1	VDDQ
BA2	O	F1	Output, Single-end	BA2: DDR address bus bank 2	VDDQ
CK	O	A1	Output, Differential	CK: DDR clock	VDDQ
CKN	O	B1	Output, Differential	CKN: DDR inverse clock	VDDQ
CKE	O	A4	Output, Single-end	CKE: DDR clock enable	VDDQ_A
ODT0	O	G4	Output, Single-end	ODT0: DDR rank 0 On-die termination	VDDQ
RST_N	O	C4	Output, Single-end	RST_N: DDR3 reset pin	VDDQ
VREF_A	AI	D8		VREF_A: DDR/DDR2/DDR3 input reference voltage	
VREF1	AI	E10		VREF1: DDR/DDR2/DDR3 input reference voltage	
VREF	AI	E13		VREF: DDR/DDR2/DDR3 input reference voltage	
ZQ	AIO	D13		ZQ: DDR3 External reference which is connected to a 240ohm resister	

2.5.2 BOOT and storage

Table 2-2 Static-Memory/MSC0/SPI0 Pins (25)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SD0 PA00	IO IO	G20	8mA, pullup-pe	SD0: Static memory data bus bit 0 PA0: GPIO group A bit 0	VDDIO_N
SD1 PA01	IO IO	G21	8mA, pullup-pe	SD1: Static memory data bus bit 1 PA1: GPIO group A bit 1	VDDIO_N

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SD2 PA02	IO IO	F21	8mA, pullup-pe	SD2: Static memory data bus bit 2 PA2: GPIO group A bit 2	VDDIO_N
SD3 PA03	IO IO	F19	8mA, pullup-pe	SD3: Static memory data bus bit 3 PA3: GPIO group A bit 3	VDDIO_N
SD4 **MSC0_D4** PA04	IO IO IO	E19	8mA, pullup-pe	SD4: Static memory data bus bit 4 MSC0_D4: MSC (MMC/SD) 0 data bit 4 PA4: GPIO group A bit 4	VDDIO_N
SD5 **MSC0_D5** PA05	IO IO IO	E21	8mA, pullup-pe	SD5: Static memory data bus bit 5 MSC0_D5: MSC (MMC/SD) 0 data bit 5 PA5: GPIO group A bit 5	VDDIO_N
SD6 **MSC0_D6** PA06	IO IO IO	D22	8mA, pullup-pe	SD6: Static memory data bus bit 6 MSC0_D6: MSC (MMC/SD) 0 data bit 6 PA6: GPIO group A bit 6	VDDIO_N
SD7 **MSC0_D7** PA07	IO IO IO	D21	8mA, pullup-pe	SD7: Static memory data bus bit 7 MSC0_D7: MSC (MMC/SD) 0 data bit 7 PA7: GPIO group A bit 7	VDDIO_N
SD8 **PA08**	**IO** **IO**	H22	8mA, pullup-pe	**SD08: Static memory data bus bit 8** **PA08: GPIO group A bit 8**	VDDIO_N
SD9 **PA09**	**IO** **IO**	H20	8mA, pullup-pe	**SD09: Static memory data bus bit 9** **PA09: GPIO group A bit 9**	VDDIO_N
SD10 **PA10**	**IO** **IO**	H21	8mA, pullup-pe	**SD10: Static memory data bus bit 10** **PA10: GPIO group A bit 10**	VDDIO_N
SD11 **PA11**	**IO** **IO**	J21	8mA, pullup-pe	**SD11: Static memory data bus bit 11** **PA11: GPIO group A bit 11**	VDDIO_N
SD12 **PA12**	**IO** **IO**	H19	8mA, pullup-pe	**SD12: Static memory data bus bit 12** **PA12: GPIO group A bit 12**	VDDIO_N
SD13 **PA13**	**IO** **IO**	K22	8mA, pullup-pe	**SD13: Static memory data bus bit 13** **PA13: GPIO group A bit 13**	VDDIO_N
SD14 **PA14**	**IO** **IO**	J19	8mA, pullup-pe	**SD14: Static memory data bus bit 14** **PA14: GPIO group A bit 14**	VDDIO_N
SD15 **PA15**	**IO** **IO**	K21	8mA, pullup-pe	**SD15: Static memory data bus bit 15** **PA15: GPIO group A bit 15**	VDDIO_N
SA0 (CL) PB00	O IO	G18	8mA, pulldown-pe, rst-pe	SA1: Static memory address bus bit 0 If NAND flash is used, this pin is used as NAND CL (command latch) pin PB0: GPIO group B bit 0	VDDIO_N
SA1 (AL) PB01	O IO	G19	8mA, pulldown-pe, rst-pe	SA1: Static memory address bus bit 1 If NAND flash is used, this pin is used as NAND AL (address latch) pin PB1: GPIO group B bit 1	VDDIO_N
FRE_ **MSC0_CLK** **SSI0_CLK** PA18	O O **IO** IO	D20	8mA, pullup-pe, rst-pe	FRE_: NAND read enable MSC0_CLK: MSC (MMC/SD) 0 clock output **SSI0_CLK: SSI 0 clock output** PA18: GPIO group A bit 18	VDDIO_N
FWE_ **MSC0_CMD** **SSI0_DT** PA19	O IO **IO** IO	D19	8mA, pullup-pe, rst-pe	FEW_: NAND write enable MSC0_CMD: MSC (MMC/SD) 0 command **SSI0_DT: SSI 0 data output** PA19: GPIO group A bit 19	VDDIO_N
FRB0 **MSC0_D0** **SSI0_DR** PA20	**I** IO **IO** IO	C22	8mA, Schmitt, Input filter pullup-pe	**FRB0: NAND flash FRB input 0 candidate** MSC0_D0: MSC (MMC/SD) 0 data bit 0 **SSI0_DR: SSI 0 data input** PA20: GPIO group A bit 20.	VDDIO_N
CS1_ **MSC0_D1** **SSI0_GPC** PA21	O IO **IO** IO	C21	8mA, pullup-pe, rst-pe	CS1_: NAND/NOR/SRAM chip select 1 MSC0_D1: MSC (MMC/SD) 0 data bit 1 **SSI0_GPC: SSI 0 general-purpose control signal** PA21: GPIO group A bit 21	VDDIO_N
CS2_ **MSC0_D2** **SSI0_CE1_** PA22	O IO **IO** IO	B22	8mA, pullup-pe, rst-pe	CS2_: NAND/NOR/SRAM chip select 2 MSC0_D2: MSC (MMC/SD) 0 data bit 2 **SSI0_CE1_: SSI 0 chip enable 1** PA22: GPIO group A bit 22	VDDIO_N

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CS3_ FRB1 MSC0_D3 SSI0_CE0_ PA23	O I IO IO IO	B21	rst-pe	CS3_: NAND/NOR/SRAM chip select 3 FRB1: NAND flash FRB input 1 candidate MSC0_D3: MSC (MMC/SD) 0 data bit 3 SSI0_CE0_: SSI 0 chip enable 0 PA23: GPIO group A bit 23.	VDDIO_N
NDQS PA29	IO IO	F22	8mA pullup-pe	NDQS: Toggle nand DQS pin. PA29: GPIO group A bit 29.	VDDIO_N

2.5.3 LCD/SLCD/EPD/SMB3/CIM

Table 2-3 LCDC Pins (22; all GPIO shared: PC0~27)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_B2 CIM0_D8 SLCD_D0 EPD_D0 PC02	O IO O O IO	M4	8mA, pullup-pe	LCD_B2: LCD Blue data bit 2 CIM0_D8: CIM data input bit 8. (output for test) SLCD_D0:SLCD data 0 EPD_D0:EPD data 0 PC02: GPIO group C bit 2	VDDIO
LCD_B3 CIM0_D9 SLCD_D1 EPD_D1 PC03	O IO O O IO	N3	8mA, pullup-pe	LCD_B3: LCD Blue data bit 3 CIM0_D9: CIM data input bit 9. (output for test) SLCD_D1:SLCD data 1 EPD_D1:EPD data1 PC03: GPIO group C bit 3	VDDIO
LCD_B4 SLCD_D2 EPD_D2 PC04	O O O IO	K5	8mA, pullup-pe	LCD_B4: LCD Blue data bit 4 SLCD_D2:SLCD data 2 EPD_D2:EPD data 2 PC04: GPIO group C bit 4	VDDIO
LCD_B5 SLCD_D3 EPD_D3 PC05	O O O IO	R2	8mA, pullup-pe	LCD_B5: LCD Blue data bit 5 SLCD_D3:SLCD data 3 EPD_D3:EPD data 3 PC05: GPIO group C bit 5	VDDIO
LCD_B6 SLCD_D4 EPD_D4 PC06	O O O IO	T1	8mA, pullup-pe	LCD_B6: LCD Blue data bit 6 SLCD_D4:SLCD data 4 EPD_D4:EPD data 4 PC06: GPIO group C bit 6	VDDIO
LCD_B7 SLCD_D5 EPD_D5 PC07	O O O IO	L4	8mA, pullup-pe	LCD_B7: LCD Blue data bit 7 SLCD_D5:SLCD data 5 EPD_D5:EPD data 5 PC07: GPIO group C bit 7	VDDIO
LCD_PCLK SLCD_D6 EPD_D6 PC08	O O O IO	N2	16mA, pullup-pe	LCD_PCLK: LCD pixel clock SLCD_D6:SLCD data 6 EPD_D6:EPD data 6 PC8: GPIO group C bit 8	VDDIO
LCD_DE SLCD_D7 EPD_D7 PC09	O O O IO	P2	8mA, pullup-pe	LCD_DE: STN AC bias drive/non-STN data enable SLCD_D7:SLCD data 7 EPD_D7:EPD data 7 PC09: GPIO group C bit 9	VDDIO
LCD_G2 CIM0_D0 SLCD_D8 EPD_GDCLK PC12	O IO O O IO	P1	8mA, pullup-pe	LCD_G2: LCD Green data bit 2 CIM_D0: CIM data input bit 0. (output for test) SLCD_D8:SLCD data 8 EPD_GDCLK:EPD YCLK PC12: GPIO group C bit 12	VDDIO
LCD_G3 CIM0_D1 SLCD_D9 EPD_GDSP PC13	O IO O O IO	J4	8mA, pullup-pe	LCD_G3: LCD Green data bit 3 CIM_D1: CIM data input bit 1. (output for test) SLCD_D9:SLCD data 9 EPD_GDSP:EPD YDIUO PC13: GPIO group C bit 13	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_G4 CIM0_D2 SLCD_D10 EPD_GDOE PC14	O IO O O IO	M2	8mA, Schmitt, Input filter pullup-pe	LCD_G4: LCD Green data bit 4 CIM_D2: CIM data input bit 2. (output for test) SLCD_D10:SLCD data10 EPD_GDOE:EPD YOE PC14: GPIO group C bit 14	VDDIO
LCD_G5 CIM0_D3 SLCD_D11 EPD_SDCLK PC15	O IO O O IO	M1	8mA, Schmitt, Input filter pullup-pe	LCD_G5: LCD Green data bit 5 CIM_D3: CIM data input bit 3. (output for test) SLCD_D11:SLCD data 11 EPD_SDCLK: EPDC XCLK PC15: GPIO group C bit 15	VDDIO
LCD_G6 CIM0_D4 SLCD_D12 EPD_SDOE PC16	O IO O O IO	L2	8mA, Schmitt, Input filter pullup-pe	LCD_G6: LCD Green data bit 6 CIM_D4: CIM data input bit 4. (output for test) SLCD_D12:SLCD data 12 EPD_SDOE:EPD source driver output enable PC16: GPIO group C bit 16	VDDIO
LCD_G7 CIM0_D5 SLCD_D13 EPD_SDLE PC17	O IO O O IO	K2	8mA, Schmitt, Input filter pullup-pe	LCD_G7: LCD Green data bit 7 CIM_D5: CIM data input bit 5. (output for test) SLCD_D13: SLCD data 13 EPD_SDLE:EPD source driver latch signal PC17: GPIO group C bit 17	VDDIO
LCD_HSYN CIM0_D6 SLCD_D14 EPD_SDCE0 PC18	IO IO O O IO	M3	8mA, Schmitt, Input filter pullup-pe	LCD_HSYN: LCD line clock/horizonal sync CIM_D6: CIM data input bit 6. (output for test) SLCD_D14:SLCD data 14 EPD_SDCE0:EPD XDIOL PC18: GPIO group C bit 18	VDDIO
LCD_VSYN CIM0_D7 SLCD_D15 EPD_SDCE1 PC19	IO IO O O IO	K4	8mA, Schmitt, Input filter pullup-pe	LCD_VSYN: LCD frame clock/vertical sync CIM_D7: CIM data input bit 7. (output for test) SLCD_D15:SLCD data 15 EPD_SDCE1:EPD XDIOR PC19: GPIO group C bit 19	VDDIO
LCD_R2 SMB3_SCK ISP_RST EPD_PWR0 PC22	O IO O O IO	G5	8mA, pullup-pe	LCD_R2: LCD Red data bit 2 SMB3_SCK: SMB 3 serial clock ISP_RST: ISP reset signal for sensor EPD_PWR0:EPD power 0 PC22: GPIO group C bit 22	VDDIO
LCD_R3 SMB3_SDA ISP_PWD EPD_PWR1 PC23	O IO O O IO	J2	8mA, pullup-pe	LCD_R3: LCD Red data bit 3 SMB3_SDA: SMB 3 serial data ISP_PWD: ISP power down signal for sensor EPD_PWR1: EPD power 1 PC23: GPIO group C bit 23	VDDIO
LCD_R4 CIM0_MCLK ISP_CLK EPD_PWR2 PC24	O O O O IO	H4	8mA, pullup-pe	LCD_R4: LCD Red data bit 4 CIM_MCLK: CIM master clock output ISP_CLK: ISP clock output for sensor EPD_PWR2: EPD power 2 PC24: GPIO group C bit 24	VDDIO
LCD_R5 CIM0_VSYN SLCD_WR EPD_PWR3 PC25	O IO O O IO	H2	8mA, pullup-pe	LCD_R5: LCD Red data bit 5 CIM_VSYN: CIM vertical sync input (output is just use for test) SLCD_WR:SLCD write signal EPD_PWR3: EPD power 3 PC25: GPIO group C bit 25	VDDIO
LCD_R6 CIM0_HSYN SLCD_DC EPD_BD0 PC26	O IO O O IO	H3	8mA, pullup-pe	LCD_R6: LCD Red data bit 6 CIM_HSYN: CIM horizontal sync input (output is just use for test) SLCD_DC:SLCD data/command signal EPD_BD0:EPD border0 PC26: GPIO group C bit 26	VDDIO
LCD_R7 CIM0_PCLK SLCD_TE EPD_BD1 PC27	O IO I O IO	K1	8mA, pullup-pe	LCD_R7: LCD Red data bit 7 CIM_PCLK: CIM pixel clock input (output is just use for test) SLCD_TE:SLCD tearing effect signal EPD_BD1: EPD border1 PC27: GPIO group C bit 27	VDDIO

2.5.4 PCM0/I2S/DMIC/UART2 (with input filter)

Table 2-4 PCM0/I2S/DMIC/UART2 Pins (6; all GPIO shared: PF6, 7,10~15)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DMIC0_CLK UART2_TxD PF06	O O IO	U15	8mA, pulldown-pe	DMIC0_CLK: Digital MIC0 clock output UART2_TxD: UART 2 transmitting data PF06: GPIO group F bit 6.	VDDIO
DMIC0_IN UART2_RxD PF07	I I IO	V16	8mA, pulldown-pe	DMIC0_CLK: Digital MIC0 clock output UART2_RxD: UART 2 Receiving data PF07: GPIO group F bit 7.	VDDIO
PCM0_DO PF12	O IO	W16	8mA, pullup-pe	PCM0_DO: PCM 0 data out PF12: GPIO group F bit 12	VDDIO
PCM0_CLK PF13	O IO	T14	8mA, pullup-pe	PCM0_CLK: PCM 0 clock PF13: GPIO group F bit 13	VDDIO
PCM0_SYN PF14	IO IO	V15	8mA, pullup-pe	PCM0_SYN: PCM 0 sync PF14: GPIO group F bit 14	VDDIO
PCM0_DI F15	I IO	V14	8mA, pullup-pe	PCM0_DI: PCM 0 data in F15: GPIO group F bit 15	VDDIO

2.5.5 SMB3/ISP (with input filter)

Table 2-5 SMB3/ISP Pins (2; all GPIO shared: PB7,8)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SMB3_SDA ISP_SDA PB07	IO IO IO	V18	8mA, pullup-pe	SMB3_SDA: SMB 3 serial data ISP_SDA: ISP serial data PB07: GPIO group B bit 7	VDDIO
SMB3_SCK ISP_SCK PB08	O IO IO	V19	8mA, pullup-pe	SMB3_SCK: SMB 3 serial clock ISP_SCK: ISP serial clock PB08: GPIO group B bit 8	VDDIO

2.5.6 UART0(with input filter)

Table 2-6 UART0 Pins (4; all GPIO shared: PF0~3)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART0_RxD PF00	I IO	L19	8mA, pullup-pe	UART0_RxD: UART 0 Receiving data PF00: GPIO group F bit 0	VDDIO
UART0_CTS_ UART4_RxD PF01	I I IO	M21	8mA, pullup-pe,	UART0_CTS_: UART 0 CTS_ input UART4_RxD: UART 4 Receiving data PF01: GPIO group F bit 1	VDDIO
UART0_RTS_ UART4_TxD PF02	O O IO	M22	8mA, pullup-pe,	UART0_RTS_: UART 0 RTS_ output UART4_TxD: UART 2 transmitting data PF02: GPIO group F bit 2	VDDIO
UART0_TxD PF03	O IO	L21	8mA, pullup-pe,	UART0_TxD: UART 0 transmitting data PF03: GPIO group F bit 3	VDDIO

2.5.7 UART1 (DEBUG) (with input filter)

Table 2-7 UART1 Pins (4; all GPIO shared: PD26~29)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART1_RxD PD26	I IO	R7	8mA, pullup-pe	UART1_RxD: UART 1 Receiving data PD26: GPIO group D bit 26	VDDIO2
UART1_CTS_ PD27	I IO	T6	8mA, pullup-pe	UART1_CTS_: UART 1 CTS_ input PD27: GPIO group D bit 27	VDDIO2
UART1_RTS_ PD28	O IO	W4	8mA, pullup-pe, **rst-pe**	UART1_RTS_: UART 1 RTS_ output PD28: GPIO group D bit 28	VDDIO2
UART1_TxD PD29	O IO	U6	8mA, pullup-pe, **rst-pe**	UART1_TxD: UART 1 transmitting data PD29: GPIO group D bit 29	VDDIO2

2.5.8 JTAG/UART3 (DEBUG Used)

Table 2-8 JTAG/UART3 (5, GPIO PA31 are used to control)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
TRST_	I	R13	Schmitt, pull-down	TRST_: JTAG reset	VDDIO
TCK UART3_RTS_	I O	T13	8mA, Schmitt, pulldown-pe, **rst-pe**	TCK: JTAG clock UART3_RTS_: UART 3 RTS_ output	VDDIO
TMS UART3_CTS_	I I	W14	8mA, Schmitt, pullup-pe, **rst-pe**	TMS: JTAG mode select UART3_CTS_: UART 3 CTS_ input	VDDIO
TDI UART3_RxD	I I	V13	8mA, Schmitt, pullup-pe, **rst-pe**	TDI: JTAG serial data input UART3_RxD: UART 3 Receiving data	VDDIO
TDO UART3_TxD	O O	R12	8mA, Schmitt, pullup-pe, **rst-pe**	TDO: JTAG serial data output UART3_TxD: UART 3 transmitting data	VDDIO

2.5.9 SMB0/1

Table 2-9 SMB0/SMB1 Pins (4; all GPIO shared: PD30~31, PE30~31)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SMB0_SDA PD30	IO IO	N20	8mA, pullup-pe	SMB0_SDA: SMB 0 serial data PD30: GPIO group D bit 30	VDDIO
SMB0_SCK PD31	IO IO	M19	8mA, pullup-pe	SMB0_SCK: SMB 0 serial clock PD31: GPIO group D bit 31	VDDIO
SMB1_SDA PE30	IO IO	K18	8mA, pullup-pe	SMB1_SDA: SMB 1 serial data PE30: GPIO group E bit 30	VDDIO
SMB1_SCK PE31	IO IO	K19	8mA, pullup-pe	SMB1_SCK: SMB 1 serial clock PE31: GPIO group E bit 31	VDDIO

2.5.10 MSCx/SSI1

Table 2-10 MSCx/SSI1 (6; all GPIO shared: PE20~23, PE28~29)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC0_CLK MSC1_CLK SSI1_CLK PE28	O O IO IO	V17	8mA, pullup-pe	MSC0_CLK: MSC (MMC/SD) 0 clock output MSC1_CLK: MSC (MMC/SD) 1 clock output SSI1_CLK: SSI 1 clock output PE28: GPIO group E bit 28	VDDIO
MSC0_CMD MSC1_CMD SSI1_CE0_ PE29	IO IO IO IO	T15	8mA, pullup-pe	MSC0_CMD: MSC (MMC/SD) 0 command MSC1_CMD: MSC (MMC/SD) 1 command SSI1_CE0_: SSI 1 chip enable 0 PE29: GPIO group E bit 29	VDDIO
MSC0_D0 MSC1_D0 SSI1_DR PE20	IO IO IO IO	W18	8mA, pullup-pe	MSC0_D0: MSC (MMC/SD) 0 data bit 0 MSC1_D0: MSC (MMC/SD) 1 data bit 0 SSI1_DR: SSI 1 data input PE20: GPIO group E bit 20	VDDIO
MSC0_D1 MSC1_D1 SSI1_DT PE21	IO IO IO IO	U16	8mA, pullup-pe	MSC0_D1: MSC (MMC/SD) 0 data bit 1 MSC1_D1: MSC (MMC/SD) 1 data bit 1 SSI1_DT: SSI 1 data output PE21: GPIO group E bit 21	VDDIO
MSC0_D2 MSC1_D2 SSI1_GPC PE22	IO IO IO IO	T16	8mA, pullup-pe	MSC0_D2: MSC (MMC/SD) 0 data bit 2 MSC1_D2: MSC (MMC/SD) 1 data bit 2 SSI1_GPC: SSI 1 general-purpose control signal PE22: GPIO group E bit 22	VDDIO
MSC0_D3 MSC1_D3 SSI1_CE1_ PE23	IO IO IO IO	R16	8mA, pullup-pe	MSC0_D3: MSC (MMC/SD) 0 data bit 3 MSC1_D3: MSC (MMC/SD) 1 data bit 3 SSI1_CE1_: SSI 1 chip enable 1 PE23: GPIO group E bit 23	VDDIO

2.5.11 PWM/SMB2/I2S

Table 2-11 PWM/SMB2/I2S Pins (4; all GPIO shared: PE0~3)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM0 SMB2_SDA PE00	IO IO	M20	8mA, **pullup-pe**	PWM0: PWM output or pulse input 0 SMB2_SDA: SMB 2 serial data PE00: GPIO group E bit 0.	VDDIO
PWM1 CLK32K PE01	O O IO	R21	8mA, pulldown-pe **rst-pe**	PWM1: PWM 1 output. This PWM can run in sleep mode in RTCLK clock CLK32K: 32768Hz clock output PE01: GPIO group E bit 1.	VDDIO
PWM2 EXCLKO_ PE02	O O IO	P22	8mA, pulldown-pe **rst-pe**	PWM2: PWM 2 output. This PWM can run in sleep mode in RTCLK clock EXCLKO_: output external clock PE02: GPIO group E bit 2. Pull-up not enabled at and after reset	VDDIO
PWM3 SMB2_SCK SYSCLK PE03	IO IO IO IO	N21	8mA, pullup-pe,	PWM3: PWM output or pulse input 3 SMB2_CLK: SMB 2 serial clock SYSCLK: I2S system clock output PE03: GPIO group E bit 5	VDDIO

2.5.12 System

Table 2-12 System Pins (3, all GPIO shared: PD17~19)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PD17	I	N19	8mA,	PD17: GPIO group D bit 17	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
(BOOT_SEL0)	I		pullup-pe	It is taken as BOOT select bit 0 by Boot ROM code	
PD18 (BOOT_SEL1)	I I	T22	8mA, pullup-pe	PD18: GPIO group D bit 18 It is taken as BOOT select bit 1 by Boot ROM code	VDDIO
PD19 (BOOT_SEL2)	I I	P21	8mA, pullup-pe	PD19: GPIO group D bit 19 It is taken as BOOT select bit 2 by Boot ROM code	VDDIO

2.5.13 DMIC/USB OTG Digital

Table 2-13 DMIC/USB OTG Digital Pins (1, all GPIO shared: PE10)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DRV_VBUS DMIC1_IN PE10	O I IO	V12	8mA, **Schmitt, Input filter** pulldown-pe, **rst-pe**	DRVVBUS: USB OTG VBUS driver control signal DMIC1_IN: Digital MIC1 input PE10: GPIO group E bit 10	VDDIO

2.5.14 Digital power/ground

Table 2-14 IO/Core power supplies for BGAs (46)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VDDQ(VDDMEM)	P	G9 G13 G14 H10 H13 J9 J14		VDDMEM: IO digital power for DRAM(No retention part) 1.2V~1.8V	-
VDDQ_A(VDDMEM_A)	P	G10		VDDMEM_A: IO digital power for DRAM(retention part) 1.2V~1.8V	-
VSSQ(VSSMEM)	P	G8 G11 G12 G15 H8 H15 J11 J12		VSSMEM: IO digital ground for DRAM, 0V	-
VDDIO_N	P	H16 J16		VDDIO_N: IO digital power for NAND power domain, 1.8V~3.3V	-
VDDIO	P	N8 N9 N10		VDDIO: IO digital power for none DRAM/NAND(group 1), 1.8~3.3V	-
VDDIO2	P	P7		VDDIO2: IO digital power for none DRAM/NAND(group 2), 1.8~3.3V	
VSS	P	R8 K10 K13 K15 K16 L11 L12 L14 L16 M13 M15 M16 N12 N13 N14 N15		VSS: IO digital gound for none DRAM and CORE digital ground, 0V	-
VDD	P	K7 K8 L9 M7 M8 M10 N11 K16 N16		VDD: CORE digital power, 1.1V	-
VDD_DLL	P	H7 J7		VDD_DLL: DRAM DLL digital power, 1.1V	-

2.5.15 Analog

Table 2-15 Audio CODEC Pins (14)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
AOHPL	AO	V8		AOHPL: Left headphone out	AVD_{CDC}
AOHPR	AO	V9		AOHPR: Right headphone out	AVD_{CDC}
AOLOP	AO	U10		AOLOP: Line out positive	AVD_{CDC}
AOLON	AO	T10		AOLON: Line out negative	AVD_{CDC}
MICBIAS1	AO	U7		MICBIAS1: Microphone bias	AVD_{CDC}
AIP1	AI	V5		AIP1: Single-ended or differential analog input. positive 1	AVD_{CDC}
AIN1	AI	W6		AIN1: Single-ended or differential analog input. negative 1	AVD_{CDC}
AIP2	AI	T7		AIP2: Single-ended analog left channel input.	AVD_{CDC}
VCAP	AO	W8		VCAP: Voltage Reference Output. An 10μF ceramic or tantalum capacitor in parallel with a 0.1μF ceramic capacitor attached from this pin to AVSCDC eliminates the effects of high frequency noise.	AVD_{CDC}
HP_SENSE	AI	U9		HP_SENSE: Sense of headphone jack insertion	AVD_{CDC}
VREFP_CODEC	P	V6		VREFP_CODEC: Internal nLR output	-
AVDCDC	P	V7		AVDCDC: CODEC analog power, 3.3V, internal nLR input.	-
AVSCDC	P	T8		AVSCDC: CODEC analog ground	-
AVSAO_CDC	P	T9		AVSAO_CDC: CODEC analog ground	

Table 2-16 USB 2.0 OTG (8)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
USB_DP0	AIO	W12		USB_DP0: USB OTG data plus	AVDUSB33
USB_DM0	AIO	V11		USB_DM0: USB OTG data minus	AVDUSB33
USB_VBUS	AIO	R10		USB_VBUS: USB 5-V power supply pin for USB OTG. An external charge pump must provide power to this pin	5V
USB_ID	AI	U12		USB_ID: USB mini-receptacle identifier. It differentiates a mini-A from a mini-B plug. If this signal is not used, internal resistance pulls the signal's voltage level to AVDUSB25.	AVDUSB25
USB_TXR_RKL	AIO	U11		USB_TXR_RKL: Transmitter resister tune. It connects to an external resistor of 43.2Ω with 1% tolerance to analog ground, that adjusts the USB 2.0 high-speed source impedance	AVDUSB25
AVDUSB33	P	V10		AVDUSB33: USB analog power.3.3V	-
AVSUSB	P	T11		AVSUSB: USB analog ground.	
AVDUSB25	P	W10		AVDUSB25: USB OTG analog power, 2.5V	-

Table 2-17 MIPI(DSI/CSI) (17)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DSI_CLKP	AIO	U20		Positive DPHY differential clock line transceiver output	DSI_AVDD
DSI_CLKN	AIO	V20		Negative DPHY differential clock line transceiver output	DSI_AVDD

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DSI_CLKP	AIO	U20		Positive DPHY differential clock line transceiver output	DSI_AVDD
DSI_CLKN	AIO	V20		Negative DPHY differential clock line transceiver output	DSI_AVDD
DSI_DATAP0	AIO	T19		Positive DPHY differential data line transceiver output,lane0	DSI_AVDD
DSI_DATAN0	AIO	U19		Negative DPHY differential data line transceiver output,lane0	DSI_AVDD
DSI_DATAP1	AIO	W22		Positive DPHY differential data line transceiver output,lane1	DSI_AVDD
DSI_DATAN1	AIO	W21		Negative DPHY differential data line transceiver output,lane1	DSI_AVDD
DSI_REXT	AIO	V22		External resistor connection(6.04KΩ E96 resistor)	
DSI_AVDD	P	W20		MIPI Analog 2.5V Power supply	
CSI_CLKP	AIO	U21		Positive DPHY differential clock line transceiver input	CSI_AVDD
CSI_CLKN	AIO	V21		Negative DPHY differential clock line transceiver input	CSI_AVDD
CSI_DATAP0	AIO	T20		Positive DPHY differential data line transceiver input,lane0	CSI_AVDD
CSI_DATAN0	AIO	R19		Negative DPHY differential data line transceiver input,lane0	CSI_AVDD
CSI_DATAP1	AIO	N18		Positive DPHY differential data line transceiver input,lane1	CSI_AVDD
CSI_DATAN1	AIO	P19		Negative DPHY differential data line transceiver input,lane1	CSI_AVDD
CSI_REXT	AIO	U22		External resistor connection(6.04KΩ E96 resistor)	
CSI_AVDD	P	T21		MIPI Analog 2.5V Power supply	
MIPI_AVSS	P	T18		MIPI Analog Supply ground return	

Table 2-18 SAR ADC Pins (5)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
ADC_AUX1	AI	V3		ADC_AUX1: ADC general purpose input	AVDSADC
ADC_AUX2	AI	U4		ADC_AUX2: Top sheet connection for 5-wire touch screen or ADC general purpose input	AVDSADC
ADC_VBAT	AI	T4		ADC_VBAT: Battery voltage input with external resistance divider or ADC general purpose input	AVDSADC
AVDSADC	P	V4		AVDSADC: ADC analog power, 3.3 V	-
AVSSADC	P	T5		AVSSADC: ADC analog ground	-

Table 2-19 EFUSE Pins for Two EFUSE (1)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
AVDEFUSE	P	T17		AVDEFUSE: EFUSE programming power, 0V/2.5V	AVEFUSE

Table 2-20 CPM Pins (5)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLK_XI	AI	W2	2~48 MHz Oscillator	EXCLK_XI: OSC input.	VDDIO
EXCLK_XO	AO	W3		EXCLK_XO: OSC output.	VDDIO
PLLVDD11	P	U3		PLLVDD11:PLL power, 1.1V	-
PLLVSS	P	R4		PLLVSS:PLL ground	-
PLLVDD25	P	T3		PLLVDD25: PLL power, 2.5V(When PLL VCO is not larger than 1.6GHz, 1.8V is recommend)	-

Table 2-21 RTC Pins (9, 2 with GPIO input: PA30, PD14)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
RTCLK	AI	W1	32768Hz Oscillator	RTCLK: 32768Hz clock input	VDDRTC33
NC	AO	V1		NC: Not Connect	-
PWRON	O	U1	8mA	PWRON: Power on/off control of main power	VDDRTC33
CLK32K PD14	O IO	N4	8mA, pulldown-pe **rst-pe**	CLK32K: 32768Hz clock output PD14: GPIO group D bit 14. When main power down, this pin is controlled by RTC register.	VDDRTC33
WKUP PA30	I I	T2	Schmitt	WKUP: Wakeup signal after main power down PA30: GPIO group A bit 30, input/interrupt only	VDDRTC33
PPRST_	I	U2	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDDRTC33
TEST_TE	I	N5	Schmitt, pull-down	TEST_TE: Manufacture test enable, program readable	VDDRTC33
VDDRTC33	P	V2		VDDRTC33: 3.3V power for RTC and hibernating mode controlling that never power down(normally you can use 1.8V instead to reduce power consumption)	-
VDDRTC11	P	P4		VDDRTC11: 1.1V power for RTC core that never power down	-

2.5.16 Summary

BGA270 7.7mm x 8.9mm x 0.6mm, 0.4 pitch, 22 x 19 matrix

Blocks	Notes		
	BGA10 x10	**mA**	
DRAM	76		Include VREFmem
Boot & storage	25	8	
LCDC/SLCD/EPD/SMB3/CIM	22	8	PCLK 8mA
PCM0/I2S/DMIC/UART2	6	8	
SMB3/ISP	2	8	
UART0	4	8	
UART1	4	8	

JTAG/UART3	5		
SMB0/SMB1	4	8	
MSC0/MSC1/SSI1	6	8	
PWM/SMB2/I2S	4	8	
BOOT_SEL	3	8	
OTG DRVVBUS	1	8	
CODEC	14		
USB OTG	8		
MIPI(DSI/CSI)	17		
SARADC	5		
EFUSE	1		
OSC + PLL	5		EXCLK/EXCLKo/PLL power
RTC	9		PA30 is only input/int
Core power(VDD)	9		
Ground for core/IO	16		
IO power/ground for DRAM	18		VDDQ(VDDMEM),VDDQ_A(VDDMEM_A),VSSQ(VSSMEM_A),VDD_DLL
IO power for NAND	2		
IO power for other none DRAM	4		
NC	0		
SUM	**270**		

NOTES:

1 The meaning of phases in IO cell characteristics are:

a Bi-dir, Single-end: bi-direction and single-ended DDR IO are used.

b Output, Single-end: output and single-ended DDR IO are used.

c Output, Differential: output and differential signal DDR IO are used.

d Bi-dir, Differential: bi-direction and differential signal DDR IO are used.

e 4mA, 8mA, 16mA out: The IO cell's output driving strength is about 4mA,8mA,16mA.
4/8mA means the IO cell's output driving strength is selected and can be set as 4mA or 8mA.
2/4mA means the IO cell's output driving strength is selected and can be set as 2mA or 4mA.

f Pull-up: The IO cell contains a pull-up resistor.

g Pull-down: The IO cell contains a pull-down resistor.

h Pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register.

i Pulldown-pe: The IO cell contains a pull-down resistor and the pull-down resistor can be enabled or disabled by setting corresponding register.

j rst-pe: these pins are initialed (during reset and after reset) to IO internal pull (up or down) enabled. Otherwise, the pins are initialed to pull disabled

k Schmitt: The IO cell is Schmitt trig input.

l ~SL: The IO cell do not limited slew rate.

2 All GPIO shared pins are reset to GPIO input

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDQ power supplies voltage	-0.5	1.98	V
VDDQ_A power supplies voltage	-0.5	1.98	V
VDDIO power supplies voltage	-0.5	3.6	V
VDDIO2 power supplies voltage	-0.5	3.6	V
VDDIO_N power supplies voltage	-0.5	3.6	V
VDD core power supplies voltage	-0.2	1.21	V
VDD_DLL power supplies voltage	-0.2	1.21	V
VDDPLL11 power supplies voltage	-0.2	1.21	V
VDDPLL25 power supplies voltage	-0.5	2.75	V
AVDEFUSE power supplies voltage	-0.5	2.75	V
VDDRTC33 power supplies voltage	-0.5	3.63	V
VDDRTC11 power supplies voltage	-0.2	1.21	V
AVDUSB25 power supplies voltage	-0.5	2.75	V
AVDUSB33 power supplies voltage	-0.5	3.63	V
AVDSADC power supplies voltage	-0.5	3.63	V
AVDCDC power supplies voltage	-0.5	3.63	V
CSI_AVDD power supplies voltage	-0.5	2.75	V
DSI_AVDD power supplies voltage	-0.5	2.75	V
Input voltage to VDDQ supplied non-supply pins	-0.3	1.98	V
Input voltage to VDDQ_A supplied non-supply pins	-0.3	1.98	V
Input voltage to VDDIO supplied non-supply pins with 5V tolerance	-0.5	6.0	V
Input voltage to VDDIO supplied non-supply pins without 5V tolerance	-0.5	3.6	V
Input voltage to VDDIO2 supplied non-supply pins without 5V tolerance	-0.5	3.6	V
Input voltage to VDDIO_N supplied non-supply pins	-0.5	3.6	V
Input voltage to VDDRTC33 supplied non-supply pins	-0.5	3.6	V
Input voltage to VDDRTC11 supplied non-supply pins	-0.2	1.21	V
Input voltage to AVDCDC supplied non-supply pins	-0.5	3.63	V
Input voltage to AVDUSB25 supplied non-supply pins	-0.5	2.75	V

Input voltage to AVDUSB33 supplied non-supply pins	-0.5	3.63	V
Input voltage to AVDSADC supplied non-supply pins	-0.5	3.63	V
Input voltage to CSI_AVDD supplied non-supply pins	-0.5	2.75	V
Input voltage to DSI_AVDD supplied non-supply pins	-0.5	2.75	V
Output voltage from VDDQ supplied non-supply pins	-0.5	1.98	V
Output voltage from VDDQ_A supplied non-supply pins	-0.5	1.98	V
Output voltage from VDDIO supplied non-supply pins	-0.5	3.6	V
Output voltage from VDDIO2 supplied non-supply pins	-0.5	3.6	V
Output voltage from VDDIO_N supplied non-supply pins	-0.5	3.6	V
Output voltage from VDDRTC33 supplied non-supply pins	-0.5	3.6	V
Output voltage from VDDRTC11 supplied non-supply pins	-0.2	1.21	V
Output voltage from AVDUSB25 supplied non-supply pins	-0.5	2.75	V
Output voltage from AVDUSB33 supplied non-supply pins	-0.5	3.6	V
Output voltage from AVDSADC supplied non-supply pins	-0.5	2.75	V
Output voltage from AVDCDC supplied non-supply pins	-0.5	3.63	V
Output voltage from CSI_AVDD supplied non-supply pins	-0.5	2.75	V
Output voltage from DSI_AVDD supplied non-supply pins	-0.5	2.75	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
VMEM	VDDQ/VDDQ_A voltage for LPDDR2	1.08	1.2	1.32	V
	VDDQ/VDDQ_A voltage for LPDDR	1.65	1.8	1.95	V
	VDDQ/VDDQ_A voltage for SSTL18 (DDR2)	1.7	1.8	1.9	V
	VDDQ/VDDQ_A voltage for DDR3	1.425	1.5	1.575	V
	VDDQ/VDDQ_A voltage for DDR3L	1.28	1.35	1.45	V
VIO(1.8V)	VDDIO voltage, use as 1.8V	1.62	1.8	1.98	V
VIO2(1.8V)	VDDIO2 voltage, use as 1.8V	1.62	1.8	1.98	V
VION(1.8V)	VDDIO_N voltage, use as 1.8V	1.62	1.8	1.98	V
VIO(2.5V)	VDDIO voltage, use as 2.5V	2.25	2.5	2.75	V
VIO2(2.5V)	VDDIO2 voltage, use as 2.5V	2.25	2.5	2.75	V
VION(2.5V)	VDDIO_N voltage, use as 2.5V	2.25	2.5	2.75	V
VIO(3.3V)	VDDIO voltage, use as 3.3V	2.97	3.3	3.63	V
VIO2(3.3V)	VDDIO2 voltage, use as 3.3V	2.97	3.3	3.63	V
VION(3.3V)	VDDIO_N voltage, use as 3.3V	2.97	3.3	3.63	V
VCORE	VDD core voltage	0.99	1.1	1.21	V

VPLL11	AVDPLL 1.1v analog voltage	0.99	1.1	1.21	V
VPLL25	AVDPLL 2.5v analog voltage, PLL's VCO can achieve 2.0GHz	2.25	2.5	2.75	V
VPLL25(1.8v)	AVDPLL 2.5v analog voltage(Connect to 1.8V), PLL's VCO can achieve 1.6GHz	1.62	1.8	1.98	V
VDLL	VDD_DLL voltage	0.99	1.1	1.21	V
VEFUSE	AVDEFUSE voltage	2.25	2.5	2.75	V
VRTC33	VDDRTC33 voltage	1.8	1.8	3.63	V
VRTC11	VDDRTC11 voltage	0.99	1.1	1.21	V
VUSB25	AVDUSB25 voltage	2.25	2.5	2.75	V
VUSB33	AVDUSB33 voltage	3.0	3.3	3.6	V
VADC	AVDSADC voltage	3.0	3.3	3.6	V
VCDC	AVDCDC voltage	2.97	3.3	3.63	V
VCSI	CSI_AVDD voltage	2.25	2.5	2.75	V
VDSI	DSI_AVDD voltage	2.25	2.5	2.75	V

Table 3-3 Recommended operating conditions for VDDQ/VDDQ_A supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
VI18	Input voltage for DDR2/LPDDR applications	0		1.9	V
VO18	Output voltage for DDR2/LPDDR applications	0		1.9	V
VI15	Input voltage for DDR3 application	0		1.575	V
VO15	Output voltage for DDR3 application	0		1.575	V
VI135	Input voltage for DDR3L application	0		1.45	V
VO135	Output voltage for DDR3L application	0		1.45	V
VI125	Input voltage for DDR3U application	0		1.31	V
VO125	Output voltage for DDR3U application	0		1.31	V
VI12	Input voltage for LPDDR2 application	0		1.3	V
VO12	Output voltage for LPDDR2 application	0		1.3	V

Table 3-4 Recommended operating conditions for VDDIO/VDDIO2//VDDIO_N/VDDRTC33 supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH18}	Input high voltage for 1.8V I/O application	1.17		3.6	V
V_{IL18}	Input low voltage for 1.8V I/O application	–0.3		0.63	V
V_{IH25}	Input high voltage for 2.5V I/O application	1.7		3.6	V
V_{IL25}	Input low voltage for 2.5V I/O application	–0.3		0.7	V
V_{IH33}	Input high voltage for 3.3V I/O application	2		3.6	V
V_{IL33}	Input low voltage for 3.3V I/O application	–0.3		0.8	V

Table 3-5 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	–20		85	°C

Table 3-6 Recommended operating conditions for ADC pins

Symbol	Description	Min	Typical	Max	Unit
Vbat	VBAT input voltage range	0		1.15	V
V_{IADC}	ADC_XP/ADC_XM/ADC_YP/ADC_YM/ADC_AUX1/ADC_AUX2 input voltage range	0		AVDS ADC	V

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-7 DC characteristics for V_{REFMEM} and V_{TT}

Symbol	Parameter	Min	Typical	Max	Unit
VREFM	Reference voltage supply	0.49	0.5	0.51	VMEM
VTT	Terminal Voltage	VREFM – 0.4	VREFM	VREFM + 0.4	V

Table 3-8 DC characteristics for VDDmem supplied pins in DDR3 application

Symbol	Parameter	Min	Typical	Max	Unit
VIH(DC)	DC input voltage High	VREFMEM + 0.1		VMEM	V
VIL(DC)	DC input voltage Low	-0.3		VMEM -0.1	V
VOH	DC output logic High	0.8 * VMEM			V
VOL	DC output logic LOW			0.2 * VMEM	V
RTT	Input termination resistance (ODT) to VMEM/2	100 54 36	120 60 40	140 66 44	Ω
IOHL(DC)	PAD pin, 34Ω Output source/sink DC current, RTT=120		5.07	5.48	mA
IOHL(DC)	PAD pin, 34Ω Output source/sink DC current, RTT=60		8.45	9.28	mA
IOHL(DC)	PAD pin, 34Ω Output source/sink DC current, RTT=40		10.80	11.97	mA

IOHL(DC)	PAD pin, 50Ω Output source/sink DC current, RTT=120		4.53	5.13	mA
IOHL(DC)	PAD pin, 50Ω Output source/sink DC current, RTT=60		6.97	8.24	mA
IOHL(DC)	PAD pin, 50Ω Output source/sink DC current, RTT=40		8.42	10.21	mA
IMEM	VMEM standby current; ODT OFF		0.02	14.47	uA
IMEM	Output Low Drv/RTT=34/60, IMEM DC current		9.49	10.68	mA
IMEM	Output High Drv/RTT=34/60, IMEM DC current		0.74	1.31	mA
IMEM	Input Low ODT/Drv=60/34, IMEM DC current		6.51	7.65	mA
IMEM	Input High ODT/Drv=60/34, IMEM DC current		12.45	15.31	mA
ILS	Input leakage current, SSTL mode, un-terminated		0.02	5.06	uA

Table 3-9 DC characteristics for VDDmem supplied pins in DDR3L application

Symbol	Parameter	Min	Typical	Max	Unit
VIH(DC)	DC input voltage High	VREF + 0.09		VMEM	V
VIL(DC)	DC input voltage Low	-0.3		VREF -0.09	V
VOH	DC output logic High	0.8 * VMEM			V
VOL	DC output logic Low			0.2 * VMEM	V
RTT	Input termination resistance (ODT) to VMEM/2	100 54 36	120 60 40	140 66 44	ohm
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=120		4.55	4.99	mA
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=60		7.58	8.36	mA
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=40		9.66	10.70	mA
IOHL(DC)	PAD pin, 50-ohm Output		4.17	4.65	mA

	source/sink DC current, RTT=120				
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=60		6.50	7.37	mA
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=40		7.93	9.05	mA
IMEM	VMEM standby current; ODT OFF		0.02	13.48	uA
IMEM	Output Low Drv/RTT=34/60, IMEM DC current		8.25	9.40	mA
IMEM	Output High Drv/RTT=34/60, IMEM DC current		0.48	1.02	mA
IMEM	Input Low ODT/Drv=60/34, IMEM DC current		5.41	6.35	mA
IMEM	Input High ODT/Drv=60/34, IMEM DC current		11.29	13.28	mA
ILS	Input leakage current, SSTL mode, un-terminated		0.01	4.80	uA

Table 3-10 DC characteristics for VDDmem supplied pins in DDR3U application

Symbol	Parameter	Min	Typical	Max	Unit
VIH(DC)	DC input voltage High	VREF + 0.09		VMEM	V
VIL(DC)	DC input voltage Low	-0.3		VREF -0.09	V
VOH	DC output logic High	0.8 * VMEM			V
VOL	DC output logic Low			0.2 * VMEM	V
RTT	Input termination resistance (ODT) to VMEM/2	100 54 36	120 60 40	140 66 44	ohm
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=120		4.24	4.56	mA
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=60		7.07	7.74	mA
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=40		9.04	9.98	mA
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current,		3.89	4.23	mA

	RTT=120				
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=60		6.09	6.74	mA
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=40		7.44	8.3	mA
IMEM	VMEM standby current; ODT OFF		0.02	12.39	uA
IMEM	Output Low Drv/RTT=34/60, IMEM DC current		7.6	8.42	mA
IMEM	Output High Drv/RTT=34/60, IMEM DC current		0.34	0.78	mA
IMEM	Input Low ODT/Drv=60/34, IMEM DC current		4.34	5.03	mA
IMEM	Input High ODT/Drv=60/34, IMEM DC current		9.38	10.76	mA
ILS	Input leakage current, SSTL mode, un-terminated		0.005	4.53	uA

Table 3-11 DC characteristics for VDDmem supplied pins in DDR2 application

Symbol	Parameter	Min	Typical	Max	Unit
VIH(DC)	DC input voltage High	V_{REF} + 0.125		VMEM+0.3	V
VIL(DC)	DC input voltage Low	-0.3		VREF -0.125	V
VOH	DC output logic High	VMEM-0.28			V
VOL	DC output logic Low			+0.28	V
RTT	Input termination resistance (ODT) to VMEM/2	120 60 40	150 75 50	180 90 60	Ω
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=120		4.24	4.56	mA
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=60		7.07	7.74	mA
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=40		9.04	9.98	mA
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=120		3.89	4.23	mA

IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=60		6.09	6.74	mA
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=40		7.44	8.3	mA
IMEM	VMEM standby current; ODT OFF		0.02	12.39	uA
IMEM	Output Low Drv/RTT=34/60, IMEM DC current		7.6	8.42	mA
IMEM	Output High Drv/RTT=34/60, IMEM DC current		0.34	0.78	mA
IMEM	Input Low ODT/Drv=60/34, IMEM DC current		4.34	5.03	mA
IMEM	Input High ODT/Drv=60/34, IMEM DC current		9.38	10.76	mA
ILS	Input leakage current, SSTL mode, un-terminated		0.005	4.53	uA

Table 3-12 DC characteristics for VDDmem supplied pins in LPDDR application

Symbol	Parameter	Min	Typical	Max	Unit
$V_{IH(DC)}$	Input logic threshold High	0.7* VMEM		VMEM+0.3	V
$V_{IL(DC)}$	Input logic threshold Low	VMEM-0.3		0.3* VMEM	V
VIH(AC)	AC Input logic High	0.8* VMEM		VMEM+0.3	V
VIL(AC)	AC Input logic Low	VMEM-0.3		0.2* VMEM	V
VOH	DC output logic High (IOH=-0.1mA)	0.9*VMEM			V
VOL	DC output logic Low (IOL=0.1mA)			0.1 *VMEM	V
ILL	Input leakage current		0.01	6.45	uA
IMEM	VMEM quiescent current		0.02	15.03	uA

Table 3-13 DC characteristics for VDDmem supplied pins in LPDDR2 application

Symbol	Parameter	Min	Typical	Max	Unit
$V_{IH(DC)}$	DC input voltage High	VREF + 0.13		VMEM	V
$V_{IL(DC)}$	DC input voltage Low	-0.3		VREF- 0.13	V
V_{OH}	DC output logic High	0.9 * VMEM			V
V_{OL}	DC output logic Low			0.1 * VMEM	V
IMEM	VMEM standby current		0.02	12.31	uA

IMEM	Output Low IMEM DC current		0.30	0.79	mA
IMEM	Output High IMEM DC current		0.28	0.76	mA
IMEM	Input Low IMEM DC current		0.30	0.79	mA
IMEM	Input High IMEM DC current		0.28	0.76	mA
ILL	Input leakage current		0.01	4.51	uA

Table 3-14 DC characteristics for VDDIO/VDDIO2/VDDIOn/VDDRTC supplied pins for 1.8V application

Symbol	Parameter		Min	Typical	Max	Unit
V_T	Threshold point		0.77	0.84	0.92	V
V_{T+}	Schmitt trig low to high threshold point		0.99	1.1	1.19	V
V_{T-}	Schmitt trig high to low threshold point		0.62	0.73	0.82	V
V_{TPU}	Threshold point with pull-up resistor enabled		0.77	0.84	0.91	V
V_{TPD}	Threshold point with pull-down resistor enabled		0.77	0.85	0.92	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		0.99	1.1	1.19	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		0.62	0.73	0.81	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		0.99	1.1	1.2	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		0.62	0.73	0.82	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	μA
R_{PU}	Pull-up Resistor		79	129	218	kΩ
R_{PD}	Pull-down Resistor		73	127	233	kΩ
V_{OL}	Output low voltage				0.45	V
V_{OH}	Output high voltage		1.35			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	6.9	12.5	20.1	mA
		16mA	11.5	20.8	33.5	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	4.9	11.6	22.6	mA
		16mA	8.4	19.9	38.8	mA

Table 3-15 DC characteristics for VDDIO/VDDIO2/VDDIOn/VDDRTC supplied pins for 2.5V application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	1.03	1.13	1.23	V

V_{T+}	Schmitt trig low to high threshold point		1.32	1.45	1.56	V
V_{T-}	Schmitt trig high to low threshold point		0.92	1.01	1.12	V
V_{TPU}	Threshold point with pull-up resistor enabled		1.03	1.13	1.23	V
V_{TPD}	Threshold point with pull-down resistor enabled		1.05	1.14	1.23	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		1.32	1.45	1.55	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		0.91	1	1.12	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		1.33	1.46	1.56	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		0.92	1.01	1.13	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	μA
R_{PU}	Pull-up Resistor		53	82	132	kΩ
R_{PD}	Pull-down Resistor		51	82	143	kΩ
V_{OL}	Output low voltage				0.7	V
V_{OH}	Output high voltage		1.7			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	15.1	25.3	37.3	mA
		16mA	25.1	42.2	62.2	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	13.3	26.6	46.4	mA
		16mA	22.8	45.7	79.6	mA

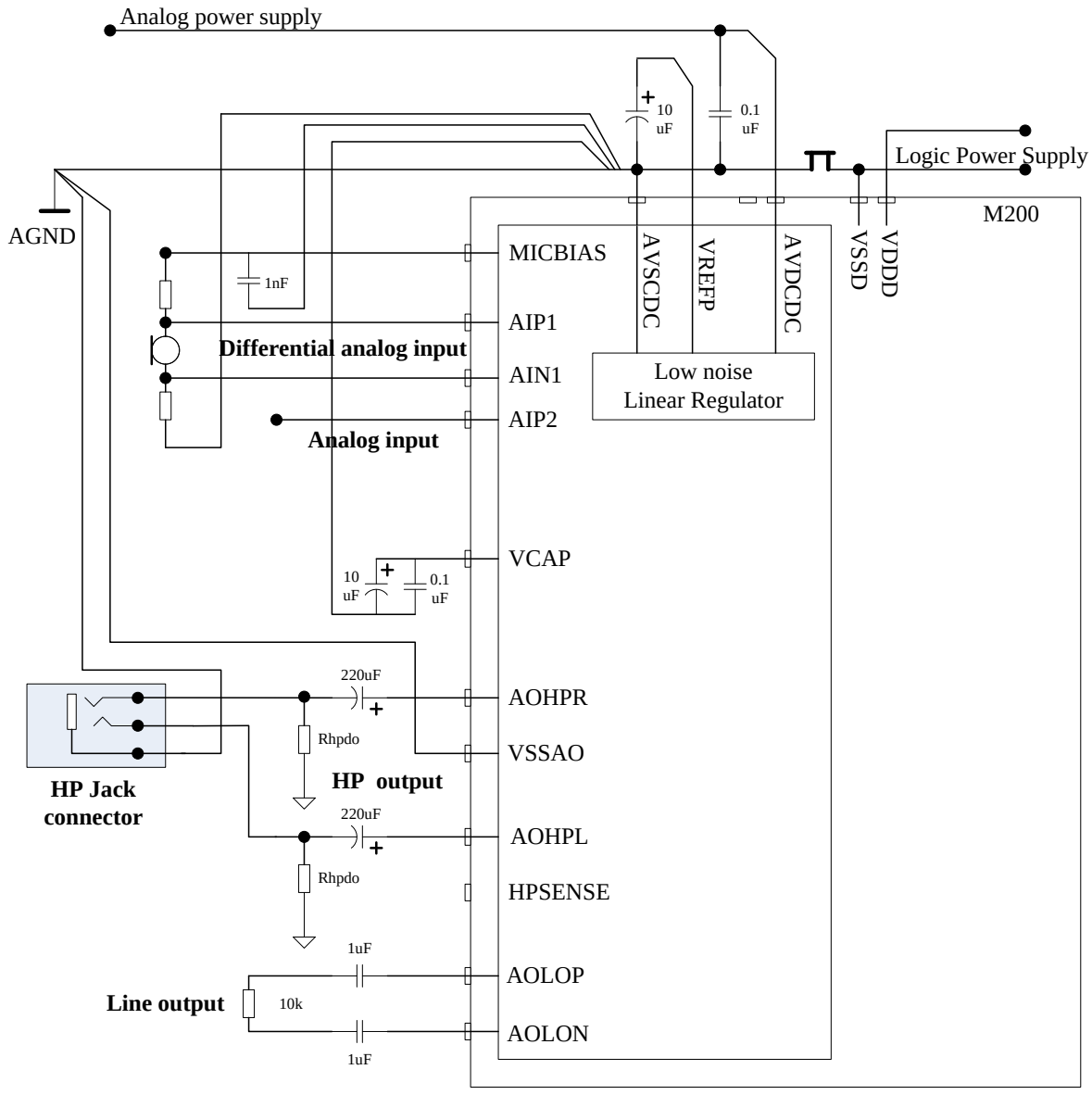
Table 3-16 DC characteristics for VDDIO/VDDIO2/VDDIOn/VDDRTC supplied pins for 3.3V application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	1.34	1.46	1.6	V
V_{T+}	Schmitt trig low to high threshold point	1.69	1.83	1.96	V
V_{T-}	Schmitt trig high to low threshold point	1.21	1.32	1.46	V
V_{TPU}	Threshold point with pull-up resistor enabled	1.33	1.44	1.59	V
V_{TPD}	Threshold point with pull-down resistor enabled	1.36	1.47	1.6	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled	1.69	1.82	1.94	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled	1.2	1.31	1.45	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled	1.71	1.84	1.97	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled	1.23	1.33	1.46	V
I_L	Input Leakage Current @ V_I=1.8V or 0V			±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V			±10	μA

R_{PU}	Pull-up Resistor		41	60	92	kΩ
R_{PD}	Pull-down Resistor		43	64	104	kΩ
V_{OL}	Output low voltage				0.4	V
V_{OH}	Output high voltage		2.4			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	13.1	20.2	27.4	mA
		16mA	21.9	33.8	45.7	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	19.3	38.2	64.5	mA
		16mA	33.1	65.4	110.5	mA

3.4 Audio codec

3.4.1 Application schematic



Note: 1. The Rhpdo value is 470 Ohm, it use to prevent pop-up noise.

2. The single-ended/differential input port AIP1/AIN1 and single-ended input port AIP2/AIP3 can be configure to microphone input or line input by software.

3. VCAP/AVDCDC each of them requires connecting decoupling capacitors (0.1uF) between the pads VCAP/AVDCDC and AVSCDC. This ceramic capacitor has to be kept as close as possible to IC package (closer than 0.2 inch)

3.4.2 Line input to audio ADC path

Measurement conditions:
T = 25°C, AVDCDC = 3.3 V, input sine wave with a frequency of 1 kHz, Fmclk = 12 MHz, Fs = 8 to 96 kHz, measurement bandwidth 20 Hz – 20 kHz, unless otherwise specified.

Parameter	Test conditions	Min.	Typ	Max.	Unit
Input level	Full Scale, Gain GIDL, GIDR = 0dB (note 1)	1.89	2.12	2.39	Vpp
	Full Scale, Gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 20 dB	0.189	0.212	0.239	
SNR	A-weighted, 1 kHz sine wave @ Full Scale and gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 0 dB	85	90		dB
	A-weighted, 1 kHz sine wave @ Full Scale and gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 20 dB	75	80		dB
THD	1 kHz sine wave @ Full Scale -1 dB and gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 0 dB		-80	-70	dB
	1 kHz sine wave @ Full Scale -1 dB and gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 20 dB		-70	-60	dB
Dynamic range	A-weighted, 1 kHz sine wave @ Full Scale -60 dB and gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 0 dB (note 1)	85	90		dB
	A-weighted, 1 kHz sine wave @ Full Scale -60 dB and gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 20 dB (note 1)	75	80		dB
PSRR	100 mVpp 1 kHz sine wave is applied to AVD, input data is 0 and gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 20 dB		90		dB

Gain boost accuracy	GIM1, GIM2 @1 kHz	-1		+1	dB
Input resistance	Boost gain GIM1, GIM2 = 0 dB	63	80	96	kOhm
	Boost gain GIM1, GIM2 = 20 dB	10	12.5	15	
Input capacitance	Includes 10pF for ESD, bonding and package pins capacitances			25	pF
Input bypass capacitor	Input capacitance		1		uF

Note 1: The specified value is extrapolated by adding 60 dB to the measured SNR.

Note 2: The Full Scale input voltage scales with LDO output: VREFP.

3.4.3 Audio DAC to headphone output path

Measurement conditions: T = 25°C, AVDCDC = 3.3 V, input sine wave with a frequency of 1 kHz, Fmclk = 12 MHz, Fs = 8 to 96 kHz, measurement bandwidth 20 Hz – 20 kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Output level (3)	Full Scale, Gain GOL, GOR = 0 dB, GODL, GODR = 0 dB, 10 kOhm load	1.89	2.12	2.39	Vpp
	Full Scale, Gain GOL, GOR = -3 dB, GODL, GODR = 0 dB, 16 Ohm load	1.33	1.5	1.69	Vpp
Maximum output power	Rl = 16 Ohm		17.6		mW
SNR	A-weighted, 1 kHz sine wave @ Full Scale, Gain GOL, GOR = 0 dB, GODL, GODR = 0 dB, 10 kOhm load	95	100		dB
Idle Noise	A-weighted with no signal and gain GOL, GOR= -10 dB, GODL, GODR = 0 dB, 16 Ohm load		-103	-98	dBV
THD, THD+N	1 kHz sine wave @ Full Scale -1 dB, GOL, GOR = 0 dB, GODL, GODR = 0 dB, 10 kOhm load		-85	-75	dB
	1 kHz sine wave @ Full Scale -1 dB and gain GOL, GOR = -3 dB, GODL, GODR = 0 dB, 16 Ohm load		-70	-65	dB
Dynamic range	A-weighted, 1 kHz sine wave @ Full Scale -60 dB, Gain GOL, GOR = 0 dB, GODL, GODR = 0 dB, 10 kOhm load (note 1)	95	100		dB
Wide Band Noise	1 kHz sine wave @ Full Scale and gain		65		dB

	GOL, GOR = 0 dB, GODL, GODR = 0 dB, 10 kOhm load, measurement bandwidth 20 kHz – 100 kHz				
PSRR	100 mVpp 1 kHz sine wave is applied to AVD, input data is 0 and gain GOL, GOR = 0 dB, GODL, GODR = 0 dB, 10 kOhm load		90		dB
	100 mVpp 1 kHz sine wave is applied to AVD, input data is 0 and gain GOL, GOR = -25 dB, GODL, GODR = 0 dB, 16 Ohm load		90		dB
PuN	Active <-> inactive, 10 kOhm load		-60		dBVp
	Active <-> inactive, 16 Ohm load		-60		dBVp
Output resistance	Rl	16			Ohm
Output bypass capacitor	Cl (Rl = 10 kOhm)			1	uF
	Cl (Rl = 16 Ohm)			220	uF

Note 1: The specified value is extrapolated by adding 60 dB to the measured SNR with a FS-60 dB input signal.

Note 2: Output may oscillate above specified load capacitances. The capacitance is equivalent to a 2-meter cable.

Note 3: The Full Scale input voltage scales with the nLR output: VREFP.

3.4.4 Audio DAC to mono line output path

Measurement conditions:
T = 25°C, AVD = 3.3 V, input sine wave with a frequency of 1 kHz, Fmclk = 12 MHz, Fs = 8 to 96 kHz, measurement bandwidth 20 Hz – 20 kHz, unless otherwise specified.

Parameter	Test conditions	Min.	Typ	Max.	Unit
Output level (2)	Full Scale, Gain GODL, GODR = 0 dB	3.78	4.25	4.78	Vpp
SNR	A-weighted, 1 kHz sine wave @ Full Scale, Gain GODL, GODR = 0 dB	90	95		dB
THD+N	1 kHz sine wave @ Full Scale -1 dB, Gain GODL, GODR = 0 dB		-85	-75	dB
Dynamic range	A-weighted, 1 kHz sine wave @ Full Scale – 60 dB, Gain GODL, GODR = 0 dB (note 1)	90	95		dB
PSRR	100 mVpp 1 kHz sine wave is applied to AVD, Gain GODL, GODR = 0 dB, input data is 0		90		dB
Output resistance	Rl	10			kOhm

Output capacitance	Cp			100	pF

Note 1: The specified value is extrapolated by adding 60 dB to the measured SNR.

Note 2: The Full Scale input voltage scales with the nLR output: VREFP.

3.4.5 Line input to headphone output path (analog bypass)

Measurement conditions:
T = 25°C, AVDCDC = 3.3 V, input sine wave with a frequency of 1 kHz, Fmclk = 12 MHz, Fs = 8 to 96 kHz, measurement bandwidth 20 Hz – 20 kHz, unless otherwise specified.

Parameter	Test conditions	Min.	Typ	Max.	Unit
Input level	Full Scale	1.89	2.12	2.39	Vpp
	Full Scale, Gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 20 dB	0.189	0.212	0.239	
Input resistance		10k			Ohm
Output level (2)	Full Scale, Gain GOL, GOR = 0 dB, GIL, GIR = 0 dB, 10 kOhm load (note 1)	1.89	2.12	2.39	Vpp
	Full Scale, Gain GOL, GOR = -3 dB, GIL, GIR = 0 dB, 16 Ohm load	1.33	1.5	1.69	Vpp
SNR	A-weighted, 1 kHz sine wave @ Full Scale, Gain GOL, GOR = 0 dB, GIL, GIR = 0 dB	95	100		dB
THD, THD+N	1 kHz sine wave @ Full Scale -1 dB, Gain GOL, GOR = 0 dB, GIL, GIR = 0 dB, 10 kOhm load		-85	-75	dB
	1 kHz sine wave @ Full Scale -1 dB and gain GOL, GOR = -3 dB, GIL, GIR = 0 dB, 16 Ohm load		-70	-65	dB
Dynamic range	A-weighted, 1 kHz sine wave @ Full Scale -60 dB, Gain GOL, GOR = 0 dB, GIL, GIR = 0 dB, 10 kOhm load (note 1)	95	100		dB
PSRR	100 mVpp 1 kHz sine wave is applied to AVD, input data is 0 and gain GOL, GOR = 0 dB, GIL, GIR = 0 dB, 10 kOhm load		90		dB
	100 mVpp 1 kHz sine wave is applied to AVD, input data is 0 and gain GOL, GOR = -25 dB, GIL, GIR = 0 dB, 16 Ohm load		90		dB
PuN	Active <-> inactive, 10 kOhm load		-60		dBVp
	Active <-> inactive, 16 Ohm load		-60		dBVp
Output resistance	Rl	16			Ohm

Gain accuracy	GIL, GIR @1 kHz	-0.5		+0.5	dB
Input capacitance	Includes 10 pF for ESD, bonding and package pins capacitances			25	pF
Input bypass capacitor	Cbyline		1		uF
Polarity	AIL,R to AOL,R		+1		

Note 1: The specified value is extrapolated by adding 60 dB to the measured SNR.
Note 2: The Full Scale input voltage scales with the nLR output: VREFP.

3.4.6 Micbias and reference

Measurement conditions: T = 25°C, AVDCDC=3.3 V, input sine wave with a frequency of 1 kHz, Fmclk = 12 MHz, Fs = 8 to 96 kHz, measurement bandwidth 20 Hz – 20 kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Micbias output level		2.35	2.5	2.65	V
Micbias output current				4	mA
Micbias output noise	A-weighted		30	40	uVrms
Micbias decoupling capacitor	Cmic	0.75	1	1.25	nF
VCAP voltage			2		V
VREFP		2.35	2.5	2.65	V

3.5 Power On, Reset and BOOT

3.5.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the M200 processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1 shows this sequence and Table 3-17 gives the timing parameters. Following are the name of the power.

- VDDRTC: VDDRTC11 VDDRTC33,(VDDRTC11 can be slightly earlier than VDDRTC33)
- AVDAUD: AVDCDC
- VDD: all 1.1V power supplies, include VDDCORE, PLLVDD11, VDD_DLL
- VDDIO: all other digital IO, include DDR power supplies: VDDQ, VDDQ_A, VDDIO, VDDIO2, VDDIO_N, PLLVDD25
- AVD: all other analog power supplies: AVDSADC, AVDUSB25, AVDUSB33, DSI_AVDD, CSI_AVDD
- AVDEFUSE

Table 3-17 Power-On Timing Parameters

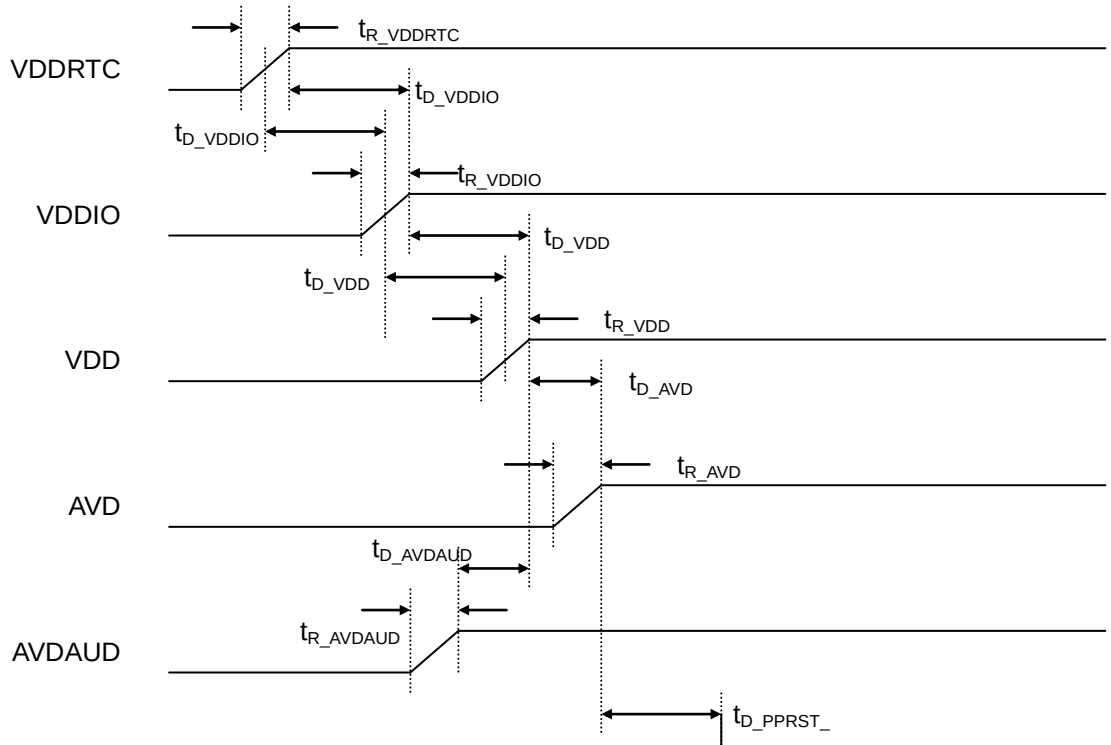
Symbol	Parameter	Min	Max	Unit
t_{R_VDDRTC}	VDDRTC rise time[1]	0	5	ms
t_{R_VDDIO}	VDD rise time[1]	0	5	ms
t_{D_VDDIO}	Delay between VDDRTC arriving 50% (or 90%) to VDD arriving 50% (or 90%)	0	–	ms
t_{R_VDD}	VDD rise time[1]	0	5	ms
t_{D_VDD}	Delay between VDDIO arriving 50% (or 90%) to VDD arriving 50% (or 90%)	0	1	ms
t_{R_AVDAUD}	AVDAUD rise time[1]	0	5	ms
t_{D_AVDAUD}	Delay between AVDAUD arriving 90% to VDD arriving 90%	0.01	1	ms
t_{R_AVD}	AVD rise time[1]	0	5	ms
t_{D_AVD}	Delay between VDDIO arriving 90% to AVD arriving 90%	0	1	ms
$t_{D\_PPRST\_}$	Delay between AVD stable and PPRST_ deasserted	TBD[3]	–	ms[2]
$t_{D\_VPEFUSE}$	Delay between PPRST_ finished and E-fuse programming power apply	0	–	ms

NOTES:

1 The power rise time is defined as 10% to 90%.

2 The PPRST_ must be kept at least 100us. After PPRST_ is deasserted, the corresponding chip reset will be extended at least 40ms.

3 It must make sure the EXCLK is stable and all power(except AVDEFUSE) is stable.



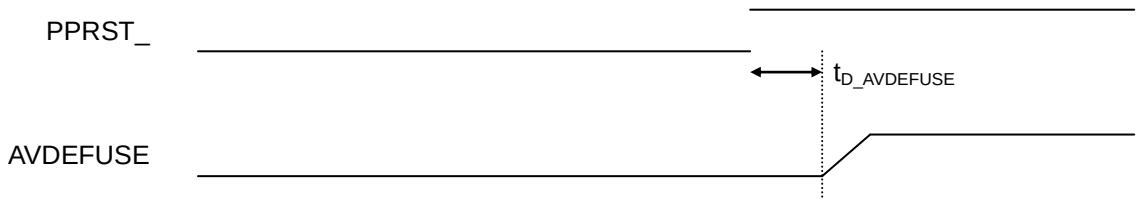


Figure 3-1 Power-On Timing Diagram

3.5.2 Reset procedure

There 3 reset sources: 1 PPRST_ pin reset; 2 WDT timeout reset; and 3 hibernating reset when exiting hibernating mode. After reset, program start from boot.

1 PPRST_ pin reset.
This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.

2 WDT reset.
This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.

3 Hibernating reset.
This reset happens in case of wakeup the main power from power down. The reset keeps for about 1ms ~ 125ms programable, plus 1M EXCLK cycles, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins are put to GPIO input function and most of their internal pull-up/down resistor are set to on, see “2.5 Pin Descriptions” for details. The PWRON is output 1. The oscillators are on. The USB 2.0 OTG PHY, the audio CODEC DAC/ADC, the SAR-ADCs is put in suspend mode.

3.5.3 BOOT

The boot sequence of the M200 is controlled by boot_sel [2:0] pin values. The following table lists them:

Table 3-18 Boot Configuration of M200

boot_sel[2:0]	Boot method
111	USB boot @ USB 2.0 device, EXTCLK=24MHz
110	NAND boot @ CS1
101	MMC/SD boot @ MSC0 (MMC/SD use GPIO Port A)
100	MMC/SD boot @ MSC1 (MMC/SD use GPIO Port E)
011	eMMC boot @ MSC0 (use GPIO Port A)

001	USB boot @ USB 2.0 device, EXTCLK=26MHz
000	SPI boot @ SPI0/CE0

The boot procedure is showed in the following flow chart:

- In case of NAND/MMC0/SD0/EMMC/ SPI boot, if it fails, enter MSC1 boot.
- In case of NOR/MMC1/SD1 boot, if it fails, enter USB boot.
- In case of USB boot, if wait USB cable insert timeout, restart the boot procedure.
- All the boot model except USB boot, if more than 6 seconds no response, reset will happen.
- If the boot procedure has been repeated more than 3 times, enter hibernating mode.

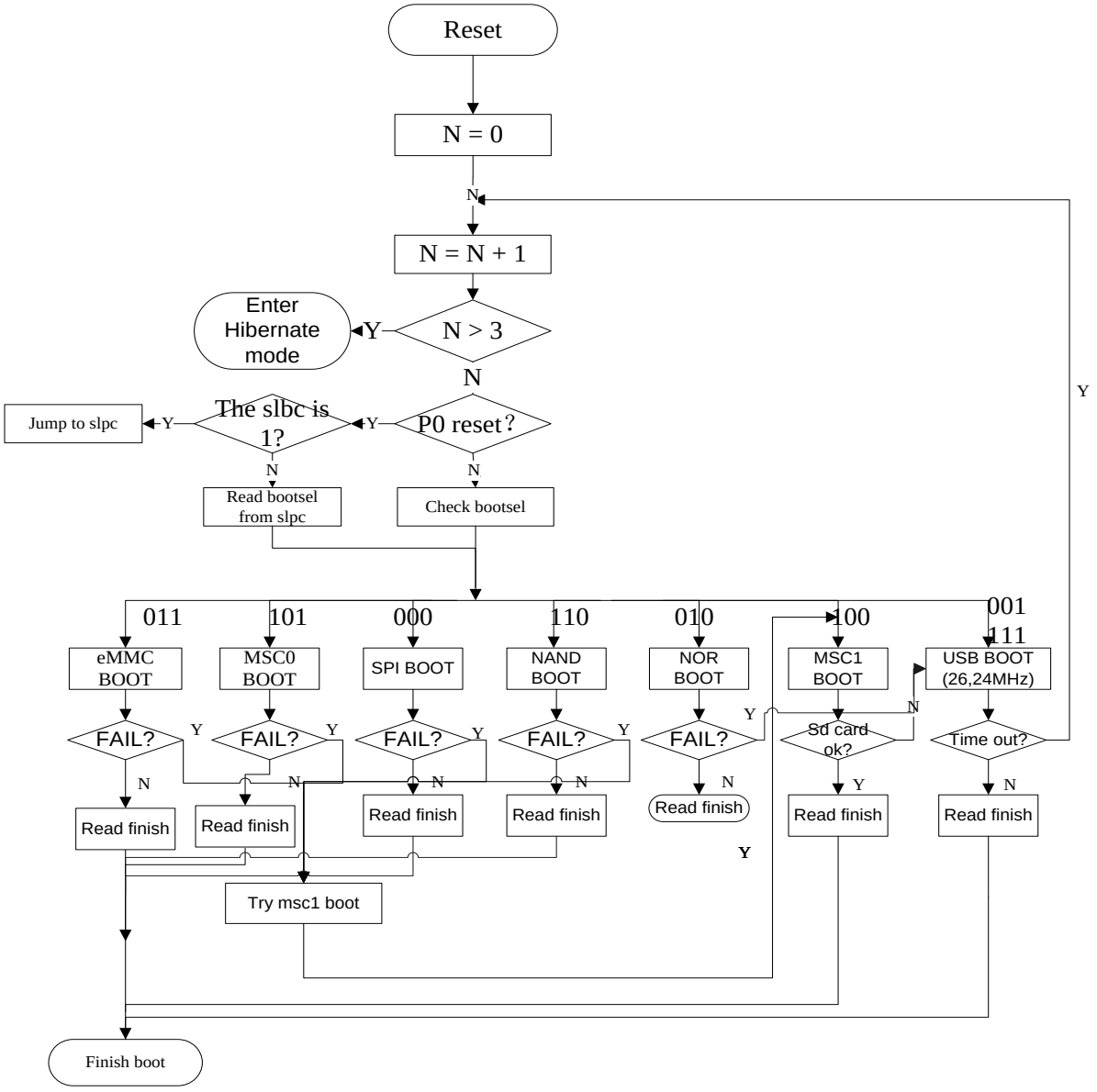


Figure 3-2 Boot flow diagram of M200