Leo Ling

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Professional Experience

Cisco Milpitas, CA

Hardware Engineer, System Application January 2025 – Present

- Created wafer-level electrical validation methodologies for SERDES functional blocks inside high-speed Ethernet PHYs for network ASICs
- Drove methodology development including best practices to handle different system cases for high-speed solutions and platforms utilizing supported PHYs
- Developed automation and analysis tools for lab measurements and data processing in Python and MATLAB
- Supported characterization, validation, compliance, and system integration of SERDES devices and firmware across a wide range of internal and external engineering teams

Intel Hillsboro, OR

Signal Integrity Engineer July 2022 – December 2024

- Measured and modeled high speed digital interfaces (PCIe, ENET) using various test equipment to debug and evaluate signal integrity performance on a system level including PCB and package layout
- Developed MATLAB and python automation for test equipment (VNA, oscilloscope, BERT, etc.) and post-processing to analyze the impact of common impairments (noise, skew, crosstalk, etc.) on high-speed interfaces
- Created methodology for optimizing transceiver equalization (CTLE, FFE, etc.) in the lab leading to significant time savings compared to previous brute force approaches on ENET systems
- Developed scripting around HFSS's python API to automatically generate PCB and package via layouts for signal integrity analysis and optimization
- Adapted machine learning workflows for signal integrity needs by generating behavioral models from HSPICE silicon model using MATLAB

Project Experience

Northwestern University Evanston, IL

Student Researcher October 2018 – June 2022

- Created custom hardware measurement setup to characterize high impedance electronics using pattern generators, digital multimeters, and low noise amplifiers in coordination with Sandia National Labs
- Designed python GUI to automate collection of IV and CV behavior of electronic devices using lab instruments
- Modeled performance of fabricated memristor arrays on machine learning benchmarks

Skills

Programming	MATLAB, Python (Scikit-RF, matplotlib, numpy, pytorch), C/C++, TS/JS, GIT, Linux
Electronics	Cadence Virtuoso, PathWave ADS, Ansys AEDT (HFSS), HSPICE, Verilog-A, EAGLE
Laboratory	Oscilloscope (real time & sampling), TDR, VNA, BERT, PPG, Spectrum Analyzer

Education

Northwestern University, Evanston, IL June 2022

Bachelor of Science in Electrical Engineering cum laude | Minor in Material Science

Northwestern University, Evanston, IL June 2022

Master of Science in Electrical Engineering | BS/MS Program

- Sodium-Doped Titania Self-Rectifying Memristors for Crossbar Array Neuromorphic Architectures (2021)
- Linear and Symmetric Li-Based Composite Memristors for Efficient Supervised Learning (2022)