Design and Simulation of a USB 2.0 Transceiver in System Verilog

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Abstract

USB 2.0 Transceiver Macrocell Interface (UTMI)

1 Technical

1.1 Overview

Hardware & Software

Numerous pieces of software were used to help develop this project, along with mutliple coding languages. The names of the products used, along with their purpose in the project, are listed below.

Type	Name	Purpose
Software	Google Docs	Research/brainstorming
	Figma	Research/brainstorming, and creating diagrams
	Google Slides	Slideshow software that the Final Presentation was created in.
	Visual Studio Code	IDE used for coding the project and writing the final report.
	Github	Project was hosted and shared
	MyFPGA	In web-browser simulation tool for testing System Verilog code
Programming Language	System Verilog	Language that the UTMI was written in
	LaTeX	Final project report (this document) was written in LaTeX

Table 1: Products used to develop the project

Division of Labor

Andrew:

Jiayi:

Leo:

Nhan:

Timeline

Large picture of the timeline to be placed here

1.2 Design

1.3 Simulation

Testing & Benchmarks

Operation Documentation

Expansion/Next Steps

2 Reflection

Learning Outcomes

Helped with system verilog knowledge Helped with reading technical documentation

Preferences

Andrew:

Jiayi:

Leo:

Nhan:

Challenges

Learning complicated concepts.
Doing a larger project in a newly learned language.
Managing the timeline over a long period with other to-dos
Communicating/organizing progress with each other.