

# Design and Simulation of a USB 2.0 Transceiver Macrocell Interface in System Verilog

Andrew Lu, Jiayi Liu, Leo Lesmes, Nhan Do

December 9, 2025

## Abstract

UTMI

## 1 Technical

### 1.1 Project Overview

#### 1.1.1 Hardware & Software

Numerous pieces of software were used to help develop this project, along with multiple coding languages. The names of the products used, along with their purpose in the project, are listed below.

Type	Name	Purpose
Software	Google Docs	Research/brainstorming
	Figma	Research/brainstorming, and creating diagrams
	Google Slides	Slideshow software that the Final Presentation was created in.
	Visual Studio Code	IDE used for coding the project and writing the final report.
	Github	Project was hosted and shared
	MyFPGA	In web-browser simulation tool for testing System Verilog code
Programming Language	System Verilog	Language that the UTMI was written in
	LaTeX	Final project report (this document) was written in LaTeX

Table 1: Products used to develop the project

#### 1.1.2 Division of Labor

**Andrew:**

**Leo:**

**Jiayi:**

Nhan:

1.1.3 Timeline

1.2 Simulating the UTMI

1.2.1 Testing & Benchmarks

1.2.2 Operation Documentation

1.2.3 Expansion/Next Steps

## 2 Reflection

2.1 Learning Outcomes

2.2 Preferences

2.3 Challenges