# Designing a USB 2.0 Transceiver Macrocell Interface in System Verilog

Contributers

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## 1 Technical

### 1.1 Division of Labor

### 1.2 Hardware & Software

### 1.3 Testing & Benchmarks

## 2 Reflection

### 2.1 Learning Outcomes

### 2.2 Preferences

### 2.3 Challenges