

Design and Simulation of a USB 2.0 Transceiver in SystemVerilog

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Abstract

With SystemVerilog code, model a USB 2.0 Transceiver Macrocell Interface (UTMI) that acts as takes in data packets from a Serial Interface Engine (SIE) and outputs. With SystemVerilog code, model a USB 2.0 Transceiver Macrocell Interface (UTMI) that acts as takes in data packets from a Serial Interface Engine (SIE) and outputs . With SystemVerilog code, model a USB 2.0 Transceiver Macrocell Interface (UTMI) that acts as takes in data packets from a Serial Interface Engine (SIE) and outputs . With SystemVerilog code, model a USB 2.0 Transceiver Macrocell Interface (UTMI) that acts as takes in data packets from a Serial Interface Engine (SIE) and outputs . With SystemVerilog code, model a USB 2.0 Transceiver Macrocell Interface (UTMI) that acts as takes in data packets from a Serial Interface Engine (SIE) and outputs . With SystemVerilog code, model a USB 2.0 Transceiver Macrocell Interface (UTMI) that acts as takes in data packets from a Serial Interface Engine (SIE) and outputs .

1 Technical

1.1 Overview

We are designing the part in green, the Low speed

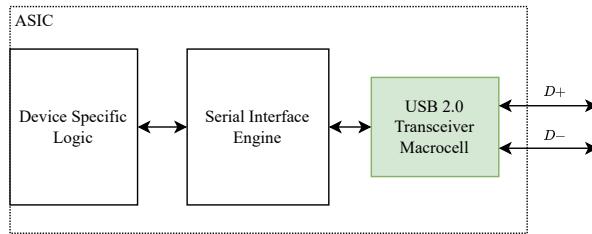


Figure 1: ASIC Functional Blocks

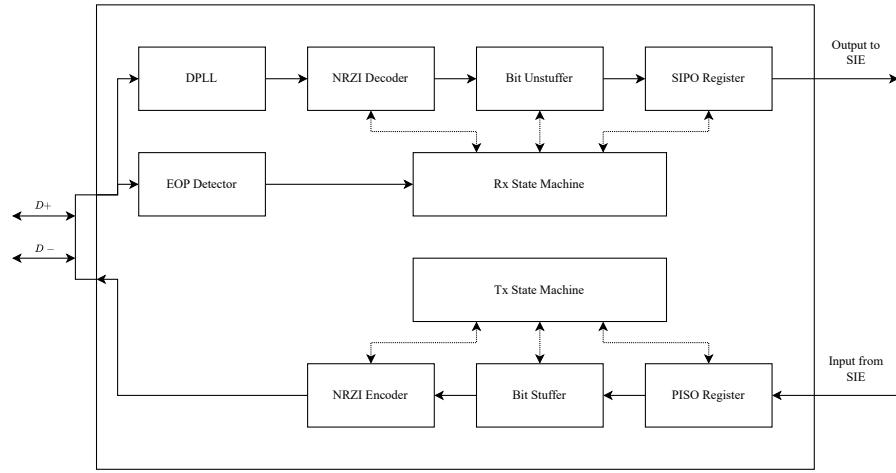


Figure 2: UTMI RTL Diagram

Hardware & Software

Numerous pieces of software were used to help develop this project, along with multiple coding languages. The names of the products used, along with their purpose in the project, are listed below.

Type	Name	Purpose
Software	Google Docs	Research/brainstorming
	Figma	Research/brainstorming, and creating diagrams
	Google Slides	Slideshow software that the Final Presentation was created in.
	Visual Studio Code	IDE used for coding the project and writing the final report.
	Github	Project was hosted and shared
	MyFPGA	In web-browser simulation tool for testing SystemVerilog code
Code Language	SystemVerilog	Language that the UTMI was written in
	LaTeX	Final project report (this document) was written in LaTeX

Table 1: Products used to develop the project

Division of Labor

Everyone: Researched the various aspects of USB 2.0, drew diagrams, debugged and final testing, wrote final presentation, designed final presentation. Presented final presentation to class.

Andrew: Coded the

Jiayi: Coded th

Leo: Coded the . Main person for Final Report and Presentaion.

Nhan: Coded the . Worked to integrate

Timeline

Large picture of the timeline to be placed here

1.2 Design

1.3 Simulation

Testing & Benchmarks

Operation Documentation

Expansion/Next Steps

2 Reflection

Learning Outcomes

Helped with SystemVerilog knowledge Helped with reading technical documentation

Preferences

Andrew:

Jiayi:

Leo:

Nhan:

Challenges

Learning complicated concepts.

Doing a larger project in a newly learned language.

Managing the timeline over a long period with other to-dos

Communicating/organizing progress with each other.